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NASA CR- 160006

(NASA-CR-160006) [RESULTS OF AN ISEE-1 EXPERIMENT TO STUDY THE INTERACTIONS BETWEEN ENERGETIC PARTICLES AND DISCRETE VLF WAVES IN THE MAGNETOSPHERE] Final Report (Stanford Univ.) 241 p HC A11/MF A01 — N80-27421 — Unclas G3/19 25331

FINAL REPORT

on work carried out under

NASA Contract NAS5-20871

STANford UNIV
STANford, CA

April, 1980

I. CONTRACT PURPOSE

The purpose of this contract (NAS5-20871) was twofold: To support the construction of a scientific instrument for the ISEE-1 spacecraft, and to support the analysis and reduction of data obtained by this instrument for a period of two years following launch of the spacecraft.

II. PERIOD OF PERFORMANCE

The period of performance under this contract extended from February 11, 1975 to October 31, 1979.

III. WORK PROVIDED

During the period of performance of this contract, Stanford University provided all materials, services, facilities, and personnel necessary for the design, development, fabrication, testing, checkout and calibration of a scientific instrument for the Study of Interactions in the Magnetosphere between Energetic Particles and Discrete VLF Waves for the International Sun-Earth Explorer Spacecraft A (ISEE-1).

In addition, Stanford University did also analyze and reduce data to a usable format for a period of two years after launch of the Stanford ISEE-1 instrument. This work was performed in strict accordance with contract NAS5-20871 and specifications included and referenced therein.

Since November 1, 1979, further data has been obtained from the Stanford University experiment on ISEE-1 and analysis of existing data continues under a new contract, NAS5-25744.

Upon completion of the Stanford University involvement in the ISEE-1 project, disposition of the Stanford University ISEE-1 data will be made to the National Space Science Data Center (NSSDC). This data will be contained on magnetic tapes in analog form and the data tapes will be the original analog data tapes prepared at NASA telemetry stations during data acquisition on ISEE-1. The format of the analog signal on these magnetic tapes is described in detail in references [1] and [4].

IV. INSTRUMENTATION

The ISEE-1 instrumentation produced by Stanford University under contract NAS5-20871 consisted of a broadband VLF receiver and two instruments for ground support activities, each characterized as a Data Converter/Spacecraft Command Simulator. All instrumentation was produced within budgeted costs and delivered to NASA on time, as specified in the contract.

A complete description of the VLF receiver and ground-support equipment is given in references [1], [2], [3] and [4]. A copy of each of these references is appended to this report.

V. DISPOSITION OF INSTRUMENTATION

The VLF receiver produced under this contract is presently incorporated within the ISEE-1 spacecraft. The ground-support equipment is presently located in Rm 224 of the Electronics Research Laboratories of Stanford University, Stanford, California. The ground-support equipment is routinely used for analysis of the data obtained by the Stanford experiment on ISEE-1.

VI. SCIENCE OBJECTIVES

The main purpose of the Stanford ISEE-1 experiment is to study interactions in the magnetosphere between coherent VLF waves and energetic particles, with the goal of achieving a better understanding of this important aspect of the earth's environment.

A detailed discussion of the scientific objectives of the experiment can be found in reference [4] (appended).

VII. SPACECRAFT INSTRUMENT STATUS

At the present time the analog portion of the Stanford instrument is functioning as designed and is acquiring excellent data concerning the wave spectrum and relative amplitude. The digital portion of the experiment, involving the housekeeping data, has developed a malfunction and is encoding the absolute amplitude of the wave spectrum with a fixed bias of approximately 20 dB. We are presently working with the University of Iowa experimenters in order to recalibrate the housekeeping data and effectively eliminate this bias. Progress to date is promising and we anticipate no serious problems in achieving all objectives of the Stanford experiment.

An investigation is presently underway to attempt to pinpoint the circuit or component whose failure has led to the malfunction of the digital portion of the experiment. Upon completion of this investigation the results will be reported by letter to Dr. Keith Ogilvie, the ISEE-1 Project Scientist.

VIII. HIGHLIGHTS OF EXPERIMENTAL RESULTS

During the two years following launch, the Stanford University Wave-Injection Experiment on ISEE-1 has acquired a solid base of data in a number of areas, notably:

(1) Emission generation by nonducted coherent waves, and

(2) The cold plasma distribution in the inner magnetosphere ($2 < L < 5$).

In each of these areas the ISEE-1 data have led to unexpected findings which appear to have important implications for magnetospheric wave-particle interactions. We discuss these findings below:

1. Emission Generation by Nonducted Coherent Waves.

In general, signals from ground transmitters propagate up to the satellite in a nonducted mode and at any given time there exists more than one magnetospheric path over which the signal may reach the satellite. The time delay difference between the various paths ranges from a few hundred milliseconds up to a few seconds, and the duration of the received signal may exceed that of the transmitted signal by up to a factor of three or more. In general, the larger time delay paths extend out to higher L-shells where the wave normal of the signal is inclined at a larger angle with respect to the static magnetic field direction.

Signals from the Omega, N.D., transmitter have been routinely observed on ISEE-1 over the American longitudinal sector. These signals, nominally one second in length, often have been observed to endure up to three seconds or more. On a number of occasions, signals from Omega, N.D., have been observed to trigger VLF emissions somewhere along their path between the ground and the satellite. In nearly every case triggering took place only along a path of longer time delay and not along the most direct path. This unexpected triggering mode appeared to require no unusual magnetic conditions.

Thus a general condition for nonducted triggering appears to be that triggering occurs on paths which reach out to the relatively higher L-shells than the most direct path. In some cases this condition may result from the possibility that the emission generation process is much more efficient when the ratio of wave frequency to local gyrofrequency approaches the value 1/2. Such an increase in the interaction efficiency has been associated with cases of ducted triggering [5]. Another possibility is that the nonducted triggering mechanism actually favors larger wave normal angles. However, the linear theory of the whistler-mode instability predicts that the growth rate of the instability should actually decrease as the wave normal is increased, due to increased Landau damping [6].

A second interesting feature of the emission events was the occurrence in a number of cases of triggering on magnetic shells near and below L = 2. Triggering on such low L-shells has not previously been reported and apparently involves interactions with quasi-relativistic electrons. Thus our results show that emissions can be generated under much more general conditions than previously believed. Our findings in this area have been reported in recent papers (see Table 1).

2. The Cold Plasma Distribution in the Inner Magnetosphere.

It is generally believed that the cold plasma distribution in the magnetosphere can be represented by a diffusive equilibrium (DE) model inside the plasmasphere ($1.2 \leq L \leq 4$) and a collisionless model outside the plasmapause ($4 < L < 10$) [7]. These models have been generally consistent with both ground-based measurements of ducted whistler time delays [8], and with local satellite measurements of equatorial cold electron densities.

However, in recent years there have been theoretical arguments advanced which indicate that the $L = 3$-4 regions may be a location where some hybrid model may best apply [9]. This view is supported by recent data from the ISEE-1 satellite which indicate that the DE model may break down on L-shells between 3 and 4 and that a collisionless model may better describe the cold plasma distribution in this region.

It has been shown [10] that the time delay of nonducted signals from VLF ground transmitters can be used to determine the cold plasma density along the propagation path between a satellite and the transmitter. Using ISEE-1 time delay measurements of nonducted pulses from the Omega, N.D., transmitter, the cold plasma distribution was calculated for a large number of orbits during the October 1977-October 1979 period on which the ISEE-1 satellite passed over the North American sector. In 70% of these cases it was found that the DE model was not applicable on L-shells greater than 3, and that the inferred distribution fits a collisionless model more closely. A corollary of this finding was the fact that the inferred cold plasma gradients were much larger than those predicted by the DE model and these larger gradients tended to minimize the wave normal angle with respect to the earth's magnetic field.

One possible interpretation of these results is that the distribution of cold plasma outside of ducts differs significantly from that inside ducts and that in the range of L ≈ 3-4 the DE model applies only to ducts. However, additional experimental and theoretical work must be done before these recent results can be interpreted satisfactorily.

Since the cold plasma density and gradients determine the wave phase velocity and wave normal direction that occurs during VLF wave-particle interactions, an accurate description of the cold plasma distribution is necessary for quantitative studies of these interactions. For this reason, increasing our understanding of the quantitative details of the cold plasma distribution in the magnetosphere is an important goal of the Stanford experiment on ISEE.

Results obtained from this study have been reported at scientific conferences and are soon to be submitted for publication (see Table 1). Interesting data have also been obtained on power line radiation in the magnetosphere, as well as the doppler-shift signatures of nonducted coherent VLF waves. Results from these studies have also been reported at scientific conferences and are also soon to be submitted for publication (see Table 1).

In these broad general areas, the ISEE-1 data have led to significant and unexpected findings which have important implications for magnetospheric wave-particle interactions.

IX. REPORTING OF SCIENTIFIC RESULTS

Results of our analysis of the first two years of ISEE-1 data have been reported in a number of papers. A complete list of these papers, current as of April, 1980, is given in Table 1.

Table 1

PAPERS CONCERNING THE STANFORD UNIVERSITY EXPERIMENT ON ISEE-1
(list current as of April 1, 1980)

PUBLICATIONS:

Bell, T. F., and R. A. Helliwell, The Stanford University VLF wave injection experiment on the ISEE-A spacecraft, Geosci. Electr. GE-16, 8248, 1978.

Bell, T. F., U. S. Inan and R. A. Helliwell, ISEE-1 satellite observations of the triggering of VLF emissions by nonducted coherent waves in the magnetosphere, submitted to J. Geophys. Res., 1980.

Bell, T. F., and U. S. Inan, Remote sensing of the magnetospheric cold plasma using VLF data acquired on ISEE-1 spacecraft, in preparation for J. Geophys. Res., 1980.

Bell, T. F., and U. S. Inan, VLF doppler signatures detected on ISEE-1 and the distribution of cold plasma in the magnetosphere, in preparation for J. Geophys. Res., 1980.

Bell, T. F., and U. S. Inan, The characteristics of VLF emissions triggered by nonducted coherent waves, in preparation for J. Geophys. Res., 1980.

Inan, U. S., and T. F. Bell, ISEE-1 satellite observations of signals from the Siple transmitter, Antarctic Journal, December, 1978.

Luette, J. P., T. F. Bell, and R. A. Helliwell, ISEE-1 observations of power line radiation in the magnetosphere, in preparation for J. Geophys. Res., 1980.

PAPERS PRESENTED AT SCIENTIFIC CONFERENCES:

Bell, T. F., U. S. Inan, and R. A. Helliwell, Early results of the Stanford University VLF wave injection experiment in the ISEE-1 satellite, ESLAB Symposium, Innsbruck, Austria, June 1978.

Bell, T. F., and U. S. Inan, Observations on the ISEE-1 satellite of the triggering of VLF emissions by nonducted coherent VLF waves in the magnetosphere, accepted for presentation at URSI General Assembly, Helsinki, Finland, August 1978.

Bell, T. F., U. S. Inan, and R. A. Helliwell, ISEE-1 satellite observations of signals from ground transmitters, AGU Meeting, San Francisco, December 1978.

Bell, T. F., U. S. Inan, and R. A. Helliwell, ISEE-1 observations of VLF emissions triggered by nonducted coherent VLF waves from ground transmitters, IMS Symposium and IAGA Meeting, Melbourne/Canberra, Australia, 1979.

Inan, U. S., and T. F. Bell, The distribution of cold plasma in the inner magnetosphere as deduced from ISEE-1 VLF wave measurements, AGU Meeting, December 1979.

REFERENCES

[1] Develco Report No. 983-761029, "VLF wave injection receiver," Develco, Inc., 404 Tasman Dr., Sunnyvale, CA 94086.

[2] Develco Report No. 983-761208, "Data converter/spacecraft command simulator (106075-01), ground support equipment for the Helliwell VLF wave experiment spacecraft receiver," Develco, Inc., 404 Tasman Dr., Sunnyvale, CA 94086.

[3] Develco Report No. 983-761209, "Data converter (106075-02) ground support equipment for the Helliwell VLF wave experiment spacecraft receiver," Develco, Inc., 404 Tasman Dr., Sunnyvale, CA 94086.

[4] Bell, T. F., and R. A. Helliwell, The Stanford University VLF wave injection experiment on the ISEE-1 spacecraft, Geosci. Electr., GE-16, 248, 1978.

[5] Carpenter, D. L., and S. Lasch, An effect of a transmitter frequency increase on the occurrence of VLF noise triggered near L = 3 in the magnetosphere, J. Geophys. Res., 74, 1859, 1969.

[6] Brinca, A. L., On the stability of obliquely propagating whistlers, J. Geophys. Res., 77, 3495, 1972.

[7] Angerami, J. J., A whistler study of the distribution of thermal electrons in the magnetosphere, Tech. Rept. 3412-7, Radioscience Lab., Stanford Electronics Lab.,

Stanford University, Stanford, CA, May 1966.

[8] Park, C. G., D. L. Carpenter, and D. B. Wiggin, Electron density in the plasmasphere: Whistler data on solar cycle, annual, and diurnal variations, J. Geophys. Res., 83, 3137, 1978.

[9] Park, C. G., and C. I. Meng, After effects of isolated magnetospheric substorm activity on the mid-latitude ionosphere: Localized depressions in F-layer electron densities, J. Geophys. Res., 81, 4571, 1976.

[10] Inan, U. S., T. F. Bell, and R. R. Anderson, Cold plasma diagnostics using satellite measurements of VLF signals from ground transmitters, J. Geophys. Res., 82, 1167, 1977.

APPENDICES

The Stanford University VLF Wave Injection Experiment on the ISEE-A Spacecraft

T. F. BELL AND R. A. HELLIWELL

Abstract—A Stanford University VLF wave injection experiment will be carried out as part of the ISEE mission. This experiment consists essentially of three basic components; a broad-band VLF receiver on ISEE-A, a broad-band VLF transmitter located at Siple Station in the Antarctic, and a number of ground stations in the Antarctic and Canada. This experiment is an outgrowth of VLF wave injection experiments carried out over the past four years using the Stanford University transmitter at Siple Station, Antarctica. The purpose of this experiment is to study VLF-wave–particle interactions in the magnetosphere, with the goal of achieving a better understanding of this important portion of the earth's environment. In the present paper we sketch briefly the scientific background of the experiment and describe the functions of the ISEE-A instrument.

I. Introduction

THE STANFORD University VLF wave injection experiment for the ISEE mission consists essentially of three separate components: 1) a broadband VLF receiver on ISEE-A, 2) a broad-band VLF transmitter located at Siple Station in the Antarctic, 3) ground stations in the Antarctic and Canada.

This experiment is an outgrowth of VLF wave injection experiments carried out over the past four years using the Stanford University broad-band (1-20-kHz) transmitter at Siple Station, Antarctica [2], [5].

The Siple Station wave-injection experiment is an active experiment designed to study VLF-wave–particle interactions in the magnetosphere. One goal of the experiment is to develop a sufficient understanding of the physics of wave–particle interactions to allow the control of the energetic particles by the injected waves.

Once control is established, the energetic particles can then be used as tools to study other important processes. For example, the control of energetic particle precipitation would allow interesting studies of X-ray, ionization and radiation emission processes in the ionosphere. Furthermore, modulation of precipitation flux might provide a means to produce Pc-1 ULF waves [1] on a controlled basis. Numerous other applications can be envisioned.

A second goal of the experiment is to determine the effects upon energetic particles in the magnetosphere of electrical power transmission line radiation.

Harmonics radiated by electrical power distribution systems are frequently observed to enter the magnetosphere where they are amplified to a level that is sufficient to stimulate VLF emissions, scatter energetic electrons and produce strong wave–

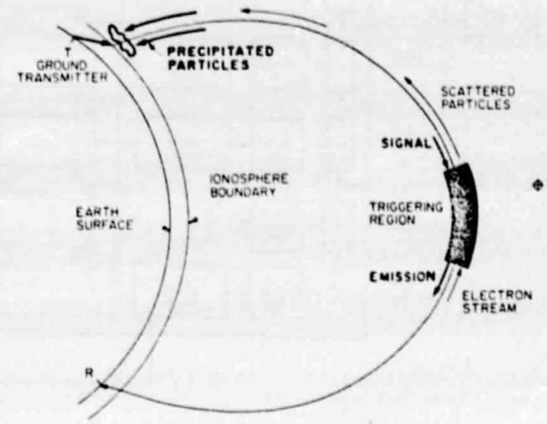

Fig. 1. Schematic representation of the ISEE VLF wave injection experiment (HEM).

wave interactions [3], [4]. In fact, the bulk of the data acquired at ground stations shows evidence of electrical power line radiation that propagates in the whistler mode within the magnetosphere and influences natural wave–particle interactions.

In general, the power line radiation effects are studied through the injection into the magnetosphere by the Siple Station transmitter of wave structures similar in form to those typically generated by electrical power distribution systems. Since these injected waves produce effects similar to those produced by power line radiation, a controlled study of power line radiation effects is possible.

The basic mode of operation of the wave-injection experiment is depicted in Fig. 1. VLF signals from the Siple Station transmitter are radiated from the 21.2-km long antenna and propagate through the ionosphere above the antenna and into the magnetosphere. Once in the magnetosphere the signals follow the Earth's magnetic-field lines until they approach the magnetic equatorial plane, at which point they begin to interact strongly with energetic electrons through gyroresonance. During the interaction the injected wave amplitude may grow as much as 30 dB [6], VLF emissions may be produced, and significant numbers of resonant energetic electrons are pushed into the loss cone. After the interaction the injected waves, plus stimulated emissions, travel along the field lines until they reach the ionosphere above Roberval, the ground station conjugate to Siple Station. At the same time the loss cone particles travel down the magnetic-field lines and precipitate into the atmosphere over Siple Station.

It is clear that there are a number of important questions which cannot be answered using ground data alone.

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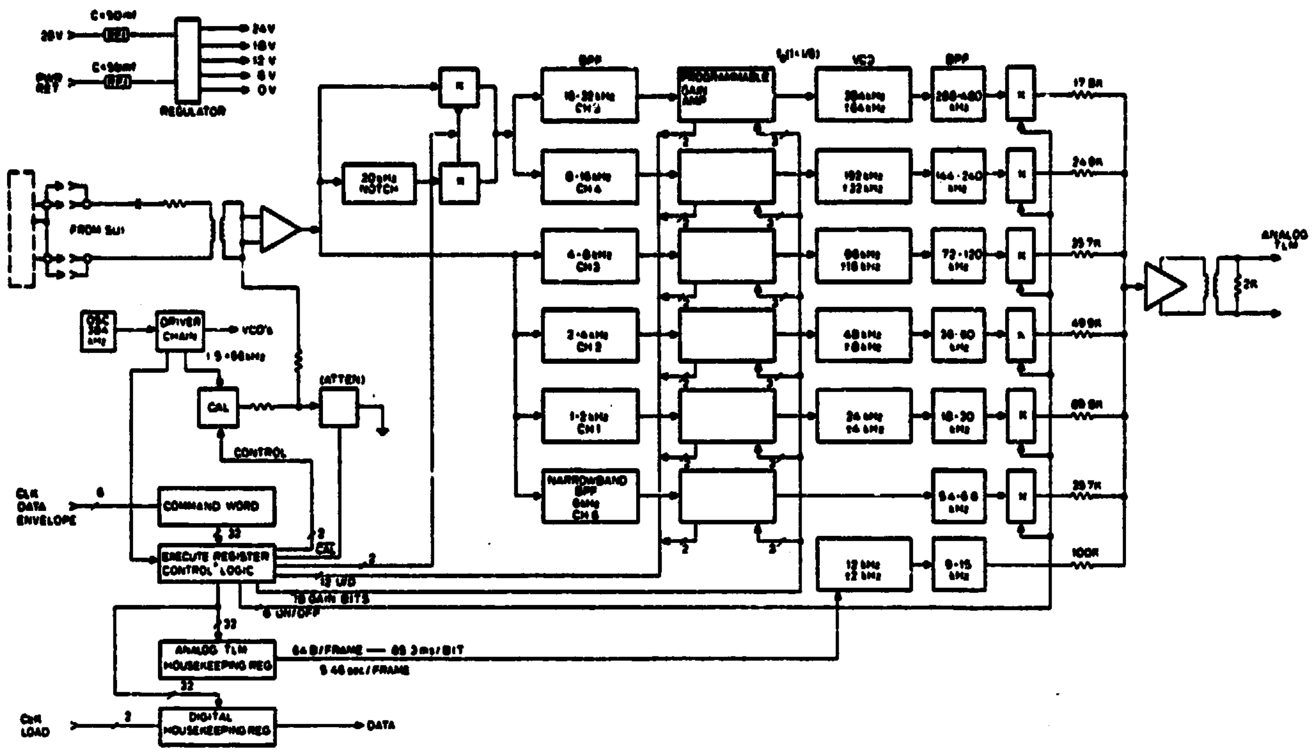

Fig. 2. Block diagram of HEM VLF receiver.

1) Where is the exact location of the interaction region in which VLF emissions are produced and what is the distribution of wave amplitude within this region?

2) What is the magnitude of the energetic particle scattering due to the injected waves and stimulated emissions?

3) What is the relative efficiency of nonducted waves in producing emissions?

All of these questions involve quantities which at our present state of knowledge can only be measured *in situ*, by satellites. Thus an important component of the wave-injection experiment is the measurement by the ISEE satellites of the characteristics of waves and particles in the magnetosphere during the wave-injection process.

The primary wave measurement device during the ISEE wave-injection experiments is the Stanford University multichannel broad-band (1-32 kHz) VLF receiver. This receiver is designed to make rapid and accurate frequency and amplitude measurements of the injected signals as a function of time. Rapid measurements are necessary since the injected waves may grow as much as 30 dB during the initial 100 ms of interaction. A multichannel receiver is necessary since strong natural background noise (10-30 dB above injected signal levels) is a common feature of the wave spectrum in the 1-10 kHz range and this noise will cause suppression of the injected signal in single channel receivers employing automatic gain control (AGC). Energetic particle measurements during the wave-injection experiments will be carried out by the FRM and WIM experiments.

Wave and particle measurements from the ISEE spacecraft should serve to answer the questions posed above and increase our understanding of VLF wave-particle interactions in the magnetosphere.

II. Instrument Description

A. *Theory of Instrument Operation*

The receiver package contains signal filtering, amplification, gain control, switching, calibration, and other functions necessary to transfer the 1- to 32-kHz signal from the preamplifier to the analog telemetry system. The system block diagram in Fig. 2 shows the major receiver functions.

Signals in the 1- to 32-kHz band from the preamplifer (supplied by the University of Iowa) are fed to a parallel bank of six filters. Five of the filters are broad-band octave width filters and one filter is a narrow-band filter centered at 6 kHz, an operating frequency of the Siple transmitter. A 20-kHz notch filter is incorporated into the 8- to 16-kHz and 16- to 32-kHz bandpass filters to minimize interference arising from the spacecraft power converter which operates at 20 kHz.

The outputs of the filters are fed into six programmable gain amplifiers (PGA). The purpose of the variable gain for each band is to maintain output signal levels within the range required by the spacecraft telemetry. The signal level is maintained below telemetry saturation and above telemetry system noise levels. The gain of each channel is adjustable in 10-dB steps over a 0- to 70-dB range by ground command or by automatic signal level sensing. When a ground command for automatic gain is received, the amplitude envelope of signals in each channel is monitored and the gain adjusted to maintain a prescribed level. This adjustment is made in 10-dB increments at intervals of about 5.4 s.

Each signal channel, except for the 6-kHz channel, drives a voltage controlled oscillator (VCO). Normally the output of each VCO and a housekeeping VCO are summed, and the resultant signal used to modulate the analog telemetry trans-

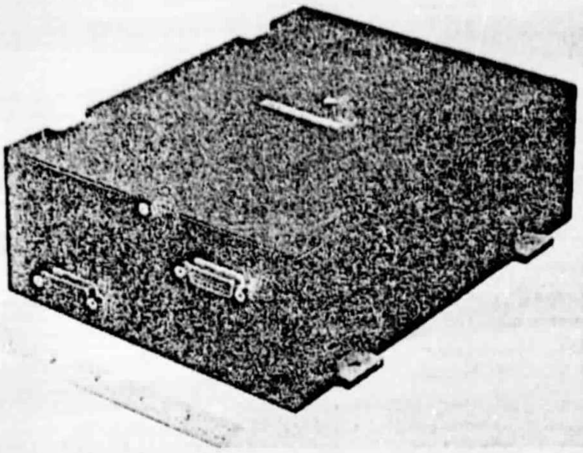

Fig. 3. External physical characteristics of HEM instrument.

mitter. When all channels are summed, the transmission of the VLF data requires a 500-kHz bandwidth analog telemetry link. However, the output of any signal channel can be turned off by ground command. This allows the telemetry power to be concentrated on a desired channel for maximum signal-to-noise ratio.

A relatively narrow-band VCO is provided to generate an FSK signal for housekeeping functions. The PGA gain levels, channel ON/OFF, and AUTO/MAN mode for each channel, and notch filter ON/OFF and CAL ON/OFF data are transmitted over this VCO.

System calibration signals are generated in the receiver package. The amplitude and duration of the CAL signal is sufficient to cause each channel to step from 70- to 0-dB gain over a period of approximately 45 s. Provision to inhibit its operation after a preset length of time is also incorporated into the source as a safety precaution against intermittent operation.

The spacecraft can verify that the experiment has received the proper command word through the digital telemetry link between the experiment and spacecraft controller. Upon request from the spacecraft, a 32-bit telemetry word will be serial shifted from the experiment under spacecraft control.

B. *Power, Weight, and Dimensions*

The instrument requires the following power source:

Voltage: 28-V dc ± 5 percent
Current: 25 mA average, 30 mA peak, 250 mA surge (power up)
Average Power: 0.7 W.

The +28-V dc source is regulated to supply +24, +18, +12, and +6 V.

In order to minimize power consumption, the supply is a totem-pole configuration.

The weight and dimensions of the instrument are as follows:

Weight: 1303 g
Height: 2.75 in
Length: 9.02 in (does not include connector protrusions)
Width: 7.25 in (including mounting feet).

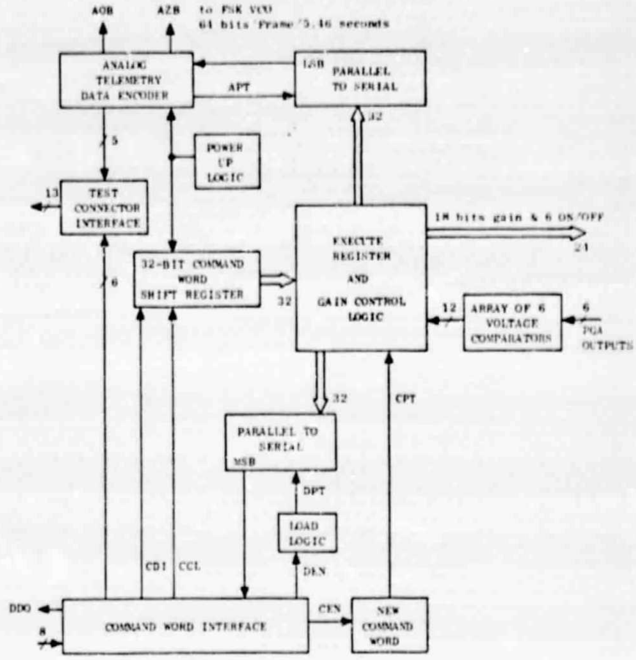

Fig. 4. Block diagram of digital command link circuitry.

TABLE I
GLOSSARY

AOB	Analog Telemetry One Bit
APT	Analog Telemetry Parallel Transfer
AZB	Analog Telemetry Zero Bit
CCL	Command Word Clock
CDI	Command Word Data In
CEN	Command Word Envelope
CPT	Command Word Parallel Transfer
DDO	Digital Telemetry Data Out
DEN	Digital Envelope
DPT	Digital Telemetry Parallel Transfer
LSB	Least Significant Bit
MSB	Most Significant Bit

The external characteristics of the instrument are depicted in Fig. 3.

C. *Circuit Description*

1) Digital Command Link: The digital section of the HEM experiment provides gain control settings to 6 channels of VLF amplifiers, output summing control for 6 VLF amplifier outputs, digital telemetry information to the spacecraft computer, analog telemetry information to the ground, known "power up" status, calibration function, and interfacing for digital signals between the spacecraft and experiment. A block diagram of the digital command link circuitry is shown in Fig. 4. A list of abbreviations used in Fig. 4 is contained in Table I.

The digital electronics operates on a synchronous 5.4-s cycle with the exception of command word and digital telemetry transfers which are under control of the spacecraft computer. The HEM experiment interfacing circuit translates up lower level experiment input signals to the experiment 12-V dc level and translates down the experiment output signals to the required levels. The input interfacing elements are implemented by 2N5116 J-FETS and 2N2484 transistors, while the DDO output line is stepped down by two 6.2-kΩ resistors. A zener diode clamping circuit is used for the signal return. Six translators are used for the 3 pairs of redundant signals: namely, CDE, CCL, and CEN. An additional two translate DEN and the digital telemetry clock.

The 32-bit command word, CDI, is clocked by CCL into a 32-bit serial to parallel register implemented with four CD4034 integrated circuits. At the end of the CEN gate, the new command word is parallel loaded to the execute registers made up by CD4042 and CD4029 integrated circuits. This loaded command word can be read back to the spacecraft computer through line DDO by activating line DEN along with the digital telemetry clock.

The line DEN parallel loads the command word into four CD4021 integrated circuits. These ICS are 8-bit parallel in, serial out, devices. The NRZ output data is interfaced to the computer.

When a command word is received, the gain control bits will be loaded into the CD4029 UP/DOWN counters, and the remaining bits into the CD4042 latches; in turn, the command word is loaded into the analog telemetry shift registers (four CD4021). The command word stored in the CD4029 and CD4042 set up the state of the experiment.

During each frame, the data loaded in the analog telemetry register is formatted and encoded to a 2-line tristate code by the encoder implemented by one CD4040, two CD4017, and two CD4013. The 2 tristate lines named AOB and AZB drive the 12-kHz HK VCO, and they are organized as a 48-bit word instead of 32 for purposes of decoding and data verification.

At the beginning of each frame cycle, a double clock pulse is provided to the gain control logic for the purposes of updating the gain setting. Whether the CD4029 UP/DOWN counter will retain, increase, or decrease its 3-gain bits depends on the state of the AUTO/MAN bit and the UP/DOWN lines from the PGA threshold detectors.

Immediately after the gain bits double clock pulse, new commands will be loaded into the execute registers whenever there is a new command stored. If not, the information in the latches stays, and will be transmitted via the analog telemetry registers.

2) Input Amplifier and Bandpass Filter Board: The input amplifier and bandpass filter board contains the input signal conditioning amplifier, 20-kHz notch filter and associated switching circuitry, calibrate signal injection switching, and 6 bandpass filters. The bandpass filters divide the 1- to 32-kHz spectrum into five octave bands, and one 6-kHz narrow-band segment.

The input amplifier incorporates four transistors and provides a voltage gain of approximately 3. (Overall gain including transformer loss is about 1.5.) Feedback is established by a combination of resistors. The calibration signal is injected into the emitter of the primary transistor and may be switched on or off by a CD4016 CMOS quad-analog gate. Low output impedance, a requirement for driving the bandpass filter array properly, is obtained by a complimentary emitter-follower output stage.

The 6-kHz narrow-band filter and the three lowest octave frequency band filters (covering 1 through 8 kHz) are driven directly by the input amplifier. The two higher octave band filters covering the frequency range 8 through 32 kHz are driven via the 20-kHz notch filter and filter switch, two sections of a CD4016 analog gate, and by an emitter-follower. The emitter-follower exhibits high input impedance to minimize loading of the 20-kHz notch filter, while providing a low output impedance required to drive the two bandpass filters. The notch filter is a second order Chebyshev bandstop filter with a maximum attenuation of 30 dB at 20 kHz.

The 1- to 2-kHz, 2- to 4-kHz, 8- to 16-kHz, and 16- to 32-kHz bandpass filters are third order Chebyshev octave band filters with 1-dB passband ripple. These filters provide approximately 38 dB of attenuation an octave above or below the band edges. The 4- to 8-kHz bandpass filter is a fourth order Cauer parameter filter with 0.28-dB passband ripple. This filter provides about 40-dB attenuation below 2.9 kHz and above 10.9 kHz. The 6-kHz narrow bandpass filter is a second order Chebyshev, 1-dB passband ripple filter. The measured 1-dB bandwidth is 226 Hz, and the 3-dB bandwidth 377 Hz. All filters have transformer-coupled outputs.

3) Programmable Gain Amplifier: The programmable gain amplifier is a 5 stage switched gain amplifier having a maximum voltage gain of 96 dB. Gain may be varied in 10-dB steps over a 70-dB range by means of gain control lines in a 4-2-1 binary coded sequence.

Each stage is comprised of a dual-transistor differential pair with emitter-follower output. This type of configuration provides symmetrical limiting and rapid recovery range from signal overloading.

The first stage is a fixed-gain signal conditioning stage providing a gain of approximately 26 dB. Accounting for the filter voltage loss due to impedance transformation ratio, the actual gain is 10-dB gain referring to the filter input.

Stages two through five are gain programmed by switching the resistors between the emitters of the differential pair by means of a CD4066 analog gate. Stages two, three, and four each have a switched gain of either 0 or 20 dB. Stages two and three are switched simultaneously by a control line to provide an overall gain of either 0 or 40 dB. Stage four is switched to provide a gain of 0 or 20 dB. The fifth stage is switched to provide a gain of 0 or 10 dB.

4) Power Supply and Threshold Detector: The power regulator accepts unregulated 28 V and provides four regulated voltages at +6, +12, +18, and +24 V. The +6, +12, and +18 V supplies are obtained from voltage followers, which provide a low output impedance for driving the experiment circuitry. Increased current drive capability for the +12-V buss is provided by a complimentary emitter follower.

The threshold detectors provide digital output signals used to initiate an increase or decrease in gain of the PGA. The circuit consists of a signal amplitude detector and two comparators.

The detector output is applied to two comparators. The output of the upper threshold comparator is the compliment of the command to change amplifier gain downward, and is normally at a +12-V logic level, going to 0 V when the input signal level exceeds the upper threshold. The output of the lower threshold comparator is the compliment of the command to change amplifier gain upward. It is normally at a +12-V logic level, changing to 0 V when signal amplitude is below the lower threshold.

The upper threshold and lower threshold are established by a voltage divider network. A small amount of hysteresis is provided in each comparator.

5) Voltage-Controlled Oscillator: An array of six VCO's is implemented by the integrated circuit CD4046. The center frequency of each VCO is spaced octavely starting at 12 kHz, and the highest center frequency is 384 kHz. With the exception of the 12-kHz VCO (HK VCO), each VCO is driven by its corresponding PGA; the frequency deviation is ±16.7 percent of center frequency for ±5 V referring to the input.

The output of all six VCO's are filtered by their respective two-pole Cheyshev bandpass filters. Harmonic suppression for these filters is about 30 dB.

With the exception of the HK VCO, the outputs of all VCO's can be switched in or out from the output amplifier by five transmission gates (CD4016). The HK VCO stays on at all times. Another transmission gate couples the 6-kHz NB channel to the output amplifier. The lines feeding to the output amplifier are voltage summed by weighted resistors to scale the subcarrier power distribution.

The output amplifier, implemented by two 2N2605 and two 2N2484 transistors, provides 14-dB voltage gain. It has an output impedance of 100 Ω, and it is transformer coupled to its load.

An *L-C* type oscillator is chosen for power and stability tradeoff. A CMOS Device CD4007 is used for the gain element for the *L-C* oscillator. A CD4040 device generates all the reference frequencies for the VCO's and the 187.5-Hz clock. A CD4013 device is used to generate to 1.5-kHz calibrate pulse. Zener diodes are used to translate the signals from the binary divider to the pulse generator.

III. Summary

The Stanford University broad-band VLF receiver on ISEE-A is an integral part of the Stanford University VLF wave injection experiment being carried out as part of the ISEE mission. Data acquired with this instrument will help achieve a better understanding of dynamical processes in the magnetosphere, an important portion of the earth's environment.

Acknowledgment

We wish to acknowledge the many valuable discussions we have held with our colleagues at the Radioscience Laboratory. We also wish to acknowledge the efforts and dedication of the engineering staff of Develco, Inc., Mountain View, CA, in developing and building our ISEE-A VLF wave-injection receiver.

References

[1] T. F. Bell, "VLF wave generation through particle precipitation induced by VLF transmitters," *J. Geophys. Res.*, vol. 81, p. 3316, 1976.

[2] R. A. Helliwell and J. P. Katsufrakis, "VLF wave injection into the magnetosphere from Siple Station, Antarctica," *J. Geophys. Res.*, vol. 79, p. 2511, 1974.

[3] R. A. Helliwell, J. P. Katsufrakis, T. F. Bell, and R. Raghuram, "VLF line radiation in the earth's magnetosphere and its association with power system radiation," *J. Geophys. Res.*, vol. 80, p. 4249, 1975.

[4] C. G. Park, "The role of manmade VLF signals and noise in wave-particle interactions in the magnetosphere," in *Proc. Int. Sym. Solar-Terrestrial Physics* (Boulder, CO), D. Williams, Ed., June 1976.

[5] R. Raghuram, R. L. Smith, and T. F. Bell, "VLF Antarctic antenna: Impedance and efficiency," *IEEE Trans. Antennas Propagat.*, vol. AP-22, pp. 334–338, 1974.

[6] G. S. Stiles and R. A. Helliwell, "Frequency-time behavior of artificially stimulated VLF emissions," *J. Geophys. Res.*, vol. 80, p. 608, 1975.

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Report No. 983-761029

VLF WAVE INJECTION RECEIVER

Prepared for:

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Stanford University
Stanford, CA 94305

Under:

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1. BACKGROUND

The Helliwell experiment for the ISEE-A Satellite is a VLF wave injection experiment with the purpose of determining, under controlled conditions, the basic mechanisms of interaction between energetic particles and discrete VLF waves in the magnetosphere. The main wave injection device is the Stanford VLF transmitter presently in operation at Siple Station in the Antarctic. For the ISEE mission the transmitter will be used to inject VLF waves throughout the magnetosphere, producing both VLF emissions and energetic particle pitch-angle scattering. In the general case the injected signal, as well as any stimulated VLF emissions, will be detected on the ISEE-A satellite by the Helliwell broadband VLF receiver. Information gained from the wave injection experiment should prove invaluable in increasing the understanding of the basic physical processes which determine the characteristics of waves and particles in the magnetosphere, and also in the support of future space missions. In particular, it should be an invaluable aid in planning VL. wave injection missions for the Plasma Physics and Environmental Perturbation Laboratory, which has been established as part of the shuttle-bus scientific program.

Professor R.A. Helliwell of Stanford University is the Principal Investigator and Dr. T.F. Bell, also of Stanford University, is the Co-Investigator.

2. THEORY OF OPERATION

The receiver package contains signal filtering, amplification, gain control, switching, calibration, and other functions necessary to transfer the 1- to 32-kHz signal from the preamplifier to the analog telemetry system. The system block diagram in Drawing 106013 shows the major receiver functions.

Signals in the 1- to 32-kHz band from the preamplifier are fed to a parallel bank of six filters. Five of the filters are broadband octave-width filters and one filter is a narrow-band filter centered at 6 kHz, an operating frequency of the Siple transmitter. A 20-kHz notch filter is incorporated into the 8- to 16-kHz and 16- to 32-kHz bandpass filters to minimize interference expected from the spacecraft power converter which operates at 20 kHz.

The outputs of the filters are fed into six amplifiers with variable gain. The purpose of the variable gain for each band is to maintain output signal levels within the range required by the spacecraft telemetry. The signal level is maintained below telemetry saturation and above telemetry system noise levels. The gain of each channel is adjustable in 10-dB steps over a 0- to 70-dB range by ground command or by automatic signal level sensing. When a ground command for automatic gain is received, the amplitude envelope of signals in each channel is monitored and the gain adjusted to maintain a prescribed level. This adjustment is made in 10-dB increments at intervals of about 5.4 seconds.

Each signal channel, except for the 6-kHz channel, drives a Voltage-Controlled Oscillator (VCO). Normally the output of each VCO and a housekeeping VCO are summed, and the resultant signal used to modulate the analog telemetry transmitter. However, the output of any signal channel can be turned off by ground command. This allows the telemetry power to be concentrated on a desired channel for long-distance operation during apogee. Generally the frequencies of interest decrease with increasing distance from the earth and the higher frequency VCO's with their attendant wide bandwidths can be turned off to maintain a useful signal-to-noise ratio.

A relatively narrow-band VCO is provided to generate an FSK signal for housekeeping functions. The PGA gain levels, channel ON/OFF, and AUTO/MAN mode for each channel, and notch filter ON/OFF and CAL ON/OFF data are transmitted over this VCO.

System calibration signals are generated in the receiver package. System stability is sufficient so that only infrequent calibration is required. The receiver is calibrated by injecting the harmonics of 1.5 kHz into the input amplifier. Thus each band is excited at least by a harmonic component during the calibration cycle. The calibration signal will automatically turn itself off after eight cycles of operation. Provisions to inhibit its operation after a preset length of time is also incorporated into the source as a safety precaution against intermittent operation. The amplitude and duration of the CAL signal is sufficient to cause each channel to step from 70-dB to 0-dB gain over a period of approximately 45 seconds.

3. DIGITAL COMMAND

The Helliwell VLF Experiment requires a 32-bit serial command word received under spacecraft control asynchronously to the experiment control logic. The spacecraft may generate more than 32 bits and clock pulses but the 32-bit word must be contained in the last 32 bits of the serial stream.

The command word format is listed in Table 1. The tables assumes a 37-bit clock burst, as defined in ISEE-714-75-005 (May 1975), with Bit 37 (the MSB) the last bit received.

The command word provides gain and mode control for 6 channels of VLF amplifiers plus control of a calibrate function and a 20-kHz notch filter. The bit functions are as follows:

CH(#) ON/OFF:	Determines if the output of the amplifier is summed in the telemetered signal ("1" level is ON or summed)
CH(#) AUTO/MANUAL:	Determines if the programmable amplifer is in an automatic or manual gain control mode ("1" level = automatic)
10-, 20-, and 40-dB Bits:	The sum determines the gain of the amplifier in the manual mode or the initial gain in the automatic mode.
CAL:	When set, this bit will cause the experiment to go into the Cal mode.
20-kHz Notch Filter ON/OFF:	When set, any 20-kHz signals will be filtered in the 8- to 16-kHz and 16- to 32-kHz channels (Channels 4 and 5).

Verification that the experiment received the command word may be accomplished by the digital telemetry link between the spacecraft and experiment.

TABLE 1

COMMAND WORD FORMAT

BIT NO.	FUNCTION	CHANNEL
1-5	Unassigned	
6 (LSB)	CH 1 ON/OFF	1-2 kHz
7	AUTO/MAN	
8	10 dB	
9	20 dB	
10	40 dB	
11	CH 2 ON/OFF	2-4 kHz
12	AUTO/MAN	
13	10 dB	
14	20 dB	
15	40 dB	
16	CH 3 ON/OFF	4-8 kHz
17	AUTO/MAN	
18	10 dB	
19	20 dB	
20	40 dB	
21	CAL	
22	CH 4 ON/OFF	8-16 kHz
23	AUTO/MAN	
24	10 dB	
25	20 dB	
26	40 dB	
27	CH 5 ON/OFF	16-32 kHz
28	AUTO/MAN	
29	10 dB	
30	20 dB	
31	40 dB	
32	CH 6 ON/OFF	6 kHz NB
33	AUTO/MAN	
34	10 dB	
35	20 dB	
36	40 dB	
37 (MSB)	20 kHz Notch Filter ON/OFF	

4. DIGITAL TELEMETRY

The spacecraft can verify that the experiment has received the proper command word through the digital telemetry link between the experiment and spacecraft controller. Upon request from the spacecraft, a 32-bit telemetry word will be serial shifted from the experiment under spacecraft control. The first bit will be the MSB and correspond to Bit 37 in the command word format. The last bit will be the LSB and correspond to Bit 6 in the command word format.

Since the experiment may not respond to a new command word for up to 5.4 seconds, and dynamic bits may change 5.4 seconds after responding to a new command, it is only necessary that the static bits be verified after 5.4 seconds.

All AUTO/MAN, CH ON/OFF and NOTCH ON/OFF bits are static. The gain control bits are static only if the AUTO/MAN bit for that channel is set to MAN. The Cal bit is dynamic and should reset approximately 45 seconds after recognition of a command word.

5. ANALOG TELEMETRY

A 500-kHz analog transmitter is required for the transmission of receiver analog data to the ground. The signals will be in the frequency range of 6- to 500-kHz and have a maximum amplitude of 6.8 V p-p. Loading on the transformer output is not to exceed 20 kilohms and 200 pf.

6. POWER

The experiment requires the following power source:

Voltage:	28 Vdc ±5%
Current:	25 mA avg, 30 mA peak, 250 mA surge (on power up)
Average Power:	.7 watt

The +28 Vcc source is regulated to supply +24 V, +18 V, +12 V and +6 V. In order to minimize power consumption, the supply is a totem pole configuration.

7. CABLING AND CONNECTORS

The experiment requires two 26-pin AMP HD 22 Connectors. Pin assignments are as follows:

SPACECRAFT CONNECTOR PIN NO.	FUNCTION
1	Preamp 2
2	Shield for Pin 1
3	Chassis Ground
4	+28 Vdc
5	+28 Vdc
6	DSI II (data)
7	ASI I
8	Analog Transmitter
9	Analog Transmitter
10	Preamp 1
11	N/C
12	N/C
13	Circuit Ground
14	+28 V Power Return
15	DSS II (clock)
16	Envelope A
17	Clock A
18	Serial Data A
19	N/C
20	Chassis GND
21	Circuit Ground
22	+28 V Power Return
23	DSG II (envelope)
24	Envelope B
25	Clock B
26	Serial Data B

TEST CONNECTOR (to GSE) PIN NO.	FUNCTION
26	ACL #1
18	ACL #2
1	AOB
24	AZB
20	ADO #1
22	DPT
25	CDI
10	CCL
5	DDO
19	DCL
23	CEN
8	+12 V
9	0 V

8. MECHANICAL INTERFACE

See Drawing 3-105934 for dimensions for the experiment housing.

The overall dimensions are as follows:

Weight:	1303 grams
Height:	2.75 inches
Length:	9.02 inches (does not include connector protrusions)
Width:	7.25 inches (including mounting feet).

9. CIRCUIT DESCRIPTION

9.1 DIGITAL COMMAND LINK

9.1.1 Introduction

The purpose of the digital section of the HEM experiment is to provide the following functions:

A. Gain control settings to six channels of VLF amplifiers

B. Output summing control for 6 VLF amplifier outputs

C. Digital telemetry information to the spacecraft computer

D. Analog telemetry information to the ground

E. Known "power up" status

F. Calibration function

G. Interfacing digital signals between the spacecraft and experiment.

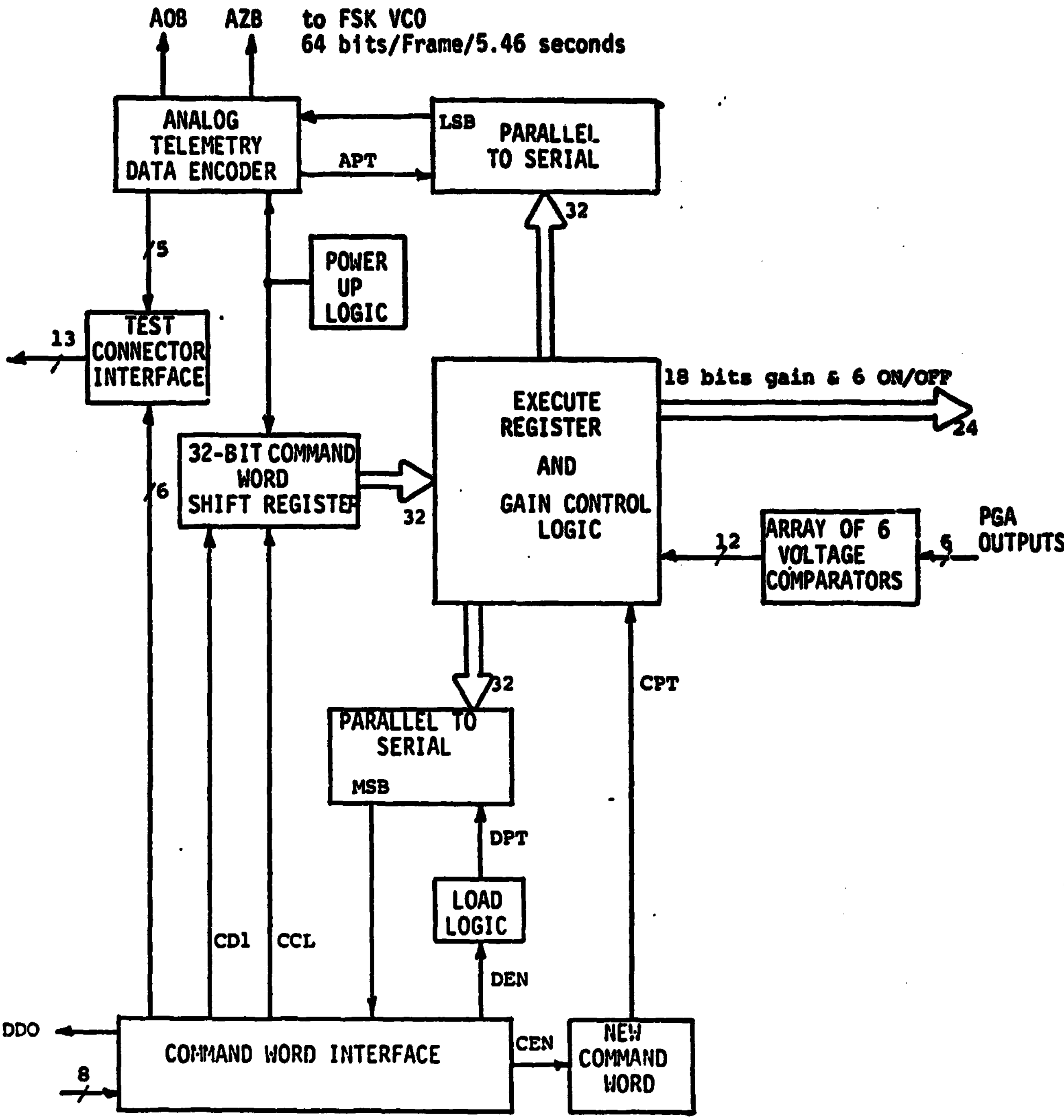
9.1.2 Glossary

A list of abbreviations used in both the experiment and GSE digital circuitry is contained in Table 2 of this manual.

9.1.3 Description of Operation

The digital electronics operates on a synchronous 5.4-second cycle with the exception of command word and digital telemetry transfers which are under control of the spacecraft computer.

The HEM experiment interfacing circuit translates up lower level experiment input signals to the experiment 12-Vdc level and translates down the experiment output signals to the required levels. The input interfacing elements are implemented by 2N5116 J-Fets and 2N2484 transistors, while the DDO output line is stepped down by two 6.2-K resistors. The zener diode clamping circuit is used for the signal return. Six of the translators are used for the 3 pairs of redundant signals: namely, CDI, CCL, and CEN. The remaining two translates DEN and DCL.



DIGITAL COMMAND LINK

H. 781208-1

TABLE 2

GLOSSARY

ACL	Analog Telemetry Clock
ADI	Analog Telemetry Data In
ADO	Analog Telemetry Data Out
AGA	Amplifier Gain - A Bit (10 dB)
AGB	Amplifier Gain - B Bit (20 dB)
AGC	Amplifier Gain - C Bit (40 dB)
AOB	Analog Telemetry One Bit
AOC	Amplifier ON/OFF Control
ASI	Power Monitor
AT	Analog Telemetry
AZB	Analog Telemetry Zero Bit
CCD	Counter Count Down
CCL	Command Word Clock
CCU	Counter Count Up
CDI	Command Word Data In
CDO	Command Word Data Out
CEN	Command Word Envelope
CPJ	Command Word Parallel Jam
CPT	Command Word Parallel Transfer
CST	Command Word Serial Transfer
CW	Command Word
DCL	Digital Telemetry Clock
DDI	Digital Telemetry Data In
DDO	Digital Telemetry Data Out
DEN	Digital Envelope
DPT	Digital Telemetry Parallel Transfer
DT	Digital Telemetry
FOB	Frequency Demodulated One Bit
ESY	Frame Sync
FZB	Frequency Demodulated Zero Bit
MCL	Monitor Data Clock
MDI	Monitor Data In
MPT	Monitor Data Parallel Transfer
MSY	Marker Sync
RDN	Redundancy
TST	Test

CDI, the 32-bit command word, is clocked by CCL into a 32-bit serial to parallel register implemented with four CD4034. At the end of the CEN gate, the new command word is parallel loaded to the execute registers made up by CD4042 and CD4029. This loaded command word can be read back to the spacecraft computer through line DDO by activating lines DCL and DEN.

DEN parallel loads the command word into four CD4021, eight-bit parallel in serial out device, while DCL clocks the word out. NRZ output data is interfaced to the computer.

The format of the command word is listed in Table 1. Note that the first 5 bits have no significance, and only the last 32 bits are active. The command word consists of (1) 3 bits of gain setting to each of the six programmable gain amplifiers (PGA), (2) six bits to set each of the PGA in either auto (automatic gain control) or manual (fixed gain) mode, and (3) another 6 bits set each of the VCO outputs - to determine whether the outputs of Channels 1-5 and the NB channel should sum into the TLM output amplifier; these bits are termed "CH ON/OFF". The remaining two bits are termed CAL (calibrate) and notch ON/OFF (20 kHz notch filter ON/OFF).

When a command word is received, the gain control bits will be loaded into the CD4029 up/down counters, and the remaining bits into the CD4042 latches; in turn, the command word is loaded into the analog telemetry shift registers (four CD4021). The command word stored in the CD4029 and CD4042 set up the state of the experiment.

During each frame, the data loaded in the analog telemetry register will be formatted and encoded to a 2-line tristate code by the encoder implemented by one CD4040, two CD4017, and two CD4013. The 2 tristate lines named AOB and AZB drive the 12-kHz HK VCO, and they are organized as a 48-bit word instead of 32 for purposes of decoding and data verification. The analog telemetry word format is shown in Table 3.

TABLE 3

ANALOG TELEMETRY WORD FORMAT

WORD NO.	BIT NO.	FUNCTION
1	1	CH 1 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
2	1	CH 2 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
3	1	CH 3 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
4	1	Calibrate
	2	No function
	3	No function 0's
	4	No function
	5	No function
	6	No code
5	1	CH 4 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
6	1	CH 5 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code

TABLE 3

(Continued)

WORD NO.	BIT NO.	FUNCTION
7	1	CH 6 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
8	1	Notch Filter ON/OFF
	2	No function
	3	No function
	4	No function
	5	No function
	6	No code (remains until next transmission)

At the beginning of each frame cycle, a double clock pulse is provided to the gain control logic for the purposes of updating the gain setting. Whether the CD4029 up/down counter will retain, increase, or decrease its 3-gain bits depends on the state of the AUTO/MAN bit and the UP/DOWN lines from the PGA threshold detectors.

Immediately after the gain bits double clock pulse, new commands will be loaded into the execute registers whenever there is a new command stored. If not, the information in the latches stays, and will be transmitted via the analog telemetry registers. When the experiment is turned on, the power-up logic will - by means of jamming the command register - set all PGA's to its maximum gain at auto mode; sum all VCO outputs to the output amplifier; turn the 20-kHz notch filter and the calibration generator on. Since the PGA is in auto mode, and the calibration pulse in full amplitude, the PGA will step down 10-dB gain on every frame cycle. At the end of 8 frame cycles, the PGA will have stepped to its minimum gain; then the CAL function will turn off by itself, and the PGA will start stepping up in gain. The CAL function can be commanded on or off at any time and it also turns itself off after 8 frame cycles without command.

9.2 INPUT AMPLIFIER AND BANDPASS FILTER BOARD

The schematic of the input amplifier and bandpass filter board is shown in Drawing D6-105937. The board contains the input signal conditioning amplifier, 20-kHz notch filter and associated switching circuitry, calibrate signal injection switching, and six bandpass filters. The bandpass filters divide the 1- to 32-kHz spectrum into five octave bands, and one 6-kHz narrow-band segment.

The input amplifier consists of transistors Q1 through Q4, and provides a voltage gain of approximately 3. (Overall gain including the transformation loss of Transformer T1 is about 1.5.) Feedback is established by R7 and the parallel combinations of R6 and R3. A calibration signal is injected into the emitter of Q1 via the network formed by R3, R20, and C78. The calibration signal may be switched on or off by a section of the Analog Switch U1 (a CD4016 CMOS quad-analog gate). Low output impedance, a requirement for driving the bandpass filters array properly, is obtained by the complimentary emitter follower output stage formed by Q3 and Q4.

The 6-kHz narrow-band filter and the three lowest octave frequency band filters (covering 1 through 8 kHz) are driven directly by the input amplifier. The two higher octave band filters covering the frequency range 8 kHz through 32 kHz are driven via the 20-kHz notch filter and filter switch, two sections of a CD4016 analog gate, by emitter follower Q7. The emitter follower exhibits high input impedance to minimize loading of the 20-kHz notch filter, while providing a low output impedance required to drive the two bandpass filters. The notch filter is a second order Tchebychev bandstop filter with a maximum attenuation of 30 dB at 20 kHz.

The 1- to 2-kHz, 2- to 4-kHz, 8- to 16-kHz, and 16- to 32-kHz bandpass filters are third order Tchebychev octave band filters with 1-dB passband ripple. These filters provide approximately 38 dB of attenuation an octave above or below the band edges. The 4- to 8-kHz bandpass filter is a fourth order Cauer parameter filter with 0.28-dB passband ripple. This filter provides about 40-dB attenuation below 2.9 kHz and above 10.9 kHz. The 6-kHz narrow bandpass filter is a second order Tchebychev, 1-dB passband ripple filter. The measured 1-dB bandwidth is 226 Hz, and the 3-dB bandwidth 377 Hz. All filters have transformer-coupled outputs.

9.3 PROGRAMMABLE GAIN AMPLIFIER

The schematic of the programmable gain amplifier is shown in Drawing D6-105929. The programmable gain amplifier is a five-stage switched gain amplifier having a maximum voltage gain of 96 dB. Gain may be varied in 10-dB steps over a 70-dB range by means of the gain control lines AGA, AGB, and AGC in a 4-2-1 binary coded sequence.

Each stage is comprised of a dual-transistor differential pair with emitter follower output. This type of configuration provides symmetrical limiting and rapid recovery from large signal overloading.

The first stage is a fixed-gain signal conditioning stage providing a gain of approximately 26 dB. Accounting for the filter voltage loss due to impedance transformation ratio, the actual gain is 10 dB gain referring to the filter input (on the input amplifier and bandpass filter board).

Stages two through five are gain programmed by switching the resistors between the emitters of the differential pair by means of a CD4066 analog gate. Stages two, three, and four each have a switched gain of either 0 dB or 20 dB. Stages two and three are switched simultaneously by control line AGC to provide an overall gain of either 0 dB or 40 dB. Stage four is switched by line AGB to provide a gain of 0 dB or 20 dB. The fifth stage is switched by line AGA to provide a gain of 0 dB or 10 dB.

9.4 POWER SUPPLY AND THRESHOLD DETECTOR

The schematic for the power supply and threshold detector is shown in Drawing D6-105899.

The power regulator accepts unregulated 28 volts and provides four regulated voltages at +6 V, +12 V, +18 V, and +24 V. The regulator is comprised of Q3, Q4, and Reference Diode CR9. Error feedback is obtained from R65.

The +6, +12, and +18 volt supply voltages are obtained from voltage followers A12, A13, and A14. Output voltages are obtained from the divider string R65, R67, R68 and R69. These voltages are applied to the noninverting input terminals of A12, A13, and A14. The voltage followers provide a low output impedance for driving the experiment circuitry. Increased current drive capability for the +12-V buss is provided by the complimentary emitter follower, Q5 and Q6.

The threshold detectors provide digital output signals used to initiate an increase or decrease in gain of the programmable gain amplifier. The circuit consists of a signal amplitude detector and two comparators.

The detector consists of Transistor Q9, Diodes CR10, CR11, and CR12, and associated circuitry. The detector function is performed by CR12 and Q9. CR10 and CR11 are temperature compensating diodes which compensate for the drift in forward voltage drop of CR12 and the base-emitter junction of Q9. The detector time constant is established by the low-pass filter formed by R87 and C64, and is approximately 1.5 seconds.

The detector output is applied to two comparators. Q11 and Q8 with associated circuitry comprise the upper threshold comparator, and Q10 with Q7 form the lower threshold comparator. The output of the upper threshold comparator, $\overline{CCD}$, is the compliment of the command to change amplifier gain downward, and is normally at a +12-V logic level, going to zero volts when the input signal level exceeds the upper threshold. The output of the lower threshold comparator, $\overline{CCU}$, is the compliment of the command to change amplifier gain upward. It is normally at a +12 V logic level, changing to zero volts when signal amplitude is below the lower threshold.

The upper threshold is established by the voltage divider network formed by R78 and R81. The lower threshold voltage divider network is R79 and R80. A small amount of hysteresis is provided in each comparator by R82 and R72.

9.5 VOLTAGE CONTROLLED OSCILLATOR

The schematic for the voltage controlled oscillator is shown in Drawing D6-105930.

An array of six Voltage Controlled Oscillators (VCO's) is implemented by CD4046. The center frequency of each VCO is spaced octavely starting at 12 kHz, and the highest center frequency is 384 kHz. With the exception of the 12-kHz VCO, which is also called HK VCO, each VCO is driven by its corresponding PGA; the frequency deviation is ±16.7% of center frequency for ±5 V refering to the input.

The transmission mode for the HK VCO is FSK. The encoded lines AOB and AZB are level translated by two zener diodes. Another zener diode translates the FSY line which is the auto-zero gating line for the HK VCO.

The output of all six VCO's are filtered by their respective two-pole Tchebychev bandpass filters.

Harmonic suppression for the above filters is about 30 dB.

With the exception of the HK VCO, the outputs of all VCO's can be switched in or out from the output amplifier by five transmission gates (CD4016). The HK VCO stays on at all times. Another transmission gate couples to 6 kHz NB to the output amplifier. The lines feeding to the output amplifier are voltage summed by weighted resistors to scale the subcarrier power distribution. The analog switches are controlled by Command Bits AOC1 to AOC6.

The output amplifier, implemented by two 2N2605 and two 2N2484 transistors, provides 14-dB voltage gain. It has an output impedance of 100 ohms, and it is transformer coupled to its load.

An L-C type oscillator is chosen for power and stability trade-off. CMOS Device CD4007 is used for the gain element for the L-C oscillator. CD4040 generates all the reference frequencies for the VCO's and the 187.5-Hz clock. A CD4013 is used to generate the 1.5 kHz calibrate pulse. Again, zener diodes are used to translate the signals from the binary divider to the pulse generator.

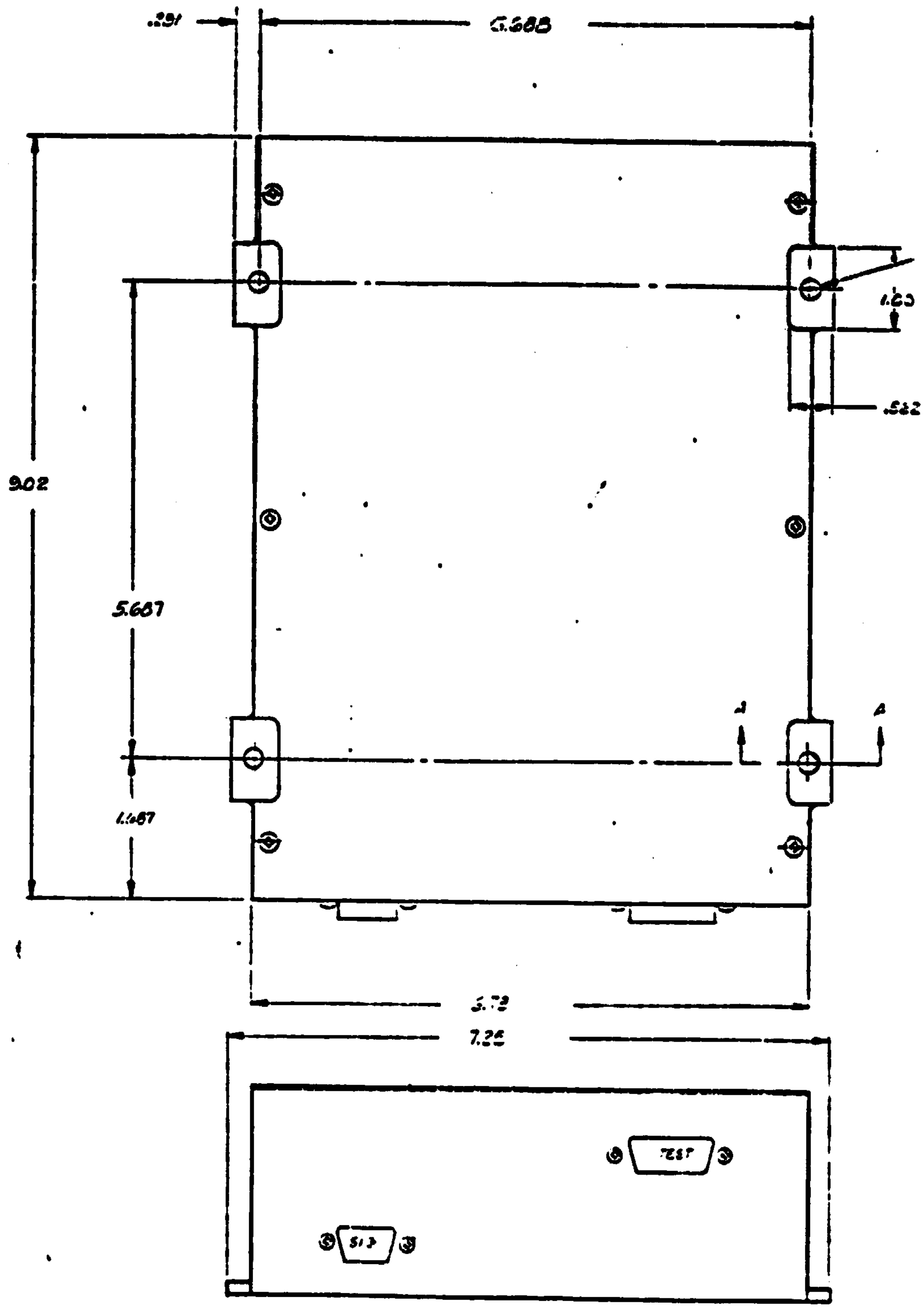
ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.
1	105920	OUTLINE DWG D5		R
2	105938	INTERCONNECT DWG D5		R
3	106013	VLF REC. BLOCK DIA C9		R
4	105934	HOUSING D3		1
		ZE10A-H24 MAGNESIUM		
		DOW 23 FINISH REF		1
5	105935	COVER C3		1
		ZE10A-H24 MAGNESIUM		
		DOW 23 FINISH REF		1
6		SCREW 4-40 X 1/4 FD SST		1
7	106009-01	STANDOFF TEFLON B3		6
8	-02	" " B3		6
9	106009-03	" " B3		12
10		NUT 4-40 SST		4
11	1060117	STANDOFF SPECIAL TEFLON B3		2
12	1060118	" " " B3		2
13		SCREW 6-32 X 1/4 FLAT HT SST		6
14	105946-01	SPACER FOAM B3		50
15	-02	" " ECCOFOAM		50
16	-03	" " FPH CATALYST		50
17	-04	" " 12-10-H		100
18	105946-05	SPACER - FOAM B3		50
19	105947-	SUPPORT, SIDE - FOAM B3		8
20		SCREW 4-40 X 1/4 PAN HD SST		8
21	105899	PWR SUPPLY THRESHOLD DET PL		1
22	105937	INPUT AMP BD. PL		1
23	105392	DIGITAL COMMAND BD. PL		1
24	105929	PROGRAMMABLE GAIN AMP BD. PL		1
25	105930	VCO & OUTPUT AMP BD. PL		1
26		CONN. AMP 311P407-2P-B-15		*
27		CONN. AMP 311P407-2S-B-15		*
28		WIRE 26 AWG STRANDED WHT		AR
29		* CUSTOMER SUPPLIED		

REV		
D	REWRITTEN 6-1-76 MMM	
E	GENERAL ... UPDATE ...	

ORIGINAL PAGE IS OF POOR QUALITY

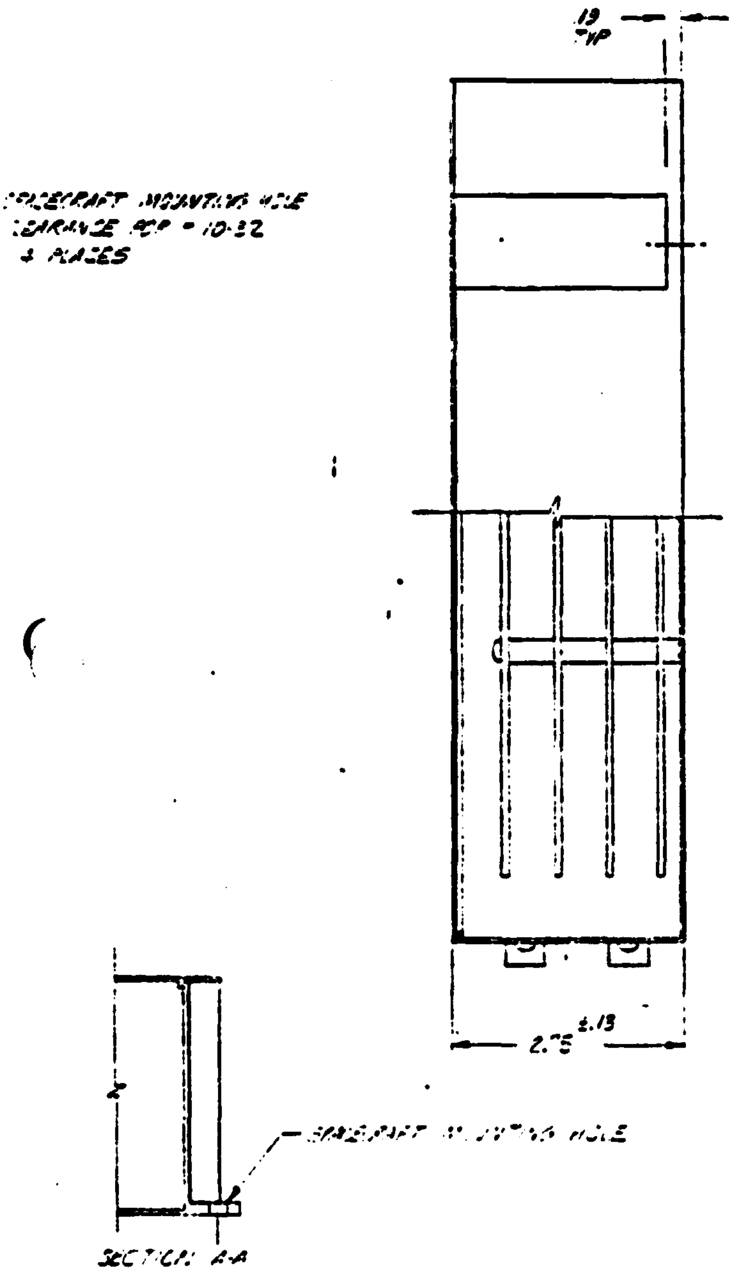
BY MSM	CK.
APR. BN 6/1/76	APR.
TITLE ULF WAVE PROPAGATION RECEIVER MODEL 105936	
PARTS LIST NUMBER P/L 105936	REV E
SHEET 1 OF 1	

DEVELCO, INC.


.281
6.688
1.60
.522
9.02
5.687
1.687
A
A
5.72
7.25
TEST
S13

REVISIONS						
SYM	DATE	DESCRIPTION	DRN	CKD	APPR	DATE
A	[illegible]	[illegible]				
B	[illegible]	[illegible]				
C	[illegible]	[illegible]				

1



SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

USED ON | NEXT ASSY | QTY REQD

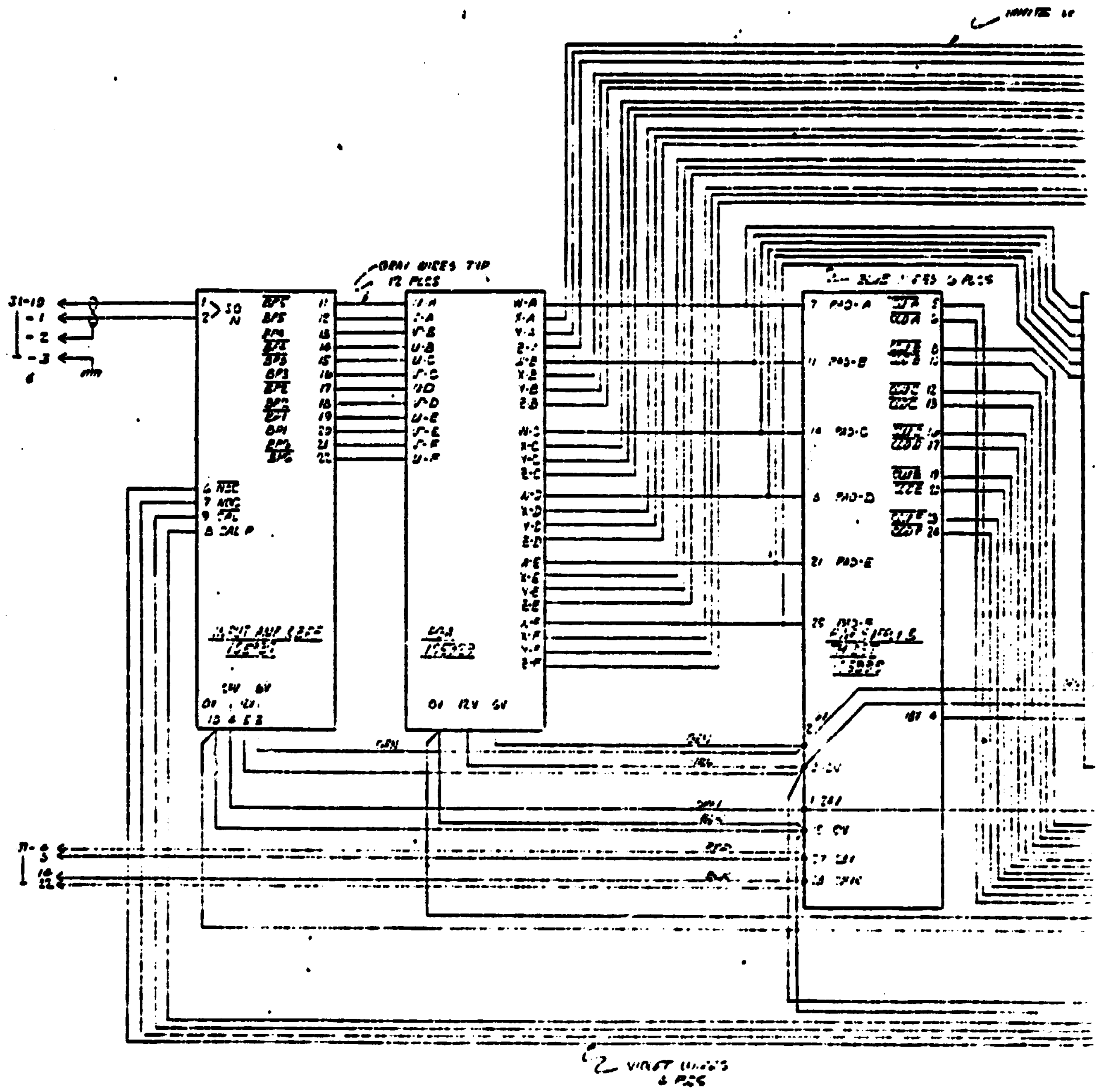
APPLICATION

DEVELCO INC.

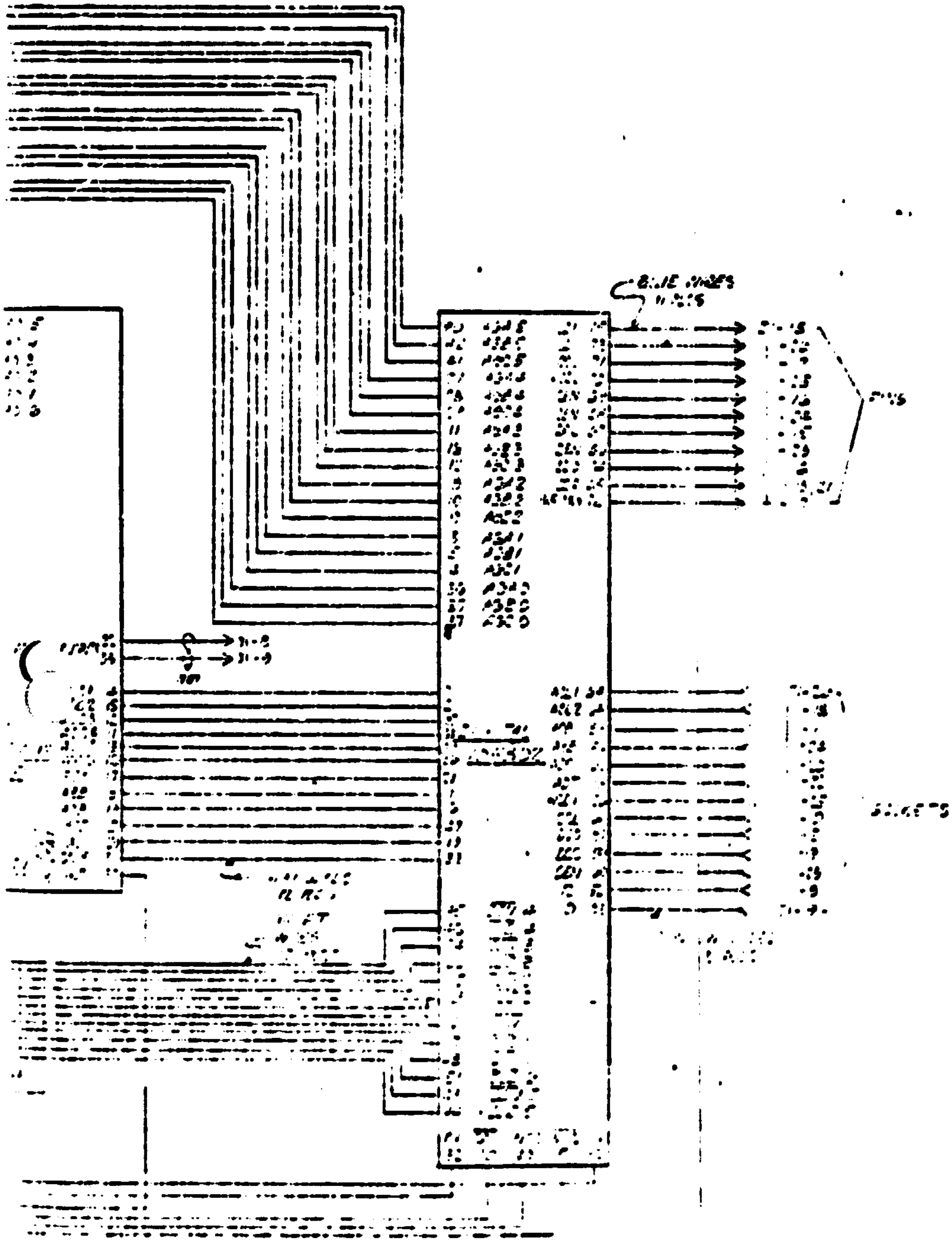
TITLE

SIZE | CODE IDENT NO | DWG NO | REV

D | 30002 | [illegible] | C



REVISIONS						
SYM	DATE	DESCRIPTION	DRN	CKD	APPD	DATE



USED ON	NEXT ASSY	QTY REQD
APPLICATION		

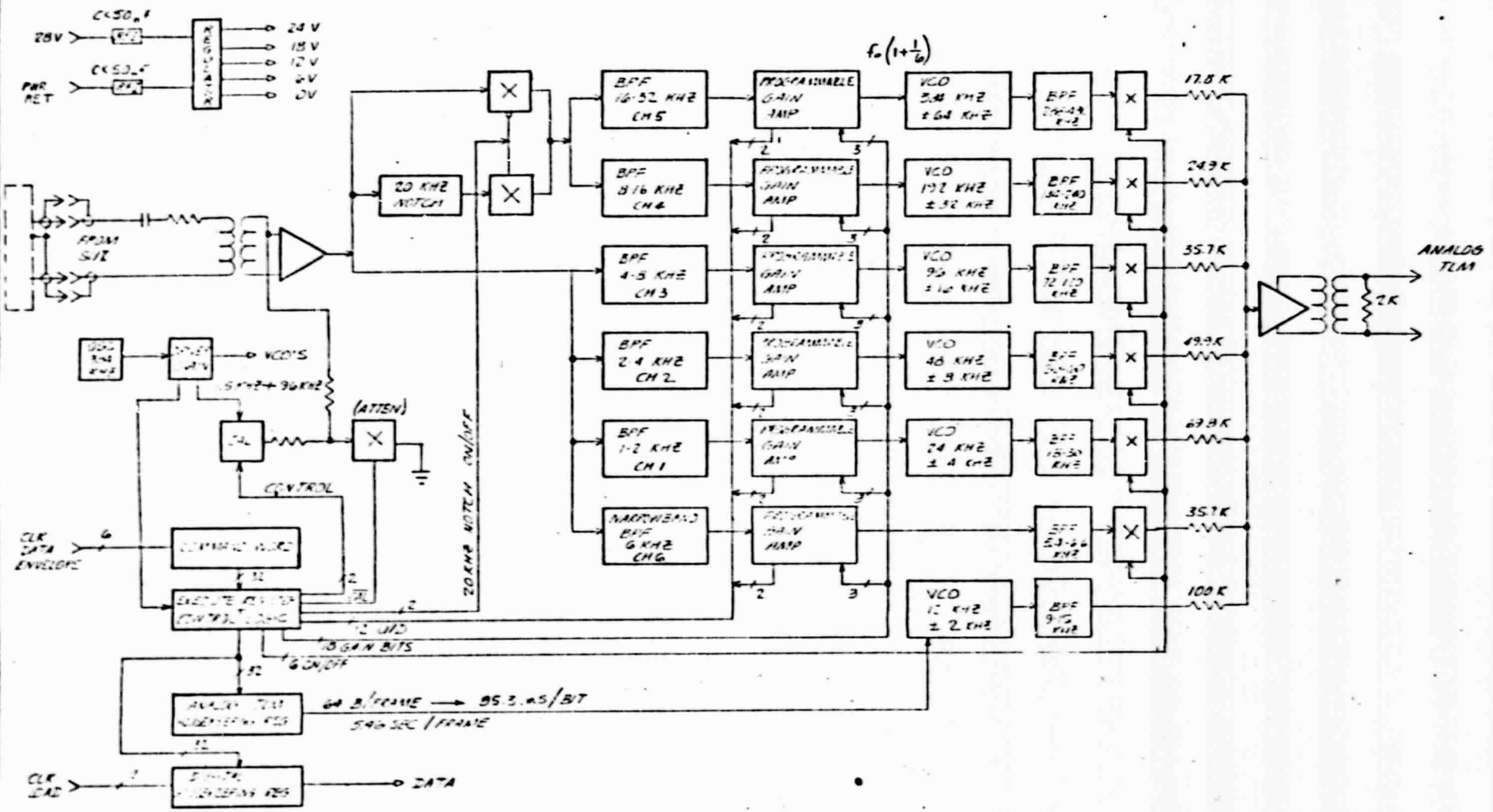
SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

DEVELCO INC.

TITLE [illegible]

SIZE	CODE IDENT NO.	DWG NO.	REV
D	30002	[illegible]	-

REVISIONS					
SYM	DATE	DESCRIPTION	CHD	APPR	DATE
A	[illegible]	PRODUCTION RELEASE			



USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

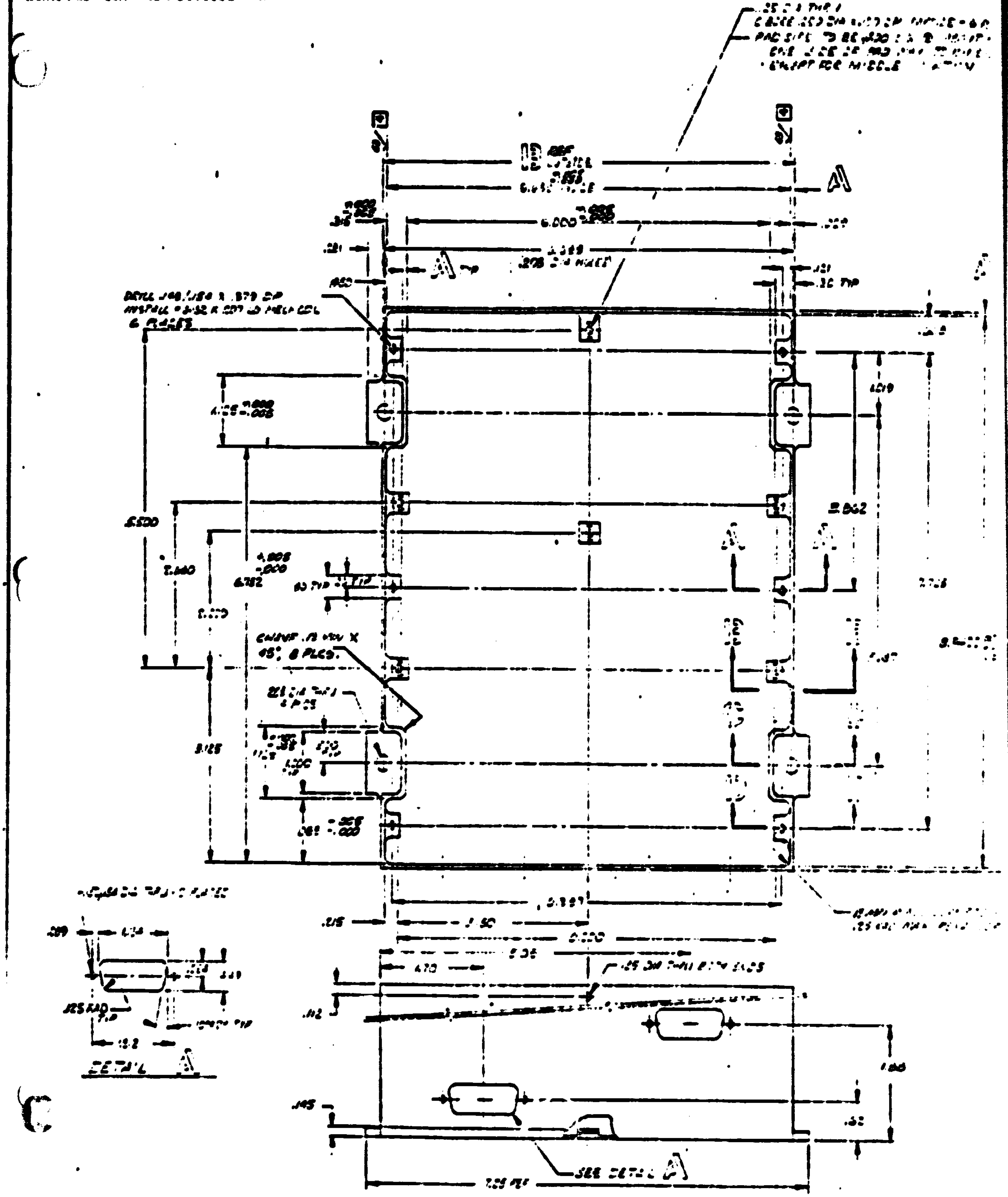
SIGN OFF	INITIALS	DATE
DRAWN	[illegible]	[illegible]
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

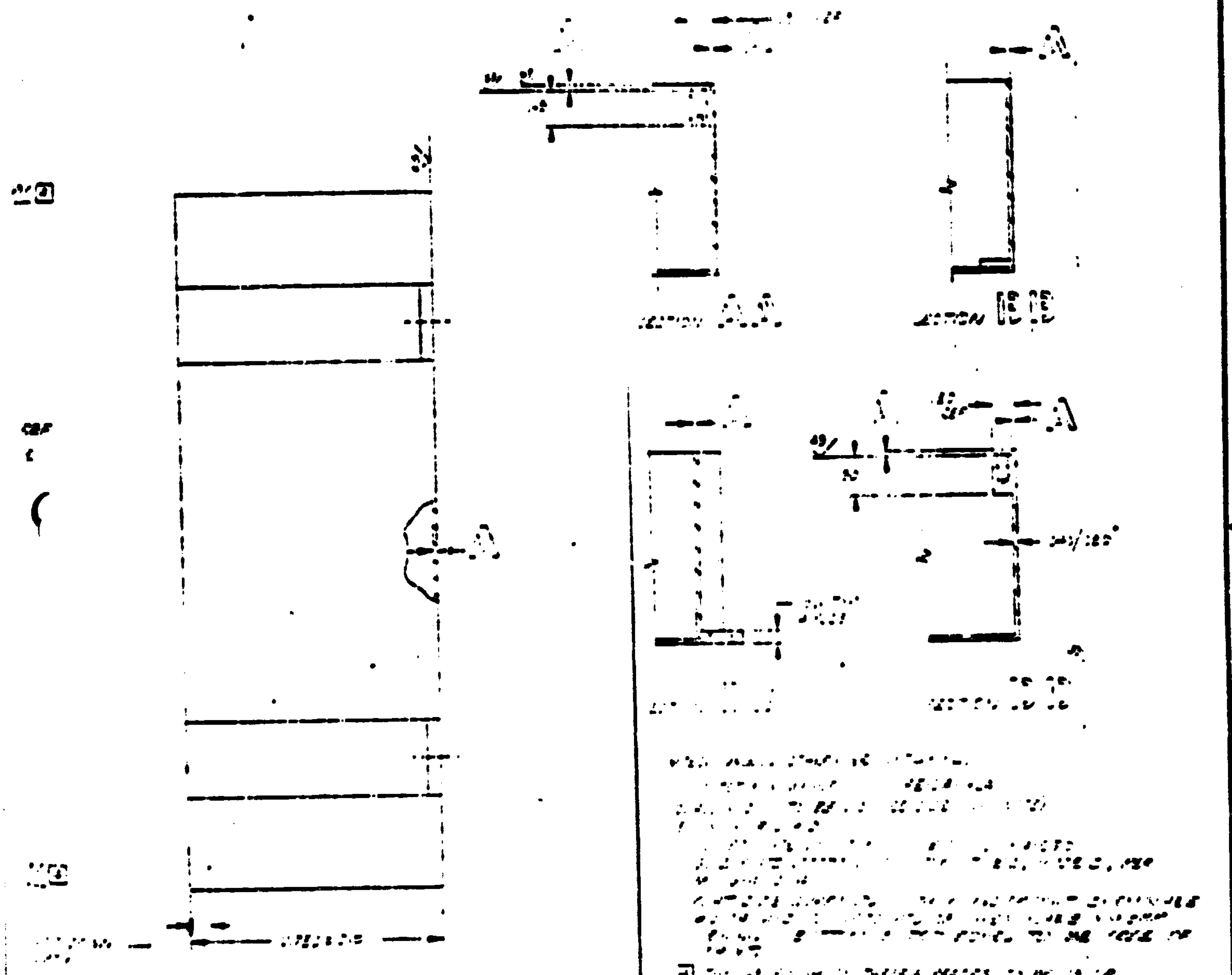
TITLE: VLF RECEIVER BLOCK DIAGRAM

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	100013.	A

SCALE — DO NOT SCALE DRAWING SHEET 1 OF 1


6.000
6 PLACES
CHAMF .15 MAX X
45°, 8 PLCS.
DETAIL A
SEE DETAIL A
7.25 REF

REVISIONS



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USED ON	NEXT ASSY
APPLICATION	

DEVELCO INC.

D 30002

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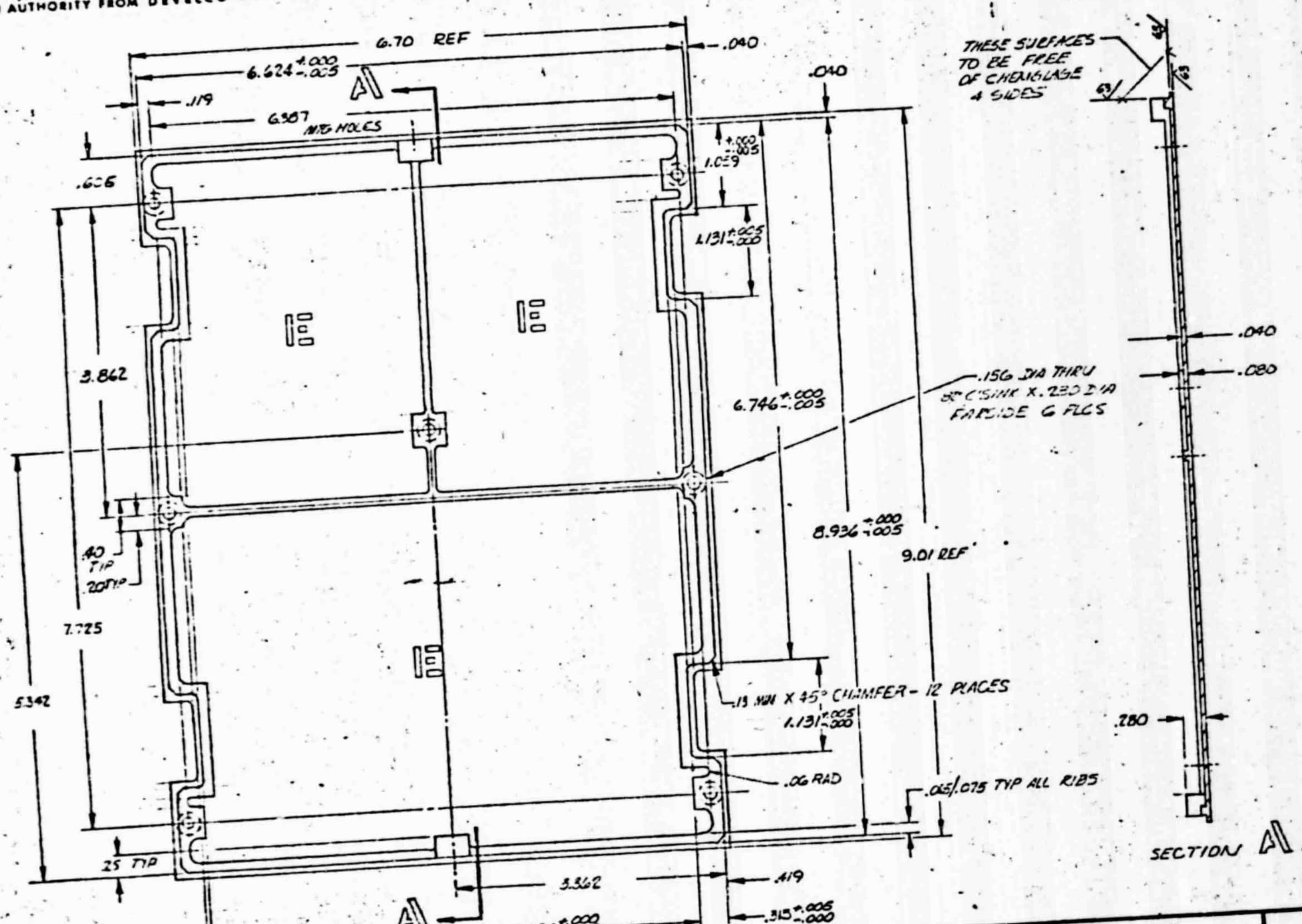
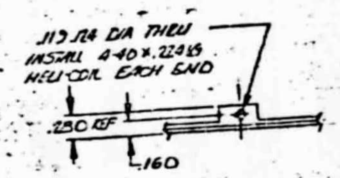
REVISIONS						
SYM	DATE	DESCRIPTION		CAD	APPR	DATE
A	12-16-75	CORRECTED FINISH NOTE	RL			
B	1-12-76	UP DATE DWG				
C	1-26-76	ADDED ENGRAVING INFO SH 2				
D	4-23-76	REDESIGN PER ECO 1676				





NOTES: (UNLESS OTHERWISE SPECIFIED)

1. MATERIAL: MAGNESIUM ZE10A-H24
2. FINISH: ZIC AID
   COPPER PLATE .001 THK MIN PER MIL-C-14-550
   GOLD PLATE CLASS 0 .00002/.00005 THK TYPE 2 GRADE C PER MIL-G-45204.
   SURFACES MARKED 'E' AND FARSIDE TO HAVE ONE COAT CHEMGLAZE + 9924, TWO COATS CHEMGLAZE + Z306.
   REFER TO SHEET TWO (2) FOR MASKING INFO.
3. ALL RADII TO BE .13.

SEE NOTE 1

SEE NOTE 2

USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

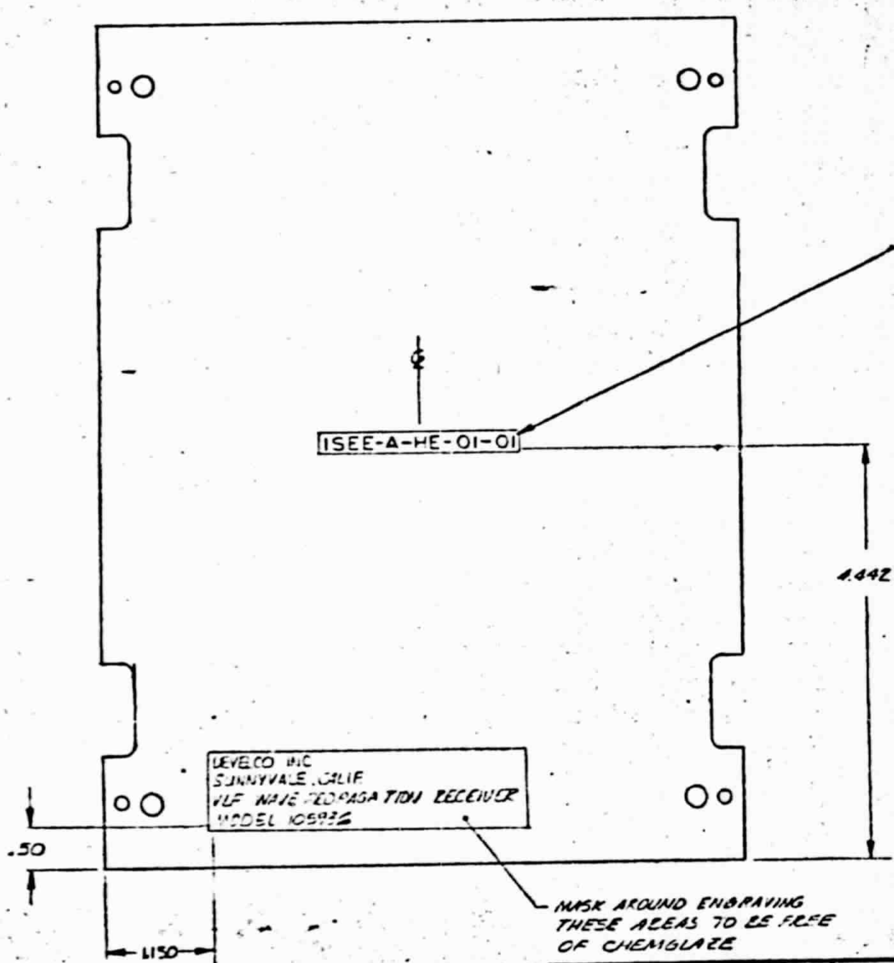
SIGN-OFF	INITIALS	DATE
DRAWN		
CHECKED		1-20-76
APPROVED		
ENGINEER		1/21/76
PROJ ENGR		

DEVELCO INC.

TITLE: COVER, HOUSING STANFORD

SIZE	CODE IDENT NO	DRW NO	REV
C		3-105935	D
SCALE 1/1		DO NOT SCALE DRAWING	SHEET 1 OF 2

SYM	DATE	REVISIONS DESCRIPTION	CKD	APPR	DATE



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL CHARACTERS TO BE 8 POINT GORTON NORMAL, CENTERED ABOUT ℄ AT DIM SHOWN.
   ENGRAVING TO BE .010 MAX DP.
2. BLACK EPOXY FILL ALL CHARACTERS.

USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN	MGM	1-26-76
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE: COVER HOUSING ENGRAVING INFO STANFORD

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	3-105935	—
SCALE		DO NOT SCALE DRAWING	SHEET 2 OF 2

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.					
1	RNC50H1003FS	RESISTOR 1/20W 1% 100K	R67, 68, 69	3					
2	RNC55H4993FS	1/8W 499K	R78*	6					
3	RNC65H6043FS	1/4W 604K	R79*	6					
4	RNC50H1242FS	1/20W 12.4K	R80*	6					
5	RNC50H6982FS	1/20W 1% 69.8K	R81*	6					
6									
7									
8	RJ526BW104	VARIABLE 100K	R65	1					
9									
10	RCR07G226JS	1/4W 5% 22MΩ	R82*, R72*	12					
11	RCR05G301JS	1/8W 300Ω	R70	1					
12	471	470Ω	R94	1					
13	124	120K	R74*, 75*	12					
14									
15	123	12K	R71*, 83*	12					
16	563	56K	R76*, 77*	12					
17	275	2.7M	R84*, 85*	12					
18	393	39K	R86*, 87*	12					
19	RCR05G103JS	RESISTOR 1/8W 5% 10K	R73*	6					
20									
21	CKR05BX104K-1593	CAPACITOR CERAMIC .1uf	C63*	6					
22	CSR13F226K-3026	TANTALUM 22uf 35V	C61	1					
23	F685K-3024	6.8uf 35V	C55, 66	2					
24	C475K-2974	4.7uf 10V	C62*	6					
25	C396K-2979	39uf 10V	C64*	6					
26	D186K-2990	18uf 15V	C49 - 53	5					
27	CSR13D566K-2993	TANTALUM 56uf 15V	C57 - 60	4					
28	CKR05BX101K-1229	CERAMIC 100pf	C54 - 56	3					
29	CKR05BX473K-1587	CAPACITOR " .047uf/100V	C46	1					
30	CSR13G475K-3088	CAPACITOR, TANTALUM 4.7uf 50V	C42, 43	2					
31									
32									
33									

REV.	
A	ENG UP-DATE 10-15-75
B	11-24-75 ENG UP-DATE PRODUCTION RELEASE
D	PRODUCTION RELEASE 1-23-76
E	ECO 1630
F	ECO 1896 7-13-76

NEXT ASSY

USED ON

BY AKM 10-15-75 CK.

APR. APR.

TITLE POWER SUPPLY THRESHOLD DETECTOR

PARTS LIST NUMBER REV

P/L 105899 F

SHEET 1 OF 2

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO					
34	M38510/10104 BHC OR BHA	INTERGRATED CIRCUIT LM108		A12-14	3					
36	JANTX 2N2484	TRANSISTOR 2N2484		Q4,5	2					
37	2N2605	2N2605		Q6,Q7,8,9*	19					
38	2N3700	2N3700		Q3	1					
39	JANTX 2N2920	TRANSISTOR 2N2920		Q10*,11*	12					
40										
41										
42	JANTX 1N3614	DIODE 1N3614		CR6,8	2					
43	JANTX 1N4153	1N4153		CR10*,11,12*	18					
44	JANTXV1N4115	1N4115 22V		CR9	1					
45	1N5297	DIODE 1N5297		CR7	1					
46										
47	—	BUY TO MOTROLA #								
48		M04BARB04208A								
49										
50										
51		* ITEMS QTY = 6								
52										
53										
54	LT10K096	INDUCTOR 1mH		L1,2	2					
56	105899	ASSY	C1		R					
57	105899	FAB	C3		1					
58	105899	ARTWORK	D4		R					
59	105899	SCHEMATIC	D6		R					
60		TERMINAL H.H. SMITH 2033B			28					

REV | NEXT ASS'Y | USED ON

BY MMM10455 CK.

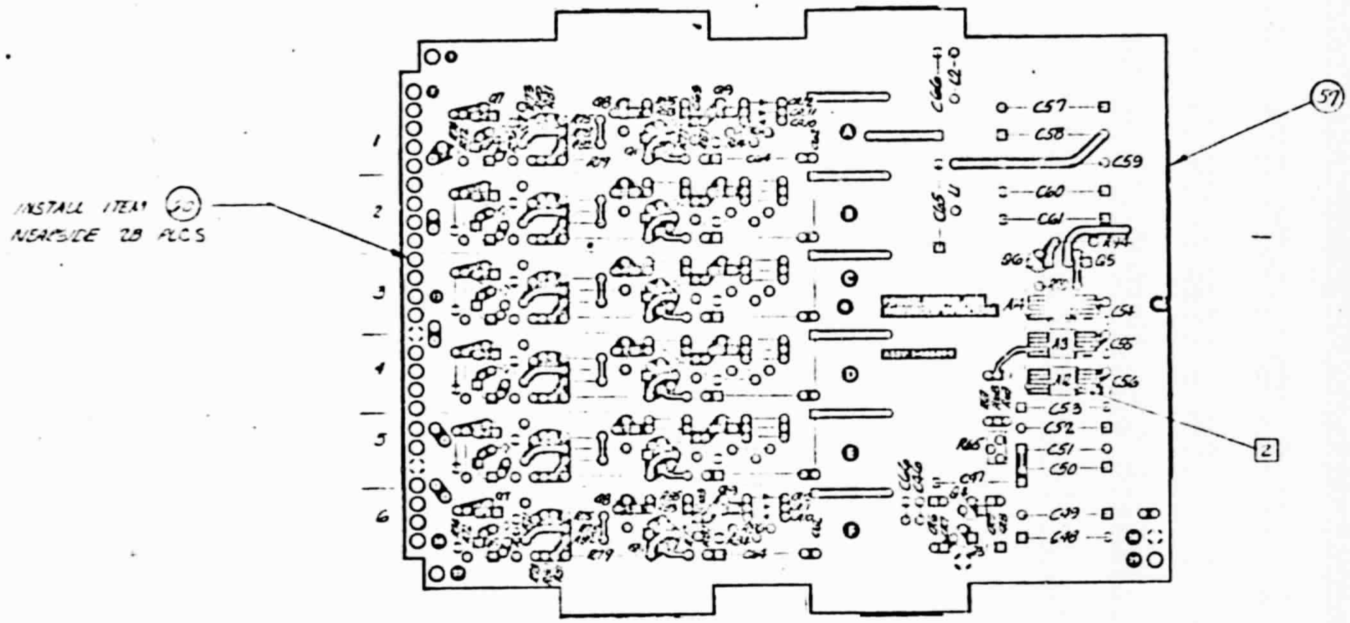
APR. APR.

TITLE POWER SUPPLY THRESHOLD DETECTOR

PARTS LIST NUMBER P/L 105899 REV F

SHEET 2 OF 2

REVISIONS					
SYM	DATE	DESCRIPTION	CKD	APPR	DATE



NOTE:
1. THIS BOARD HAS SIX (6) REPEAT CIRCUITS ALL COMPONENTS WITHIN THESE AREAS LOAD THE SAME.

2. A14, A13, A12 MUST HAVE MYLAR PLACED UNDER BODY TO PREVENT SHORTS.

CONVERTED	PC 105936	1
USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN	A.E.W	4.12.76
CHECKED		
APPROVED		
ENGINEER	AJ	4/17/76
PROJ ENGR		

DEVELCO INC.

TITLE: POWER SUPPLY THRESHOLD DETECTORS

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	1-105399	

SCALE FULL | DO NOT SCALE DRAWING | SHEET 1 OF 1

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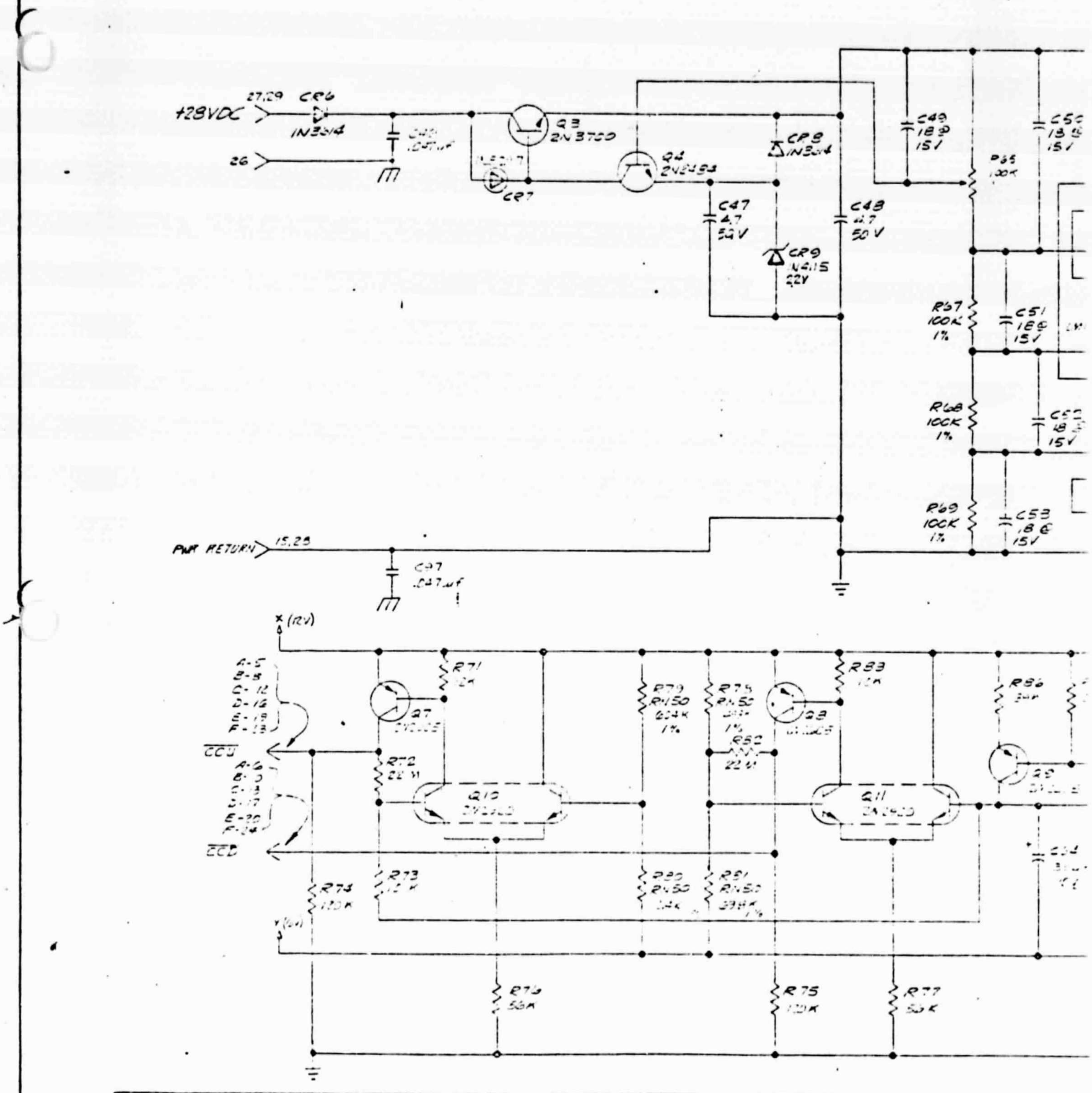
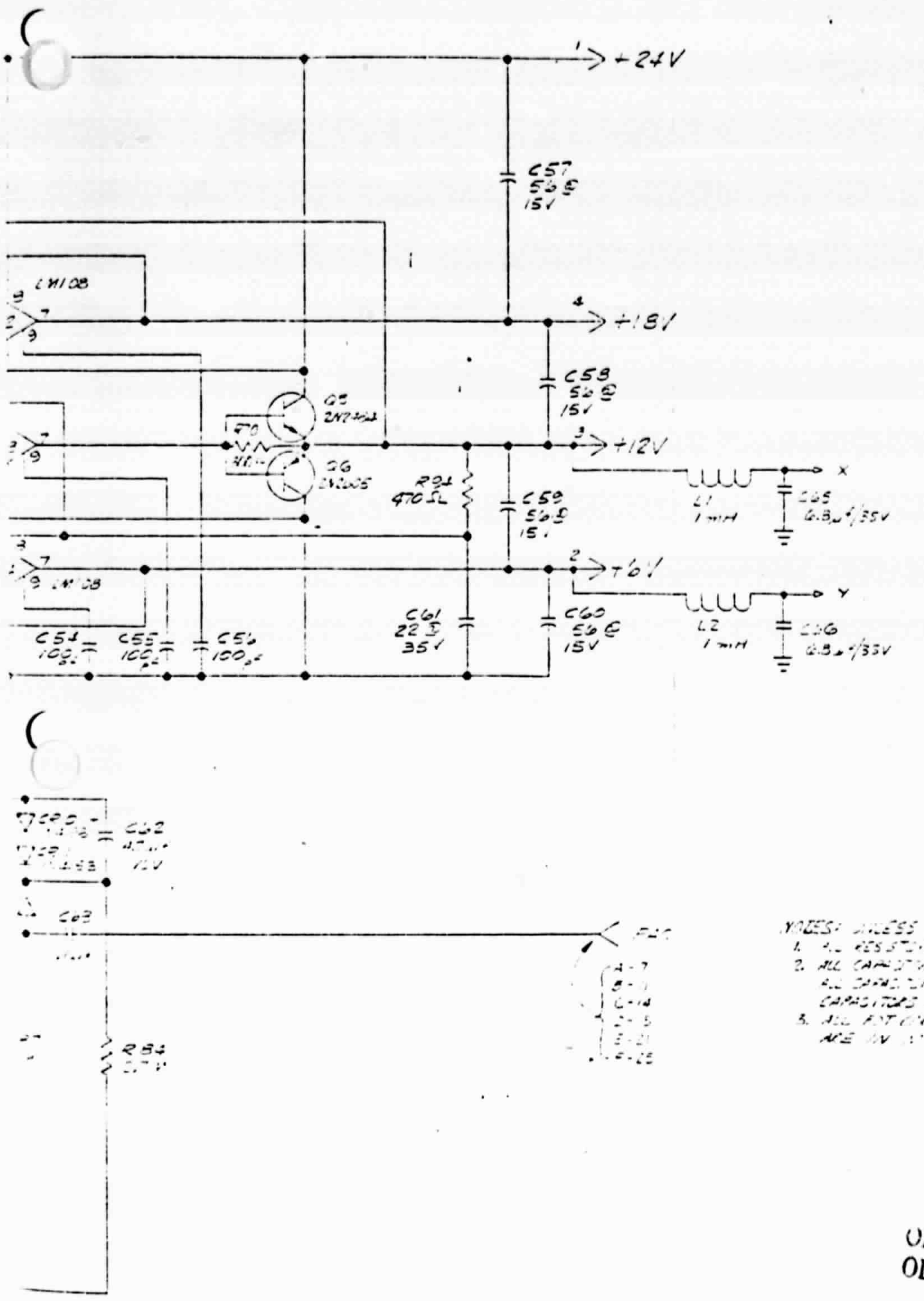


REF	R71	R72	R73	R74	R75	R76	R77	R78	R79	R80	R81	R82	R83	R84	R85	R86	R87	Q7	Q8	Q9	Q10	Q11	[illegible]
A	12K	22K	10K	120K	120K	56K	56K	[illegible]	[illegible]	[illegible]	[illegible]	22K	12K	[illegible]	[illegible]	39K	39K	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
B																							
C																							
D																							
E																							
F	12K	22K	10K	120K	120K	56K	56K	[illegible]	[illegible]	124K	[illegible]	22K	12K	2.7M	[illegible]	39K	39K	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

SYM	DATE	REVISIONS DESCRIPTION	DRW	CKD	APPR	DATE
C	[illegible]	[illegible]				
D	[illegible]	[illegible]				



NOTES: UNLESS OTHERWISE SPECIFIED.
1. [illegible] OHMS.
2. ALL CAPACITORS [illegible] PICOFARADS. [illegible] CAPACITORS ARE OF THE [illegible] SERIES.
3. [illegible]

ORIGINAL PAGE IS OF POOR QUALITY

USED ON	NEXT ASSY	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

DEVELCO INC.

TITLE [illegible]

SIZE	CODE IDENT NO	DWG NO	REV
D	30002	[illegible]	D

SCALE DO NOT SCALE DRAWING SHEET OF

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.
1	RCR05G203JS	RESISTOR 1/8 W 5 % 20K Ω	R1, R19	2
[illegible]	RNC50H2212FS	1/20 W 1 % 22.1K	R3	1
3	RCR05G302JS	1/8 W 5 % 3K	R8, R10-12, 25, 26	6
4	RCR05G332JS	1/8 W 5 % 3.3K	R9	1
5	RNC50H4642FS	1/20 W 1 % 46.4K	R7	1
6	RCR50G331JS	1/8 W 5 % 330	R17, 2	2
7	RCR05G204JS	1/8 W 5 % 200K	R6	1
8	RCR05G511JS	1/8 W 5 % 510	R27	1
9	RCR05G200JS	1/8 W 5 % 20	R14, R15	2
10	152JS	1/8 W 5 % 1.5K	R13	1
11	301JS	1/8 W 5 % 300	R5	1
12	153JS	1/8 W 5 % 15K	R4	1
13	103JS	1/8 W 5 % 10K	R20	1
14	393JS	1/8 W 5 % 39K	R18	1
15	RCR05G682JS	RESISTOR-1/8 W 5 % 6.8K Ω	R16, R24	2
16	D51C103 FSA	CAPACITOR .01 µf 100V	C42, 61, 63	3
17	102	.001	C28, 81	2
18	273	.027	C45, 86	2
[illegible]	223	.022	C68	1
[illegible]	183	.018	C55	1
21	123	.012	C15, 85	2
22	203	.020	C74	1
23	333	.033	C76	1
24	272	.0027	C29	1
25				
26	122	.0012	C16, 22, 43, 51	4
27	222	.0022	C23, 33	2
28	562	.0056	C40	1
29	472	.0047	C37	1
30	182	.0018	C46	1
31	502	.005	C48	1
32	822	.0082	C50	1
33	D51C392 FSA	CAPACITOR .0039 µf 100V	C44	1

REV B — ECO #1895 JL 7-13-76

NEXT ASS'Y

USED ON

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BY R.C. 3-26-76 CK. [illegible] 3-30-76

APR. [illegible] 4/6/76 APR.

TITLE INPUT AMP & BANDPASS FILTER

PARTS LIST NUMBER P/L 6-105937 REV B

SHEET 1 OF 3

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.
34	D51C474 FSA	CAPACITOR .47 uf 100V	C84	1
[illegible]	CKR05BX104-1593	CAPACITOR .1 uf 100V	C7,78	2
36	CKR05BX103K-1575	CAPACITOR .01 uf 50V	C1, 2, 5	3
37	CSR13F685K-3024	CAPACITOR 6.8 uf 35V	C12, 67	2
38				
39	633063-A1121-H9	CAPACITOR 120 pf	C4	1
40	A1911	910	C32	1
41	A1200	20	C41	1
42	A1821	820	C54	1
43	A1301	300	C39	1
44	633063-A1560-H9	CAPACITOR 56 pf	C83	1
45	CKR06BX105K-1419	CAPACITOR 1uf	C13	1
46		SELECT AT TEST CAPACITORS	C47, C49	2
47				
48	CD4016AK/IN*-OR-	INTEGRATED CKT. CD4016	U1	1
49	CD4016AK/IN			
50				
51	47-101228-01	POT CORE 6.7 MH	T1	1
[illegible]	269	22.49	T2	1
53	266	42.13	T3	1
54	231	74.45	T4	1
55	263	316.6	T5	1
56	260	383.3	T6	1
57	234	1.46	T7	1
58	267	41.44	L5	1
59	268	41.24	L6	1
60	264	73.29	L8	1
61	265	89.95	L9	1
62	240-01	151.4	L10	1
63	241-01	105.4	L11	1
64	241-02	107	L12	1
65	261-01	175.9	L14	1
66	47-101262-01	POT CORE 316.6 MH	L15	1

REV | NEXT ASS'Y | USED ON

BY R.C. | CK.

APR. | APR.

TITLE INPUT AMP & BANDPASS FILTER

PARTS LIST NUMBER P/L 6-105937 | REV B

SHEET 2 OF 3

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
67	47-101258-01	POT CORE 575.6 MH	L17	1					
68	-259	633.2	L18	1					
69	246	727	L19	1					
70	218	4.7	L2	1					
71	47-101248-01	POT CORE 72.2 MH	L3	1					
72									
73									
74	JANTX1N483B	DIODE 1N483B	CR1,2	2					
75									
76									
77	JANTX2N2484	TRANSISTOR 2N2484	Q1,3	2					
78	JANTX2N2605	TRANSITOR 2N2605	Q2,4,7	3					
80	105937	ASSY C1		R					
81	105937	FAB C3		1					
82	105937	ARTWORK D4		R					
83	105937	SCHEMATIC D6		R					
84		TERMINAL HHSMITH 2023B -		22					

REV

NEXT ASS'Y

USED ON

BY R.C. CK.

APR. APR.

TITLE INPUT AMP & BANDPASS FILTER

PARTS LIST NUMBER P/L 6-105937 REV B

SHEET 3 OF 3

DEVELCO, INC.

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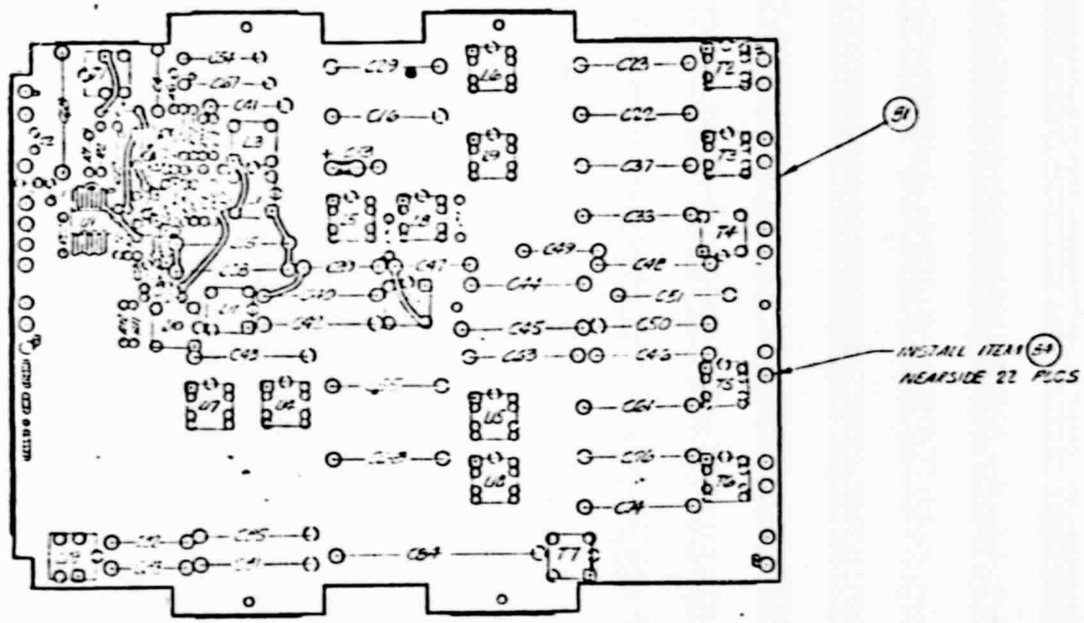
REVISIONS					
SYM	DATE	DESCRIPTION	CKD	APPR	DATE



1-…-…	2-105936	1
USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

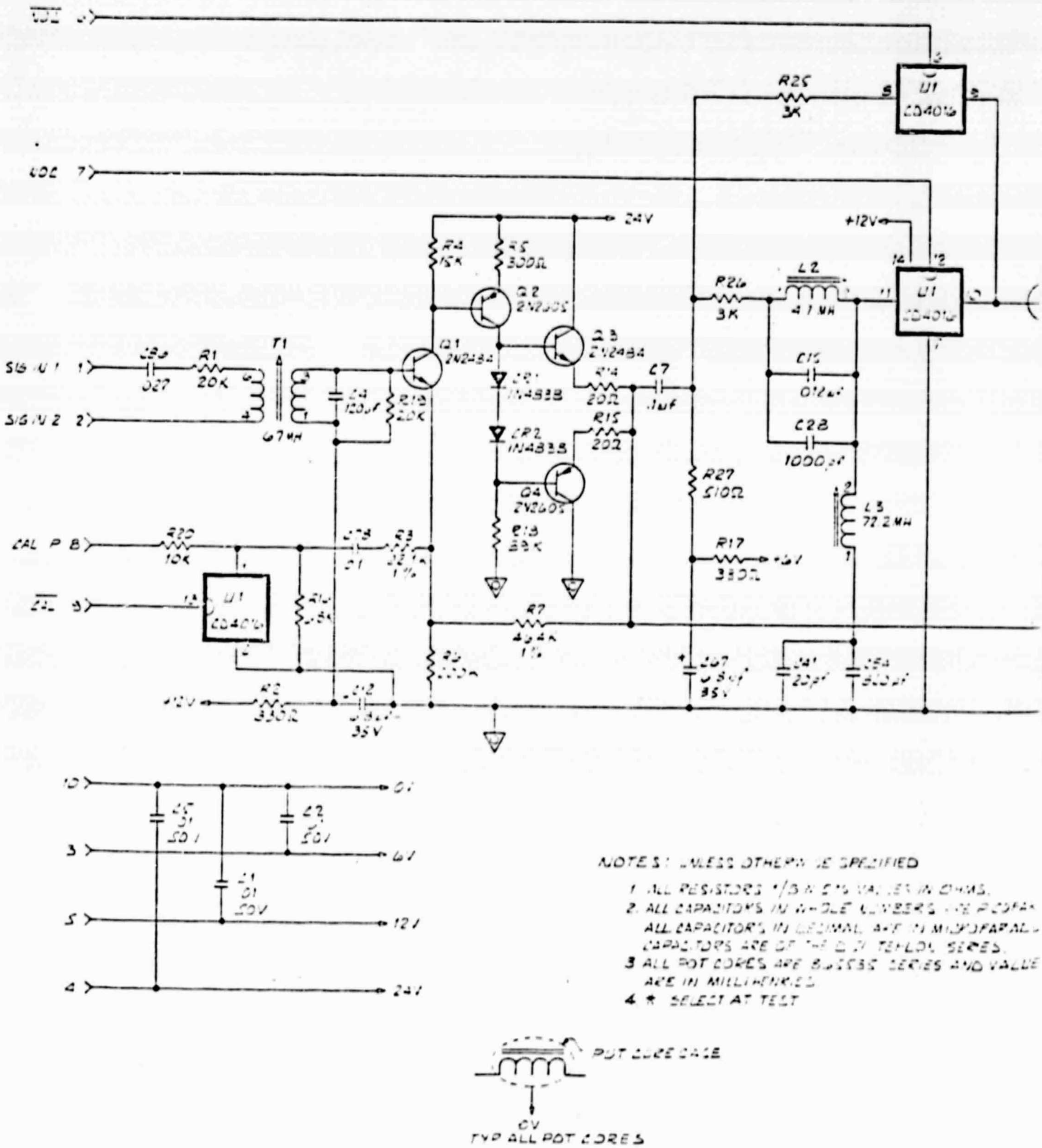
SIGN OFF	INITIALS	DATE
DRAWN	[illegible]	4-12-7…
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE: INPUT AMP BD

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	1-105937	—

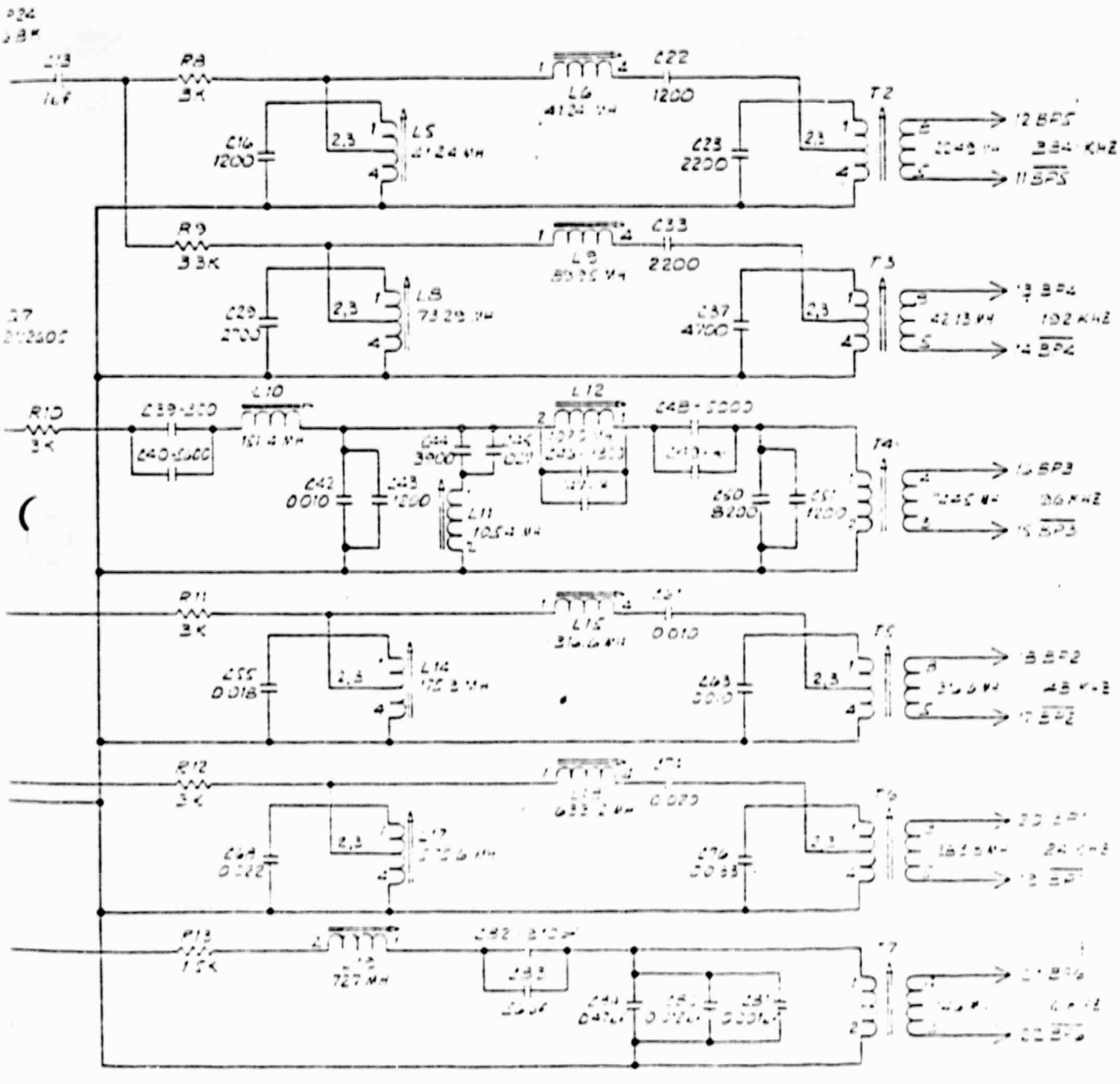
SCALE 1:1 | DO NOT SCALE DRAWING | SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS 1/8 W 5% VALUES IN OHMS.
2. ALL CAPACITORS IN WHOLE NUMBERS ARE PICOFARADS. ALL CAPACITORS IN DECIMAL ARE IN MICROFARADS. CAPACITORS ARE OF THE D.M. TEFLON SERIES.
3. ALL POT CORES ARE B65535 SERIES AND VALUE ARE IN MILLIHENRIES.
4. * SELECT AT TEST

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CHD	APPR	DATE



USED ON	NEXT ASSY	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

DEVELCO INC.

TITLE INPUT AMP BANDPASS FILTER

SIZE CODE IDENT NO DWG NO REV

D 30002

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO.					
1	RCR05G 102 JS	RESISTOR 1/8 W 5%	1K	R3–15	13					
2	622 JS		6.2 K	R37,38	2					
3	103 JS		10K	R29-34	6					
4	153 JS		15 K	R41	1					
5	303 JS		30K	R40	1					
6	332 JS		3.3 K	R35,36	2					
7	104 JS		100 K	R1,2,24-28	7					
8	105 JS		1M Ω	R16-23	8					
9	RCR05G 101JS	RESISTOR 1/8W 5%	100 Ω	R39	1					
10										
11										
12		TERMINAL H.H. SMITH 2023B			75				–	
13										
14	JANTX2N2484	TRANSISTOR	2N2484	Q9-16	8					
15	2N5116 PER	TRANSISTOR	2N5116	Q1-8	8					
16	MIL-S-19500/476									
17										
18										
19										
20	CSR13F226K3026	CAPACITOR TANTALUM	22µf/35V	C2	1					
21	CKR05BX473K-1587	" CERAMIC	.047µf/50V	C3	1					
22	CKR06BX105K-1419	" "	1µf/50V	C1	1					
23	CKR05 BX103K-1575	" "	.01µf/100V	C4-30	27					
24										
25										
26										
27										
28										
29										
30	JANTX1N754A	DIODE ZENER 6.8V 1N754A		CR2 & 3	2					
31	JANTXV1N964B	13V 1N964B		CR1	1					
32										
33										

REV	
A	ENG UP DATE
B	PRODUCTION RELEASE 11-24-75
C	PRODUCTION RELEASE
D	ECO 1031 MOD by 4/1/76

NEXT ASS'Y

USED ON

BY NHN 8-21-75	CK.
APR.	APR. [illegible] 1/12/7[illegible]
TITLE DIGITAL COMMAND LINK	
PARTS LIST NUMBER P/L 6-105892	REV D
SHEET 1 OF 2	

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
34	LT10K096	INDUCTOR 1 MH	L1	1					
36									
37									
38									
39	M38510/05202ADC	INTERGRATED CIRCUIT CD4001AK	U24	1					
40	05001ADC	CD4011AK	U8,25,18,27,19,42,39,21	8					
41	05101ADC	ADC COULD BE ADA CD4013AK	U13,36,1	3					
42	05601AFC	AFC COULD BE AFA CD4017AK	U23,15,26	3					
43	05704AFC	CD4021AK	U11,12,6,7,29,30,34,35	8					
44	M38510/05003ADC	CD4023AK	U16	1					
45	CD4029AK/IN*	CD4029AK	U3,10,4,22,33,40	6					
46	CD4034AK/IN*	-OR- W/O* CD4034AK	U2,3,37,38	4					
47	CD4040AK/IN*	CD4040AK	U14	1					
48	CD4042AK/IN*	CD4042AK	U5,20,28,41	4					
49	M38510/05503AFC	AFC COULD BE CD4049AK	U31,17	2					
50	M38510/05504AFC	AFA -- CD4050AK	U22	1					
55	105892	ASSY C1		R					
56	105892	FAB C3		1					
57	105892	ARTWORK D4		R					
58	105892	SCHEMATIC D6		R					

REV	NEXT ASS'Y	USED ON

BY FAKN 8-21-75 CK.
APR. APR.
TITLE DIGITAL COMMAND LINK

PARTS LIST NUMBER P/L 6-105892 REV D

SHEET 2 OF 2

DEVELOP INC

REVISIONS					
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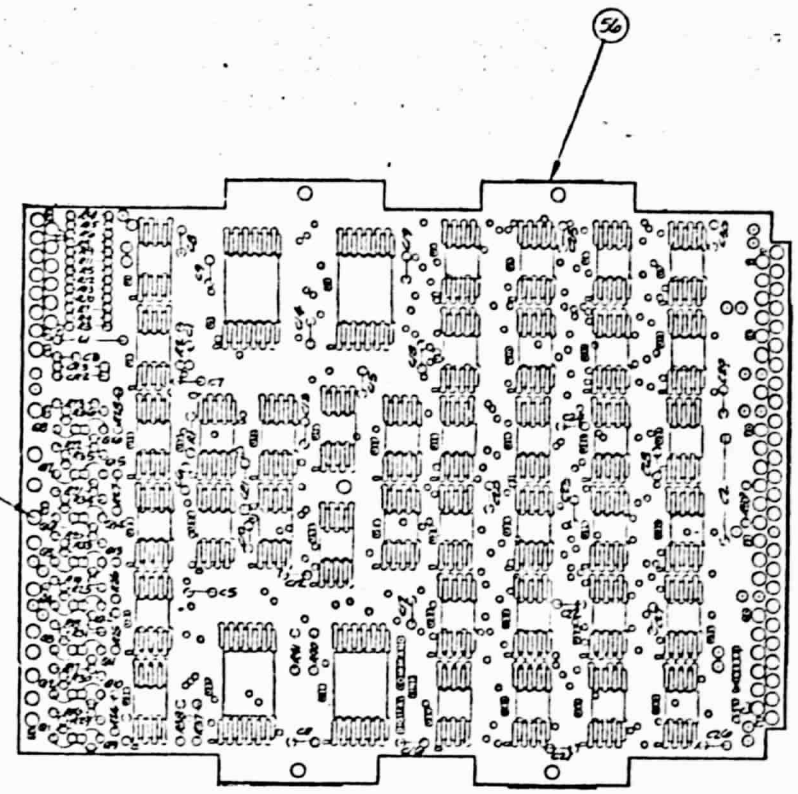

2044700	PL 105136	1
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APPLICATION		

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DRAWN	[illegible]	4 12 76
CHECKED		
APPROVED		
ENGINEER	RJ	1/14/76
PROJ ENGR		

DEVELCO INC.

TITLE: DIGITAL COMMAND LINK

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	7-105892	—

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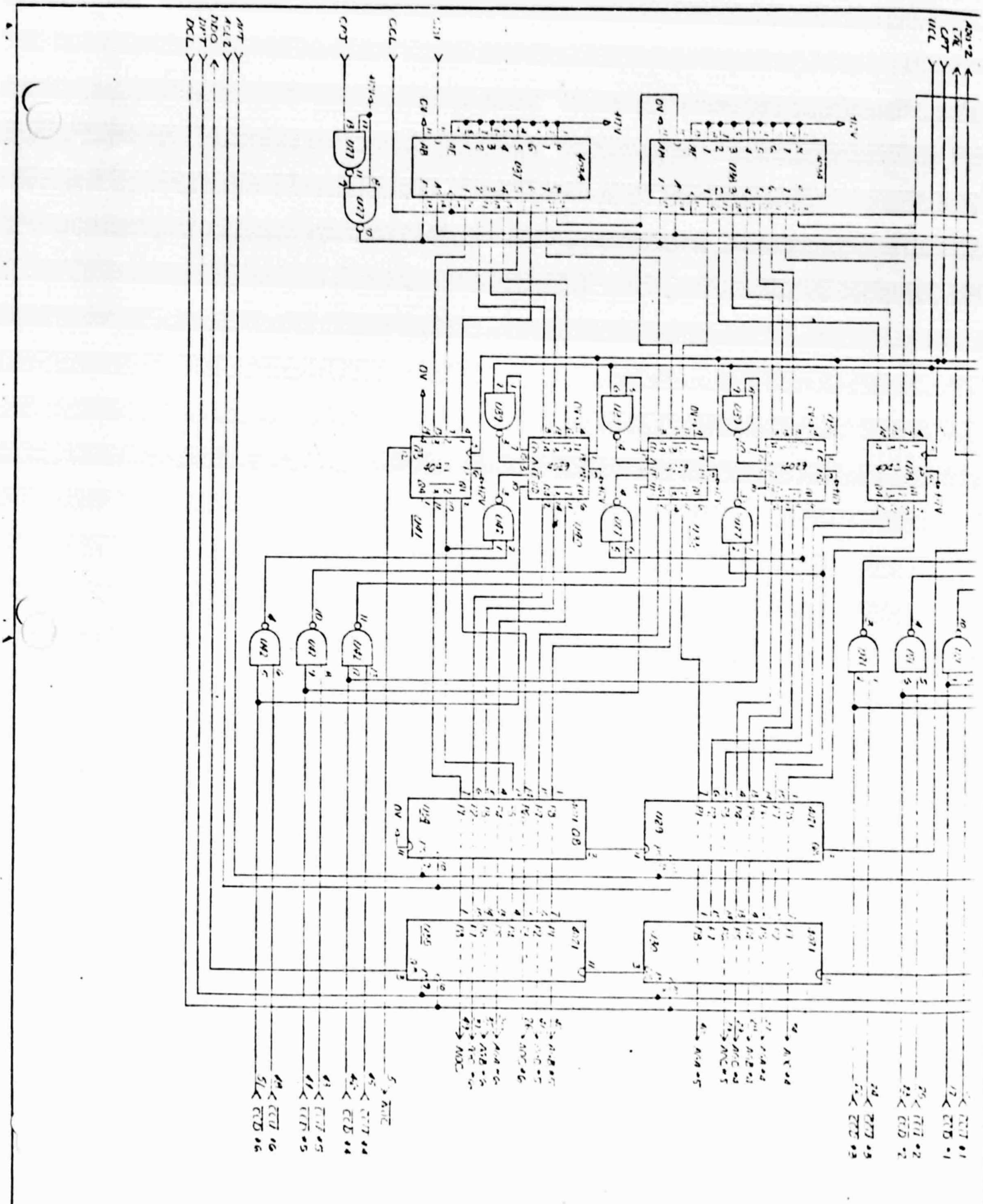

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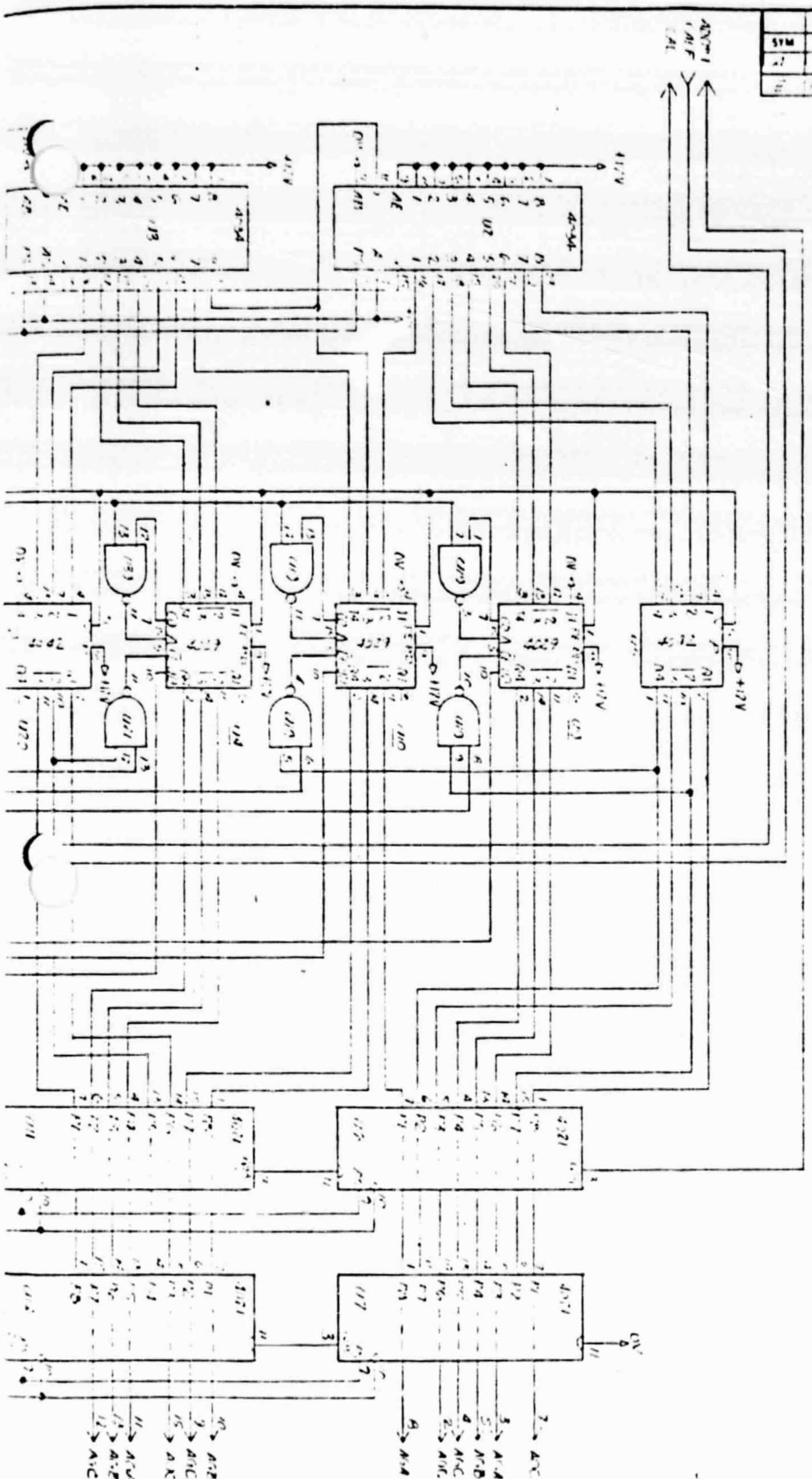
E	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]



USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN	[illegible]	
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE

SIZE	CODE IDENT NO	DWG NO	REV
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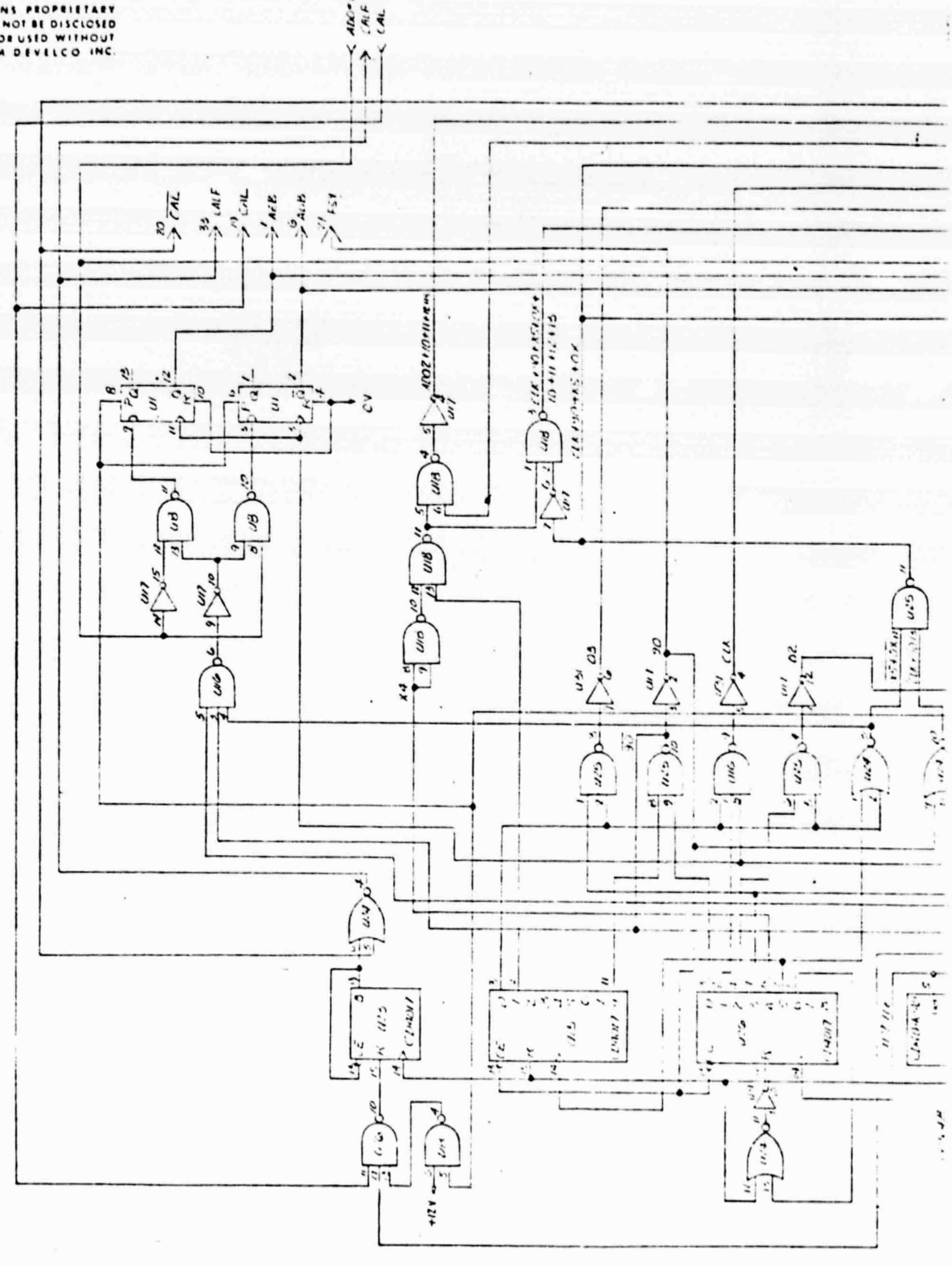
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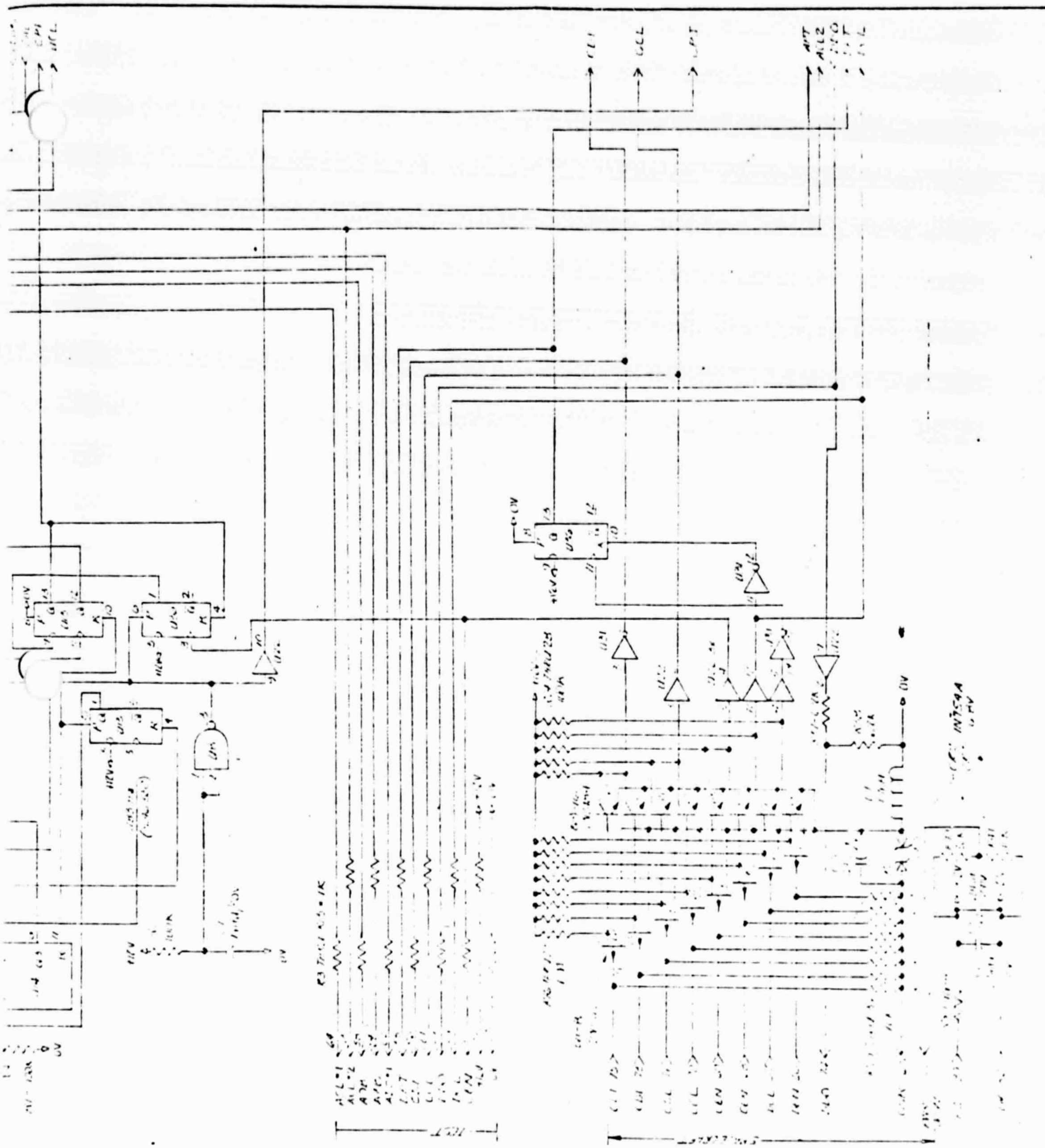
+12V



USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

DEVELCO INC.

TITLE

CONTROL LOGIC

SIZE	CODE IDENT NO	DWG NO	REV
D	30002	[illegible]	E

SCALE | DO NOT SCALE DRAWING | SHEET [illegible]

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO. 1
[illegible]	RCR05G-511JS	RESISTOR 1/8W 5% 510 Ω	1 CHANNEL C ONLY	1
[illegible]				
3	513JS	51K	3	12
4	564JS	560K	5	[illegible]
5				
6	823JS	82K	7	24
7	RCR05G 512JS	5.1K	8	24
8	RNC50H3920FS	1/20W 1% 392	12	6
9	RCR05G 433JS	RESISTOR 1/8W 5% 43K	13	24
10	273JS	27K	14	12
11	104JS	100K	15	6
12	RCR05G202JS	2K	1 CHAN F ONLY	1
13	RNC50H 1272 FS	RESISTOR 1/20W 1% 12.7K	10	[illegible]
14	RNC50H 2491 FS	RESISTOR 1/10W 1% 2.49K	9	12
15				
16	RNC50H3012FS	RESISTOR 1/20W 1% 30.1K Ω	4	24
17	RNC50H 1472FS	RESISTOR 1/20W 1% 14.7K Ω	11, 17	48
18				
[illegible]	RCR05G153JS	RESISTOR 1/8W 5% 15K	16	6
20				
21		TERMINAL H.H. SMITH 2023 B		40
22				
23		—		
24	JANTX2N2920	TRANSISTOR 2N2920	[illegible]	36
25	JANTX2N2484	TRANSISTOR 2N2484	25	48
26				
27				
28	CD4046AK/LN*	INTERGRATED CIRCUIT CD4046AK	30	6
29	-OR- W/O*			
30	D6-105927	SCHEMATIC		R
31	C1-105929	ASSY DWG		R
32	C3-105929	FAB DWG		1
33	D4-105929	ARTWORK		R

REV	
A	UP-DATE PER ENG.
B	ENG UP-DATE 10-15-75
C	~~PRODUCTION RELEASE~~
D	PRODUCTION RELEASE [illegible]
E	ECO# 1617 MGM
F	ECO 1938 JKL 2-13-76 [illegible]

NEXT ASS'Y | USED ON

BY MGM 3-10-75 CK.

APR. APR. [illegible]

TITLE PROGRAMMABLE GAIN AMP.

PARTS LIST NUMBER P/L 6-105929 REV F

SHEET 1 OF 2

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO. 1
34	CSR13D686K-2994	CAPACITOR TANTALUM 68 uH/15V	37	6
	CSR13F476K-3032	" " 47 uH/35V	36	6
3.	CKR05BX470K-1333	CAPACITOR 47 pf	39	6
37	CKR05BX151K-1342	" 150pf	38	6
38	CKR06BX224K-1356	CAPACITOR CERAMIC .22uf/50V	34	6
39	CKR06BX105K-1419	" " 1uf/50V	35	18
40				
41				
42	LT10K227	INDUCTOR 100 uH	44	12
43				
44				
45				
46				
47				
48				
49				
50				

ORIGINAL PAGE IS OF POOR QUALITY

REVI

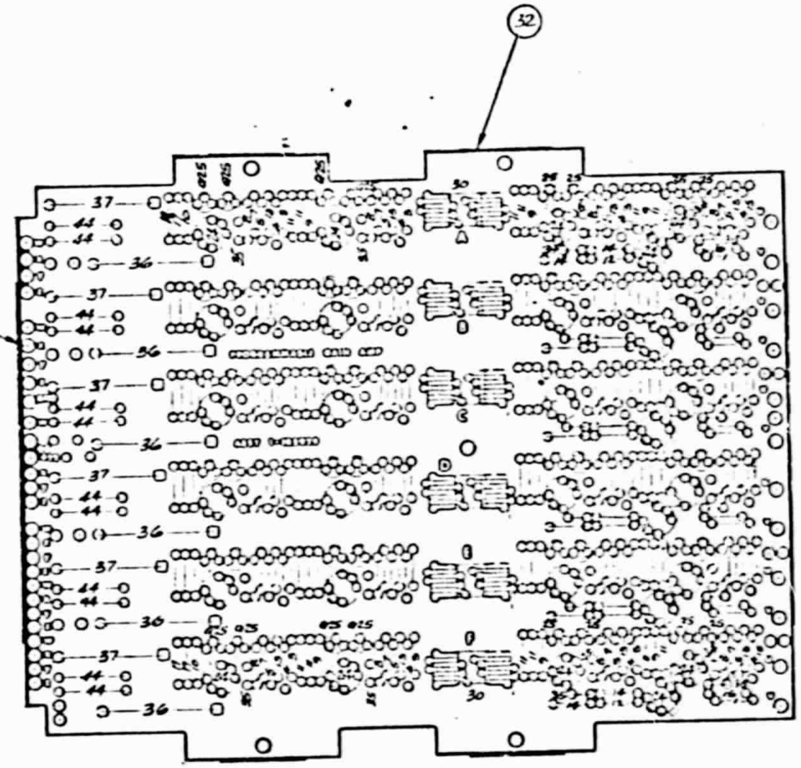
NEXT ASS'Y

USED ON

BY MCM 8-10-75	CK.
APR.	APR.
TITLE PROGRAMMABLE GAIN AMP	
PARTS LIST NUMBER P/L 6-105929	REV F
SHEET 2 OF 2	

DEVELCO, INC.

REVISIONS					
SYM	DATE	DESCRIPTION	CKD	APPR	DATE



NOTE: THIS BOARD HAS SIX (6) REPEAT CIRCUITS. ALL COMPONENTS WITHIN THESE AREAS LOAD THE SAME.

SANRED	PL 105926	1
USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN	AJM	4-12-70
CHECKED		
APPROVED		
ENGINEER		4/14/70
PROJ ENGR		

DEVELCO INC.

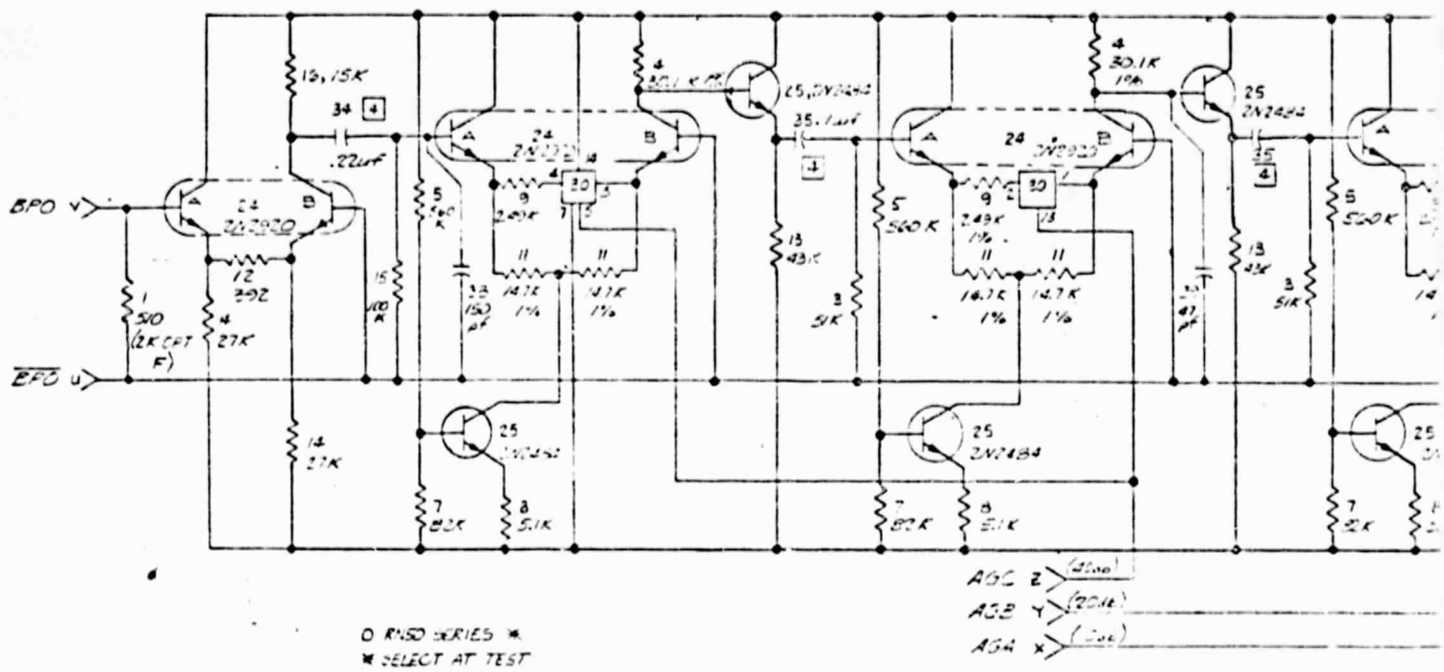
TITLE: PROGRAMMABLE GAIN AMP

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	1-105929	—

SCALE FULL | DO NOT SCALE DRAWING | SHEET 1 OF 1

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS 1/8 W, 5%, VALUES IN OHMS.
2. ALL CAPACITOR VALUES ARE IN µF.
3. [3] CASE SIZE CSR13.
4. [4] CASE SIZE CK05 OR CK06.
5. REF NUMBERS NOT USED 18 [illegible] 31-33, 40-42, 45, 46



O RN50 SERIES *
* SELECT AT TEST

	REF	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CH 1	A	—		51K	30.1K 1%	560K		82K	5.1K	2.49K 1%	[illegible] 1%	[illegible] 1%	[illegible] 1%	43K	27K	100K	15K	14.7K						
2	B	—																						
3	C	510																						
4	D	—																						
5	E	—																						
CH 6	F	2K		51K	30.1K 1%	560K		82K	5.1K	2.49K 1%	[illegible]	[illegible]	[illegible]	43K	27K	100K	15K	14.7K						

	REF	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46
CH 1	A	2N2920	2N2484					CD4066				.22/20V	1/35V	[illegible]	47/35V	[illegible]	[illegible]					[illegible]		
2	B																							
3	C																							
4	D																							
5	E																							
CH 6	F	2N2920	2N2484					CD4066				.22/20V	1/35V	[illegible]	47/35V	[illegible]	47pF					[illegible]		

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO
1	RNC50H6042 FS	RESISTOR 1/10W 1% 60.4K	R1	1
2	6982	69.8K	R2,54	2
3	8062	80.6K	R3,31	2
4	8252	82.5K	R4,5	2
5	RNC50H1003 FS	RESISTOR 1/10W 1% 100K	R26,88	2
6	RNC50H1872 FS	1/10W 1% 18.7K	R97	1
7	RNC50H7501FS	1/10W 1% 7.5K	R93	1
8	RJ-26BW103	VARIABLE 10K	R19	1
9	RJ 26BW503	50K	R23	1
10	RJ 26BW104	100K	R21,R20	2
11	RJ 26BW203	20K	R22	1
12	RJ 26BW254	VARIABLE 250K	R24	1
13	RNC50H2492 FS	RESISTOR 1/10W 1% 24.9K	R27,51	2
14	55H1503	150K	R29	1
15	55H3013	301K	R25,26,32	3
16	50H2211	2.21K	R39,40,41,42,43,44	6
17	2002	20K	R33 THRU R38	6
18	4642	46.4K	R46	1
19	RNC50H4992 FS	1/10W 1% 49.9K	R53	1
20	RCR05G106JS	1/8W 5% 10M	R14 THRU R18 R45	6
21	RNC50H1782FS	1/10W 1% 17.8K	R50	1
22	RNC50H3572FS	" " 35.7K	R52,R95	2
23	RCR05G622JS	1/8W 5% 6.2K	R89	1
24	RCR05G475JS	4.7M	R57	1
25	RCR05G153JS	15K	R58	1
26	RCR05G301JS	300Ω	R59	1
27	RCR05G105JS	1/8W 5% 1M	R56	1
28	RNC50H1501FS	1/10W 1% 1.5K	R60	1
29	RNC50H6191FS	1/20W 1% 6.19K	R96	1
30	RNC55H6042FS	1/10W 1% 60.4K	R30	1
31	RCR05G242JS	1/8W 5% 2.4K	R63,64	2
32	RCR05G103JS	1/10W 5% 10K	R62	1
33	RNC50H4022FS	RESISTOR 1/10W 1% 40.2K	R6 THRU R10	5

REVISIONS	
A	ENG UP-DATE 9-30-75
B	ENG UP DATE 10-15-75
C	11-24-75 ENG UP-DATE ~~PRODUCTION RELEASE~~
D	PRODUCTION RELEASE
E	ECO #1613 MCM 1/14/76
F	ECO #1300 1894 MCM 9/76

NEXT ASS'Y

USED ON

BY MCM 9-19-75 CK.

APR. APR 1/14/76

TITLE VCO & OUTPUT AMPLIFIER

PARTS LIST NUMBER REV

P/L 105930 F

SHEET 1 OF 4

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
34	C1-105930	ASSY DWG		R					
[illegible]	C3-105930	FAB DWG		1					
36	D6-105930	SCHEMATIC		R					
37	D4-105930	ARTWORK		R					
38									
39		TERMINAL H.H. SMITH 2023B		34					
40									
41									
42									
43									
44									
45									
46	RCR05G243JS	RESISTOR 1/8W 5% 24K	R99	1					
47	RCR05G202JS	RESISTOR 1/8W 5% 2K	R93	1					
48	RCR05G101JS	100Ω	R92	1					
49	RCR05G104JS	100K	R100-105 R11,12,13,47,48,61	12					
50	RCR05G200JS	RESISTOR 1/8W 5% 20Ω	R90,91	2					
51	B33063-A1390-H9	CAPACITOR POLYPROPYLENE 39pf	C23	1					
[illegible]	CYR41E510G	CAPACITOR GLASS 51pf	C10,11,13	3					
53	CYR41E181G	GLASS 180pf	C12,14,15	3					
54	B33063-A1621-H9	POLYPROPYLENE 620PF	C22	1					
55	A1561	560pf	C27	1					
56	A1301	300pf	C20,37,25	3					
57									
58	A1511	510pf	C45	1					
59	B33063-A1151-H9	POLYPROPYLENE 150pf	C18,33,34	3					
60	D51C183 FSA	TEFLON .018 μf	C39	1					
61	122	.0012	C24,36	2					
62	472	.0047	C30,38	2					
63	222	.0022	C26,29	2					
64	822	.0082	C31	1					
65	D51C102 FSA	CAPACITOR TEFLON .001μf	C28	1					
66	B33063-A1681-H9	CAPACITOR POLYPROPYLENE 680PF	C40	1					

REV

NEXT ASS'Y

USED ON

BY [illegible] 9-17-75	CK.
APR.	APR.
TITLE VCO & OUTPUT AMPLIFIER	
PARTS LIST NUMBER P/L 105930	REV F
SHEET 2 OF 4	

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO
67	CKR05BX103K-1575	CAPACITOR CERAMIC .01uf	C5 THRU 9,42	6
68	D51C203FSA	" . TEFLON .02uf	C68,C16	2
69	CKR05BX104K-1593	" .1uf	C43,65	2
70	PC26	CAPACITOR .8-10pF	C67	1
71				
72	CSR13F685K-3024	CAPACITOR, TANTALUM 6.8uf 35V	C3,4,5	3
73	CSR13G475K-3088	CAPACITOR, TANTALUM 4.7uf 50V	C1,C2	2
74				
75		CAPACITOR, SELECT AT TEST	C17,19,21,32	5
76			35	
77				
78				
79				
80				
81				
82	CD4046AK/IN* -OR- W/O*	INTERGRATED CIRCUIT 4046	A1 THRU 6	6
83	CD4016AK/IN* -OR- W/O*	4016	A7,8,12	3
84	M38510/05101 ADC-OR-ADA	4013	A9	1
85	M38510/05301ADC-OR-ADA	CD4007	A10	1
86	CD4040AK/IN* -OR- W/O*	INTERGRATED CIRCUIT 4040	A11	1
87				
88				
89	JANTX 2N2484	TRANSISTOR 2N2484	Q1,12	2
90	JANTX 2N2605	" 2N2605	Q2,13	2
91				
92				
93				
94				
95				
96				
97				
98	JANTXV1N964B	DIODE 1N964B	CR1 THRU 5	5
99	JANTX 1N483B	DIODE 1N483B	CR13,14	2

REV | NEXT ASS'Y | USED ON

BY AKM 9-19-75 CK.

APR. APR.

TITLE VCO & OUTPUT AMPLIFIER

PARTS LIST NUMBER: P/L 105930 REV F

SHEET 3 OF 4

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO.					
1	101215-01	TRANSFORMER		T1	1					
1										
102	47-101216-01	INDUCTOR	1.172 MH	L5	1					
103	217-01		2.345	L6	1					
104	218-01		4.69	L7	1					
105	219-01		9.38	L8	1					
106	220-01		18.76	L9	1					
107	221-01		37.5 MH	L10	1					
108	222-01		313 μH	L11 & 18	2					
109	223-01		625	L12	1					
110	224-01		1.25 MH	L13	1					
111	225-01		2.50 MH	L14	1					
112	226-01		.5 MH	L15	1					
113	47-101227-01	INDUCTOR	10 MH	L16	1					
114	LT10K096	INDUCTOR	1 MH	L2, L4	2					
115	47-101249-01	INDUCTOR	35.2 MH	L19	1					
116	LT10K227	INDUCTOR ½W	100 μH	L1, L3	2					
119										
120										

REVISI[illegible]

NEXT ASS'Y

USED ON

BY AKM 9-19-75 CK.

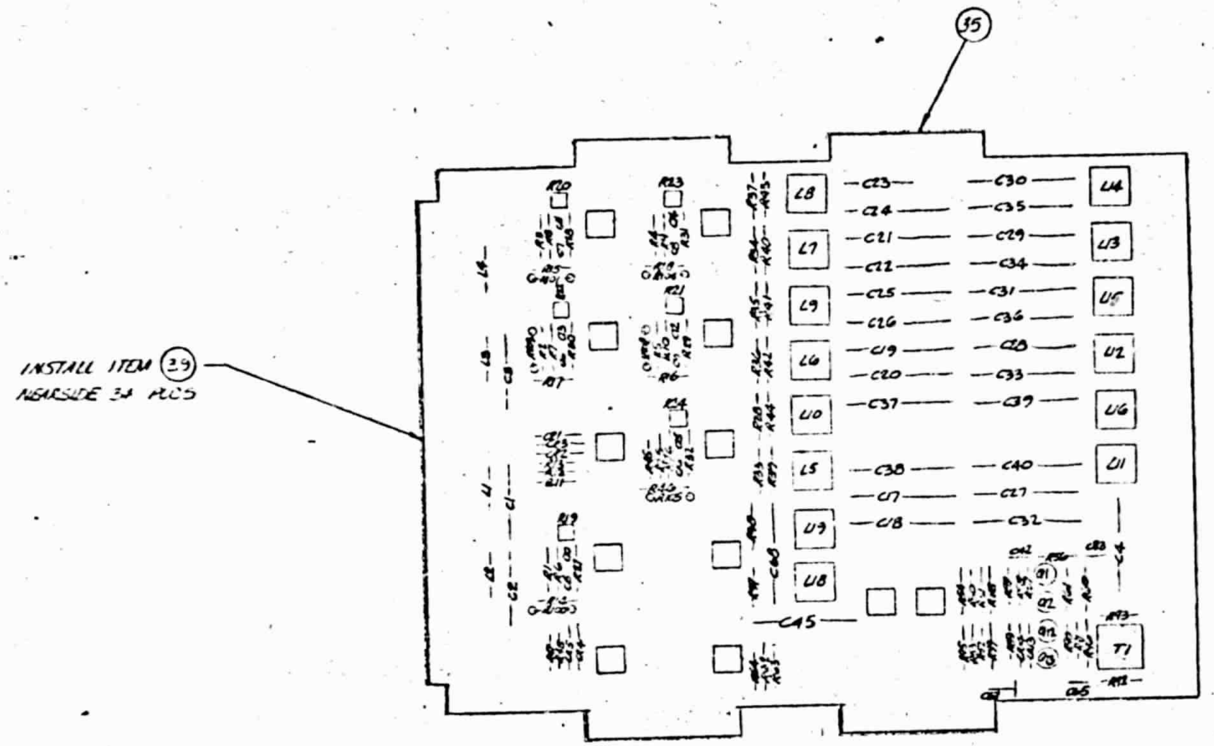
APR. APR.

TITLE VCO & OUTPUT AMPLIFIER

PARTS LIST NUMBER P/L 105930 REV F

SHEET 4 OF 4

REVISIONS					
SYM	DATE	DESCRIPTION	CKD	APPR	DATE



CANFORD	H 105936	1
USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN	MMM	4-12-76
CHECKED		
APPROVED		
ENGINEER	JW	4/14/76
PROJ ENGR		

DEVELCO INC.

TITLE: VCO & OUTPUT AMPLIFIER

SIZE	CODE IDENT NO	DRW NO	REV
C	30002	1-105930	

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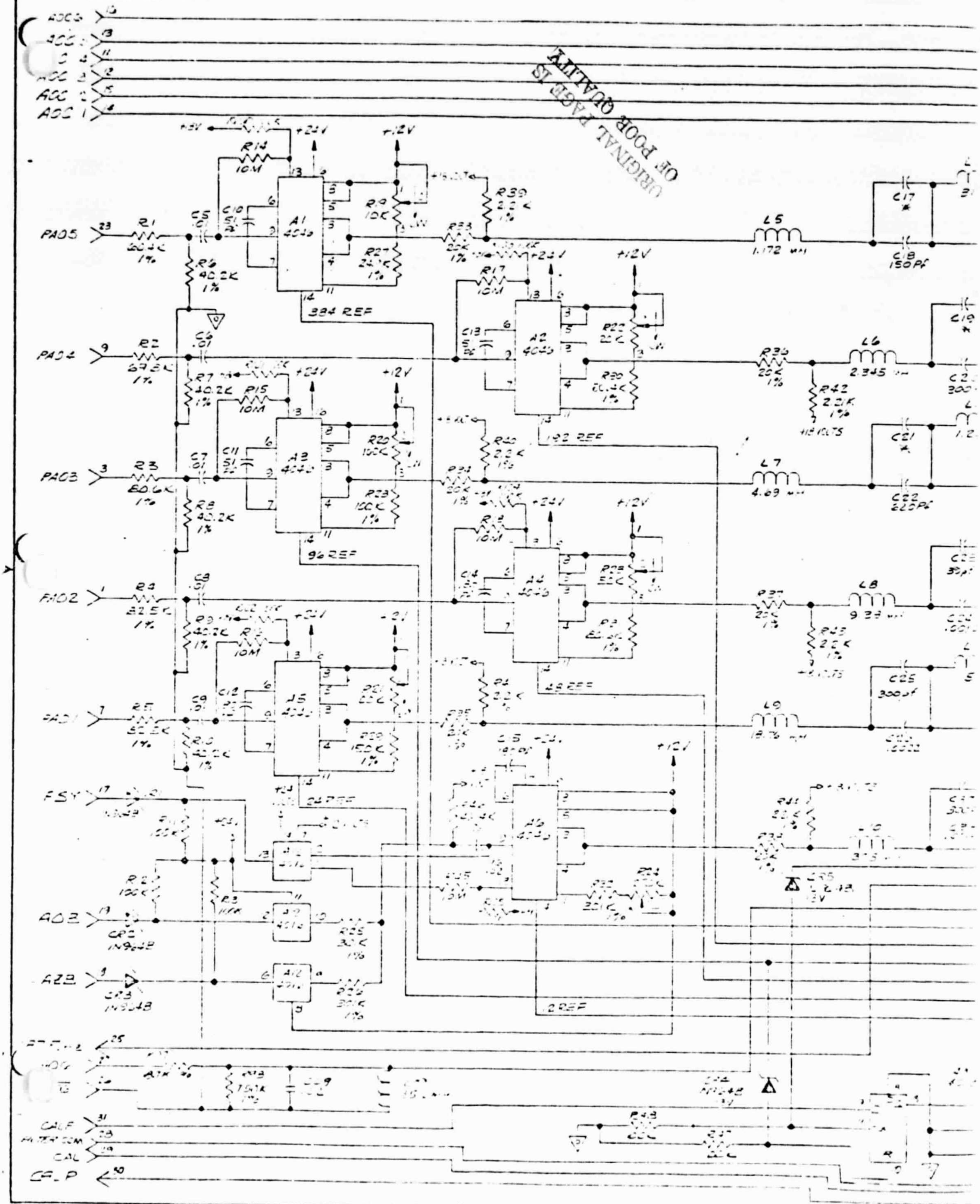
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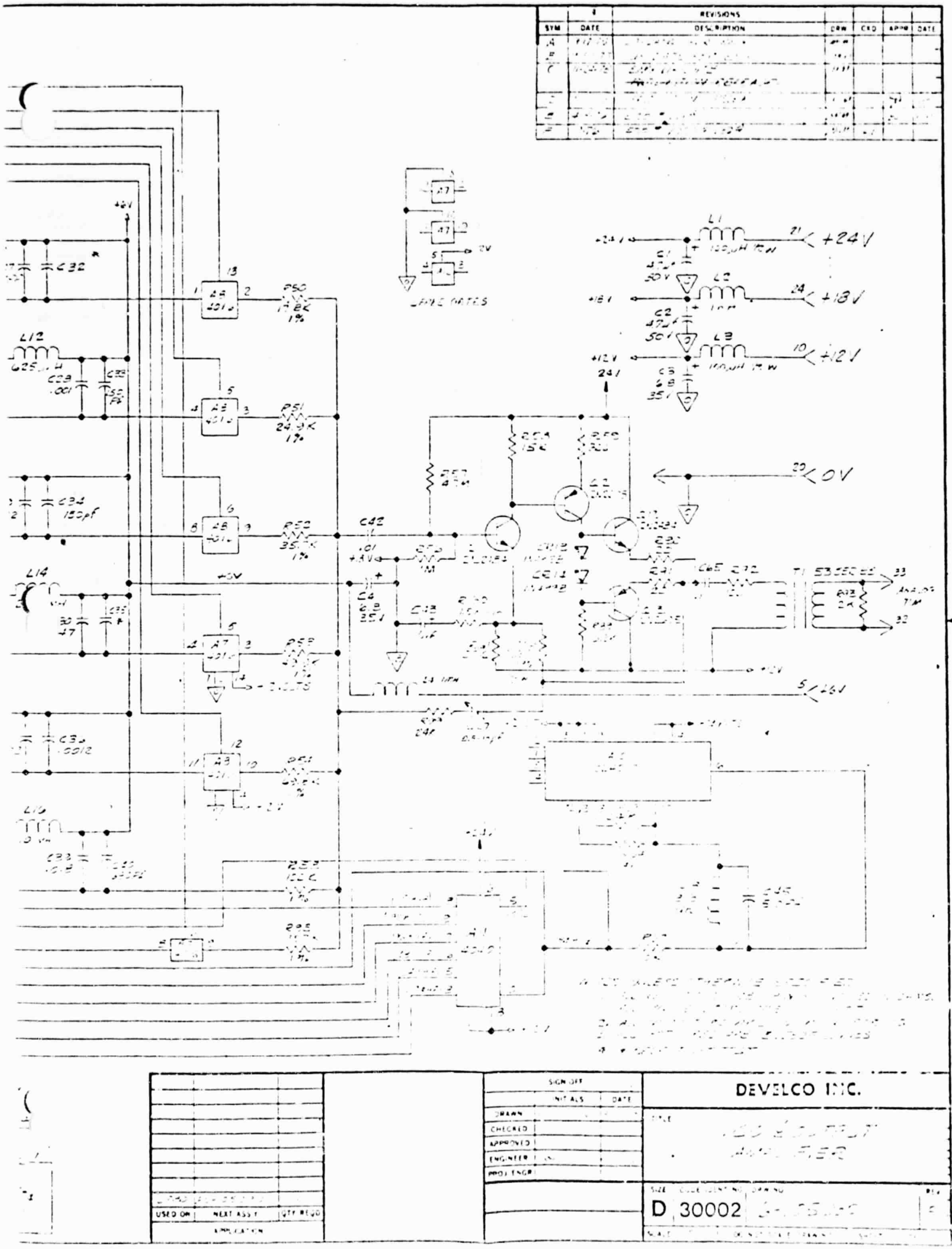
PA04
PA03
PA02
PA01
R1
R2
R3
R4
R14
R15
R17
A1 4046
A2 4046
A3 4046
A4 4046
A5 4046
L5
L6
L7
L8
L9
1.172 mH
2.345
4.69
384 REF
192 REF
96 REF
48 REF
24 REF
12 REF
+24V
+12V
C5
C6
C7
C17
C18
150PF
CR3
1N914B
CAL
CAL P


REVISIONS
SYM
DATE
DESCRIPTION
DRW
CKD
APPR
DATE
+24V
+18V
+12V
0V
L1
L2
L3
C1
C2
C3
+6V
C32
A8
4016
R50
17.8K
1%
R51
24.9K
1%
R52
35.7K
1%
L12
625μH
C28
.001
C34
150pf
C42
.01
L14
C4
6.8
35V
A7
R53
100K
1%
A1
4049
L16
C36
.0012
T1
SIGN OFF
INITIALS
DATE
DRAWN
CHECKED
APPROVED
ENGINEER
PROJ ENGR
USED ON
NEXT ASSY
QTY REQD
APPLICATION
DEVELCO INC.
TITLE
SIZE
CODE IDENT NO
DRAWING NO
REV
D
30002
SCALE

DEVELCO

Develco, Inc.
404 Tasman Dr., Sunnyvale, CA 94086
Phone (408) 734-5700 TWX 910-339-9295

Report No. 983-761208

DATA CONVERTER/SPACECRAFT COMMAND SIMULATOR (106075-01) GROUND SUPPORT EQUIPMENT FOR THE HELLIWELL VLF WAVE EXPERIMENT SPACECRAFT RECEIVER

Prepared for:

Radioscience Laboratory
Stanford University
Stanford, CA 94305

Under:

Subcontract No. PR2006

December 1976

CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF DRAWINGS AND PARTS LISTS

1. INTRODUCTION

This report describes the Ground Support Equipment (GSE) used to test the Helliwell VLF Wave Experiment spacecraft electronics.

The GSE will permit prelaunch operations, testing and telemetry data conversion for the VLF receiver unit. The GSE is capable of providing the following:

A. Power and power switching to operate the receiving system.

B. Command logic compatible with the spacecraft command word to operate all receiver command functions.

C. Test signals for the receiver.

D. Discriminators and a decoder as required to process the telemetered data, with a metered output, for recording the 1-32 kHz spectral response information.

E. Protective circuitry to prevent spacecraft receiver system damage due to GSE malfunctions such as overvoltage and grounding.

The GSE is powered by 115 volts at 60 hertz with a third ground wire and three-prong power plug. It is housed in a rugged portable case with a removable cover for protection of the controls, indicators, and connectors. The front panel for the GSE is shown in Figure 1. The front panel controls and indicators are described in Table 1.

The GSE is basically composed to two sections: a digital section and an analog section.

Three modular type power supplies are used for the GSE: one 6 volt, one 12 volt, and one 28 volt. The 28-volt power supply is also used to power the HEM VLF receiver.

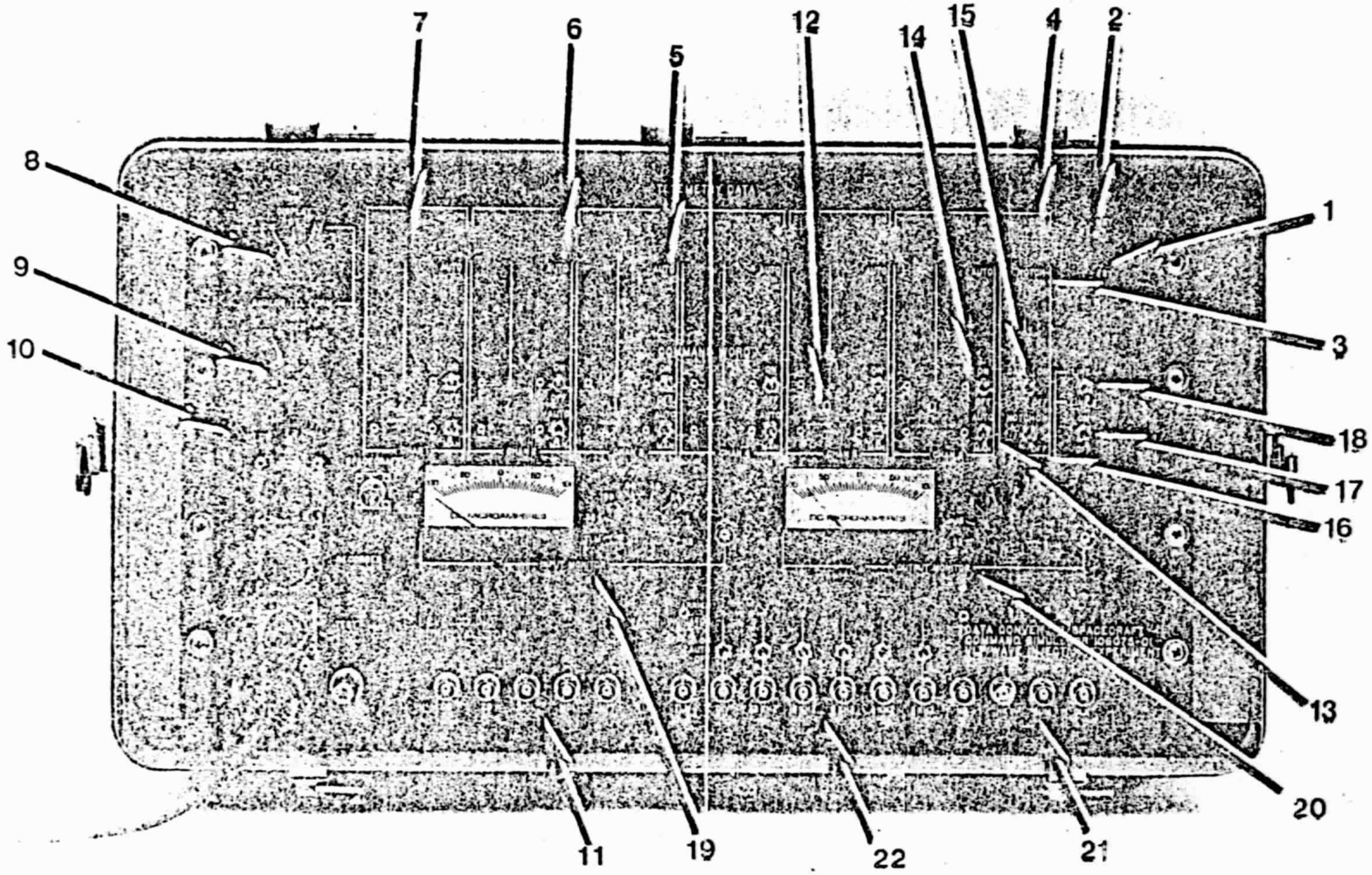


FIGURE 1

DATA CONVERTER/SPACECRAFT COMMAND SIMULATOR

TABLE 1

FRONT PANEL CONTROLS
DATA CONVERTER/SPACECRAFT SIMULATOR

FIG 1 REF	DESIGNATION	DESCRIPTION
1	FSY (frame sync)	LED indicator. During monitoring of analog telemetry data it indicates frame sync after receiving a complete telemetry message successfully. Telemetry data is updated when the FSY turns on.
2	MSY (marker sync)	LED indicator. During monitoring of analog telemetry data it indicates the 8 MSY bits in each of 8 6-bit words.
3	NOTCH ON	LED indicator. The 44th bit in the telemetry message. When the LED is on, the 20 kHz notch filter is on.
4	CAL	LED indicator. The 21st bit in the telemetry message. When the LED is on, the experiment is in the Calibrate mode.
5	AUTO GAIN	LED indicators, one for each of six channels. Illuminated LED indicates that channel is in the automatic gain mode.
6	ON	LED indicators, one for each of six channels. Illuminated LED indicates that output is summed into the Analog Telemetry link.
7	TELEMETRY WORD (gain setting display)	Single-digit display, one for each of 6 channels. Indicates the amplifier gain setting is dBx10 in a range of 0-7x10 dB.
8	DISPLAY	3-position switch. Selects one of 3 words to be displayed on the Telemetry Data display.
	CW	Displays the command word as seen by the experiment's command word register.
	DT	Displays the Digital Telemetry Word as transmitted by the Digital Telemetry register of the experiment.
	AT	Displays Analog Telemetry data from the Analog Telemetry register. The form the data is in when monitored will be function of the Analog Telemetry Form switch.

TABLE 1
(CONTINUED)

FIG 1 REF	DESIGNATION	DESCRIPTION
9	ANALOG TELEMETRY FORM	3-position switch. When the DISPLAY switch is in the AT position, this switch selects the point at which data is monitored.
	NRZ	Monitors the "Non-Return-to-Zero" data from the output of the Analog Telemetry Register.
	CODED	Monitors the data in digital form after it has been encoded.
	MOD	Monitors data from the analog demodulator as would be done in flight.
10	XMIT CW	Momentary pushbutton. When pressed, the Command Word set on the front panel will be transmitted to the experiment.
11	Digital Signal Monitor	BNC test points for troubleshooting. The signals are only time and "1" and "0" level relative and are not absolute level relative signals.
	OB	Monitors the "1" coded bit from either the demodulated or coded signal depending on the position of the AT Form switch [9].
	ZB	Monitors the "0" coded bit under the same conditions at OB.
	MCL	Monitors the CCL, DCL or ACL depending on the position of switch [8].
	MDI	Monitors the serial data CDI, DDO, or decoded ADO as determined by switch [8].
	MPT	Monitors the CEN, DPT or ESY depending on the position of switch [8].
12	GAIN	Thumbwheel switch, one for each of six channels. Sets the gain bits in the command word for the respective channels. Represents gain in dBx10.

TALBE 1

(CONTINUED)

FIG 1 REF	DESIGNATION	DESCRIPTION
13	AUTO/MANUAL	2-position toggle switches, one for each of six channels. Sets the state of the auto/manual bit in the command word for the respective channels.
	AUTO	The gain of the channel will be determined internal to the experiment.
	MANUAL	The gain will be set to the setting in the appropriate thumbwheel switch.
14	CHANNEL ON/OFF	2-position toggle switch, one for each of 6 channels. Sets the state of the on/off bit in the command word for the appropriate channel.
	ON	The output of the channel is summed in the Analog Telemetry signal.
	OFF	The channel functions but its output is not summed into the telemetry signal.
15	CAL ON/OFF	2-position toggle switch. Set the CAL bit in the command word.
16	NOTCH ON/OFF	2-position toggle switch. Sets the 20 kHz notch filter on/off bit in the command word.
17	RDN ON/OFF	2-position toggle switch. Determines if the command word will be transmitted redundantly.
18	LINE 1/2	2-position toggle switch. Selects which pair of redundant lines the signal will be transmitted over when the RDN switch is in the OFF position.
19	INPUT MONITOR	8-position switch selects any one or all input subcarriers for the scaled peak detector meter. BNC is connected in parallel for external monitor.
	TLM	Monitors the sum of all subcarriers
	384	Monitors the subcarrier with f_o = 384 kHz

TABLE 1

(CONTINUED)

FIG 1 REF	DESIGNATION	DESCRIPTION
	192	Monitors the subcarrier with f_0 = 192 kHz
	96	Monitors the subcarrier with f_0 = 96 kHz
	48	Monitors the subcarrier with f_0 = 48 kHz
	24	Monitors the subcarrier with f_0 = 24 kHz
	12	Monitors the subcarrier with f_0 = 12 kHz (Housekeeping)
	NB	Monitors the 5 kHz narrowband incoming signal.
20	OUTPUT MONITOR	8-position switch selects any one or all output signals for the scaled peak detector meter. BNC is connected in parallel for external monitor or measurement.
	32	Monitors the 16-32 kHz signal channel
	16	Monitors the 8-16 kHz signal channel
	8	Monitors the 4-8 kHz signal channel
	4	Monitors the 2-4 kHz signal channel
	2	Monitors the 1-2 kHz signal channel
	DIV	Monitors the divided HK subcarrier signal
	HK	Monitors the trilevel housekeeping data
	SUM	Monitors the summed signals
21	ANALOG BNC MONITOR	BNC test points for troubleshooting
	TLM	The incoming subcarriers at the buffer output
	HK	Trilevel housekeeping data
	SYN	The output signal of the summing amplifier
	CLK	96 kHz

TABLE 1

(CONTINUED)

FIG 1 REF	DESIGNATION	DESCRIPTION
22	CARRIER INFORMATION	
	CARRIER INDICATORS	Indicates which carrier frequencies have been detected
	AMPLIFIER SWITCHES	3-position switch
	ON	Channel is turned on
	AUTO	Channel is turned on if carrier is detected
	OFF	Channel is turned off
	CARRIER MONITORS	Monitors same information as described in Reference 20

2. ANALOG SECTION

A block diagram of the data converter is shown in Drawing 7-105945. The incoming signal is transformer coupled to the buffer amplifier. The buffer amplifier has a gain of 14 dB, giving an overall gain of 7 dB referred to the input of the isolation transformer. The output of the buffer amplifier drives an array of six frequency discriminators, and a 6-kHz narrowband 2-pole filter.

Each discriminator board contains an input bandpass filter, a buffer stage immediately following the bandpass filter for subcarrier monitoring, a phase-locked-loop discriminator, a lowpass filter and a highpass filter. The highpass filter for the HK discriminator is deleted, since it has little effect in the performance in the circuit. A phase-locked-loop type discriminator is used because it is compatible to the VCO type used in the Helliwell receiver; hence, linearity improves. In addition, this type of discriminator provides carrier phase detection.

An array of seven analog switches is used to connect the outputs of the analog discriminators, the divided HK subcarrier, and the 6-kHz narrowband input to the current summing output amplifier. The analog switch used for the 6-kHz narrowband input is always on; the other switches are gated by their respective channel carrier detectors. Provision to override the carrier detect gate is also incorporated.

The discriminated tristate data from the HK discriminator is fed to Detector Board 105944 along with the HK subcarrier. The tristate data is converted to 2-line code with CMOS logic level for the HK decoder. The HK subcarrier is divided down 20 times and then fed to the summing amplifier; the HK subcarrier synthesizes the 96-kHz VCO so that the frequency of the master oscillator inside the HEM receiver can be monitored.

Two meter circuits are included in the HEM GSE to provide a fast functional check of the HEM receiver.

One meter circuit is a peak-detection type and it is used to monitor the telemetry and subcarrier signal. The other meter circuit is a true-RMS type and it monitors the discriminated signals and the summing output.

Functions 19 to 22 of Table 1 (front panel controls and indicators) describe the operation and testing capabilities of the analog section.

3. DIGITAL SECTION

The purpose of the digital section of the GSE is to provide the following functions (refer to Figure 4 for a block diagram of the digital section):

A. Spacecraft signal simulation and controls to demonstrate that the experiment functions properly and reliably during the bench test prior to spacecraft integration.

B. Selectable monitoring of key points for display in the digital electronic circuits during spacecraft integration for the purpose of general troubleshooting. The monitoring points include: (a) Command Word transmitted by the spacecraft computer, (b) Digital Telemetry Word transmitted to the computer, and (c) Analog Telemetry Word at 3 points in the coding and decoding process.

A list of abbreviations used in both the experiment and GSE digital circuitry is contained in Table 2. Functions 1 through 18 of Table 1 (front panel controls and indicators) basically describe the operation and testing capabilities of the digital section.

3.1 CONNECTORS

Two connectors are provided on the GSE for use during spacecraft integration and/or bench test prior to integration: the Test Monitor connector and the Spacecraft Simulator connector. When the Spacecraft Simulator cable is connected during bench test, the Analog Telemetry Data (ADO) will be monitored from the spacecraft connector. During spacecraft integration, this connector will not be used and ADO will be monitored via the test connector. When the test connector cable is connected, the front panel selector switches are enabled and Telemetry Data may be monitored as selected. After completion of integration, the GSE may be used as a data monitoring unit.

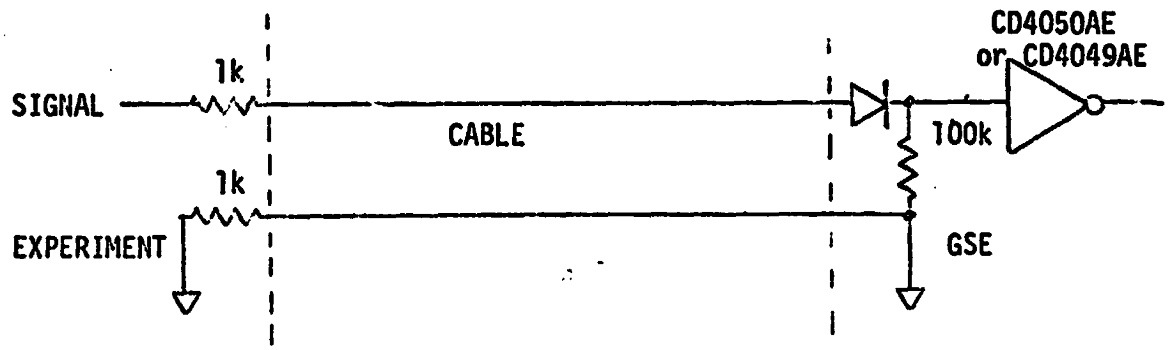


FIGURE 2

GSE INTERFACE

TABLE 2

GLOSSARY

ACL	Analog Telemetry Clock	RDN	Redundancy
ADI	Analog Telemetry Data In	TST	Test
ADO	Analog Telemetry Data Out		
AGA	Amplifier Gain - A Bit (10 dB)		
AGB	Amplifier Gain - B Bit (20 dB)		
AGC	Amplifier Gain - C Bit (40 dB)		
AOB	Analog Telemetry One Bit		
AOC	Amplifier ON/OFF Control		
ASI	Power Monitor		
AT	Analog Telemetry		
AZB	Analog Telemetry Zero Bit		
CCD	Counter Count Down		
CCL	Command Word Clock		
CCU	Counter Count Up		
CDI	Command Word Data In		
CDO	Command Word Data Out		
CEN	Command Word Envelope		
CPJ	Command Word Parallel Jam		
CPT	Command Word Parallel Transfer		
CST	Command Word Serial Transfer		
CW	Command Word		
DCL	Digital Telemetry Clock		
DDI	Digital Telemetry Data In		
DDO	Digital Telemetry Data Out		
DEN	Digital Envelope		
DPT	Digital Telemetry Parallel Transfer		
DT	Digital Telemetry		
FOB	Frequency Demodulated One Bit		
ESY	Frame Sync		
FZB	Frequency Demodulated Zero Bit		
MCL	Monitor Data Clock		
MDI	Monitor Data In		
MPT	Monitor Data Parallel Transfer		
MSY	Marker Sync		

3.2 CONNECTOR INTERFACE

All test connector signals (including common) are terminated with a series 1-kilohm resistor at the experiment. The signals are diode blocked and returned through 100 kilohm resistors at the GSE. Refer to Figure 2.

The experiment/GSE interface is designed to meet the requirements of ISEE-733-74-001, Revision B. Refer to Figure 3.

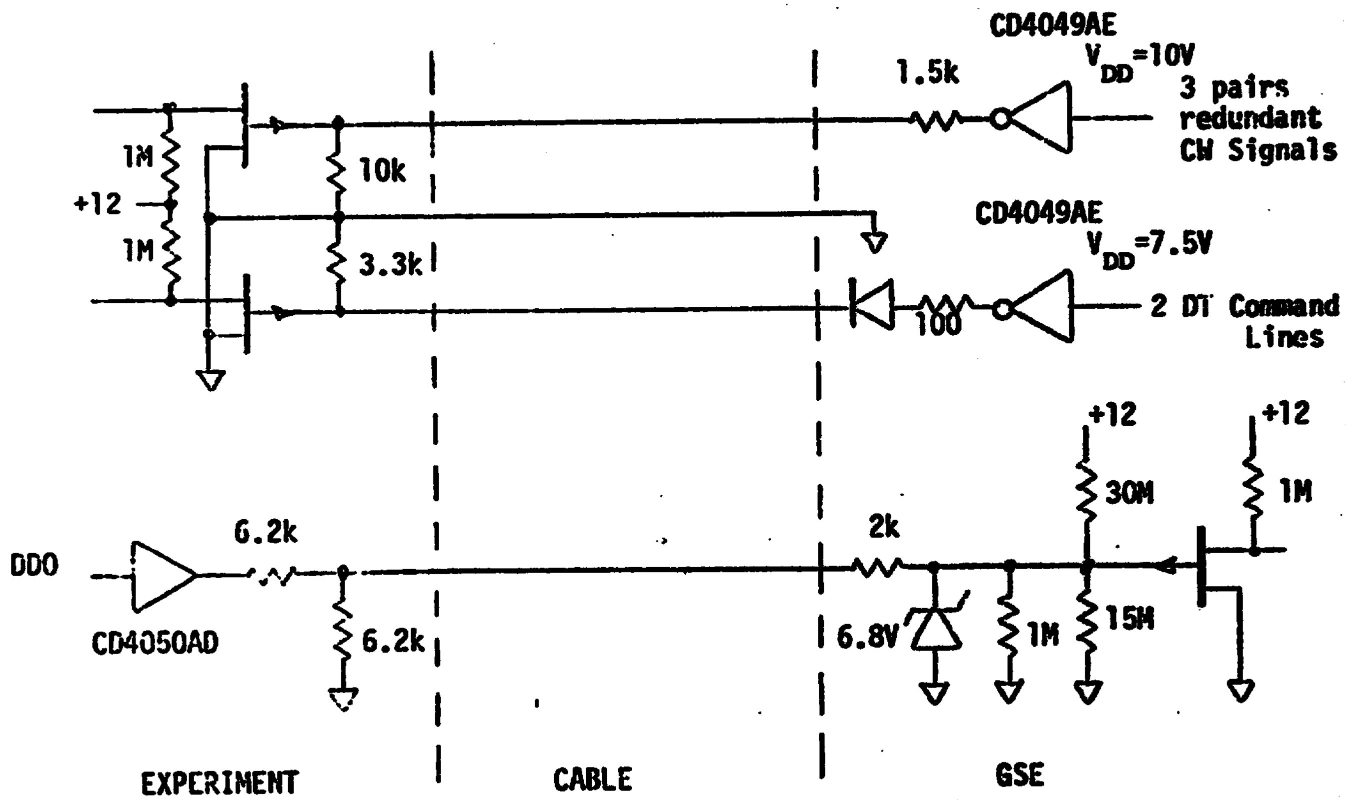


FIGURE 3

EXPERIMENT GSE INTERFACE

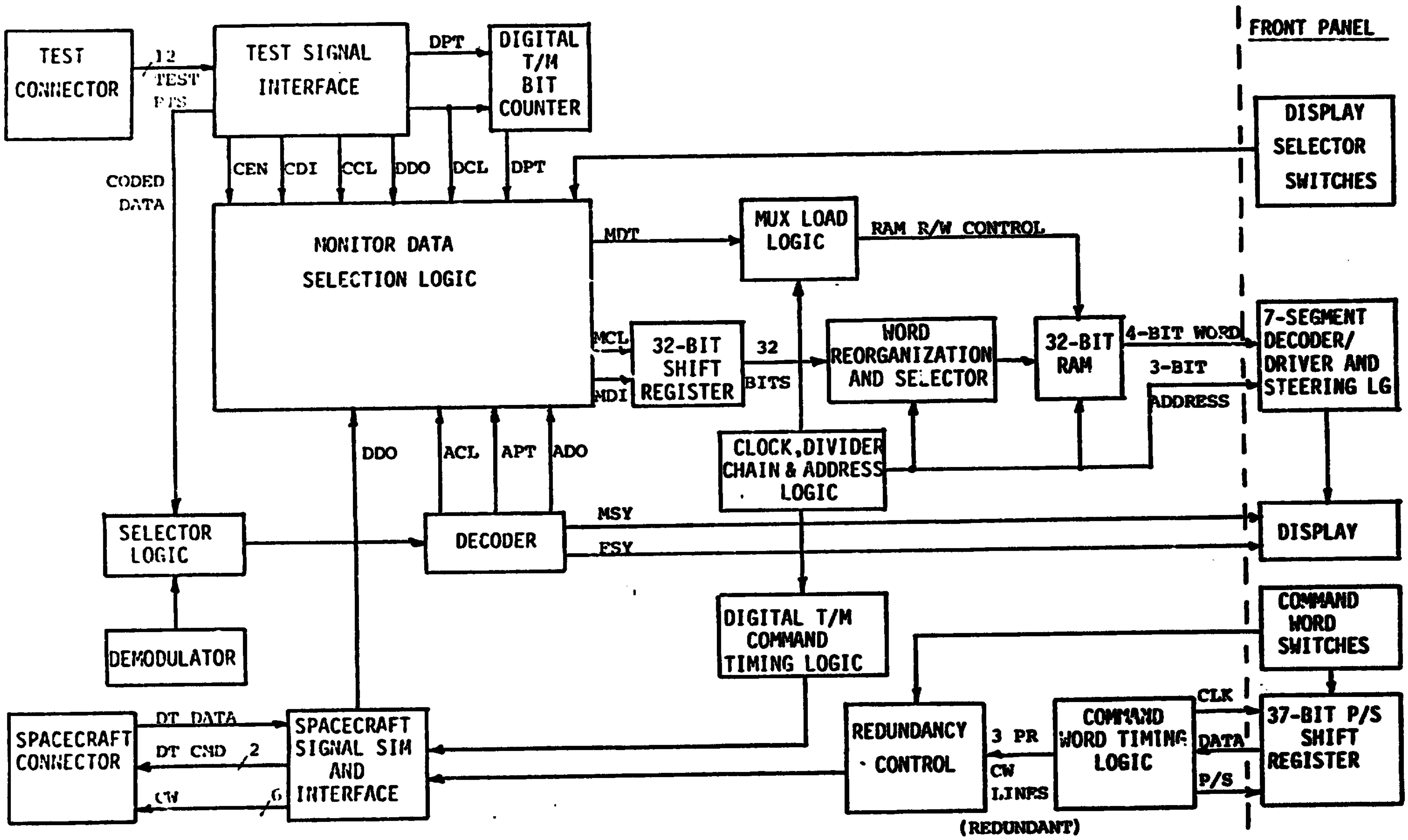


FIGURE 4

BLOCK DIAGRAM FOR DIGITAL SECTION OF HEM GSE

4. ANALOG CIRCUIT DESCRIPTION

The following describes the analog circuits in the GSE. Refer to Drawing 105945 for a complete block diagram of all the analog circuits. Drawing 105948 is the backplane interconnect wiring for all the boards and the front panel connectors.

4.1 INPUT BUFFER - Drawing 6-105940 (Board 1)

Transformer T1 couples the incoming TLM signal to Amplifier U1. Amplifier U1 has a gain of 14 dB, giving an overall gain of 7 dB including the 7-dB loss of the transformer. The maximum input level without suffering severe distortions is 7 volts peak to peak. The output is ac coupled to the discriminators through Pin 2, named BFR, and dc coupled to the 6-kHz filter. Two resistors attenuate the BFR signal which is then fed to Pin 1 for monitoring purposes.

The 6-kHz filter has a bandwidth of 1 kHz, and an insertion loss of 6 dB; it is buffered by device U2 and then brought out to three places - TP8, RD8 and NB out. 100-ohm isolation resistors are used at the output of U2.

The remaining circuitry on Board 1 includes U3 and Q1. The function of this circuitry is to generate two reference voltages. One of the voltages is 6 volts and named Sig Com, while the other one is 6-7 volts and named V_j.

4.2 DISCRIMINATOR - Drawing 6-105942 (Boards 2-6)

Board 2 to Board 6 are the discriminator boards, and they share a common schematic since their circuitry configuration is identical. The main difference among the discriminator boards is their center frequencies which are spaced an octave apart starting at 24 kHz.

Each discriminator board has a three-pole, 1-dB ripple, Tchebychev bandpass input. This filter has a bandwidth of one-fourth of its center frequency and an insertion loss of 6 dB. Transistor 2N2484 buffers the filter for monitoring purposes at Pin 4. The buffered output from the 2N2484 is also capacitor coupled to limiter 1A. 1A is a CA3080 having a gain of 40 dB. A small hysteresis is also included for 1A.

2A is a CD4046 CMOS phase lock loop device. This device has two phase comparators and one voltage controlled oscillator. Capacitor C_0 and the combination resistance of R1 and R2 set up the free running frequency of the VCO. The output of the VCO is tied to one input of phase comparator No. 1, while the remaining input receives the incoming signal from the Limiter 1A. The output voltage of phase comparator 1 is integrated by D10 then fed back to the VCO. With this closed-loop configuration, comparator 1 will force the VCO to phase track the incoming signal, giving a conversion gain of 6 V/fc. Further description of this PLL can be found in RCA Application Note No. ICAN-6101.

Phase Comparator 2 is used for carrier detection. When the VCO is phase locked to the incoming signal, the output of phase comparator 2 will be a 75% duty cycle pulse; if not, its output will have an average duty cycle of 50%. Voltage comparator 3A, CA3080, detects the average output voltage of phase comparator 2. The output of 3A will become true, whenever the duty cycle of phase comparator 2 output exceedes 65%. The output of 3A is isolated by two 30 K resistors and brought out at Pin 12 and 13 to drive a front panel mounted LED and the analog switch for the summing amplifier on Board 8.

Post filtering for the PLL discriminator is performed by op-amps 4A and 5A (CA3094). 4A is configured as a 3-pole, 1-dB ripple, Tchebychev low pass filter, while 5A is configured as a 2-pole, 1-dB ripple, Tchebychev high pass. The drive capacity of the CA3094 is high enough to drive a 50-ohm load with 10 dB loss. The output of 5A is brought to Pins 16, 17, and 18 through 100-ohm resistors for the summing amplifier and the monitor circuitry.

4.3 HK DISCRIMINATOR - Drawing 6-105941 (Board 7)

The housekeeping discriminator is very similar to the other five discriminators with the following differences: the center frequency of the HK discriminator is 12 kHz; the bandwidth of the input 3-pole filter is 4 kHz, that is, one-third of center frequency.

The low pass filter is a 3-pole Bessel filter with the cut-off frequency at 40 Hz. The high pass filter is not used in the HK discriminator because dc information is required by the following detector board (6-105944, Board 9).

4.4 SUMMING AMPLIFIER - Drawing 6-105939 (Board 8)

U3, a CA3100, is the current summing amplifier. Current summing was chosen instead of voltage summing because current summing provides a better approximation of the received signal.

The supply voltage of U3 is 28 volts and 0 V to provide higher output level for the current summing. The 12-volt supply establishes the bias voltage for U3.

U1 and U2 are CD4066 analog gates. With the exception of the gate that is used for the 6-kHz NB channel, all gate controls are pulled down to V_{ss} with a 1 megohm resistor; that is, all channels are normally off except for the NB channel which is always on.

4.5 DETECTOR - Drawing 6-105944 (Board 9)

The detector circuitry receives the discriminated HK signal through Pin 14. U1 is the positive peak buffer amplifier while U2 is the negative peak buffer amplifier for the incoming HK signal. Two 51 K resistors and one 100 K resistor establish the reference voltage for U3 and U4, upper and lower threshold voltage comparators. The output of U3 will become true if the incoming signal voltage is greater than 75% of its maximum-to-minimum value, while U4 will become true when the signal is less than 25%. Two sections of U6, CD4066, are used to reduce the leakage current of the detector diodes (1N270) by feeding back the compared outputs as the gating signals. U14 (CD4030) buffers the compared outputs, and two 6.8 K isolation resistors connect them to Pins 12 and 13.

For summing purposes, the 12-kHz HK subcarrier is divided down to 600 Hz so that it will not interfere with the data signal. One CD4029, U7, and half a CD4013, U8, is used as the divider chain. The divided signal is filtered by a 3-pole Tchebychev, 1-dB ripple, low pass filter after a 31-dB attenuator pad. This low pass filter, having a cut-off frequency of 750 Hz, is implemented by a CA3094, U5, and its output is brought to Pins 16, 17 and 18 through 100 ohm isolation resistors. The harmonic level is at least 40 dB down referred to the data channels.

The generated 600 Hz is also used to clock the 213 ms digital one shot, implemented by U10, U11, and one-half of U8, while another section of U14 resets it on either a "ONE" or "ZERO" code. This one shot has a delay of 138 clock periods; and, since it is reset by either a "ONE" or "ZERO" code, it can fire only once during the frame sync (FSY - refer to Table 1 for FSY definition). The output of this digital one shot controls the analog switch, U6, which gates the servo loop of the 96-kHz synthesized clock.

The 96-kHz synthesized clock is built by U9, and U12. U12 is configured as a divide-by-eight counter. U9 contains a phase comparator and a voltage controlled oscillator. A 50 kΩ variable resistor finely adjusts the center frequency of the VCO. The phase comparator produces an error voltage proportional to the phase difference between the 12-kHz HK subcarrier and the divided 96 kHz. During the frame sync of each data cycle, the VCO is allowed to phase lock to the HK subcarrier which is locked to the master oscillator in the HEM receiver.

4.6 METER AMPLIFIER - 6-105943 (Board 10)

The meter amplifier board contains two meter circuits; one monitors the subcarriers and the other one monitors the discriminated signals. Both the input monitor and the output monitor meters are panel mounted and zero centered.

The input monitor switch selects any one subcarrier signal or the TLM signal and feeds it to the buffer transistor 2N2484 via Pin 4. External monitoring is made possible by bringing back the buffered signal to a front panel mounted BNC through Pin 6.

Op-amp U1 is a CA3080, and it is configured as a positive peak detector with the introduction of another 2N2484. The peak value is brought to the scaling resistors gauged with the front panel input selector switch through Pin 7 and back on Pin 8. Pin 8 is tied to the current summing point of a log converter, implemented by U2 and U3.

U2 is a LM4250 op-amp, and U3 is a CA3096 NPN, PNP transistor array package. The matching characteristic of CA3096 provides temperature compensated operations. Potentiometer R2 is the 0 dB reference adjustment, while R1 is the conversion factor adjustment. Pins 9 and 10 are used for meter drive. The circuit element values have been chosen so that the conversion factor for 0 dB is equal to 100 μA.

The log converter in the output monitor meter circuitry is identical to the one in the input monitor; hence, they have the same conversion factor. However, a true-RMS circuitry is used instead of a peak detector in the output monitor. The RMS function is performed by an Analog Devices Model 440 module. U4 is used to buffer the front-panel-selected signal. A 100-ohm resistor connects the buffered signal to the monitor BNC via Pin 16. The scaling element is an onboard 10 KΩ 1% resistor; hence Pin 17 is jumpered to Pin 18 on the back plane.

5. DIGITAL CIRCUIT DESCRIPTION

The following describes the digital circuits in the GSE. Refer to Figure 4 for a block diagram of the digital section. Drawing 6-105948 includes the backplane wiring for the digital boards and the front panel wiring.

5.1 DISPLAY BOARD FOR HEM GSE - Drawing 106082

The display board (Figure 5) contains six numerical displays to read out gain settings for each PGA located in the HEM receiver and sixteen LED's to indicate (a) the mode (AUTO/MAN) and ON/OFF for each channel, (b) the status of the notch filter and calibration pulse, and (c) the detection of the marker sync and frame sync.

The power switches for the LED displays are constructed with eight 2N2907 transistors buffering a SN7445 (B8) BCD-to-decimal decoder. The "D" input of B8 is grounded since only eight switches are required. The purpose of the power switches is to demultiplex the 4-bit data bus by decoding the address lines to apply power to the proper display group one at a time. This method of displaying data reduces both hardware and power consumption.

Three lines of the data bus are fed to a SN7447A (B3) BCD-to-seven-segment decoder. Since the largest number to be displayed is only seven, the unused "D" input of B3 is grounded. The outputs of B3 are bussed to the inputs of the DL-10 (A4, 6, 8, 10, 12, 14) numerical displays.

Four of the inverters of B2, SN7406, are used by the 4-bit serial data bus (B0-B3) to drive their corresponding LED's. The remaining two inverters (of B2) are used exclusively for marker sync and frame sync.

Interface to the decoder boards, which has CMOS logic level instead of TTL level, is implemented with two CD4050's, B4 and B9. Five volts used to power TTL devices is derived by inserting a 1N4005 diode in the six-volt power line.

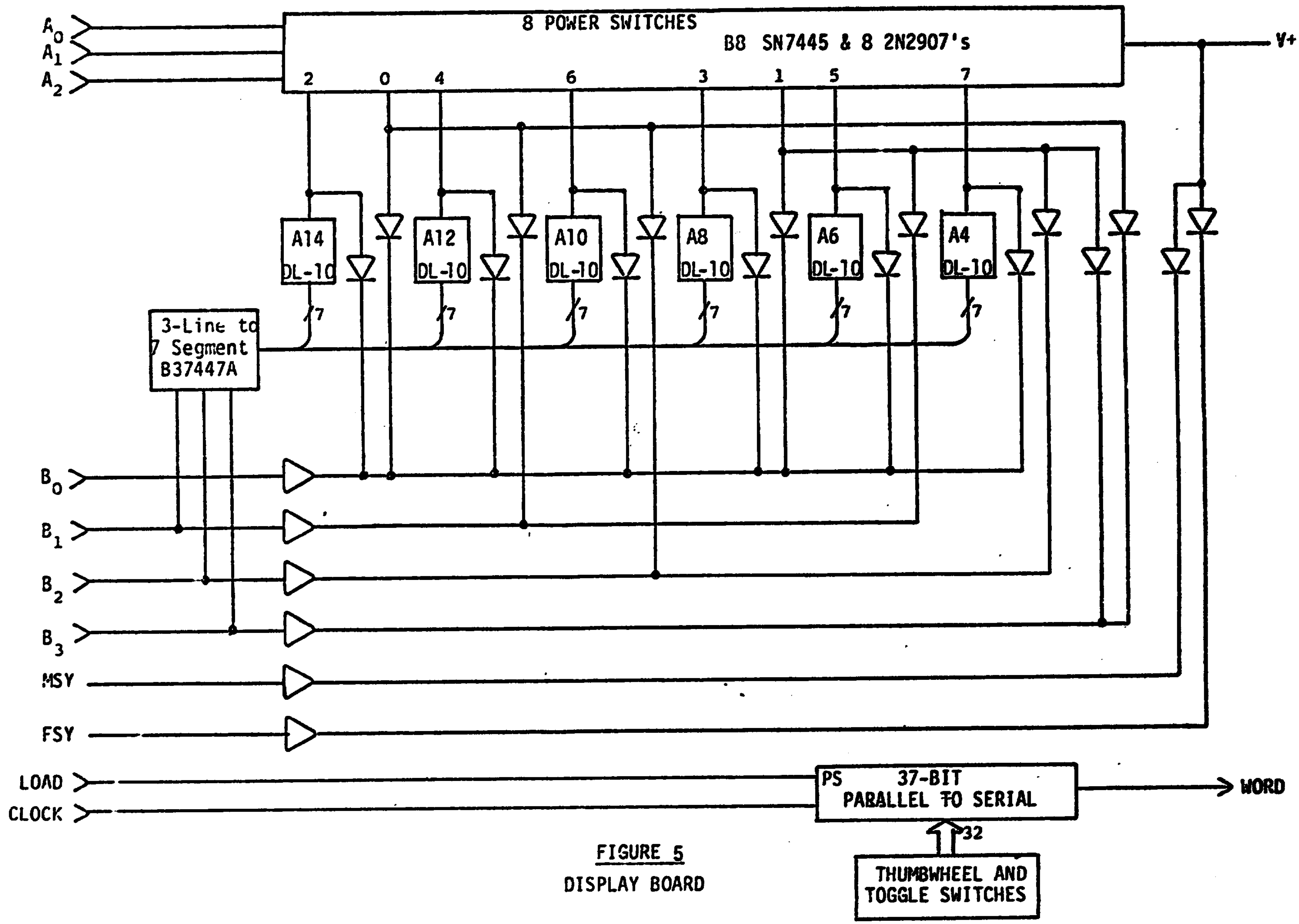


FIGURE 5
DISPLAY BOARD

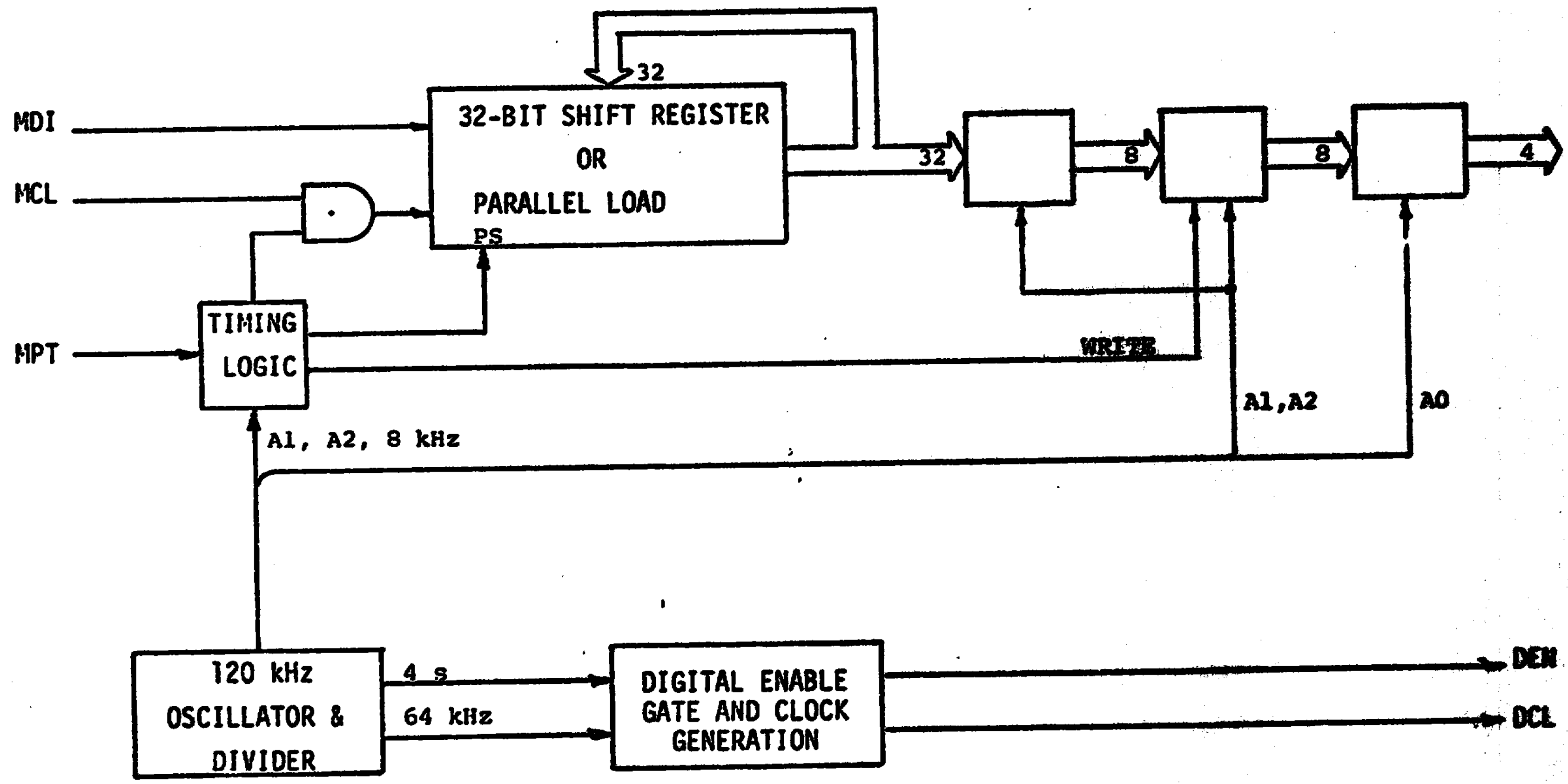


FIGURE 6

DISPLAY MULTIPLEXER AND DIGITAL TELE TIMING
Drawing 6-105894

To simplify the hardware, the 37-bit parallel-to-serial register, implemented with five CD4021's, for the command simulator is located on the display board. Front-panel-mounted thumbwheel switches and toggle switches are wired to the display board to set up the selected command word for the CD4021's, B1 to B5. Thumbwheel switches are used exclusively to program the gain setting for the PGA inside the HEM receiver. 10 KΩ pull-down resistors are used throughout for the switches.

5.2 HEM GSE DISPLAY MUX AND DIGITAL TELEMETRY COMMAND TIMING - Drawing 6-105894

Figure 6 is a block diagram of the board. An onboard 128-kHz oscillator, implemented by B4-10 and B5-4 is divided down to 64 kHz, 8 kHz, 1 kHz, 500 Hz and 250 Hz by A4. It is further divided to a four-second gate by A3 (CD4040). The 1-kHz, 500-Hz and 250-Hz lines constitute the address lines A0, A1, and A2, respectively. These address lines are used to multiplex the incoming 32-bit serial data for the 4 x 8 RAM (C1) and the display board.

The 32-bit serial data, MDI, is clocked into the 32-bit shift register (E1-E4) by MCL via B5-11. After the serial data has been shifted in, the transfer gate, MPT, will initiate a sequence of actions. When MPT becomes true, it will arm flip-flop C4-13 which in turn will allow C5-1 to be clocked true at the next zero address time decoded by B5-3. This B5-3 output signals the following: (a) it signals flip-flop C5 to turn off the data clock as soon as the next 8-kHz line becomes high; (b) it signals the 32-bit shift register to do parallel transfer providing the data clock, MCL, is high - which is the case for digital telemetry; (c) it enables B4-11 to generate the WRITE command for C1 (CD4036 4 x 8 RAM); and (d) it signals C4-1 to reset C4-13, C5-1 and C5-13 on the next zero address time.

The serial shifted MDI is parallel written into the 4 x 8 RAM, eight bits at a time in four steps. The multiplexing function is performed by four CD4052's, D2 to D5 (refer to Table 3), and controlled by address lines A1 and A2.

TABLE 3

HOUSEKEEPING DATA

BIT	FUNCTION		DEVICE LOCATION
1	CH 1	ON/OFF	D2- 2
2		AUTO/MAN	11
3		10 dB	12
4		20 dB	13
5		40 dB	10
6	CH 2	ON/OFF	3
7		AUTO/MAN	4
8		10 dB	5
9		20 dB	D3- 2
10		40 dB	11
11	CH 3	ON/OFF	12
12		AUTO/MAN	13
13		10 dB	10
14		20 dB	3
15		40 dB	4
16	CAL		5
17	CH 4	ON/OFF	D4- 2
18		AUTO/MAN	11
19		10 dB	12
20		20 dB	13
21		40 dB	10
22	CH 5	ON/OFF	3
23		AUTO/MAN	4
24		10 dB	5
25		20 dB	D5- 2
26		40 dB	11
27	CH 6	ON/OFF	12
28		AUTO/MAN	13
29		10 dB	10
30		20 dB	3
31		40 dB	4
32	NOTCH	ON/OFF	5

Two CD4053's, C3 and C2, read the four eight-bit data words (refer to Table 4) back out to the display board in four-bit BCD format (refer to Table 5). Address line A0 conducts the multiplexing.

The digital enable gate, DEN, is generated by B3-1 and its associated counters and gates while A1-10 generates the digital clock, DCL. Both B2 and B1, (CD4017) are configured as modulo-eight counters by feeding the reset input with the eight-count output. 64 kHz from A4 clocks B2 which in turn clocks B1 with its carry-out output. B4-4 decodes the fifth 64-kHz clock and sets the DEN flip-flop B3. After 16 clock periods, B4-3 decodes the twenty-first 64-kHz clock and resets DEN. A1-10 is inhibited during the even number time of B1. As a result, DCL is generated in four groups of eight clock bursts. Both B2 and B1 are reset when they reach sixty-four counts by B3-13. The clock and gate generation is delayed for four seconds until B3-13 is released by A3, and then the whole cycle repeats again.

5.3 HEM GSE TELEMETRY AND DECODING LOGIC - Drawing 6-105896

Figure 7 is the block diagram for Board 12. Since the display board (106082) can be used to display one of the five data different words (refer to Figure 1 and Table 1, ref. 8 and 9): (a) the command word received by the HEM receiver, (b) the status word in the execution register of the HEM receiver that the mission programmer will receive, (c) the NRZ HK data at the test connector, (d) the encoded HK data at the test connector, and (e) the HK data from the HK discriminator, a 3 wide 5-channel multiplexer is constructed using CD4053's - devices 4C, 2B, 4D and 3B. The steering logic is controlled by two front-panel-mounted rotary switches labeled DISPLAY.

Interface to the EXP test connector is implemented by 1N4148 diodes (1C and 1D), 100 k resistors (2C and 2D), and CD4050 buffers (3C, 3D and 5B).

The HK data (AOB and AZB) process requires an additional decoding stage. Exclusive OR gate 6D-3 serves as the clock synthesizer by ORing the two line tristate code, which is a self-clocking code.

TABLE 4

4-WORD BY 8-BIT DATA FORMAT
(CD4036-C1)

ADDRESS	00	01	10	11	
	WORD 1	WORD 2	WORD 3	WORD 4	
	CH 1 ON/OFF	CH 1 AUTO/MAN	CH 2 AUTO/MAN	CH 3 AUTO/MAN	D1
	CH 2 ON/OFF	10 dB	10 dB	10 dB	D2
	CH 3 ON/OFF	20 dB	20 dB	20 dB	D3
	CAL	40 dB	40 dB	40 dB	D4
	CH 4 ON/OFF	CH 4 AUTO/MAN	CH 5 AUTO/MAN	CH 6 AUTO/MAN	D5
	CH 5 ON/OFF	10 dB	10 dB	10 dB	D6
	CH 6 ON/OFF	20 dB	20 dB	20 dB	D7
	NOTCH ON/OFF	40 dB	40 dB	40 dB	D8

TABLE 5

4-BIT SERIAL DATA (8-WORD BY 4-BIT)

	WORD 1	WORD 2	WORD 3	WORD 4	WORD 5	WORD 6	WORD 7	WORD 8
B0	CH 1 ON/OFF	CH 4 ON/OFF	CH 1 AUTO/MAN	CH 4 AUTO/MAN	CH 2 AUTO/MAN	CH 5 AUTO/MAN	CH 3 AUTO/MAN	CH 5 AUTO/MAN
B1	CH 2 ON/OFF	CH 5 ON/OFF	10 dB	10 dB	10 dB	10 dB	10 dB	10 dB
B2	CH 3 ON/OFF	CH 6 ON/OFF	20 dB	20 dB	20 dB	20 dB	20 dB	20 dB
B3	CAL	NOTCH ON/OFF	40 dB	40 dB	40 dB	40 dB	40 dB	40 dB

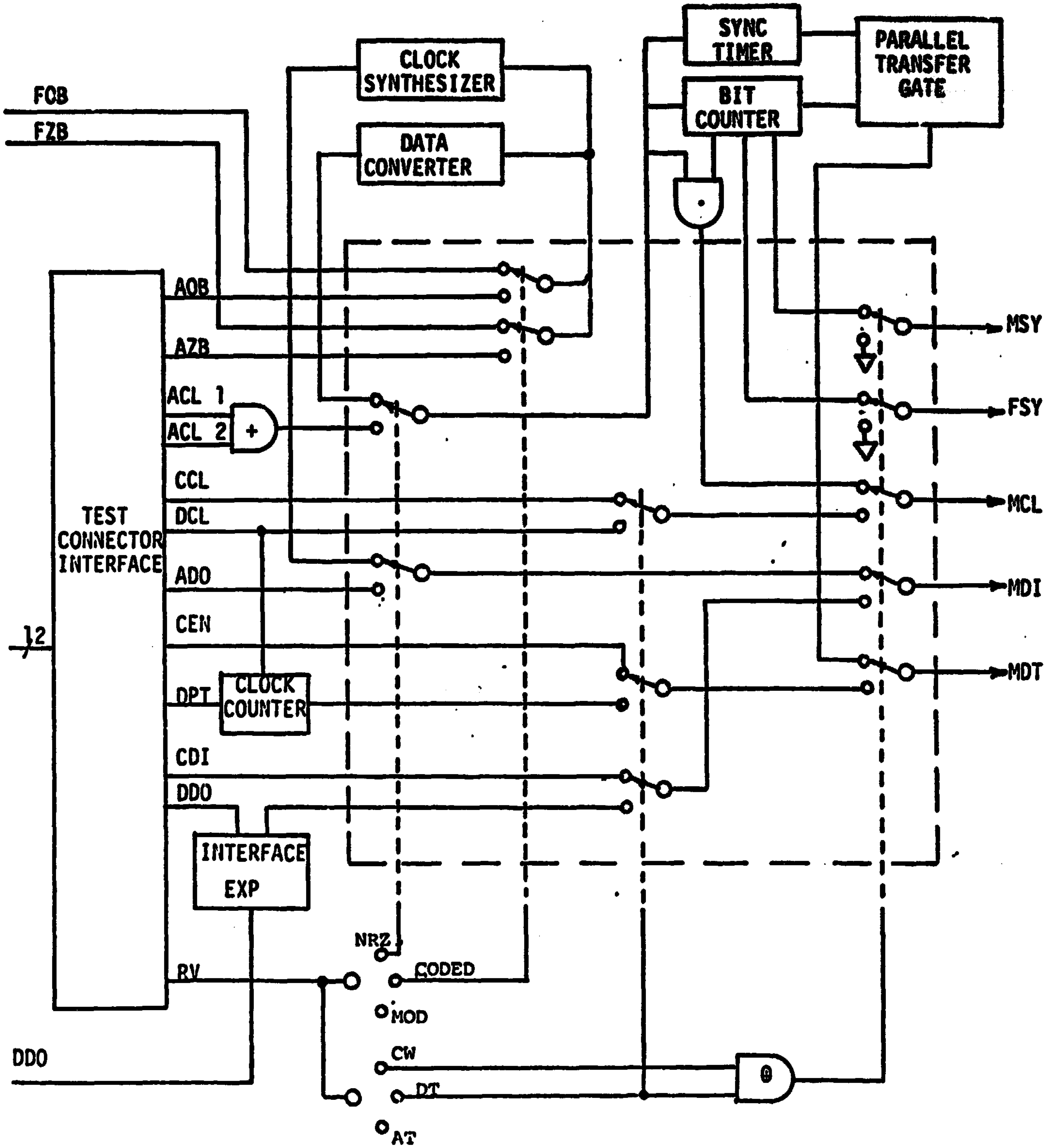


FIGURE 7

TELEMETRY AND DECODING LOGIC
Drawing 6-105896

The self-generated clock is multiplexed along with the NRZ data clock by device 4C. Gates 3A-10 and 3A-11 are configured as an RS flip-flop to convert the tristate code back to NRZ code which is then multiplexed.

Device 6C and 6B (CD4017's) make up the synchronization timer. This timer is driven by the 250-Hz line from Board 11 via Pin 5, and reset by the multiplexed data clock. Further discussion of the synchronization timer follows.

The bit counter is constructed also with CD4017's (7A and 7B). 7B is configured as a modulo six counter by using the reset line to simplify the Marker Sync hardware. The Marker Sync flip-flops, 6A-11 and 4A-10, is set by 4A-6 and reset by 5B-2 or monitor clock. 4A-6 decodes 84 ms from the sync timer and the fifth count from 7B. That is, the Marker Sync flip-flop fires 84 ms after the negative-going edge of the fifth bit which is the center of the sixth bit or marker bit. The timing of the incoming monitor clock has to match the timer before the Marker Sync flip-flop will be set.

7A can be called Marker counter, since it is clocked essentially by recognition of the Marker Sync. This counter is reset by the sync timer on 360 ms; the same line that jams the Marker Sync flip-flop and the sync timer. The sync timer can time up to 360 ms only during the frame sync time slot providing the HK data is detected correctly.

Flip-flop 5A-13 and associated gates implemented the parallel transfer gate. 5A-B is clocked by the same line that reset the Marker Counter 7A. If exactly eight markers have been registered prior to this time, Gate 4B-11 will enable 5A-13 to be clocked true which is the recognization of frame sync or parallel transfer signal. This signal is multiplexed with the other enable gate (4D-4) to Board 11. 5A-13 is ripple reset by the next data clock through 6C.

The function of 5A-2 is to blank out the data clock for the 32-bit shift registers located on Board 11 during Words 4 and 8 of the analog telemetry word format (refer to Table 6) since these two words have no significance. 6A-3 and 6A-4 decode words 4 and 8 for 5A-1.

When the DISPLAY mode is set at digital telemetry, the monitor data parallel transfer (MDT) line is generated on board by counting the incoming clock. The clock counter is implemented by two CD4017's, 5D and 5C, and reset by DPT. This clock counter is necessary so that the shift register on Board 11 will not overflow.

An interface circuit, implemented by a 2N5116 and a 2N2222 transistor and a CD4053, is used to receive the status word in the HEM receiver which has different logic levels.

5.4 GSE CODE TRANSMITTER SIMULATOR - Drawing 6-105953

Figure 8 is the block diagram of the command word simulator, and Table 7 is the command word format. Front-panel-mounted manual switches are used to set up the desired command word to be simulated. Refer to Figure 1 for front panel layout. Thumbwheel switches are used to set up the channel gain bits, while all other bits are programmed by toggle switches.

An onboard 8.54-kHz oscillator is constructed with 2B-10 and 2B-4 (CD4001). The remaining gates of 2B are wired as a bounceless switch buffering the transmit execute momentary switch coming in on Pins 3 and 5. 3B-1 generates the 4.27-kHz clock by dividing the local oscillator.

Upon execution of command, 3B-13 will be clocked to true immediately, and in turn 3A-1 will be clocked true at the beginning of the next clock pulse. When 3A-1 is true, the following occurs: (a) the command word bit counters 3D and 3C are reset, (b) 3B-13 is reset, and (c) the 37-bit parallel-to-serial registers on the display board are signalled to parallel load the manually set command bits via 7B-9. The command envelope will come up as soon as flip-flop 4C is clocked by the local

TABLE 6

ANALOG TELEMETRY WORD FORMAT

WORD NO.	BIT NO.	FUNCTION
1	1	CH 1 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
2	1	CH 2 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
3	1	CH 3 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
4	1	Calibrate
	2	No function
	3	No function 0's
	4	No function
	5	No function
	6	No code
5	1	CH 4 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
6	1	CH 5 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code

TABLE 6

(Continued)

WORD NO.	BIT NO.	FUNCTION
7	1	CH 6 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
8	1	Notch Filter ON/OFF
	2	No function
	3	No function
	4	No function
	5	No function
	6	No code (remains until next transmission)

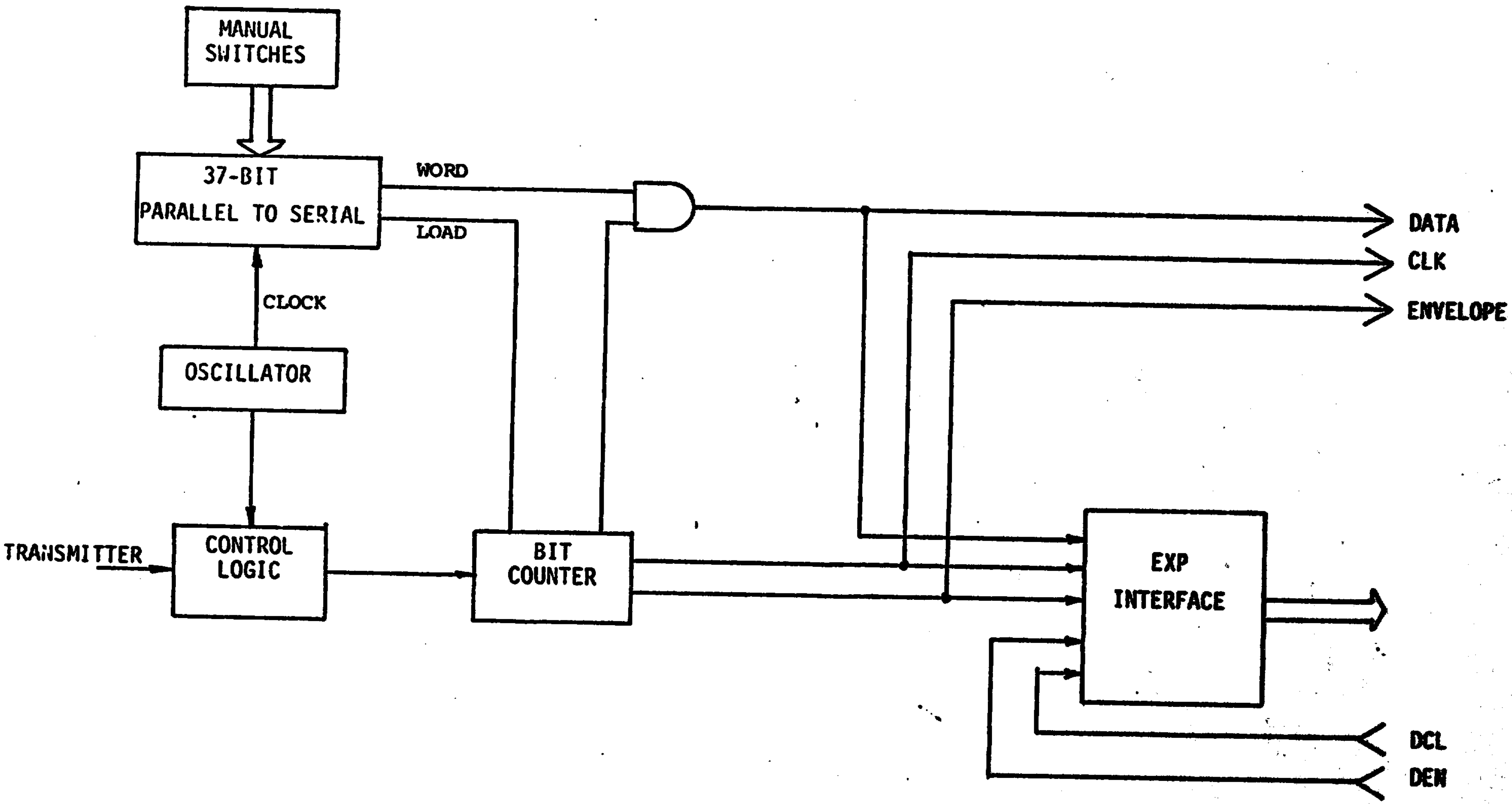


FIGURE 8
COMMAND WORD SIMULATOR

TABLE 7

COMMAND WORD FORMAT

BIT NO.	FUNCTION	CHANNEL
1-5	Unassigned	
6 (LSB)	CH 1 ON/OFF	1-2 kHz
7	AUTO/MAN	
8	10 dB	
9	20 dB	
10	40 dB	
11	CH 2 ON/OFF	2-4 kHz
12	AUTO/MAN	
13	10 dB	
14	20 dB	
15	40 dB	
16	CH 3 ON/OFF	4-8 kHz
17	AUTO/MAN	
18	10 dB	
19	20 dB	
20	40 dB	
21	CAL	
22	CH 4 ON/OFF	8-16 kHz
23	AUTO/MAN	
24	10 dB	
25	20 dB	
26	40 dB	
27	CH 5 ON/OFF	16-32 kHz
28	AUTO/MAN	
29	10 dB	
30	20 dB	
31	40 dB	
32	CH 6 ON/OFF	6 kHz NB
33	AUTO/MAN	
34	10 dB	
35	20 dB	
36	40 dB	
37 (MSB)	20 kHz Notch Filter ON/OFF	

oscillator. At the leading edge of next clock, 3A-13 will be clocked true which in turn resets 3A-1. 3A-13 enables bit clock gate 2C-4 which supplies bit clocks to the 37-bit parallel-to-serial shift register on the display board, the command bit counter (3D), the HEM receiver, and the command envelope flip-flop 4C. After thirty-seven clocks, the bit counter will enable gate 2C-11 which in turn resets 3A-13 and terminates further bit clocks. The command envelope will go low shortly afterwards.

Interface to the display board is made through an onboard ribbon socket connector, 7B. Command bits from the display board appear at 7B-2, when the bit clock is fed to the registers at 7B-10. The command bits are gated by 2C-10 and buffered by 2D-6. 4B-3 and 4B-4 make up the latch which gates the command bits.

Two sets of redundant lines are implemented by 5A, 5B and 5C for command bits, clock and envelope. An interface network for the redundant lines is provided by 15 KΩ resistors and 1000 pF capacitors. 5A-3, 5A-4 and 2D-4 are the controlling gates to activate both or either set of the redundant lines.

Device 6C provides two interface lines for the HEM GSE Display MUX and Digital Telemetry Command Timing Board (Drawing 6-105894); namely, DEN and DCL. Device 6C (CD4049) is powered by a 7.5-volt zener diode, while device 5C is powered by a 10-volt zener diode to simulate the actual mission programmer interface inside the spacecraft. Other onboard circuitry includes a buffered line implemented by the 2N5816 transistor and 4B-11 intended for the PWR MON line from HEM receiver.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
1	105894	SCHEMATIC & ASSY DWG		R					
	105789-1	P.C. BD DOUGLAS 12DE6GP		1					
4									
5									
6	CD4025AE	IC	A1	1					
7	4049		A2	1					
8	4040		A3, A4	2					
9	4017		B1, B2	2					
10	4013		B3, C4, C5	3					
11	4011		B4	1					
12	4001		B5	1					
13	4036		C1	1					
14	4053		C2, C3	2					
15	4052		D2, D3, D4, D5	4					
16	CD 4034 AE	IC	E1, E2, E3, E4	4					
17									
18		RESISTOR 1/4W 5% 220K	A5-1	1					
19		" POT 1 TURN 20K	A5-3	1					
21		CAPACITOR DIP MICA 270PF	A5-3	1					
22									
23		SOCKET 14 PIN WIRE WRAP		7					
24		" 16 PIN " "		12					
25		" 24 PIN " "		5					
26									
27									
28		WIRE 26 AWG		AR					

RE[V]

BY | CK.

APR. AN 9/1/72 | APR.

TITLE NEW GSE DISPLAY UNIT & DIGITAL TELEMETRY COMMAN

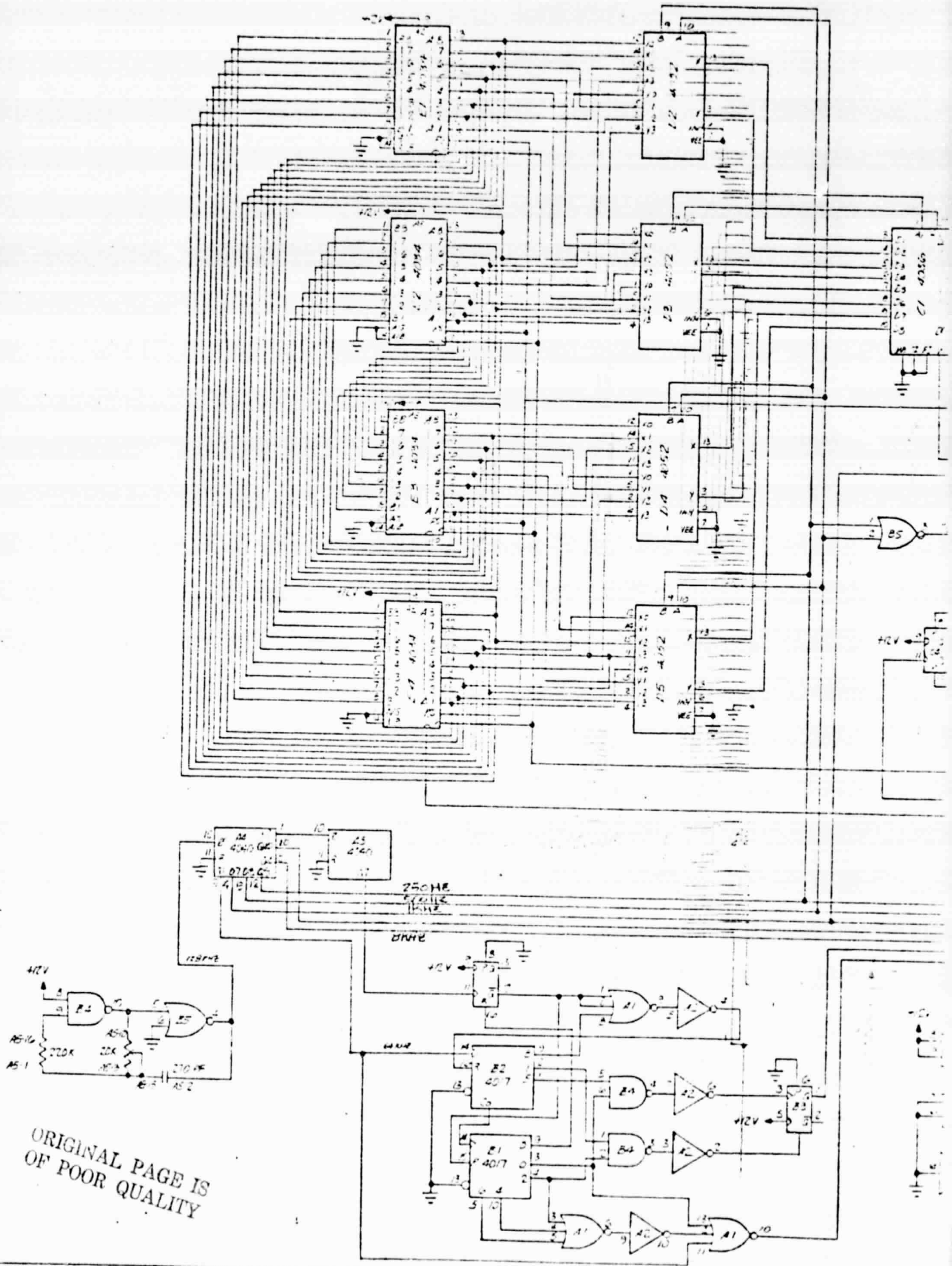
PARTS LIST NUMBER

P/L 105894

REV –

SHEET 1 OF 1

DEVELCO, INC.



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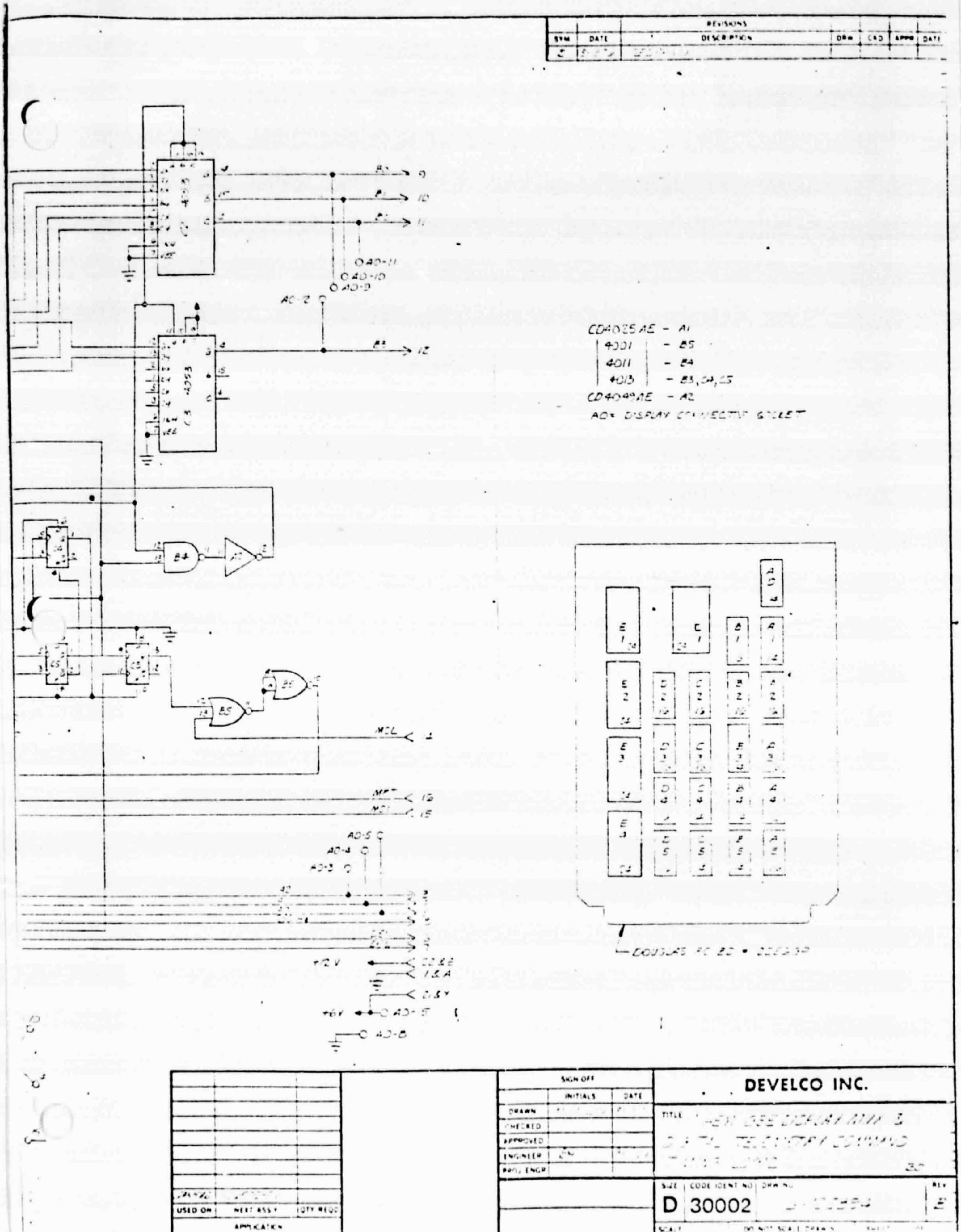
1KHZ
8KHZ
+12V
B5
B4
A1
A2
E2 4017
E1 4017
B3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DATE
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CD4025AE - A1
4001 - B5
4011 - B4
4013 - B3, C4, C5
CD4049AE - A2
B4
A2
C4
C5
B5
MCL
AO-2
AO-3
AO-4
AO-5
AO-8
AO-9
AO-10
AO-11
+12V
+6V
SIGN OFF
INITIALS
DATE
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APPROVED
ENGINEER
PROJ ENGR
DEVELCO INC.
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30002
DWG NO
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APPLICATION

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2	105637	P.C. BD C3		1					
3									
4	CD4001AE	IC	3A	1					
5	4050		3C.3D	2					
6	4023		4A	1					
7	4011		4E.6A	2					
8	4013		5A	1					
9	4049		5B	1					
10	4030		6D	1					
11	4053		2A.2B.4C.9D.3B	5					
12	CD4017AE	IC	5C.5D.6B.6C						
13			7A.7B	6					
14									
15		SOCKET 14 PIN WIRE WRAP		6					
16		SOCKET 16 PIN " "		21					
17									
18		TRANSISTOR 2N2222	1A	1					
19		2N5116	1A	1					
20									
21		RESISTOR 1/4W 5% 100K	1B.2C.2D.1A	18					
22		1M	1A.1B	2					
23		30M	1B	1					
24		RESISTOR 1/4W 5% 15M	1A	1					
25									
26		DIODE 1N4148	1C.1D	12					
27		ZENER 6.2V 1N753		1					
28									
29		CAPACITOR DIP MICA 500 PF	1A	1					
30									
31									
32									
33									

RE[illegible]

BY [illegible] | CK.

APR. [illegible] 9/1/1[illegible] | APR.

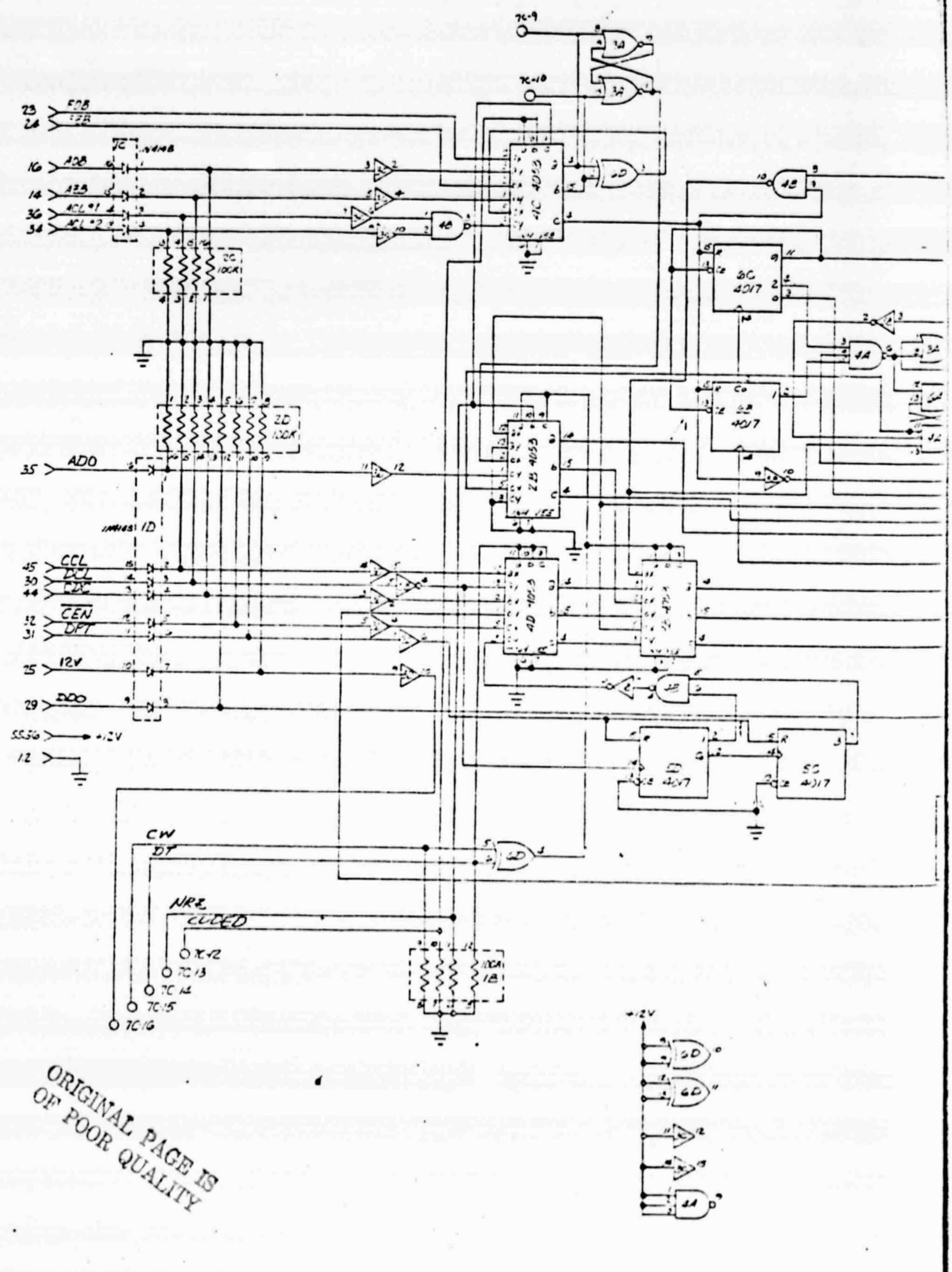
TITLE HELI CSE TELEMETRY E DECODING LOGIC

PARTS LIST NUMBER | REV

P/L 105876 | —

SHEET 1 OF 1

DEVELCO, INC.



ADB
AZB
ACL*1
ACL*2
FDB
FZB
1N4148
7C-9
7C-10
1C 4053
2C 100K
2D 100K
ADO
1N4148 1D
CCL
DCL
CDC
CEN
DPT
12V
DOO
+12V
2B 4053
3C 4017
4B 4017
4D 4053
5D 4017
5C 4017
CW
DT
NRZ
CODED
7C-12
7C-13
7C-14
7C-15
7C-16
100K 1B
6D

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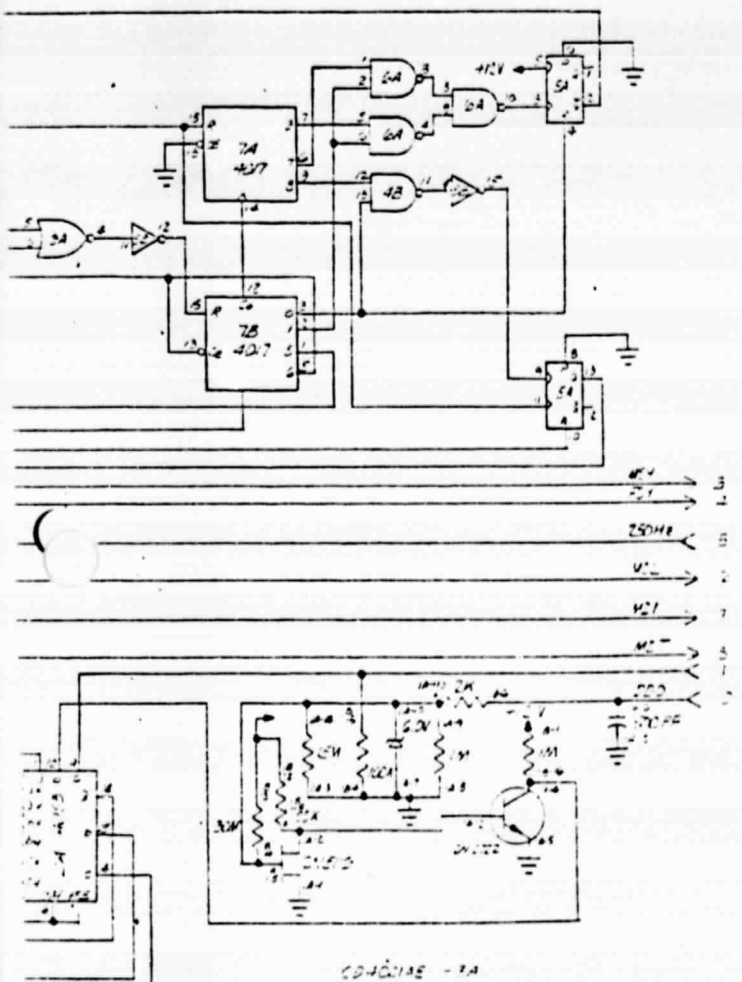
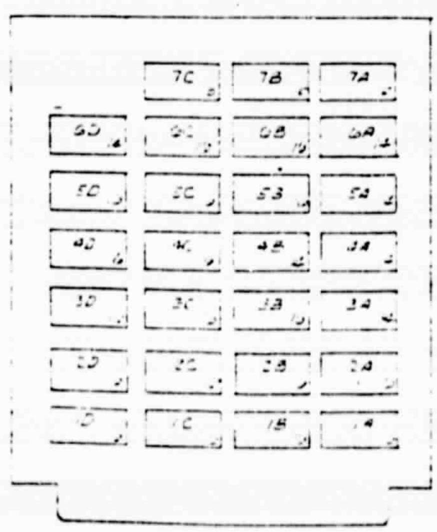


CD4021AE - 7A
4050 - 3C, 3D
4023 - 4A
4011 - 4B 6A
4013 - 5A
4049 - 5B
CD4030AE - 6D
CONNECTOR SOCKET - 7C
D SOCKET FOR RIBBON CABLE



PC BD [illegible]

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APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE NEW 3SE TELEMETRY LOGIC AND DECODING LOGIC

BD 12

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	C-105826	A

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ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO.					
1	105139	SCHEMATIC & ASSY	BG		R					
2		IC BOARD R.DEBGP			1					
3										
4		IC CA3100T			1					
5		" CD4066AE			2					
6		RESISTOR 1/4W 5% 470			1					
7		RESISTOR 1/4W 5% 100			2					
8		" " " 20K			10					
9		RESISTOR 1/4W 5% 10K			1					
10		" " " 1M			3					
11		CAPACITOR TANT 6.8 35V			1					
12		" MICA 33 P			1					
		" CMOS .1			3					

REV

BY MCM CK.

APR. DN 9/1/76 APR.

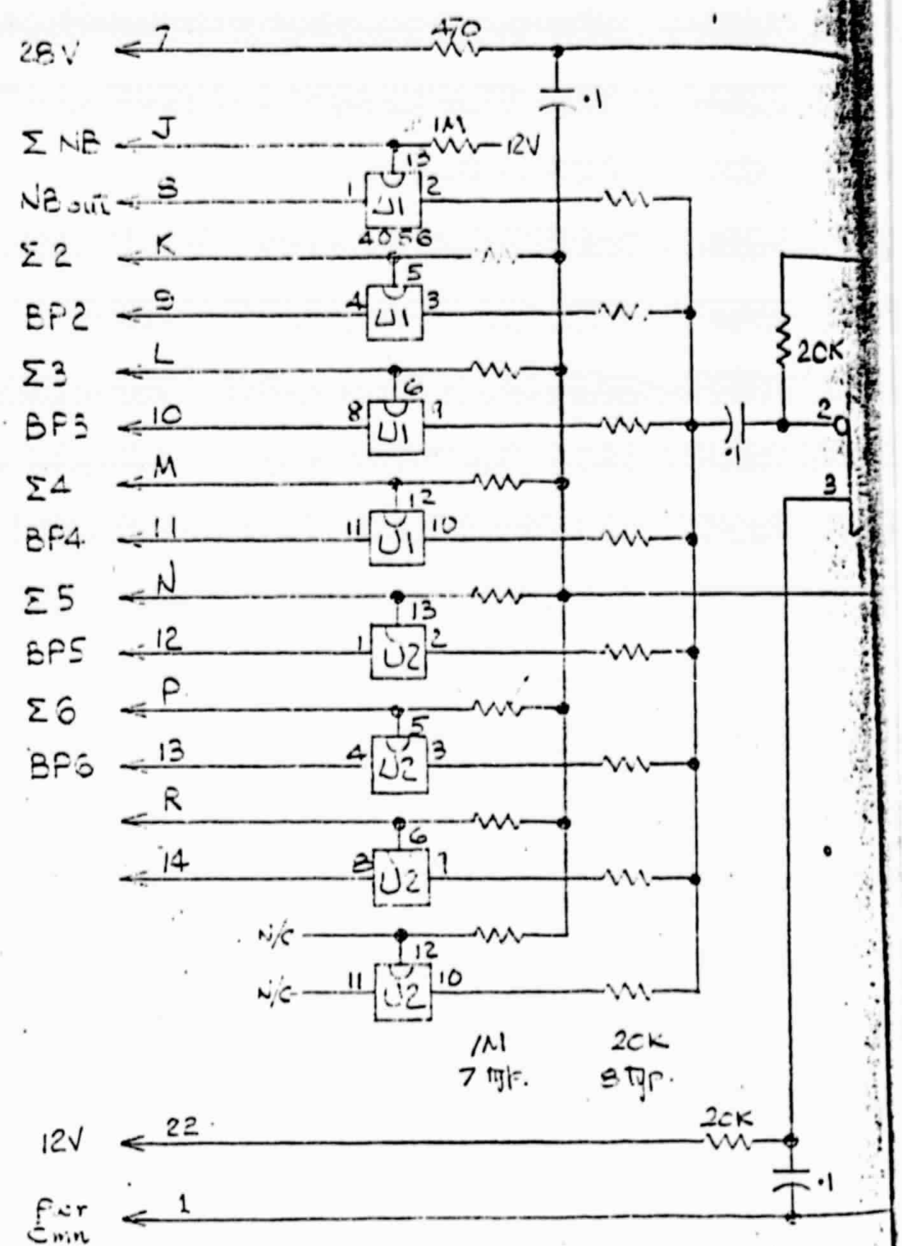
TITLE

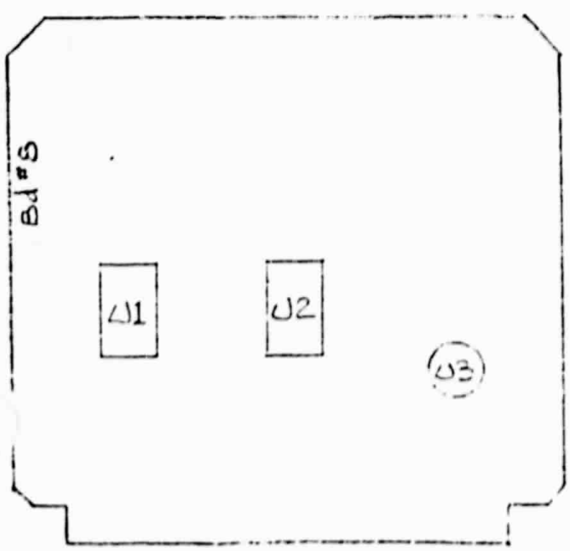
SUMMING AMPLIFIER

PARTS LIST NUMBER REV

P/L 105939 —

SHEET 1 OF 1





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APPLICATION		

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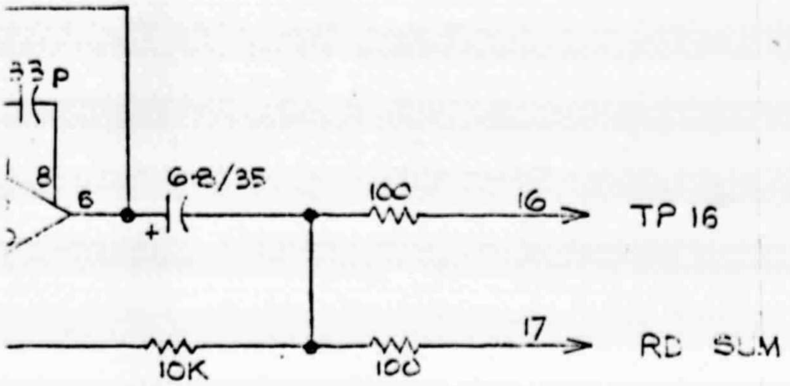

NOTES: (1) U1 & U3 have pin #4 to 12V & pin #7 to power common.

SIGN OFF	INITIALS	DATE
DRAWN	[illegible]	[illegible]
CHECKED		
APPROVED		
ENGINEER	C Kwong	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE
SUMMING AMPLIFIER
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SIZE	CODE IDENT NO	DRW NO	REV
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ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO
1	105940	SCHEMATIC & ASSY | B6		R
[illegible]		PC BOARD 12DE3GP		1
3				
4		IC RCA CA3080A		2
5		" " CA 3100T		1
6		" " CA3094T		1
7		TRANSFORMER	T1	1
8	—			
9	47-101277-01	INDUCTOR 225 mH	L1	1
10	47-101278-01	" 3.19 mH	L2	1
11				
12		RESISTOR 1/4W 5% 2.7 Ω		1
13		470 Ω		3
14		5.1K		2
15		100 Ω		4
16		1K		3
17		27K		2
18		110K		1
[illegible]		4.7K		1
20		1.1K		1
21		110		1
22		1/4W 5% 1.2K		1
23		RESISTOR 1/8W 1% 10K		2
24		" 1/4W 5% 390 Ω		1
25		" " " 560 Ω		1
26		TRANSISTOR 2N2484		1
27		CAPACITOR D.Tant 6.8 10V		2
28		" " 6.8 35V		1
29		MICA 10P		1
30		CK05 .1		5
31		[illegible] 110		1
32		[illegible] 3000P		1
33		CAPACITOR Sprague .22		1

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BY MCM | CK.

APR. [illegible] 9/1/76 | APR.

TITLE INPUT BUFFER & CHANNEL 6KHZ

PARTS LIST NUMBER: P/L 105940 | REV —

SHEET 1 OF 2

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NC					
34		CAPACITOR CK05 1000P		1					
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36		" CK05 150P		1					
37									
38									
39									
40									
41									
42									
43									
44									
45									
46				–					
47									
48									
49									
50									
51									
52									
53									
54									
55									
56									

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TITLE INPUT BUFFER & CHANNEL GATE	
PARTS LIST NUMBER P/L 105940	REV –
SHEET 2 OF 2	

DEVELCO, INC.

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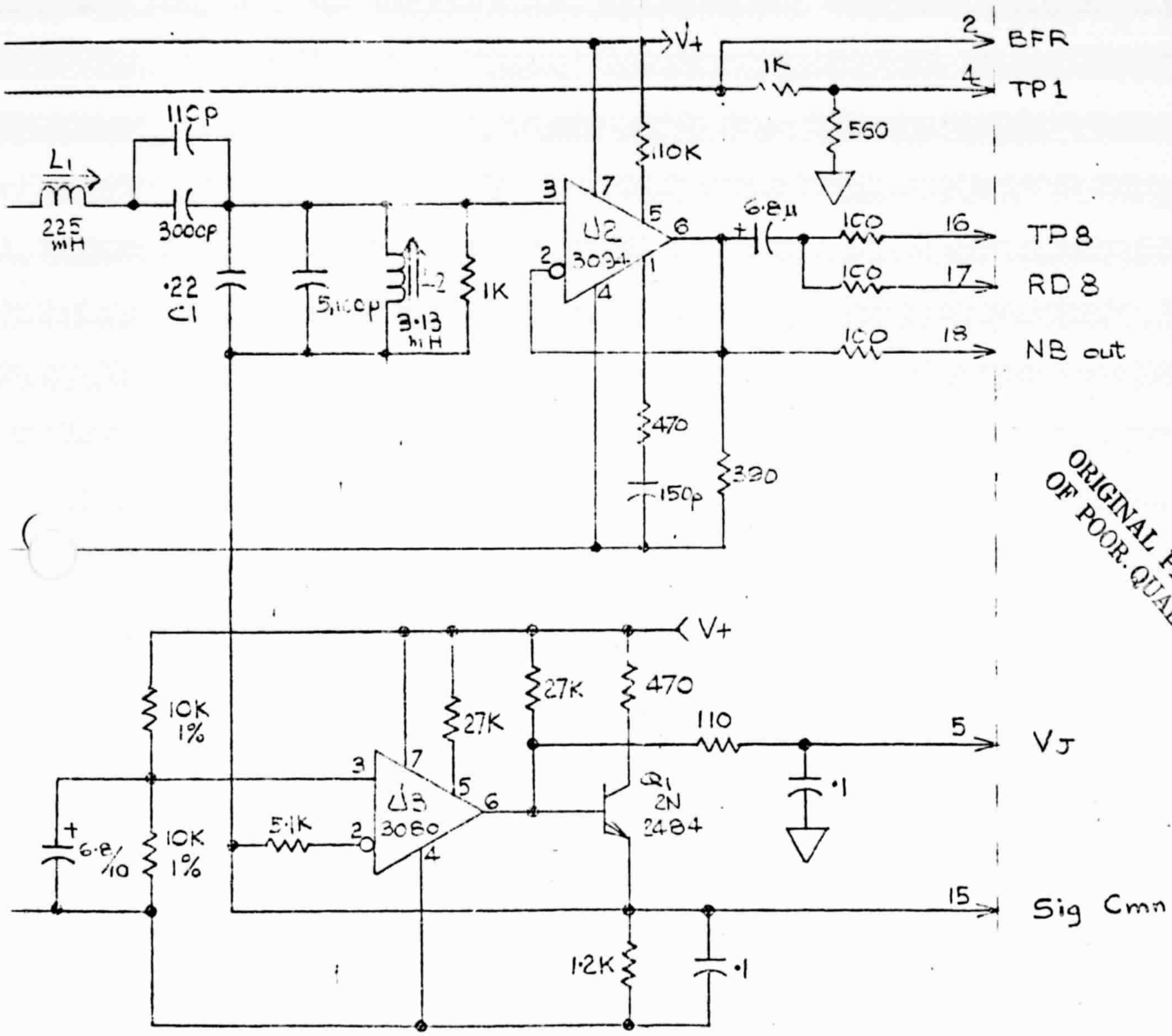
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



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DRAWN	[illegible]	[illegible]
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APPROVED		
ENGINEER	C. Kuong	15Jul76
PROJ ENGR		

DEVELCO INC.

TITLE: INPUT BUFFER & CH 6KHz SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
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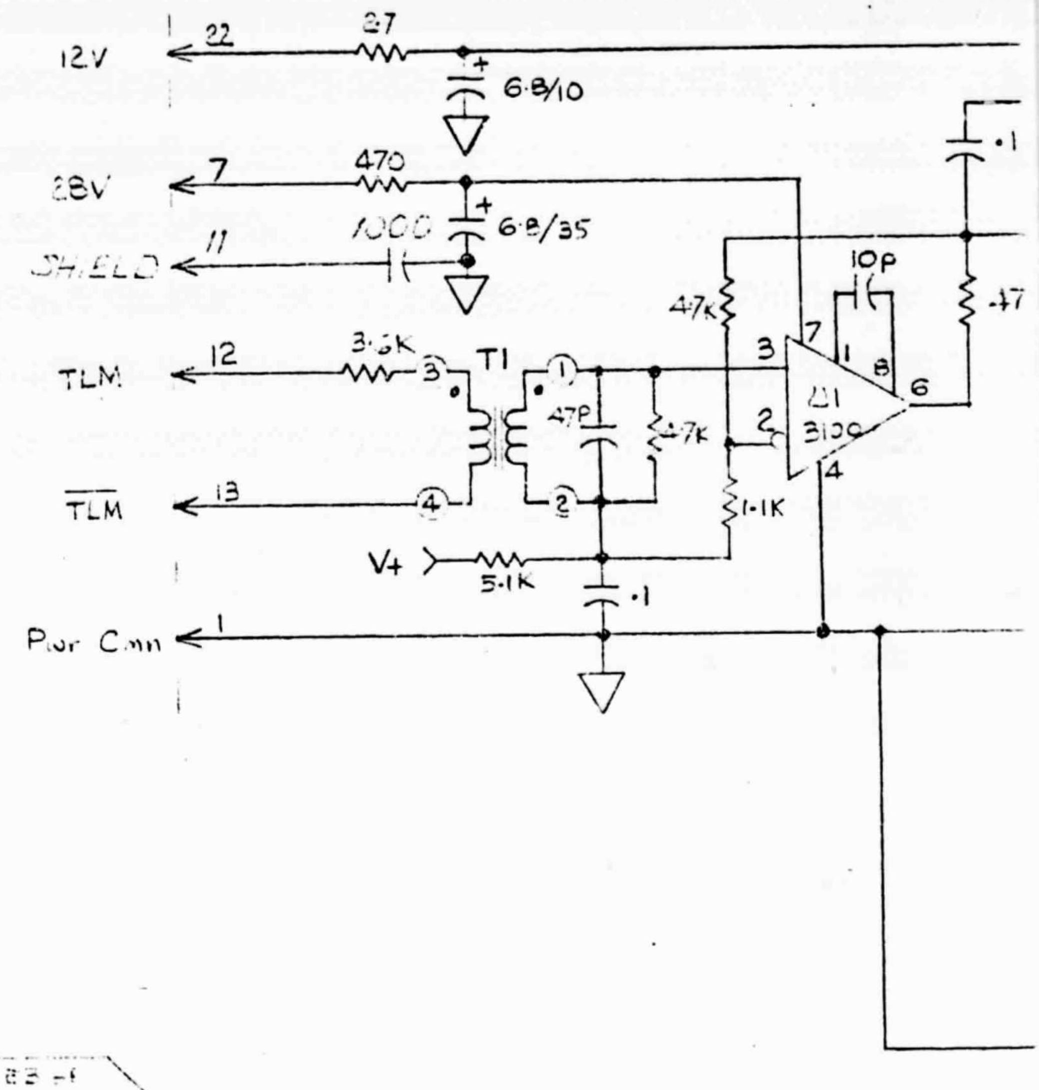

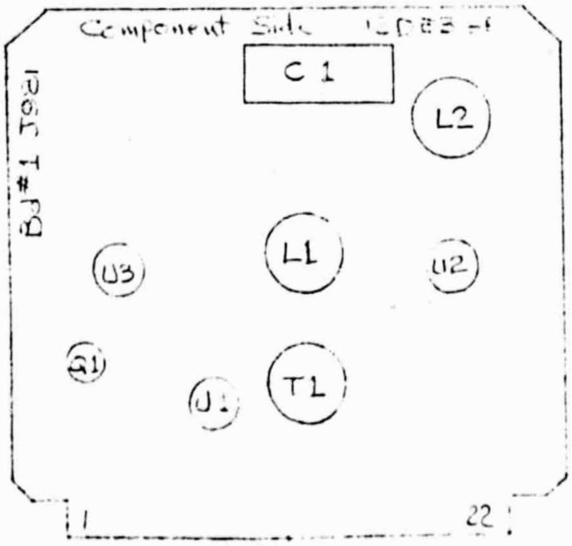

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APPLICATION		

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1	105941	SCHEMATIC & ASSY B6		R
2		PC BOARD 120E36P		1
3		IC CD4046AE		1
4		" CA3080A		2
5		" CA3094T		1
6		RESISTOR 1/4W 5% 10K		1
7		160Ω		1
8		30K		1
9		20K		4
10		62K		1
11		33K		1
12		56K		1
13		220		3
14		2.7		2
15		1K		2
16		11K		2
17		5.1K		1
18		27K		1
19		91K		1
20		620K		1
21		RESISTOR 1/4W 5% 100K		2
22		" 1/8W 1% 301K		1
23		CAPACITOR STYRO 390		2
24		" 2000		2
25		CK05 1000P		2
26		STYRO .036		1
27		" 1200		1
28		D TANT 6.3 /10V		4
29		CK05 .01		1
30		MYLAR 5% .1		4
31		" " .027		1
32		CYFD FTR 130P		1
33		CAPACITOR MYLAR 5% .15		1

REV

BY MCM | CK.

APR. EN 9/11/.. | APR.

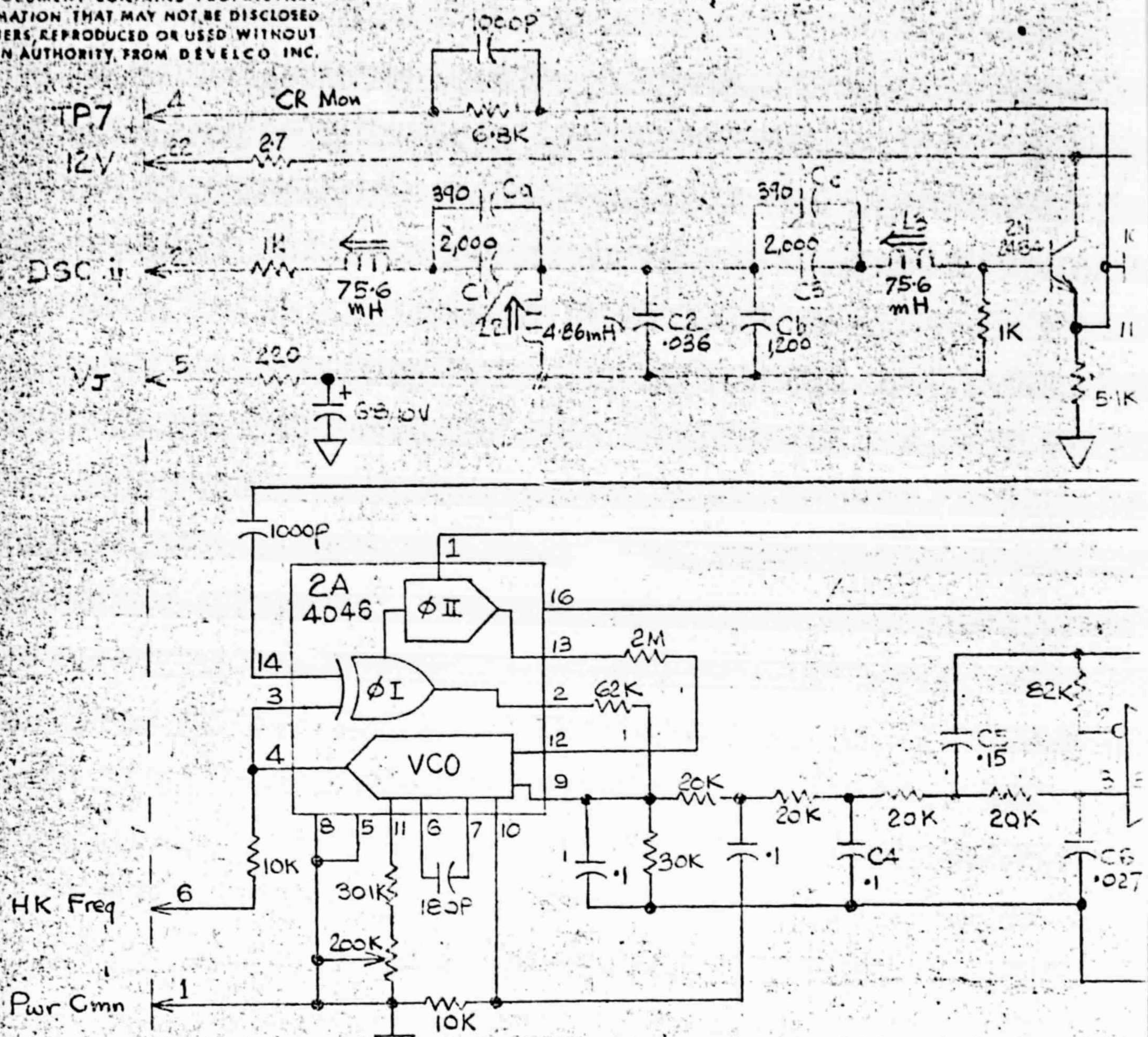
TITLE DISCRIMINATOR

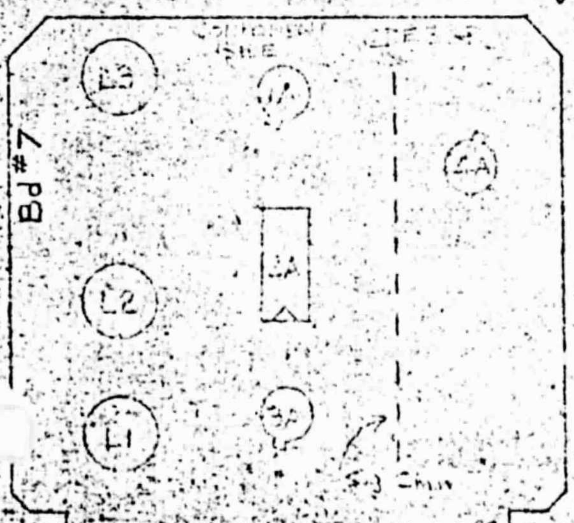
PARTS LIST NUMBER | REV

P/L 105941 | —

SHEET 1 OF 2

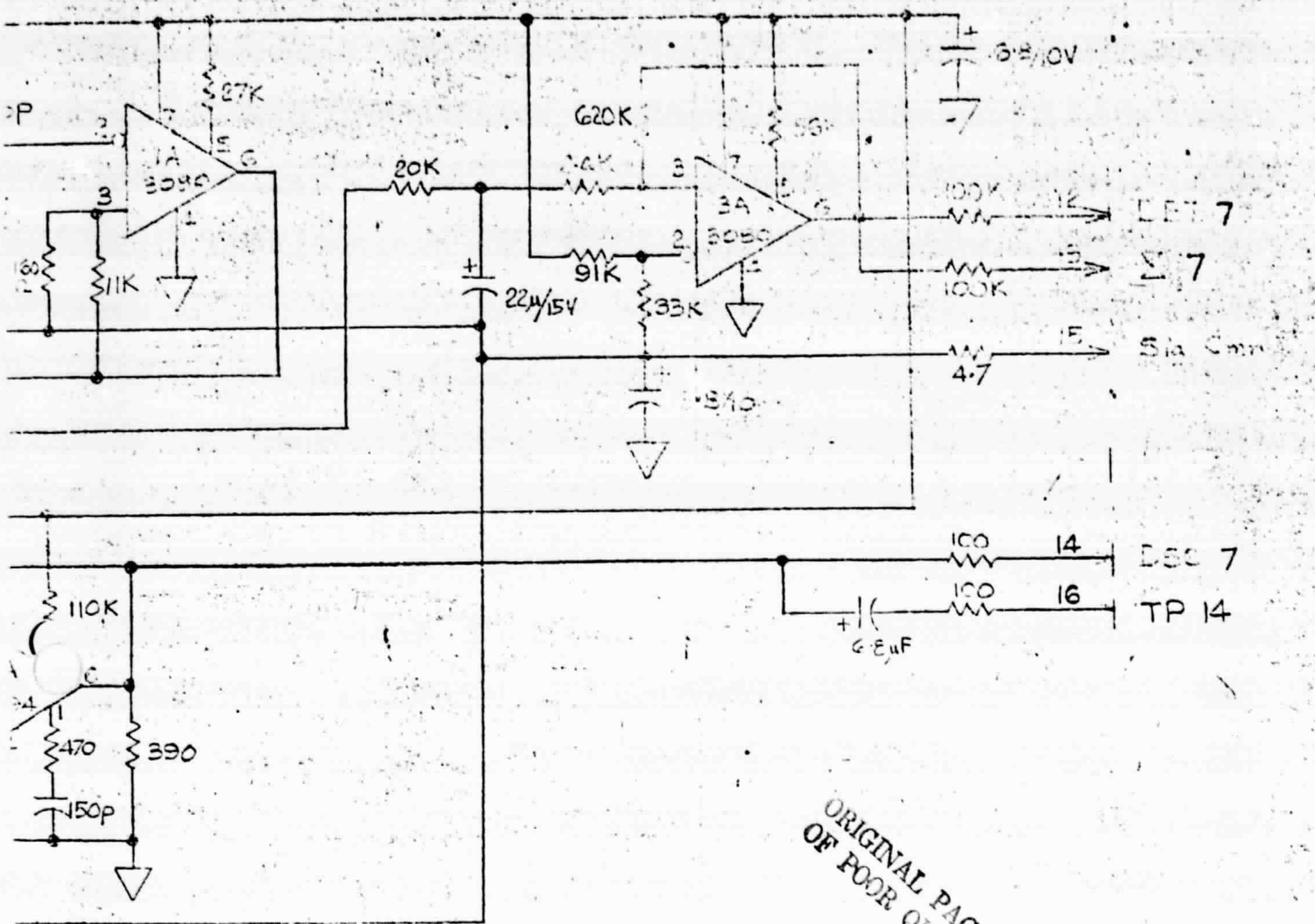
DEVELCO, INC.





USED ON	NEXT ASS'Y	QTY REQD
	APPLICATION	

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



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SIGN-OFF	INITIALS	DATE
DRAWN	ea	3/10/75
CHECKED		
APPROVED		
ENGINEER	C. Kwong	13 Jy 76
PROJ ENGR		

House Keeping Channel

DEVELCO INC.

TITLE: DISCRIMINATOR SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105941	

SCALE | DO NOT SCALE DRAWING | SHEET OF

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO. -1	-2	-3	-4	-5	
1	105942	SCHEMATIC & ASSY BC		R	R	R	R	R	
[illegible]		PC BOARD 12DE3GP		1	1	1	1	1	
3		IC CD4046AE		1	1	1	1	1	
4		" CA3080A		2	2	2	2	2	
5		IC CA3094T		2	2	2	2	2	
6									
7		TRANSISTOR 2N2434		1	1	1	1	1	
8									
9		RESISTOR 1/4W 5% 6.8K		2	2	2	3	2	
10		4.7Ω		1	1	1	1	1	
11		1K		5	2	2	2	2	
12									
13		10K		3	3	3	3	3	
14		3.6K		1	1	1	1	1	
15		2.4K		4	3	3	3	3	
16		5.1K		1	1	1	1	1	
17		11K		2	2	2	2	2	
18		160Ω		1	1	1	1	1	
[illegible]		27K		2	2	2	2	2	
20		20K		1	1	1	2	1	
21		2.7Ω		1	1	1	1	1	
22		620K		1	1	1	1	1	
23		91K		1	1	1	1	1	
24		33K		1	1	1	1	1	
25		30K		2	2	2	2	2	
26		100Ω		3	3	3	3	3	
27		390		1	1	1	1	1	
28		110K		2	2	2	2	2	
29		470		2	2	2	2	2	
30		10K		-	-	1	-	-	
31		39K		-	-	-	-	1	
32		820Ω		1	-	-	-	-	
33		RESISTOR 1/4W 5% 1.6K		-	1	-	-	-	

REV

FREQ
-1 384 KHz
-2 192 "
-3 96 "
-4 48 "
-5 24 "

BY MCM | CK.

APR. [illegible] 9/1/7[illegible] | APR.

TITLE DISCRIMINATOR

PARTS LIST NUMBER P/L 105942 | REV —

SHEET 1 OF 3

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	-1	-2	-3	-4	-5
34		RESISTORS 1/4W 5% 3.3K		-	-	1	-	-
[illegible]		13K		-	-	-	-	1
36		2K		-	3	-	-	-
37		3.9K		-	-	3	-	-
38		8.2K		-	-	-	3	-
39		16K		-	-	-	-	3
40		240K		1	-	-	-	-
41		510K		-	1	-	-	-
42		1M		-	-	1	1	-
43		1/4W 5% 2M		-	-	-	-	1
44								
45		1/8W 1% 40.2K		-	1	-	-	-
46		20K		1	-	-	-	-
47		30.6K		-	-	1	1	-
48		RESISTOR 1/8W 1% 150K		-	-	-	-	1
49								
50		RESISTOR POT BECKMAN 3329H 10K		1	-	-	-	-
51		" 20K		-	1	-	-	-
[illegible]		" 50K		-	-	1	1	-
[illegible]		RESISTOR POT " 100K		-	-	-	-	1
54								
55								
56		CAPACITOR DIP TANT 6.8/10V		4	4	4	4	4
57		CK05 1000P		3	3	3	3	3
58		DIP TANT 22μ/15V		1	1	1	1	1
59		CK05 .01		2	2	2	2	2
60		CK05 150P		1	1	1	1	1
61		STYRO 360P		1	1	1	1	1
62		[illegible] MYLAR .047		1	1	1	1	1
63		STYRO 9100P		1	1	1	1	1
64		[illegible] .1		1	1	1	1	1
65		NPO CER 51P		1	1	1	-	-
66		CAPACITOR [illegible] 180P		-	-	-	1	1

REV

BY	CK.
APR.	APR.
TITLE DISCRIMINATOR	
PARTS LIST NUMBER P/L 105742	REV -
SHEET 2 OF 3	

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION			REFERENCE	QUANTITY/DASH. NO -1	-2	-3	-4	-5
67		CAPACITOR	STYRO	110P		2	–	–	–	–
[illegible]			"	220P		–	2	–	–	–
69			"	430P		–	–	2	–	–
70			"	910P		–	–	–	2	–
71			"	1900		–	–	–	–	2
72			"	680P		1	–	–	–	1
73			"	1500P		–	1	–	–	–
74			"	3000		–	–	1	–	–
75			"	6200		–	–	–	1	–
76			"	.012		–	–	–	–	1
77			"	100P		1	–	–	–	–
78			"	68p		–	1	–	–	–
79			"	150p		–	–	1	–	–
80			STYRO	15p		–	–	1	–	–
81			CK05	510		1	–	–	–	–
82			"	1000		–	1	–	–	–
83			"	2000		–	–	1	–	–
84			"	3900		–	–	–	1	–
85		CAPACITOR	"	8200		–	–	–	–	1
86										
87	47-101279-01	INDUCTOR		1.61 mH	L1, L3	2	–	–	–	–
88	1281			3.22 "	L1, L3	–	2	–	–	–
89	1283			6.43 "	L1, L3	–	–	2	–	–
90	1285			12.9 "	L1, L3	–	–	–	2	–
91	1287			25.7 "	L1, L3	–	–	–	–	2
92	1280			231 μH	L2	1	–	–	–	–
93	1282			462 "	L2	–	1	–	–	–
94	1284			926 "	L2	–	–	1	–	–
95	1286			1.85 mH	L2	–	–	–	1	–
96	47-101288-01	INDUCTOR		3.70 "	L2	–	–	–	–	1
97										
98										
99										

REV

BY | CK.

APR. | APR.

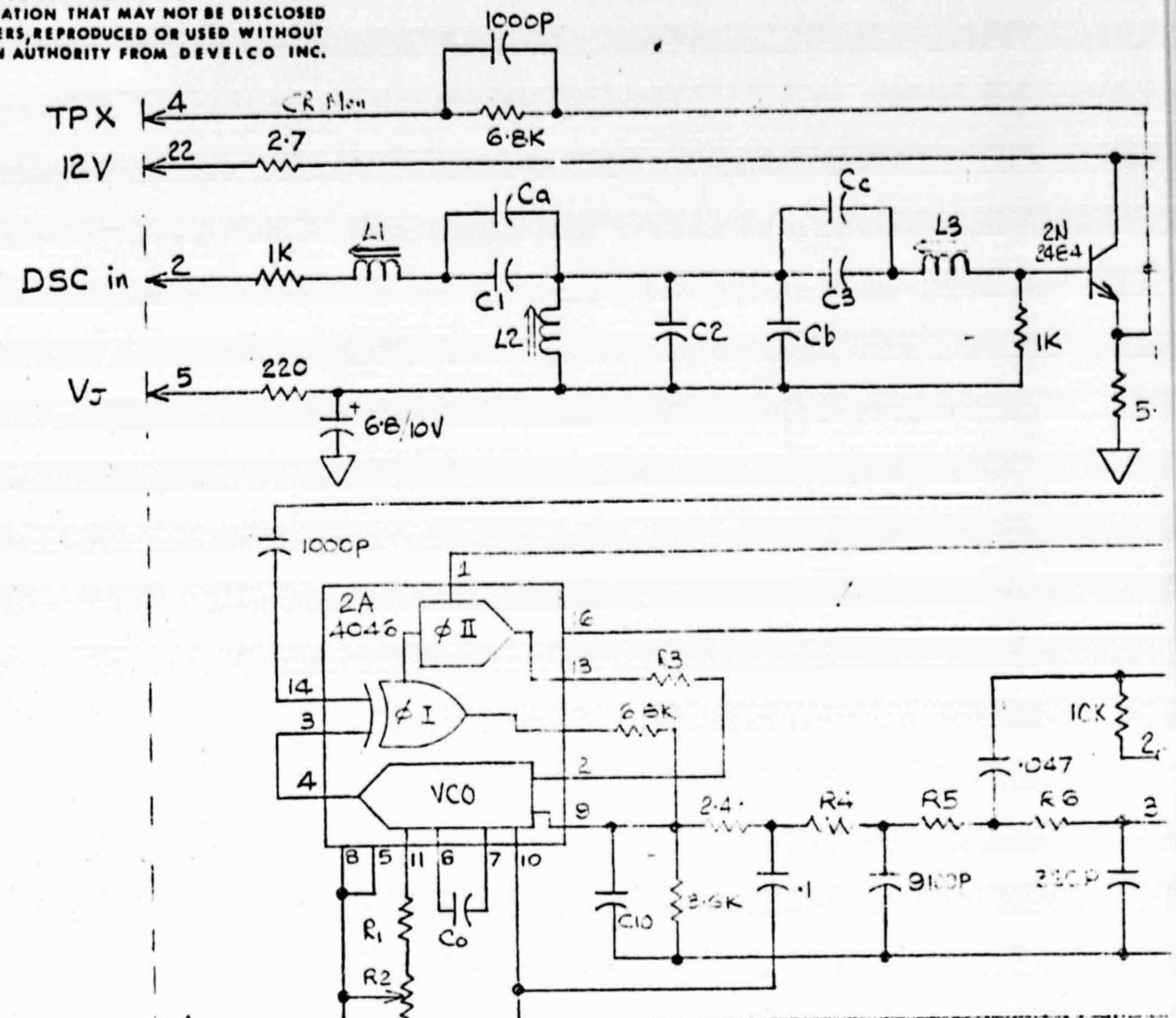
TITLE DISCRIMINATOR

PARTS LIST NUMBER | RE

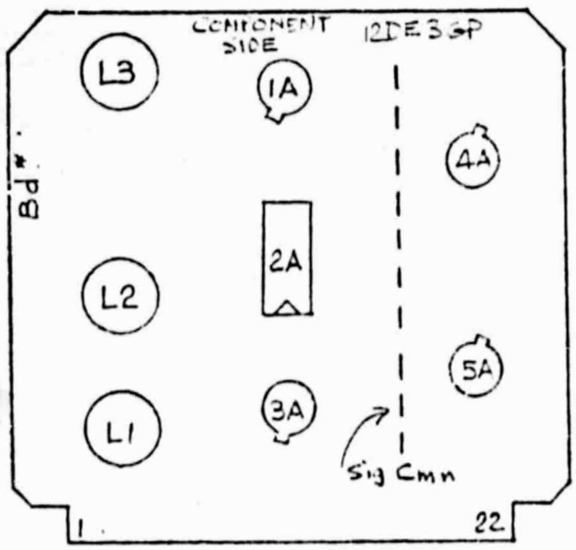
P/L 105942

SHEET 3 OF 3

DEVELCO, INC.

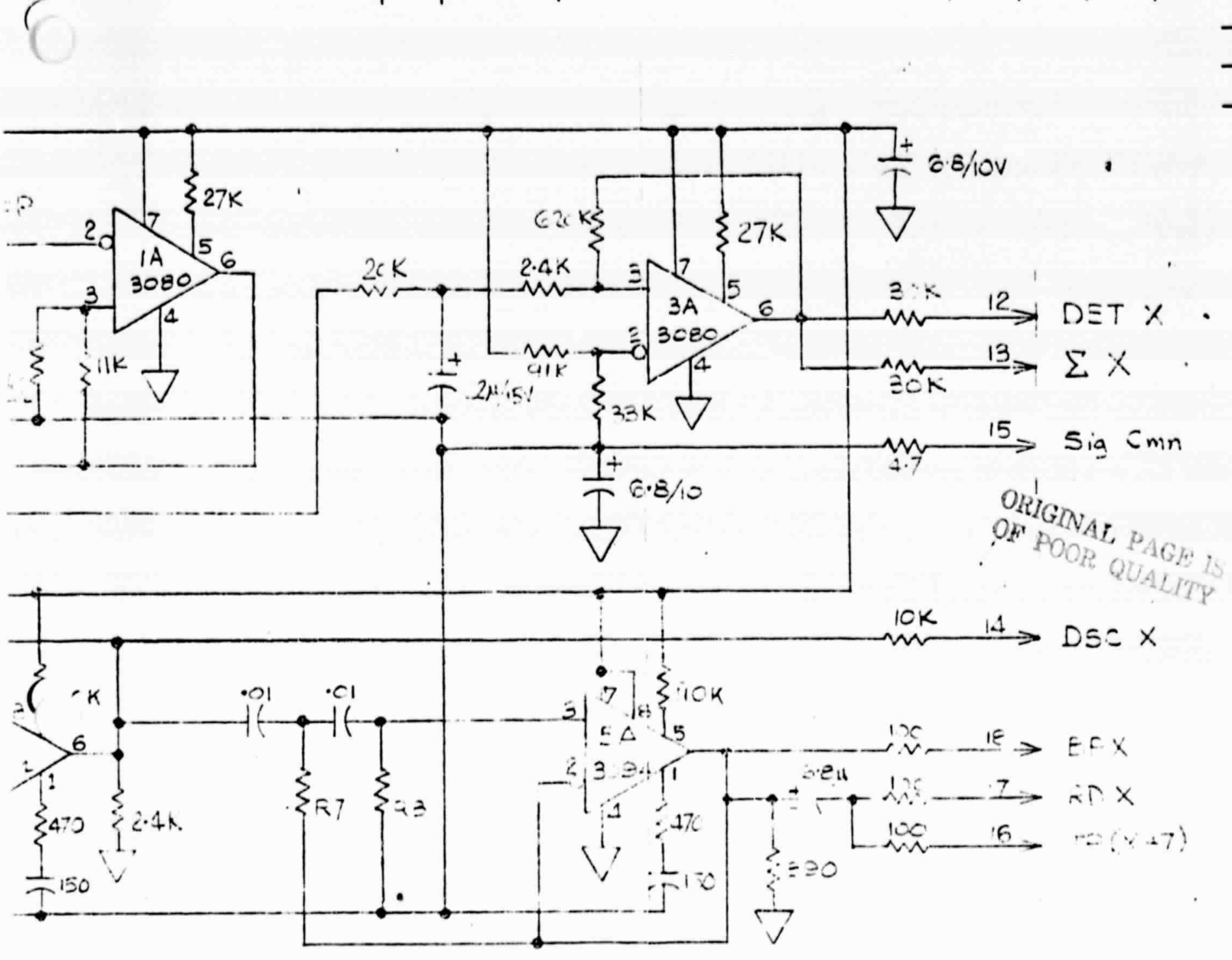


f_0 (kHz)	Co	R_1	R_2	L_1, L_3	L_2
384	51 P	20K	10K	1.6 mH	231
192	51 P	40.2K	20K	3.22mH	46
96	51 P	80.6K	50K	6.43	92
48	180 P	80.6K	50K	12.9	1.85
24	180P	150K	100K	25.7	3.70



USED ON	NEXT ASS'Y	QTY REQ
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



C3	Ca, Cc	C2	Cb	R	R4,5,6	R7	R8	C4	[illegible]	B1#
[illegible]F	—	680P	100P	240K	1K	820Ω	2.4K	510	[illegible]	2
220P	—	1,500P	68P	510K	2K	1.6K	4.7K	1,000	[illegible]	3
130P	15P	2,000P	15P	1M	3.3K	3.3K	10K	2,000	[illegible]	4
[illegible]10P	—	6,200P	110P	1M	8.2K	6.8K	20K	3,900	[illegible]	5
800P	—	.012	680P	2M	16K	13K	39K	8,200	[illegible]	6

SIGN OFF	INITIALS	DATE
DRAWN	[illegible]	[illegible]
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE

DISCRIMINATOR
SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	[illegible]	

SCALE | DO NOT SCALE DRAWING | SHEET OF

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO
1	105943	SCHEMATIC & ASSY	B6		R
2		PC BOARD [illegible]			1
3		IC RCA CA3080A		U1	1
4		" " CA3094T		U4	1
5		" [illegible] 440T		U5	1
6		IC RCA CA3096E		U3, U7	2
7		IC NATIONAL [illegible]		[illegible] U6	[illegible]
8		TRANSISTOR 2N2484		-	2
9		RESISTOR 1/4W 5% 100Ω			2
10		10K			[illegible]
11		4.7			2
12		390			1
13		27K			2
14		47K			1
15		220			1
16		100K			1
17		68K			1
18		6.8K			2
19		470			1
20		560K			2
21					
22		30K			[illegible]
23		9.1K			4
24		300			2
25		33K			2
26		51K			2
27		VARIABLE 10K		R2, R4, R3	3
28		" 100Ω		R5	1
29		RESISTOR " 200Ω		R1	1
30					
31		CAPACITOR CK05 .001			2
32		" .01			2
33		D. [illegible] 6.8 [illegible]			[illegible]

BY [illegible] | CK.

APR. [illegible] 9/1/7[illegible] | APR.

TITLE METER AMP

REV

PARTS LIST NUMBER

P/L 105943

REV —

SHEET 1 OF 2

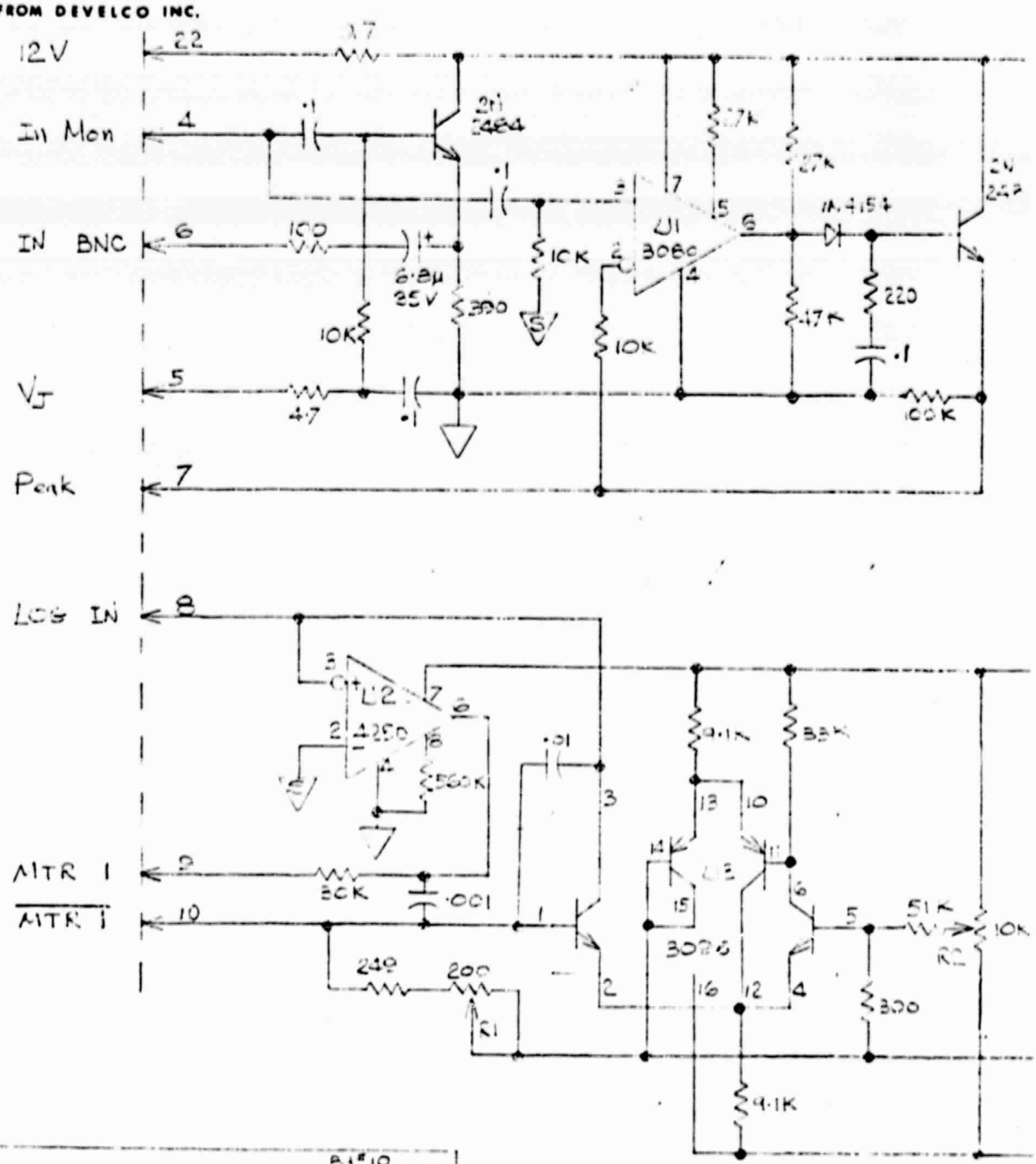
DEVELCO, INC.

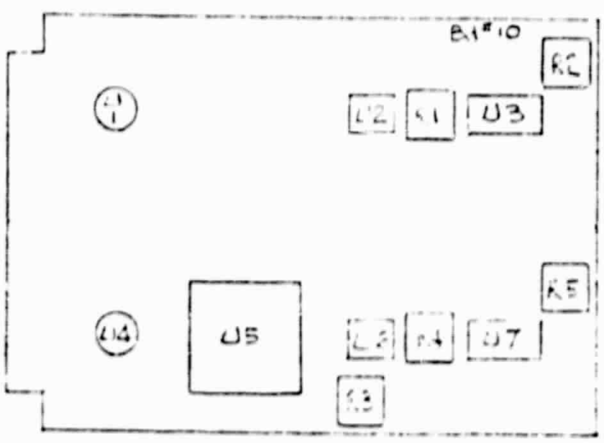
ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.
34		CAPACITOR CK05 .1		5
		" CK05 150pf		1
36		" DIP TANT 22uf		1
37				
38				
39		DIODE 1N4154		1
40				
41		RESISTOR 1/8W 1% 249		2
42		" " " 10K		1

BY MCM	CK.
APR.	APR.
TITLE METER AMP	
PARTS LIST NUMBER P/L 105943	REV —
SHEET 2 OF 2	

REV

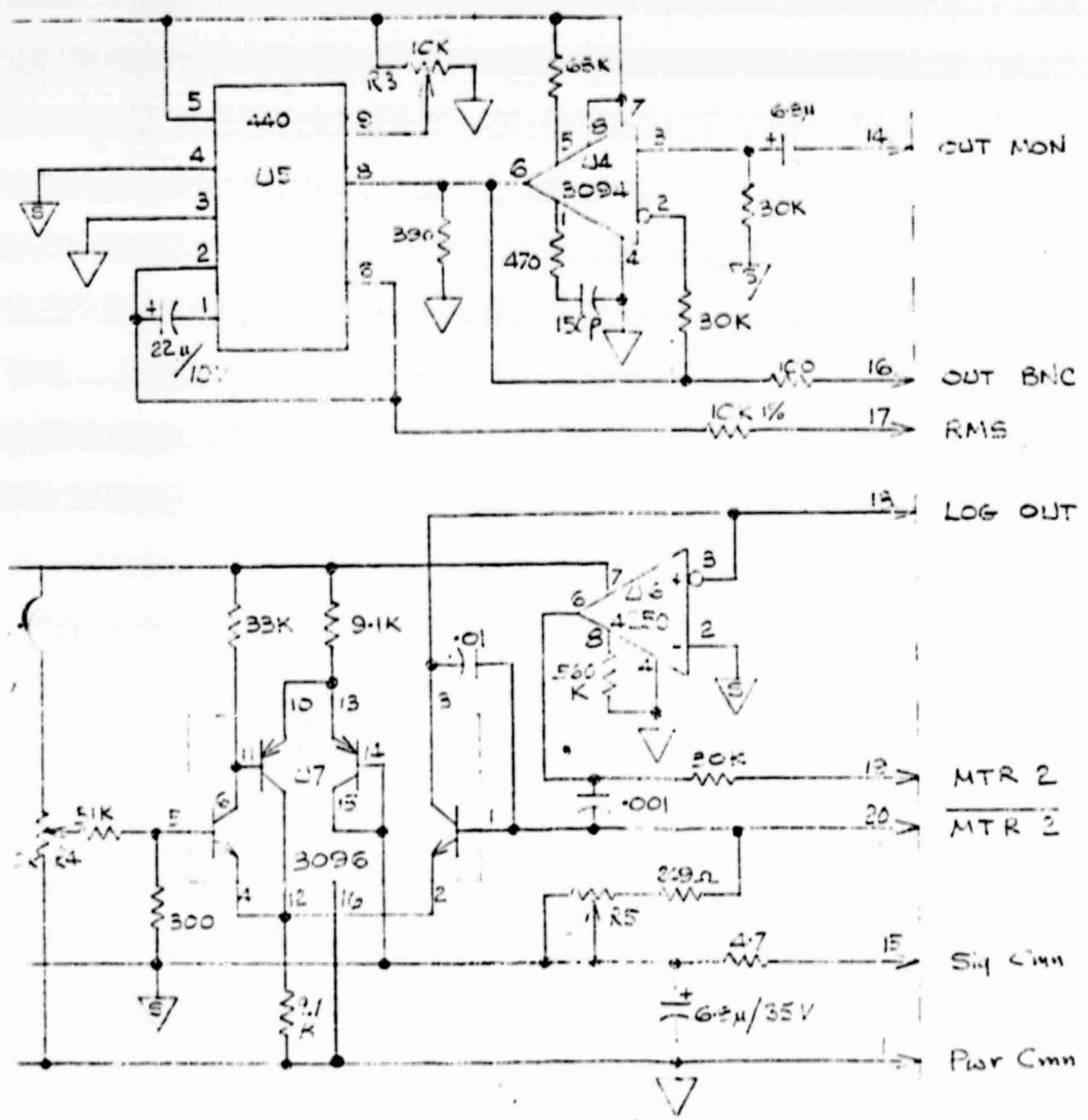
DEVELCO, INC.





USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



SIGN OFF	INITIALS	DATE
DRAWN	EJC	
CHECKED		
APPROVED		
ENGINEER	C Curry	13 Jul 76
PROJ ENGR		

B1#10

DEVELCO INC.

TITLE: METER AMP
SU/G8E

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105143	

SCALE | DO NOT SCALE DRAWING | SHEET | OF

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.					
1	105944	SCHEMATIC & ASSY | 8G		R					
2		PC BOARD 112DE6G:P		1					
3	CD4029AE	IC	U7,U12,U10,U11	4					
4	" 4046 "	"	U9,	1					
5	CD4013AE	"	U3,	1					
6	CA3080A	"	U1 THRU U4	4					
7	CD4066AE	"	U6	1					
8	CD4030AE	IC	U14	1					
9	CA3094T	IC	U5	1					
10		RESISTOR 1/4W 5% 2.7		1					
11		56M		1					
12		560K		2					
13		51K		2					
14		33K		2					
15		3.3M		2					
16		120K		2					
17		10M		2					
18		.82M		1					
19		100K		2					
20		200K		1					
21		220		1					
22		110 K		1					
23		10K		2					
24		5.6K		5					
25		1M		1					
26		390Ω		1					
27		430Ω		1					
28		1/4W 5% 150K		1					
29	BECKMAN 3329H-50K	RESISTOR, VARIABLE 50K		1					
30									
31		CAPACITOR D.TANT 6.8 35V		1					
32		" CK05 1000 P		3					
33	ET1405K.5A REL CAP.	" POLY 4		3					

REV

BY MCM	CK.
APR. [illegible] 9/1/7.	APR.
TITLE DETECTOR & CLOCK GEN	
PARTS LIST NUMBER P/L 105944	REV —
SHEET 1 OF 2	

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO
34		CAPACITOR STYRO 2,200p		1
35		STYRO 6,200P		1
[illegible]		5% MYLAR .082		1
37		NPO CER 180p		1
38				
39		CAPACITOR POLY .1u		2
40		" POLY .56		1
41				
42		DIODE 1N270		2
43				
44				
45				
46				
47				
48				
49				
50				

RE

BY | CK.

APR. | APR.

TITLE

DETECTOR & CLOCK GEN

PARTS LIST NUMBER | REV

P/L 105944 | —

SHEET 2 OF 2

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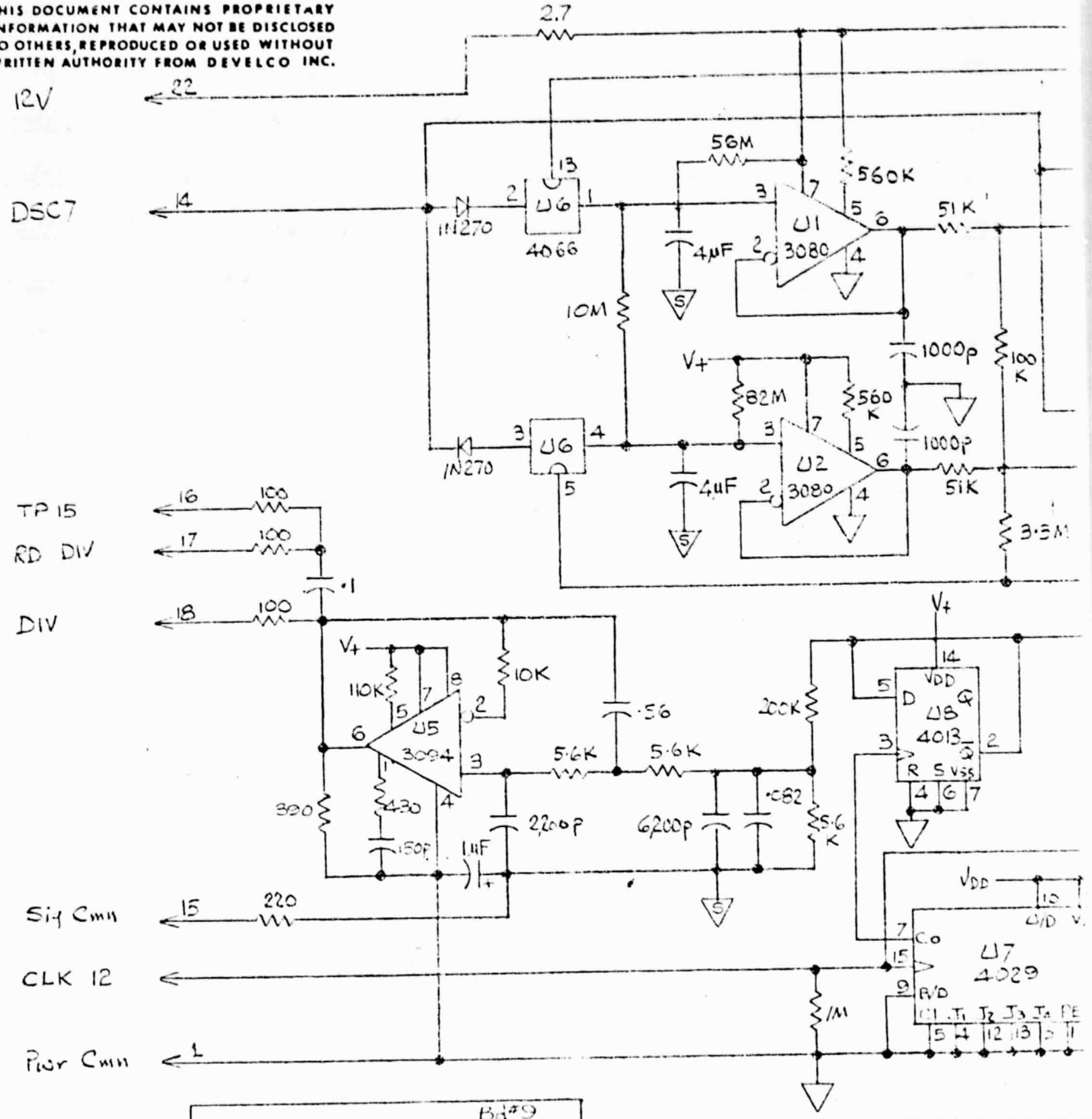
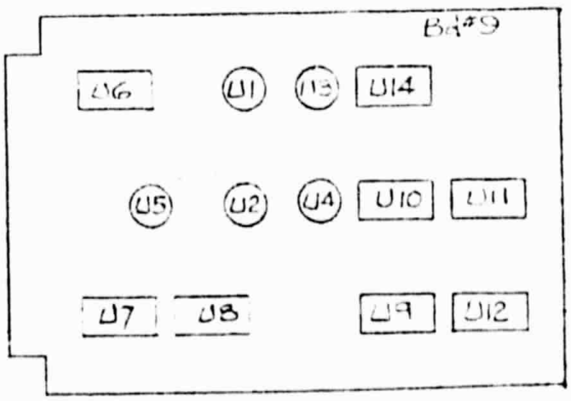
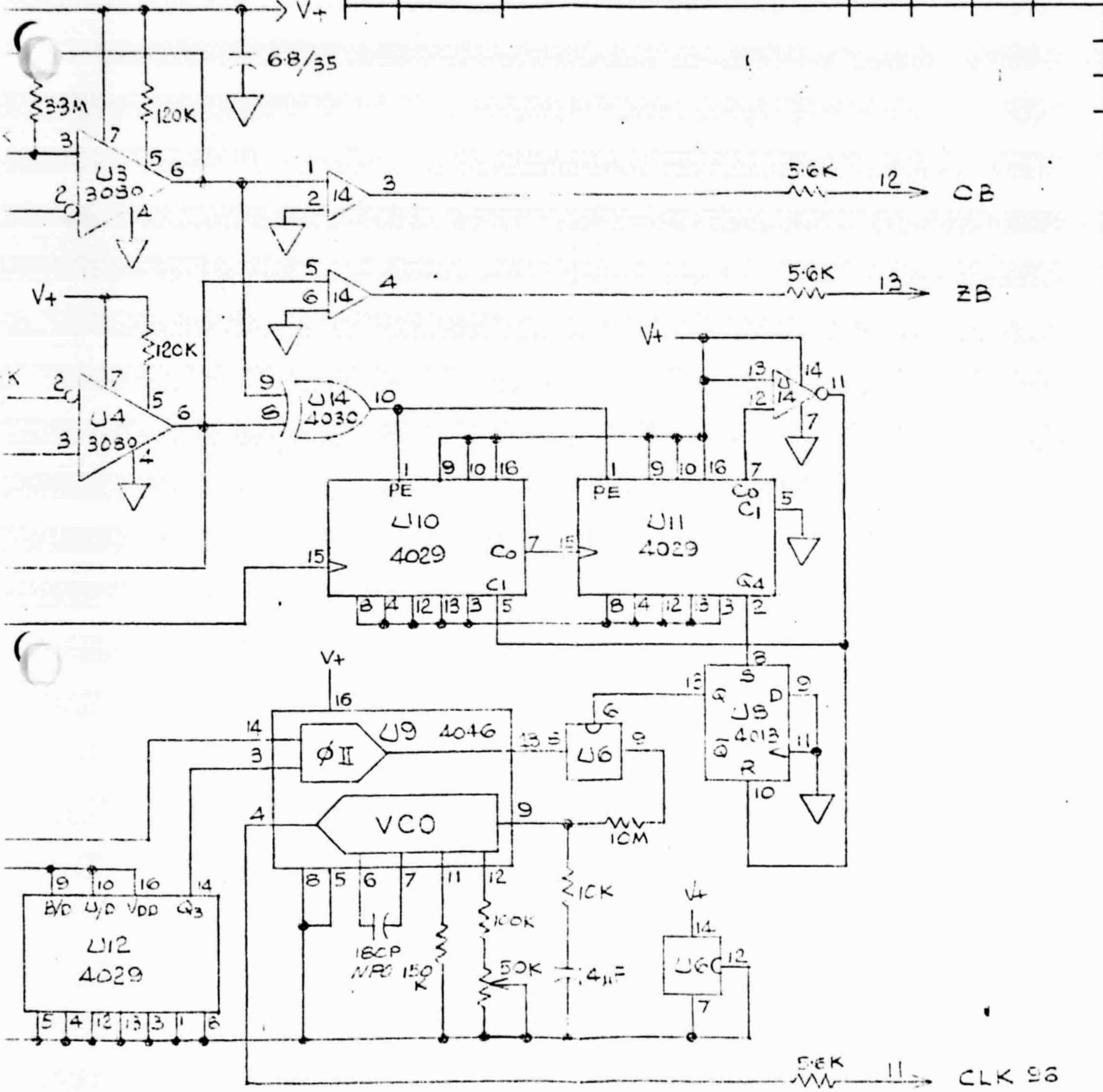




USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



SIGN OFF		
	INITIALS	DATE
DRAWN	Ca	11Nov75
CHECKED		
APPROVED		
ENGINEER	C.Kwon	13Jul76
PROJ ENGR		

Bd # 9

DEVELCO INC.

TITLE: DETECTOR & CLOCK GEN. SU / GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105944	

SCALE	DO NOT SCALE DRAWING	SHEET	OF

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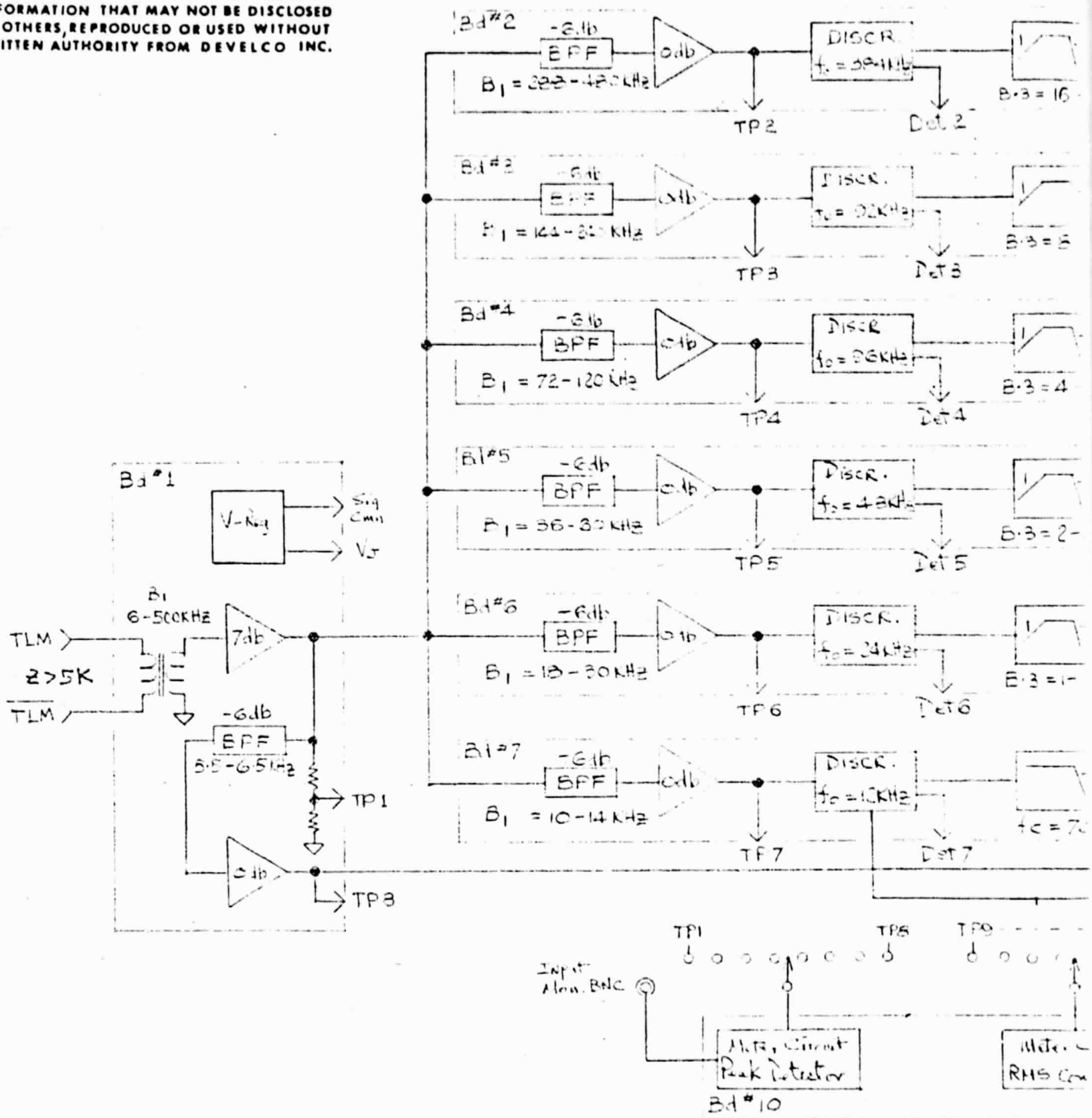
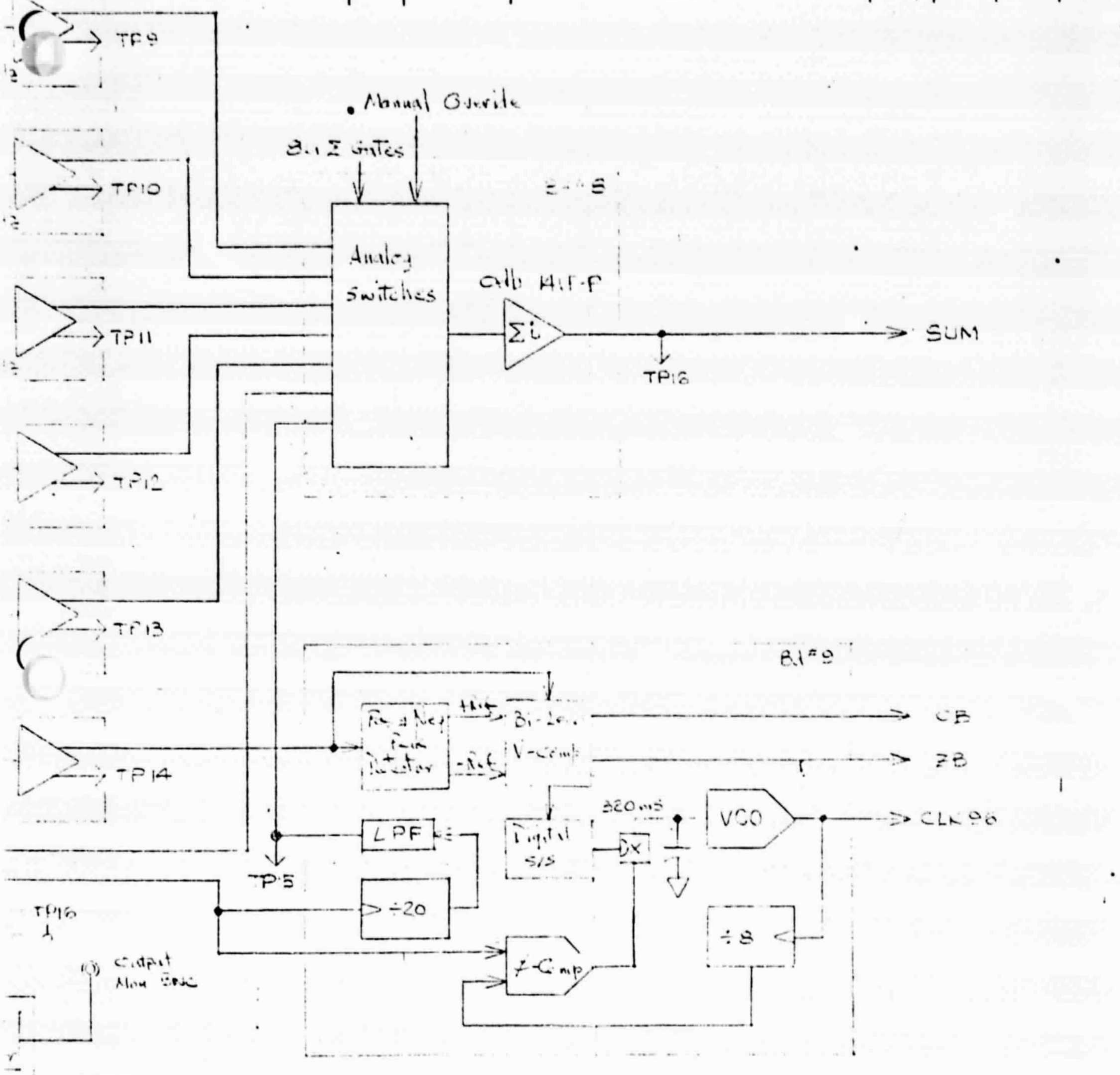


USED ON	NEXT ASS'Y	QTY REQ
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



SIGN-OFF	INITIALS	DATE
DRAWN		13Nov75
CHECKED		
APPROVED		
ENGINEER	C. Lucena	13Jul75
PROJ ENGR		

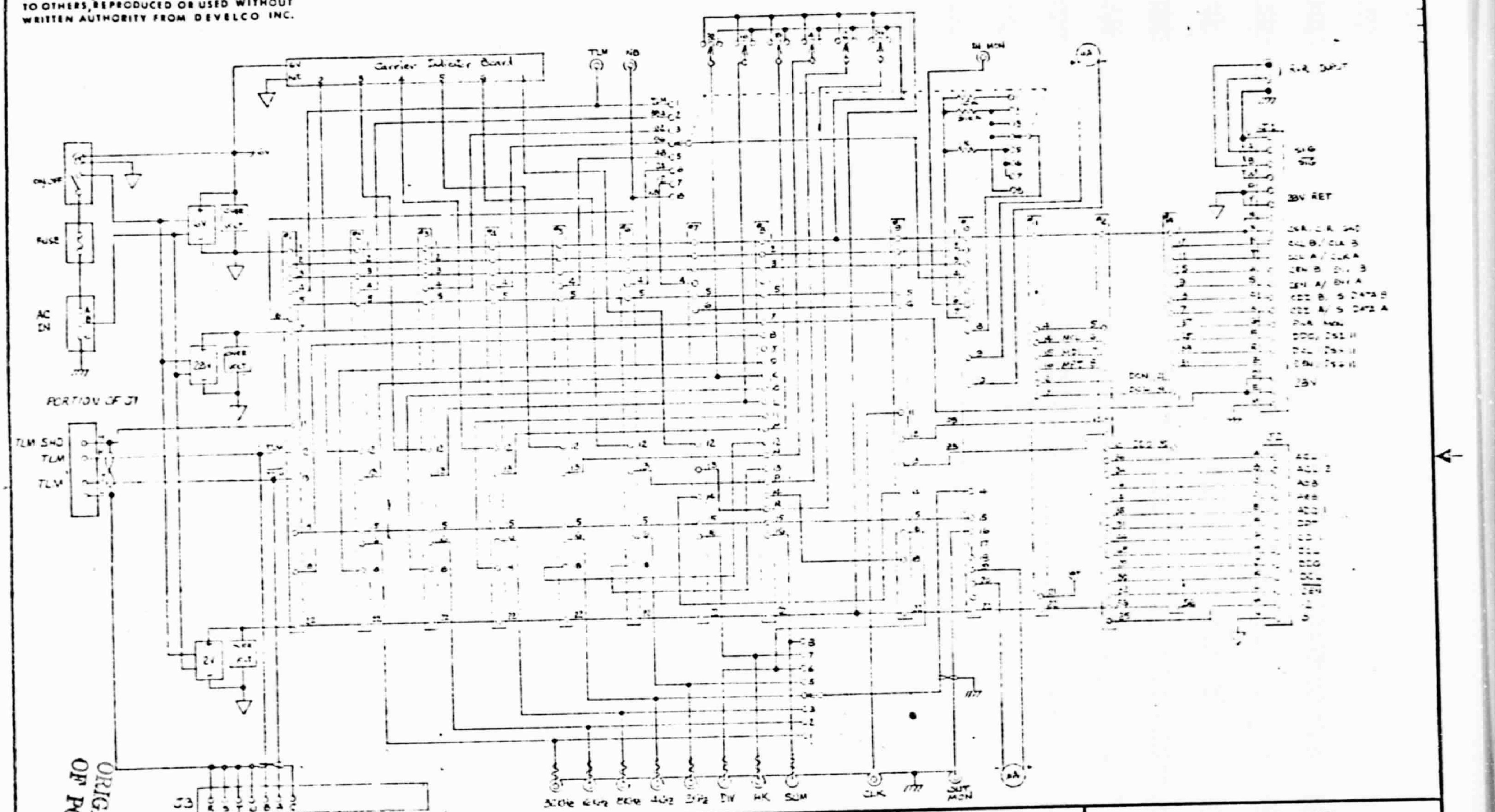
DEVELCO INC.

TITLE ANALOG BLOCK DIAGRAM SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	105945	

SCALE DO NOT SCALE DRAWING SHEET OF

REVISIONS					
SYM	DATE	DESCRIPTION	CKD	APPR	DATE



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			SIGN OFF	INITIALS	DATE
			DRAWN		
			CHECKED		
			APPROVED		
			ENGINEER	C Ca	5 Aug 75
			PROJ ENGR		
USED ON	NEXT ASS'Y	QTY REQD			
APPLICATION					

DEVELCO INC.

TITLE: HEM GSE BACK PLANE

SIZE	CODE IDENT NO	DRW NO	REV
C		G - 105948	
SCALE		DO NOT SCALE DRAWING	SHEET OF

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
1	105953	SCHEMATIC & ASSY D6		R					
	103637-2	P.C. BD C3		1					
4		SOCKET 14 PIN WIRE WRAP		8					
5		" 16 PIN " "		10					
6									
7	CD4011AE	IC	2C,4B,5A,5B	4					
8	4049		2D,5C,6C	3					
9	4013		3A,3B,4C	3					
10	4001		2B	1					
11	CD4017AE	IC	3C,3D	2					
12									
13		TRANSISTOR 2N5816	4D	1					
14									
15		DIODE ZENER 10V 1N961	4D	1					
16.		" " 7.5V 1N953	4D	1					
17		" 1N4143	6D	2					
18		CAPACITOR DIP MICA 500PF		2					
19		" " " 1000PF		7					
20									
21									
22		RESISTOR 1/4W 50% 220K	4A	1					
23		470Ω	4D	1					
24		620Ω	4D	1					
25		100Ω	6D	2					
26		RESISTOR 1/4W 5% 15K	5D	6					
27		" " " 100K	4D,4A	3					
28	-	RESISTOR POT 1 TURN 100K	4A	1					
		" 1/4W 5% 47K	4D	2					

REV		
	PART NO WAS 105885	
A		

BY MCM CK.

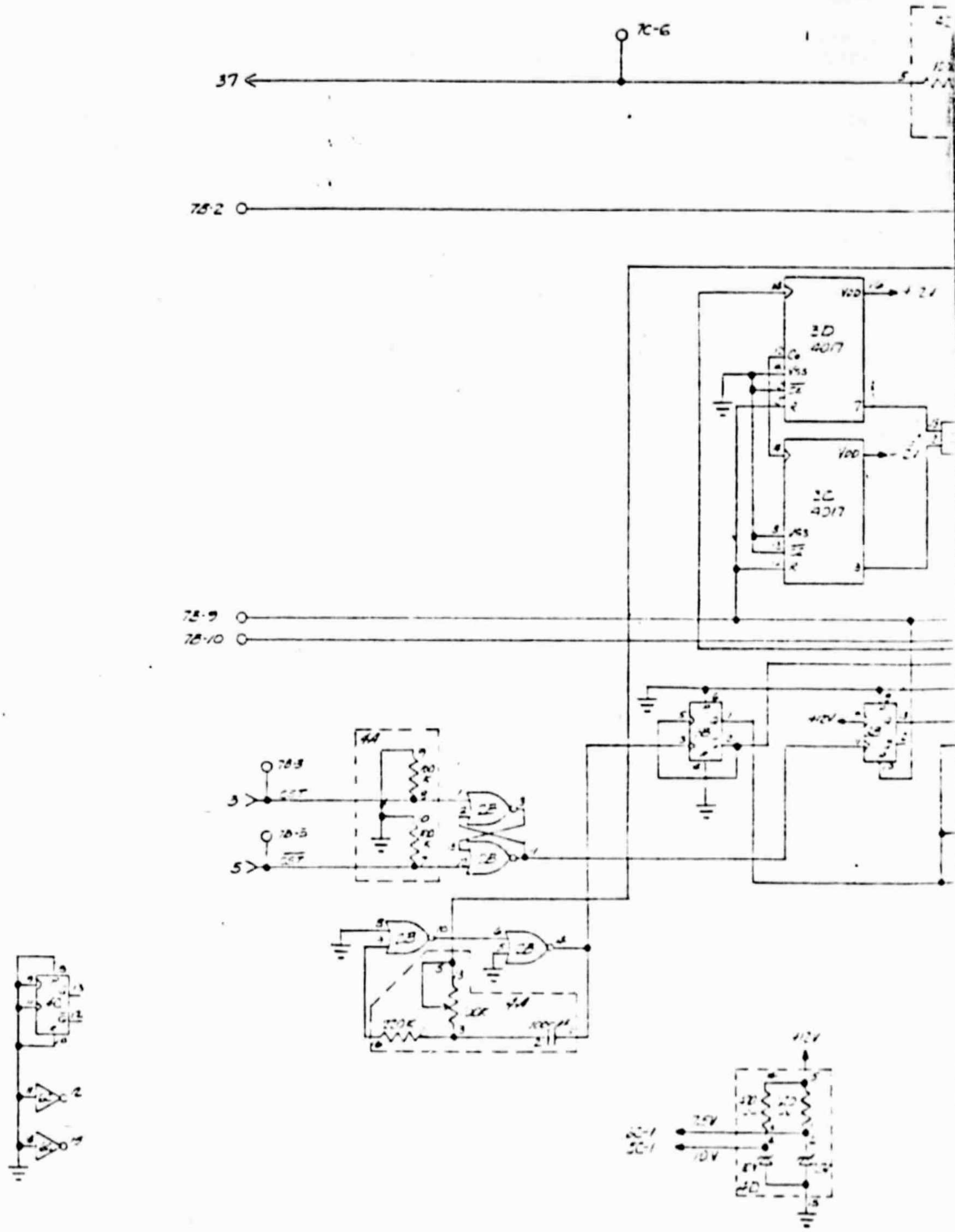
APR. BN 9/1/77 APR.

TITLE GSE CODE TRANSMITTER SIMULATOR

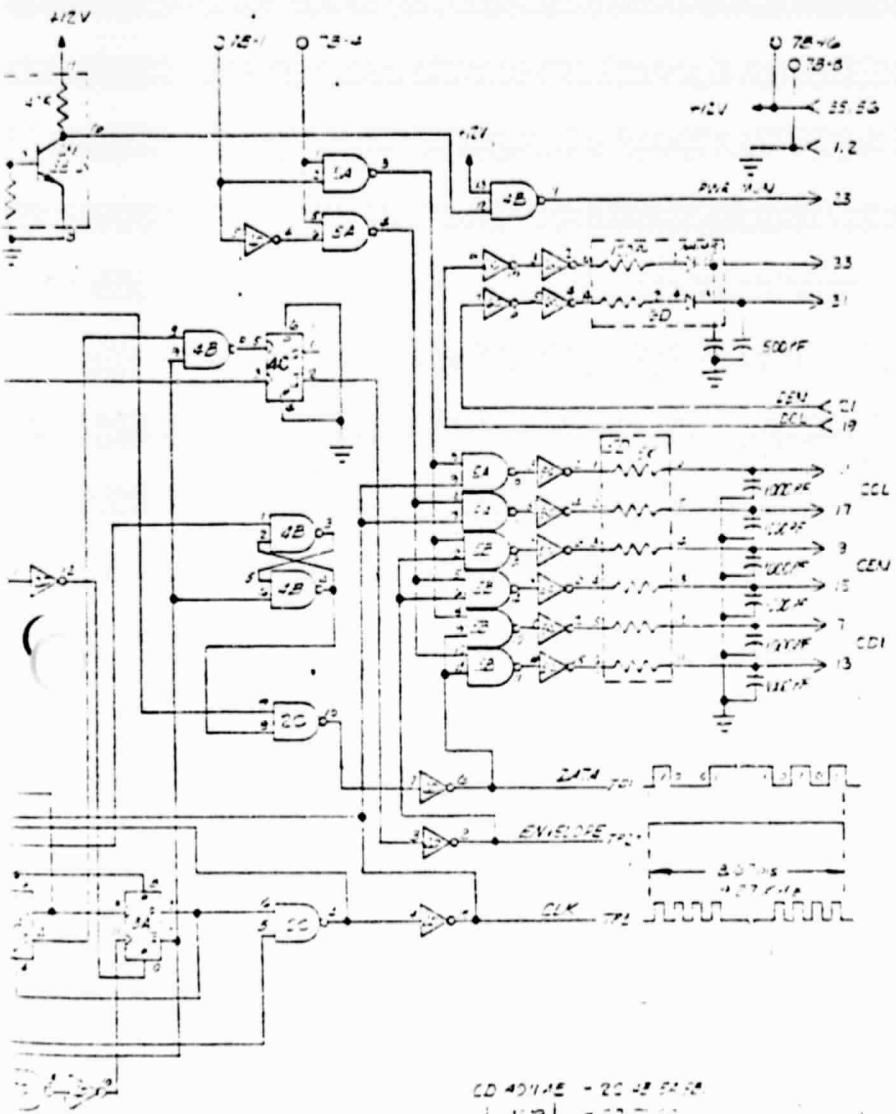
PARTS LIST NUMBER P/L 105953 REV A

SHEET 1 OF 1

DEVELCO, INC.



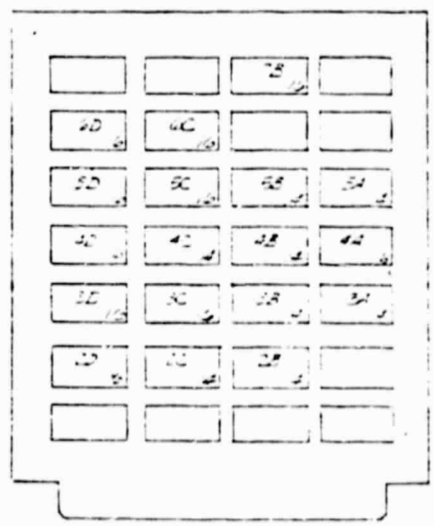
REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE
C						



CD 4011AE – 2C 4B 5A 5B
4049 – 2D [illegible]
4013 – 3A 3B 4C
4001 – 2B

NOTE 5C & 3C NOT HOOKED TO +12, ALL OTHER IC'S HOOKED TO +12 PER [illegible]

O INDICATES SOCKET FOR RIBBON CABLE



	100375-[illegible]	
USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

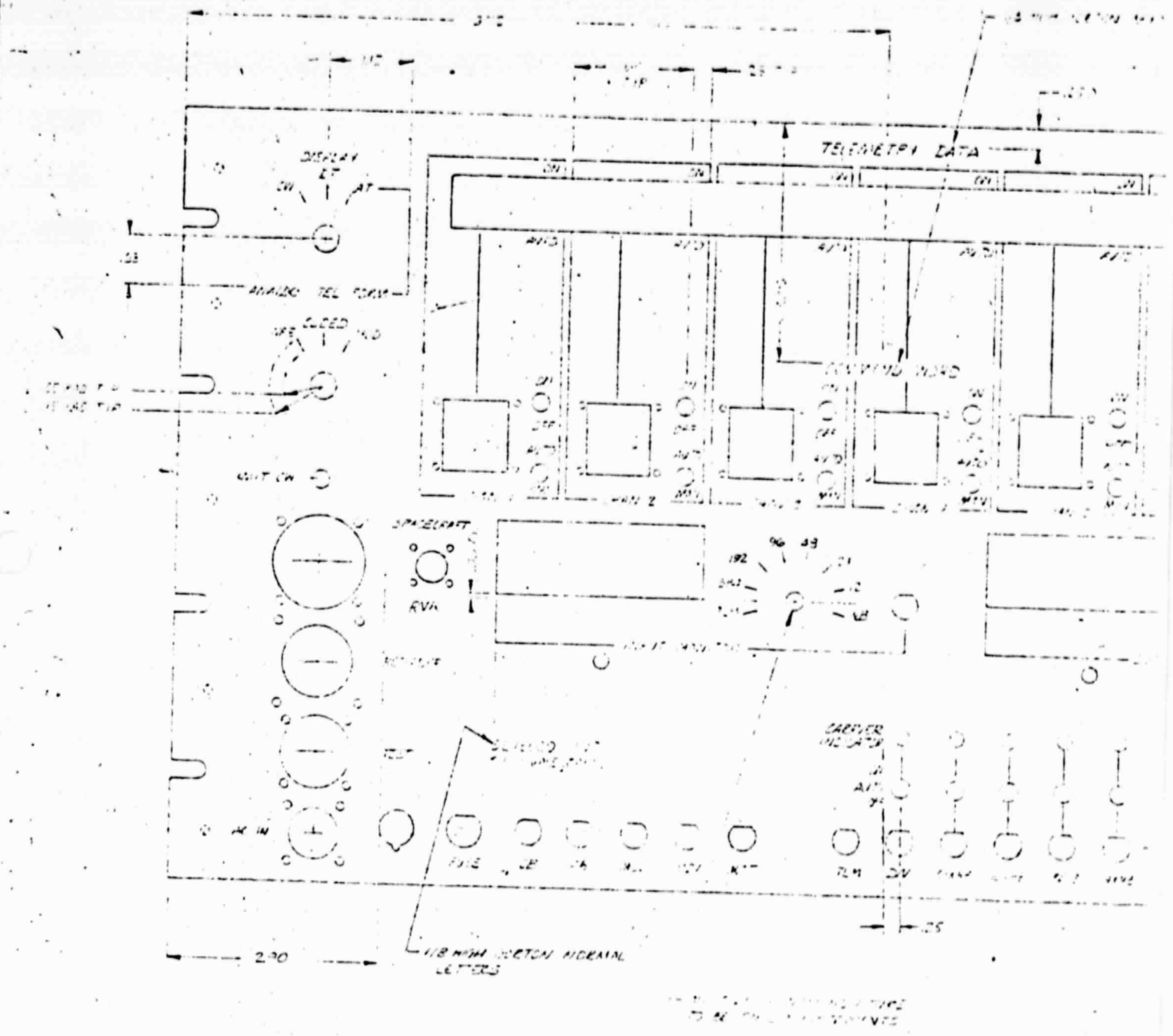
SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

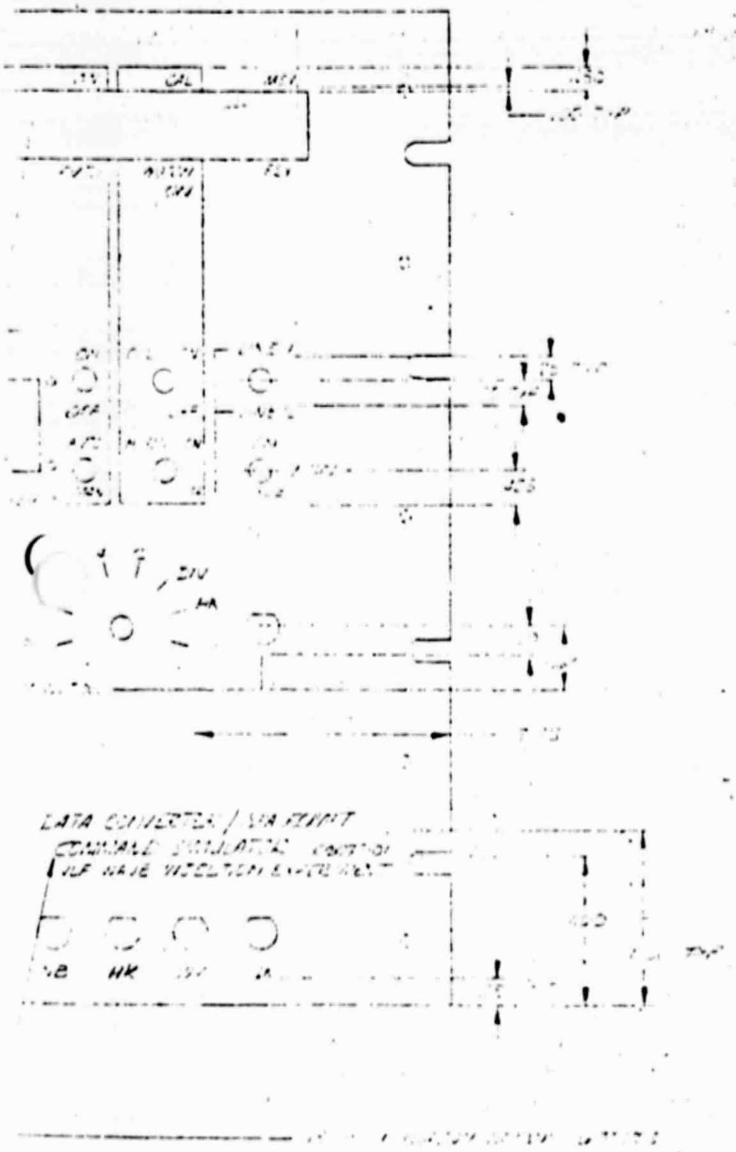
DEVELCO INC.

TITLE [illegible] CODE TRANSMITTER SIMULATOR

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	[illegible]55953	C

SCALE — DO NOT SCALE DRAWING SHEET OF


TELEMETRY DATA
DISPLAY
CW
AT
ANALOG TEL FORM
CLOSED
COMMAND WORD
SPACECRAFT
RVN
192
96
48
2.90
.25
1/8 HIGH LEROY NORMAL LETTERS



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APPROVED		
ENGINEER		
PROJ ENGR		

NEXT ASSY	USED ON
106075-01	

APPLICATION

DEVELCO INC.

TITLE
FRONT PANEL ENGRAVING
DATA CONVERTER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	30002	3-106073	C

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO 01	02
1	106075	DATA CONVERTER ASSY (LAYOUT)	C1		R	R
[illegible]	106073	FRONT PANEL	D3		1	—
3	106074	FRONT PANEL	D3		—	1
4	106076-01	SIDE SUPPORT	C3		1	1
5	106076-02	SIDE SUPPORT	C3		1	1
6	106077	COVERS TOP & BOTTOM	C3		2	2
7	106078	SUPPORT PWR SUPPLY	C3		1	1
8	106079	REAR COVER	C3		1	1
9	106080	CARD STOP	B3		1	1
10	106081	CARD STOP	B3		1	1
11	106114-2	ENGRAVING DWG - BOX	C3		1	—
12	106082-01	DISPLAY P.C. BD ASSY	PL		1	—
13		BOX ZERO SR409946	—		1	1
14		SUPPORT BAR SAE 4025	—		6	6
15		CONN. FOOT SAE 2422	—		30	30
16		CARD GUIDE SAE 1650	—		30	30
17		LOCKING TAB SAE 3000	—		90	90
18		P.C. CONN 22/44 .156 SPACE				
[illegible]		W.W. SAE SAW22/D3-2	—		11	11
20		P.C. CONN 28/54 .125 SPACE				
21		W.W. SAE CPH.3100-56	—		2	2
22	106083	METER BRACKET	B3		2	2
23		CONN, BENDIX PT02A18-32S		J1		
24		ALT # MS3112E18-32S	—		1	—
25		CONN, BENDIX PT02A(SR)18-32P		P1		
26		ALT # MS3116E(SR) 18-32P	—		1	—
27		CONN BENDIX PT02A14-19P		J3		
28		ALT # MS3112E14-19P	—		1	—
29		CONN BENDIX PT06A(SR)14-19S		P3		
30		ALT # MS3116E (SR) 14-19S	—		1	—
31		CONN BENDIX PT02A16-26S		J2		
32		ALT # MS3112E16-26S	—		1	1
33	106114-1	ENGRAVING DWG - BOX	C3		—	1

REVIS

A ITEM 72 PN WAS 105395

NEXT ASS'Y

USED ON

BY MSW 12-18-5 CK.

APR. 1/4/76 APR.

TITLE DATA CONVERTER STANFORD

PARTS LIST NUMBER

P/L 106075

REV A

SHEET 1 OF 3

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO. 01	02				
34		CONN BENDIX PT06A(SR)16-26 P		P2						
[illegible]		ALT # MS3116E (SR) 16-26 P	–		1	1				
36		CONN MS3102E10SL-3P	–	J4	1	1				
37		CONN MS3106E10SL-3S	–	P4	1	1				
38		KNOB ALCO KN5701BA-1/4	–		2	–				
39		PWR SUPPLY LAMBDA # LZS-30	–		1	1				
40		PWR SUPPLY LAMBDA # LZS-33	–		1	1				
41		PWR SUPPLY LAMBDA # LZD-22	–		1	1				
42		OVERVOLTAGE PROT. LAMBDA # L12-OV6	–		1	1				
43		" " " L12-OV-12	–		1	1				
44		" " " L12-OV-28	–		1	1				
45		KNOB ALCO KN5701BA-1/8	–		2	2				
46		METER MODUTEC T2-W3-DUA-1H1	–		2	2				
47		SWITCH ROT. CENTRLAB PS107	–		2	2				
48		PWR SWITCH DIALIGHT 513-1401-604	–		1	1				
49		LENS - DIALIGHT 186-5071								
50		MOD TO 105991	B3		1	1				
51		LAMP T-1 3/4, 5V DIALIGHT 7332	–		1	1				
[illegible]		FUSE HOLDER LITTLEFUSE # 342014	–		1	1				
53		FUSE, SLO BLO 1 AMP	–		1	1				
54		BNC CONN UG-1094A U	–		18	18				
55		SWITCH PUSH-BUTTON C/K 8221	–		1	–				
56		SWITCH TOGGLE C&K 7101	–		16	–				
57		SW. THUMBWHEEL CHERRY, T20-47A	–		6	–				
58		SW. ROT. CTS T205	–		2	–				
59	4-40 x 3/8	SCREW MACH PAN HD	–		25	25				
60	#4	WASHER LOCK	–		25	25				
61	#4	WASHER FLAT	–		25	25				
62	6-32 x 3/8	SCREW MACH PAN HD	–		36	36				
63	#6	WASHER LOCK	–		46	46				
64.	#6	WASHER FLAT	–		46	46				
65	4-40 x 5/32	SCREW, MACH. FLAT HD (BLK)	–		10	10				
66										

REV.

NEXT ASSY

USED ON

BY WM 12-13-5 CK. [illegible]

APR. APR.

TITLE DATA CONVERTER STANFORD

PARTS LIST NUMBER

P/L 106075 REV A

SHEET 2 OF 3

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO -01	-02				
67		BACKPLANE INTERCONNECT	D5		R	R				
68	105945	ANALOG BLOCK DIAGRAM	B7		R	R				
69		—PRINTED CIRCUIT BOARDS—								
70	106037	HEM DATA MONITOR DECODER &								
71		DISPLAY MULTIPLEXER	PL		–	1				
72	105953	GSE CODE TRANSMITTER SIMULATOR			1	–				
73	105896	HEM GSE TELEMETRY LOGIC &								
74		DECODING LOGIC	PL	BD 12	1	–				
75	105894	HEM GSE DISPLAY MUX & DIGITAL								
76		TELEMETRY COMMAND TIMING								
77		LOGIC	PL	BD 11	1	–				
78	105939	SUMMING AMPLIFIER	PL	BD 8	1	1				
79	105940	INPUT BUFFER & CH 6KHZ	PL	BD 1	1	1				
80	105941	DISCRIMINATOR	PL	BD 7	1	1				
81	105942 -01	DISCRIMINATOR	PL	BD 2	1	1				
82	-02		PL	3	1	1				
83	-03		PL	4	1	1				
84	-04		PL	5	1	1				
85	105942 -05	DISCRIMINATOR	PL	BD 6	1	1				
86	105943	METER AMP	PL	BD 10	1	1				
87	105944	DETECTOR & CLOCK GEN	PL	BD 9	1	1				
88										
89	106082-02	DISPLAY P.C. BD ASSY	PL		–	1				
90	105948	HEM GSE BACK PLANE	C6		R	–				
91	105958	HEM GSE BACK PLANE	C6		R					

RE

BY MKM	CK.
APR.	APR.
TITLE DATA CONVERTER STANFORD	
PARTS LIST NUMBER P/L 106075	REV A
SHEET 3 OF 3	

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO -1	-2				
1		SCHEMATIC & ASSY D6		R	R				
2	169P44-062	VECTOR BD 17.00X 4.5		1	1				
3									
4		IC LITRONIX DL10A	A4 A6 A8 A10						
5			A12 A14	6	6				
6		CD4049AE	B2	1	1				
7		SN7442AN	B3	1	1				
8		CD4050AE	B4, B9	2	2				
9		SN7445N	B8	1	1				
10		IC CD4021AE	B1A B2A B3A						
11			B4A B5A	5	–				
12									
13		SOCKET 14 PIN WIRE WRAP		10	10				
14		" 16 PIN " – "		25	17				
15									
16		TRANSISTOR 2N2907		8	8				
17		LED LITRONIX PL-2		16	16				
18		RESISTOR 1/4W 5% 1.5K		8	8				
19		120Ω		8	8				
20		1K		3	3				
21		470Ω		4	4				
22		RESISTOR 1/4W 5% 10K		18	–				
23									
24		DIODE 1N4005		1	1				
25	CK05BX105K	CAPACITOR CERAMIC .1		1	1				
26									
27		CABLE RIBBON ANSLEY 171-26	FA9, 11, 13	A/R	A/R				
28		CONN DIP 3M 3406	"	6	6				
29		STRAIN RELIEF 3M 3448-8	"	6	6				
30									
31									
32									
33									

REV

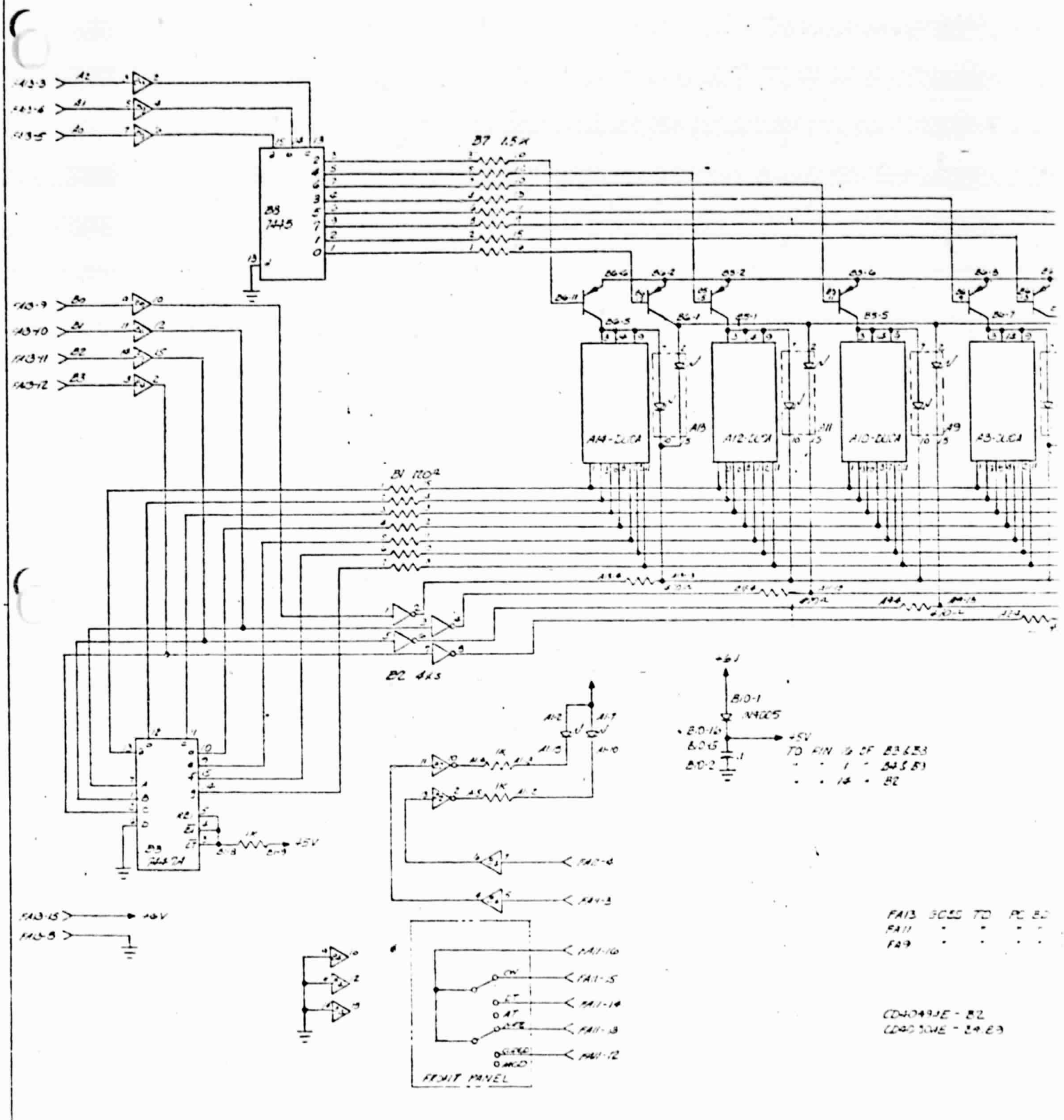
BY MCM CK.

APR. [illegible] 9/1/77 APR.

TITLE DISPLAY BOARD, MEM GSE F.P. INTERCONNECT

PARTS LIST NUMBER P/L 106082 REV –

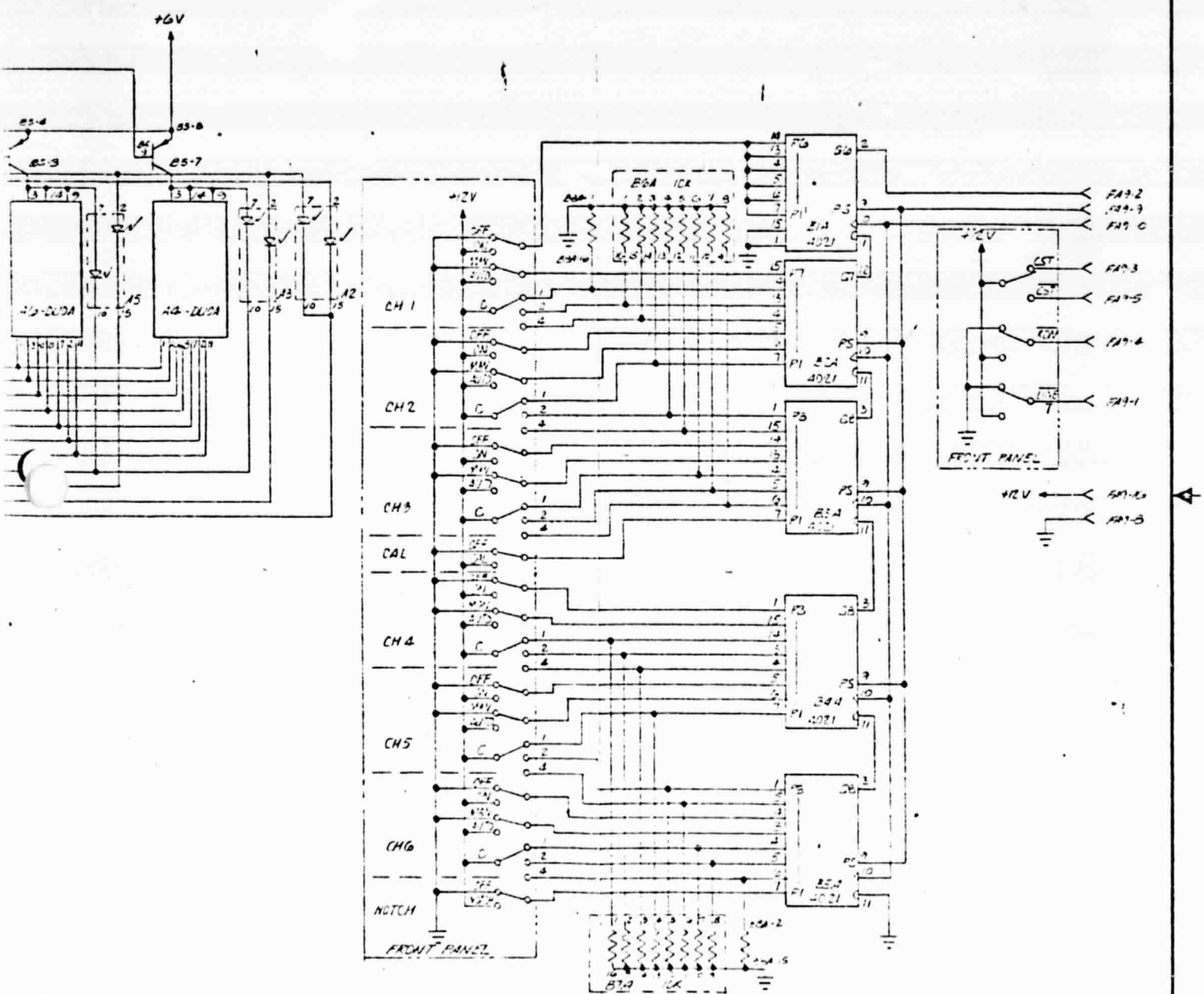
SHEET 1 OF 1



3. ALL TRANSISTORS ARE
2. ALL LEDS ARE
1. ALL CONNECTIONS TO
WIRED DIRECTLY FROM

SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE
E	5-03-76	REDRAWN				

(REVISIONS)



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APPLICATION		

DEVELCO INC.

TITLE: DISPLAY BOARD FOR NEW 3SE & FRONT PANEL INTERCONNECT

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	6-106082	E

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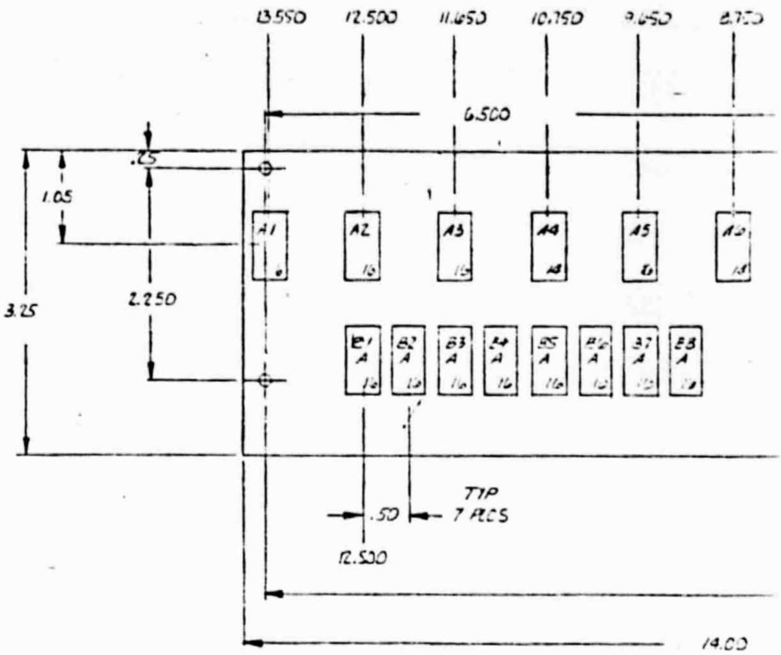
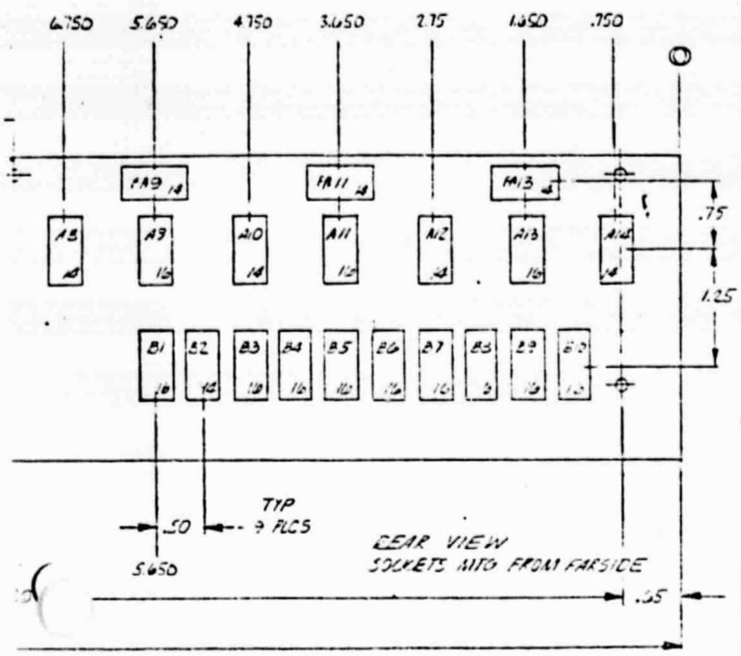


13.550
12.500
11.650
10.750
6.500
.25
1.05
3.25
2.250
A1
A2
A3
A4
A5
TYP
7 PCS
.50
12.500
14.00

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



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APPROVED		
ENGINEER		
PROJ ENGR		

USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

DEVELCO INC.

TITLE DISPLAY BOARD MTG HEW USE & FRONT PANEL INTERCONNECT

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	5-106082	F

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DEVELCO

Develco, Inc.
404 Tasman Dr., Sunnyvale, CA 94086
Phone (408) 734-5700 TWX 910-339-9295

Report No. 983-761209

DATA CONVERTER (106075-02) GROUND SUPPORT EQUIPMENT FOR THE HELLIWELL VLF WAVE EXPERIMENT SPACECRAFT RECEIVER

Prepared for:

Radioscience Laboratory
Stanford University
Stanford, CA 94305

Under:

Subcontract No. PR2006

December 1976

CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF DRAWINGS AND PARTS LISTS

1. INTRODUCTION

This report describes the Data Converter Ground Support Equipment (GSE) used to process received or taped telemetered data from the Helliwell VLF Receiver.

The data converter incorporates a complete set of discriminators to process 1-32 kHz data from the Helliwell VLF receiver. The housekeeping data will be decoded and displayed on the front panel (Figure 1). Table 1 describes the front panel controls and indicators.

The Data Converter is powered by 115 volts at 60 hertz with a third ground wire and three-prong power plug. It is housed in a rugged portable case with a removable cover for protection of the controls, indicators, and connectors.

The data converter is basically composed of two sections: a digital section which decodes the housekeeping data and displays this data on the front panel, and an analog section which discriminates the telemetered subcarrier frequencies from the Helliwell VLF receiver to the information band of 1-32 kHz and provides BNC outputs for use with a spectrum analyzer.

Three modular type power supplies are used for the GSE: one 6 volt, one 12 volt, and one 28 volt.

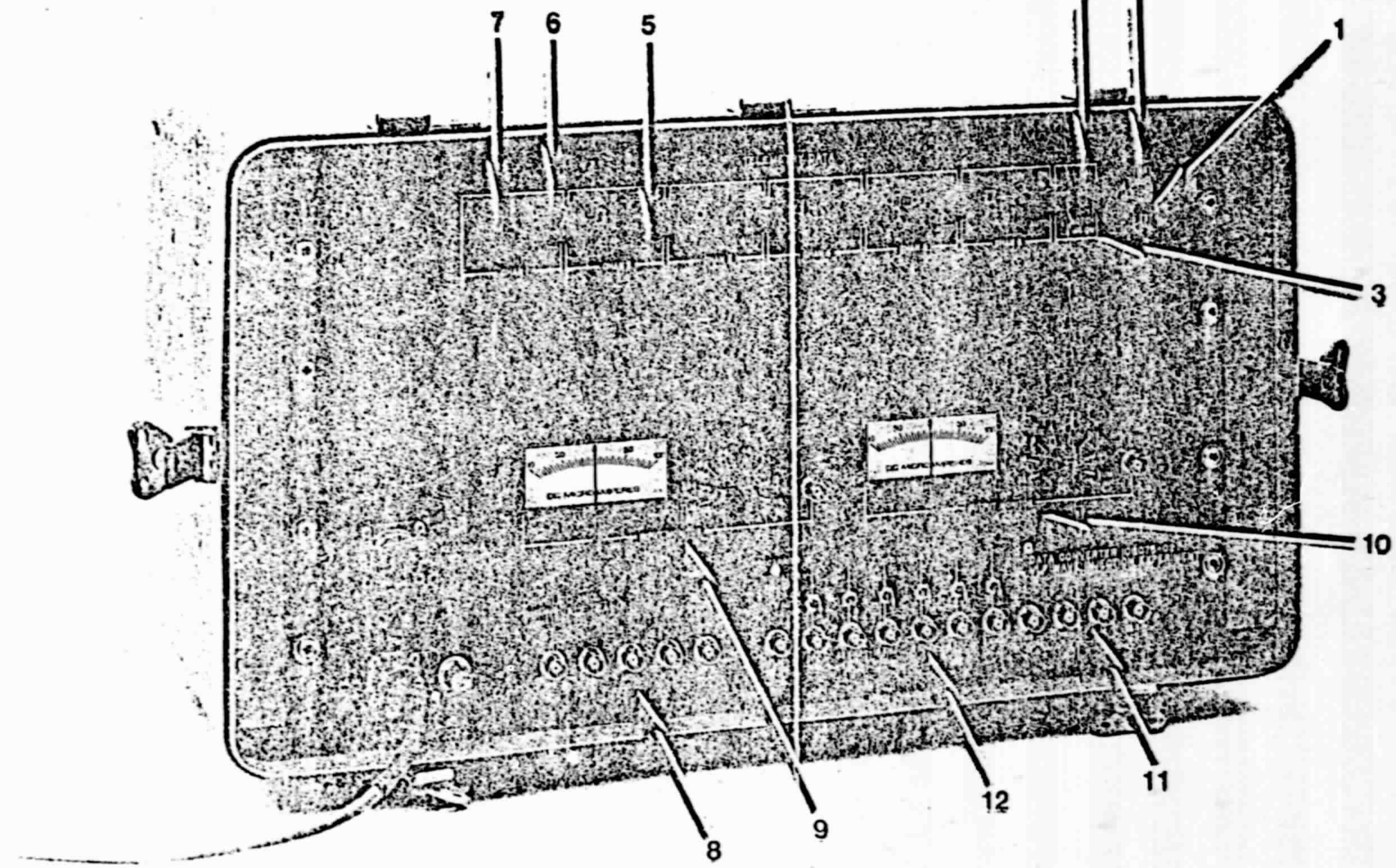

FIGURE 1

DATA CONVERTER

TABLE 1

FRONT PANEL CONTROLS
DATA CONVERTER

FIG 1 REF	DESIGNATION	DESCRIPTION
1	FSY (frame sync)	LED indicator. During monitoring of analog telemetry data it indicates frame sync after receiving a complete telemetry message successfully. Telemetry data is updated when the FSY turns on.
2	MSY (marker sync)	LED indicator. During monitoring of analog telemetry data it indicates the 8 MSY bits in each of 8 6-bit words.
3	NOTCH ON	LED indicator. The 44th bit in the telemetry message. When the LED is on the 20 kHz notch filter is on.
4	CAL	LED indicator. The 21st bit in the telemetry message. When the LED is on the experiment is in the Calibrate mode.
5	AUTO GAIN	LED indicator, one for each of six channels. Illuminated LED indicates that channel is in the automatic gain mode.
6	ON	LED indicators, one for each of six channels. Illuminated LED indicates that output is summed into the Analog Telemetry link.
7	TELEMETRY WORD (gain setting display)	Single-digit display, one for each of six channels. Indicates the amplifier gain setting is dB x 10 in a range of 0-7 x 10 dB.
8	DIGITAL SIGNAL MONITOR	BNC test points for troubleshooting. The signals are only time and "1" and "0" level relative and are not absolute level relative signals.
	OB	Monitors the "1" coded bit from the demodulated signal
	ZB	Monitors the "0" coded bit
	MCL	Monitors the clock derived from the data lines

FIGURE 1

(CONTINUED)

FIG 1 REF	DESIGNATION	DESCRIPTION
	MDI	Monitors the serial decoded analog telemetry data
	MPT	Monitors the FSY
9	INPUT MONITOR	8-position switch selects any one or all input subcarriers for the scaled peak detector meter. BNC is connected in parallel for external monitor.
	TLM	Monitors the sum of all subcarriers
	384	Monitors the subcarrier with f_o = 384 kHz
	192	Monitors the subcarrier with f_o = 192 kHz
	96	Monitors the subcarrier with f_o = 96 kHz
	48	Monitors the subcarrier with f_o = 48 kHz
	24	Monitors the subcarrier with f_o = 24 kHz
	12	Monitors the subcarrier with f_o = 12 kHz (Housekeeping)
	6	Monitors the 6 kHz narrowband incoming signal
10	OUTPUT MONITOR	8-position switch selects any one or all output signals for the scaled peak detector meter. BNC is connected in parallel for external monitor or measurement.
	32	Monitors the 16-32 kHz signal channel
	16	Monitors the 8-16 kHz signal channel
	8	Monitors the 4-8 kHz signal channel
	4	Monitors the 2-4 kHz signal channel
	2	Monitors the 1-2 kHz signal channel
	DIV	Monitors the divided HK subcarrier signal
	HK	Monitors the trilevel housekeeping data
	SUM	Monitors the summed signals

TABLE 1

(CONTINUED)

FIG 1 REF	DESIGNATION	DESCRIPTION
11	ANALOG BNC MONITOR	BNC test points for troubleshooting
	TLM	The incoming subcarriers at the buffer output
	HK	Trilevel housekeeping data
	SUM	The output signal of the summing amplifier
	CLK	96 kHz
12	CARRIER INFORMATION	
	Carrier Indicators	Indicates which carrier frequencies have been detected
	Carrier Switches	3-position switch
	ON	Channel is turned on
	AUTO	Channel is turned on if carrier is detected
	OFF	Channel is turned off
	Carrier Monitors	Monitors same information as described in Reference 10

2. ANALOG SECTION

A block diagram of the data converter is shown in Drawing 7-105945. The incoming signal is transformer coupled to the buffer amplifier. The buffer amplifier has a gain of 14 dB, giving an overall gain of 7 dB referred to the input of the isolation transformer. The output of the buffer amplifier drives an array of six frequency discriminators, and a 6-kHz narrowband 2-pole filter.

Each discriminator board contains an input bandpass filter, a buffer stage immediately following the bandpass filter for subcarrier monitoring, a phase-locked-loop discriminator, a lowpass filter and a highpass filter. The highpass filter for the HK discriminator is deleted, since it has little effect in the performance in the circuit. A phase-locked-loop type discriminator is used because it is compatible to the VCO type used in the Helliwell receiver; hence, linearity improves. In addition, this type of discriminator provides carrier phase detection.

An array of seven analog switches is used to connect the outputs of the analog discriminators, the divided HK subcarrier, and the 6-kHz narrowband input to the current summing output amplifier. The analog switch used for the 6-kHz narrowband input is always on; the other switches are gated by their respective channel carrier detectors. Provision to override the carrier detect gate is also incorporated.

The discriminated tristate data from the HK discriminator is fed to Detector Board 105944 along with the HK subcarrier. The tristate data is converted to 2-line code with CMOS logic level for the HK decoder. The HK subcarrier is divided down 20 times and then fed to the summing amplifier; the HK subcarrier synthesizes the 96-kHz VCO so that the frequency of the master oscillator inside the HEM receiver can be monitored.

Two meter circuits are included in the HEM GSE to provide a fast functional check of the HEM receiver.

One meter circuit is a peak-detection type and it is used to monitor the telemetry and subcarrier signal. The other meter circuit is a true-RMS type and it monitors the discriminated signals and the summing output.

Functions 19 to 22 of Table 1 (front panel controls and indicators) describe the operation and testing capabilities of the analog section.

3. DIGITAL SECTION

The purpose of the digital section is to decode housekeeping data from the analog telemetry word and display this information on the front panel (refer to Table 3).

A list of abbreviations used in the GSE digital circuitry is contained in Table 2.

The detected HK data is in the form of a 2-line tristate code. It is decoded to NRZ data and stored in 32-bit shift register by the self-generating clock. Marker and frame synchronization is also timed by the 64 kHz onboad oscillator. If the marker and frame synchronization times out properly at the end of each data frame, the stored data will be written into a 4 x 8 memory, and then multiplexed and read to the display board.

TABLE 2

GLOSSARY

FOB	Frequency demodulated - One bit
FSY	Frame sync
FZB	Frequency demodulated - Zero bit
MCL	Monitor data clock
MDI	Monitor data in
MPT	Monitor data parallel transfer
MSY	Marker sync

TABLE 3

ANALOG TELEMETRY WORD FORMAT

WORD NO.	BIT NO.	FUNCTION
1	1	CH 1 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
2	1	CH 2 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
3	1	CH 3 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
4	1	Calibrate
	2	No function
	3	No function 0's
	4	No function
	5	No function
	6	No code
5	1	CH 4 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
6	1	CH 5 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code

TABLE 3

(Continued)

WORD NO.	BIT NO.	FUNCTION
7	1	CH 6 ON/OFF
	2	AUTO/MAN
	3	10 dB
	4	20 dB
	5	40 dB
	6	No code
8	1	Notch Filter ON/OFF
	2	No function
	3	No function
	4	No function
	5	No function
	6	No code (remains until next transmission)

4. ANALOG CIRCUIT DESCRIPTION

The following describes the analog circuits in the GSE. Refer to Drawing 105945 for a complete block diagram of all the analog circuits. Drawing 105958 is the backplane interconnect wiring for all the boards and the front panel connectors.

4.1 INPUT BUFFER - Drawing 6-105940 (Board 1)

Transformer T1 couples the incoming TLM signal to Amplifier U1. Amplifier U1 has a gain of 14 dB, giving an overall gain of 7 dB including the 7-dB loss of the transformer. The maximum input level without suffering severe distortions is 7 volts peak to peak. The output is ac coupled to the discriminators through Pin 2, named BFR, and dc coupled to the 6-kHz filter. Two resistors attenuate the BFR signal which is then fed to Pin 1 for monitoring purposes.

The 6-kHz filter has a bandwidth of 1 kHz, and an insertion loss of 6 dB; it is buffered by device U2 and then brought out to three places - TP8, RD8 and NB out. 100-ohm isolation resistors are used at the output of U2.

The remaining circuitry on Board 1 includes U3 and Q1. The function of this circuitry is to generate two reference voltages. One of the voltages is 6 volts and named Sig Com, while the other one is 6-7 volts and named V_j.

4.2 DISCRIMINATOR - Drawing 6-105942 (Boards 2-6)

Board 2 to Board 6 are the discriminator boards, and they share a common schematic since their circuitry configuration is identical. The main difference among the discriminator boards is their center frequencies which are spaced an octave apart starting at 24 kHz.

Each discriminator board has a three-pole, 1-dB ripple, Tchebychev bandpass input. This filter has a bandwidth of one-fourth of its center frequency and an insertion loss of 6 dB. Transistor 2N2484 buffers the filter for monitoring purposes at Pin 4. The buffered output from the 2N2484 is also capacitor coupled to limiter 1A. 1A is a CA3080 having a gain of 40 dB. A small hysteresis is also included for 1A.

2A is a CD4046 CMOS phase lock loop device. This device has two phase comparators and one voltage controlled oscillator. Capacitor C_0 and the combination resistance of R1 and R2 set up the free running frequency of the VCO. The output of the VCO is tied to one input of phase comparator No. 1, while the remaining input receives the incoming signal from the Limiter 1A. The output voltage of phase comparator 1 is integrated by D10 then fed back to the VCO. With this closed-loop configuration, comparator 1 will force the VCO to phase track the incoming signal, giving a conversion gain of 6 V/fc. Further description of this PLL can be found in RCA Application Note No. ICAN-6101.

Phase Comparator 2 is used for carrier detection. When the VCO is phase locked to the incoming signal, the output of phase comparator 2 will be a 75% duty cycle pulse; if not, its output will have an average duty cycle of 50%. Voltage comparator 3A, CA3080, detects the average output voltage of phase comparator 2. The output of 3A will become true, whenever the duty cycle of phase comparator 2 output exceedes 65%. The output of 3A is isolated by two 30 K resistors and brought out at Pin 12 and 13 to drive a front panel mounted LED and the analog switch for the summing amplifier on Board 8.

Post filtering for the PLL discriminator is performed by op-amps 4A and 5A (CA3094). 4A is configured as a 3-pole, 1-dB ripple, Tchebychev low pass filter, while 5A is configured as a 2-pole, 1-dB ripple, Tchebychev high pass. The drive capacity of the CA3094 is high enough to drive a 50-ohm load with 10 dB loss. The output of 5A is brought to Pins 16, 17, and 18 through 100-ohm resistors for the summing amplifier and the monitor circuitry.

4.3 HK DISCRIMINATOR - Drawing 6-105941 (Board 7)

The housekeeping discriminator is very similar to the other five discriminators with the following differences: the center frequency of the HK discriminator is 12 kHz; the bandwidth of the input 3-pole filter is 4 kHz, that is, one-third of center frequency.

The low pass filter is a 3-pole Bessel filter with the cut-off frequency at 40 Hz. The high pass filter is not used in the HK discriminator because dc information is required by the following detector board (6-105944, Board 9).

4.4 SUMMING AMPLIFIER - Drawing 6-105939 (Board 8)

U3, a CA3100, is the current summing amplifier. Current summing was chosen instead of voltage summing because current summing provides a better approximation of the received signal.

The supply voltage of U3 is 28 volts and 0 V to provide higher output level for the current summing. The 12-volt supply establishes the bias voltage for U3.

U1 and U2 are CD4066 analog gates. With the exception of the gate that is used for the 6-kHz NB channel, all gate controls are pulled down to V_{ss} with a 1 megohm resistor; that is, all channels are normally off except for the NB channel which is always on.

4.5 DETECTOR - Drawing 6-105944 (Board 9)

The detector circuitry receives the discriminated HK signal through Pin 14. U1 is the positive peak buffer amplifier while U2 is the negative peak buffer amplifier for the incoming HK signal. Two 51 K resistors and one 100 K resistor establish the reference voltage for U3 and U4, upper and lower threshold voltage comparators. The output of U3 will become true if the incoming signal voltage is greater than 75% of its maximum-to-minimum value, while U4 will become true when the signal is less than 25%. Two sections of U6, CD4066, are used to reduce the leakage current of the detector diodes (1N270) by feeding back the compared outputs as the gating signals. U14 (CD4030) buffers the compared outputs, and two 6.8 K isolation resistors connect them to Pins 12 and 13.

For summing purposes, the 12-kHz HK subcarrier is divided down to 600 Hz so that it will not interfere with the data signal. One CD4029, U7, and half a CD4013, U8, is used as the divider chain. The divided signal is filtered by a 3-pole Tchebychev, 1-dB ripple, low pass filter after a 31-dB attenuator pad. This low pass filter, having a cut-off frequency of 750 Hz, is implemented by a CA3094, U5, and its output is brought to Pins 16, 17 and 18 through 100 ohm isolation resistors. The harmonic level is at least 40 dB down referred to the data channels.

The generated 600 Hz is also used to clock the 213 ms digital one shot, implemented by U10, U11, and one-half of U8, while another section of U14 resets it on either a "ONE" or "ZERO" code. This one shot has a delay of 138 clock periods; and, since it is reset by either a "ONE" or "ZERO" code, it can fire only once during the frame sync (FSY - refer to Table 1 for FSY definition). The output of this digital one shot controls the analog switch, U6, which gates the servo loop of the 96-kHz synthesized clock.

The 96-kHz synthesized clock is built by U9, and U12. U12 is configured as a divide-by-eight counter. U9 contains a phase comparator and a voltage controlled oscillator. A 50 kΩ variable resistor finely adjusts the center frequency of the VCO. The phase comparator produces an error voltage proportional to the phase difference between the 12-kHz HK subcarrier and the divided 96 kHz. During the frame sync of each data cycle, the VCO is allowed to phase lock to the HK subcarrier which is locked to the master oscillator in the HEM receiver.

4.6 METER AMPLIFIER - 6-105943 (Board 10)

The meter amplifier board contains two meter circuits; one monitors the subcarriers and the other one monitors the discriminated signals. Both the input monitor and the output monitor meters are panel mounted and zero centered.

The input monitor switch selects any one subcarrier signal or the TLM signal and feeds it to the buffer transistor 2N2484 via Pin 4. External monitoring is made possible by bringing back the buffered signal to a front panel mounted BNC through Pin 6.

Op-amp U1 is a CA3080, and it is configured as a positive peak detector with the introduction of another 2N2484. The peak value is brought to the scaling resistors gauged with the front panel input selector switch through Pin 7 and back on Pin 8. Pin 8 is tied to the current summing point of a log converter, implemented by U2 and U3.

U2 is a LM4250 op-amp, and U3 is a CA3096 NPN, PNP transistor array package. The matching characteristic of CA3096 provides temperature compensated operations. Potentiometer R2 is the 0 dB reference adjustment, while R1 is the conversion factor adjustment. Pins 9 and 10 are used for meter drive. The circuit element values have been chosen so that the conversion factor for 0 dB is equal to 100 μA.

The log converter in the output monitor meter circuitry is identical to the one in the input monitor; hence, they have the same conversion factor. However, a true-RMS circuitry is used instead of a peak detector in the output monitor. The RMS function is performed by an Analog Devices Model 440 module. U4 is used to buffer the front-panel-selected signal. A 100-ohm resistor connects the buffered signal to the monitor BNC via Pin 16. The scaling element is an onboard 10 KΩ 1% resistor; hence Pin 17 is jumpered to Pin 18 on the back plane.

5. DIGITAL CIRCUIT DESCRIPTION

The following describes the digital circuits in the GSE.

5.1 DISPLAY BOARD FOR HEM GSE - Drawing 106082

The display board (Figure 2) contains six numerical displays to read out gain setting for each PGA located in the HEM receiver and sixteen LED to indicate (a) the mode (AUTO/MAN) and ON/OFF for each channel, (b) the status of the notch filter and calibration pulse, and (c) the detection of the marker sync and frame sync.

The power switches for the LED displays are constructed with eight 2N2907 transistors buffering a SN7445 (B8) BCD to decimal decoder. The "D" input of B8 is grounded since only eight switches are required. The purpose of the power switches is to demultiplex the 4-bit data bus by decoding the address lines to apply power to the proper display group one at a time. The method of displaying data has the advantages of reduced hardware and power consumption.

Three lines of the data bus is fed to a SN7447A (B3) BCD to seven segment decoder. Since the largest number to be displayed is only seven, the used "D" input of B3 is grounded. The outputs of B3 are bussed to the inputs of the DL-10 (A4, 6, 8, 10, 12, 14) numerical displays.

Four of the inverters of B2, SN7406, are used by the 4-bit serial data bus (B0-B3) to drive their corresponding LEDs. The remaining two of the inverters (of B2) are used exclusively for marker sync and frame sync.

Interface to the decoder boards which has CMOS logic level instead of TTL level is implemented with two CD4050, B4 and B9. Five volts used to power TTL devices is derived by inserting a IN4005 diode to the six-volt power line.

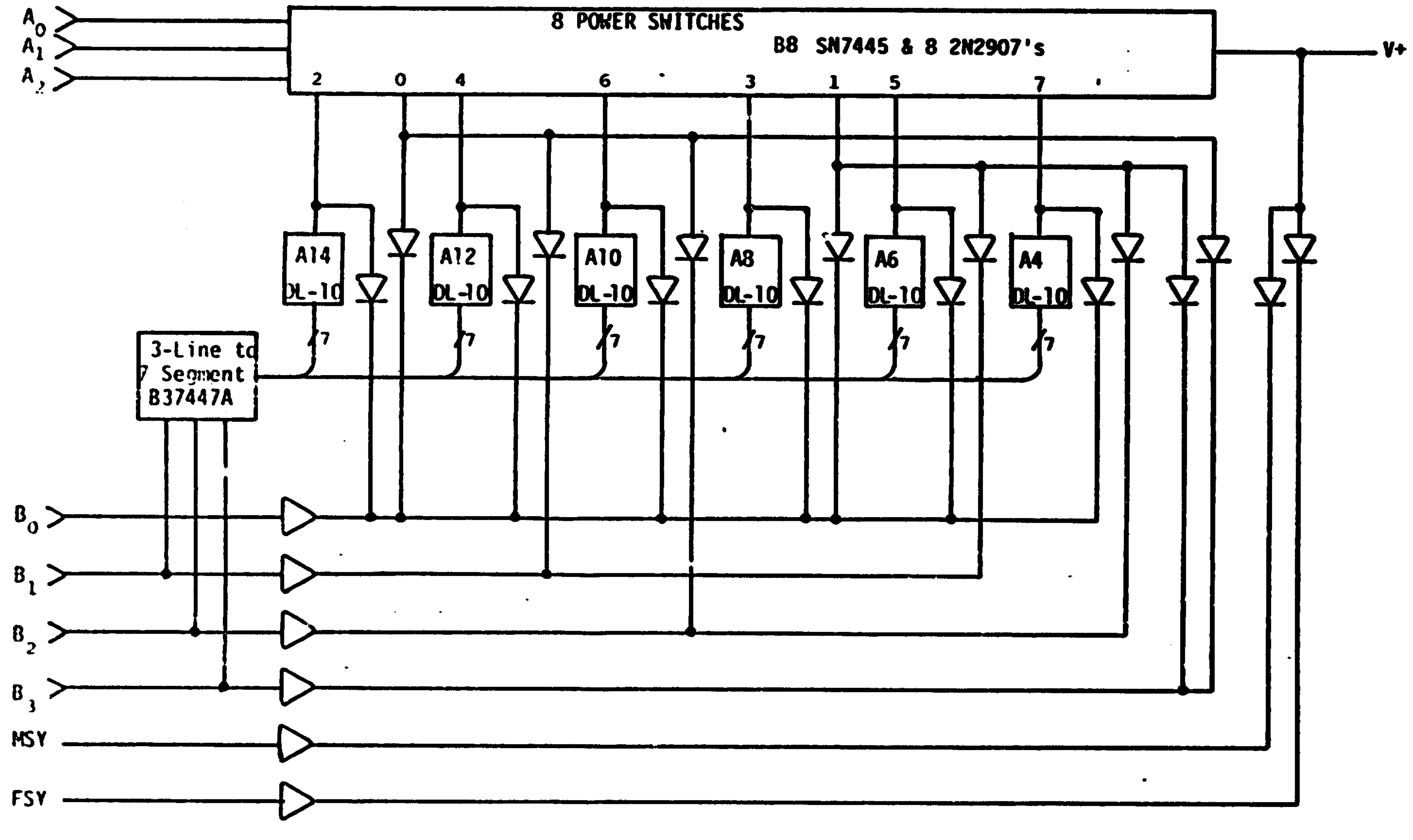

FIGURE 2

DISPLAY BOARD

5.2 HEM DATA MONITOR DECODER AND DISPLAY MULTIPLEXER - Drawing 6-106037

Figure 3 is the block diagram for the HK data decoder. The incoming HK data from the discriminator is in the form of 2 line tristate code, and it comes in on Pin 12 and Pin 13. Each line represents a Logic "1" or Logic "0". If the ONE line is high, the bit is a Logic "1". Logic "0" is represented when the ZERO line goes high, while neutral state is represented by having both lines at low level. Each bit, whether "1" or "0", will go high only on the first half of the bit time and then return to the neutral state. This way the code is self-clocking.

NRZ data is recovered by setting and resetting flip-flop E5 (CD4013) with the FOB and FZB lines, respectively; while clock is recovered by "ORing" the two lines with NOR Gate F5.

An onboard 64-kHz oscillator is implemented by half a CD4011, D1. Device B3 divides down the frequency to 1 kHz, 500 Hz, and 250 Hz, which are also the address lines labeled A0, A1, and A2, respectively. The frequency can be fine adjusted by the 20 kΩ variable resistor.

Device E4 and F4 (both CD4017) are configured as the synchronization timer. This timer is driven by the 250-Hz line from the local oscillator and reset by the derived data clock. Further discussion of the synchronization timer follows.

The bit counter is constructed also with a CD4017, E2 and F2. F2 is configured as a modulo six counter by using the reset line to simplify the marker sync hardware. The marker sync flip-flop, E3-3 and F3-9, is set by F3-6 and reset by E1-4 or the monitor clock. F3-6 decodes 84 ms from the sync timer and the fifth count from F2. That is, the marker sync flip-flop fires 84 ms after the negative-going edge of the fifth bit which is the center of the sixth bit or marker bit. If the timing of the incoming clock is improper, the Marker sync flip-flop will not be latched (set).

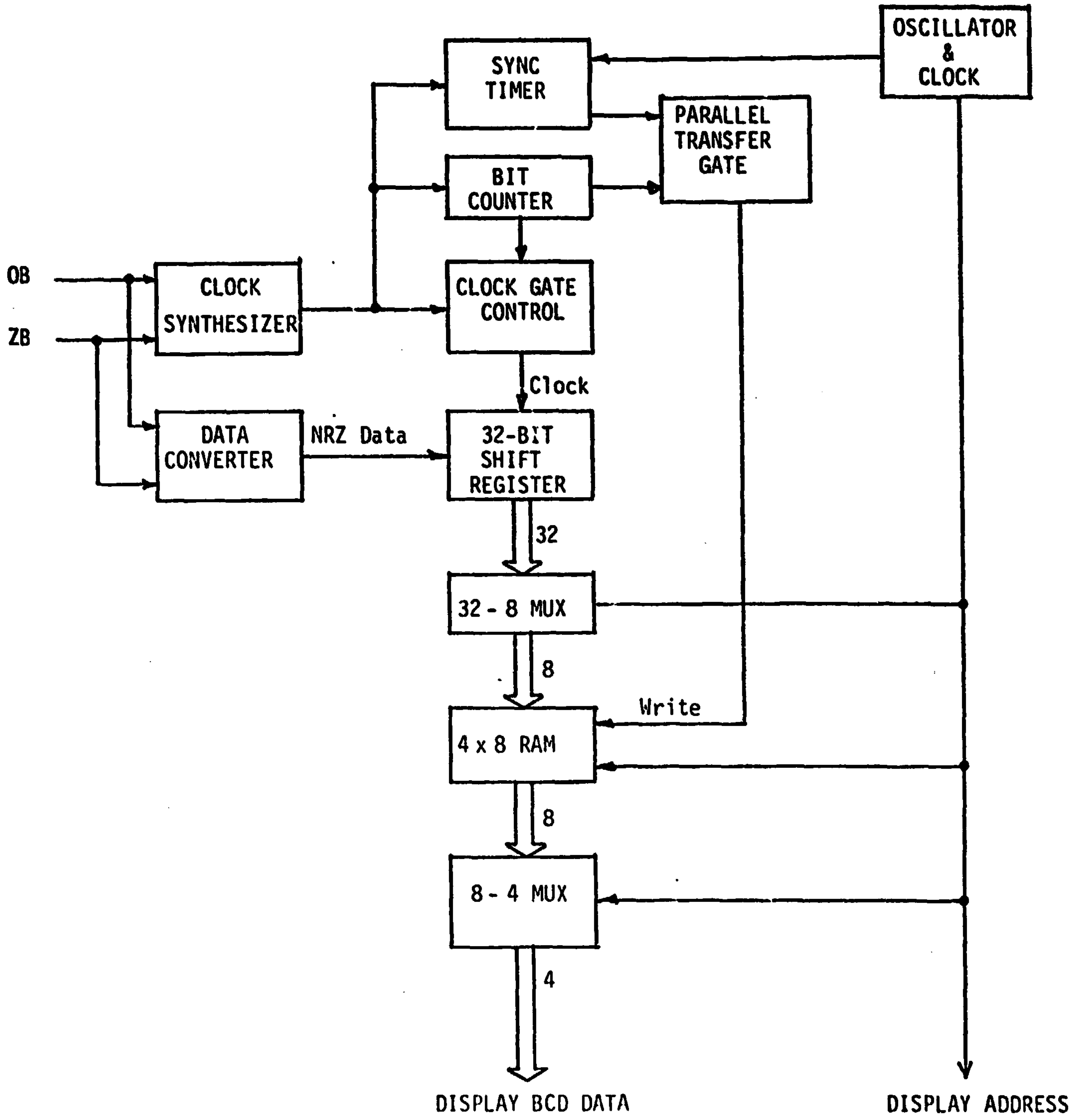

FIGURE 3

DECODER LOGIC

E2 can be called the Marker counter, since it is clocked essentially by recognition of the Marker Sync. This counter is reset by the sync timer on 360 ms; in the same time, the sync timer is hung up and the marker sync flip-flop is jammed. If the incoming HK data is detected correctly, the sync timer can count up to 360 ms only during the frame sync time slot.

F1 (CD4013 flip-flop) and associated gates implement the parallel transfer gate. F1-13 is clocked at the same time when the Marker Counter E-2 is reset. If exactly eight markers have elapsed prior to this time, Gate D1-3 will allow F1-13 to be clocked true which is the recognition of the frame sync. F1-13 is ripple reset by the next data clock through E4.

The function of F1-2 is to blank out the data clock for the 32-bit shift register, during Words 4 and 8, since these bits have no significance. This function is accomplished by decoding Words 4 and 8 with E3-10 and E3-11, respectively.

The 32-bit shift register is implemented with four CD4015, D2 to D5. HK data (Table 4) is shifted in by the self-generated data clock from the blanking gate F3-10. At the end of each frame, a four-wide, eight-bit multiplexer, four CD4052, is used to organize the shifted serial data to a 4 x 8 format (Table 5), then written into a CD4036 4 x 8 RAM. Address Lines A1 and A2 conduct the data traffic.

The write command is initiated by the Frame Sync flip-flop F1, and synchronized to the address lines by clocking in the frame sync signal into C1-1 at the beginning of the display cycle decoded by F5-11. F5-11 also terminates the write command at the follow display cycle by clocking the disarm flip-flop C1-13. C1-13 is self-reset.

Devices A2 and B2 are CD4053. Their function is to convert the 8-line data buss of the CD4036 into 4 lines serial data buss (Table 6) for the display board. The serial data is brought out on Pin C0-9 (B0), 10 (B1), 11 (B2), and 12 (B3) with Pin C0-12 (B3) being the most significant line.

TABLE 4

HOUSEKEEPING DATA

BIT	FUNCTION		DEVICE LOCATION
1	CH 1	ON/OFF	D2- 2
2		AUTO/MAN	11
3		10 dB	12
4		20 dB	13
5		40 dB	10
6	CH 2	ON/OFF	3
7		AUTO/MAN	4
8		10 dB	5
9		20 dB	D3- 2
10		40 dB	11
11	CH 3	ON/OFF	12
12		AUTO/MAN	13
13		10 dB	10
14		20 dB	3
15		40 dB	4
16	CAL		5
17	CH 4	ON/OFF	D4- 2
18		AUTO/MAN	11
19		10 dB	12
20		20 dB	13
21		40 dB	10
22	CH 5	ON/OFF	3
23		AUTO/MAN	4
24		10 dB	5
25		20 dB	D5- 2
26		40 dB	11
27	CH 6	ON/OFF	12
28		AUTO/MAN	13
29		10 dB	10
30		20 dB	3
31		40 dB	4
32	NOTCH ON/OFF		5

TABLE 5

4-WORD BY 8-BIT DATA FORMAT
(CD4036-A1)

ADDRESS	00	01	10	11	
	WORD 1	WORD 2	WORD 3	WORD 4	
	CH 1 ON/OFF	CH 1 AUTO/MAN	CH 2 AUTO/MAN	CH 3 AUTO/MAN	D1
	CH 2 ON/OFF	10 dB	10 dB	10 dB	D2
	CH 3 ON/OFF	20 dB	20 dB	20 dB	D3
	CAL	40 dB	40 dB	40 dB	D4
	CH 4 ON/OFF	CH 4 AUTO/MAN	CH 5 AUTO/MAN	CH 6 AUTO/MAN	D5
	CH 5 ON/OFF	10 dB	10 dB	10 dB	D6
	CH 6 ON/OFF	20 dB	20 dB	20 dB	D7
	NOTCH ON/OFF	40 dB	40 dB	40 dB	D8

TABLE 6

4-BIT SERIAL DATA (8-WORD BY 4-BIT)

	WORD 1	WORD 2	WORD 3	WORD 4	WORD 5	WORD 6	WORD 7	WORD 8
B0	CH 1 ON/OFF	CH 4 ON/OFF	CH 1 AUTO/MAN	CH 4 AUTO/MAN	CH 2 AUTO/MAN	CH 5 AUTO/MAN	CH 3 AUTO/MAN	CH 5 AUTO/MAN
B1	CH 2 ON/OFF	CH 5 ON/OFF	10 dB	10 dB	10 dB	10 dB	10 dB	10 dB
B2	CH 3 ON/OFF	CH 6 ON/OFF	20 dB	20 dB	20 dB	20 dB	20 dB	20 dB
B3	CAL	NOTCH ON/OFF	40 dB	40 dB	40 dB	40 dB	40 dB	40 dB

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO					
1	105939	SCHEMATIC & ASSY	BG	-	R					
2		PC BOARD 12DE3GP			1					
4		IC CA3100T			1					
5		" CD4066AE			2					
6		RESISTOR 1/4W 5% 470			1					
7		RESISTOR 1/4W 5% 100			2					
8		" " " 20K			10					
9		RESISTOR 1/4W 5% 10K			1					
10		" " " 1M			8					
11		CAPACITOR D. TANT 6.8 35V			1					
12		" MICA 33P			1					
		" CK05 .1			3					

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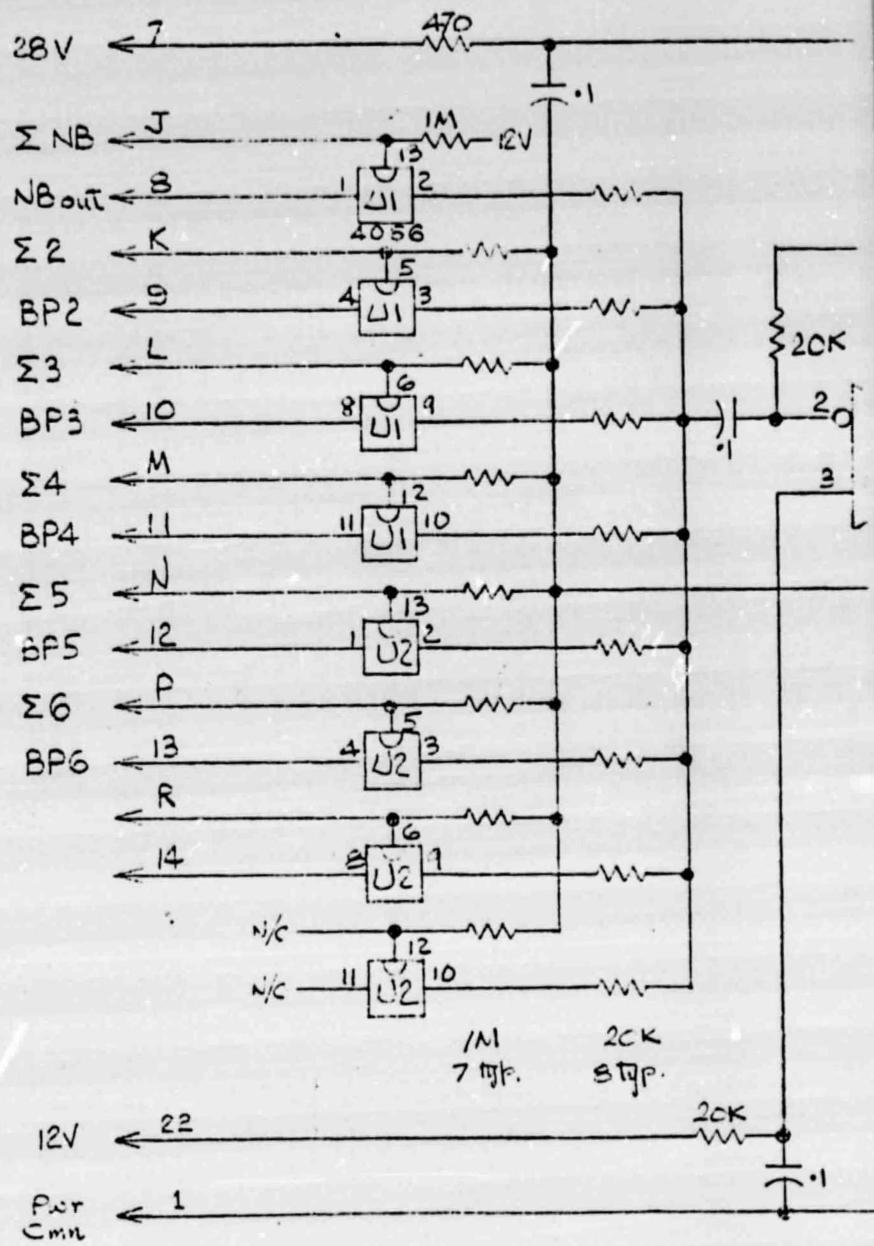
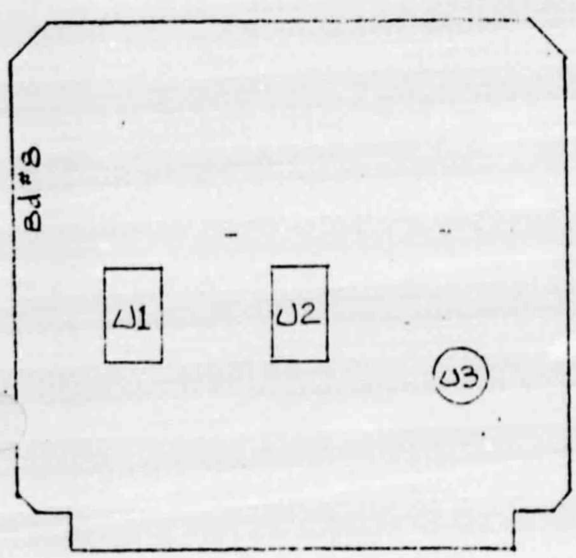
APR. DN 9/1/75	APR.
TITLE SUMMING AMPLIFIER	
PARTS LIST NUMBER P/L 105939	REV -
SHEET 1 OF 1	





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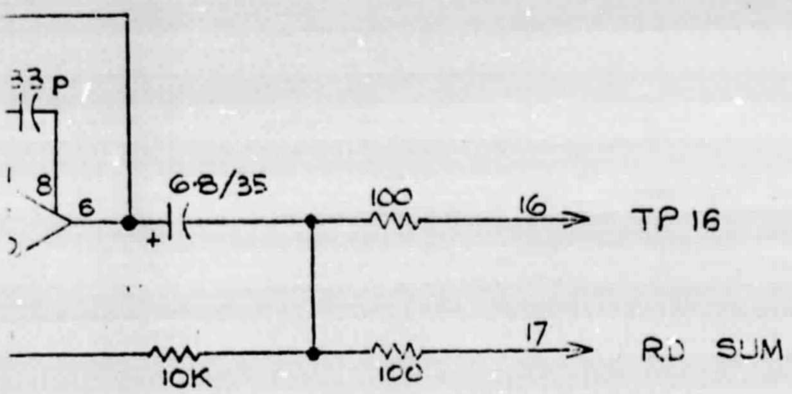

NOTES: (1) U1 & U3 have pin #14 to 12V & pin #7 to power common.

SIGN OFF	INITIALS	DATE
DRAWN	EC	5 Jun 75
CHECKED		
APPROVED		
ENGINEER	C. Kwan	13 Jul 76
PROJ ENGR		

DEVELCO INC.

TITLE

SUMMING AMPLIFIER

SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105739	

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ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
1	105940	SCHEMATIC & ASSY B6		R					
2		PC BOARD 12DE3GP		1					
3									
4		IC RCA - CA3080A		2					
5		" " CA3100T		1					
6	-	" " CA3094T		1					
7		TRANSFORMER	T1	1					
8									
9	47-101277-01	INDUCTOR 225 mH	L1	1					
10	47-101278-01	" 3.19 mH	L2	1					
11									
12		RESISTOR 1/4W 5% 2.7 Ω		1					
13		470 Ω		3					
14		5.1K		2					
15		100 Ω		4					
16		1K		3					
17		27K		2					
18		110K		1					
19		4.7K		1					
20		1.1K		1					
21		110		1					
22		1/4W 5% 1.2K		1					
23		RESISTOR 1/8W 1% 10K		2					
24		" 1/4W 5% 390 Ω		1					
25		" " " 560 Ω		1					
26		TRANSISTOR 2N2484		1					
27		CAPACITOR D.Tant 6.8 10V		2					
28		" " 6.8 35V		1					
29		MICA 10P		1					
30		CK05 .1		5					
31		STYRO 110P		1					
32		STYRO 3000P		1					
33		CAPACITOR 5% mylar .22		1					

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APR. [illegible] 9/1/7[illegible]	APR.
TITLE INPUT BUFFER & CHANNEL 6KHZ	
PARTS LIST NUMBER P/L 105940	REV —
SHEET 1 OF 2	

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.					
34		CAPACITOR CK05 1000P		1					
		" STYRO 5100P		1					
		" CK05 150P		1					
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38									
39									
40									
41									
42									
43									
44									
45									
46									
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48									
49									
50									
51									
2									
3									
54									
55									
56									

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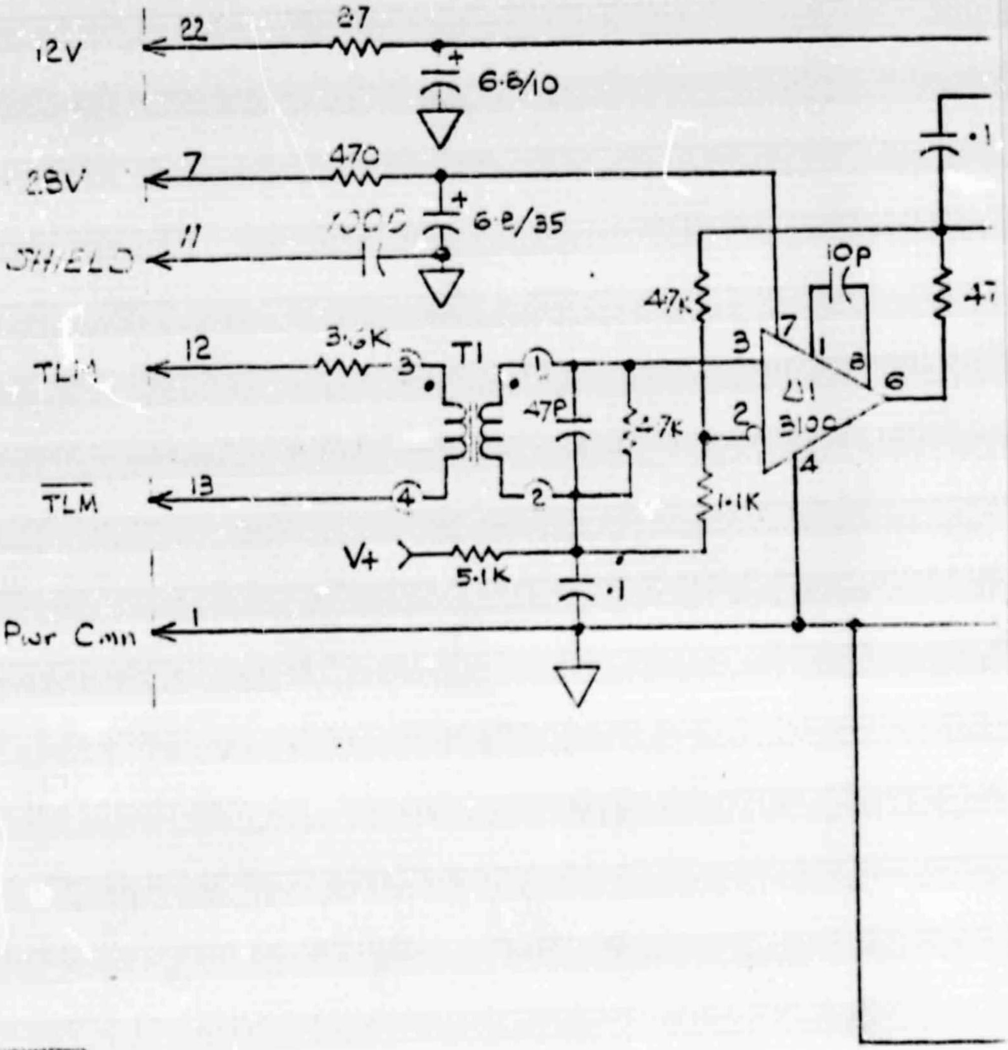
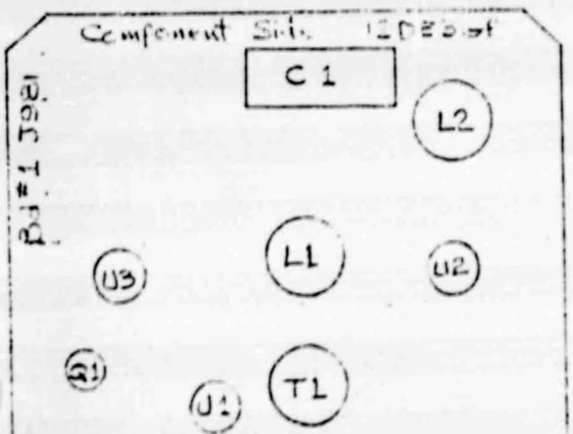
TITLE INPUT BUFFER & CHANNEL 6KHZ	
PARTS LIST NUMBER P/L 105940	REV —
SHEET 2 OF 2	

DEVELCO, INC.





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APPLICATION		

REVISIONS						
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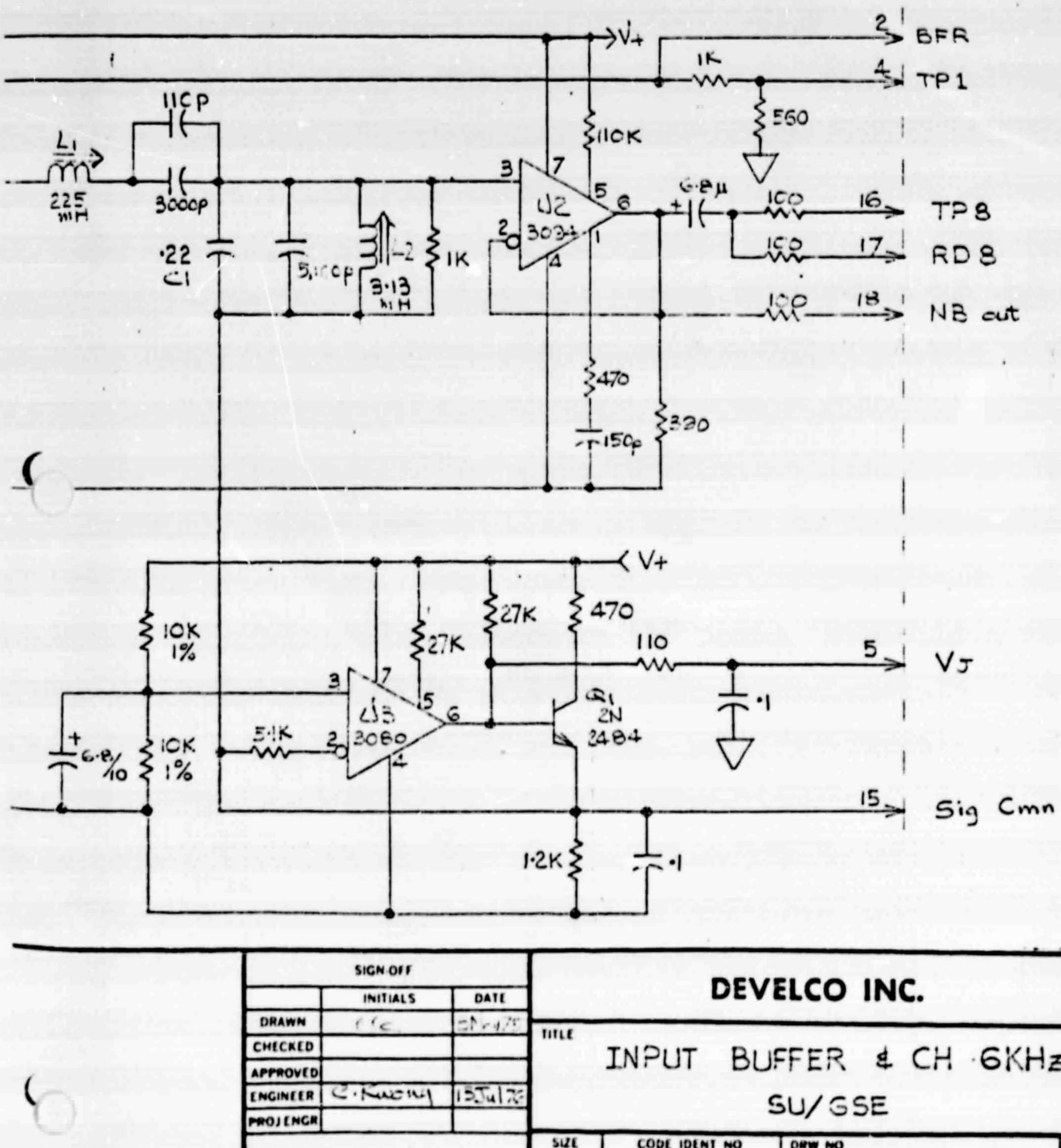

SIGN OFF	INITIALS	DATE
DRAWN	C.C.	5Nov75
CHECKED		
APPROVED		
ENGINEER	C. Kwong	13Jul76
PROJ ENGR		

DEVELCO INC.

TITLE: INPUT BUFFER & CH 6KHz SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105740	

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ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
1	105941	SCHEMATIC & ASSY · B6		R					
2		PC BOARD 122E3GP		1					
3		IC CD4046AE		1					
4		" CA3080A		2					
5		" CA3094T		1					
6		RESISTOR 1/4W 5% 10K		1					
7		160Ω		1					
8		30K		1					
9		20K		4					
10		62K		1					
11		33K		1					
12		56K		1					
13		220		3					
14		2.7		2					
15		1K		2					
16		11K		2					
17		5.1K		1					
18		27K		1					
19		91K		1					
20		620K		1					
21		RESISTOR 1/4W 5% 100K		2					
22		" 1/8W 1% 301K		1					
23		CAPACITOR STYRO 390		2					
24		" 2000		2					
25		CK05 1000P		2					
26		STYRO .036		1					
27		" 1200		1					
28		D TANT 6.3 /10V		4					
29		CK05 .01		1					
30		MYLAR 5% .1		4					
31		" " .027		1					
32		CHIP CER 180P		1					
33		CAPACITOR MYLAR 5% .15		1					

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BY MCM
CK.
APR. EN 9/1/76
APR.

TITLE DISCRIMINATOR

PARTS LIST NUMBER
P/L 105941
REV —

SHEET 1 OF 2

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO.					
34	47-101389-01	INDUCTOR 75.6mH	L1,L3	2					
35	47-101390-01	" 4.36 mH	L2	1					
36									
37		TRANSISTOR 2N2484		1					
38									
39	BECKMAN 3329H	RESISTOR POT 200K		1					
40									
41		RESISTOR 1/4W 5% 390Ω		1					
42		" " " 470Ω		1					
43		" " " 52Ω		1					
44									
45									
46									
47									
48									
49									
50									

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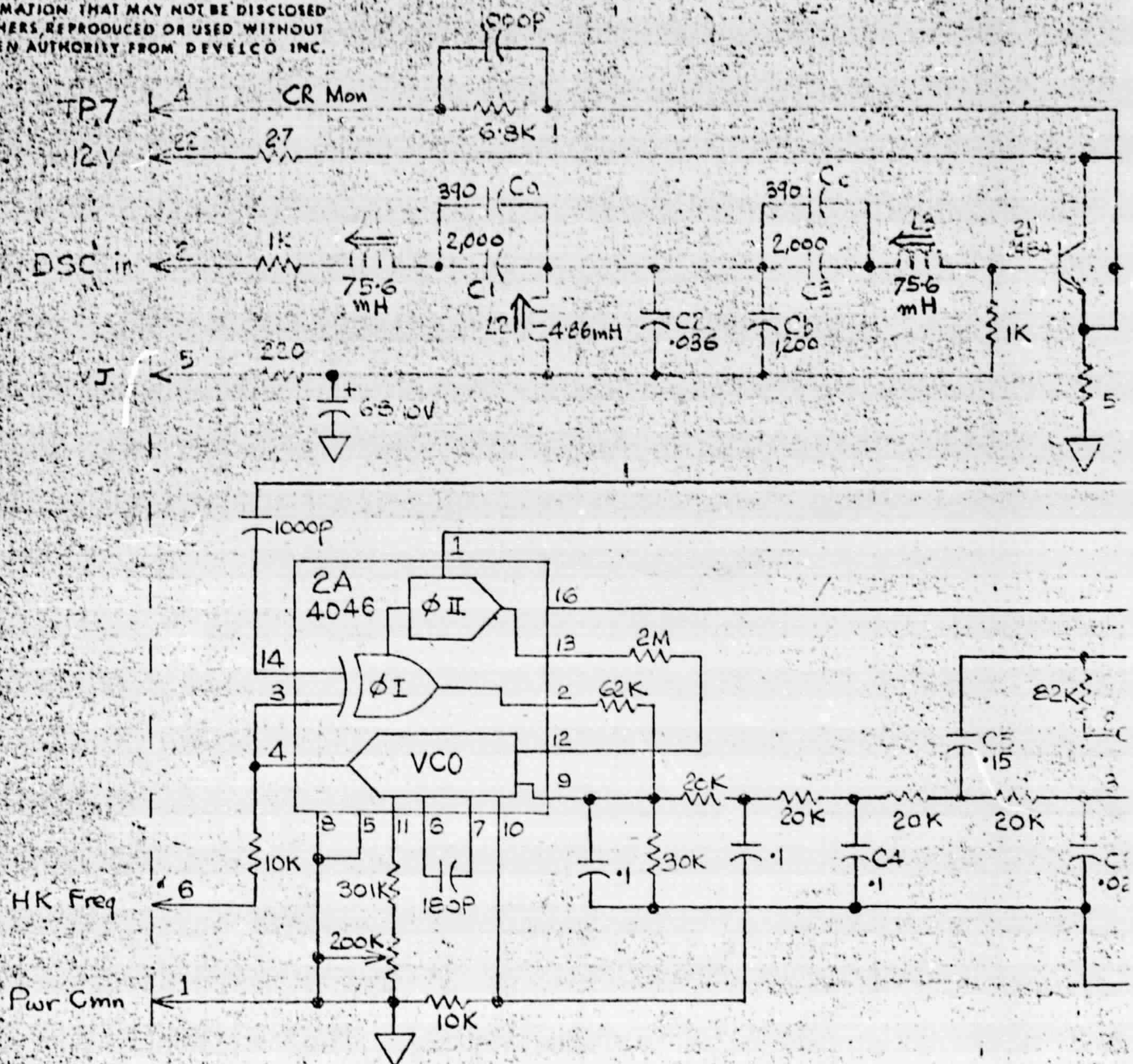
APR. | APR.

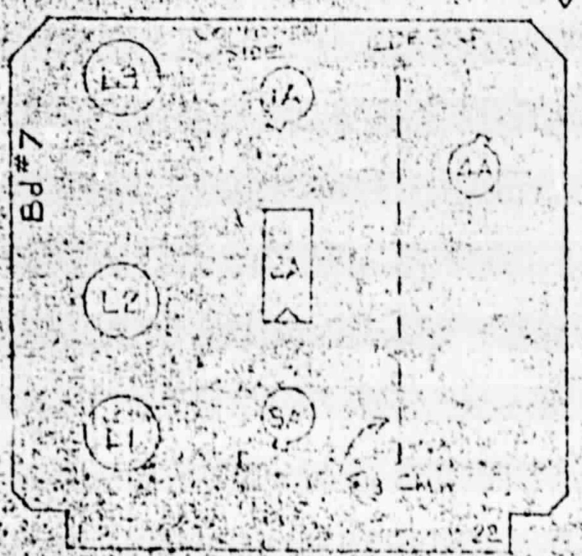
TITLE DISCRIMINATOR

PARTS LIST NUMBER P/L 105941 | REV —

SHEET 2 OF 2

DEVELCO, INC.





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	APPLICATION	

REVISIONS						
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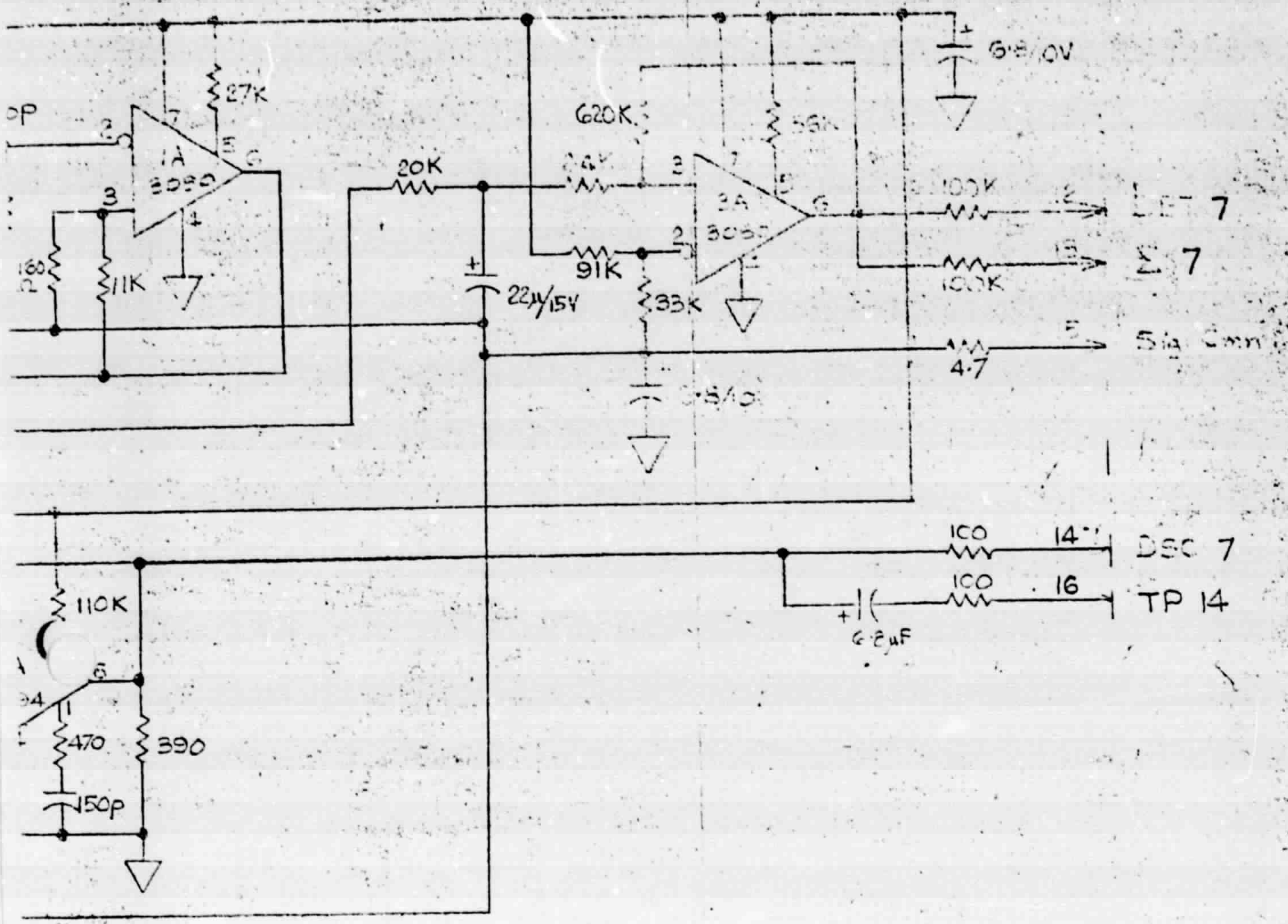

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DRAWN	e2	31Oct75
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APPROVED		
ENGINEER	C. Kwang	13Jul76
PROJ ENGR		

House Keeping Channel

DEVELCO INC.

TITLE

DISCRIMINATOR

SU/GCE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105941	

SCALE | DO NOT SCALE DRAWING | SHEET OF

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	-1	-2	-3	-4	-5
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3		IC CD4046AE		1	1	1	1	1
4		" CA3080A		2	2	2	2	2
5		IC CA3094T		2	2	2	2	2
6								
7		TRANSISTOR 2N2484		1	1	1	1	1
8								
9		RESISTOR 1/4W 5% 6.8K		2	2	2	3	2
10		4.7Ω		1	1	1	1	1
11		1K		5	2	2	2	2
12								
13		10K		3	3	3	3	3
14		3.6K		1	1	1	1	1
15		2.4K		4	3	3	3	3
16		5.1K		1	1	1	1	1
17		11K		2	2	2	2	2
18		160Ω		1	1	1	1	1
19		27K		2	2	2	2	2
20		20K		1	1	1	2	1
21		2.7Ω		1	1	1	1	1
22		620K		1	1	1	1	1
23		91K		1	1	1	1	1
24		33K		1	1	1	1	1
25		39K		2	2	2	2	2
26		100Ω		3	3	3	3	3
27		390		1	1	1	1	1
28		110K		2	2	2	2	2
29		470		2	2	2	2	2
30		10K		-	-	1	-	-
31		39K		-	-	-	-	1
32		820Ω		1	-	-	-	-
33		RESISTOR 1/4W 5% 1.6K		-	1	-	-	-

REV

FREQ
-1 384 KHz
-2 192 "
-3 96 "
-4 48 "
-5 24 "

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TITLE DISCRIMINATOR

PARTS LIST NUMBER P/L 105942 REV —

SHEET 1 OF 3

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	-1	-2	-3	-4	-5
34		RESISTORS 1/4W 5% 3.3K		–	–	1	–	–
35		13K		–	–	–	–	1
36		2K		–	3	–	–	–
37		3.9K		–	–	3	–	–
38		8.2K		–	–	–	3	–
39		16K		–	–	–	–	3
40		240K		1	–	–	–	–
41		510K		–	1	–	–	–
42		1M		–	–	1	1	–
43		1/4W 5% 2M		–	–	–	–	1
44								
45		1/8W 1% 40.2K		–	1	–	–	–
46		20K		1	–	–	–	–
47		30.6K		–	–	1	1	–
48		RESISTOR 1/8W 1% 150K		–	–	–	–	1
49								
50		RESISTOR POT BECKMAN 3329H 10K		1	–	–	–	–
51		" 20K		–	1	–	–	–
52		" 50K		–	–	1	1	–
53		RESISTOR POT " 100K		–	–	–	–	1
54								
55								
56		CAPACITOR DIP TANT 6.8/10V		4	4	4	4	4
57		CK05 1000P		3	3	3	3	3
58		DIP TANT 22μ/15V		1	1	1	1	1
59		CK05 .01		2	2	2	2	2
60		CK05 150P		1	1	1	1	1
61		STYRO 360P		1	1	1	1	1
62		[illegible] .047		1	1	1	1	1
63		STYRO 9100P		1	1	1	1	1
64		CK05 .1		1	1	1	1	1
65		NPO [illegible] 51P		1	1	1	–	–
66		CAPACITOR NPO [illegible] 180P		–	–	–	1	1

BY	CK.
APR.	APR.
TITLE DISCRIMINATOR	
PARTS LIST NUMBER P/L 105742	REV –
SHEET 2 OF 3	

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO. -1	-2	-3	-4	-5
67		CAPACITOR STYRO 110P		2	–	–	–	–
68		" 220P		–	2	–	–	–
69		" 430P		–	–	2	–	–
70		" 910P		–	–	–	2	–
71		" 1800		–	–	–	–	2
72		" 680P		1	–	–	–	1
73		" 1500P		–	1	–	–	–
74		" 3000		–	–	1	–	–
75		" 6200		–	–	–	1	–
76		" .012		–	–	–	–	1
77		" 100P		1	–	–	–	–
78		" 68P		–	1	–	–	–
79		" 150P		–	–	1	–	–
80		STYRO 15P		–	–	1	–	–
81		CK05 510		1	–	–	–	–
82		" 1000		–	1	–	–	–
83		" 2000		–	–	1	–	–
84		" 3900		–	–	–	1	–
85		CAPACITOR " 8200		–	–	–	–	1
86								
87	47-101279-01	INDUCTOR 1.61 mH	L1, L3	2	–	–	–	–
88	1281	3.22 "	L1, L3	–	2	–	–	–
89	1283	6.43 "	L1, L3	–	–	2	–	–
90	1285	12.9 "	L1, L3	–	–	–	2	–
91	1287	25.7 "	L1, L3	–	–	–	–	2
92	1280	231 μH	L2	1	–	–	–	–
93	1282	462 "	L2	–	1	–	–	–
94	1284	926 "	L2	–	–	1	–	–
95	1286	1.85 mH	L2	–	–	–	1	–
96	47-101288-01	INDUCTOR 3.70 "	L2	–	–	–	–	1
97								
98								
99								

REV

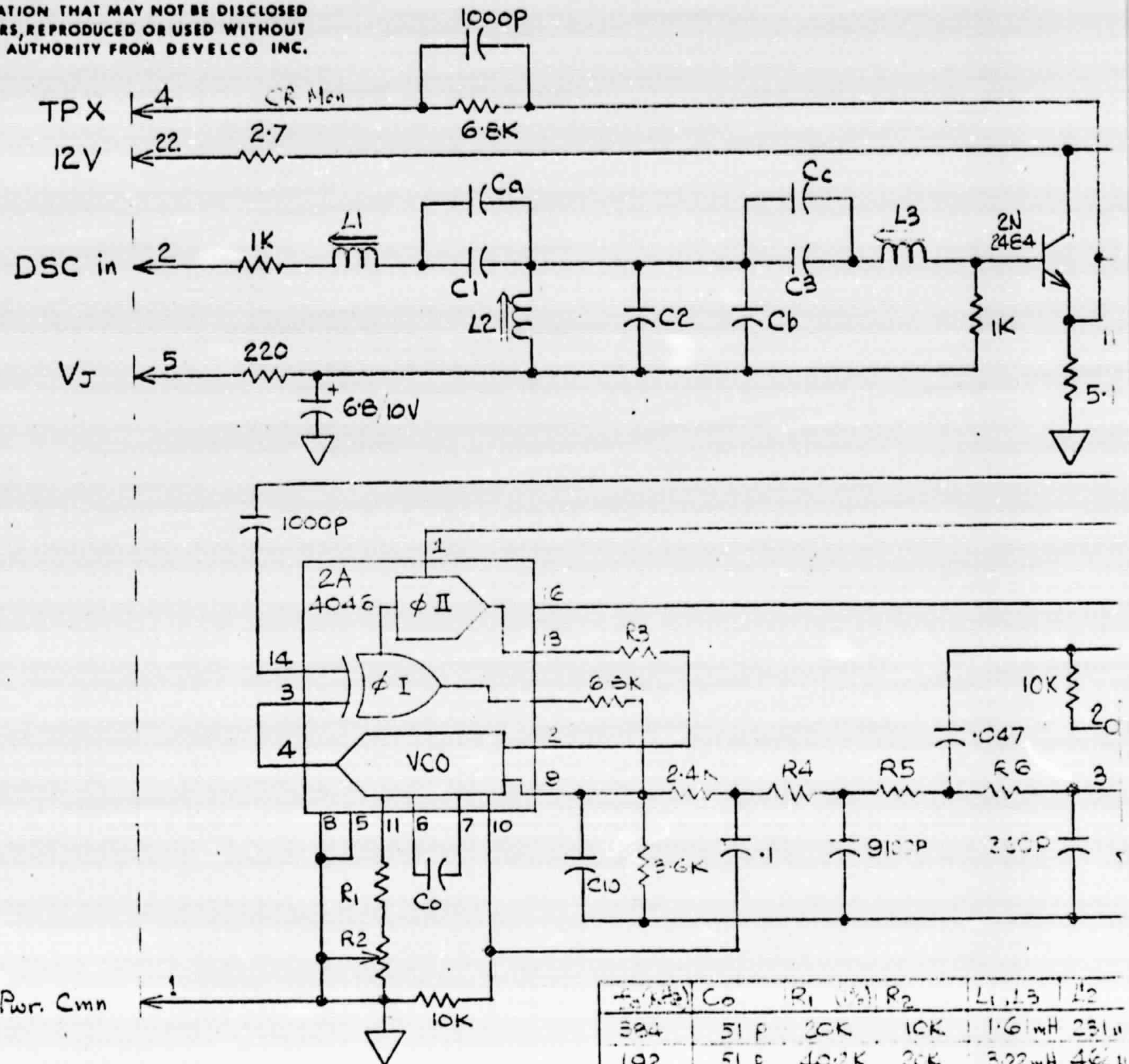
BY | CK.
APR. | APR.

TITLE DISCRIMINATOR

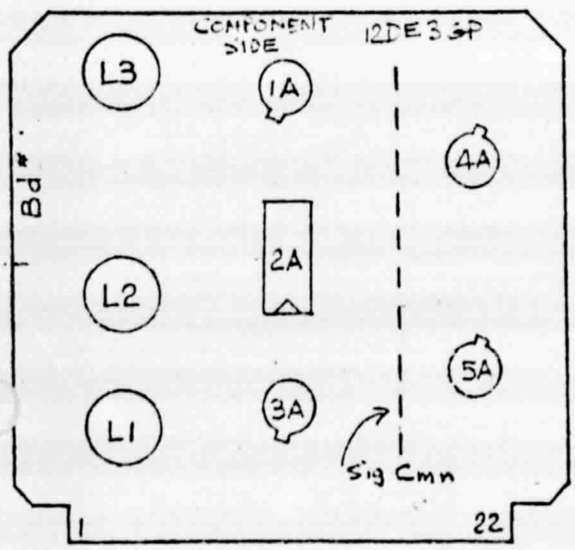
PARTS LIST NUMBER P/L 105942 | REV

SHEET 3 OF 3

DEVELCO, INC.

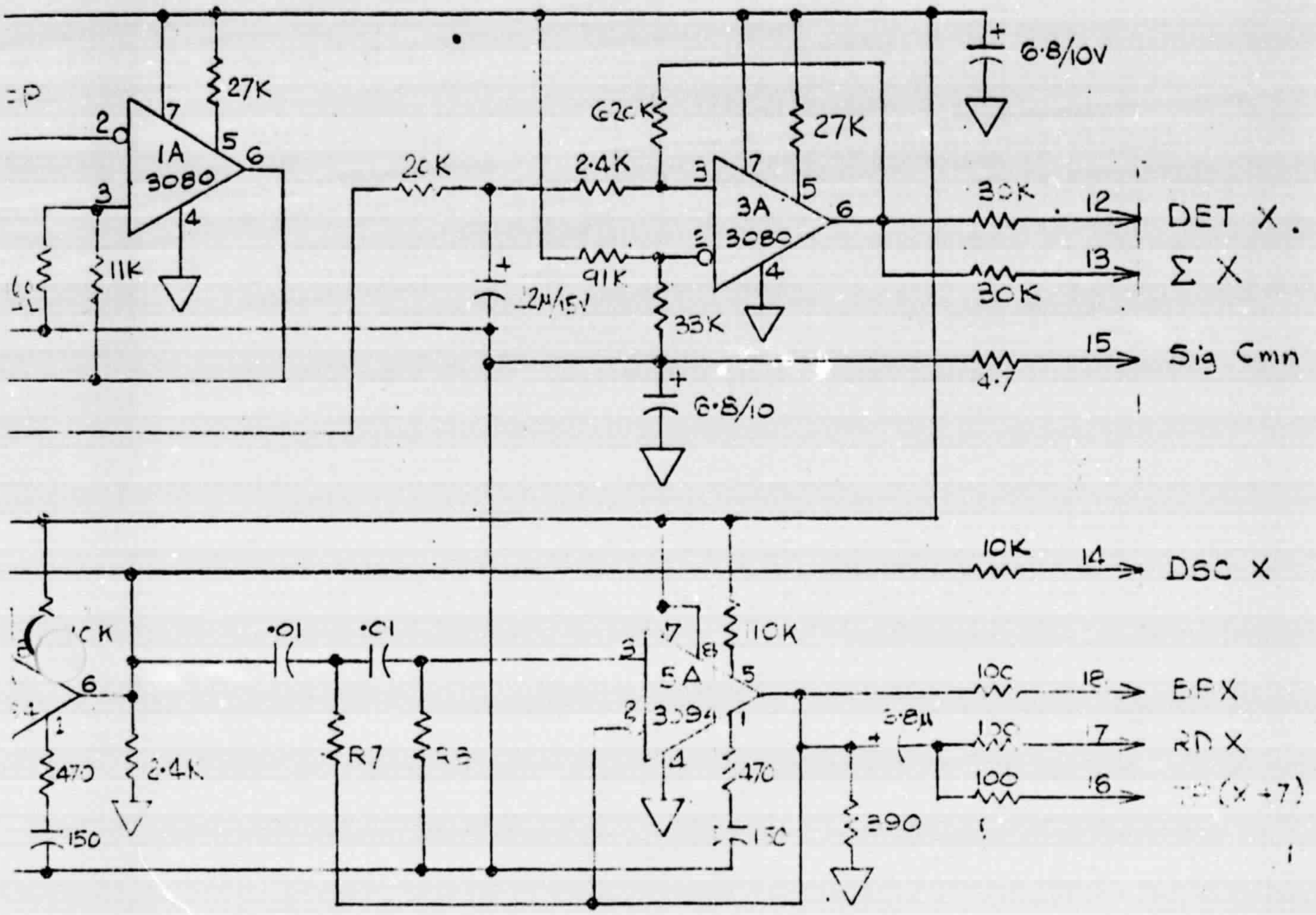


f_o (kHz)	C_o	R_1 (1%)	R_2	L_1, L_3	L_2
384	51 p	20K	10K	1.6 mH	231u
192	51 p	40.2K	20K	3.22 mH	46
96	51 p	80.6K	50K	6.43	926
48	180 p	80.6K	50K	12.9	1.85
24	180P	150K	100K	25.7	3.70



USED ON	NEXT ASS'Y	QTY REQ
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



,C3	Ca, Cc	C2	Cb	R	R4,5,6	R7	R8	C4	OPT. N	B.I#
10P	—	680P	100P	240K	1K	820Ω	2.4K	510	[illegible]	2
220P	—	1,500P	68P	510K	2K	1.6K	4.7K	1,000	[illegible]	3
430P	15P	3,000P	15P	1M	3.3K	3.3K	10K	2,000	[illegible]	4
910P	—	6200P	110P	1M	8.2K	6.8K	20K	3,900	[illegible]	5
800P	—	.012	680P	2M	16K	13K	39K	8,200	[illegible]	6

ORIGINAL PAGE IS OF POOR QUALITY

SIGN-OFF	INITIALS	DATE
DRAWN	[illegible]	[illegible]
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE

DISCRIMINATOR

SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	[illegible]	

SCALE | DO NOT SCALE DRAWING | SHEET OF

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO.
1	105943	SCHEMATIC & ASSY	B6		R
2		PC BOARD 12DEGGP			1
3		IC RCA CA3080A		U1	1
4		" " CA3094J		U4	1
5		" MODULE ANALOG DEVICES 440J		U5	1
6		IC RCA CA3096E		U3, U7	2
7		IC NATIONAL LM2500N		U2, U6	2
8		TRANSISTOR 2N2484			2
9		RESISTOR 1/4W 5% 100Ω			2
10		10K			2
11		4.7			2
12		390			1
13		27K			2
14		47K			1
15		220			1
16		100K			1
17		68K			1
18		6.8K			2
19		470			1
20		560K			2
21					
22		30K			4
23		9.1K			4
24		300			2
25		33K			2
26		51K			2
27		VARIABLE 10K		R2, R4, R3	3
28		" 100Ω		R5,	1
29		RESISTOR " 200Ω		R1	1
30					
31		CAPACITOR CK05 .001			2
32		" .01			2
33		D. TANT 6.8μ/35V			3

REV

BY AKM | CK.

APR. [illegible] 9/1/76 | APR.

TITLE METER AMP

PARTS LIST NUMBER P/L 105943 | REV –

SHEET 1 OF 2

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
				.					
34		CAPACITOR CK05 .1		5					
35		" CK05 •150pf		1					
36		" DIP TANT 22µf/10V		1.					
37									
38									
39		DIODE 1N4154		1					
40									
41		RESISTOR 1/8W 1% 249		2					
42		" " " 10K		1					

BY MCM	CK.
APR.	APR.

TITLE

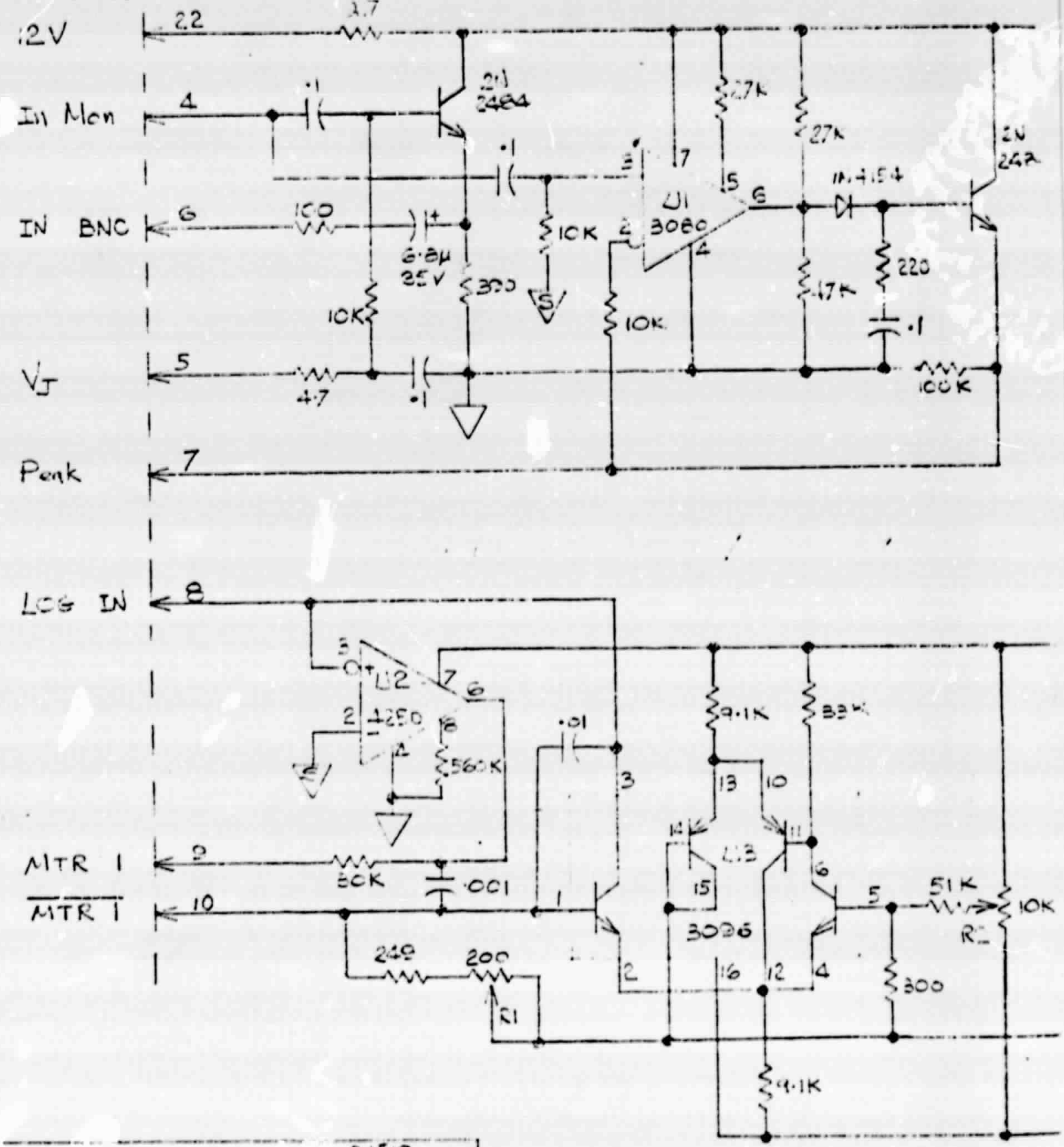
METER AMP

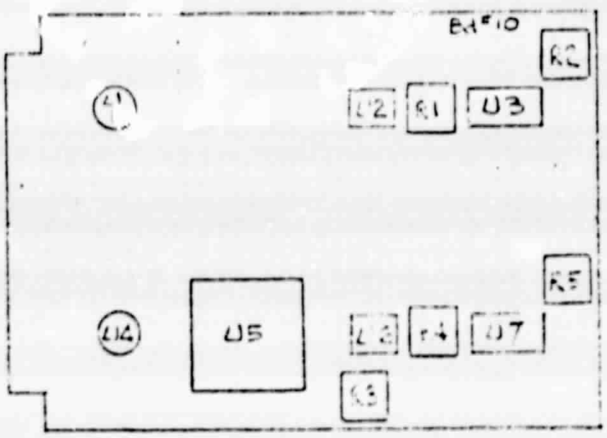
PARTS LIST NUMBER	REV
P/L 105943	—

SHEET 2 OF 2

REV

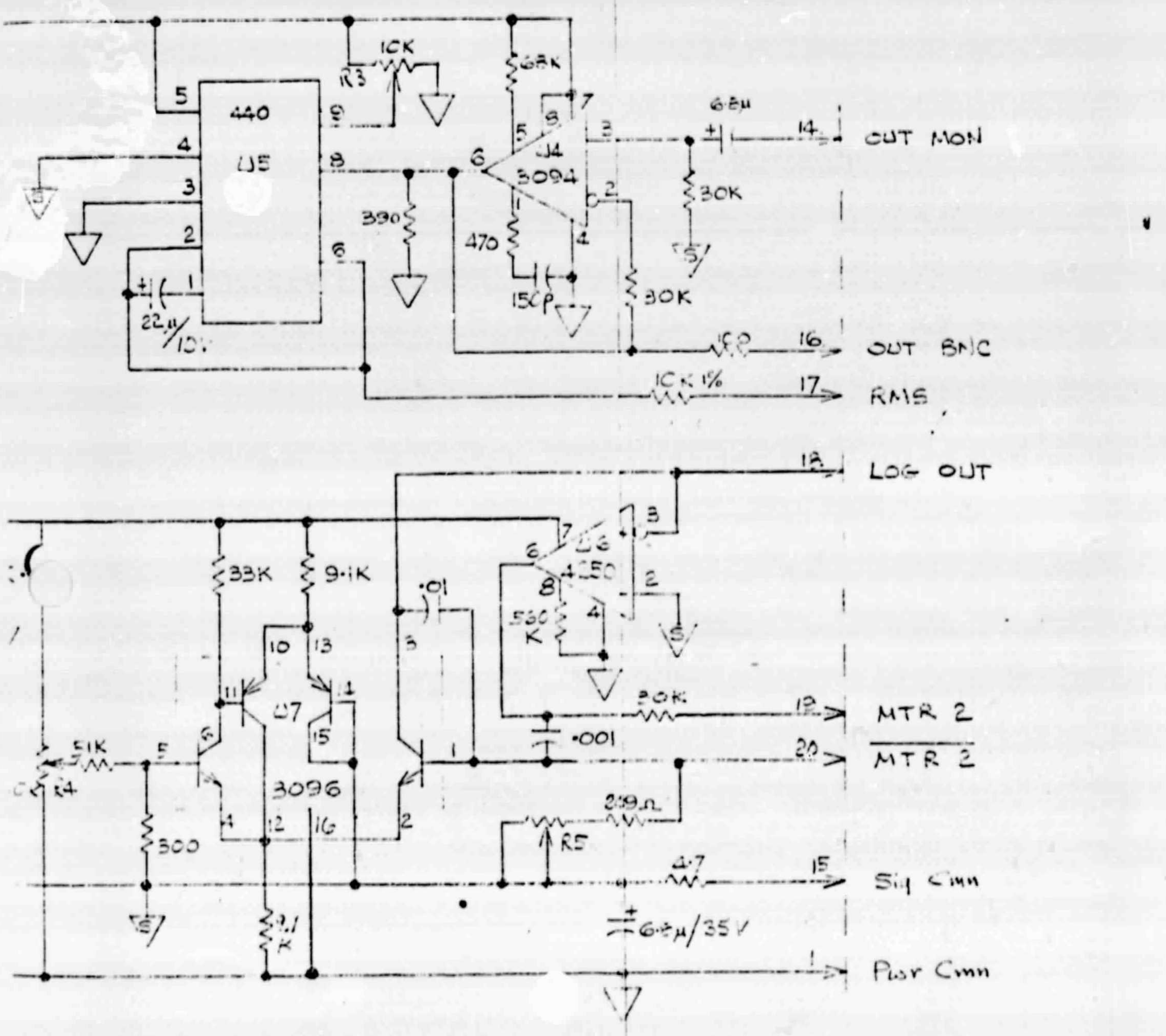
DEVELCO, INC.





USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



SIGN OFF	INITIALS	DATE
DRAWN	ESC	
CHECKED		
APPROVED		
ENGINEER	C Gorman	13Jul76
PROJ ENGR		

B1#10

DEVELCO INC.

TITLE

METER AMP

SJ/G8E

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105743	

SCALE	DO NOT SCALE DRAWING	SHEET	OF

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO					
1	105944	SCHEMATIC & ASSY	B6		R					
		PC BOARD RDE6GP			1					
	CD4029AE	IC		U7,U12,U10 U11	4					
4	" 4046 "	"		U9,	1					
5	CD4013AE	"		U3,	1					
6	CA3080A	"		U1 THRU U4	4					
7	CD4066AE	"		U6	1					
8	CD4030AE	IC		U14	1					
9	CA3094T	IC		U5	1					
10		RESISTOR 1/4W 5%	2.7		1					
11			56M		1					
12			560K		2					
13			51K		2					
14			33K		2					
15			3.3M		2					
16			120K		2					
17			10M		2					
18			82M		1					
9			100K		2					
			200K		1					
21			220		1					
22			110K		1					
23			10K		2					
24			5.6K		5					
25			1M		1					
26			390Ω		1					
27			430Ω		1					
28		1/4W 5%	150K		1					
29	BECKMAN 3329H-50K	RESISTOR, VARIABLE	50K		1					
30										
31		CAPACITOR D.TANT	6.8 35V		1					
32		" CK05	1000 pF		3					
33	ITX405K.5A REL CAP.	" POLY	4u		3					

BY MCM	CK.
APR. [illegible] 9/1/7.	APR.

TITLE
DETECTOR & CLOCK GEN

PARTS LIST NUMBER	REV
P/L 105944	—

SHEET 1 OF 2

REV

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO
34		CAPACITOR STYRO 2,200P		1
35		STYRO 6,200P		1
36		5% MYLAR .082		1
37		NPO CER 180P		1
38				
39		CAPACITOR POLY .1µ		2
40		" POLY .56		1
41				
42		DIODE 1N270		2
43				
44				
45				
46				
47				
48				
49				
50				

BY

CK.

APR.

APR.

TITLE

DETECTOR & CLOCK GE

PARTS LIST NUMBER

P/L 105944

REV —

SHEET 2 OF 2

DEVELCO, INC.

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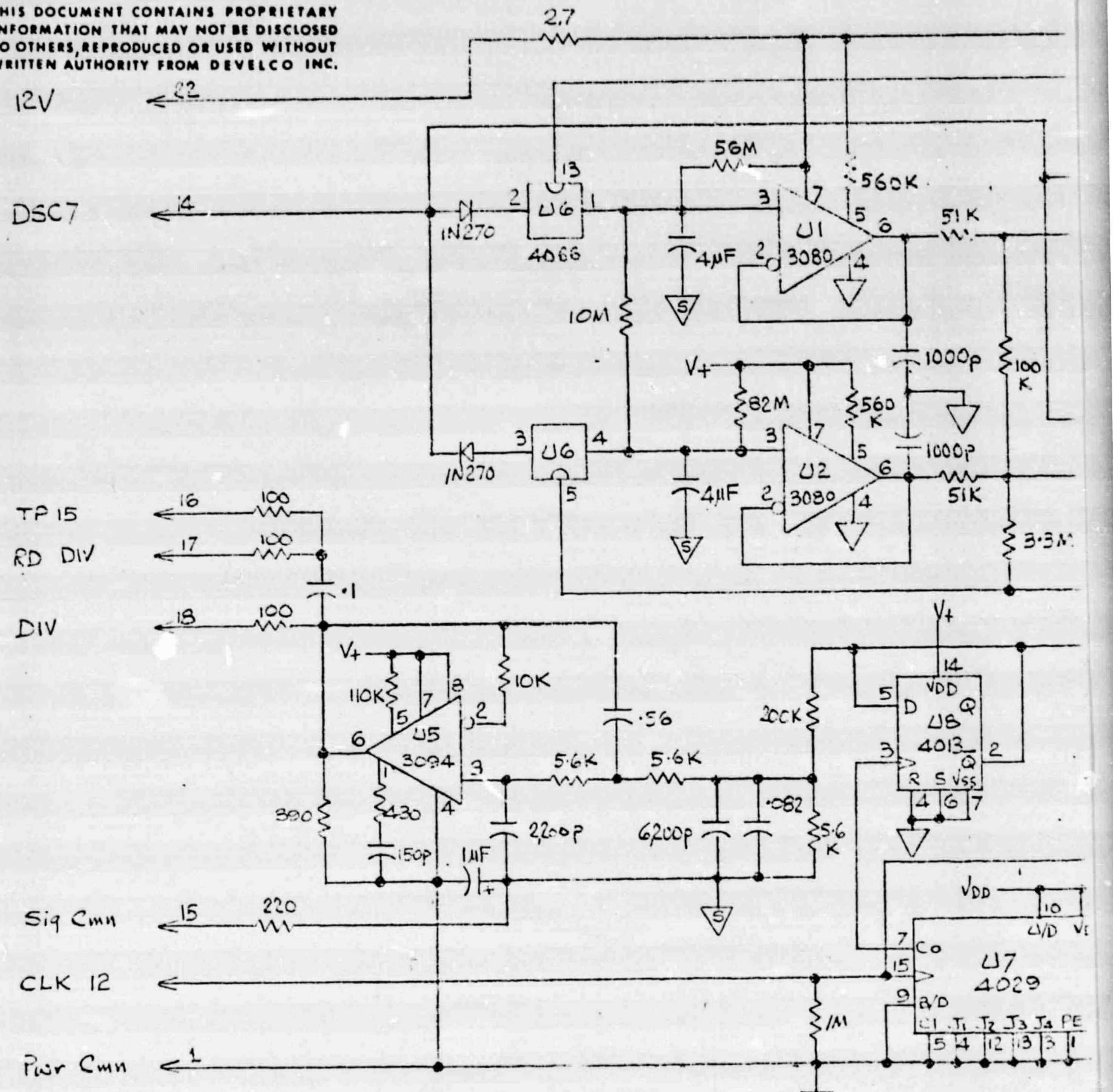
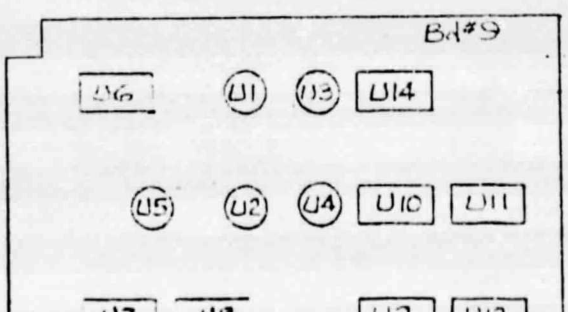
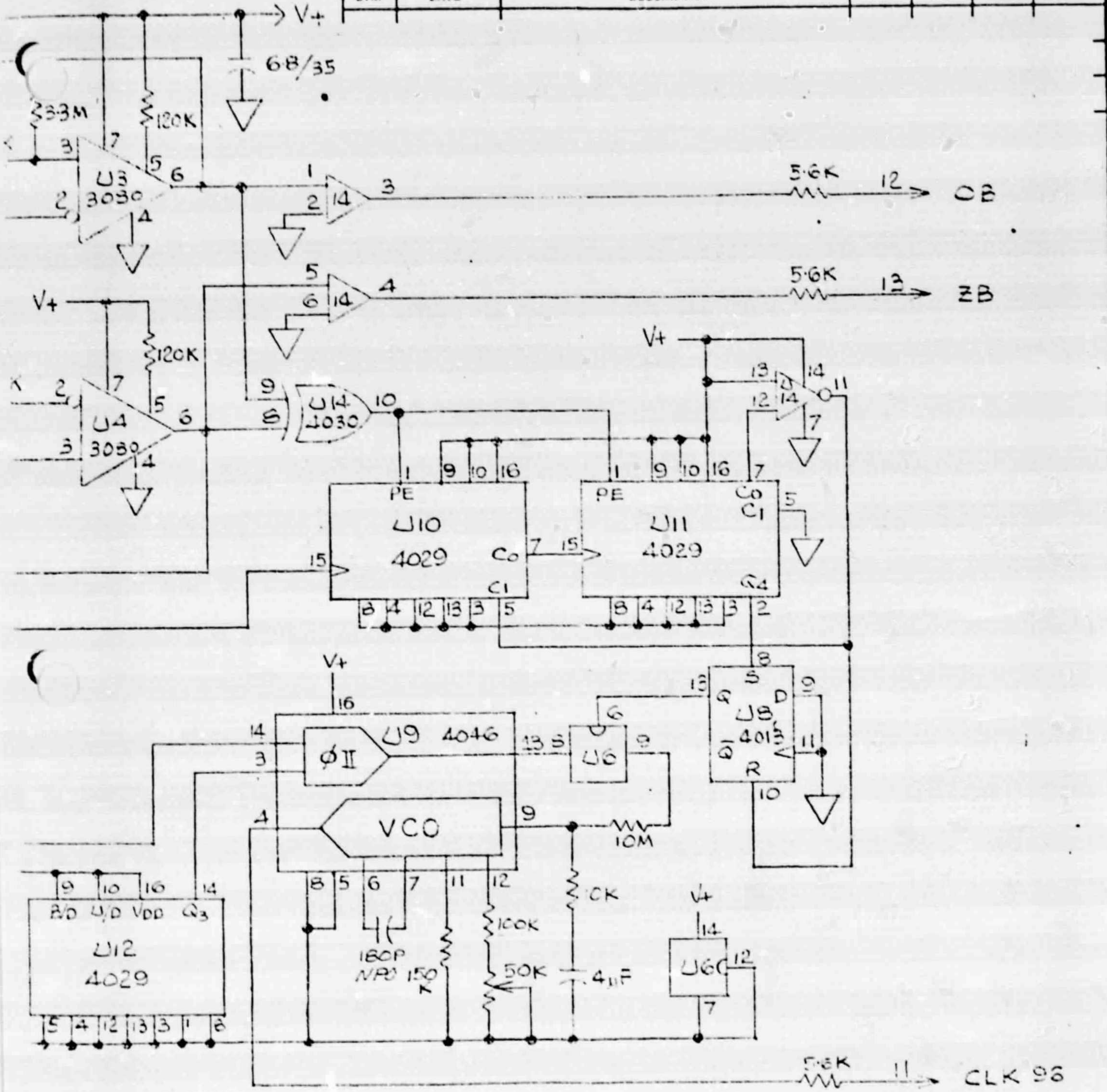




USED ON	NEXT ASS'Y	QTY REQD

APPLICATION

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



SIGN OFF	INITIALS	DATE
DRAWN	TCa	11Nov75
CHECKED		
APPROVED		
ENGINEER	C. Kuxcm	13Jul76
PROJ ENGR		

Bd # 9

DEVELCO INC.

TITLE
DETECTOR & CLOCK GEN.
SU / GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	6-105944	

SCALE	DO NOT SCALE DRAWING	SHEET	OF

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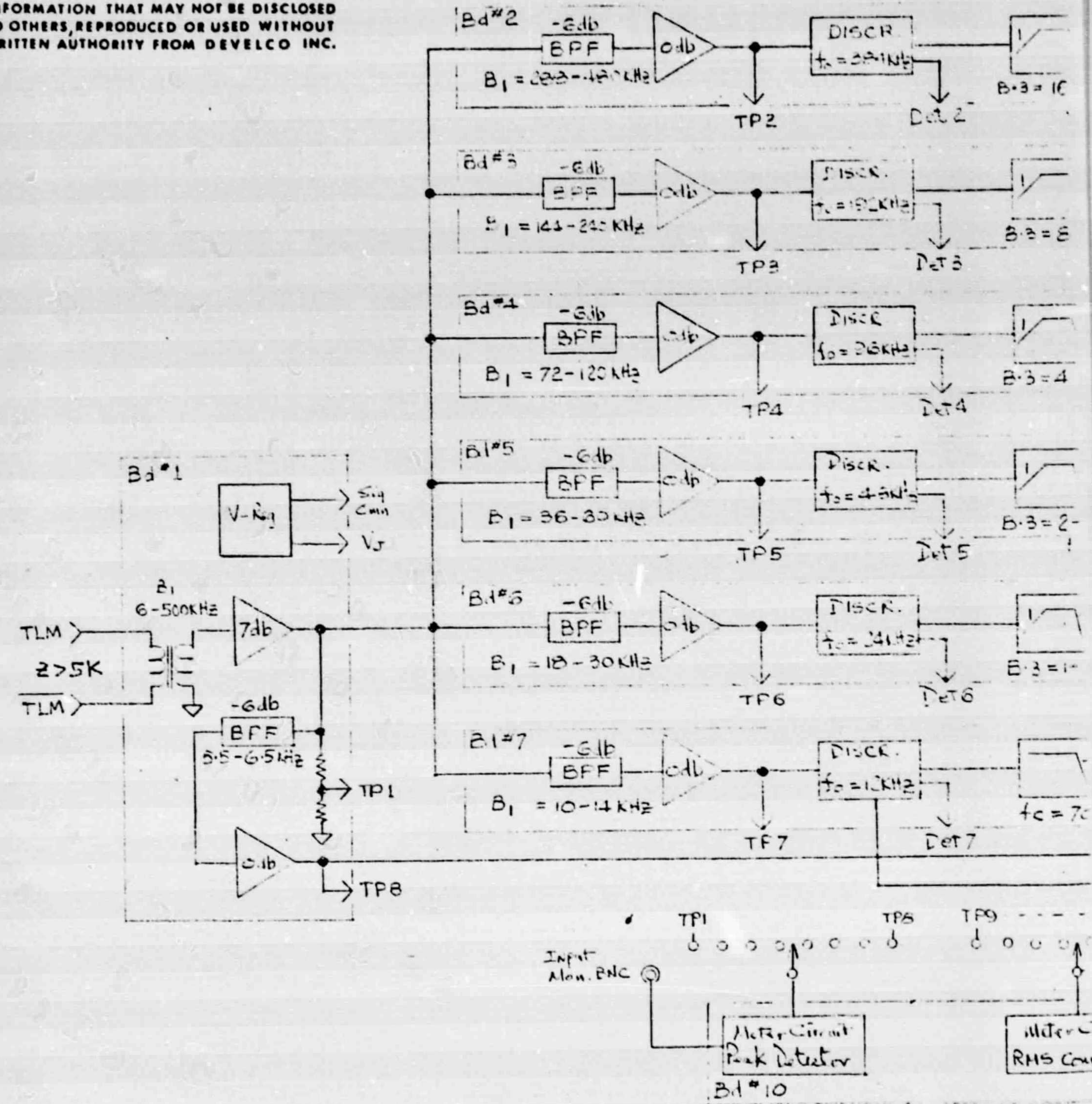
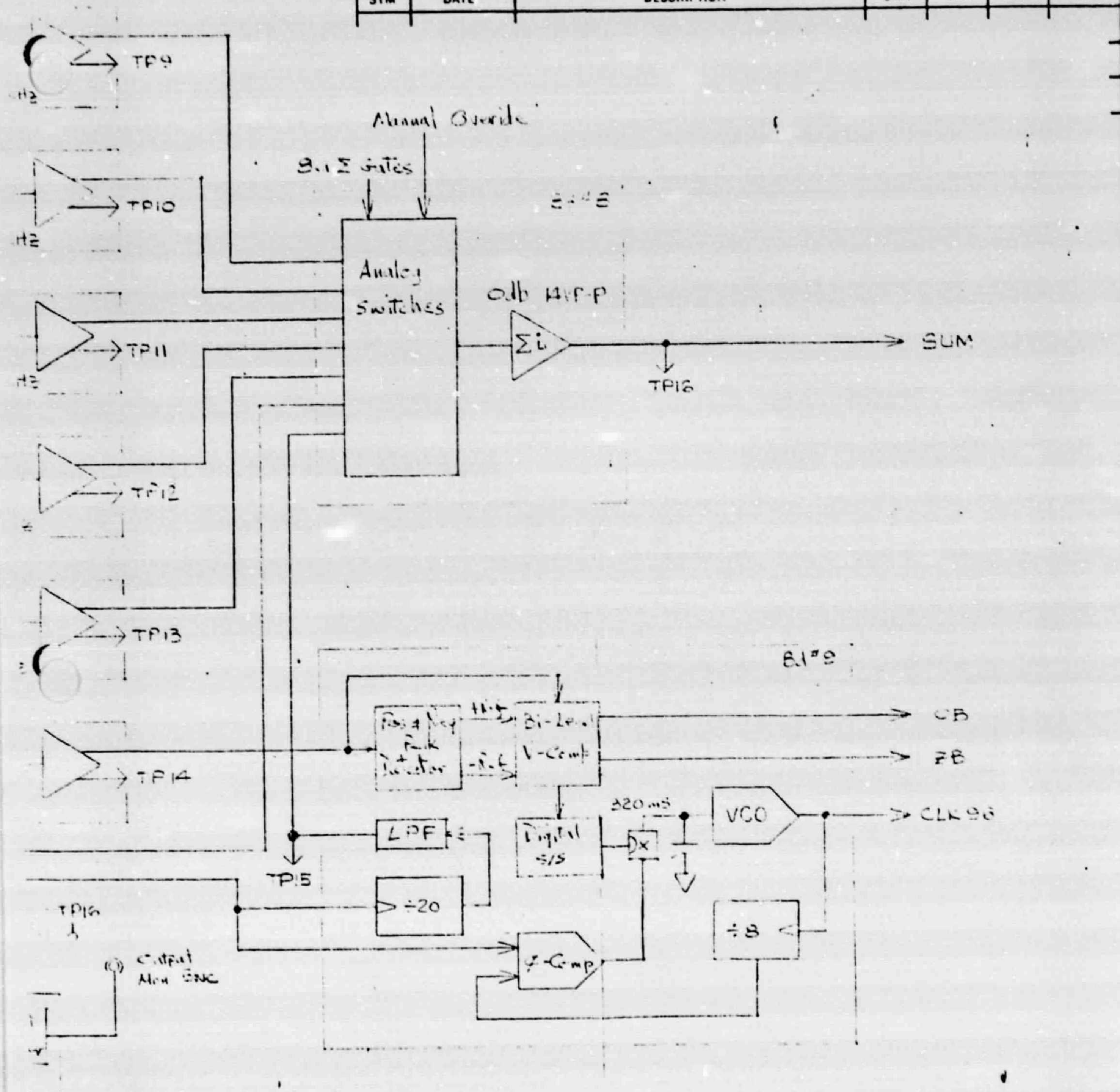


USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



SIGN OFF	INITIALS	DATE
DRAWN		13 Nov 75
CHECKED		
APPROVED		
ENGINEER	C. Cheung	13 Jul 75
PROJ ENGR		

DEVELCO INC.

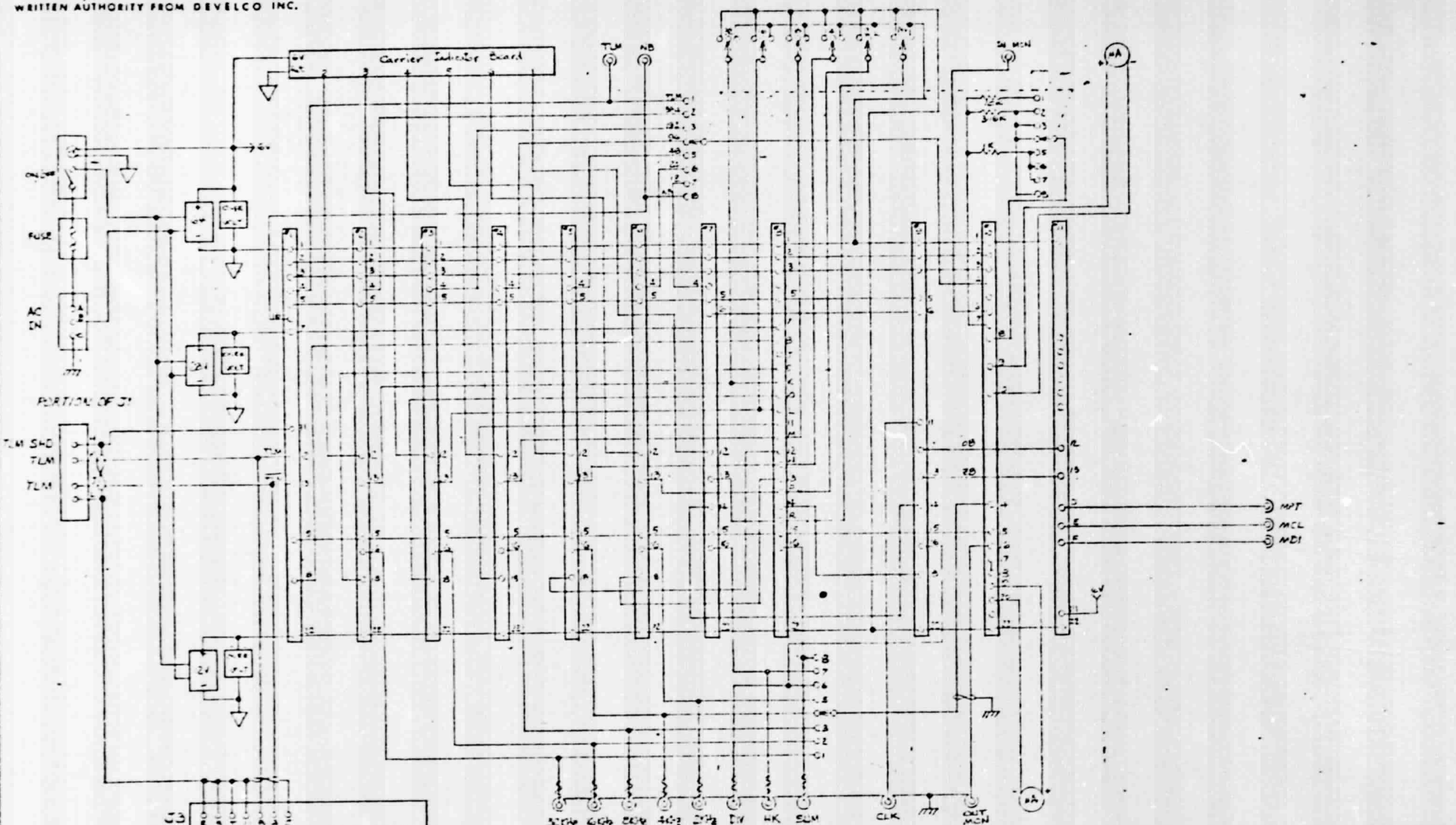
TITLE ANALOG BLOCK DIAGRAM

SU/GSE

SIZE	CODE IDENT NO	DRW NO	REV
B	30002	105945	

SCALE	DO NOT SCALE DRAWING	SHEET	OF

REVISIONS					
SYM	DATE	DESCRIPTION	CKD	APPR	DATE



USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER	C Cuning	5 Aug 75
PROJ ENGR		

DEVELCO INC.

TITLE: HEM GSE BACK PLANE

SIZE	CODE IDENT NO	DRW NO	REV
C		6-105958	

SCALE | DO NOT SCALE DRAWING | SHEET OF

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO					
1	106037	SCHEMATIC & ASSY D6		R					
2	105739-2	PC BD PLUGGP		1					
3									
4	CD4011AE	IC	D1.E3	2					
5	4023		F3	1					
6	4001		F5	1					
7	4013		C1.E5.F1	3					
8	4049		E1	1					
9	4017		E2.F2.E4.F4	4					
10	4015		D2-D5	4					
11	4052		C2-C5	4					
12	4053		A2.B2	2					
13	4036		A1	1					
14	CD 4040AE	IC	B3	1					
15									
16		SOCKET 14 PIN WIREWRAP		5					
17		" 16 " "		6					
18		" 24 " "		1					
19									
20		RESISTOR 1/4W 5% 220K		1					
21		" POT 1 TURN 20K		1					
22									
23		CAPACITOR DIP MICA 270PF		1					
24		" CK05 .001		1					
25									
26		CABLE ANSLEY 171-26		A/R					
27		CONNECTOR DIP 3M 3406		2					
28		STRAIN RELIEF 3M 3448-8		2					
29									
30									
31									
32									
33									

REV

BY [illegible] CK.

APR. [illegible] 9/1/76 APR.

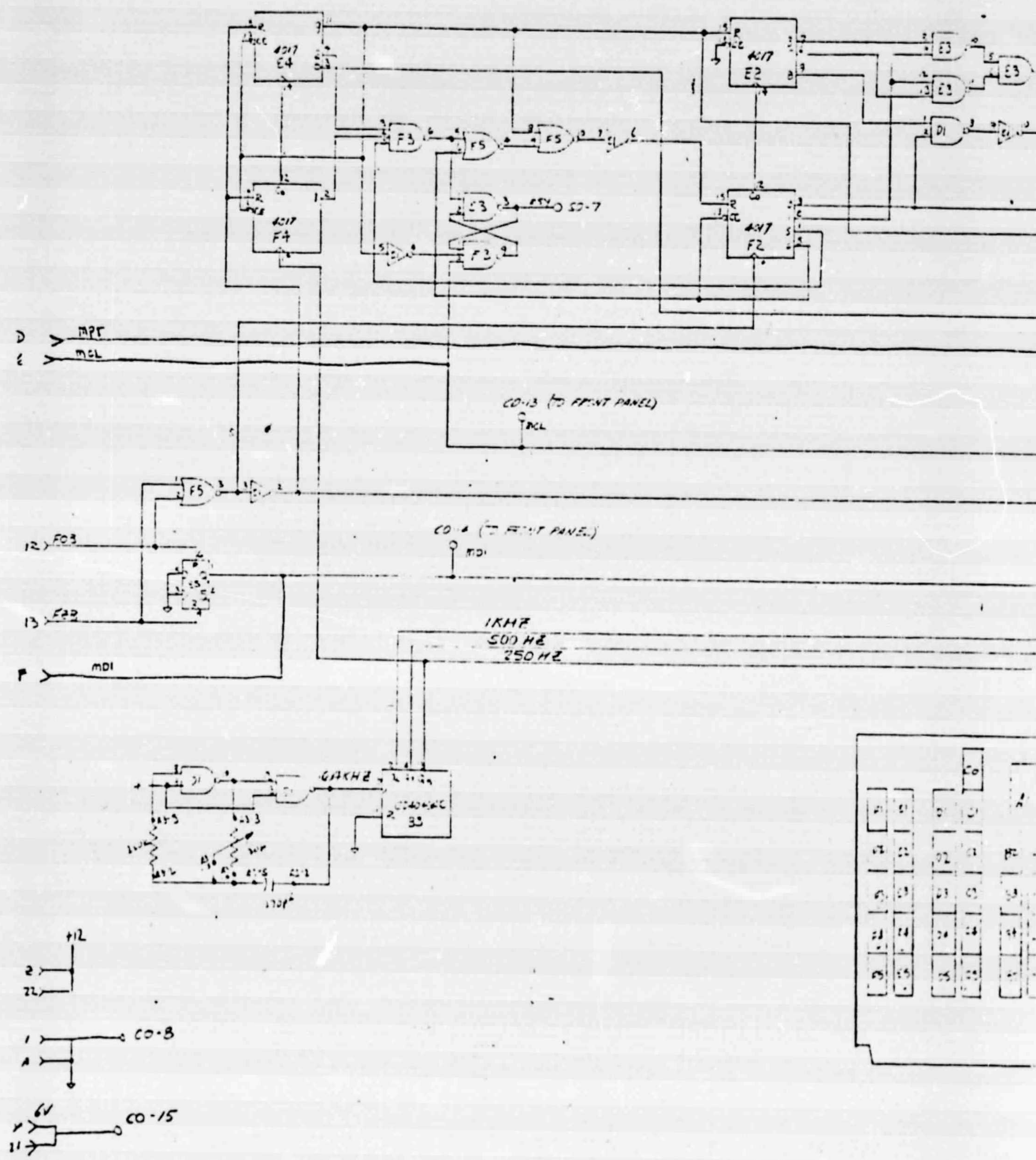
TITLE HEM DATA MONITOR DECODER-DISPLAY MULTIPLEX

PARTS LIST NUMBER REV

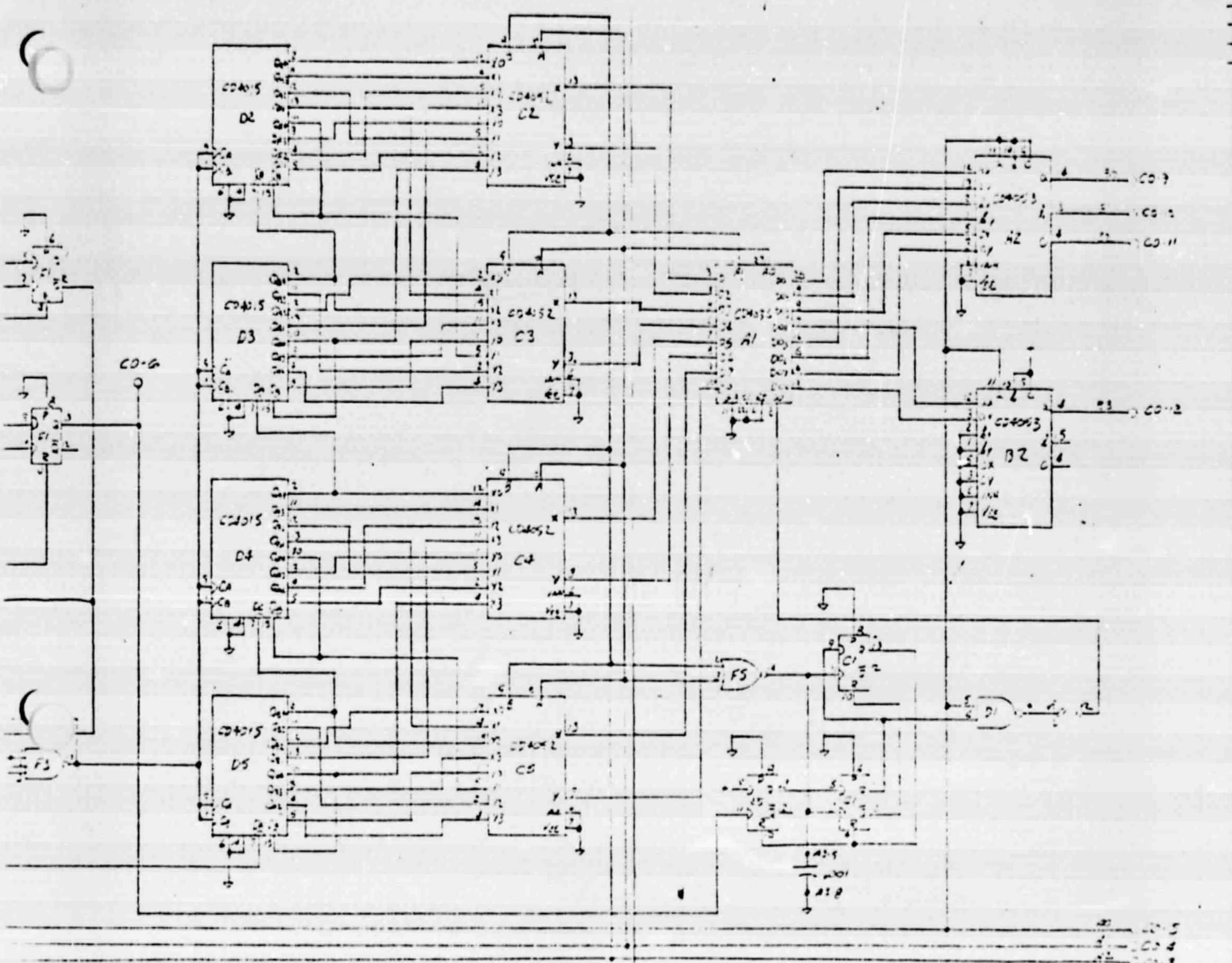
P/L 106037 –

SHEET 1 OF 1

DEVELCO, INC.


4017
E4
4017
F4
4017
E2
4017
F2
F3
F5
E3
F3
D1
MPT
MCL
CO-13 (TO FRONT PANEL)
MDI
1KHZ
500 HZ
250 HZ
64KHZ
B3
+12
CO-8
6V
CO-15

SYM	DATE	REVISIONS DESCRIPTION	DRN	CKD	APPR	DATE



NOTE
CO IS 3M CABLE SOCKET

SKT NO	P/N	# OF PINS	VDD PIN #	VSS PIN #
D1, E3	CD4011	14	14	7
F3	CD4023	14	14	7
F5	CD40[illegible]	14	14	7
C1, E5, F1	CD4013	14	14	7
E1	CD4049	16	1	8
C2, F2, E4 [illegible]	CD40[illegible]7	16	16	8
D2-D5	CD4015	16	16	8
C2-C5	CD4052	16	16	8
A2, B2	CD4053	16	16	8
A1	CD40[illegible]2	24	24	12
E3	[illegible]	14	14	7

USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

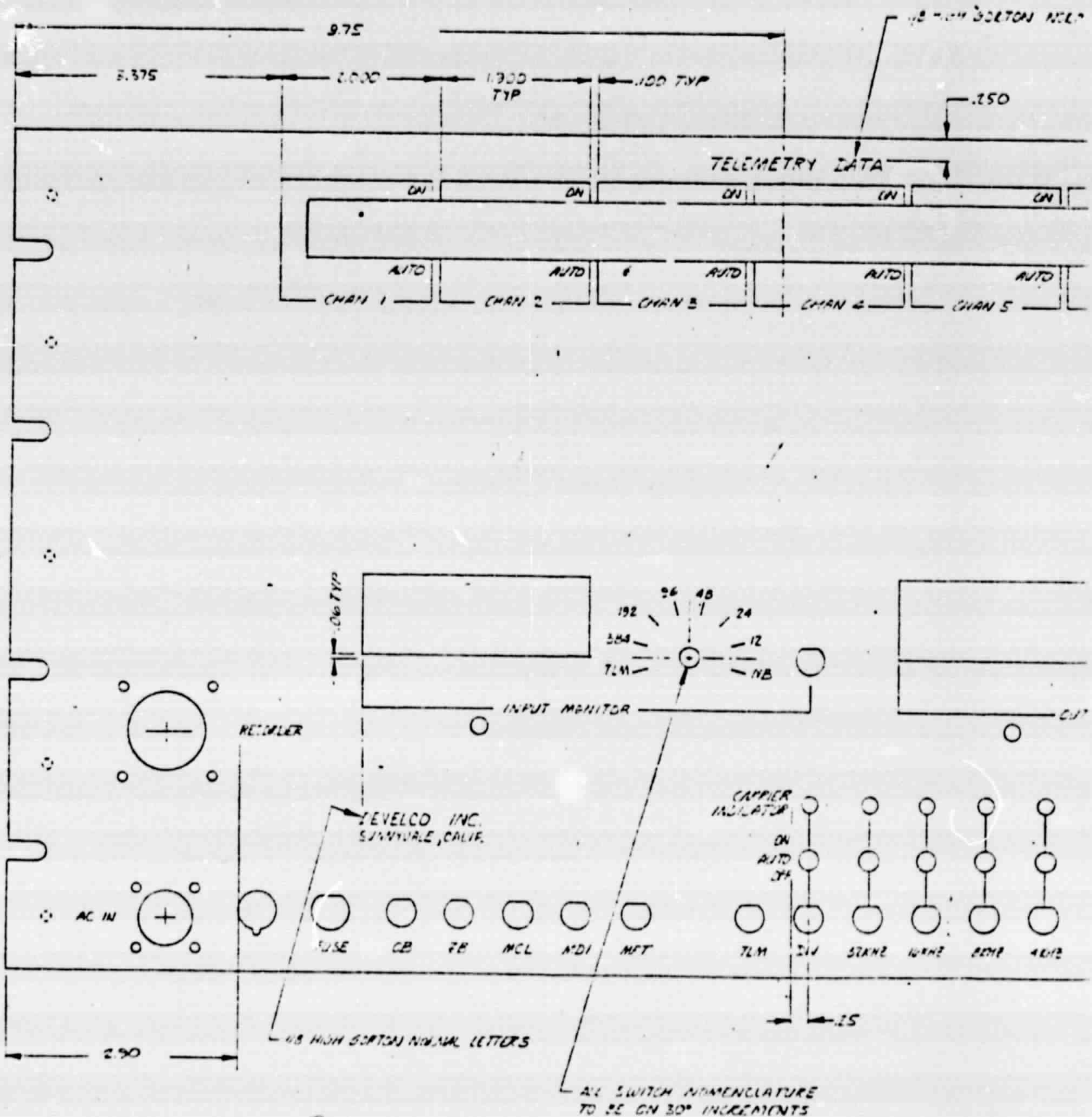
SIGN OFF	INITIALS	DATE
DRAWN	[illegible]	[illegible]
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

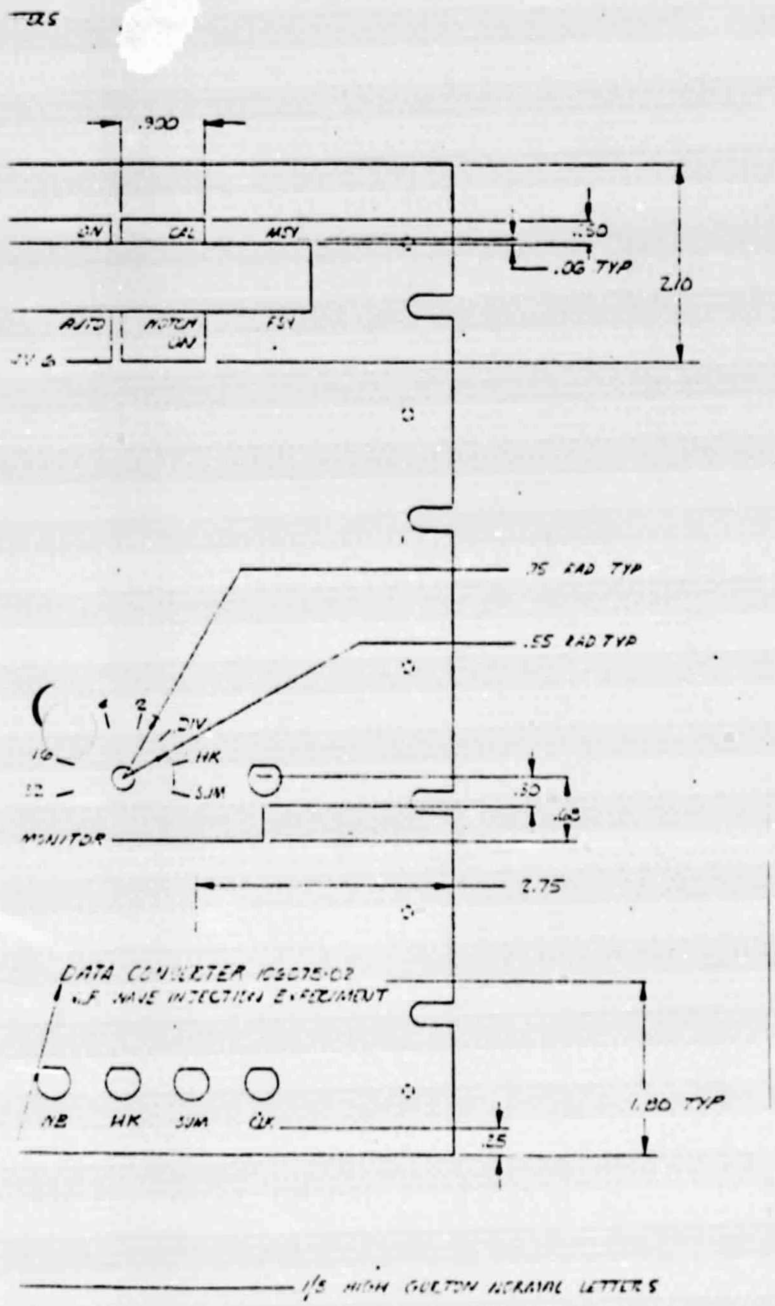
TITLE: MEM DATA MONITOR DECODER & DISPLAY/MULTIPLEXER

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	6-102-037	

SCALE | DO NOT SCALE DRAWING | SHEET [illegible] OF [illegible]


9.75
3.375
2.000
1.900 TYP
.100 TYP
.250
TELEMETRY DATA
ON
AUTO
CHAN 1
CHAN 2
CHAN 3
CHAN 4
CHAN 5
192
96
48
24
12
384
TLM
NB
INPUT MONITOR
RECORDER
DEVELCO INC.
SUNNYVALE, CALIF.
CARRIER INDICATOR
AC IN
FUSE
CB
MCL
MFT
TLM
.25
2.90
.48 HIGH GORTON NORMAL LETTERS
ALL SWITCH NOMENCLATURE TO BE ON 30° INCREMENTS

REVISIONS						
SYM	DATE	DESCRIPTION	DRN	CKD	APPR	DATE
A	[illegible]	[illegible] CHANGES	[illegible]			
B	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]



NOTES (UNLESS OTHERWISE SPECIFIED)

1. PANEL COLOR REF SHEET 1 THIS DWG.
2. ALL CHARACTERS TO BE .[illegible] HIGH GORTON NORMAL. ALL [illegible] CENTERED ABOUT [illegible] AS SHOWN. ALL VERTICAL & HORIZONTAL LINES TO BE .[illegible] WIDE
3. WHITE EPOXY FILL ALL CHARACTERS, EXCEPT DEVELCO INC. [illegible], CALIF. TO BE RED.

	106075-02	
USED ON	NEXT ASSY	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED	[illegible]	
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

DEVELCO INC.

TITLE: FRONT PANEL ENGRAVING DATA CONVERTER

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	[illegible]	B

SCALE — DO NOT SCALE DRAWING — SHEET [illegible]

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. N 01	02
1	106075	DATA CONVERTER ASSY (LAYOUT)	C1		R	R
	106073	FRONT PANEL	D3		1	—
3	106074	FRONT PANEL	D3		—	1
4	106076-01	SIDE SUPPORT	C3		1	1
5	106076-02	SIDE SUPPORT	C3		1	1
6	106077	COVERS TOP & BOTTOM	C3		2	2
7	106078	SUPPORT PWR SUPPLY	C3		1	1
8	106079	REAR COVER	C3		1	1
9	106080	CARD STOP	B3		1	1
10	106081	CARD STOP	B3		1	1
11	106114-2	ENGRAVING DWG - BOX	C3		1	—
12	106082-01	DISPLAY P.C. B.D ASSY	PL		1	—
13		BOX ZERO SR409916	—		1	1
14		SUPPORT BAR SAE 1025	—		6	6
15		CONN. FOOT SAE 2422	—		30	30
16		CARD GUIDE SAE 1650	—		30	30
17		LOCKING TAB SAE 3000	—		90	90
18		P.C. CONN 22/44 .156 SPACE				
19		W.W. SAE SAW22/D3-2	—		11	11
20		P.C. CONN 28/59 .125 SPACE				
21		W.W. SAE CPH3100-56	—		2	2
22	106083	METER BRACKET	B3		2	2
23		CONN, BENDIX PT02A18-32S		J1		
24		ALT # MS3112E18-32S	—		1	—
25		CONN. BENDIX PT02A(SR)18-32P		P1		
26		ALT # MS3116E(SR) 18-32P	—		1	—
27		CONN BENDIX PT02A14-19P		J3		
28		ALT # MS3112E14-19P	—		1	—
29		CONN BENDIX PT06A(SR)14-19S		P3		
30		ALT # MS3116E (SR) 14-19S	—		1	—
31		CONN BENDIX PT02A16-26S		J2		
32		ALT # MS3112E16-26S	—		1	1
33	106114-1	ENGRAVING DWG - BOX	C3		—	1

REV. A — ITEM 72 PN WAS 103395

NEXT ASS'Y

USED ON

BY MGM 12-18-5 CK. [illegible]

APR. [illegible] 1/4/76 APR.

TITLE DATA CONVERTER STANFORD

PARTS LIST NUMBER P/L 106075 REV A

SHEET 1 OF 3

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	01	02				
34		CONN BENDIX PT06A(SR)16-26 P		P2						
		ALT = MS3116E (SR) 16-26 P	–		1	1				
36		CONN MS3102E10SL-3P	–	J4	1	1				
37		CONN MS3106E10SL-3S	–	P4	1	1				
38		KNOB ALCO KNS701BA-1/4	–		2	–				
39		PWR SUPPLY LAMBDA # LZS-30	–		1	1				
40		PWR SUPPLY LAMBDA # LZS-33	–		1	1				
41		PWR SUPPLY LAMBDA # LZD-22	–		1	1				
42		OVERVOLTAGE PROT. LAMBDA # L12-OV6	–		1	1				
43		" " " L12-OV-12	–		1	1				
44		" " " L12-OV-23	–		1	1				
45		KNOB ALCO KNS701BA-1/8	–		2	2				
46		METER MODUTEC T2-W3-DUA-1H1	–		2	2				
47		SWITCH ROT. CENTRLAB PS107	–		2	2				
48		PWR SWITCH DIALIGHT 513-M01-604	–		1	1				
49		LENS - DIALIGHT 186-5071								
50		MOD TO 105991	B3		1	1				
51		LAMP T-1 3/4, 5V DIALIGHT 7332	–		1	1				
52		FUSE HOLDER LITTLEFUSE # 342014	–		1	1				
53		FUSE, SLO BLO 1 AMP	–		1	1				
54		BNC CONN UG-1094AU	–		18	18				
55		SWITCH PUSH-BUTTON C&K 8221	–		1	–				
56		SWITCH TOGGLE C&K 7101	–		16	–				
57		SW. THUMB WHEEL CHERRY, T20-47A	–		6	–				
58		SW. ROT. CTS T205	–		2	–				
59	4-40 x 3/8	SCREW MACH PAN HD	–		25	25				
60	#4	WASHER LOCK	–		25	25				
61	#4	WASHER FLAT	–		25	25				
62	6-32 x 3/8	SCREW MACH PAN HD	–		36	36				
63	#6	WASHER LOCK	–		46	46				
64	#6	WASHER FLAT	–		46	46				
65	4-40 x 5/32	SCREW, MACH. FLAT HD (BLK)	–		10	10				
66										

REVISIONS

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NEXT ASSY

USED ON

BY AKM 12-13-5 CK. AK/AJ
APR. APR.
TITLE DATA CONVERTER STANFORD

PARTS LIST NUMBER
P/L 106075 REV A
SHEET 2 OF 3

ITEM	PART NUMBER	DESCRIPTION		REFERENCE	QUANTITY/DASH. NO -01	-02				
67		BACKPLANE INTERCONNECT	D5		R	R				
68	105945	ANALOG BLOCK DIAGRAM	B7		R	R				
69		—— PRINTED CIRCUIT BOARDS ——								
70	106037	HEM DATA MONITOR DECODER &								
71		DISPLAY MULTIPLEXER	PL		–	1				
72	105953	GSE CODE TRANSMITTER SIMULATOR			1	–				
73	105896	HEM GSE TELEMETRY LOGIC &								
74		DECODING LOGIC	PL	BD 12	1	–				
75	105894	HEM GSE DISPLAY MUX & DIGITAL								
76		TELEMETRY COMMAND TIMING								
77		LOGIC	PL	BD 11	1	–				
78	105939	SUMMING AMPLIFIER	PL	BD 8	1	1				
79	105940	INPUT BUFFER & CH 6KHZ	PL	BD 1	1	1				
80	105941	DISCRIMINATOR	PL	BD 7	1	1				
81	105942 -01	DISCRIMINATOR	PL	BD 2	1	1				
82	-02		PL	3	1	1				
83	-03		PL	4	1	1				
84	-04		PL	5	1	1				
85	105942 -05	DISCRIMINATOR	PL	BD 6	1	1				
86	105943	METER AMP	PL	BD 10	1	1				
87	105944	DETECTOR & CLOCK GEN	PL	BD 9	1	1				
88										
89	106082-02	DISPLAY P.C. BD ASSY	PL		–	1				
90	105948	HEM GSE BACK PLANE	C6		R	–				
91	105958	HEM GSE BACK PLANE	C6		R					

REV	BY MCM	CK.
	APR.	APR.
	TITLE DATA CONVERTER STANFORD	
	PARTS LIST NUMBER P/L 106075	REV A
	SHEET 3 OF 3	

DEVELCO, INC.

ITEM	PART NUMBER	DESCRIPTION	REFERENCE	QUANTITY/DASH. NO. -1	-2				
1		SCHEMATIC & ASSY DC		R	R				
2	169P44-062	VECTOR BD 17.00 X 4.5		1	1				
3									
4		IC LITRONIX DL10A	A4 A6 A8 A10						
5			A12 A14	6	6				
6		CD4049AE	B2	1	1				
7		SN7447AN	B3	1	1				
8		CD4050AE	B4, B9	2	2				
9		SN7445N	B8	1	1				
10		IC CD4021AE	B1A B2A B3A						
11			B4A B5A	5	—				
12									
13		SOCKET 14 PIN WIRE WRAP		10	10				
14		" 16 PIN " "		25	17				
15									
16		TRANSISTOR 2N2907		8	8				
17		LED LITRONIX PL-2		16	16				
18		RESISTOR 1/4W 5% 1.5K		8	8				
19		120 Ω		8	8				
20		1K		3	3				
21		470 Ω		4	4				
22		RESISTOR 1/4W 5% 10 K		18	—				
23									
24		DIODE 1N4005		1	1				
25	CK05BX105K	CAPACITOR CERAMIC .1		1	1				
26									
27		CABLE RIBBON ANSLEY 171-26	FA9, 11, 13	A/R	A/R				
28		CONN DIP 3M 3406	"	6	6				
29		STRAIN RELIEF 3M 3448-8	"	6	6				
30									
31									
32									
33									

BY MCM — CK.

APR. DN 9/11/7- — APR.

TITLE DISPLAY BOARD, HDM GSE F.P. INTERCONNECT

PARTS LIST NUMBER P/L 106082 — REV —

SHEET 1 OF 1

REV

DEVELCO, INC.

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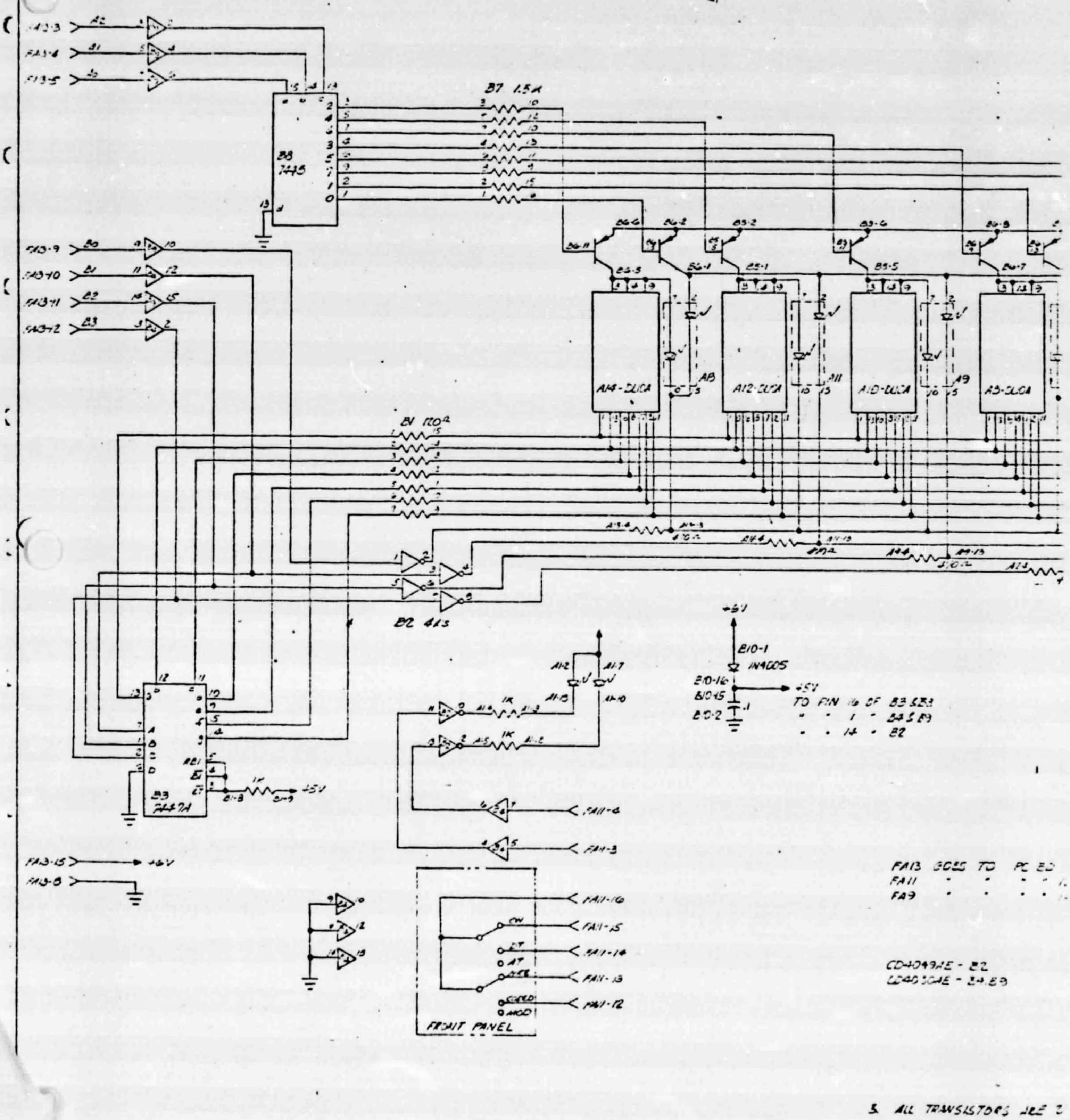
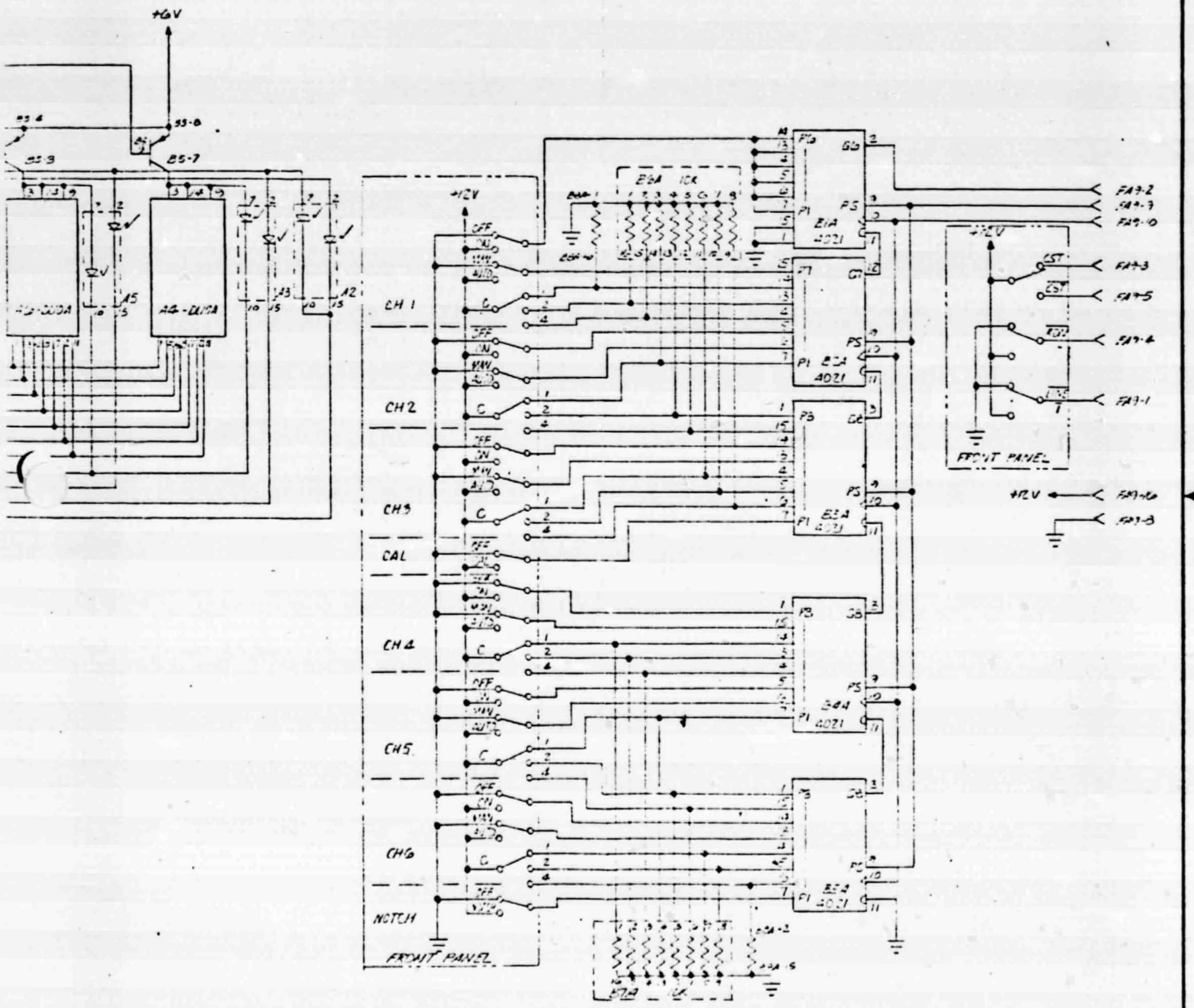


FA13 GOES TO PC BD
FA11 " " " "
FA9 " " " "

CD4049AE - B2
CD4050AE - B4, B9

3. ALL TRANSISTORS ARE 2
2. ALL LEDS ARE LITRONIX F
1. ALL CONNECTIONS TO FRONT WIRED DIRECTLY FROM

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE
B	[illegible]	REDRAWN	[illegible]			



ABOVE CIRCUITRY -01 ONLY

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER	[illegible]	[illegible]
PROJ ENGR		

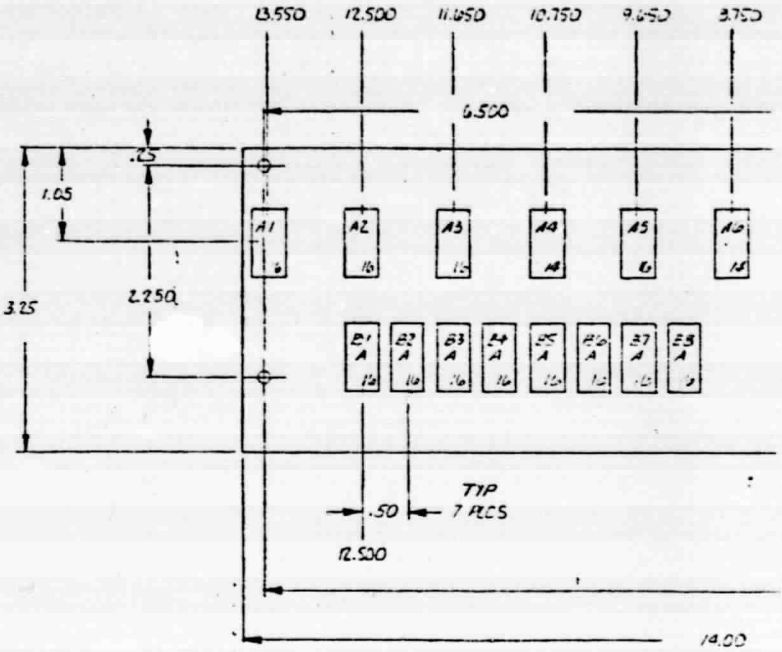
USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

DEVELCO INC.

TITLE: [illegible]RAY BOARD FOR HEM 33E & [illegible]NT PANEL INTERCONNECT

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	6-106062	B

SCALE | DO NOT SCALE DRAWING | SHEET [illegible] OF [illegible]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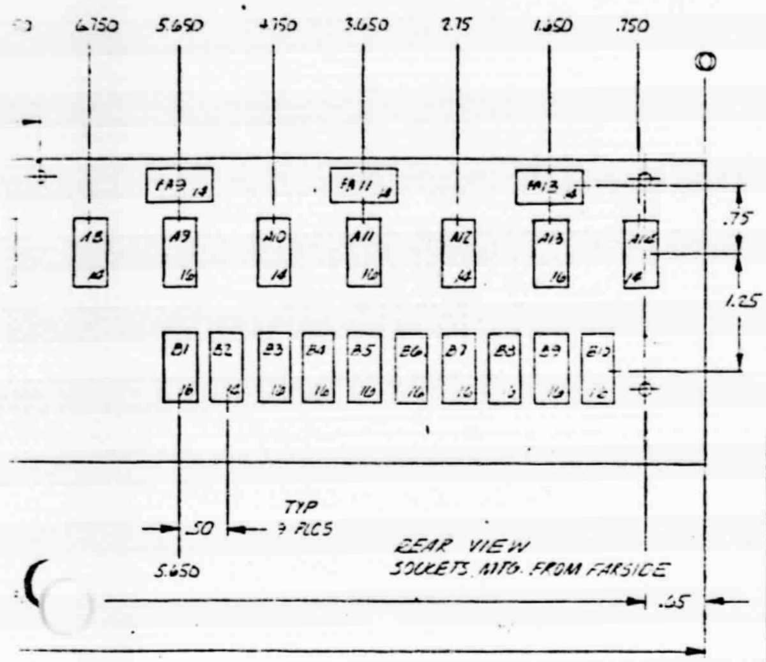
12.500
11.650
10.750
6.500
.25
1.05
3.25
2.250
A1
A2
A3
A4
A5
B1 A
B2 A
B3 A
B4 A
B5 A
B6 A
B7 A
B8 A
TYP
7 PLCS
.50
12.500
14.00

REVISIONS						
SYM	DATE	DESCRIPTION	DRW	CKD	APPR	DATE



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USED ON	NEXT ASS'Y	QTY REQD
APPLICATION		

SIGN OFF	INITIALS	DATE
DRAWN		
CHECKED		
APPROVED		
ENGINEER		
PROJ ENGR		

DEVELCO INC.

TITLE: DISPLAY BOARD FOR NEW USE & FRONT PANEL INTERCONNECT

SIZE	CODE IDENT NO	DRW NO	REV
D	30002	6-106032	3

SCALE | DO NOT SCALE DRAWING | SHEET 2 OF