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IC KU-BAND IMPATT AMPLIFIER

V. Sokolov
M. R. Namordi
F. H. Doerbeck
W. R. Wisseman
Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75265

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GODDARD SPACE FLIGHT CENTER

Greenbelt, Maryland 20771

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SECTION I

INTRODUCTION AND SUMMARY

This report presents the results of work performed under Contract No.
NAS5-24182 to develop a Ku-band Solid State Spacecraft Transmitter. Under a
previous two-year NASA contract, NAS5-20894, a breadboard version of an all-
IMPATT spacecraft transmitter was developed. The accomplishments made during
the earlier program formed part of the technology base for the next phase of
development under the current contract. The principal difference in the
programs under the two contracts is that under Contract NAS5-24182 the center
operating frequency was shifted from 13.525 GHz to 15.085 GHz, and increased
emphasis was placed on transmitter reliability. The program goal was to
achieve an operating lifetime of five years. In response to these new require-
ment goals and to the need for further transmitter performance improvement,
significant changes in both device and circuit design were implemented during
the development of the transmitter amplifier delivered to NASA under the current
contract. These included: (1) implementation of high power, high efficiency, and
high reliability GaAs Schottky-Read IMPATTs; (2) incorporation of a six-stage FET
preamplifier; (3) incorporation of a two-way power combiner in the final power
output stage; and (4) more complete microstrip circuit integration of preamplifier,
driver, and power amplifier chassis, resulting in substantial transmitter size
reduction.

Table 1 shows the performance requirements as specified at the beginning of
the contract. Two of the requirements were later modified with the consent of
the NASA contract monitor. First, the restriction of having the amplifier powered
from an unregulated 28 V power supply was removed, and instead it was decided to
establish the bias requirements during the course of the amplifier development.
Second, OSM connectors rather than waveguide signal connectors were used in the
delivered amplifier.

Key accomplishments and progress made toward the achievement of the performance
goals include the following:

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Table I
Performance Requirements

Center Frequency:	15. 085 GHz
Bandwidth (1 dB):	250 MHz
Bandpass Ripple:	± 0.4 dB max
Gain: (Threshold to - 30 dBm)	63 dB min
(- 20 dBm)	57 dB min
(Rate of Change)	< 0.2 dB/10 MHz
Voltage Available:	28 ± 1 V dc unregulated
Overall Amplifier Efficiency (including power supply interface):	10% min
Intermodulation:	All intermodulation products generated by two - 33 dBm cw signals separated by 10 MHz at any frequency in the pass-band must be no greater than + 18 dBm at the amplifier output when operating in the normal full gain condition.
Operating Temperature Range:	0°C to + 50°C
Operaing Lifetime:	5 years
Spurious Output Radiation:	< - 20 dBm for input signals
	< - 20 dBm or absence thereof
Cooling:	Conducting heat sink only
Total Volume:	1000 cm^3
Signal Connectors:	Waveguide

● Development and fabrication of high power Schottky-Read IMPATTs with low-high-low doping profiles incorporating titanium tungsten barrier metallization in the Schottky junction for high reliability. Output powers of up to 2 W with dc-rf conversion efficiencies of 23% have been obtained for single-mesa diodes operating at 15.7 GHz as free-running oscillators in waveguide. For these devices an extrapolated mean time to failure (MTTF) of greater than 5×10^5 hours (as determined from extensive life testing) is obtained for typical junction operating temperatures of 200°C.

● Development of a six-stage FET preamplifier with a 1 dB gain compression point of 20 dBm and a linear gain of 41 dB at 15 GHz. An output third-order intermodulation intercept point of 25 dBm was achieved with this amplifier.

● Development of a balanced power output stage incorporating two single-mesa IMPATTs yielding an output power of 4.2 W, with 52 dB gain and an intrinsic power-added efficiency (i.e., excluding bias distribution circuits) of 15.7%.

● Delivery of an all-solid-state, 4.1 W, 56 dB gain, 15 GHz amplifier with an overall dc-to-rf efficiency of 10.8%. The amplifier has greater than a 250 MHz 1 dB bandwidth, operates over the 0° to 50°C (base plate) temperature range with less than 0.5 dB change in the power output, weighs 444 grams, and has a volume of 220 cm^3.

Although the 5 W power output goal was not achieved, it is considered that the realization of a 4 W amplifier using proven high reliability, high efficiency GaAs diodes is indeed a significant accomplishment. It demonstrates the development of an essentially laboratory experimental device into one that is feasible for use in an important engineering application.

The remainder of this report is organized as follows. Device design and materials growth are discussed in Section II. Amplifier design and development are covered in Section III. The results of the IMPATT device reliability studies are presented in Section IV. Section V discusses conclusions drawn from the results of the work carried out during the course of the program, as well as recommendations for future work.

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SECTION II

KU-BAND IMPATT DEVELOPMENT

In this section we describe low-high-low GaAs IMPATT device design, GaAs epitaxial growth, the IMPATT fabrication process, the device rf performance in a waveguide cavity, and the device rf performance in microstrip.

A. Device Design

GaAs IMPATTs with low-high-low (LHL) and high-low (HL) impurity profiles have been shown to have the potential for high efficiency operation because of a shortened avalanche region. However, the LHL structure has a lower surface field than the HL structure and therefore a lower field emission (tunneling) current component. Since the field emission current component is not in proper phase relationship with the rf voltage, the LHL structure potentially has higher efficiency than the HL structure. Accordingly, all our efforts in this program were focussed on optimization of the LHL structure.

In the design of LHL Read diodes, three parameters are of primary importance to the device designer: (a) the drift doping, N_D; (b) the charge in the pulse clump, Q; and (c) the distance from the Schottky barrier interface to the pulse clump peak, X_p. Provided the half-width of the pulse clump, X_w, is less than 1/3 X_p, then the physical device can be idealized as shown in Figure 1. Using this model, together with the relationship between the ionization coefficient, α, and electric field, E, it is possible to calculate breakdown voltage, depletion width, and efficiency for the device. A series of nomographs for various N_D, with Q as parameter, has been constructed; a typical example is shown in Figure 2.

These nomographs are calculated using the following material parameters:

(a) GaAs dielectric constant, ϵ_r = 12.4   (Reference 1)

Actual

Idealized

Log N

Q

$X_w \leq 500$ Å

N_D

x

$-X_p$ 0 W_D x

E

$\alpha = A\epsilon^{-(b/E)^2}$

	27°C	200°C
A, μ^{-1}	16	20.7
b, V/μ	55.5	66.4

E_m

$\alpha X_p = 1 \rightarrow E = \dfrac{b}{\sqrt{\ln A X_p}}$
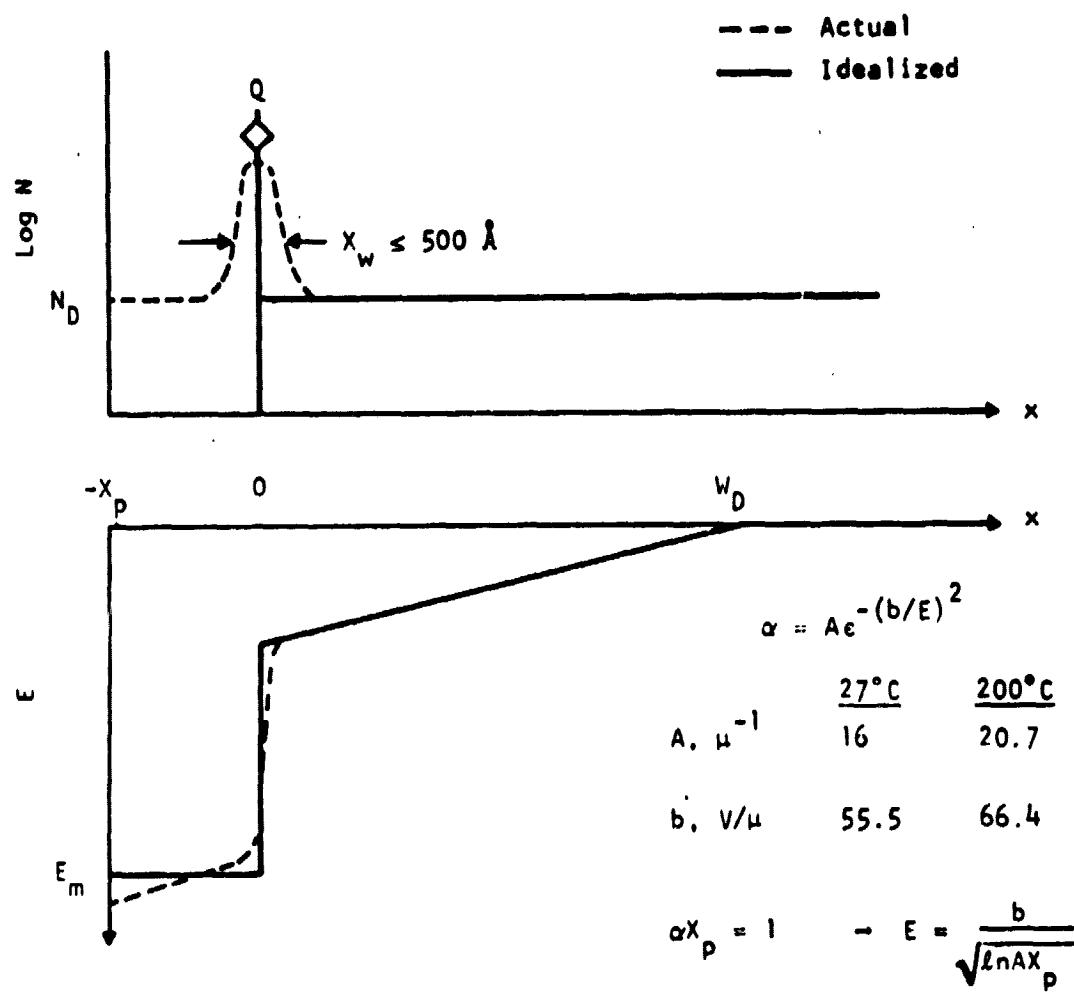
Figure 1 Idealized Low-High-Low Structure
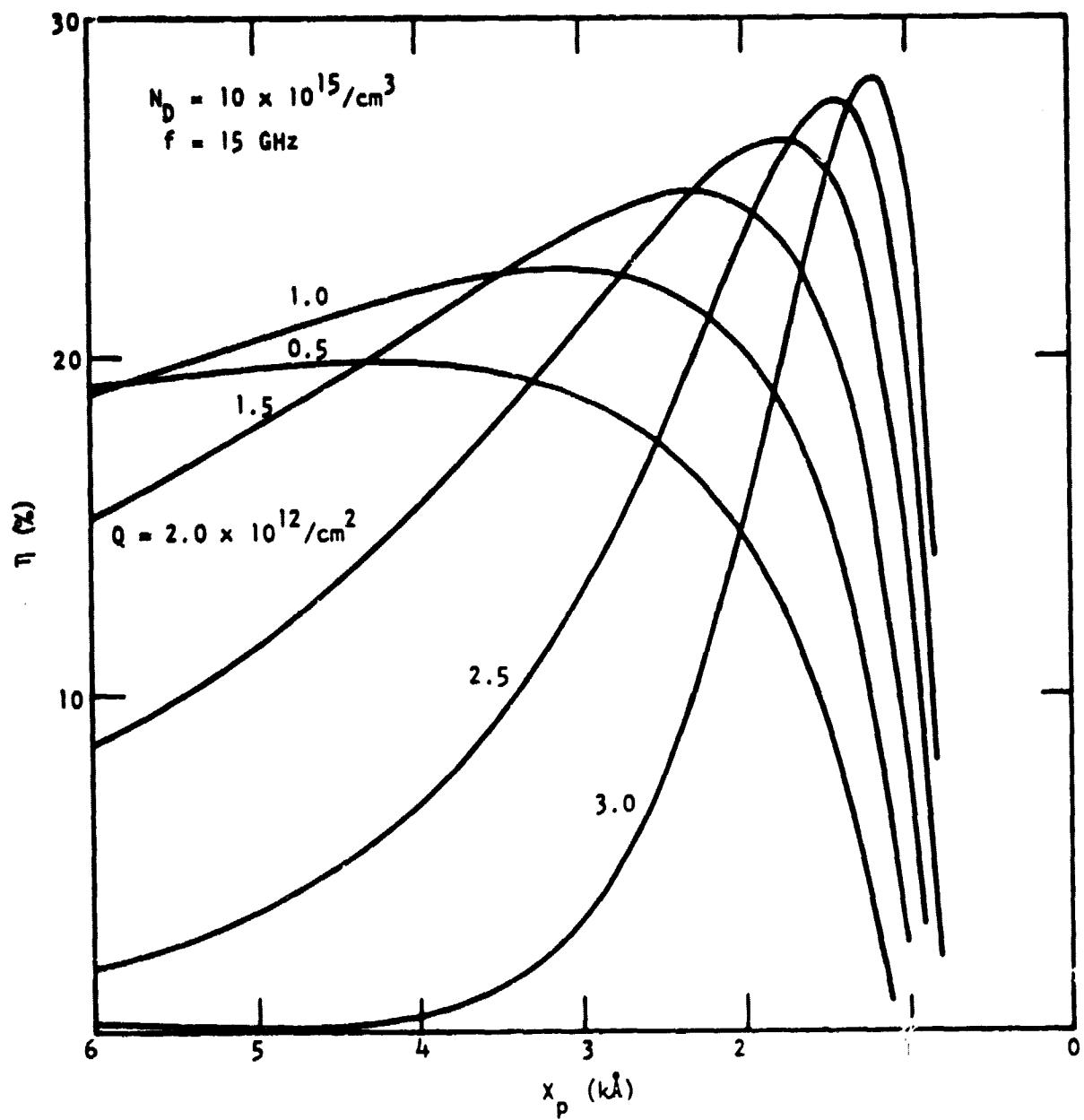
Figure 2 Calculated Intrinsic Efficiency of GaAs LHL Using
Idealized Structure

(b) Saturated drift velocity at 200°C,

$v_o = 6.88 \times 10^6$ cm/sec   (Reference 2)

(c) $\int_{-X_p}^{0} \alpha \, dx = 1$

(d) $\alpha = AE^{-(b/E)^2}$ (Reference 3)

where the values for A and b employed are shown in Figure 1.

(e) The efficiency, η, is computed by the equation

$$\eta = \frac{1}{\pi} \frac{V_d}{V_a + V_d} \frac{\sin\left[(\pi/2)\,(W_D/W_{D\,opt})\right]}{W_D/W_{D\,opt}} , \qquad (1)$$

where V_d is the voltage across the drift region,

V_a is the voltage across the avalanche region,

$W_{D\,opt} = \dfrac{v_o}{2f}$,

and f is the frequency.

This equation reduces to Read's equation[4] when $W_D = W_{D\,opt}$. The sin term in the numerator results from the Fourier series analysis of a rectangular pulse train when the pulse width is varied; the term in the denominator results from dc current considerations. Further, as is conventional, Equation (1) assumes 50% voltage modulation.

Associated with each curve in Figure 2 is a value of X_p, $X_{p\,opt}$, at which the efficiency is a maximum, η_{max}. These nomographs are then used to generate a plot of η_{max} vs Q with N_D as a parameter, from which Figure 3 is obtained. This figure identifies the appropriate range of values for N_D and Q for high efficiency operation.

Two additional constraints must be imposed: (a) the maximum field must not exceed ~ 70 V/μm in order to avoid a significant tunneling current component.

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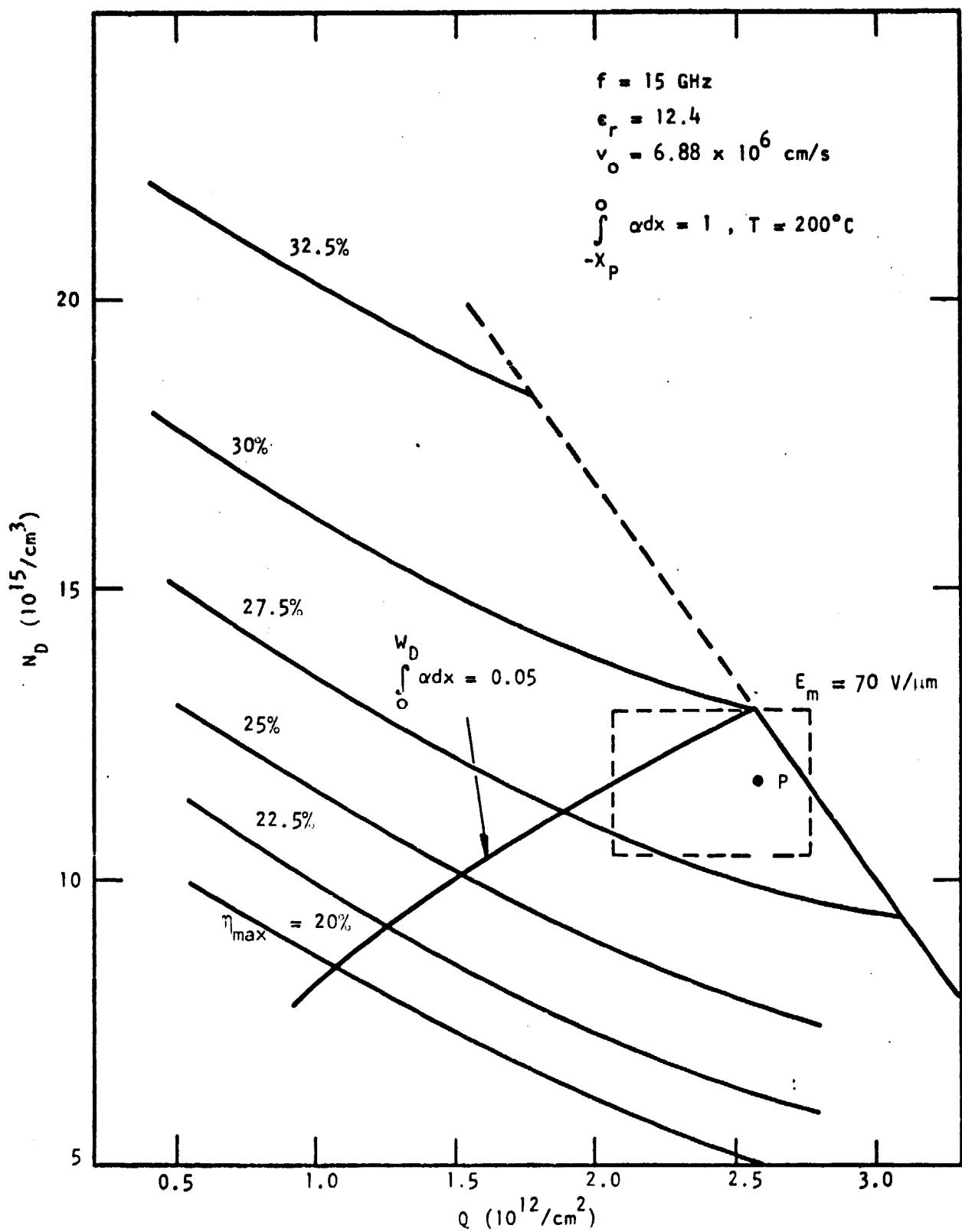
Figure 3 η_{max} Dependence on Q and N_D when $X_P = X_{P\ opt}$

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This defines the right-hand bound of the design window. (b) The ionization integral in the drift space must be < 5%. Accordingly, the left-hand bound of the design window is defined by

$$\int_0^{W_D} \alpha \, dx = 0.05.$$

If point P is defined as N_D (P) = 0.9 N_D apex, then the optimum Ku-band window results as:

$$N_D = 11.6 \times 10^{15}/cm^3 \pm 10\%$$

$$Q = 2.57 \times 10^{12}/cm^2 \, {}^{+ \, 7\%}_{- \, 20\%}$$

It should be noted that this window is essentially unchanged under any reasonable choice of saturation drift velocity, length of drift space, and/or ionization integral value over the avalance zone. In fact, any reasonable choice will result in a change in point P which is < ±3% on Q and < ±5.5% on N_D. The only parameter that significantly affects the location of the window is ϵ_r = 10.9; this value of ϵ_r will reduce both N_D and Q by ~ 13% over that depicted in Figure 3.

Three further observations with respect to Figure 3 should be made. First, the figure should be viewed as a three-dimensional plot. Its shape is that of a steep hill whose gradient decreases as the left and right boundaries are approached; the gradient becomes negative somewhere in the vicinity of these boundaries and is probably followed by a relatively steep drop. Second, the efficiencies shown are intrinsic device efficiencies that would be observed only in loss-less systems. Consideration of skin depth, operating voltage and current, cavity dimensions, and the reactive energy circulating in the cavity indicate that cavity losses vary between $f^{5/2}$ and $f^{7/2}$. The observed efficiency, η_o, is

$$\eta_o = \eta_{intrinsic} \, (1 - K_c) \quad ,$$

where K_c is the percent cavity loss (expressed in decimal units). Using low limit estimates of K_c of 0.015 - 0.025 at 10 GHz, K_c values of 0.060 to 0.165 are obtained at 15 GHz. These two items considered together therefore imply that the maximum observable efficiency possible in the Ku-band will be in the 23 to 26% range. Finally, the values of $X_{p\ opt}$ and $\Delta X_{p\ opt}$ (defined as the allowable variation in $X_{p\ opt}$ wherein the intrinsic efficiency is reduced by 1%) for the indicated design window are:

Upper right-hand corner		Lower left-hand corner	
$X_{p\ opt}$	1150 Å		1700 Å
$\Delta X_{p\ opt}$	±160 Å		±330 Å

It is the achievement of $X_{p\ opt}$ to within the tight tolerance required that makes this device particularly difficult to fabricate.

To confirm the validity of our GaAs LHL IMPATT model, the maximum efficiency achieved from various slices is superimposed on the design window as shown in Figure 4. These results are for slices processed since June 1977 for which X_p is close to its optimum value. Even though there are uncertainties associated with the profiler measurements, variation of material parameters across the slice, and waveguide circuit optimization, it is clear that the experimental results indicate the model is of reasonable utility for LHL IMPATT design.

B. GaAs Epitaxial Growth

The GaAs Read structures were grown by vapor phase epitaxy, using the well-established $Ga-AsCl_3-H_2$ process. Microwave device material is routinely produced by this technique at Texas Instruments. From the start of this program, the emphasis was placed on growing high-low-high structures having material parameters defined by the window described in Section II.A. Figure 5 shows the reactor system.

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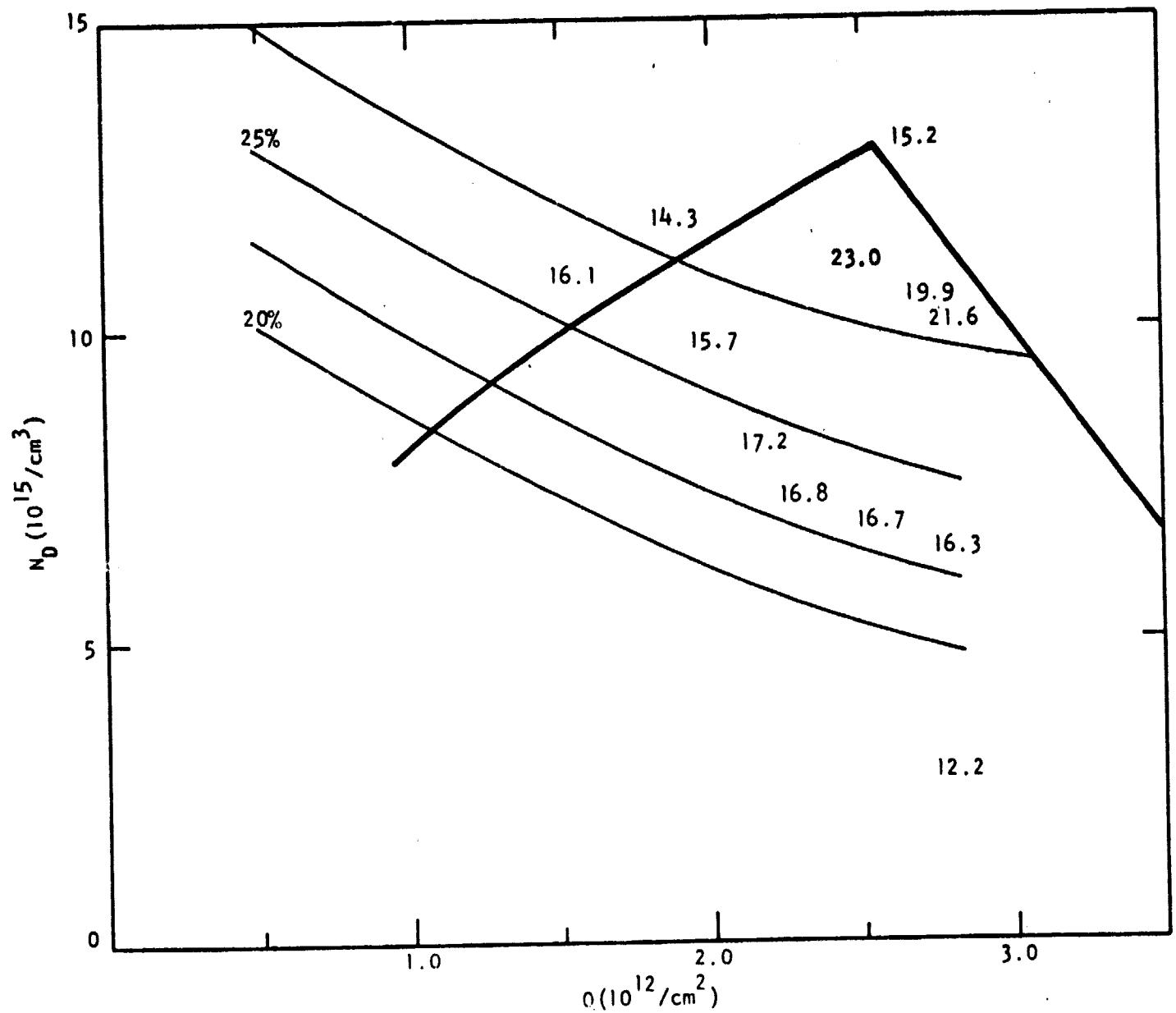
Figure 4   Maximum Efficiency Achieved from Various Slices

Figure 5 Epitaxial Growth System with Sliding Substrate Reactor

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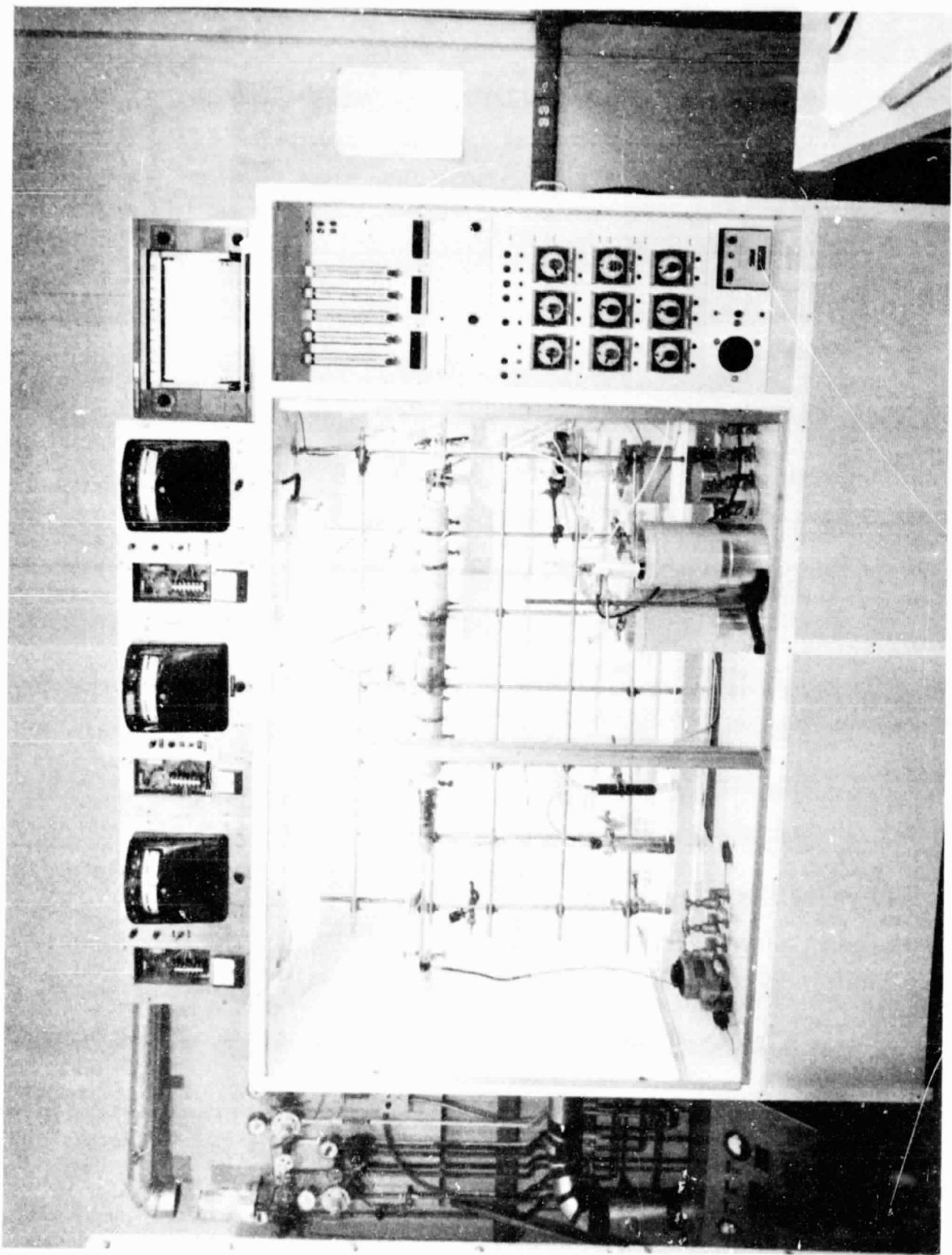
Because of the toxicity of the arsenic compounds, the reactor is mounted in a well-ventilated hood. The gas flow and the temperature cycles are controlled by electric clocks. Details of the reactor design are depicted in Figure 6.

The horizontal reactor exhibits two growth zones. In the upstream growth zone the doping concentration is controlled by the doping gas concentration entering the zone via the n^- dopant inlet. Higher carrier concentration is obtained in the downstream growth zone which is controlled via the n^+ dopant inlet.

The LHL material requirements call for the following structure, starting from a high quality, high conductivity GaAs substrate:

- Buffer layer: doped 5×10^{17} to 10^{18} cm^{-3}, about 5 μm thick

- Drift layer, doped 7×10^{16} to 1.3×10^{17} cm^{-3}, 2.5 μm to 4.0 μm thick.

- A doping pulse with a halfwidth < 500 Å, containing a charge of 2.0 to $2.6 \times 10^{12}/cm^2$. Good device performance was cbtained with doping pulses having a peak doping of 5×10^{17} cm^{-3} and a halfwidth of 300 Å.

- A surface layer, greater than 1500 Å thick, with the same doping level as the drift layer.

A complete doping profile is presented in the next section (Figure 8).

To extend the capabilities of the epitaxial growth system to pulse doping, an additional doping line had to be incorporated. With the help of a gas injection valve, such as that used for gas chromatography, a small volume, 0.5 cc, of high
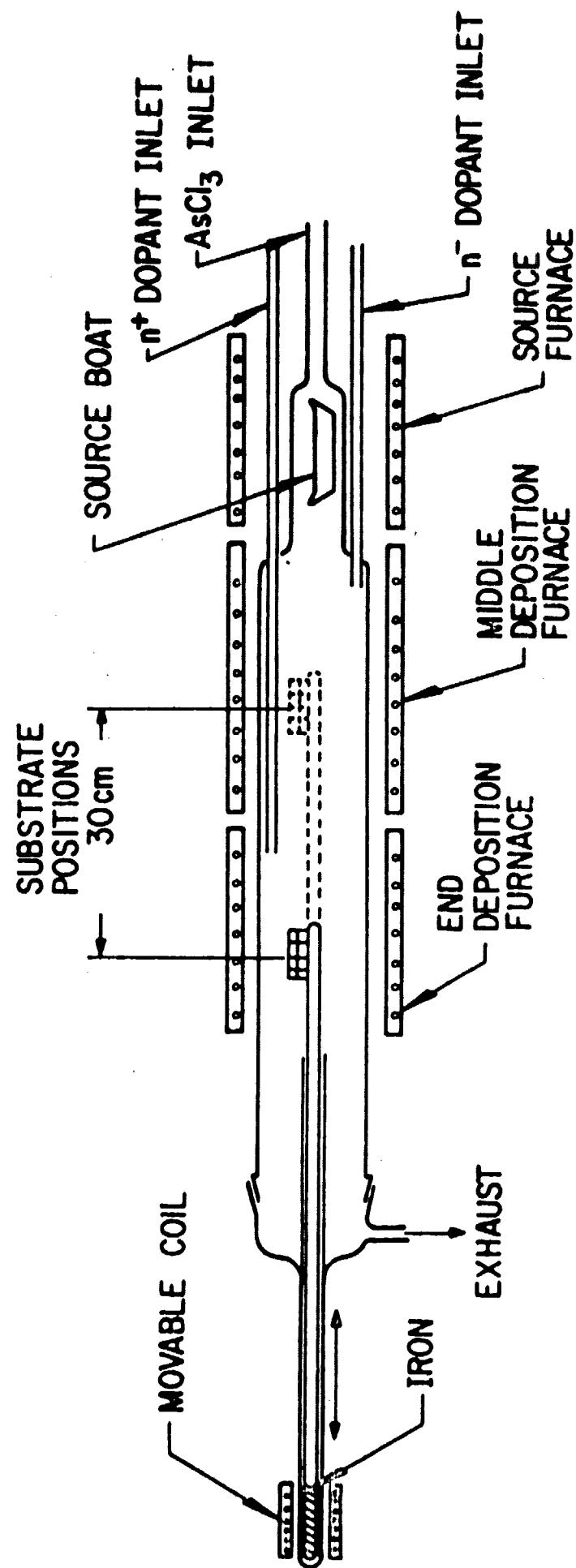
Figure 6 Schematic Diagram of Sliding Substrate, Abrupt Junction Epitaxial Reactor

concentration doping gas can be injected into the gas that enters the reactor through the n^- dopant line. The growth sequence for the complete LHL structure was then as follows:

(1) Growth of the buffer layer in the downstream n^+ zone.

(2) Moving of the slice into the n^- zone and growth of the drift layer.

(3) Injection of doping pulse.

(4) Continuation of growth until desired n^- surface layer thickness was achieved.

Evaluation of the grown epitaxial structures included thickness measurements by cleaving, staining, microscopic examination of the cross section, and C-V profiling after application of gold Schottky barriers.

C. Device Fabrication Process

The fabrication process flow chart is shown in Figure 7. In brief, it consists of three parts. First, the material is characterized to determine whether its parameters are such that high efficiency devices can reasonably be expected. Second, the slice is processed to determine whether Q, N_D, and X_p are of sufficient uniformity. Finally, the slices that pass all acceptance criteria are processed to completion.

1. Test Slice Characterization

A ~ 3 x 20 mm test slice is cleaved off the ~ 13 x 20 mm wafer for slice characterization. This test slice is always cleaved off the wafer from the bottom (referring the slice orientation during VPE growth); experience has shown that this piece accurately reflects the material parameters of the slice committed to device fabrication. The test slice is step-etched so that the first two steps etch into the substrate and buffer, respectively; the last steps, 10 to

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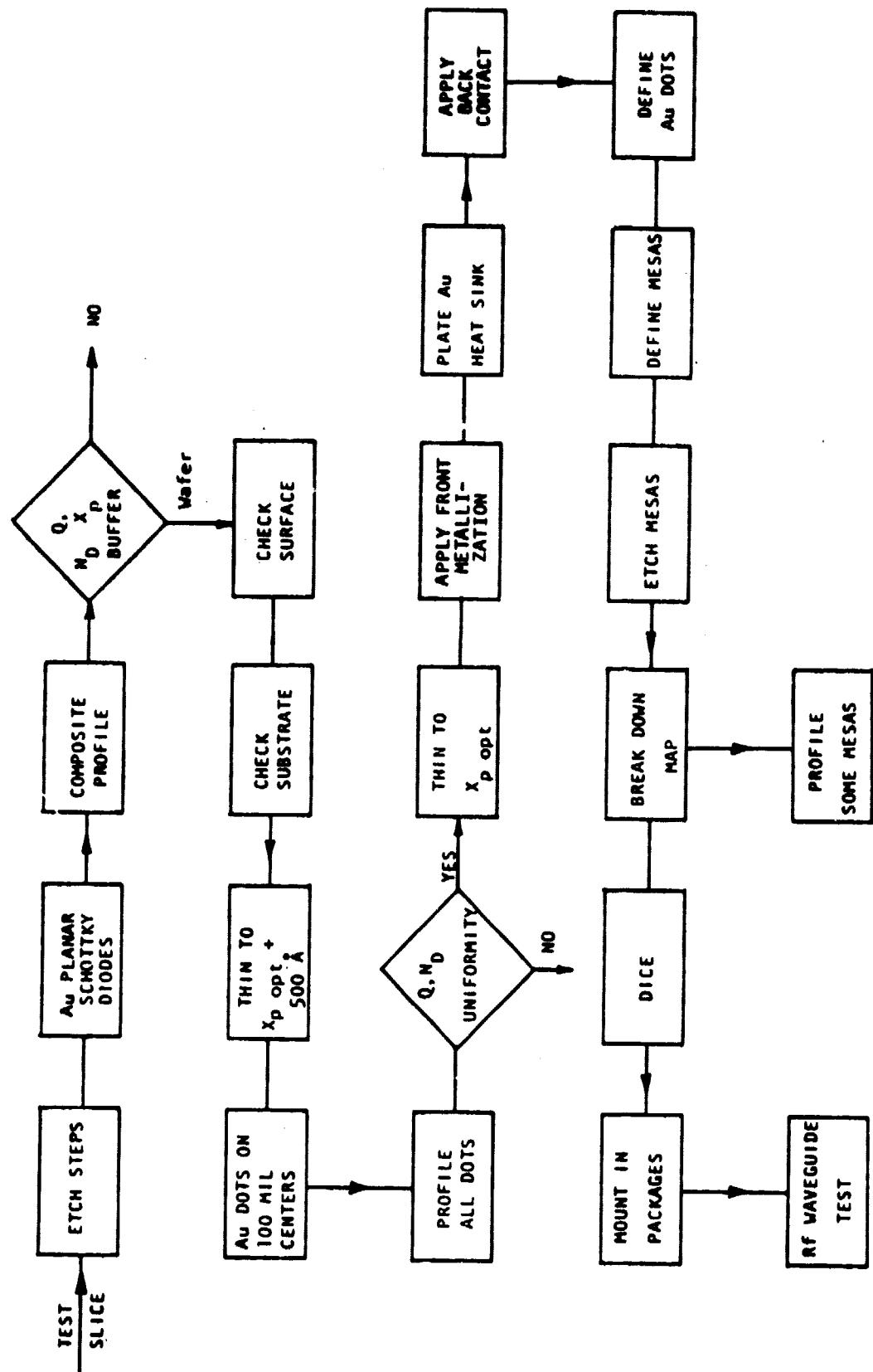
Figure 7 Low-High-Low IMPATT Device Fabrication Flow Chart

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15 in number, successively remove 500 to 1000 Å from the surface. Circular Au planar Schottky diodes are formed on the step-etched surface via standard photolithography and electroplating, together with a uniform Au contact layer on the back surface. The profile is then obtained with an analog impurity profiler. A typical example is shown in Figure 8. This profile is a composite obtained from information from many diodes on the test slice.

To ensure accuracy in the material characterization, a second operator obtains further data from the test slice. These data consist of determining (a) the accurate value of X_p, (b) the maximum value of the X_p that permits profiling over the clump and into the drift region,[*] (c) the value of Q measured for a number of diodes, and (d) the slope of N_D so that the effective drift doping can be ascertained.[†]

Our estimates of Q, effective N_D, and X_p are determined from these data. Calibration of our analog impurity profiler against a digital profiler indicates an accuracy of ±15%. In addition, experience has shown that a typical good slice will exhibit the following variations over its area:

$$N_d \pm 10\%, \quad Q \pm 10\%, \quad X_p \pm 300 \text{ Å} .$$

These uncertainties make it difficult to precisely ascertain material parameters. Consequently, all slices that have parameters within ±30% of point P, as defined in Figure 3, are accepted for further processing; about 15% of the slices grown fulfill this acceptance criterion.

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[*] This is usually a reliable indicator of the quality of a slice; good device performance has frequently been obtained when this value is in the 1500 to 2400 Å range, provided that N_D is near its optimum value.

[†] Typically, the drift doping increases toward the buffer with a slope of 10 to 50% per micrometer. Sufficient data are not available at present to correlate device performance and N_D slope.
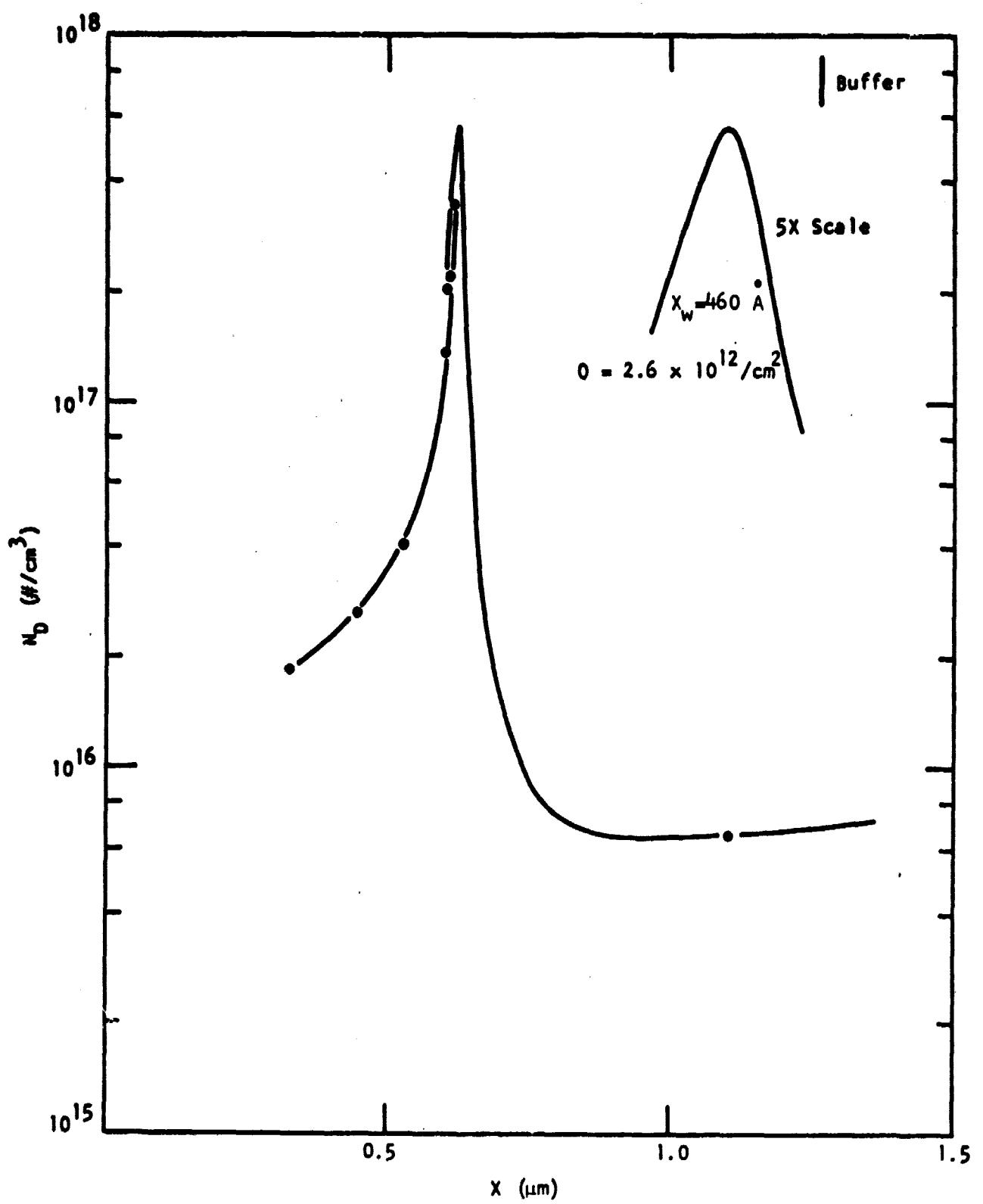
Figure 8 Composite Profile Obtained from Step-Etched Test Slice

2. Slice Uniformity Characterization

This procedure is employed to determine material parameter uniformity across the slice and to thin the wafer to the vicinity of $X_{p\ opt}$. In addition, the slice surface and substrate qualities are inspected. Typically, the 1 x 2 cm slice is cleaved in two, with one part held in reserve for use if some processing failure should occur.

a. Surface Quality

The sample is inspected under a microscope. A mirror-like finish with only a few discernible features over 70% of the sample's surface is acceptable. Samples with scaly or haze finishes, or with many pits, are rejected.

The reason for this inspection is clarified by Figure 9, which shows the normalized breakdown voltage as a function of junction curvature. Since Ku-band diodes have $W_D = 2\ \mu m$, a pit with a spherical curvature of 1 μm will have a breakdown of 50% that of the surrounding area. Defects of this type, which are practically unavoidable, can be tolerated provided their aggregate area is < 1% of the total device area. This is because the current-carrying capability of the defects is thermally limited; thus, the out-of-phase current carried by the defects is only a small part ($\sim$ 2%) of the total diode current so that the efficiency of the device is not seriously degraded. The size and number of these defects are manifested by the sharpness or lack of sharpness of the diode's reverse characteristic; obviously, sharp breakdowns are preferable. Experience has shown that when the VPE reactor is leak-free, more than 80% of the slices pass this inspection.

b. Substrate Evaluation

Substrate evaluation is accomplished simply by removing $\sim$ 6 μm from the back surface of the slice and anodically oxidizing the substrate at 40 V while protecting the epitaxial front surface. A uniform purple-colored oxide should result, indicating a substrate with a high doping concentration; otherwise, the slice is rejected. More than 90% of the slices pass this test.

$$V_B \propto \left[(n + 1 + \gamma) \, \gamma^n \right]^{1/n+1} \gamma$$

n = 1 Cylindrical

n = 2 Spherical

Cylindrical

Spherical

$\gamma = r_j / W_D$

Normalized Breakdown
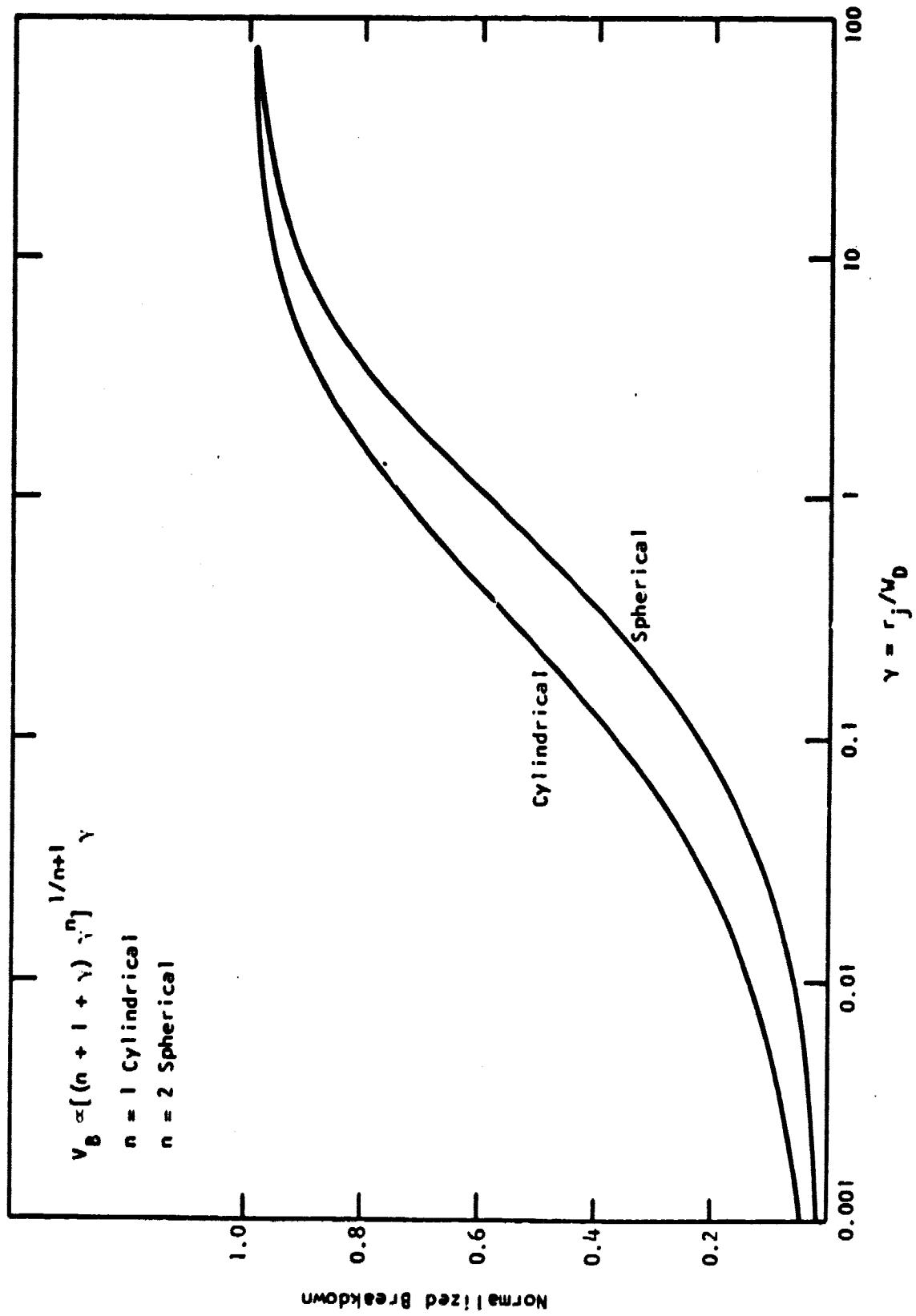
Figure 9 Normalized Breakdown as a Function of Junction Curvature

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c.   Anodic Thinning for Uniformity Evaluation

Using the material parameters obtained from the test slice, a plot of both the breakdown voltage and the efficiency as a function of X_p is generated via a computer. The difference between $X_{p\ opt}$ as obtained from the plot and the measured value of X_p from the test slice determines the amount of thinning required. The thinning is then scheduled to obtain $X_{p\ opt}$ + 500 Å for uniformity evaluation.

Thinning is accomplished by anodic oxidation[5] by alternately growing and stripping the oxide. Careful attention is paid to oxide color uniformity; thinning is terminated before the scheduled point if the oxide becomes nonuniform.

d.   Uniformity Evaluation

Circular planar Au Schottky barrier diodes are formed on 2.54 mm (100 mil) centers on the slice via standard photolithography and electroplating, together with a uniform Au contact layer on the back surface. All diodes of the typically 4 x 4 matrix are profiled to determine both the quality of the test slice data and the uniformity of the material parameters. In most cases (>70%), all the test slice material parameters are confirmed to within ±20%; a new computer efficiency plot is generated to determine $X_{p\ opt}$ using these new material parameters. Variations of material parameters across a typical good slice were noted earlier in Section II.C.1; slices with greater variation are usually processed, provided that high efficiency devices can be expected from >25% of the slice area. About 70% of the slices reaching this stage are committed for final processing.

3.   Final Processing

The Au dots are etched off with a minimum of GaAs removal (estimated as <100 Å). The slice is given a final thinning to obtain $X_p = X_{p\ opt}$ via anodic oxidation. The remainder of the fabrication procedure employs the standard TI

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IMPATT process whose main features are illustrated in Figure 10. After final thinning, a high reliability metallization system is applied to the front (junction) side, consisting of 400 Å ± 100 Å Pt/2250 Å ± 250 Å TiW (90% W by weight)/1000 Å ± 200 Å Pt. The metallization system is serially deposited by sputtering in one pumpdown after a brief sputter etch of the GaAs surface. This metallization system is employed because the reaction of a Pt/GaAs interface is known to proceed fairly rapidly,[6] thereby degrading the reliability and performance of high-efficiency, Read-type, Schottky barrier GaAs IMPATTs. By employing a thin Pt layer for Schottky barrier formation, followed by a barrier layer,[7] the deleterious Pt/GaAs reaction is terminated when the Pt is consumed. The final 1000 Å Pt layer is included to protect the barrier layer from the atmosphere upon exposure.

After front-side metallization, a 0.25 mm (10 mil) thick gold heat sink is electroplated onto the Pt. Next, the substrate is thinned by lapping and etching to ~ 25 μm, and a Au/Ge ohmic back contact is evaporated, followed by an additional 1 to 2 μm of plated Au. After mesa etch, the ohmic contacts are alloyed at 460°C for 1 minute in a He atmosphere. These ohmic back contacts are employed to counteract possible unreliability due to current crowding and thermal runaway. Mesas are then defined and etched using standard lithographic techniques; typical mesa diameters for Ku-band applications are 125 μm. The heat sink is ~ 0.50 mm (20 mils) square after sawing. The final step in device fabrication is lapping of the gold heat sink to a smooth finish that will ensure good wetting of the solder between the heat sink and the bonding pedestal of the package.

Before the slice is diced, a breakdown voltage map of the slice is obtained. A typical map for a slice that exhibited good uniformity during pro-filing is shown in Figure 11. The voltage reading is that obtained at a reverse current of 10 mA; diode spacing is on 0.50 mm (20 mil) centers. A typical breakdown characteristic of a diode from this slice is shown in Figure 12. Such characteristics are frequently obtained from slices with good surfaces.

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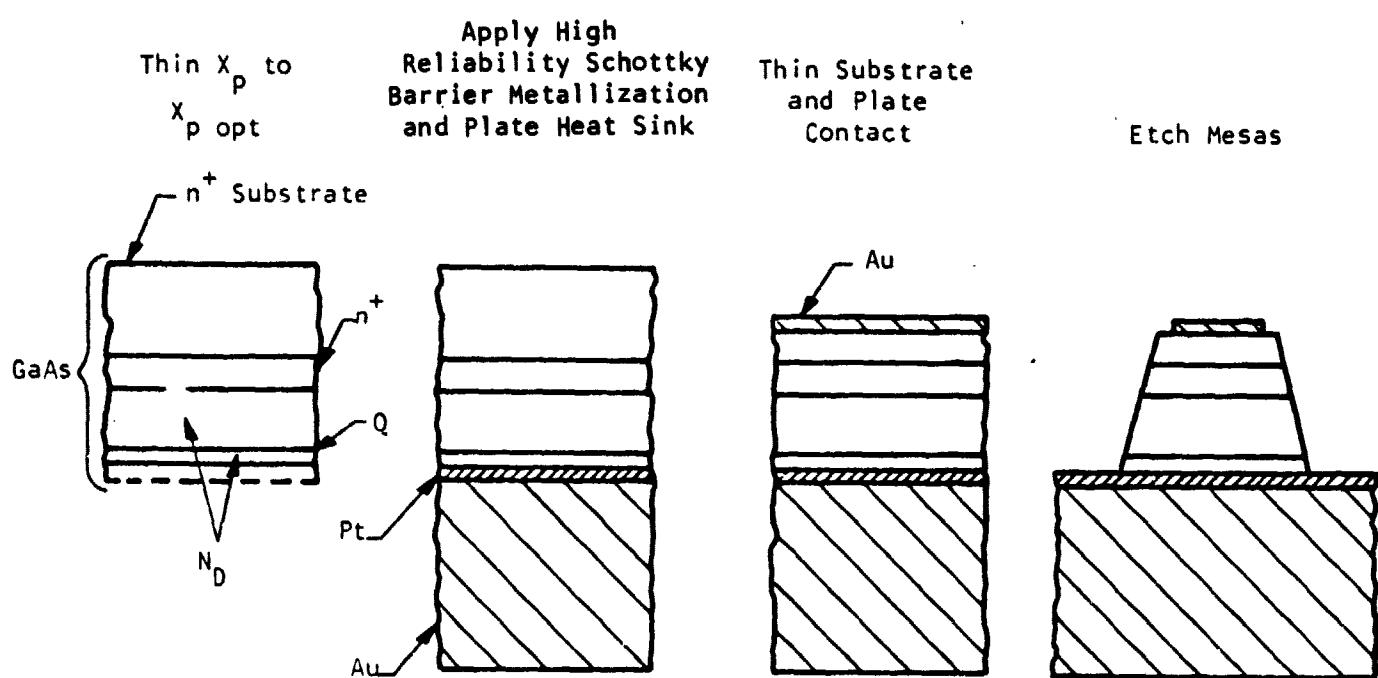
Figure 10   Procedure for Fabricating GaAs Low-High-Low IMPATT Diodes

X	X	21	25	27	27	28	14	X
X	20	24	X	28	27	27	28	28
21	16	25	28	29	25	28	X	28
20	26	30	31	33	34	X	33	34
16	21	26	26	27	27	27	28	27
15	19	22	23	24	25	25	24	23
X	17	19	21	21	22	22	19	20

Figure 11   Voltage Map of a Slice Exhibiting Good Uniformity

Reverse

0

Forward
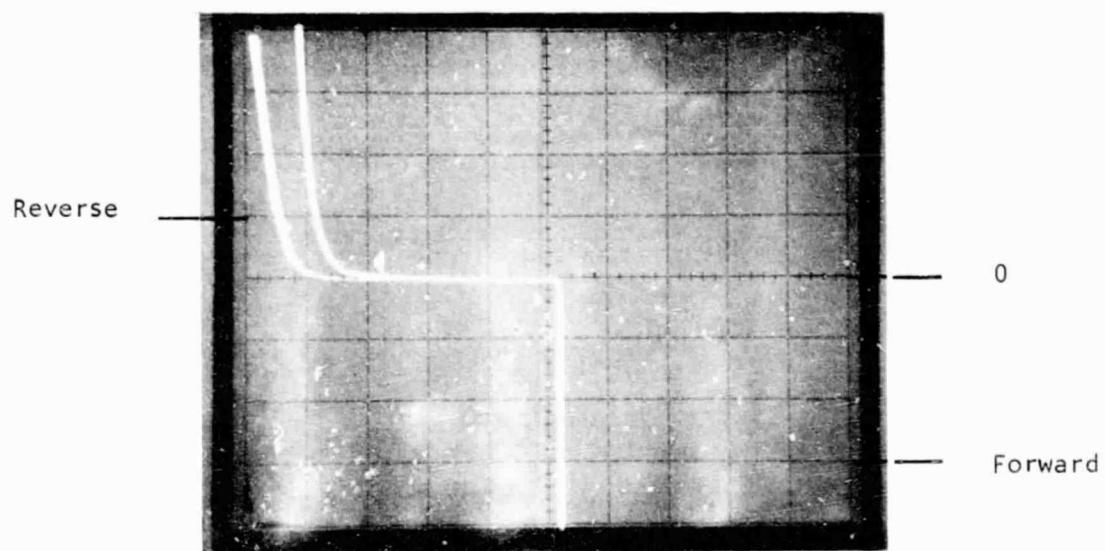
$V = 1$ and 10 mA/div
$H = 5$ V/div

Figure 12 Breakdown Characteristics of a Diode from a Slice with a
Good Surface

Profiling of mesas at this stage met with very limited success. The mask set was designed to create 0.23 mm (9 mil) diameter profiling mesas located on 2 mm (80 mil) centers. (These mesas are located at heat sink edges and are destroyed during dicing.) For profiling, these mesas must be made ohmic. The application of solder at $\sim$ 300°C to these mesas usually makes them leaky so that proper profiling cannot be accomplished. Usually, only information concerning the value of X_p could be obtained.

After dicing, mesas with the proper breakdown voltage are mounted in microwave packages for testing in the waveguide hat circuit. This package is illustrated in Figure 13. Diodes are soldered into the package by flowing a eutectic Au-Sn solder preform onto the package pedestal and placing the heat sink on the wetted solder pool under gentle pressure. The solder is then frozen, and the unit becomes securely bonded to the package. The mesa top is connected to the package flange with a crossed 0.13 mm (5 mil) Au ribbon; wire mesh straps have also been employed. Tailoring of mesa area with a high-speed jet etch can be done with either arrangement.

The yield obtained in final processing is > 80%. Yield losses are generally due to problems encountered during plating, which result in poor interfaces and therefore in devices with high thermal impedance.

D.   Device Waveguide Performance

Packaged diodes are tested in the waveguide hat circuit shown in Figure 14. Bias is supplied from a constant voltage source through a 100 Ω resistor. Bias is increased to 10 mA and the bias voltage recorded; this voltage is referred to as the breakdown voltage. The bias is increased to $\sim$ 150 mA, and the diode is tuned for maximum output power; power, bias, and frequency are recorded. Bias current is then increased in $\sim$ 25 mA increments, and the diode is retuned for maximum power. This process is continued until a maximum in efficiency or power is achieved.
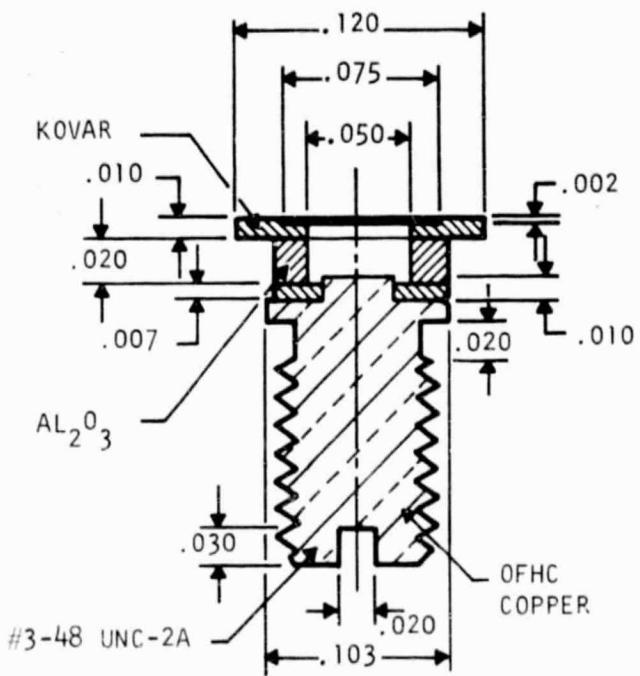
Figure 13   Detail of Package Used for Testing in Waveguide Hat Circuit
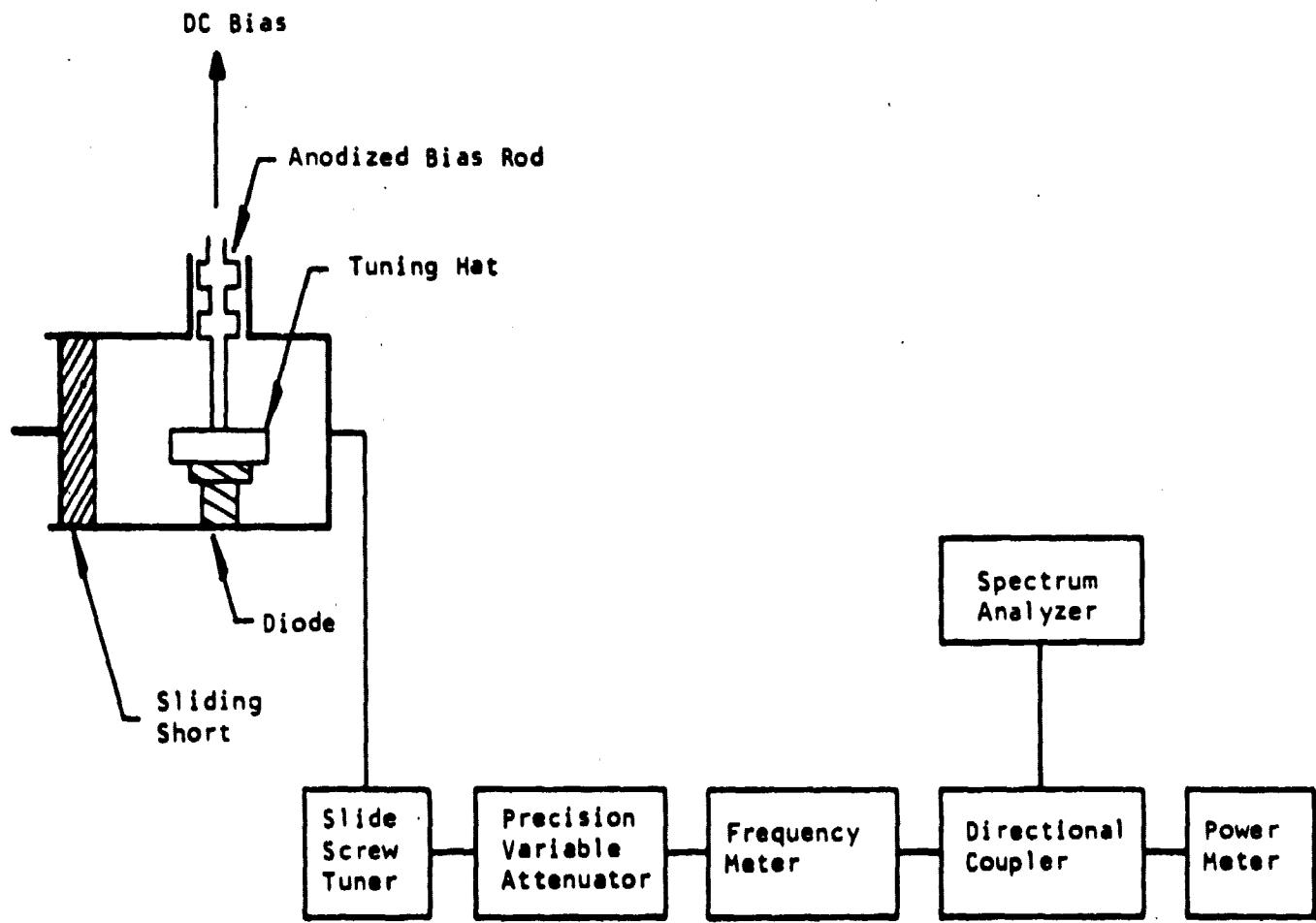
Figure 14 Ku-Band Waveguide Test Circuit

Best performance is obtained from a diode when the diode is held securely in position in the test circuit. This ensures good electrical contact between the package flange and the waveguide hat, as well as forcing intimate contact between the package screw threads and those in the heat sink; this minimizes the parasitics associated with those contacts. Further, the cavity is periodically cleaned and fresh Au electroplated as needed to ensure minimum cavity losses.

The optimum hat and diode position in the waveguide for Ku-band operation is determined by trial and error. Once these parameters are optimized, they are generally not changed; it is assumed that the configuration is near optimum for other LHL Ku-band diodes. The dimensions of the optimum hat for the Ku-band waveguide circuit used in this work are:

> Diameter = 5.08 mm (200 mils)
> Height   = 2.54 mm (100 mils).

Some representative waveguide circuit results for the LHL device lots are presented in Table 2; the rf performance data is that exhibited by the best device from the particular lot. Also included in the table are material parameters and breakdown voltage map reults. Except for the possible mix-up of slices 63 II and 64 II,[*] high confidence is placed in the reliability of these data. The device lots shown represent 60% of the lots that have efficiency > 15%. The other 40% of the device lots processed either failed due to processing errors or were experimental slices (with material parameters considerably removed from the design window) intended to test the validity of the idealized model. These latter slices, as expected, exhibit efficiency < 10%.

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[*] It is highly likely that this mix-up did in fact occur, though proof of this is, of course, not available. Assuming that there was a mix-up, then the rf performance data of 64 II and 63 II should be interchanged.

Table 2

Representative Waveguide Circuit Results

Device Lot	N_D ($10^{15}/cm^3$)	Q ($10^{12}/cm^2$)	x_p Final (Å)	BV Map	η (%)	P_{rf} (W)	f (GHz)	Hardiness	Comments
29 II	8-9	1.7-2.0	1600-2400	17-26	16.7 / 16.3	1.30 / 1.67	14.4 / 14.4	Fair-Poor	Poor surface
49 III	13	1.8-2.3	~1350	24-29	16.0 / 14.5	2.00 / 2.45	15.7 / 15.3	Fair	Leaky breakdown
61 II	~12	2.2	1500-2500	10-21	15.2 / 14.4	1.41 / 1.55	15.6 / 15.6	Fair	Poor slice uniformity
63 II	8-9	2.1-2.3	1500-2100	19-31	17.2 / 16.6	2.00 / 2.50	15.1 / 15.6	Fair	Slice mix-up with 64 II may have occurred
64 II	10-12	3.4	--	24-29	19.9 / 19.7	1.60 / 2.25	15.5 / 15.7	Very Good	
70 II	7-7.5	2.4-2.8	1350-1850	15-21	21.6 / 19.1	1.50 / 1.82	15.7 / 15.7	Poor / Poor	Poor Pt/Au interface, low yield
70 III	9.6	2.3-2.7	1500-1700	19-27	21.0 / 20.4	1.90 / 2.15	15.0 / 15.0	Fair-Good / Fair-Good	High yield. Good slice uniformity
71 II	6.6-8.5	2.0	1750-2250	17-30	18.0	2.60	15.0	Fair-Good	
76 III	6.7	1.6	2400-2700	32-43	16.3 / 15.0	0.82 / 0.93	15.7 / 15.7	Fair-Good	
79 III	7-10	2.1-2.8	2300-2900	14-30	23.0 / 22.0	1.84 / 2.10	15.7 / 15.7	Excellent / Excellent	

Notes: First line corresponds to best efficiency achieved; second to maximum power. Hardiness refers to ability to withstand electrical abuse.

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E.   Device Evaluation and Performance in Microstrip

A conventional waveguide test circuit can be used as the initial step for microwave evaluation of the diodes to be incorporated in a microstrip amplifier circuit. However, to design an optimum amplifier circuit, it is essential to characterize the diode in a microstrip circuit for large-signal operation. The main concerns for high power applications are to achieve the required circuit resistance for an optimum impedance match and the necessary bond lead inductance for the desired operating frequency.

The Read diode is evaluated as a free-running oscillator in a microstrip test fixture. The basic microstrip circuit consists of a 50 Ω transmission line, a 10 pF beam lead capacitor for dc blocking, and a $\lambda/4$ transformer section to reduce the real part of the impedance to ~ 3 Ω at the input to the diode. The microstrip circuit is fabricated on 0.25 mm thick polished alumina and mounted on a gold-plated aluminum block. The diode, which has an integral plated heat sink, is alloyed onto a gold-plated copper block (0.50 x 0.50 x 0.25 cm) and attached to the microstrip circuit block with a small screw. The diode mounting scheme used in the test fixtures is identical to that employed in the final amplifier assemblies. Figure 15 shows the microstrip oscillator test fixture.

For initial evaluation the circuit is tuned only for maximum power from the device as a free-running oscillator (i.e., no rf input). Several microstrip circuits employing transformed impedances ranging from 3 Ω to 11 Ω were investigated. Input impedance levels less than 3 Ω are difficult to produce on 0.25 mm thick alumina because the width of the transforming section becomes greater than the length ($\lambda/4$). It becomes difficult to predict the actual impedance presented to the diode in this situation. For the Ku-band Read diodes tested, the impedance level required for a 0.10 to 0.13 mm diameter mesa is approximately 3 Ω to obtain maximum power output. If two mesas are combined in parallel on a chip, the required impedance presented to the device must be approximately halved (≈ 1.5 Ω). At the 3 Ω level, the microstrip transformer is already a square ($\lambda/4 \times \lambda/4$), and thus a 50-to-1.5 Ω transformer is not easily achievable.

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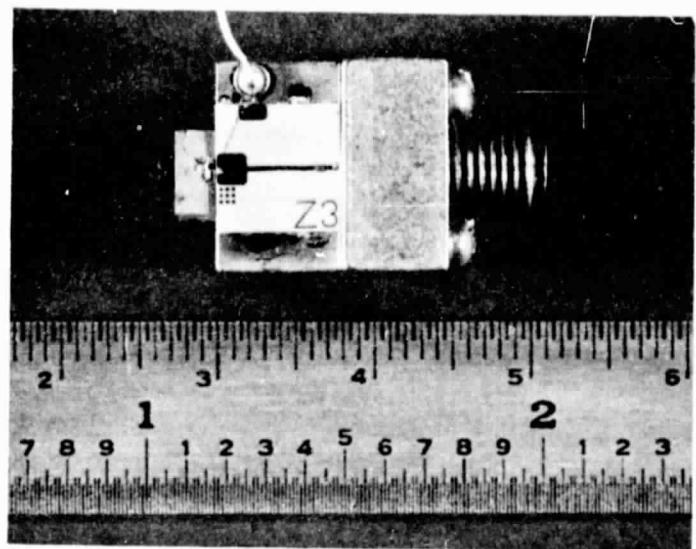
Figure 15 IMPATT Microstrip Oscillator Test Fixture

For high-power performance from a Read diode, one would like to employ as large a mesa as possible. The larger the area, however, the greater the capacitance. This necessarily requires a correspondingly smaller lead inductance to the device to cause it to resonate at the desired frequency. To obtain the optimum condition, the shortest possible 0.13 mm wide gold ribbon is bonded from the microstrip circuit to the diode. The diode is then etched until the desired operating frequency is achieved. Often the diode will require a considerable amount of etching to increase the frequency of oscillation. The lead inductance has been minimized ($\sim$ 0.25 nH), and the diode capacitance must be reduced to achieve the frequency required. In the case of double mesas (parallel combination on a single chip), the individual capacitances add, necessitating an even further reduction in the input inductance or the diode capacitance. Double-mesa operation was found to be difficult to repeat from chip to chip. Many bonding configurations were implemented with the double mesas, with most schemes yielding unpredictable results. The reactive parasitics appeared to predominate.

It was found that to achieve the highest possible output power, either a single-mesa diode with a large junction area or a multiple-mesa with the same total area must be used. The thermal advantage gained by a multiple-mesa approach appeared to be outweighed by the difficulties encountered with lower impedance levels, unpredictable results obtained with various bonding configurations, and local parasitics. From slice 79 III a single-mesa Read diode (0.10 to 0.13 mm) produced 1.8 W at 15.6 GHz as a free-running oscillator in a microstrip test circuit. Efficiency was 23%. Another single mesa delivered 1.4 W at 15.6 GHz with 19% efficiency.

SECTION III
AMPLIFIER DEVELOPMENT

A. General

Figure 16 shows a block diagram of the three main amplifier chassis: the FET preamplifier, the IMPATT driver amplifier, and the IMPATT balanced power stage. The power gain of each stage, as well as the dc input power and corresponding rf power output along the chain of amplifiers, is also indicated. The amplifier operates from 39 V, 6 V, and -1 V commercial dc power supplies. (The -1 voltage is necessary for biasing the FET gates.) All dc power losses due to biasing networks are included in the dc input values shown. The nominal rf input power to the amplifier ranges from threshold (< -30 dBm) to -20 dBm. Below threshold, amplification is no longer needed (as determined by transmitter requirements), and the driver and power amplifiers are made idle by removing bias from the IMPATT diodes. This is accomplished by a detector-activated "squelch" circuit, which monitors the output power level of the FET preamplifier.

Although it is possible to develop stable amplifiers (i.e., stable under zero rf drive) using flat profile IMPATTs, it is not practical to do so with amplifiers employing high efficiency GaAs IMFATTs with low-high-low doping profiles,[9-11] because for these diodes a large increase in negative resistance accompanies reduced rf drive levels. As a consequence, an amplifier tuned for maximum output power at a high input drive level (i.e., the real part of the circuit impedance presented to the diode is low) will oscillate at reduced or zero drive levels (because the magnitude of the diode's negative resistance has increased to a value greater than the real part of the circuit impedance). For this reason, the low-high-low GaAs IMPATTs are much more appropriate for injection-locked oscillator (ILO) operation than for stable amplifier application.[10] Other advantages of the ILO approach include: (1) higher amplifier efficiency due to higher gain (and therefore fewer) ILO stages, (2) easier and faster tuning procedure (more cost effective), and (3) improved overall amplifier gain stability with respect to changes in ambient temperature. This is because the output power

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FET Preamplifier

IMPATT Driver Amplifier

IMPATT Balanced Power Amplifier

IN

-20 dBm

+ 20 dBm

+31 dBm

+36.1 dBm

OUT

Individual Stage Power Gains (dB)

7 7 7 6 6 6 5 5

Dc Input Power

(6v)·(490 mA) = 2.9 W

(39 V)·(357 mA) = 13.9 W

(39 V)·(529 mA) = 20.6 W

Total Dc Input Power : 37.4 W

Total Dc to Rf Efficiency : 10.8 %
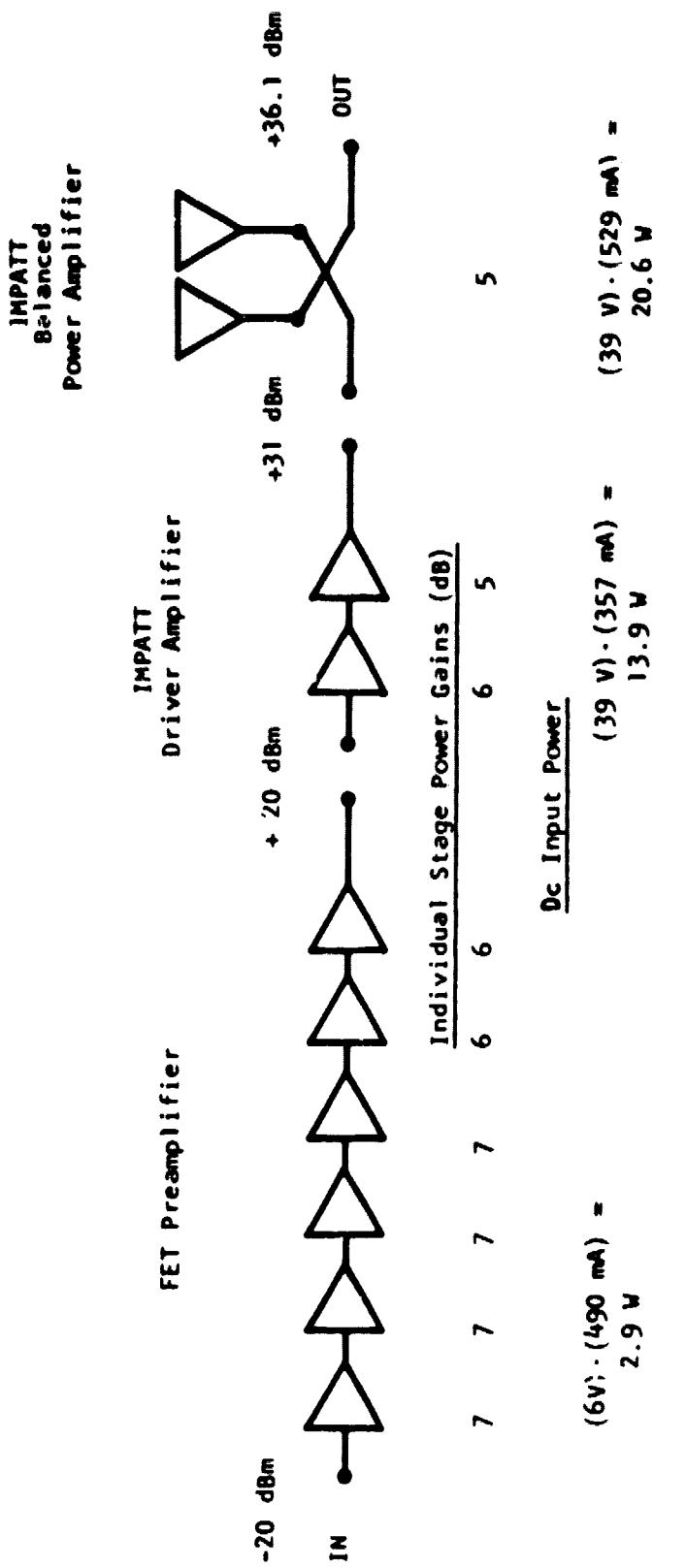
Figure 16 Block Diagram f Spacecraft Transmitter Amplifier

of an ILO stage is not directly proportional to its input power and, in fact, can be very insensitive to it. Consequently, the amplifier gain variation due to temperature changes is affected primarily by the temperature characteristics of the final ILO stage rather than by the cumulative gain variation of all preceding stages.

The primary disadvantages of an injection-locked oscillator approach are: (1) operation near power saturation over most of the input power range; (2) reduced bandwidth capability as compared to a broadband stable amplifier; (3) a locking bandwidth that is dependent on the input rf drive level; and (4) spurious output during zero input conditions. In light of the transmitter amplifier requirements however, it was possible to overcome the latter three disadvantages, as discussed later in this section. The problem of power-saturated operation results in poorer third-order intermodulation suppression at lower drive levels, e.g., at -30 dBm input power. Nevertheless, when put in perspective with the overall transmitter requirements, especially the efficiency and power output goals, the advantages of the ILO design far outweigh the disadvantages. As a consequence, the ILO approach was implemented in the IMPATT stages of the delivered amplifier.

An FET rather than an IMPATT preamplifier was chosen because of several key advantages that the former design provides. The FET preamplifier is easier to design and tune for stable operation. (Even flat profile IMPATTs are difficult to simultaneously tune for high efficiency and stable operation under zero drive conditions.) Furthermore, an FET amplifier is intrinsically less sensitive to changes in ambient temperature. Both the gain and the center band of operation drift significantly with temperature in an all-IMPATT preamplifier.[11] The FET design is more cost-effective because of a simpler, more compact MIC configuration; no ferrite material or permanent magnets are required. Finally, the FET preamplifier provides at least two orders of magnitude improvement in the noise figure, as well as improved linearity performance as compared to the IMPATT counterpart.

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The FET preamplifier is designed on the basis of small signal S-parameters. Because six stages of FET are used, attention is given to compact design to maintain the small preamplifier dimensions. Holes, 1 mm in diameter, drilled in the alumina substrate accommodate the FET chips, which are mounted on 0.15 mm thick gold discs. The FET preamplifier provides 41 dB of small signal gain and yields a 1 dB gain compression point of 100 mW.

The driver amplifier consists of two IMPATT stages of circulator-coupled reflection amplifiers operating in the ILO mode. Three of the five MIC-fabricated circulators serve as isolators at the input and output of the driver and between the two stages. The driver stage has a gain of 11 dB at an output power of 1.2 W.

The power amplifier consists of two single-mesa diodes power-combined via a 3 dB interdigitated coupler fabricated on a quartz substrate. This approach, rather than one using a single-ended amplifier with multiple-mesa chip-level power-combining, was implemented for two reasons. First, high-power multiple-mesa operation is difficult to achieve in a microstrip circuit[10,11] at mid Ku-band. Second, a balanced, circuit-power combined design is potentially a more reliable configuration, since there is more complete isolation both electrically and thermally between the combined mesas. Thus, a higher probability of optimum efficiency operation from both devices is achieved. The power amplifier stage provides an output power of 4.2 W at 5 dB gain.

All three amplifier chassis are integrated in a housing whose volume is 220 cm^3. Because of the high gain of the spacecraft transmitter amplifier, metal partition walls incorporating short sections of 50 Ω transmission line feedthroughs separate the three chassis to suppress potential signal feedback and spurious oscillation in the preamplifier. Also included in the housing are the bias distribution circuits, as well as the detector-activated IMPATT "squelch" circuit. This circuit ensures zero rf output from the amplifier for input signals below the threshold level (< -30 dBm).

B. FET Preamplifier Design and Performance

Because of the narrow bandwidth requirements of the spacecraft transmitter (fractional bandwidth of 1.7%), the circuit design for the FET preamplifier is quite straightforward. Small signal S-parameters are measured on the devices to be used, and simple single-section $\lambda/4$ microstrip transformers are designed to transform from a 50 Ω impedance level down to the required value as determined from the S-parameters. Bond wires connecting the device to the circuit provide the necessary inductance to cancel the capacitive reactance of the devices. Simple, conjugate impedance matching at 15 GHz is used for both gate and drain circuits.

The FETs are TI devices having 0.5 μm long, electron beam defined gates with total gate widths of 300 μm (four gate fingers, 75 μm each). For S-parameter measurements the FET devices are mounted in test circuits in the same manner used for the preamplifier. To minimize parasitic circuit elements associated with the device mounting scheme and to reduce the overall length of the multistage amplifier, a different mounting method was used from that usually employed at Texas Instruments for power devices. Instead of sandwiching a copper carrier block (on which the FET is soldered) between input and output microstrip circuits, a hole is drilled through the alumina substrate containing the etched circuit, and the device is mounted inside the hole and fixed to the same carrier to which the alumina microstrip circuit is attached. The FET device is soldered to a gold disc, 0.9 mm in diameter and 0.15 mm thick, and wire bond connections are made between the source pads and this disc. The disc serves two purposes: (1) it allows the ground connection to the source pads via the wire bonds, and (2) it serves as a pedestal for the device when it is placed in the hole to position the top surface of the 0.1 mm high chip level with the 0.25 mm thick alumina substrate. The disc is placed in the hole and attached to the substrate carrier block by conductive silver epoxy or solder. Wire bonds are then attached to the gate and drain pads and connected to the input and output microstrip lines, respectively.

Figure 17   FET Mounting Scheme to Reduce Parasitic Losses

```
**S PARAM. PROG.

FREQ. IN GHZ =
     15.0000
MAGN. S11?
     0.6800
ANGLE S11?
   -165.0000
MAGN. S12?
     0.1000
ANGLE S12?
    45.0000
MAGN. S21?
     1.7000
ANGLE S21?
    80.0000
MAGN. S22?
     0.4200
ANGLE S22?
   -155.0000
K=
     1.3624
MAG IN DB=
     8.7107
```

(a)
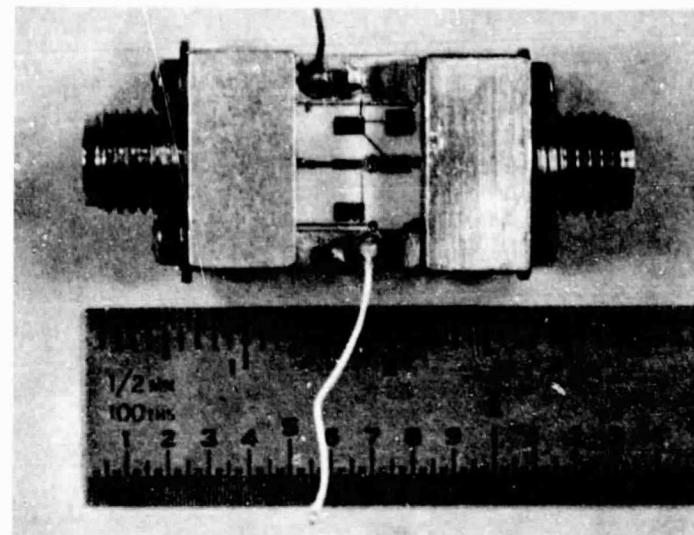
(b)
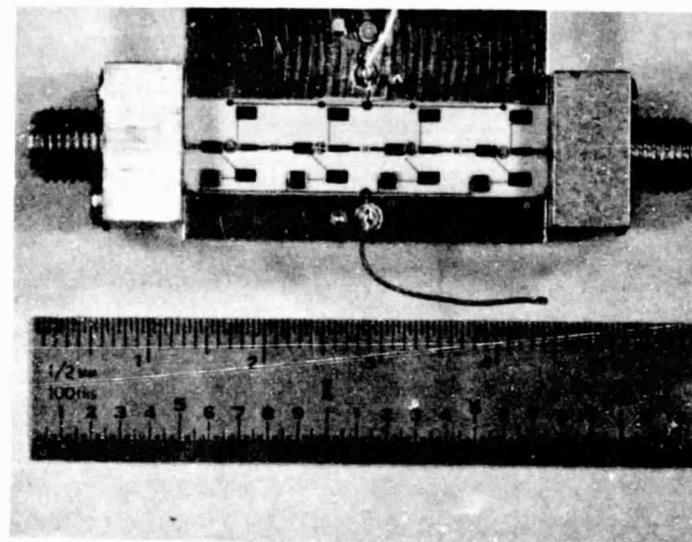
(c)

Figure 18   Single and Multistage 15 GHz FET Breadboard Amplifiers.
　　　　(a)　S-parameters for a 300 μm FET.
　　　　(b)　Single-stage amplifier with 8 dB gain.
　　　　(c)　Four-stage amplifier with 28 dB gain.
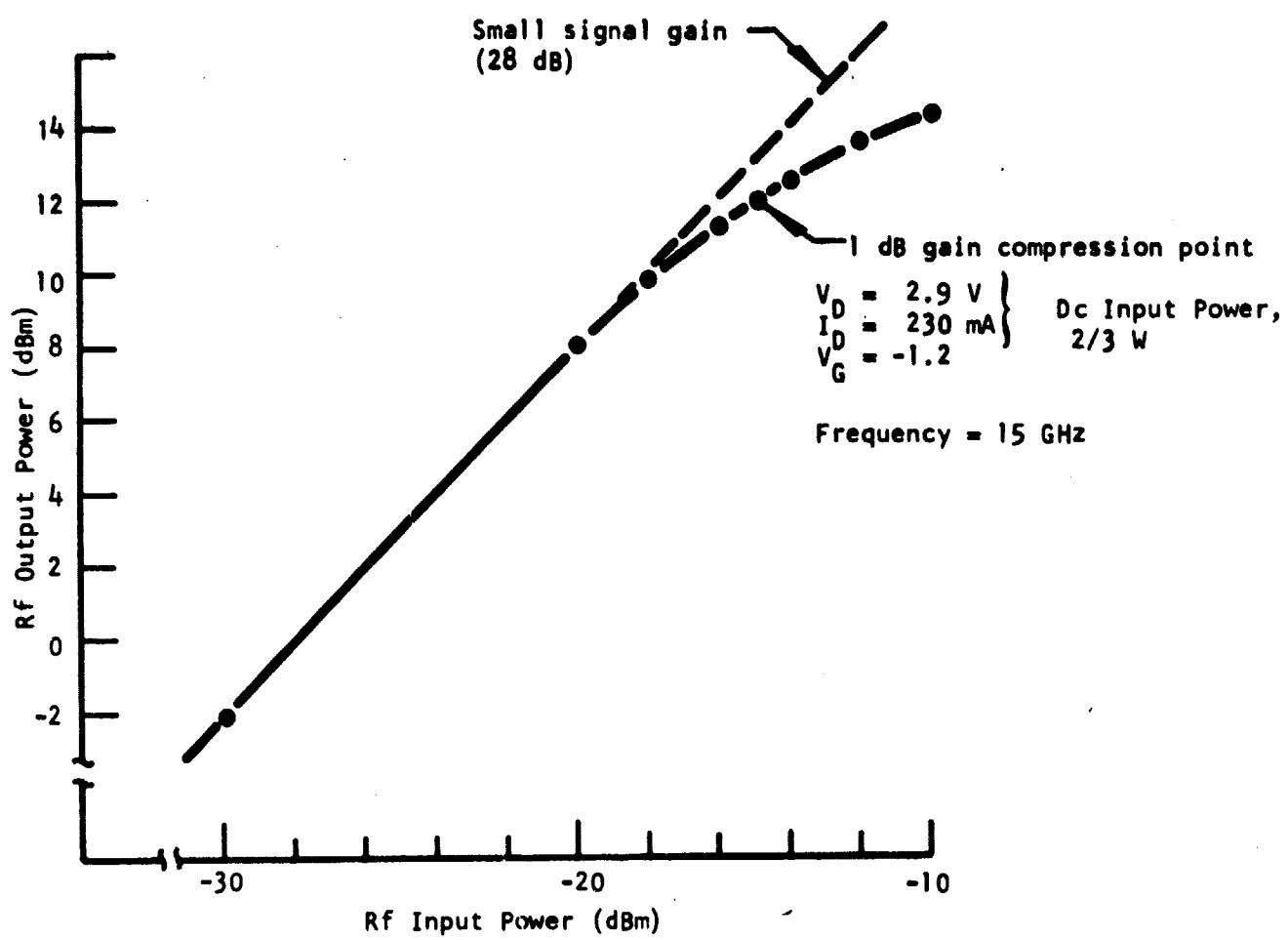
Figure 19 Gain Compression Curve For 15 GHz Preamplifiers

stages, such that the six-stage preamplifier is mounted on one carrier plate. For improved heat sinking the gold discs on which the FET chips are mounted and soldered to the carrier plate in the case of the 600 μm devices. To facilitate testing, the carrier plate is designed such that OSM connectors can be attached at three places for testing the first four, last two, or all six cascaded stages.

Figure 20 shows the FET preamplifier ready for testing the first four stages. A ribbon bonding scheme enables one to test either the first four or the last two stages. When checked out, the test microstrip line is made idle, and the main amplifier chain is connected. Also seen in Figure 20, at the extreme right of the alumina substrate, is the 10 dB coupler, which senses part of the input power and directs it to a detector for activating the shutdown circuitry for the IMPATT bias supply.

Figure 21 shows the gain compression curve for the actual preamplifier used in the final spacecraft transmitter amplifier measured at 15 GHz. A small signal gain of 42 dB and a 1 dB gain compression point of 20 dBm are achieved. Figure 22 shows the small signal gain versus frequency characteristic. Across the specified operating band a gain variation of 1.5 dB is observed for the preamplifier. For these measurements the last two stages operated at a drain voltage of 6.5 V, and the first four stages operated at a 4 V drain bias. A voltage dropping resistor was used so as to power the entire six-stage preamplifier from a single drain power supply of 6.5 V (in the final amplifier integration, the preamplifier power supply voltage for the drain was lowered to 6 V).

To further assess the linearity characteristics of this preamplifier, third-order intermodulation distortion measurements were performed at 15 GHz. Two signals separated in frequency by 10 MHz were applied to the preamplifier, and the level of the third-order products was measured. Figure 23 shows the level of the

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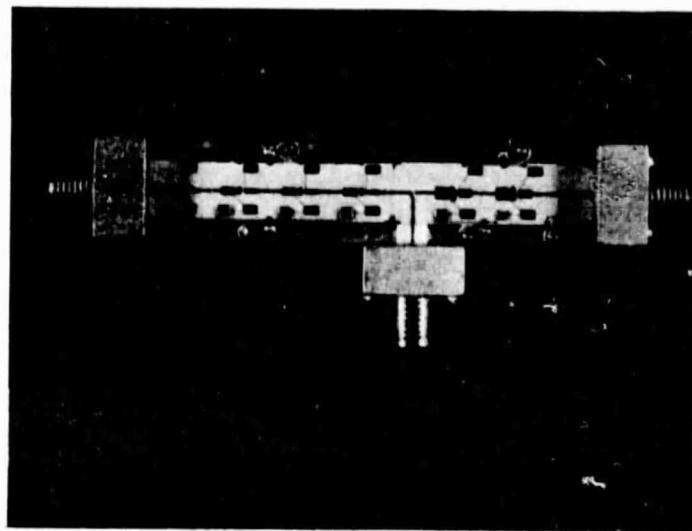
Figure 20 Six-Stage FET Preamplifier Ready for Testing
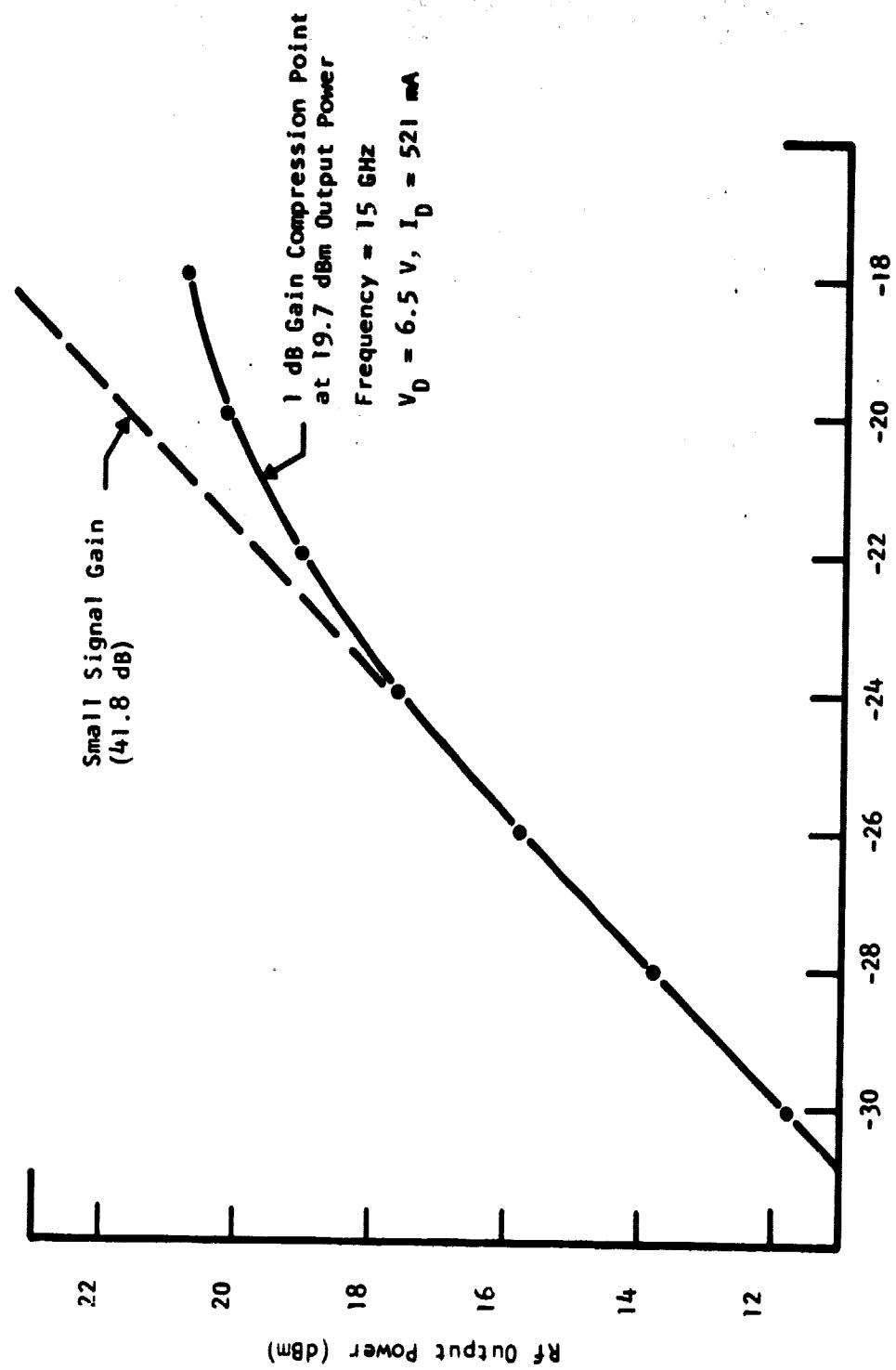
Figure 21   Gain Compression Characteristic for 15 GHz Six-Stage
Preamplifier

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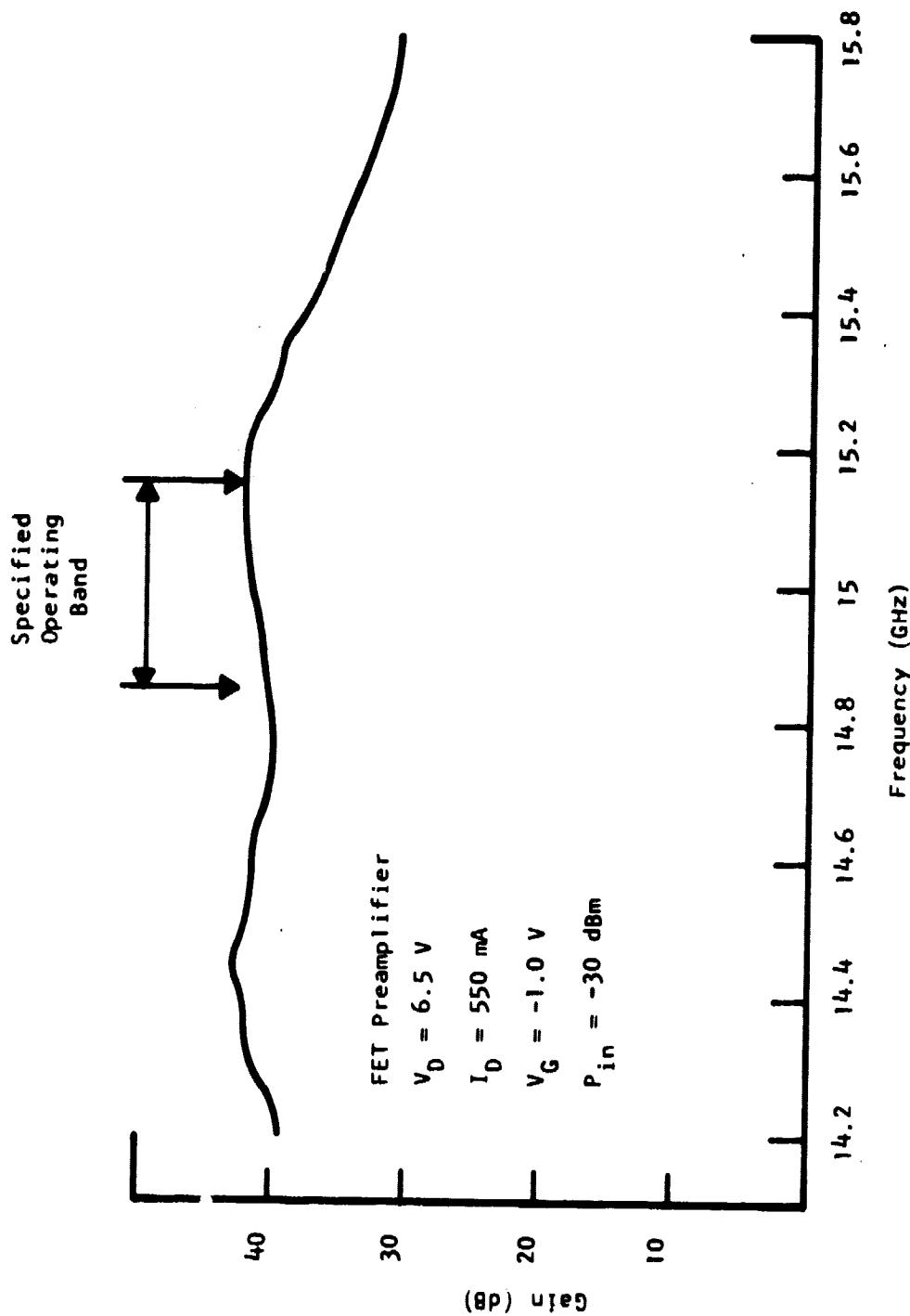
Figure 22   Gain versus Frequency Characteristic for 15 GHz Six-Stage
Preamplifier

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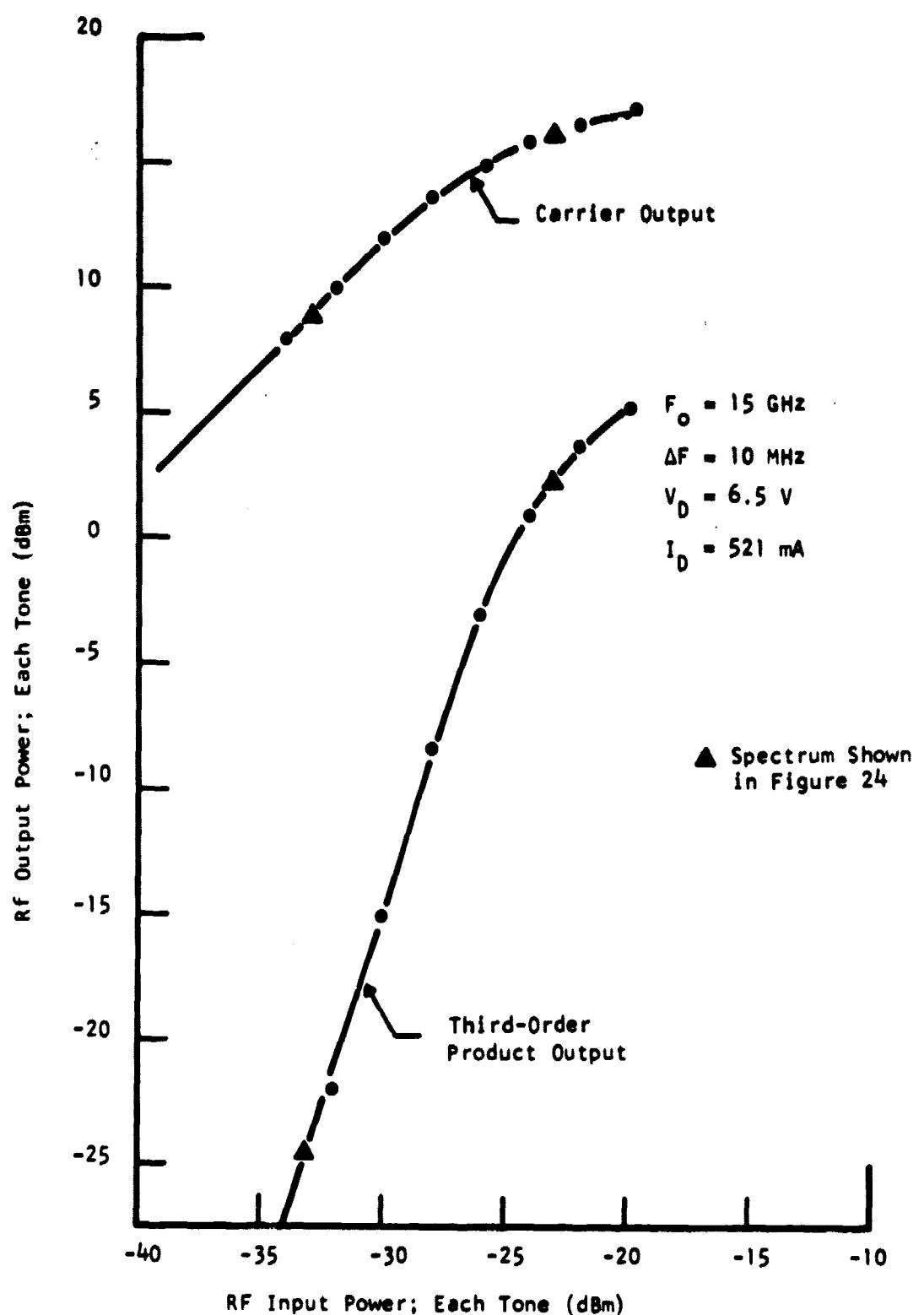
Figure 23 Third-Order Intermodulation Product vs Input
Level at Band Center of the Six-Stage FET
Preamplifier

third-order products as a function of input power. Figures 24(a) and (b) show the corresponding spectrum analyzer displays for input power levels of -33 dBm and -23 dBm, respectively. It is seen that for the former case the third-order products are 33 dB below the carrier level. This corresponds to at least a 12 dB improvement in third-order intermodulation performance over an all-IMPATT pre-amplifier operating at a lower frequency of 13.3 GHz.[11]

C.   IMPATT Driver Amplifier Design and Performance

The driver amplifier consists of two stages of circulator coupled reflection amplifiers operating in the injection-locked oscillator mode. Three additional MIC circulators serve as isolators at the input and output and between stages. The driver stage design follows closely that used previously at Texas Instruments for development of similar amplifiers.[8,10,11] A photograph of the driver chassis is shown in Figure 25. Simple $\lambda/4$ transformers (50 Ω to $\sim$ 3 Ω) and bonding ribbon inductance ($\sim$ 0.13 mm x 0.2 mm x 25 μm) are used for impedance matching to the diodes. The matching circuits are fabricated on 0.25 mm alumina substrates, while the circulator discs are etched on TTI-390 0.5 mm thick ferrite. SmCo permanent magnets (6.25 mm in diameter and 3.13 mm thick) mounted beneath the ferrite directly underneath the disc resonators bias the ferrite for circulator action.[11] For circulator optimization 0.38 mm thick shims are placed between the magnet and the bottom surface of the ferrite substrate. For additional control of the magnetic fringing field lines and circulator optimization, iron "pucks" are placed on the top surface of the ferrite. The circulator resonator disc etched on the ferrite has a diameter of 3.75 mm. A single quarter-wave transformer with a characteristic impedance of 31.6 Ω (with the ferrite demagnetized) is used for impedance matching the circulator to 50 Ω. The three isolators use the same circulator design, except that the magnets are reversed in polarity, and the circuit etched on the alumina is simply a terminated (by a thin-film resistor) 50 Ω line.

(a)

(b)
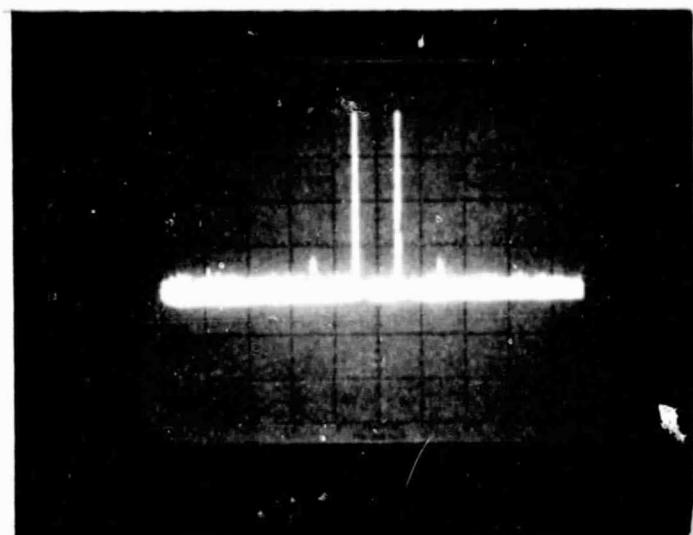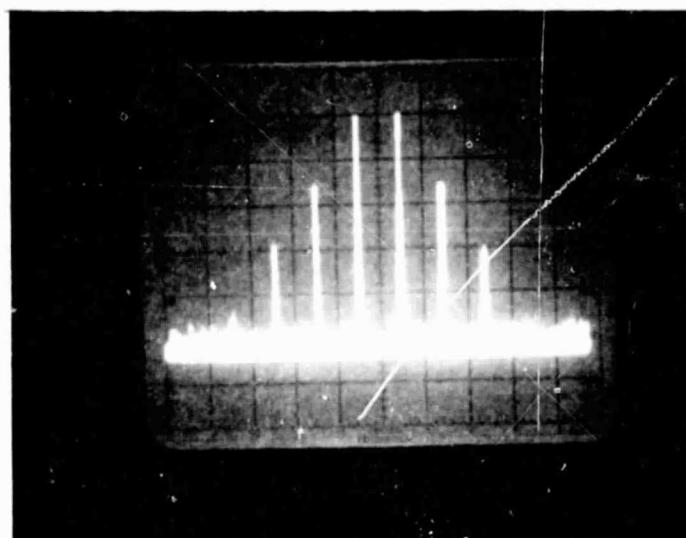
Vertical: 10 dB/div
Horizontal: 10 MHz/div
Center Frequency: 15 GHz

Figure 24   Spectrum Analyzer Display of FET Preamplifier Output With
    (a) Two -33 dBm Input Signals
    (b) Two -23 dBm Input Signals

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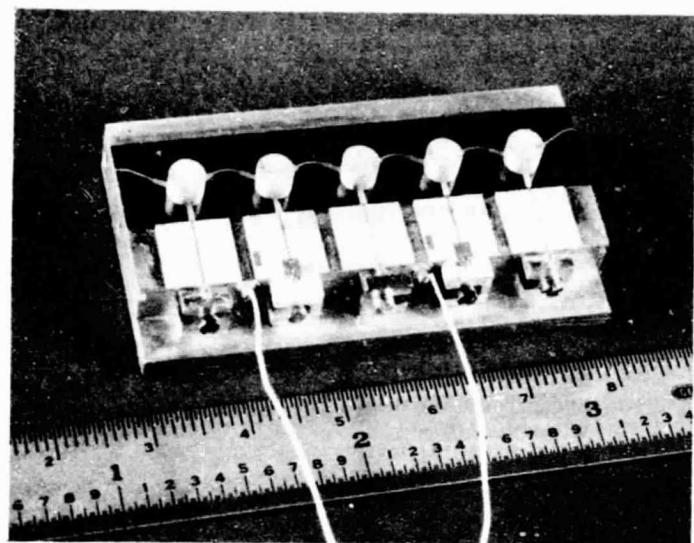
Figure 25   IMPATT Driver Amplifier Chassis

To check the total insertion loss of all circulators between 14 and 16 GHz, the magnets were positioned identically (with the same polarity) underneath the ferrite such that the signal passed only once through each disc, essentially traversing the driver chassis from input to output in a straight line. From 14 to 15.75 GHz the total insertion loss, including a pair of OSM connectors, was between 2.5 and 3.2 dB. The return loss from 14 to 15.2 GHz was greater than 20 dB, and greater than 12 dB from 15.2 to 16 GHz. Generally, the adjacent-port isolation of these circulators is also greater than 20 dB over at least a 1 GHz bandwidth for mid Ku-band center frequencies.[11]

The driver amplifier is designed to increase the power level to greater than 1 W, and yet maintain a locking bandwidth considerably in excess of 250 MHz to ensure the bandwidth performance over temperature. Because the locking bandwidth for a single-stage ILO is nominally proportional to the square root of the input power, the critical design operating point occurs at the lower input levels. Consequently, it is necessary to obtain a locking bandwidth of greater than 250 MHz at a driver input level of +10 dBm ($\sim$ -30 dBm input to the preamplifier), and yet maintain 10 or 11 dB gain at an input drive level of 20 dBm. This was achieved for the driver amplifier using single-mesa diodes (79 III) in each stage and the same impedance matching circuits used in the oscillator test fixture (Figure 15, Section II).

Table 3 summarizes the driver amplifier's performance, as well as the operating characteristics of the actual diodes used. An output power of 1.3 W and an added-power efficiency of 10% were achieved for the amplifier, including the losses in the series bias resistors. These resistors are necessary to stabilize the IMPATTs against low frequency bias oscillations. The performance of the actual devices, as characterized in the microstrip oscillator test circuit, is shown at the bottom of Table 3. Note that the efficiencies in this case include the losses in the microstrip line and OSM connector (0.2 to 0.3 dB) and do not include the losses in the bias line series resistor.

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Table 3

Driver Stage Performance

Input Power (dBm)	Locking Bandwidth (MHz)	Locking Limits (15 GHz ± MHz)	Output Power (dBm)	Diode Operating Voltage and Current and 10 mA Breakdown Voltage	
				First Stage	Second Stage
+10	420	-160, +260	31.0		
+15	820	-340, +480	31.1	26 V, 147 mA	35 V, 211 mA
+20	1500	-660, +840	31.2	$V_B = 17$ V	$V_B = 23$ V

Driver Stage Operating Voltage: 38 V

Series Bias Resistors: First Stage - 82 Ω

Second Stage - 13.3 Ω

Total Dc Input Power: 13.6 W

Power-Added Efficiency: 10%

Performance of Diodes in Microstrip Oscillator Test Circuit

First Stage Diode	Second Stage Diode
1.1 W, 14.5% at 15.5 GHz	1.4 W, 18.9% at 15.6 GHz

53

Although a 10% power-added efficiency was realized for this amplifier, a more careful pairing up of diodes, so that the operating voltage of both would be closer to the 35 V value, would result in still higher efficiency, since less power would be dissipated in the series bias resistors.

D.   IMPATT Balanced Power Amplifier Stage Design and Performance

A 3 dB microstrip interdigital hybrid coupler, the so-called Lange[12] coupler, is used to power-combine the outputs of two IMPATT diodes as shown schematically in Figure 16. Both the coupled and the direct ports of the coupler are terminated with an identical matching circuit and diode combination. Ideally, the voltage reflection coefficients looking into the diode circuits are equal in both magnitude and phase. Because of the 90° phase properties of the hybrid, the two reflected waves add in phase at the normally isolated port and cancel at the input port, resulting in the necessary isolation between input and output signals. Since the frequency of interest is mid Ku-band, the substrate chosen for fabrication of the coupler circuit is 0.25 ± 0.013 mm thick, fused quartz (GE 125) with a 60-40 surface finish. This choice of substrate for the coupler fabrication, rather than alumina, was made primarily because of the potential for lower loss due to the resulting wider line widths and smoother surface finish for the quartz substrate. The disadvantage of such thin quartz substrates, however, is that they are more fragile than equally thin alumina substrates, and extra care must be exercised during fabrication and assembly. The etched circuit dimensions for the coupler are: line widths in the coupling section, 0.075 mm; gaps between lines, 0.02 mm.

The original design and performance of this coupler were described in detail elsewhere.[10] Optimization of the coupler continue under this contract. In an attempt to reduce losses, plated-up silver (flashed with gold to prevent tarnishing)

approximately 2.5 μm thick, was used for the metallization. The pattern itself
was defined by etching a thin nichrome/Au base metallization, approximately 200 Å
thick. The insertion loss for a single pass for this coupler at 15 GHz is between
0.25 and 0.35 dB over and above the nominal 3 dB power split. Amplitude tracking
over the range of 14 to 16 GHz is better than 0.25 dB.

Figure 26 shows the balanced power stage (minus the IMPATT diodes) alongside
the other two component chassis prior to final assembly and tuning. Also shown
in the photograph is the Ku-band Lange coupler etched on a 22.5 x 10 x 0.25 mm
fused quartz substrate. The matching circuits consisting of the single section
λ/4 transformer, tuning pads, and 50 Ω line are all fabricated on the 7.5 x 7.5 x
0.25 mm alumina substrate.

Tuning of the balanced stage begins with careful selection of a pair of
nearly identical diodes. Diodes are matched to have nearly equal breakdown and
operating voltages, power output, and frequency of operation when tuned with
close to identical matching circuits. The selected pair of diodes is then
simultaneously tuned in the balanced stage to realize maximum combined output
power from the output port of the coupler, with a nominal input power of 31 dBm.
As in the case of the driver stage, both diodes are single-mesa devices that
operate in the injection-locked oscillator mode. However, since the driver stage
output power stays nearly the same at 31 dBm, the balanced stage locking bandwidth
is determined by this one input level. That is, the gain of the balanced stage
(and hence the locking bandwidth) remains constant at about 5 dB. For the diodes
and matching circuits used, the locking bandwidth at these drive levels is well
over 1 GHz.

From the coupler insertion loss measurements and from the single-mesa diode
characterization studies in the microstrip oscillator test circuits it is possible

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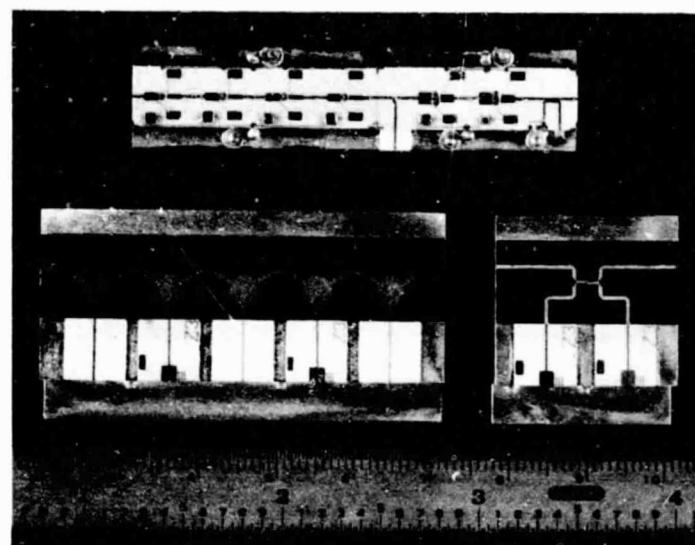
Figure 26   Preamplifier, Driver, and Balanced Power Amplifier Chassis

to estimate the anticipated balanced-stage power output performance. The assumption is made that the rf power added from each diode in the balanced ILO configuration is just equal to the oscillator output power when the diodes are tested separately in the microstrip oscillator test fixture. Figure 27 shows the calculation given a 3 dB coupler with an insertion loss of 0.3 dB (single pass) and two 1.8 W single-mesa diodes tested as free-running oscillators. An input to the balanced stage of 31 dBm is assumed. The output power is simply the addition of the available power output exhibited during free-running oscillator operation from each diode, plus the input power, minus the losses in the coupler. Note that the input power "passes" twice through the coupler, while the added power from the diodes suffers the loss corresponding to one pass through the coupler. As the figure shows, the result of the calculation is a power output of 4.5 W and a gain of 5.5 dB. To achieve the 5 W goal, diodes with microstrip oscillator powers of at least 2 W must be incorporated in the balanced stage and in the second stage of the driver amplifier.

Table 4 shows the balanced stage performance. An output power of 4.2 W at a gain of 5.2 dB and an intrinsic power-added efficiency of 16% was achieved at 15 GHz. A locking bandwidth of about 1.5 GHz was obtained. The operating characteristics of one of the diodes in the microstrip oscillator test fixture are listed at the bottom of the table. This diode yielded 1.8 W at an efficiency of 23% at 15.6 GHz. The second diode had nearly the same characteristic, with slightly less dc-to-rf efficiency ($\sim$ 20%).

In the final incorporation of the balanced stage into the spacecraft transmitter amplifier, series resistors are used to bias the two diodes from a 38 V dc source. A 9 Ω and an 11 Ω resistor are employed.

Given:

Two 1.8 W diodes (as free oscillators)
One 1.3 W driver amplifier
One 3 dB coupler with 0.3 dB loss (single pass)
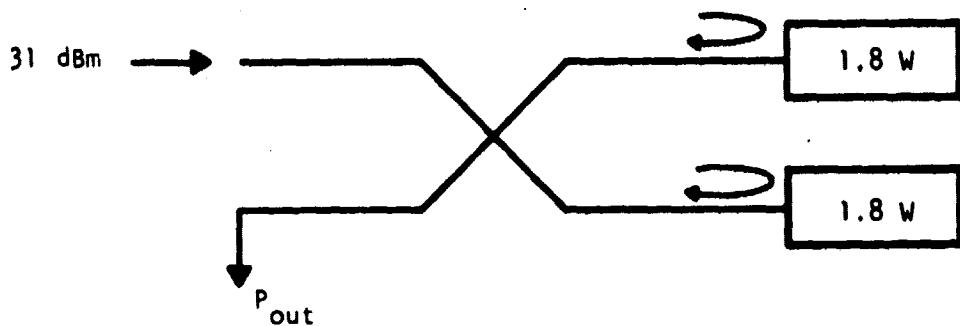
$$P_{out} = 1.3 \ (10^{-0.06}) + 2(1.8)(10^{-0.03}) = 4.5 \text{ W}$$

Gain = 5.5 dB

Figure 27   Estimated Balanced Power Stage Performance

Table 4
Balanced Stage Performance

Input Power	Output Power	Gain	Dc Input Power Diode A	Diode B
31 dBm	36.2 dBm (4.2 W)	5.2 dB	35.5 V, 279 mA	35.4 V, 242 mA

Power-Added Efficiency: 16%

Center Frequency: 15 GHz

Locking Bandwidth: ~ 1.5 GHz

Operating Characteristics of Diode B as a Free-Running Microstrip Oscillator

10 mA Breadkown Voltage: 23.6 V

Operating Voltage, Current: 35 V, 224 mA

Frequency: 15.6 GHz

Output Power: 32.5 dBm (1.8 W)

Dc-to-rf Efficiency: 23%

E. Design, Integration, and Performance of Spacecraft Transmitter Amplifier

1. Amplifier Housing

An aluminum housing is used to integrate all three amplifier chassis. This housing is shown in Figure 28 with the top lid removed. OSM connectors are used for the input and output rf ports. Three bias feedthroughs and a grounding pin are also visible in the photo on the input side of the amplifier. Two metal partition walls separate the three chassis for rf isolation between output and input. This is necessary to prevent spurious feedback, which can cause oscillation, especially for such a high gain amplifier. For example, at the lower input signal level (-30 dBm) the amplifier has a gain of 66 dB. Short sections of 50 Ω coax soldered in the 3 mm thick walls provide the rf feedthroughs from one chassis to the other. Indium "gaskets" are used on the top and bottom of the walls as well as near the rf connectors to provide good grounding. Indium wire is forced into grooves machined in the partition walls and in each amplifier chassis (two grooves can be seen in the photo of the driver stage, Figure 25). All three chassis are fastened to the base plate by screws from the underside of the housing. Thermal compound is applied between the mating surfaces to ensure good heat sinking. The bias resistors are chassis-mounted and heat-sunk in a similar fashion. All the bias shutdown circuit is likewise mounted on a circuit board and screwed to the housing. The power switching transistor is chassis-mounted and provided with good heat-sinking to the main housing. The amplifier housing, with the top cover screwed down, has a volume of 221 cm^3 and weighs 444 grams. The outside dimensions of the housing (excluding the OSM and bias connectors) are 14.9 cm x 5.7 cm x 2.6 cm.

2. Bias Shutdown Circuit

To shut off the IMPATT amplifiers when the rf input drops below the threshold level an rf detector-activated bias switching circuit with temperature compensation is used. The signal is sampled at the output of the FET preamplifier
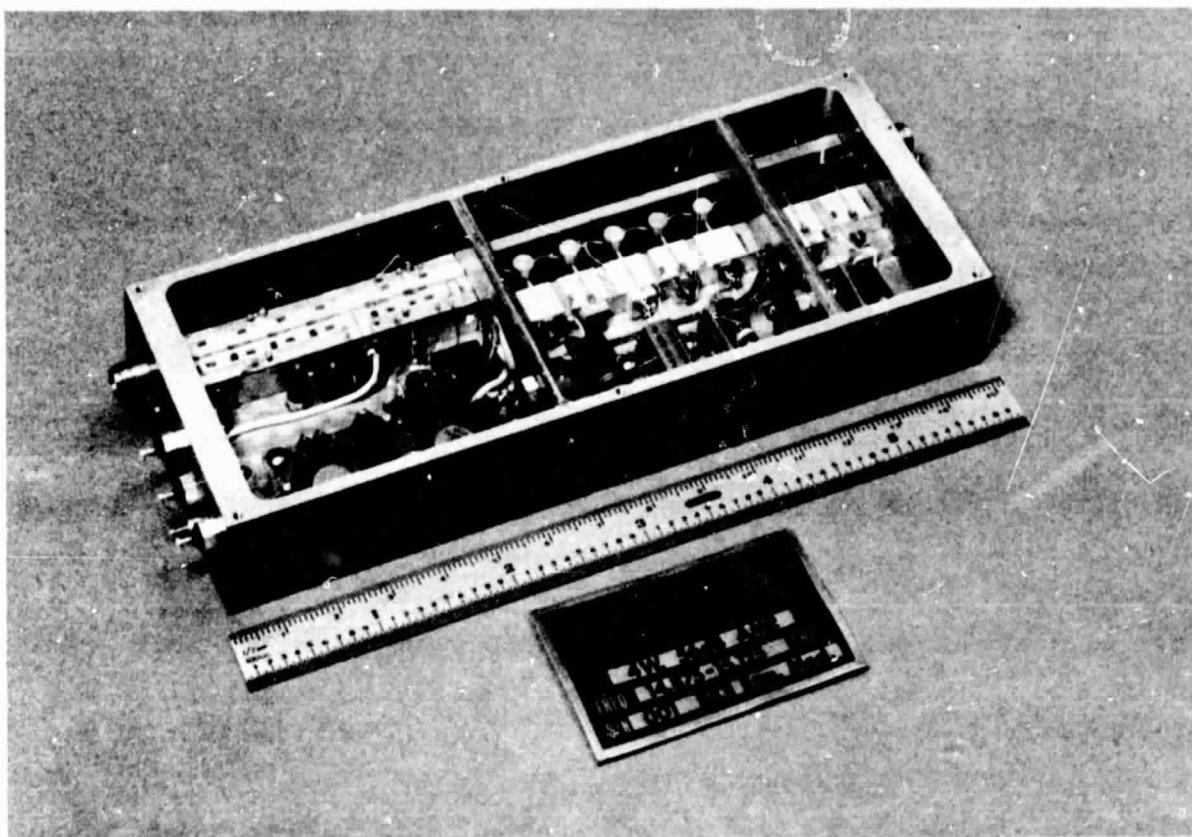
Figure 28   Integrated Spacecraft Transmitter Amplifier

by means of a 10 dB coupler etched on the alumina substrate. A beam lead Schottky detector, a beam lead 10 pF capacitor, and a 4 kΩ load resistor constitute the rf envelope detector. The circuit schematic diagram is shown in Figure 29. The major components of the circuit are the rf detector diode, the temperature-compensating (TC) diode, the operational amplifier, a comparator, and a power-switching transistor. Both the rf and TC diodes are identically biased. The operation of the circuit is as follows.

Under no rf drive the voltage at the rf and TC terminals of the Op-Amp are identical. Since the TC diode is another identical detector diode (but not embedded in any rf circuitry), these voltages will track with temperature as the forward I-V characteristic changes with temperature. Consequently, the output of the Op-Amp will remain zero as long as the sampled rf is zero. If the sampled rf is not zero, the detector voltage will drop, and a differential voltage will develop at the rf and TC terminals of the Op-Amp. This differential is amplified by a factor of 5 and applied to the comparator. If this differential voltage is higher than the fixed reference voltage at the comparator terminals, the output of the comparator will supply base current to the power-switching transistor (a Darlington pair) and switch on the primary 39 V source to all the bias resistors that connect in series to the various IMPATT diodes in the amplifier. Since the reference voltage at the comparator is adjustable via a miniature potentiometer, the level of rf drive that turns on the bias circuit can be adjusted. This potentiometer (Figure 28) is screwdriver-adjustable.

3. Integrated Amplifier Performance

Following assembly and testing, the three component amplifiers were integrated in the final amplifier housing as shown in Figure 28. The resultant 15 GHz amplifier module has an output power of 4 W (36.1 dBm) with 56 dB gain at an input of -20 dBm and 66 dB gain at an input of -30 dBm. Since the IMPATT
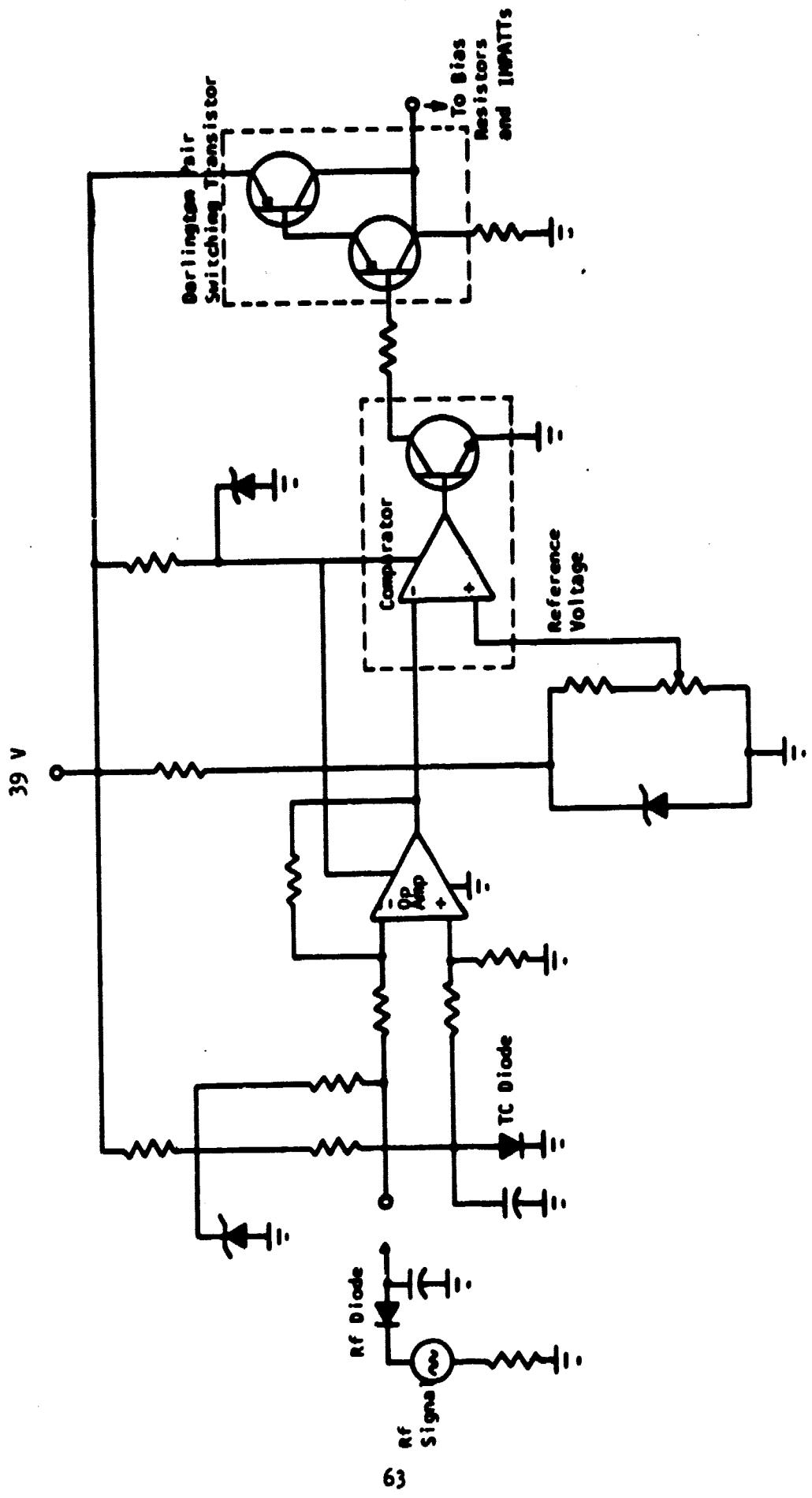
Figure 29 Automatic Shutdown Circuit and Detector Diode Temperature Compensation
Circuit for NASA Amplifier

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stages are operating in the injection-locked oscillator mode, a shut-down circuit cuts off bias to the IMPATTs whenever the input power drops below -35 dBm. A locking bandwidth of greater than 250 MHz is achieved for all input levels between -30 and -20 dBm at room temperature, at 0°C, and at 50°C. The overall dc-to-rf efficiency, including all active and passive bias circuitry, is 10.8%. Dc input power is applied via three external pin connections. The voltages and currents to these pins are:

39 V, 888 mA to IMPATT stages (including active bias circuits)

6 V, 490 mA to FET drains } FET stages (6).
-1 V, 0 mA to FET gates   }

All four IMPATT diodes used in the 1 W driver amplifier and in the final balanced power stage are from the best diodes processed to date and are from slice #77C1-79III. These diodes offer high power and efficiency and incorporate the TiW barrier for high reliability.

Measurements of amplifier gain and power output versus frequency and of locking bandwidth were performed at three different baseplate temperatures, 0°, 25° and 50°C. Third-order intermodulation distortion measurements were performed at room temperature for the integrated amplifier as well as for the FET six-stage preamplifier. The IMPATT bias supply shut-down circuit was checked at the three different temperatures for proper operation. Figure 30 shows the rf output power over the specified frequency band of 15 GHz, ±125 MHz, for the three temperatures. The output power is seen to vary no more than 0.5 dB for any frequency within the specified bandwidth over the temperature range of 0° to 50°C. At 25°C the output power varies less than 0.25 dB over the specified frequency range. Since the IMPATTs are operating in the injection-locked oscillator mode, very little output power variation is observed with changes in input power. Over the input range of -30 dBm to -20 dBm the output power varies less
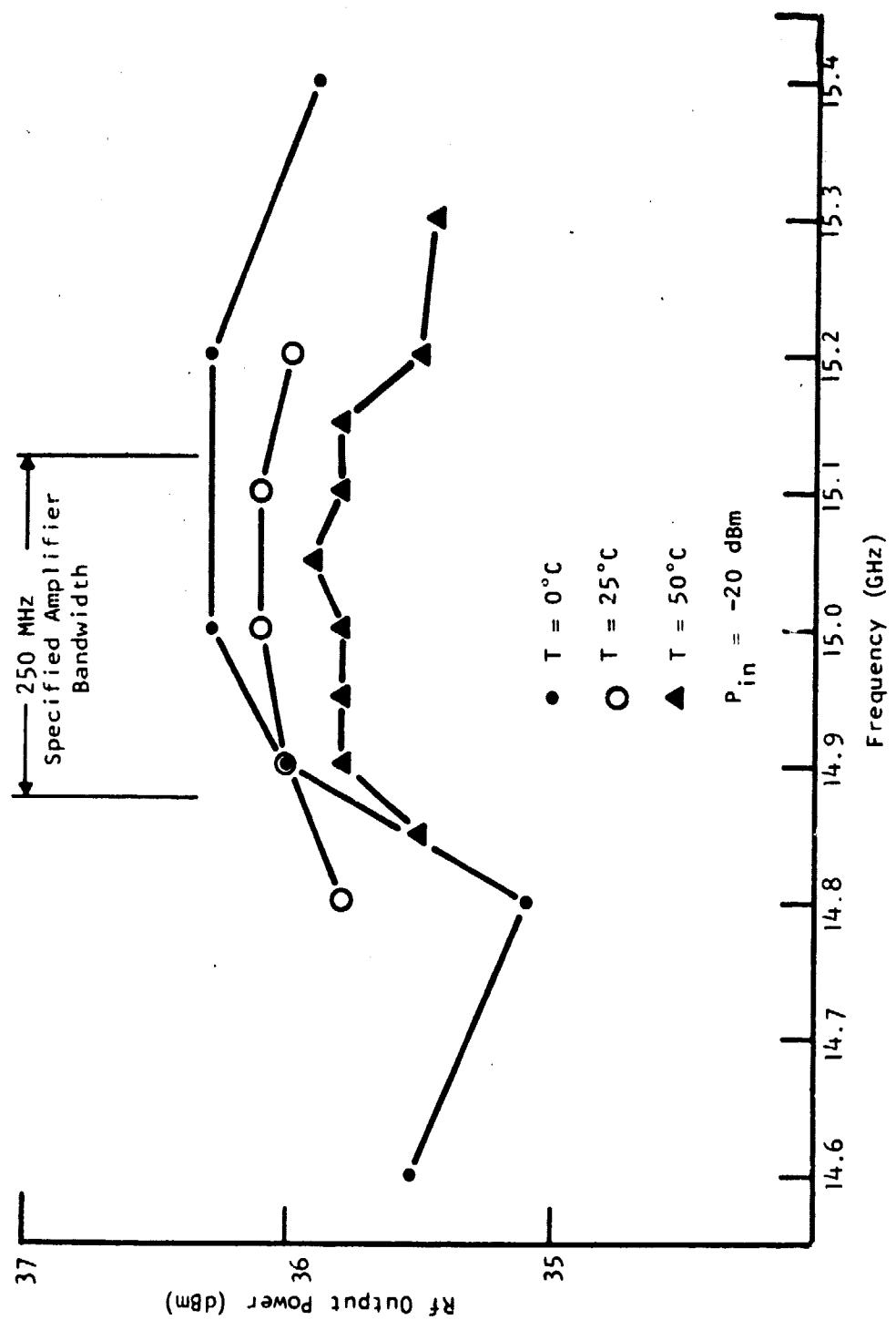
Figure 30 Output Power vs Frequency Characteristic For 4 W Amplifier
for Baseplate Temperatures of 0°C, 25°C, and 50°C

than 0.2 dB at 15 GHz for all three temperatures measured. The locking band-width, however, is about 560 MHz at -30 dBm and more than 1 GHz for -20 dBm of input power. No spurious signals were observed in the specified frequency band for all three temperatures. Figure 31, for example, shows the output spectrum of the amplifier while it was operating at a baseplate temperature of 50°C.

Figure 32(a) shows the third-order intermodulation measurement results for the total integrated amplifier. Two -33 dBm input signals separated by approximately 10 MHz were applied to the amplifier. The third-order products are down in power from the two main signals by 8 or 9 dB. This is due to the power saturated operation of the IMPATT stages. Figure 32(b) shows the corresponding output power spectrum for two -23 dBm signals.

Table 5 summarizes the locking bandwidth characteristics of the amplifier. As expected, the locking bandwidth decreases with increasing temperature. At 50°C some spurious signals 30 dB below or lower were observed at 14.4 GHz when the input signal was at 15.2 GHz, and some low-level spurious signals (out of the specified operating band) were observed at an input signal frequency of 14.94 GHz. Otherwise, the amplifier tracked the input frequency across the entire locking range.

Finally, Figure 33 shows the measured AM-to-PM conversion characteristics for the amplifier. The measurements were made at a baseplate temperature of 25°C and at three frequencies (14.9, 15, and 15.1 GHz) over the specified input range of -20 to -30 dBm. For these measurements the phase angle for an input power of -20 dBm was arbitrarily set at 0°. It is seen that the worst-case average AM-to-PM conversion over the -20 to -30 dBm input range is 4.5°/dB.
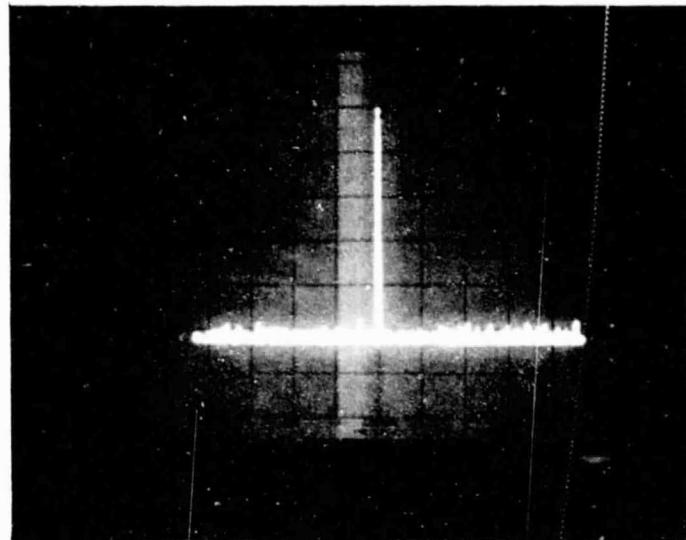
Vertical: 10 dB/div

Horizontal: 50 MHz/div

Center Frequency: 15 GHz

P_{in} = -20 dBm

P_{out} = +35.9 dBm

Figure 31 Spacecraft Transmitter Amplifier Output Spectrum at 50°C
Baseplate Temperature

(a)

(b)
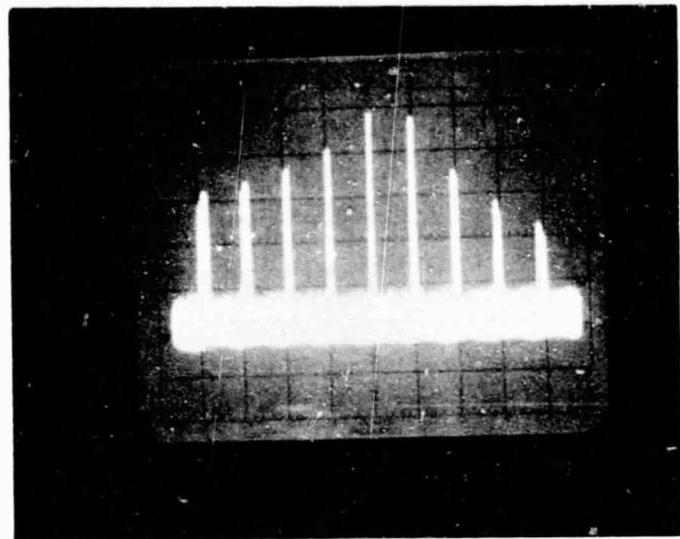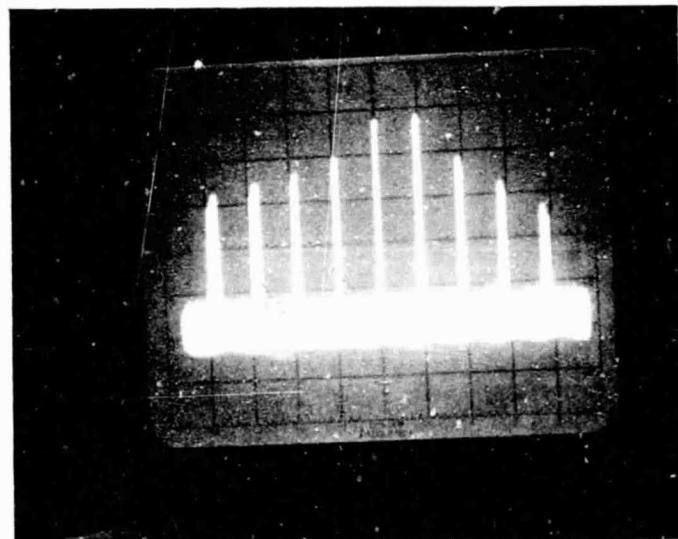
Vertical: 10 dB/div
Horizontal: 10 MHz/div
Center Frequency: 15 GHz

Figure 32   Spectrum Analyzer Display of 4 W Amplifier Output With
(a)   Two -33 dBm input signals
(b)   Two -23 dBm input signals

Table 5
Locking Bandwidth Characteristics of
Spacecraft Transmitter Amplifier

	Input Power (dBm)	Locking Bandwidth (MHz)	Locking Limits (15 GHz ± MHz)
T = 0°C	-30	620	-160, + 460
	-25	900	-300, + 600
	-20	1,440	-720, + 720
T = 25°C	-30	560	-160, + 400
	-25	1,010	-470, + 540
	-20	1,370	-800, + 570
T = 50°C	-30	380	-150, + 230
	-25	450	-150, + 300
	-20	1,180	-700, + 480
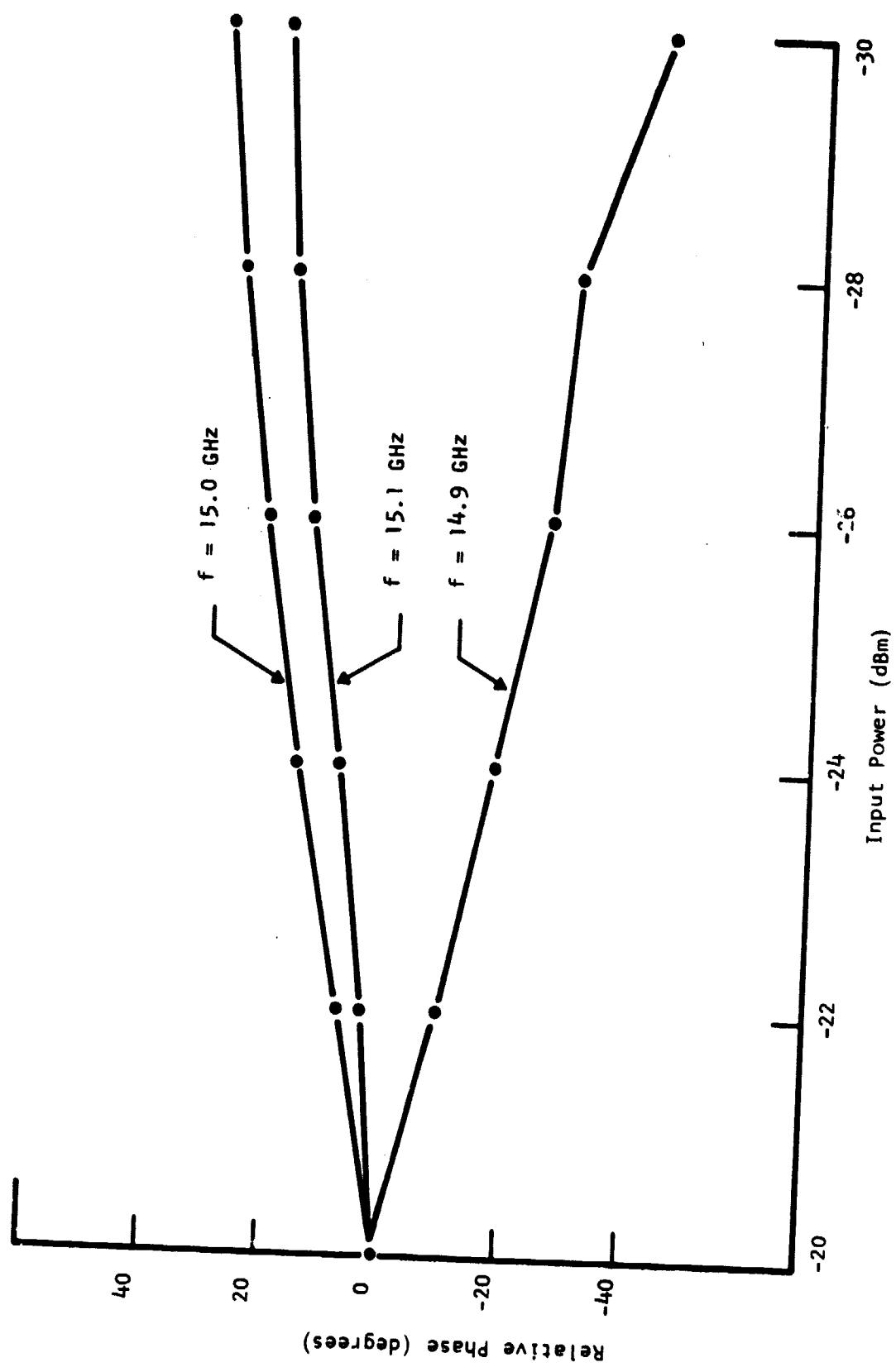
Figure 33 AM-to-PM Conversion Characteristics for Spacecraft Transmitter Amplifier

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SECTION IV
IMPATT RELIABILITY STUDIES

All the devices employed in the studies discussed in this section utilize the high reliability metallization system described in Section II.C. Following an introduction in which the pertinent reliability theory is presented, the techniques employed to measure thermal impedance are discussed. Then, the results of three reliability tests are presented in separate subsections. These test are temperature stress, dc bias-temperature stress, and rf bias-temperature stress.

A. Introduction

The mean-time-to-failure (MTTF) of semiconductor devices is found to be proportional to

$$\exp \left[E_A/kT \right] \ ,$$

where E_A is the activation energy of the dominant failure mechanism,

    k is the Boltzmann constant, and

    T is the temperature in Kelvins.

This relationship is valid provided a single failure mechanism is dominant over the temperature range of interest. By measuring the MTTF at different temperatures, the activation energy may be determined, and the MTTF at any temperature within the applicable range can be projected.

Table 6 shows the activation energy of GaAs IMPATTs incorporating various barrier metallizations published by other investigators. Since the TiW barrier metallization can be expected to have a similar activation energy, we will henceforth assume an activation energy of 1.6 eV. Clearly, our choice is somewhat conservative. It should be stressed that this activation energy is meaningful

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Table 6

Activation Energy of GaAs IMPATTs

With Different Barrier Metallizations

Reference	Type	Structure	Barrier Metal	E_A (eV)	MTTF Hours At T_j (°C)	Type Stress
1	Junction	High-Low	Ni	2.8	10^7 at 237	Temperature
2	Junction	Flat	900 Å Ti	1.8	10^7 at 240	Bias
3	Schottky	Flat	1000 Å Ti	1.6	10^7 at 245	Bias-Temperature
4	Junction	High-Low	Mo	--	$> 10^7$ at 200	?
5	Schottky	High-Low and Low-High-Low	W	--	--	Temperature
6	Schottky	Flat	750 Å Ti	1.7	--	--

1. F. E. Rosztoczy, et al., Electron. Lett. 11, 179 (1975).
   S. I. Long, et al., Microwaves, p. 56 (October 1975).

2. P. Staecker, et al., 12th Ann. Proc. Reliability Physics, p. 293 (1974).

3. W. C. Ballamy and L. C. Kimerling, IEDM Technical Digest, p. 90 (1977).

4. K. Nishitani, et al., IEEE Trans. Electron Devices ED-24, 1205 (1977).

5. G. Mahoney, Appl. Phys. Lett. 27, 613 (1975).

6. O. Wada, et al., Appl. Phys. Lett. 29, 263 (1976).

only when the dominant failure mechanism is that due to the interaction of the GaAs with the barrier metal. Consequently, any accelerated life test must be carefully devised so that extraneous failure mechanisms are not introduced. For example, a bias-temperature test conducted in the presence of ambient contaminants may result in early failures at the mesa surface and thereby become the cause of the principal failure mechanism.

Once the activation energy of a particular device configuration has been determined, accelerated life tests can be conducted. From such tests the MTTF at normal operating temperatures can then be predicted. The life test acceleration factor (LTAF) is the ratio of MTTFs,

$$\text{LTAF} = \frac{(\text{MTTF})T_1}{(\text{MTTF})T_2} = \left[\exp \frac{E_A}{k} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right] \quad . \tag{2}$$

As will be shown in Section IV.B., the junction temperature of the IMPATTs under normal operating conditions, denoted $T_j(\text{ref})$, is 200°C [this value for $T_j(\text{ref})$ will be used henceforth]. Letting T_1 represent $T_j(\text{ref})$, then the LTAF for any other temperature T_2 can be calculated by using Equation (2). For example, if $T_2 = 275$°C, then the LTAF is 215.

B. Thermal Impedance, R_θ

In this subsection we present R_θ calculations employing a thermal circuit model, a technique for determining R_θ by using the device reverse bias characteristics, and the results of some thermal impedance experiments.

1. Thermal Circuit Model

Detailed thermal impedance calculations of the IMPATTs have been made by taking into account the materials and geometries affecting the thermal circuit;

Figure 34 shows a typical thermal circuit employed for such calculations. The thermal impedance within the IMPATT structure, including the metallizations up to the plated Au heat sink, is calculated by consideration of the distribution of the dissipated power and the thermal conductivity of materials through which it flows. The heat flux is assumed to spread through a truncated conical cross section of angle ϕ. The thermal impedance of a semi-infinite heat sink is

$$\frac{1}{4kr_o} \quad ,$$

where k is the thermal conductivity and r_o the radius of the heat source. The thermal impedance of a conical section is

$$dR_\theta = \frac{1}{k} \frac{dz}{\pi r^2(z)} \quad ,$$

where

$$r(z) = r_o + z \tan \phi \quad .$$

Integrating from zero to infinity results in

$$R_\theta = \frac{1}{\pi k \tan \phi \, r_o}$$

to obtain

$$\phi = \tan^{-1} 4/\pi \cong 52° \quad .$$

It is worth noting that certain case structures have been treated more exactly by Kennedy[13]; the results obtained under the above assumption for those case structures compare very well with those obtained by the more exact computations.
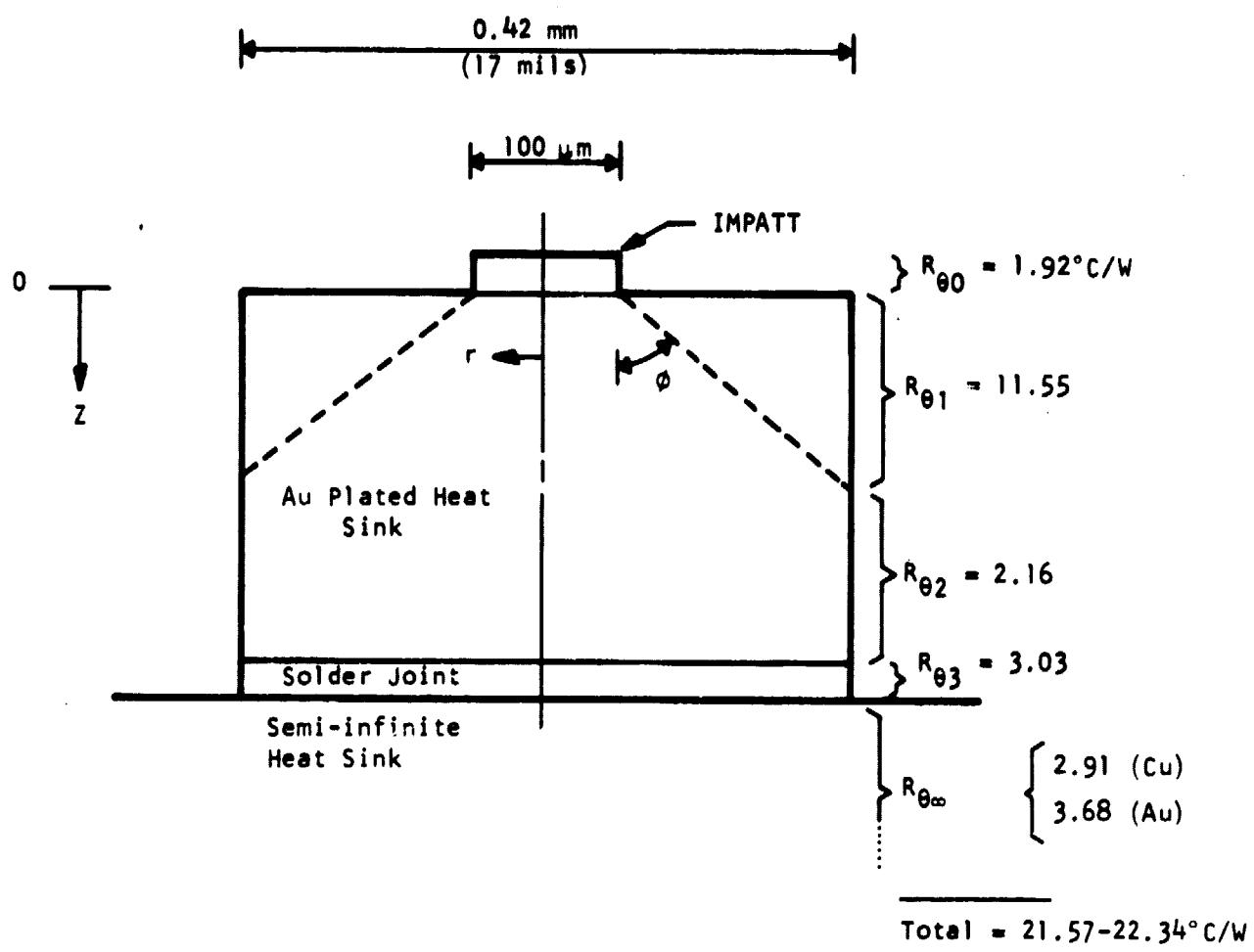
Figure 34   Thermal Circuit Model for Thermal Impedance Calculation

In Figure 34, a 100 μm IMPATT [typical 15 GHz IMPATTs have 100 to 140 μm (4.0 to 5.5 mil) diameters] attached to a 0.25 mm (10 mil) thick Au plate heat sink is shown soldered onto a semi-infinite heat sink. This configuration is representative of the thermal circuit of the IMPATTs in the delivered amplifier. As previously indicated, the IMPATT mesas are fabricated on 0.5 mm (20 mil) centers. The heat sink is then sawed with a 75 μm (3 mil) wire saw to result in a 0.42 mm (17 mil) square heat sink. The 80% Au/20% Sn solder joint is assumed to be free of voids and to be 25 μm (1 mil) thick, as typically observed on cross-section specimens.

For the thermal circuit of Figure 34, a thermal impedance of 21.6 - 22.3°C/W is obtained; for a packaged device (see Figure 13), a thermal impedance of 26.1°C/W is obtained when the screw thread boundaries are assumed to be perfectly mated. If the IMPATT is mounted directly on a semi-infinite Au heat sink, an R_θ of 17.6°C/W is obtained. Thus, the thermal circuit of Figure 34 is degraded by 27% from the "ideal," where most of the degradation is due to the solder joint. Accordingly, the design of the thermal circuit is considered satisfactory.

2. Determination of R_θ using the Reverse Bias Characteristics

Figure 35 shows the idealized reverse bias characteristics of an IMPATT under avalanche conditions at three constant junction temperatures. Since the diode voltage is a function of both current and temperature, the differential, dV, is given by

$$dV = \frac{\partial V}{\partial I} \, dI + \frac{\partial V}{\partial T} \, dT . \tag{3}$$

Also

$$R_\theta = \frac{\Delta T}{\Delta P} = \frac{dT}{d(VI)} = \frac{dT}{VdI + IdV} \quad .$$
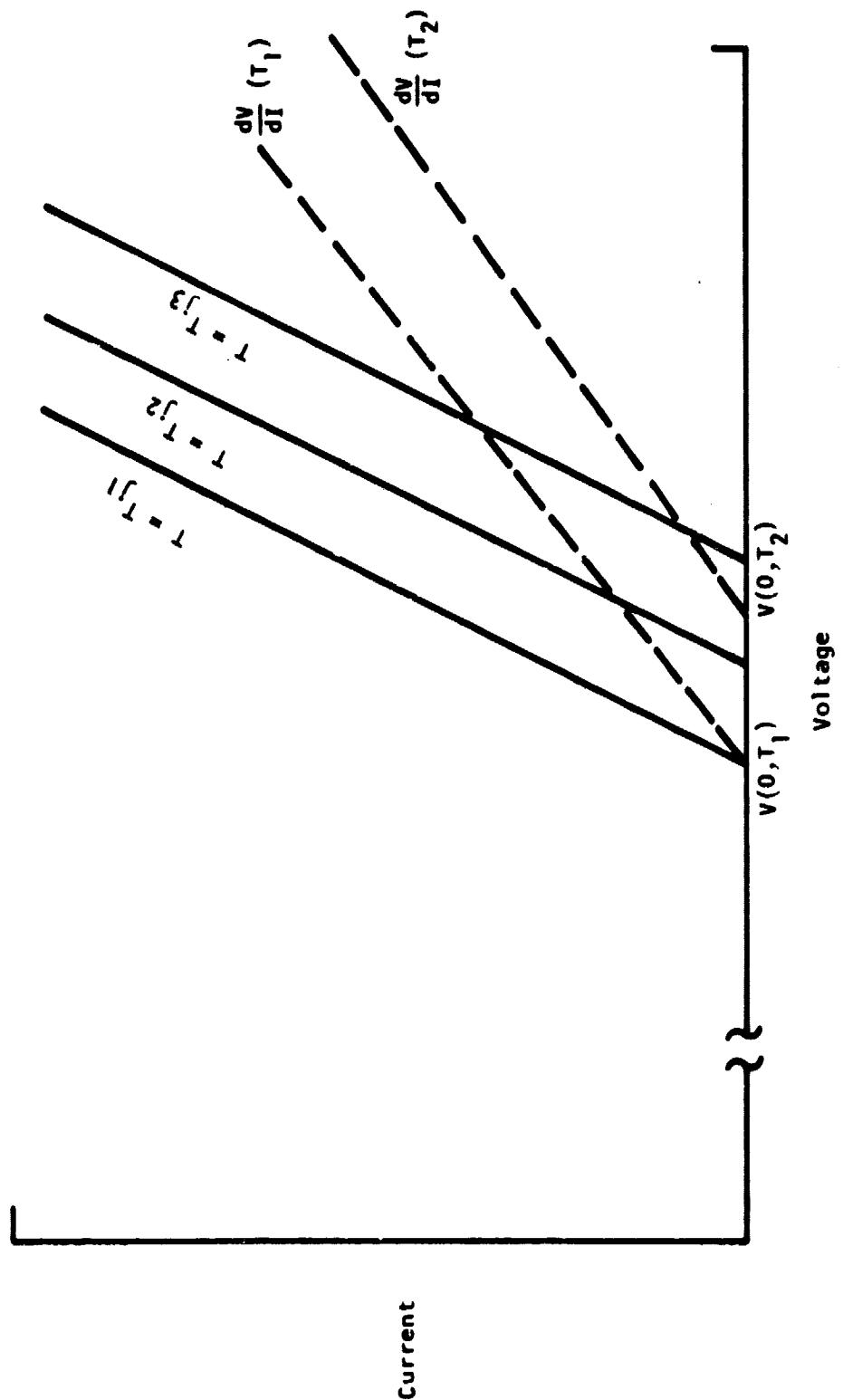
Figure 35 Idealized Reverse Bias Characteristics of an IMPATT

If the measurement is referenced to zero current such as point $V(0,T_1)$ in Figure 35, then

$$R_\theta = \frac{dT}{VdI} \cdot$$ (4)

By manipulating and combining Equations (3) and (4), we obtain

$$R_\theta = \frac{(dV/dI) - (\partial V/\partial I)}{V (\partial V/\partial T)} \cdot$$ (5)

To utilize Equation (5), the reverse voltage is measured, to four significant figures, at reverse bias currents between 10 and 50 mA in 5 mA increments with the heat sink maintained near room temperature. The measurement is repeated in the heat sink at $\sim 80°C$. The data are analyzed by linear regression to obtain dV/dI (T_1), V $(0,T_1)$, V $(0,T_2)$ and thereby $\partial V/\partial T$; typically, the correlation coefficient of the data is ≥ 0.998. It is worthwhile to note that the leakage current is typically $\ll 10$ mA; when this is not the case, such data points are discarded. The space charge resistance, $\partial V/\partial I$, is most easily measured with a vector ohmmeter; this measurement is made at 25 and ~ 50 mA with the heat sink at room temperature at 1, 3, and 9 MHz. Care is taken that the diode is not oscillating. Further, a 400 Ω series resistor is employed in the bias circuit to isolate the power supply's internal resistance from the measurement.

Analysis of the errors associated with measurement inaccuracies indicates a maximum possible (worst-case) error of $\pm$ 11% in the determination of R_θ; the probable error is $\leq 5\%$. Accordingly, high confidence is placed on this measurement technique.

All measured values of thermal impedance contained in this report were obtained by the method just described except for those cases where it is explicitly stated otherwise.

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3. R_θ Experiments

Four LHL IMPATTs with known R_θ's in the 18 to 19°C/W range were
measured. Initial measurements resulted in R_θ's ranging from 31 to 38°C/W.
It was determined that the discrepancy was due to the added thermal impedance
of two screw thread boundaries. When thermal compound was applied to these
screw thread boundaries, thermal impedances of 19 to 21°C/W were obtained,
indicating that our measurement technique is satisfactory.

In a second experiment, seven diodes were specially prepared for thermal
impedance measurements. The diodes were mounted in special packages with a
massive heat sink; also, this arrangement had only one screw thread boundary to
the heat sink. The diode areas were measured, and a simple $50.8\,\mu$m (2 mil) wire
was bonded to the mesa top.

The thermal impedance, R_θ, of each diode was then measured by three
different techniques: (a) the reverse I-V method previously described, (b)
an infrared radiometer method, and (c) a liquid crystal method. The results
are shown in Table 7. Also shown are the calculated R_θ's for the device/package
combination employed; in these calculations the screw thread boundary is assumed
to be perfectly mated to a semi-infinite copper heat sink.

It is apparent that the liquid crystal method of R_θ measurements is not
adequately reproducible due to the subjectivity required in the measurement. The
agreement between the other two methods is good. Except for one case, the
radiometer technique results in lower measured values of R_θ's; this is because
the temperature at the mesa periphery is somewhat lower than the average
junction temperature.[*] Accordingly, the IV technique is judged the more accurate.
This experiment also verifies the validity of the IV measurement technique.

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[*] The junction temperature is a function of r; it is highest at the center of the
diode and decreases toward the periphery.

Table 7
Thermal Impedance Measurements by Different Techniques

Diode	1	2	3	4	5	6	7
Diode Area (10^{-4} cm^2 units)	1.05	1.65	1.92	1.33	1.52	1.16	1.16
Ideal R_θ (°C/W)	19.4	15.0	13.7	16.9	15.8	18.3	18.3
Measured R_θ (°C/W)							
I-V Method	45.9	34.8	35.7	32.8	38.7	31.4	63.8
Radiometer Method	40.5	28.7	Shorted	25.9	33.4	32.4	40.5
Liquid Crystal Method							
Trial 1	31.8	36.0	-	34.7	48.3	33.1	45.4
Trail 2	50.0	38.1	-	31.3	52.6	36.8	53.0
Trail 3	41.9	37.6	-	28.7	39.4	34.3	52.4

In a third experiment, 16 diodes were mounted in the special package with the massive heat sink. The measured R_θ's ranged from 33 to 47°C/W, considerably greater than expected from thermal circuit calculations. The deviation between expected and measured R_θ's could not be attributed solely to imperfect screw thread boundaries and/or to metallization/solder joint imperfection. For such a large sample population, some of the diodes would exhibit R_θ's close to expected values. Furthermore, the discrepancy could not be due to measurement technique, since it was confirmed by the two previously described experiments.

Accordingly, the diodes were closely inspected. It was found that the typical size of the plated heat sink was only 0.32 mm (12.5 mils) square. This unexpected result was probably due to the ductility of gold, which "tears" to a greater extent than was anticipated. Recalculation of R_θ for the smaller heat sink size resulted in R_θ's of 35 to 39°C/W for device diameters of 100 to 140 μm.

This problem was discovered toward the end of the program, and corrective action could not be undertaken. Such corrective action would be to place the mesas on 0.75 mm (30 mil) centers; parenthetically, the mesas were put on 0.50 mm centers in order to obtain a maximum number of diodes from each slice. Other easily implemented improvements are thermocompression bonding of the plated heat sink and reducing its thickness to ~ 0.15 mm. With these improvements, thermal impedances close to the ideal of 17.5°C/W should be realized.

It should be noted that the IMPATTs employed in the delivered amplifier are of larger diameter. Although their R_θ's were not measured, their rf performance characteristics, together with the power dissipation in them, suggest R_θ's of less than 30°C/W.

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C. Temperature Stress Test

Devices from lots 77Cl-77-III and 77Cl-79-III were employed for this investigation; both incorporated the high reliability, barrier metallization system. Lot 77III had Schottky barrier back contacts, while 79III had ohmic back contacts.

The rf performance of unstressed devices from each lot was characterized. A total of 73 unpackaged devices were stressed at 400°C in a dry N_2 ambient. The forward and reverse characteristics of all devices were checked periodically, as were the impurity profiles of ~ 15% of the devices. Samples were taken at 80, 285, and 400 hours, and then packaged for testing. The rf performance of the stressed population did not differ from that of the unstressed population.

No failures were observed for the devices stressed for 80 hours and 285 hours. (The failure criterion was defined as a change of ≥ 20% in the breakdown voltage.) Only four of 35 devices stressed for 400 hours failed. No significant changes in the dc characteristics of the IMPATTs were observed. Typically, breakdown voltage changes were < 8% with a slight softening of the breakdown characteristic. In addition, 15 devices from lot 79III were stressed for 100 hours at 475°C (equivalent to 1600 hours at 400°C); only three failures occurred.

Table 8 shows the rf performance results for all devices tested that had been temperature stressed at 400°C for 400 hours (Group III) and at 475°C for 100 hours (Groups VII and VIII). The efficiencies and output powers are typical of those obtained from unstressed devices. Some of these devices were purposely not etched after mounting (as is usual); this indicates that the temperature stress is not detrimental to the mesa periphery.

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Table 8

Microwave Test Results of Temperature-Stressed Diodes

(Lot 79III)

Diode No.	V_R at 10 mA (Volts)		P_{rf} (W)	η (%)	f (GHz)	Comments
	Before TS	After TS				
III – 11	28.5	31.5	-	-	-	Mesa broken in bonding
10	27	28	1.05	17.4	15.1	-
9	25	26	0.82	20.1	15.0	-
8	23.5	24.5	1.40	21.5	15.6	-
7	22	22	1.40	20.9	15.7	-
6	19.6	20.5	1.30	21.0	15.1	-
5	17.2	17.8	-	-	-	Failed at 600 mW output
VII – 7	21.0	7.0	-	-	-	Failed unit; original characteristic not recoverable by etching
6	21	19.6	-	-	-	Failed because of very poor R_θ
VIII – 8	24.5	24.5	0.24	6.9	14.7	Very poor R_θ
7	24.5	19.5	1.70	16.8	15.0	Maximum power obtained
			1.40	20.1	15.7	Maximum η obtained

No failure analysis of the failed devices was made. However, one failure (VII-7) had been profiled before stress. After stress, the impurity profile was completely altered, suggesting that the barrier metallization for this device was defective. The original breakdown characteristic was not recoverable by repeated etching of the mesa periphery.

Our conclusions from this experiment are as follow. (1) The barrier metal is stable and effectively counteracts any deleterious metallic and metal/semiconductor interdiffusion. (2) A high temperature nitrogen ambient is not deleterious to the mesa periphery. (3) A back contact barrier metal is not required to inhibit Au diffusion from the back contact for the 12 μm high mesas typically fabricated. (4) An MTTF $> 1.8 \times 10^8$ hours is predicted for a junction temperature of 200°C.

D. Non-Rf Bias-Temperature Stress Test

A life test station to bias-temperature stress (BTS) IMPATTs under non-oscillating conditions was fabricated. Each diode's bias current could be separately controlled. To protect against large input power when failure occurs, bias shutdown protection was provided for each diode; this allows the diodes to be subjected to failure analysis. The heat sink temperature and each diode's voltage were monitored by a multichannel strip chart recorder.

Seven IMPATTs from lot 77III were employed in this test. The devices were biased to dissipate the same amount of power dissipated as when the devices were operated in the waveguide cavity at the peak efficiency point. The heat sink temperature was varied between 103°C and 166°C during the test duration of 360 hours.

All but one of the devices failed at the completion of the test. The time-to-failure of each device, including the equivalent time accumulated by the

device that did not fail, is shown on a log-normal plot is Figure 36. Each failure is plotted at the mid-point of its interval. The straight line is fitted to the data by linear regression, resulting in an MTTF of 7.6×10^6 hours. A t-test result of 7.65 is obtained, indicating a 99.9% level of certainty that the data are correlated and have a log-normal distribution.

No changes in the rf or dc characteristics were observed when the devices were periodically rf tested. It is worth noting that the device operating voltage was relatively constant during most of the test. For some devices this voltage began to increase more rapidly a few hours before failure; in these cases it is believed that this increase was due to an increase of the devices' thermal impedance. All failed devices were uncapped and recovered by a slight mesa etch. The efficiencies of the recovered diodes were measured and found to be essentially unchanged by the life test. It is concluded that the predominant failure mechanism for the devices of this test is related to surface rather than bulk effects.

E. Rf Bias-Temperature Stress Test

A preliminary rf BTS test was conducted. Seven packaged devices were individually step-stressed in a waveguide cavity to heat sink temperatures as high as 185°C. Data analysis resulted in an MTTF of 9×10^5 hours for T_j(ref) = 200°C. Examination under high power microscopy did not reveal the cause of failure; as before, failures were recovered with a slight mesa etch. The probable cause of these failures was traced to the lubricant of the micrometer controlling the sliding short. Accordingly, a more elaborate test was undertaken to remove this extraneous factor of a contaminated ambient.

Figure 37 shows various perspectives of the life test station employed for this experiment. A power supply delivered bias to a distribution system with controls to adjust each diode's bias current. To protect against large input

85
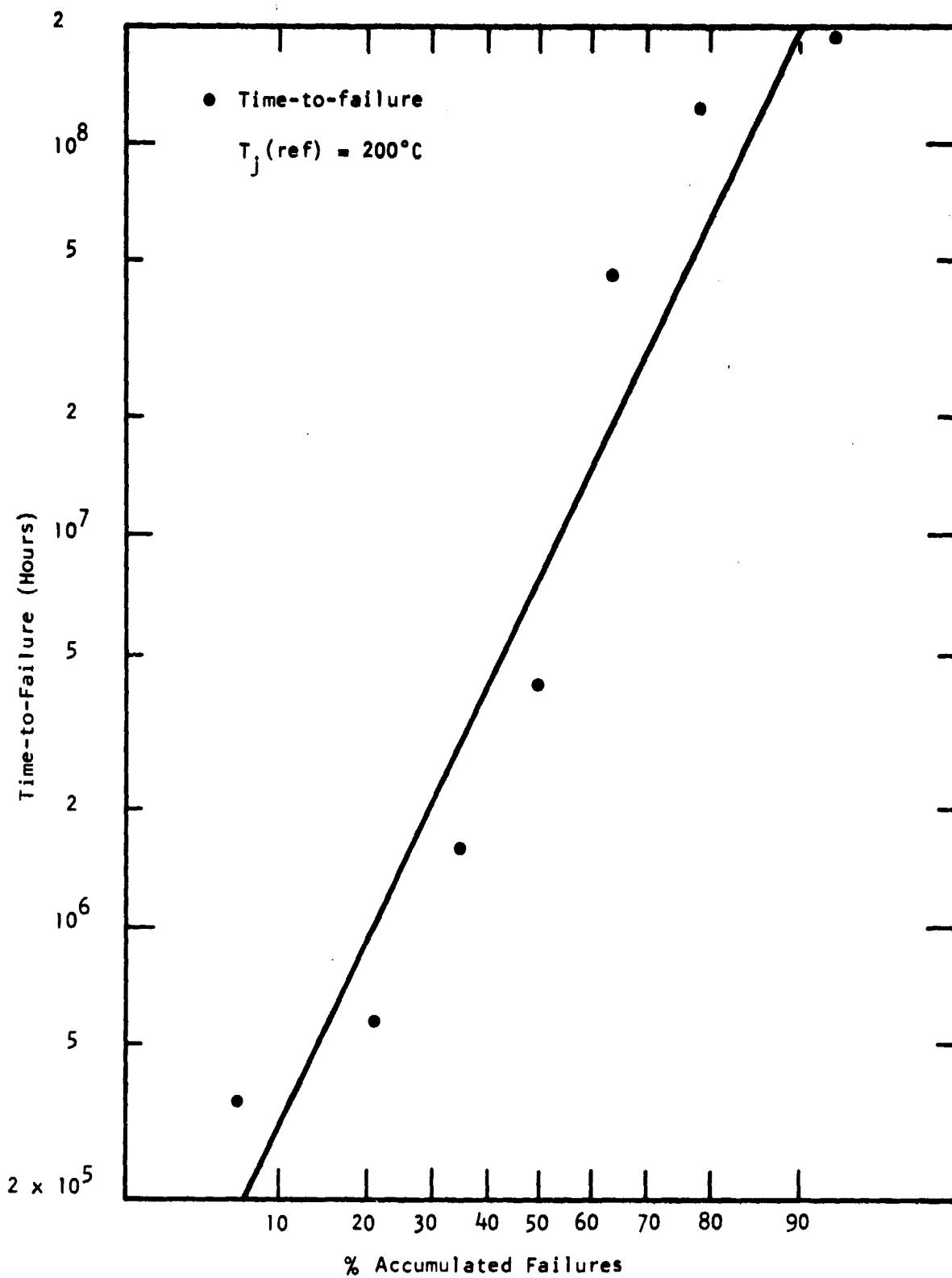
Figure 36 Results of Bias-Temperature Stress Under Non-Oscillating
Conditions
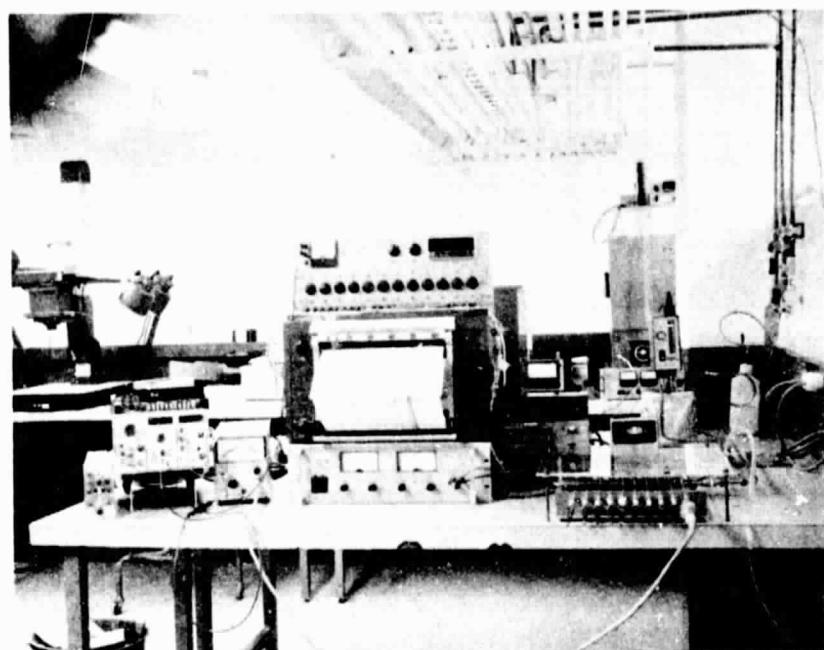
(a)
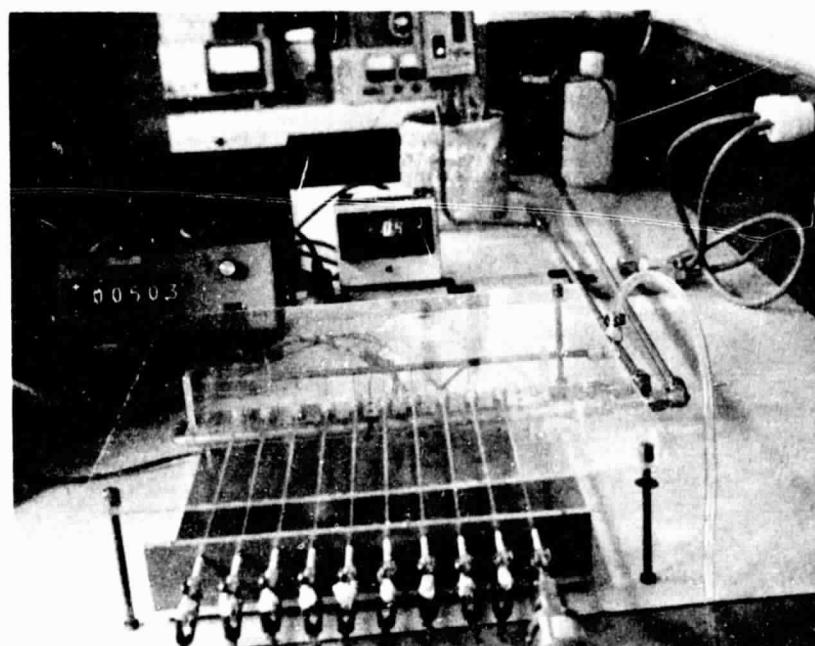
(b)

Figure 37 Photographs of Rf Life-Test Station

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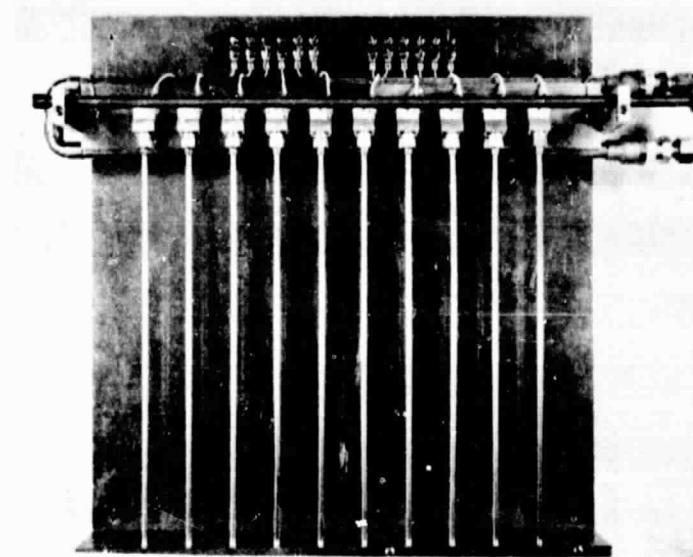
(c)
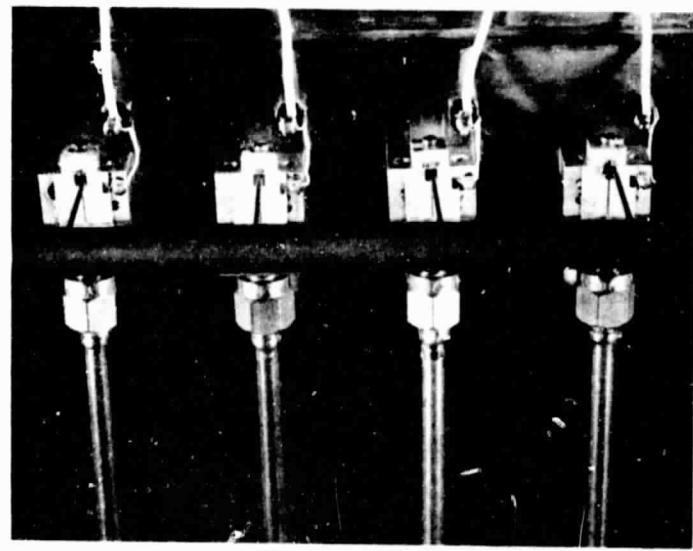
(d)

Figure 37   (Continued)

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power when failure occurs, bias shutdown protection was provided for each diode; this permits the diodes to be subjected to failure analysis. A 25 Ω series resistor is placed in close proximity to each diode to suppress oscillation in the long bias leads. The heat sink temperature and the voltage of each diode were monitored by a multichannel strip chart recorder.

A low velocity, dry N_2 gas stream was directed at each device to reduce the possibility of ambient contamination. An apparatus that pumps heated silicone diffusion pump oil (DC704), selected for its low vapor pressure, was connected to the heat sink. The oil bath was purposely located at a distance from the heat sink to reduce the possiblity of contamination. Further, in order to periodically characterize the devices at room temperature heat sink, the bath was provided with a cooling coil. To ensure heat sink temperature uniformity, 3/8-inch stainless-steel tubing was employed between the oil bath and heat sink. (The minimum fluid flow rate was 13 liters/hour and increased rapidly with bath temperature.) The oil bath temperature (over a 15 to 140°C range) was regulated by independent controls, resulting in a heat sink variation of ± 1°C during each stress step.

Oscillator test circuits having a configuration practically identical to that employed in the MIC amplifier application were employed. Figure 15 shows one such circuit with the OSM output connector. For operation on the life test station, a stainless-steel semi-rigid coaxial cable (RG#402U) was connected to the output OSM connector and terminated with a 20 dB attenuator pad. Thus, the attenuator was physically distant from the test circuit and experienced a room temperature ambient. The output power was monitored simply by connecting a power meter to the output of the attenuator.

Ten oscillator test circuits, using IMPATTs from lot 79III, were employed in this investigation. These oscillators were subjected to five stress steps

of 500 hours each at heat sink temperatures of 25, 50, 75, 100, and 125°C. At all times, the operating bias was adjusted to obtain maximum output power from each oscillator. The operating voltage, current, and rf output were periodically recorded. At the end of each stress step, dc and rf character-izations were made with the heat sink at room temperature; in addition, the thermal impedance was remeasured.

Before the results of this investigation are detailed, it is important to discuss the temperature behavior of these oscillators. Table 9 shows this behavior for an unstressed oscillator. The data show that as the heat sink temperature was increased, the output power and efficiency decreased appreciably. These were then improved by retuning the oscillator while the heat sink was at elevated temperature. When the heat sink temperature was decreased, the output power and efficiency increased slightly but were significantly lower than those obtained under the original circuit configuration. Upon retuning at the lower heat sink temperature, the original oscillator characteristics were recovered.

These same features were exhibited by the oscillators under life test. In addition, the IMPATTs showed gradual changes in electrical characteristics under continued stress. This combination of high heat sink temperature and gradual changes in device characteristics resulted sometimes in the IMPATT of the oscillator having a lower junction temperature at higher heat sink temperature and vice versa. The only practical remedy was to chip-tune the oscillators at elevated heat sink temperature. There was appreciable risk of ruining some of the oscillators during this chip-tuning operation. It was performed shortly after the start of the 100°C stress step, however, since by that time the oscillators had accumulated a considerable amount of time and hence such failures would not be catastrophic to the experiment. Four oscillators failed as a result of the chip-tuning procedure.

Table 9

Temperature Behavior of an MIC Mounted IMPATT Oscillator

Comments	Chip Retuned?	T_{HS} (°C)	V_o (V)	I_o^* (mA)	P_o (dBm)	η (%)	f (GHz)
Initial condition; chip tuned for max P_o	Yes	43	36.0	300	32.8	17.6	15.37
T_{HS} increased	No	100	38.0	195	29.0	10.7	15.23
Chip retuned	Yes	100	36.1	305	31.6	13.1	14.10
T_{HS} increased	No	125	36.7	270	30.8	12.1	14.10
Chip retuned, no change except for frequency	Yes	125	36.7	270	30.8	12.1	14.70
T_{HS} decreased	No	46	33.7	320	31.4	12.8	14.70
Chip retuned	Yes	43	34.0	300	32.3**	16.7	15.05

* For each condition, I_o adjusted for maximum output power.

** The 0.5 dB difference in P_o is due to the inability of exactly placing the tuning chip at the site it occupied at start of the experiment.

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Shortly after the start of the life test, two oscillators failed. One failed after three hours and can be considered an infant failure. The second failed due to detuning; it operated in this condition for 60 hours and with a dissipated power of 11.9 W before failing. These units were replaced and are denoted with an "A" to distinguish them from the original units.

The oscillators were completely characterized at the start of the life test; the most pertinent data are summarized in Table 10. Table 11 shows the history of oscillator #8 through the life test cycle; its behavior was representative of that exhibited by the other oscillators. Note that its spectrum when measured during the 75°C stress step was unchanged from that initially obtained; this was also true of the other oscillators.

The most important feature of Table 11 is that the IMPATT characteristics change gradually with time. This was especially evident from the thermal impedance measurements made after the completion of each stress step. Although R_θ was essentially unchanged in the course of the experiment (as anticipated, because the thermal circuit is not expected to change), the quantities V, dV/dI (T_1), etc. that were used to calculate R_θ did change significantly. The effect of the gradual change in IMPATT characteristics is readily seen from the data upon completion of the 100°C stress step. Without the tuning chip, the circuit reverts to its original configuration, and significantly lower output power is obtained; with chip tuning, the power level obtained at the start of the test is restored. The necessity for optimization of the device-circuit interaction is further verification of the gradual change that takes place in the IMPATT.

The observed change in IMPATT characteristics may be caused by defect motion in the junction region and/or by a very slow reaction (though much slower than the Pt/GaAs reaction) at the intermetallic/GaAs interface. These processes may be assisted by the presence of hot carriers, since the change in breakdown voltage

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Table 10

IMPATT Oscillators for Reliability Life Test

Oscillator No.	Reverse Voltage at 10 mA (V)	Operating Voltage (V)	Operating Current (mA)	Rf Power (dBm)	η (%)	Frequency (GHz)	Diode Diameter (μm)	R_θ (°C/W)
1	15.5	27.1	287	30.0	13.2	15.00	135	38.6
2	16.0	28.6	227	27.3	11.8	15.15	90	-
2A	19.0	30.9	175	30.2	19.0	16.56	105	58.9
3	16.7	29.8	288	28.0	8.0	14.95	100	48.5
4	17.8	31.5	239	30.4	15.1	15.10	120	43.7
5	14.2	26.6	250	30.1	17.0	16.95	105	48.1
6	13.1	24.0	357	28.0	8.5	15.35	95	-
6A	15.8	26.6	220	30.5	19.8	17.02	100	41.8
7	17.3	29.5	251	30.1	16.3	16.70	-	47.5
8	16.5	28.6	317	31.0	15.0	15.40	110	38.2
9	15.5	28.2	311	29.7	12.2	15.12	105	42.6
10	14.7	26.3	301	31.2	15.0	16.53	120	42.9

Table 11

Behavior of Oscillator #8 During rf BTS Life Test

Stress Step (°C)	V_o (V)	I_o (mA)	P (rf)	η (%)	V_B * (V)	R_θ Measured (°C/W)	Comments
25	28.6	317	1.32	15.0	16.10	-	
	29.0	253	1.35	18.4	17.42	38.2	
50	30.1	238	1.32	18.4	-	-	
	30.7	223	1.32	19.3	18.48	39.1	
75	32.6	209	1.29	18.9	-	-	Clean 15.45 GHz spectrum
	32.2	187	1.32	21.9	19.35	37.4	
100	35.6	126	0.45	10.2	-	-	w/o chip tuning
	34.2	158	0.94	17.5	-	-	Chip tuned
	32.1	144	0.77	16.6	-	-	w/o tuning chip
	32.4	223	1.32	18.3	20.29	38.1	Chip tuned
125	37.1	104	0.30	7.7	-	-	
	33.1	144	0.80	16.9	-	-	w/o tuning chip
	33.2	231	1.32	17.2	20.95	34.5	Chip tuning

*   Zero Current Intercept

Notes: First line(s) denotes results under stress temperature at start of step.

Second line(s) denotes results with heat sink at room temperature at completion of the stress step.

of the temperature stressed diodes (See Section IV.C) was significantly less than that encountered in this experiment, even though much greater temperature stress was applied in the former case. Most of the oscillators accumulated considerably more than 10^5 hours before the change in IMPATT characteristics required chip tuning; this statement is based on the dependence of the life-test acceleration factor on junction temperature. If, on the other hand, the presence of hot carriers is primarily responsible for the change in IMPATT characteristics, then the statement is invalid. Although the data base does not clearly establish whether the dominant driving force that limits device reliability is temperature or bias current, it does strongly suggest that bias current effects are dominant.

Finally, it is important to note that IMPATTs in the delivered amplifier will exhibit the same gradual change in their characteristics as observed in the oscillators. Further, until the dominant mechanism for the change in IMPATT characteristics is identified, it is not possible to predict the MTTF for the amplifier.

Assuming temperature to be the cause of the dominant failure mechanism, Table 12 shows the equivalent time accumulated by each IMPATT. On completion of the test, two devices had failed normally, four failed while the oscillators were undergoing chip-tuning at elevated temperatures, and four had not failed. Assuming they had all failed normally by the end of the test, the time-to-"failure" is plotted on log-normal graph paper as shown in Figure 38. The "failures" are plotted at the end of each interval, and all data are included to provide the most conservative MTTF for the data. As before, linear regression is used to fit the data. An MTTF of 5.5 x 10^5 hours is obtained. A t-test result of 8.08 is obtained, indicating a level of certainty > 99.9% that the data are correlated and have a log-normal distribution.

Figure 39 shows SEM photographs of two IMPATT failures (by shorting) as removed from the life-test station. Note the bevel on the mesa surface; this desirable

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Table 12

Equivalent Time Accumulated by Each IMPATT

Oscillator No.	Equivalent Time* (hrs)	Status	Failure Analysis
1	7.1×10^5	Failed--short	Mesa short with strap removed. Recovered with mesa etch.
2A	4.5×10^5	Tuning induced failure--short	Mesa short with strap removed. Recovered with mesa etch.
3	2.9×10^6	Tuning induced failure--short	Oscillator ok when removed from heat sink.
4	2.0×10^6	Failed--short	Mesa short with strap removed. Over-etched.
5	5.4×10^4	Tuning-induced failure--open	Strap separated from mesa top; mesa is ok.
6A	5.7×10^4	Not failed	
7	5.5×10^5	Not failed	
8	1.0×10^6	Not failed	
9	6.5×10^6	Tuning-induced failure--open	Bias line open; mesa is ok.
10	2.5×10^6	Not failed	

*Referenced to T_j (ref) = 200°C
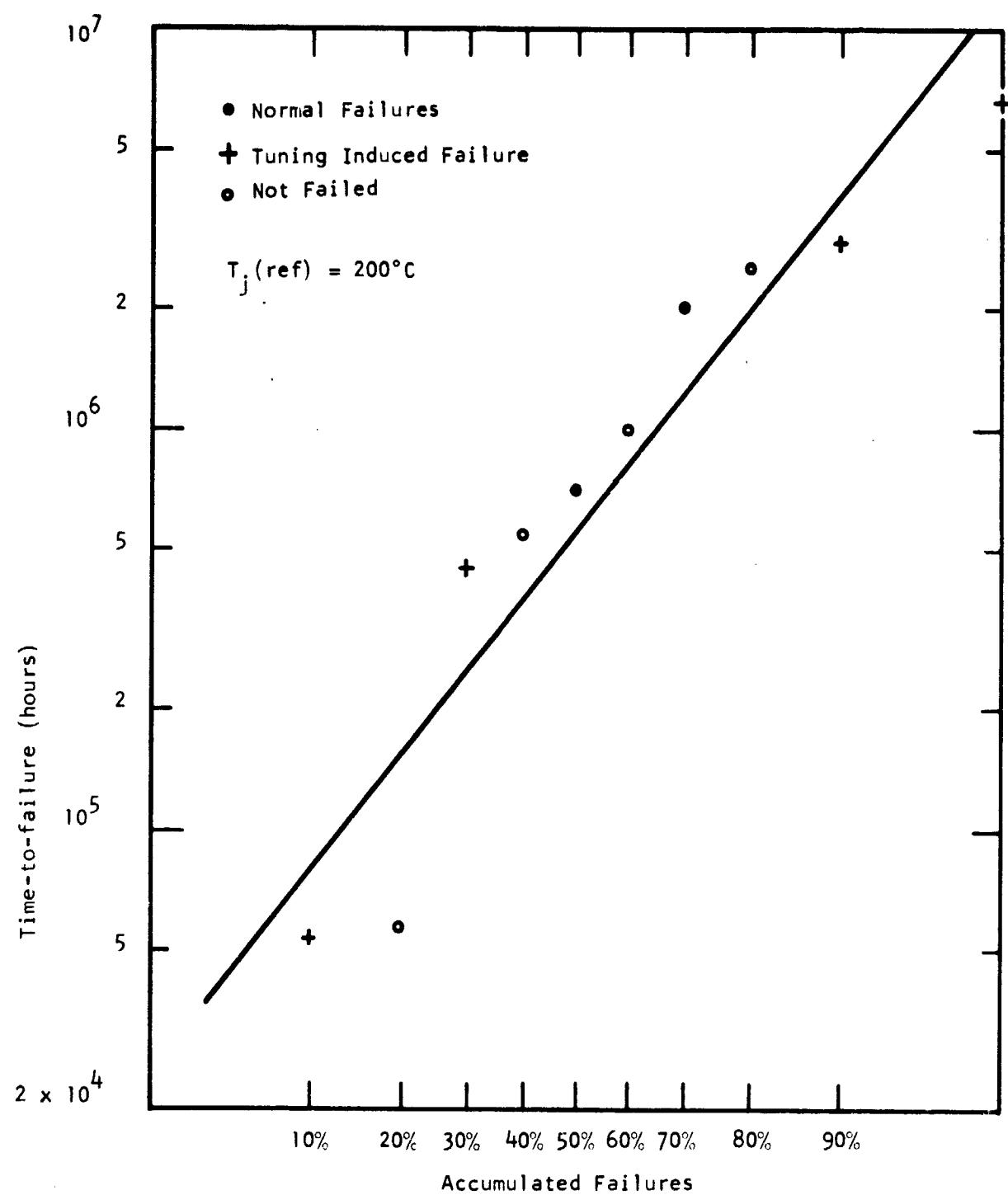
Figure 38   Results of Rf Bias-Temperature Stress Life Test
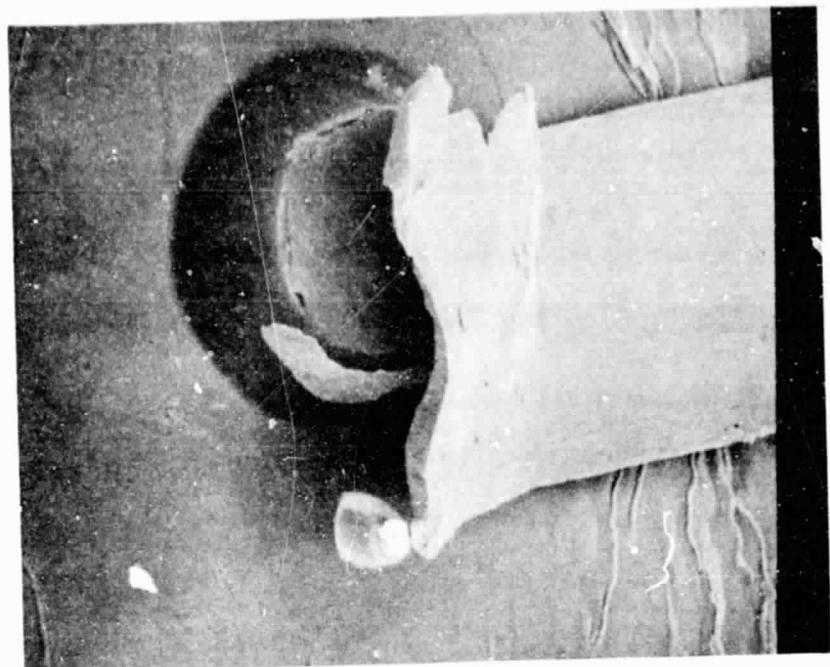
500X at 20°
(a)
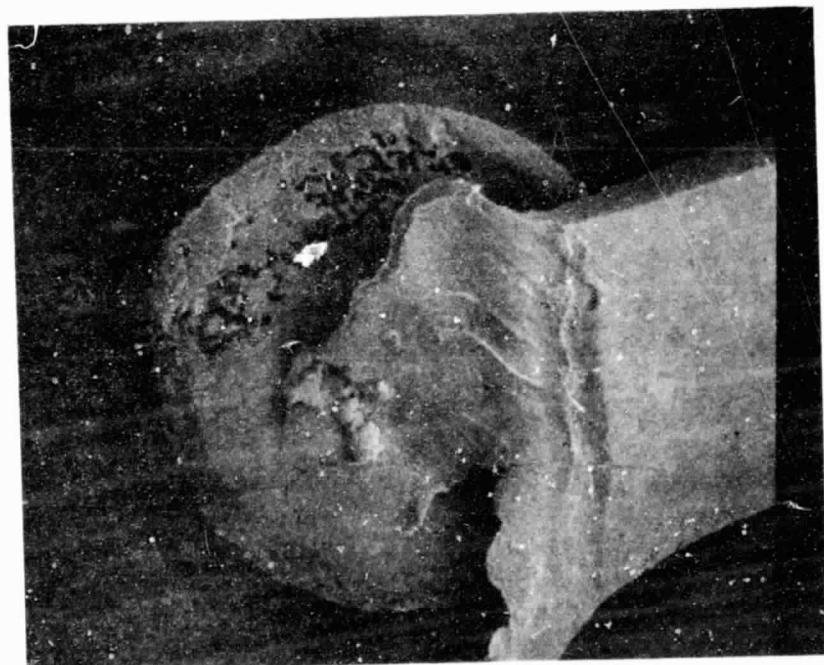
850X at 0°
(b)

Figure 39 SEM Photographs of Failed Oscillator IMPATTs

feature is purposely intended to reduce the surface electric field, thereby improving reliability. It appeared from the SEM analysis that the straps to the IMPATTs were shorting to the heat sink. Upon removal of the straps, both devices were still shorted. In the vicinity of where the strap leads away to the MIC circuit, a discoloration typical of electric discharge was observed at the vicinity of each device. It is not known if this was caused by the strap shorting, thereby causing the IMPATT to fail. It should be noted, however, that in preparation of such circuits the mesa top is purposely arranged to be a few mils below the MIC circuit with the strap slanting upward and away from the heat sink; see Figure 15.

Table 12 shows the results of failure analysis. Only three of the IMPATTs were shorted; the other mesas had not failed. Two of the shorted devices recovered to their original characteristics by slight etches ($\leq$ 10 μm) of the mesa peripheries; the other was inadvertently over-etched. As before, this suggests that device failure is surface rather than bulk-related.

SECTION V
CONCLUSIONS AND RECOMMENDATIONS

The single most important factor in the realization of high-efficiency LHL IMPATTs for this program has been the construction of the idealized model. The design window obtained from this model resulted in the specification of the material parameters. Material characterization was then employed to identify those slices capable of producing high efficiency devices. The model was also very useful during device fabrication; for each slice with particular values of N_D and Q, the optimum value of X_p was determined and implemented by anodic thinning during fabrication. As a result, slices with $\sim$ 16% efficiencies were routinely fabricated, while slices exhibiting efficiencies $\geq$ 20% were obtained from $\sim$ 25% of the slices processed.

The principal difficulty encountered in the production of high-efficiency IMPATTs in this program was related to material fabrication. The present material fabrication technology results in considerable scatter in the more important material parameters. Accordingly, considerable effort was directed toward material characterization to identify the useful material; about 15% of the slices characterized were considered suitable for further processing. This, together with material nonuniformity across the slice, makes high efficiency IMPATT fabrication a time-intensive, and therefore a costly, process. However, once an appropriate slice is identified, fabrication of high-efficiency IMPATTs from the slice is relatively straightforward.

A reliable and accurate technique for measuring the thermal impedance of the IMPATTs, based on reverse bias characteristics, has been established. Its veracity was demonstrated by comparison of thermal impedance measurements using different techniques. An important feature of the technique is that it can be employed while the IMPATT is embedded within the circuit of intended use. The thermal impedances of the IMPATTs fabricated under this program have generally

been greater than anticipated. The cause was traced to heat sink "tearing" during the sawing operation, which resulted in smaller heat sinks than intended. Fortunately, readily implemented countermeasures are available to correct this problem; such measures were not undertaken because the problem was discovered toward the end of the program.

High efficiency GaAs IMPATTs with low-high-low impurity profiles and high reliability Pt/TiW/Pt/Au metallizations were subjected to three different stress conditions. Temperature stress, non-rf bias-temperature stress, and rf bias-temperature stress tests were conducted. Assuming temperature to be the cause of the dominant failure mechanism, a mean-time-to-failure greater than 5×10^5 hours is indicated by the stress tests. However, under rf bias-temperature stress, the IMPATT characteristics were observed to change gradually with time. Such changes are not believed to be significant when the device can be periodically retuned. However, when the rf circuit is fixed, such changes can result in a significant degradation in the output power because of less than optimum device/circuit interaction.

The observed change in IMPATT characteristics may be due to defect motion in the junction region and/or due to a very slow intermetallic/GaAs reaction at the interface. These processes may be assisted by the presence of hot carriers. Although the data base does not clearly establish whether the dominant driving force that limits device reliability is temperature or bias current, it does strongly suggest that bias current effects are dominant.

To determine which mechanism is dominant, further reliability work is recommended. One possible experiment for such work is suggested: Ten MIC oscillators that have near-ideal thermal impedances and are capable of withstanding a temperature stress of ~ 300°C would be prepared. They would be thoroughly dc and rf characterized and the thermal impedances measured. These oscillators would then be temperature stressed for a total of 500 hours at 300°C (which corresponds to 5×10^5 hours at 200°C), with the recharacterizations repeated at 100, 200,

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and 500 hours. In the second half of the experiment the oscillators would be biased to operate at maximum output power with a room temperature heat sink $(T_J \cong 200°C)$ for 5×10^3 hours. If larger changes in the IMPATT characteristics should be observed in the second part of the experiment, then, clearly the effects of applied bias dominate.

The realization of the 15 GHz, 4 W, 56 dB gain microstrip amplifier using GaAs FETs and IMPATT diodes demonstrates the feasibility of utilizing both devices in an integrated power amplifier, thereby taking advantage of the unique characteristics of each. The FET preamplifier offers the advantage of simpler, more cost-effective circuitry (no circulators are required); more gain stability with changes in ambient temperature; and truly stable amplifier operation at zero rf drive. The IMPATT devices operating in the injection-locked oscillator (ILO) mode provide output powers in excess of 1 W in Ku-band, with good efficiency and high reliability.

Although the 5 W goal was not achieved, several important features and performance goals were realized in the 4 W delivered amplifier. Some of these surpassed the performance requirements listed in Table 1. Over the specified frequency band of 15 GHz ± 125 MHz the bandpass ripple is less than ± 0.25 dB at each ambient test temperature of 0°, 25°, and 50°C. At an input level of - 30 dBm the gain of the amplifier is 66 dB, while at - 20 dBm a gain of 56 dB is achieved. The rate of change of the gain with frequency is less than 0.1 dB/10 MHz within the specified frequency band for all three ambient test temperatures. The amplifier operates from 39 V, 6 V, and -1 V dc power suppliers. Dc-to-rf efficiency, including all bias circuit losses, is 10.8%. No spurious signals were observed in the specified operating bandwidth within 50 dB of the carrier signal. Third-order intermodulation measurements, however, revealed third-order products within 8 to 10 dB of the two equal-magnitude carrier signals ($\Delta f = 10$ MHz) at a total output power of 4 W. This distortion is due primarily to the large signal, nonlinear operation of the IMPATT stages. The amplifier weighs 444 grams and occupies a volume of 220 cm^3.

Recommendations for future work include replacing the IMPATT driver stage with an all-FET amplifier. This would eliminate all circulators and ferrite material from the spacecraft transmitter. To reduce gain ripple, retain driver amplifier isolation, and achieve better linearity, a balanced FET amplifier using 3 dB quadrature hybrids would be appropriate. A three-stage FET driver yielding a 1 dB gain compression point of 32 dBm at an associated gain of 12 dB is now feasible using presently available 1 W FET devices at 15 GHz. This is contingent upon demonstrating the required reliability of these devices. To achieve a 5 W IMPATT power output stage repeatably, a higher yield of single-mesa diodes capable of output powers of at least 2 W when tested in free-running microstrip oscillator circuits must be realized.

ACKNOWLEDGEMENTS

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