REPORT NO: FR-80-76-10C
HAC REF NO. E1476

QUANTITATIVE OPTICAL SCANNING TESTS OF COMPLEX MICROCIRCUITS

FINAL REPORT — FEBRUARY 1978 THROUGH JANUARY 1980

J. J. ERICKSON

MARCH 1980

Prepared under Contract No. NAS8-32665
Components Laboratory
Technology Support Division

AEROSPACE GROUPS

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Marshall Space Flight Center, Alabama 35812

QUANTITATIVE OPTICAL SCANNING TESTS OF COMPLEX MICROCIRCUITS

FINAL REPORT – FEBRUARY 1978 THROUGH JANUARY 1980

J J ERICKSON

MARCH 1980

Prepared under Contract No. NAS8-32665
Components Laboratory
Technology Support Division

AEROSPACE GROUPS

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Marshall Space Flight Center, Alabama 35812

CONTENTS

CONTENTS (continued)

ILLUSTRATIONS

ILLUSTRATIONS (continued)

ILLUSTRATIONS (continued)

ILLUSTRATIONS (continued)

ILLUSTRATIONS (continued)

LIST OF TABLES

1.0 FOREWORD

This report is a summary of work performed on NASA Contract NAS8-32665 during the period of 7 February 1978 to 20 January 1980. The investigation was conducted for the George C. Marshall Space Flight Center, Huntsville, Alabama. The Contracting Officers Technical Representative was Mr. Leon Hamiter.

The majority of the work was performed within the Advanced Technology Laboratory of the Technology Support Division of Hughes Aircraft Company. Mr. James J. Erickson was principal investigator and program manager. Mr. R. L. Barch's help with eqiupment design and technical assistance was a valuable contribution. Mr. F. A. Lucich and Mr. D. L. Mehrle along with other personnel from the Radar Division generated the image processing software and provided the computer analyses of the photoresponse data. Mr. P. G. Backes and Mrs. J. A. Sheppard generated the computer software for the automated integrated circuit test facility used to measure the electrical parameters of the test devices for this program.

2.0 SUMMARY

The work described in this report was the third phase of a project to develop and evaluate a new nondestructive inspection and test method for microcircuits. The basis of the new method is the use of a raster-scanned optical stimulus in combination with special electrical test procedures, and computer-aided image processing techniques. The raster-scanned optical stimulus is provided by an Optical Spot Scanner, an instrument that combines a scanning optical microscope with electronic instrumentation to process and display the electrical photoresponse signal induced in a Device Under Test (DUT). The resulting photoresponse images are then processed and compared using a digital computer to implement image processing techniques.

The Optical Spot Scanner itself is not a novel idea: Its ability to detect and image flaws in semiconductor devices and to check the static logic states of internal stages of microcircuits is well known. The overall purpose of this project is to devise methods by which an Optical Spot Scanner can be used for 100% screening inspection of microcircuits. Because of the time necessary to scan a raster frame and because of the number of data points (picture elements) contained in a photoresponse image of DUT, an important prerequisite for this application is that the DUT must be adequately characterized by a single photoresponse image for the accept/reject decision. A method by which this special photoresponse image can be generated was developed in the first phase of this project. The new method was named the State Superposition Technique because of the way in which it generates the photoresponse image. The work done in the first phase was described in the final report "Imaging LSI Microcircuits with Optical Spot Scanners," dated January 1976.

The goal in the second phase was to evaluate the ability of the OSS to detect flaws in CMOS microcircuits that had failed electrical tests after a 1000 hour, powered life-test at 125^{0}C. Unlike the previously examined failed microcircuits, these specimens were functional devices that had failed one or more parametric tests. A group of microcircuits that had passed electrical screening tests after the same type of life-test were used as a control group. In brief, the results of this program showed that the Optical Spot Scanner operated in combination with the State Superposition Technique can detect effects in microcircuits that are correlated with their electrical behavior. Since the effects are localized on particular portions of the microcircuit chips, the resulting information may be of value not only for screening

inspection but also for engineering studies of CMOS microcircuits.

Localized differences in photoresponse magnitudes were readily observed among all specimens, both good and reject; however, the shapes of the photoresponse image are essentially the same for all the test specimens. A few instances of qualitative differences have been observed. Some have been tentatively attributed to parasitic elements, such as parasitic bipolar phototransistors. Also, certain photoresponses were correlated with some degraded parameters. Nevertheless, the photoresponse information that best characterizes the microcircuit test specimens is believed to be contained to a significant extent in the photoresponse magnitudes of the various active elements. It became apparent that the method of comparing photoresponses by visually comparing photographs of photoresponse images displayed on a CRT is both inefficient and ineffective. The work done in the second phase was described in the final report "Optical Scanning Tests of Complex CMOS Microcircuits", dated October 1977.

The work reported here from the third phase of this project was undertaken to further develop the OSS as a screening instrument by comparing quantitative differences in the photoresponse images. This was conceived as a result of the previous program which revealed that each test device is best characterized by the information contained in the magnitude of the photoresponse, since the overall shape of the photoresponse remains fairly constant from device to device while differences in the magnitudes are observed.

The photoresponse images generated by the optical scanner have a very high data content. In order to handle the large volume of data and determine which of these data convey the information of interest, a highly versatile, high capacity data recording and processing method was used. The method that was used was to record the photoresponse image, digitize this information and then process the data by digital image-processing techniques.

The overall approach that was used was to modify the existing optical scanner so that the photoresponse images from the test devices could be recorded on magnetic tape. Photoresponse images from two different groups of test devices were recorded before and following various life-test intervals. Electrical parameters of the test devices were also measured before and after the life-test intervals. Attempts were then made to correlate differences in the photoresponse images with differences in the electrical parameters.

Two types of differences in the photoresponse images were to be considered: the differences between images of different specimens whose electrical parameters are different, and differences between images of the same device, whose electrical parameters and photoresponse images changed significantly during the course of the life test. A principal objective of this program was to determine whether the photoresponse image obtained before the life-test contained any information that could be used to predict life-test failures. The existence of such information and the methods needed to detect it will determine the basic design of optical scanners to be used for microcircuit screening or inspection.

The results of the program showed that correlations could be made between differences in optical scanner photoresponse images of devices and differences in their electrical parameters. The most obvious correlation was made for the one test device which was a parametric failure from the first electrical test. Subtractions between this device's photoresponse image and those of devices whose electrical parameters were within specification limits revealed significant differences. The other correlations between electrical parameter differences and photoresponse image differences were made through comparisons of subtle differences in the images that resulted from the subtraction of two photoresponse images. Many of the differences that were revealed by the subtraction of two images were virtually undetectable by visual comparison of the two images which demonstrated that the new approach did provide useful information that was otherwise unobtainable.

None of the test devices electrical parameters failed or degraded due to inherent problems during life tests. Therefore, no significant correlations could be made between any failed or degraded parameters and changes in the photoresponse images from any one device. The only correlation that could be made was that there were also no large changes in the photoresponse images following the life-tests. Also, since none of the devices failed or degraded as a result of inherent defects during the life tests, the initial images could not be compared to determine if they contained information which could be used to predict subsequent device failure or degradation.

Since correlations could be made between differences in device electrical parameters and subtle differences in photoresponse images that were revealed using the new approach developed during this program, the program was successful even though all the proposed correlations could not be attempted since the device parameters did not change during the life tests. Conclusions can be

drawn from these results which are encouraging with respect to the ultimate success of the optical scanner as a screening inspection instrument using the approach developed in this program. Subtle differences in photoresponse images could be correlated with differences in electrical parameters, even though the differences in the electrical parameters were small enough so that the electrical parameters were all within specification limits. (Except for one failed test device whose photoresponse image was obviously different from other test devices' photoresponse images.) Semiconductor device physics in combination with the previous observation would predict that devices whose electrical parameters are vastly different, for example, outside of specification limits, would have photoresponse images which are quite different than the photoresponse images of devices whose electrical parameters are within specification limits. Also, if the optical scanner is to be developed into an effective screening inspection instrument, small differences between devices' electrical parameters which are within specification limits should not have a large effect on the photoresponse image which would be used as a basis for an accept/reject decision. The results of this program showed that the new approach of performing quantitative analysis of the photoresponse images does not conflict with this requirement. Acceptable variations in device electrical parameters produced only subtle changes in the resulting photoresponse images.

3.0 INTRODUCTION

In recent years the growing complexity and density of microcircuits has greatly increased the difficulty of inspecting and testing them. Since the reliability requirements of space and airborne systems can be met only by 100 percent inspection and testing procedures, more efficient and effective testing and inspection methods are necessary. One prospective technique for fulfilling this need is inspection with an Optical Spot Scanner.

The Optical Spot Scanner (OSS) is an instrument that scans a focused spot of light in a raster pattern over a specimen. The electrical photoresponse signal and the reflected light signal are displayed on CRT displays. In fact, the OSS can be thought of as a Scanning Optical Microscope that is closely analogous to the Scanning Electron Microscope (SEM) operated in the Electron Beam Induced Current (EBIC) and secondary electron emission modes. However, unlike the SEM, the OSS is completely nondestructive, does not require a vacuum chamber for the test specimen, and can provide a significantly higher beam-induced signal level (by several orders of magnitude, if necessary). Research experience with the optical scanner has already established that it can detect certain important types of flaws in simple semiconductor devices. Some of these flaws cannot be detected by visual inspection or by conventional electrical tests. In microcircuits, the OSS generates a photoresponse pattern or image that depends on the circuit's digital state. In effect, the OSS can thereby monitor directly the internal operation of microcircuits. Because of the buffering effect of each succeeding state on the preceding stages of a digital microcircuit, direct monitoring of the internal operation of the circuit cannot be done by conventional electrical measurements at the external terminals.

These potential capabilities - to nondestructively monitor the internal operation of digital microcircuits and to detect and localize otherwise undetectable flaws - would make the OSS a very effective inspection instru-

ment for 100 percent screening inspection and also for engineering studies of microcircuits. Unfortunately, its use is made difficult by the complexity of the digital microcircuits themselves. For screening inspection it must be assumed that the photoresponse image data will be converted to digital form, processed, and compared to a reference image to make the accept/reject decision. The large amount of data contained in a single image can be handled rapidly enough by a modern computer, but a screening procedure that required scanning and processing several images per test device would not be practical. The use of the OSS for screening inspection therefore requires a method for generating a single photoresponse image that adequately characterizes the Device Under Test (DUT). This image then could be used as a "characteristic signature" for making the accept/reject decision. One obvious requirement for the image is that it should contain images of all photoresponsive circuit elements in it.

The difficulties with using a conventionally generated photoresponse image can be stated in several, essentially equivalent ways. One version is as follows: when the photoresponse image of a DUT is generated, the photoresponse signals from some of the circuit elements may not be accessible at the device's external terminals. The photoresponses may be shorted out by conductive paths in parallel with the circuit elements in question, or they may be prevented from reaching the external terminals by blocking series elements. Whatever the reason, these circuit elements will appear dark in the photoresponse image.

The work in the first phase of this contract addressed the problem of generating the required photoresponse image on the basis of the above statement of the problem. One promising approach was selected for further development after several possibilities had been investigated. The successful implementation of a method based on this approach was mainly the result of an improved understanding of the problem. As stated above, the difficulty is that the photoresponses from some of the circuit elements are externally inaccessible, so these circuit elements do not appear in the photoresponse image. However, which circuit elements appear and which do not is determined by the DUT's digital state. Indeed, it is the pattern of light and dark circuit elements in the photoresponse image that characterize the DUT's digital state. By analyzing this pattern it is possible to determine the state of internal circuit stages that are not accessible to measurement via the device's

external terminals. The difficulty of imaging all circuit elements in one photoresponse image is not that the photoresponses from some elements are inaccessible, but that the DUT is being examined in a single digital state. It can be assumed that if the set of photoresponse images of all possible states of the DUT were examined, any given circuit element would appear at least once in the set. In fact, for a complex microcircuit, a set of images containing each circuit element in at least one image would be a small subset of the set of all possible images. Disregarding the problems of implementation, one possible approach for generating the required "characteristic signature" image is to form an appropriately weighted superposition or average of a subset of images having each circuit element in at least one image. The method that was developed in the first phase of this work is an implementation of this approach. Because of the way in which it generates the "characteristic signature" image, the new method was named the State Superposition Technique.

Following a demonstration of the State Superposition Technique in the first phase of this effort, a second phase of the project was undertaken in order to investigate the effectiveness of the new technique in detecting flaws in microcircuit specimens. Since the initial demonstration had shown that the Optical Spot Scanner was particularly well suited to CMOS microcircuit inspection, this second phase consisted of a project to examine good and failed CMOS microcircuits with the State Superposition Technique and to correlate the photoresponse images with the electrical behavior. Twenty specimens of each of two CMOS part types were supplied by NASA MSFC. The specimens had undergone a 1000 hour 125^{0}C life-test, after which they had been tested according to tentative MIL-M-38510 specifications for the part types. The twenty specimens of each type included a group of ten reject microcircuits that had failed power supply current tests and a control group of ten good microcircuits.

For various reasons that made this approach more productive, emphasis in the laboratory work was placed on one of the two part types. In addition to a survey of State Superposition photoresponse images under conditions of normal operation, experiments were planned and carried out on this part type to detect effects whose presence was implied by results of electrical tests. Tests at high clock frequencies showed the Optical Spot Scanner's ability to localize the stages that malfunctioned at high frequency. These tests also disclosed the unexpected acti-

vation of parasitic bipolar structures that amplified the optically injected photocurrents. Experiments were also done to measure a length parameter describing the dependence of a junction's photocurrent on the distance from the junction to the focused optical spot. While not entirely conclusive, the experimental results strongly suggest that large values of the length parameter are a necessary condition for low leakage currents in the test specimens.

The laboratory work on the second part type was restricted to State Superposition image surveys at two values of power supply voltage. At the lower voltage the test specimens were operated near their upper frequency limits. A fairly consistent pattern of bipolar parasitics was detected in all the specimens. The parasitics appeared to involve diffused conductors and diodes, and also p-channel FET's in transmission gates. Some major differences between photoresponse images for different test specimens were noted, but they could not be readily correlated to the electrical test data for these specimens.

In brief, the results of this program showed that the Optical Spot Scanner operated in combination with the State Superposition Technique can detect effects in microcircuits that are correlated with their electrical behavior. Since the effects are localized on particular portions of the microcircuit chips, the resulting information may be of value not only for screening inspection but also for engineering studies of CMOS microcircuits. However, the results of this study led to the conclusion that the information provided by the photoresponse data that best characterizes the microcircuit is contained mainly in the magnitude of the photoresponse from the various active elements. Small changes in photoresponse magnitude can not be detected by visual comparisons of photographs of CRT photoresponse images which was the comparison method used. Even qualitative changes were shown to be very difficult to keep track of by visual comparisons alone, especially on complex devices.

As a result of the previous studies, the work reported here was undertaken to perform quantitative comparisons of the photoresponse images generated from the examination of the test devices by the optical scanner using the State Superposition Technique. Briefly, the tasks for this program consisted of modifying the existing optical scanner so that the photoresponse images could be recorded, digitizing the recorded data and analyzing the data using image

processing techniques. Photoresponse images and electrical parameters from groups of two different device types were recorded before and after successive life-test intervals. Correlations were then made between the differences in the photoresponse images and differences in the electrical parameters. The two device types that were examined were both CMOS devices: the CD4028A BCD-to-decimal decoder and the CD4034A eight stage bus register.

The mechanism of photoresponse image formation, using a CMOS inverter as an example, is reviewed in this section for completeness. Also, the State Superposition Technique is reviewed since it is the basis for the formation of the photoresponse images which can be used to completely characterize the microcircuit. Qualitative and quantitative image analysis are also discussed in this section. Subsequent sections include the following: a description of the modified and improved optical scanner used for this work; the hardware and software used to provide image processing of the photoresponse data; laboratory work and conclusions.

3.1 Photoresponse Image Formation

When a light beam is focussed on the surface of a semiconductor, electron-hole pairs are created. In the presence of an electric field, such as is created by a p-n junction, the electrons and holes are separated, creating an electrical photoresponse. In microcircuits, the optical scanner generates a photoresponse that depends on the circuit's internal fields. These fields are, of course, directly dependent on internal biases. In effect, the optical scanner can directly monitor the internal operation of microcircuits.

A simple CMOS inverter, as shown in Figure 3-1, will be used to demonstrate how a photoresponse image is formed and interpreted.

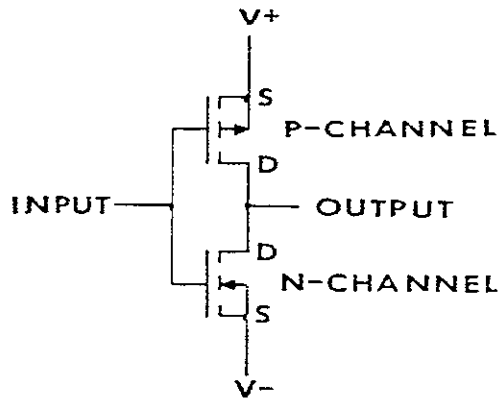

Figure 3-1. Circuit Schematic of CMOS Inverter

When the input to the inverter is "high", the n-channel FET is "on" conducting) and the p-channel FET is "off" (non-conducting). With the n-channel FET "on", the negative supply voltage (V-) is present at the drain of the n-channel FET which is the output of the inverter. Therefore there is no field across the n-channel FET. As a result, when the light beam from the optical scanner is swept across the n-channel FET, there will be no photoresponse signal.

The drain of the "off" p-channel FET is also at V- while the source is at V+. In this case, when the light beam from the optical scanner sweeps across this FET, the generated electron-hole pairs are separated by the field across this FET. This results in a photoresponse from the p-channel FET.

When the input to the inverter is "low" the p-channel FET is "on" and the n-channel FET is "off". Using the same type of analysis as for the "high" input it can be seen that there will be a photoresponse signal from the n-channel FET but there will be no signal from the p-channel FET. To generalize for either input, there is a photoresponse signal from the "off" FET while there is no signal from the "on" FET.

In CMOS circuitry, the n-channel FET's are fabricated in p-wells on the n-substrate. These p-wells are always tied to the most negative potential while the substrate is tied to the most positive potential. Therefore, the p-wells on a CMOS device always generate a photoresponse signal due to the large field between them and the substrate, regardless of the logic states on the inputs.

The previously mentioned photoresponse signal takes the form of a current which flows between V+ and V-. This signal is detected by measuring the voltage drop across a small resistor (~100Ω) inserted between the device's V- lead and the V- power supply. This voltage is then used to intensity modulate a CRT to generate a photoresponse image for the device.

An internal anomaly in a CMOS device will alter the photoresponse image in such a way that the presence of the anomaly can be inferred. For example, suppose the output of the CMOS inverter in Figure 3-1 were connected to V- through an anomalously small resistance (a short or leakage path, for example). When the input to the inverter is "high", the output would be V- and the anomaly

would have no effect. However, when the input is "low", the p-channel FET turns "on" but there is still a large potential across this FET, V+ on its source and V- on its drain. Also, the n-channel FET still has little or no potential across it. Therefore, the inverter will be imaged as if it still had a "high" input and the photoresponse images for the inverter will be the same for both inputs.

Figures 3-3 through 3-5 are photoresponse images of a CMOS inverter to demonstrate the preceding discussion. (The reflected light image of the inverter is shown in Figure 3-2). Figure 3-3 shows the photoresponse image of the inverter with a "high" input and Figure 3-4 shows the inverter with a "low" input. Figure 3-5 shows the inverter with a "low" input and a 100Ω resistor between the output and V-. It can be seen that Figure 3-5 looks like Figure 3-3 in the region of interest as anticipated.

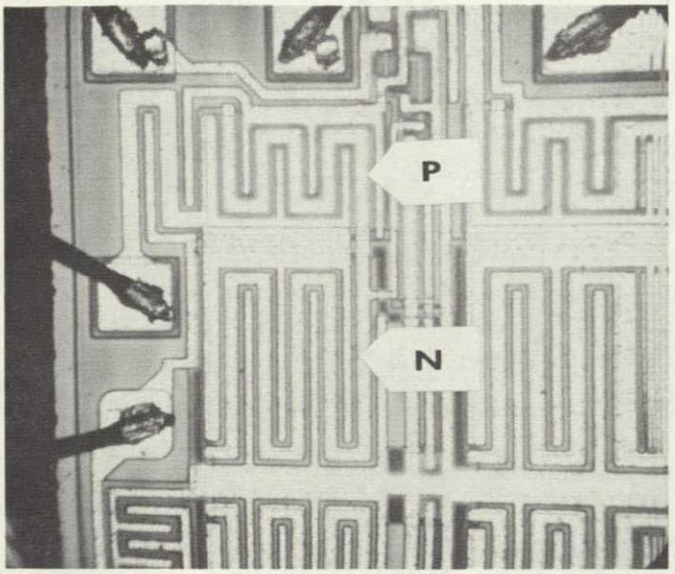

Figure 3-2 Reflected light image of a CMOS inverter on a MC14049 chip

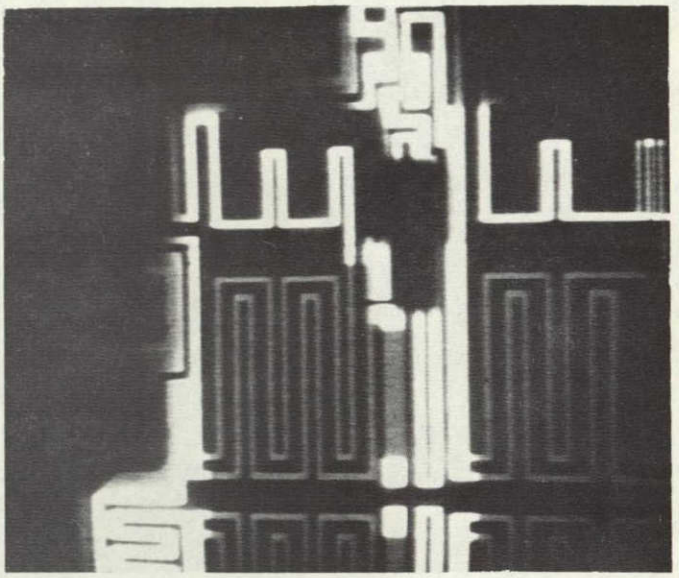

Figure 3-3 Photoresponse image of a CMOS inverter with a "high" input

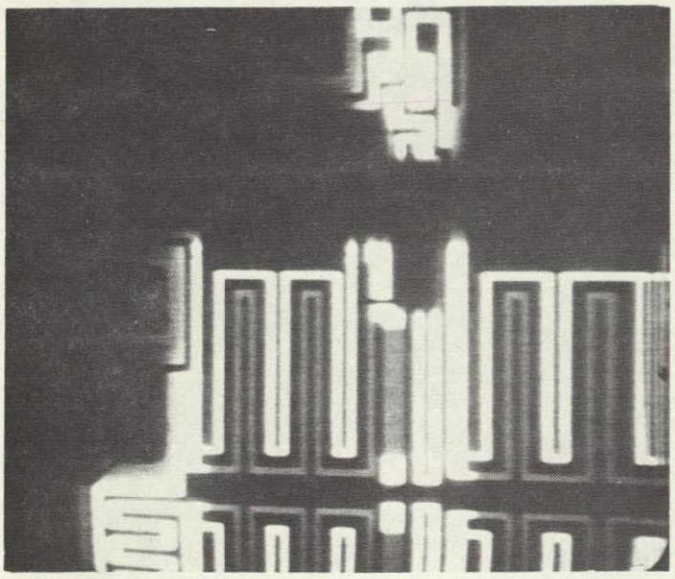

Figure 3-4 Photoresponse image of a CMOS inverter with a "low" input

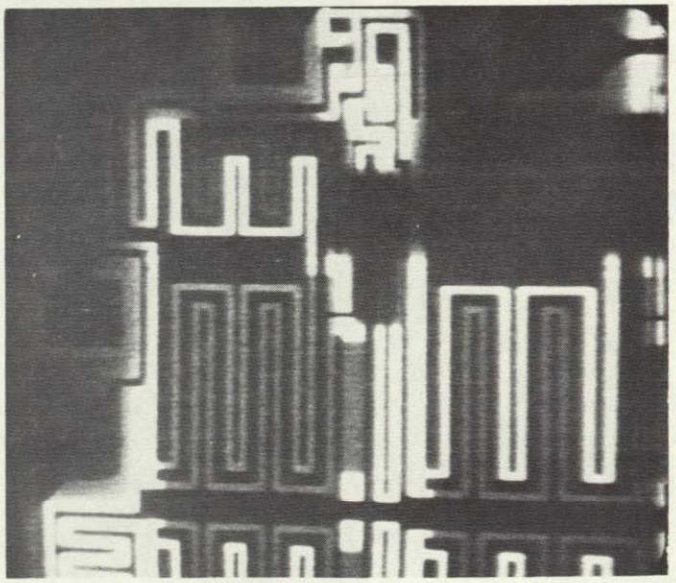

Figure 3-5 Photoresponse image of a CMOS inverter with a "low" input and a 100Ω load resistor to V-.

3.2 STATE SUPERPOSITION TECHNIQUE

As discussed previously, the objective in developing the State Superposition Technique was to generate a "characteristic signature" photoresponse image that could be used for microcircuit screening inspection. The approach is to form an appropriately weighted superposition or average of a set of images having each circuit element in at least one image.

In principle the required superposition can be effected as follows: first, a set of digital states is selected such that each circuit element appears in at least one photoresponse image corresponding to a digital state in the set. Next, a test circuit or program is devised to rapidly clock the device under test through the set of selected digital states. Then, the required superposition of images is generated by scanning the DUT with the optical scanner as it is being clocked repeatedly through the set of selected digital states.

The application of this technique to a CMOS inverter will illustrate this approach. The analysis of how the CMOS inverter's photoresponse image is formed showed that the imaged element is the "off" transistor. With a low input, the n-channel FET is imaged; with a high input, the p-channel FET is imaged. Clearly the superposition of these two images would be an image showing both FET's in the inverter. The inverter has only two states. The program that will repeatedly clock the inverter through this set of two states is an input square wave. Thus the required State Superposition image of the inverter can be obtained by scanning the DUT as it is being switched rapidly by a square-wave signal applied to the input.

This simple example of the inverter can be extended to more complex circuits, which are made by interconnecting circuit stages not much more complicated than the inverter. Instead of two possible states, a complex circuit can have a very large number of states. The problem is to choose a set of digital states that provides the desired characteristic signature image. For a given circuit this set of digital states is not unique, nor is the order in which the states occur. At a minimum, the digital state sequence will be such that every active element appears in the photoresponse image. This will happen if each active element appears in at least one of the photoresponse images that would be obtained statically for each state in the sequence.

For digital microcircuits the photoresponse is sensed at the power supply or ground terminal, where it appears superimposed on the current normally flowing through the circuit. If an attempt is made to obtain a photoresponse image of a microcircuit as it is being clocked rapidly through some sequence of states, the photoresponse signal is found to be masked by switching transients. This difficulty can be surmounted by using a light beam whose intensity is modulated at a particular frequency. The photoresponse then can be separated from the switching transients by a highly frequency-selective demodulator.

The problem of separating an optical signal from noise is well known in optical spectroscopy, where it is solved by the use of a lock-in amplifier. The basic element of the lock-in amplifier is a phase-sensitive detector in which the signal voltage is multiplied by a reference square or sine wave signal, producing sum and difference frequencies. A low-pass RC filter at the detector's output rejects the high frequency components and passes the difference frequencies of sidebands within the passband. Difference frequencies that are removed from the reference frequency by more than low-pass filter's cut-off frequency are attenuated. Thus, the filter's output is due to that portion of the signal's spectrum that lies about the reference frequency within a passband determined by the low-pass filter.

The two ideas presented here - that of rapidly clocking a microcircuit through a specially selected sequence of digital states, and then using a modulated optical beam in the optical scanner to generate a photoresponse that can be separated from the switching transients - comprise the State Superposition Technique. The photoresponse image so generated will be referred to as a State Superposition image. The sequence of digital signals applied to the microcircuit's externalleads to cause it to go through the selected sequence of digital states will be referred to as the State Superposition program.

3.3 Qualitative Image Analysis

At this point in the development of the optical scanner as a screening inspection instrument the State Superposition technique has been developed

and demonstrated to produce a "characteristic signature" photoresponse image. This image represents the electrical behavior of all the active elements on the device. The problem to be solved is how to best interpret this image in order to make a decision about the reliability of the microcircuit which produced the image.

The initial approach used to analyze these images was to perform visual comparisons of photographs of the photoresponse images displayed on CRTs. The photoresponse images were from functional devices, some of which had failed certain electrical parametric tests. It was thought that differences in devices' electrical parameters could be correlated with qualitative differences (for example, changes in overall shape) in photoresponse images. This approach would be valid in the case of devices that are malfunctional since there are some elements that generate no photoresponse. The complete absence of a portion of a photoresponse image from a malfunctioning device is very apparent when it is compared to the photoresponse image from a functional device. However, the shapes of the photoresponse images are basically the same for devices that are functional.

Some parametric failures can be correlated with changes in the shape of the photoresponse image but most will be associated with changes in magnitude of the images. Small changes in photoresponse magnitude will not be detected by visual comparisons of photographs of CRT displays on even simple microcircuits. The number of elements of a photoresponse image that have to be compared for a complex microcircuit makes the task of visual comparison of images even more difficult, if detection of variations in image brightness is the main criteria.

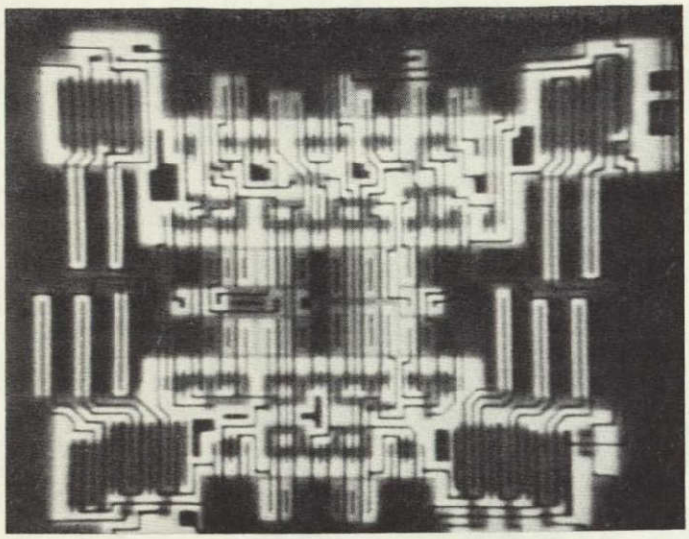

Figure 3-6. Photoresponse image of a CD4028A test device whose electrical parameters were all within specification limits.

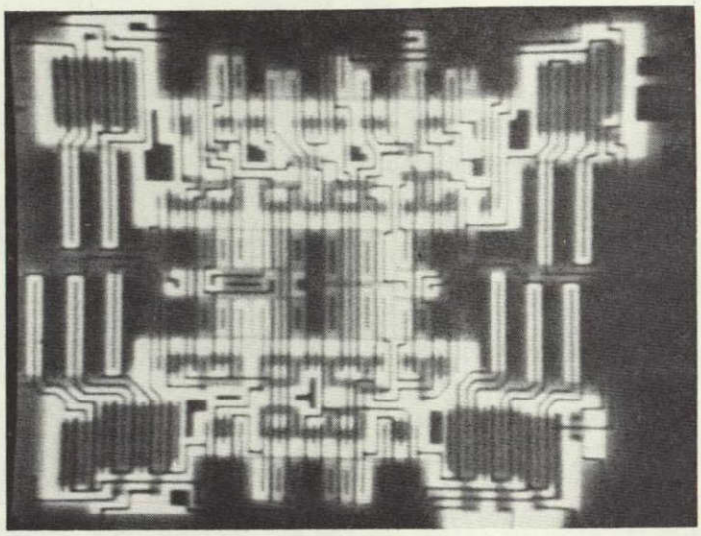

Figure 3-7. Photoresponse image of a CD4028A test device. Several of its electrical parameters were outside of specification limits.

Figure 3-6 and 3-7 are photoresponse images from two CD4028 microcircuits that were used in the preceding program "Optical Scanning Tests of Complex CMOS Microcircuits". One of the images (Figure 3-6) is from a device that passed all parametric electrical tests and the other (Figure 3-7) is from a device that failed one or more parametric electrical tests. The previous discussion of the difficulty of analyzing images by visual comparison can be better appreciated when an actual comparison is attempted between these two images. This particular device is only a MSI microcircuit. The photoresponse image from a LSI microcircuit is many times more complex.

3.4 Quantitative Image Analysis

It has been found that a defect in a microcircuit is more likely to cause a change in photoresponse magnitude rather than a change in the shape of the photoresponse image. Therefore, in order to detect defects in microcircuits, quantitative analysis of image magnitudes rather than qualitative analysis of image shapes is required. Qualitative analysis of image magnitudes by visual comparisons of images will not reveal small differences in magnitudes of the photoresponses. Also, due to the complexity of the photoresponse images from complex microcircuits this method is not very effective or efficient. For example, in the case of a device containing a hundred transistors, at least one hundred separate points must be examined in the photoresponse image and their magnitude (or brightness) compared to the magnitude of the corresponding points on another reference photoresponse image. To complete the analysis, the magnitudes of photoresponses from all other active elements also have to be compared.

The complexity and quantity of the data to be analyzed has led to the development of the instrumentation and techniques during this program to quantitatively process the data by digital image-processing techniques. In order to apply these techniques, each image was recorded on magnetic tape along with other synchronization data. This data was then processed so that each image was represented by an array of pixels (picture elements) with 512 pixels per line and 512 lines per image. The magnitude of each pixel is digitized and stored as an eight bit binary number. Each image is aligned so that corresponding pixels in different images are represented by corresponding elements in the arrays. At this point, quantitative analysis or comparisons can be performed on the images by using image process techniques to do comparisons of the elements of the arrays. Image enhancement techniques can then be applied to the results in order to generate an image representing the results of the comparisons.

4.0 OPTICAL SPOT SCANNER INSTRUMENTATION

The optical scanner instrumentation used on the previous programs was used as a basis for the setup used in this program. Modifications were made to the setup which led to improvements in both electrical and mechanical stability. Additional pieces of instrumentation along with required interface circuitry were added to provide signal recording capability. This section describes the basic optical scanner setup along with the modifications, improvements and additions developed for this program.

4.1 Basic Instrumentation

Figure 4-1 is a block diagram of the basic optical spot scanner set up for the State Superposition Technique. The light source for the optical scanner is a modulatable He-Ne laser. The red light from this laser has a wavelength of 632.8 nm and penetrates approximately 2.5 μm into silicon. The laser beam is deflected by galvanometer driven mirrors in a raster pattern while passing through the system optics, shown schematically in Figure 4-2.

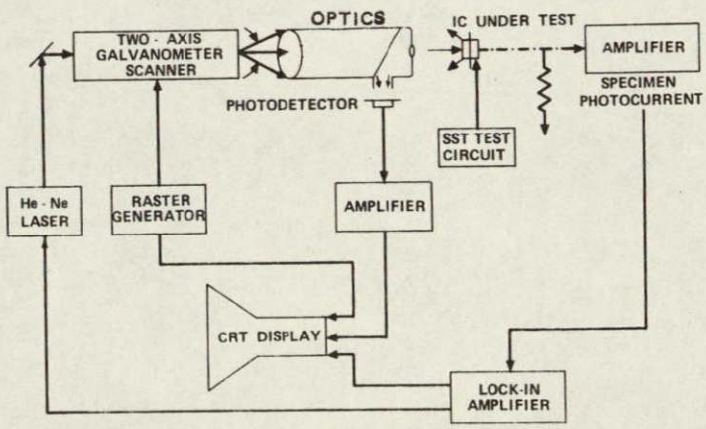

Figure 4-1. Block diagram of optical spot scanner set up for the State Superposition Technique.

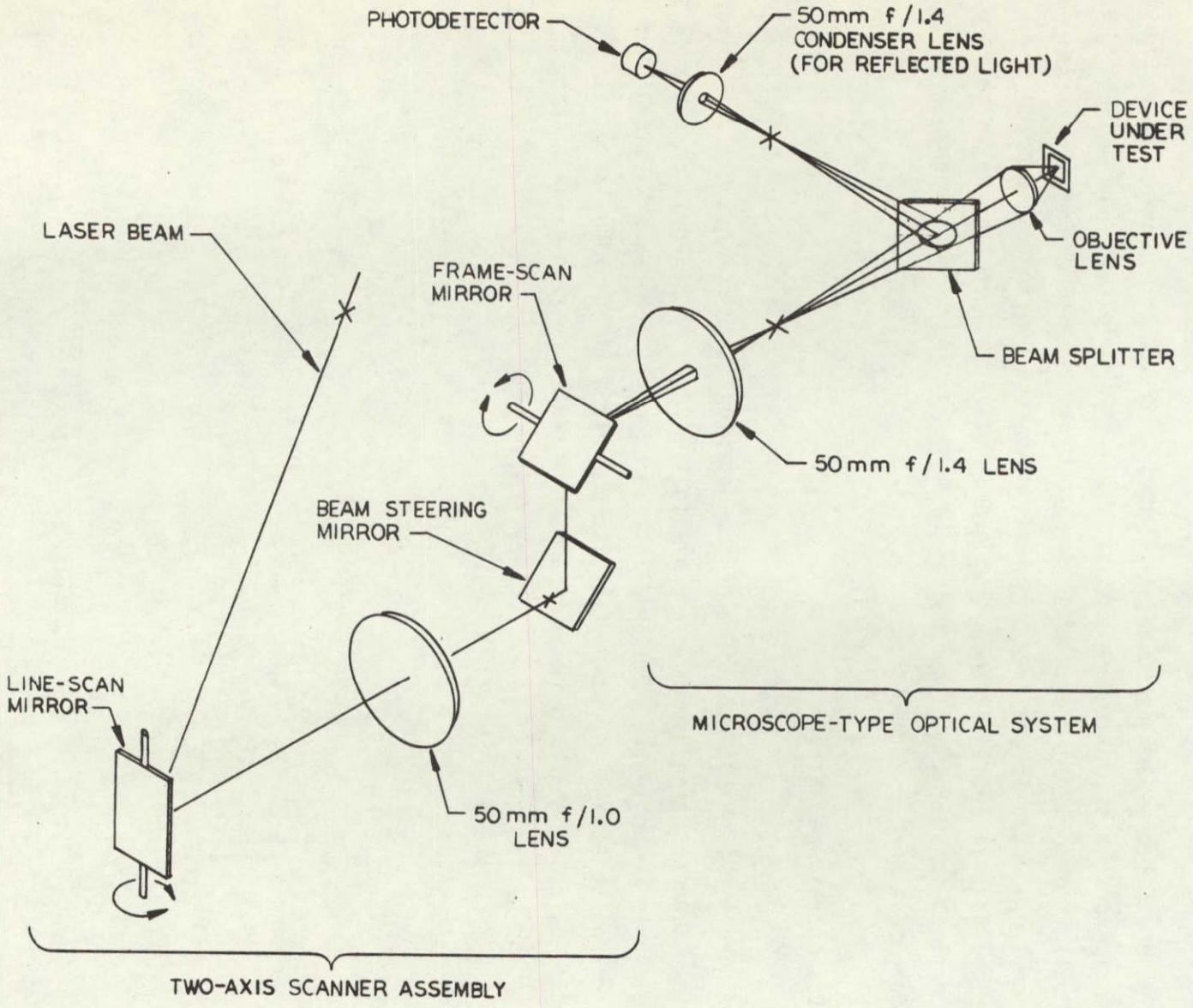

Figure 4-2. Diagram of the optical arrangement of the optical spot scanner.

The optics consist primarily of conventional long-working distance, flat-field, metallographic microscope lenses used in combination with two photographic lenses. A 50 mm f/1.4 lens is used in place of a microscope eyepiece. Two galvanometer mirror scanners separated by a 50 mm f/1.0 field lens comprise a two-axis scanner assembly. A beam splitter positioned between the 50 mm f/1.4 lens and the microscope objective directs the light that is reflected back from the test specimen to a photodetector.

The raster generator that is used to drive the galvanometer driven mirrors is also used to synchronously drive CRT displays. The induced photoresponse signal from the DUT (Device Under Test) is sensed by a small resistor (typically 100 Ω) in series with either a power supply or ground terminal of the DUT. This signal is amplified and used to intensity modulate a display CRT to generate a photoresponse image of the DUT. The display CRT has a P-7 long-persistence phosphor for easy viewing.

Reflected light from the surface of the DUT is directed to a photodetector which generates an electrical signal. This signal is amplified and used to intensity modulate a second display CRT to generate a reflected light image of the DUT. This image, which is essentially the same as that obtained by observing the DUT through a microscope, is used to position the laser raster pattern on the DUT.

Either the photoresponse or the reflected light signal can be used to intensity modulate a high resolution CRT for photographic recording of the images. Its broad-band P-4 phosphor was chosen so that false-color images could be made on color film by multiple exposures through additive primary-color filters. This method is very effective for localizing features in the photoresponse image with respect to features of the reflected light image. The reflected light image is photographed through a green filter or without a filter; the photoresponse image is photographed through a red filter. Multiple-exposures through different colored filters are also extremely valuable for comparing the photoresponse images obtained under different conditions. For example, the relative effectiveness of two State Superposition Programs in imaging all active elements can be evaluated by this method.

The lock-in amplifier in the setup generates a signal which is used to modulate the laser at a particular frequency and then demodulates the induced photoresponse. The use of the lock-in amplifier is necessary for separating the induced photoresponse signal from the switching noise generated by the DUT when

the State Superposition Technique is applied. An added advantage of using a modulated laser and lock-in amplifier is that the zero reference level of the photoresponse signal is independent of the static power supply current of the DUT.

4.2 Modifications to the Instrumentation

There were basically four areas where modifications were made in the optical scanner instrumentation: (1) the laser light source, (2) the mount for the laser, (3) the device holder/positioner and (4) the signal processing electronics. These improvements were made to meet the requirements of this program. Additionally, as part of a Hughes funded effort to improve the instrumentation, new CRT displays were added to the optical scanner setup.

4.2.1 Optical Scanner Laser

The Metrologic ML-669 0.5 mw modulatable HeNe laser that had been previously used in the optical scanner setup was replaced by a LICONIX Model 607V 2.0 mw modulatable laser. The Metrologic laser was adequate for the qualitative analyses that were performed on previous programs but it was not stable enough for the quantitative analyses that were the objective of this program. It was found that the output power of the Metrologic laser could drift by as much as 10% over a period of one hour. The long term (24 hour) stability of the LICONIX laser is specified to be at least as good as 0.5%.

Another significant advantage of the LICONIX laser over the Metrologic laser is that it can be 100% modulated from full "on" to completely "off". The Metrologic laser output could only be modulated by 15%. Thus the signal-to-noise ratio of the modulated photoresponse signal from the DUT is increased by a factor of almost seven through the use of the new LICONIX laser. This increase in signal-to-noise ratio will enable the lock-in amplifier to reject more noise than with the previous laser. This results in an overall gain in signal-to-noise ratio of even more than seven through the use of the new laser.

The LICONIX laser Model 607V is modulated through the use of an acousto optic modulation cell internal to the laser cavity. In the constant output mode, a precision beam splitter-detector combination samples a small fraction of the output beam and compares it to a stable reference voltage. The difference signal is amplified and applied via a feedback loop to the acousto optic modulation cell to obtain constant output power. In the modulated mode, a strictly linear relationship between input voltage and laser output power is achieved by matching the

output power to the applied modulation signal, through the feedback loop. The bandwidth of the feedback loop is 300 KHz. Zero volts input to the modulation system from an external source results in zero output power from the laser and 1 volt produces peak cw power.

4.2.2 Optical Scanner Laser Mount

The new LICONIX laser that was acquired to improve the optical scanner instrumentation required the design of a new mount for positioning it in the optical scanner setup since it is cylindrical. Also, the mount used for the previous laser was cumbersome, at best, when aligning the laser in the optical setup of the scanner.

The new LICONIX laser and the mount that was designed for it are shown in Figure 4-3. Clamps hold the cylindrical laser stationary in V-blocks which are fastened to a base plate. A tilt table under the base plate is connected to a height adjustable table. The post which supports this entire assembly is mounted on a linear translation stage which is, in turn, fixed to the optical bench.

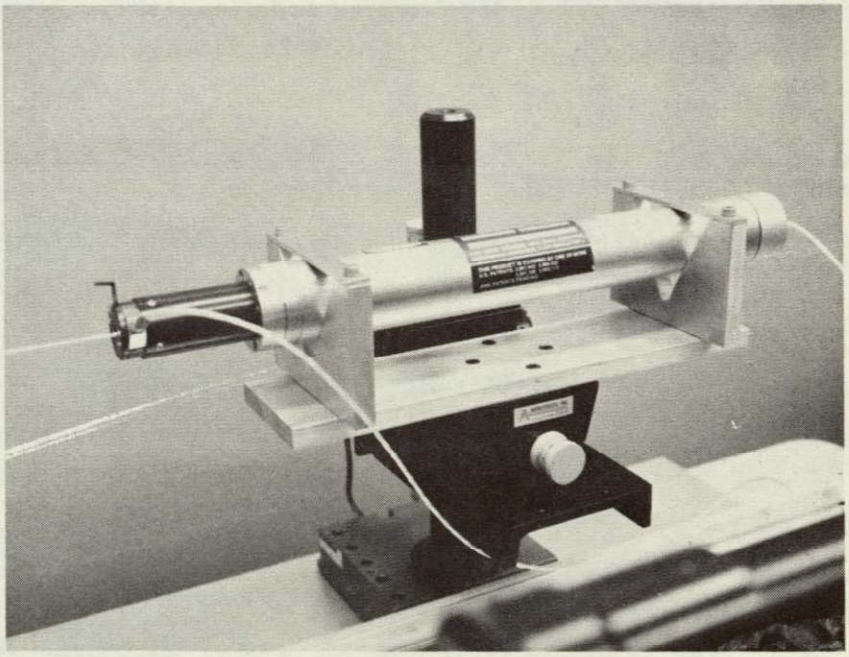

Figure 4.3. LICONIX laser in its mount.

The resulting laser mount allows for precise adjustments to the positioning of the laser resulting in a perfectly aligned optical system. Furthermore, the various components were designed and selected to provide a stable mount resulting in a vibration-free optical setup.

4.2.3 Device Holder-Positioner

An improved holder and positioner for the DUT was designed and constructed for the optical scanner. The assembly was constructed from purchased optical positioning components some of which were modified slightly for this assembly.

Two linear translation stages were used in the new assembly to provide X-Y positioning of the generated raster pattern on the DUT. A third linear translation stage provides motion in the Z direction for focussing the laser beam on the DUT. A tilt mechanism provides θ_x and θ_y adjustments to orient the surface of the DUT perpendicular to the optical axis of the system optics. This results in the laser beam being focussed throughout its entire raster pattern over the device. A rotation mechanism provides precise θ_z motion so that the device can be rotated resulting in the photoresponse image being rotated on the CRT displays.

The new sample holder-positioner is shown in Figure 4-4. The DUT is shown mounted in its test socket. The socket for the DUT, as well as connections for cables leading to other remote circuitry which provides electrical biases and input signals for the State Superposition Technique, are mounted on a circuit board. The circuit board is mounted on stand-offs which are fastened to one of the positioning components. The Zero Insertion Pressure (ZIP) socket allows test samples to be easily inserted and removed. Several circuit boards have been assembled to allow parts with different packages and lead configurations to be tested.

As in the case of the mount that was constructed for the laser, the components chosen for the construction of the device holder-positioner provide a stable, vibration free assembly. Also, these are precision components which enables photoresponse images to be aligned for image recording and subsequent processing.

4.2.4 Signal Processing Electronics

The lock-in amplifier used for the optical scanner is a Princeton Applied Research HR-8 Lock-in Amplifier with a Type C Preamplifier. The maximum reference oscillator frequency (f_m) at which it operates is 160 KHz. The manner in which the image information is impressed on the modulated photoresponse signal places certain restrictions on the choice of f_m. If the photoresponse image is to contain the maximum amount of information, the beam dwell time on each pixel

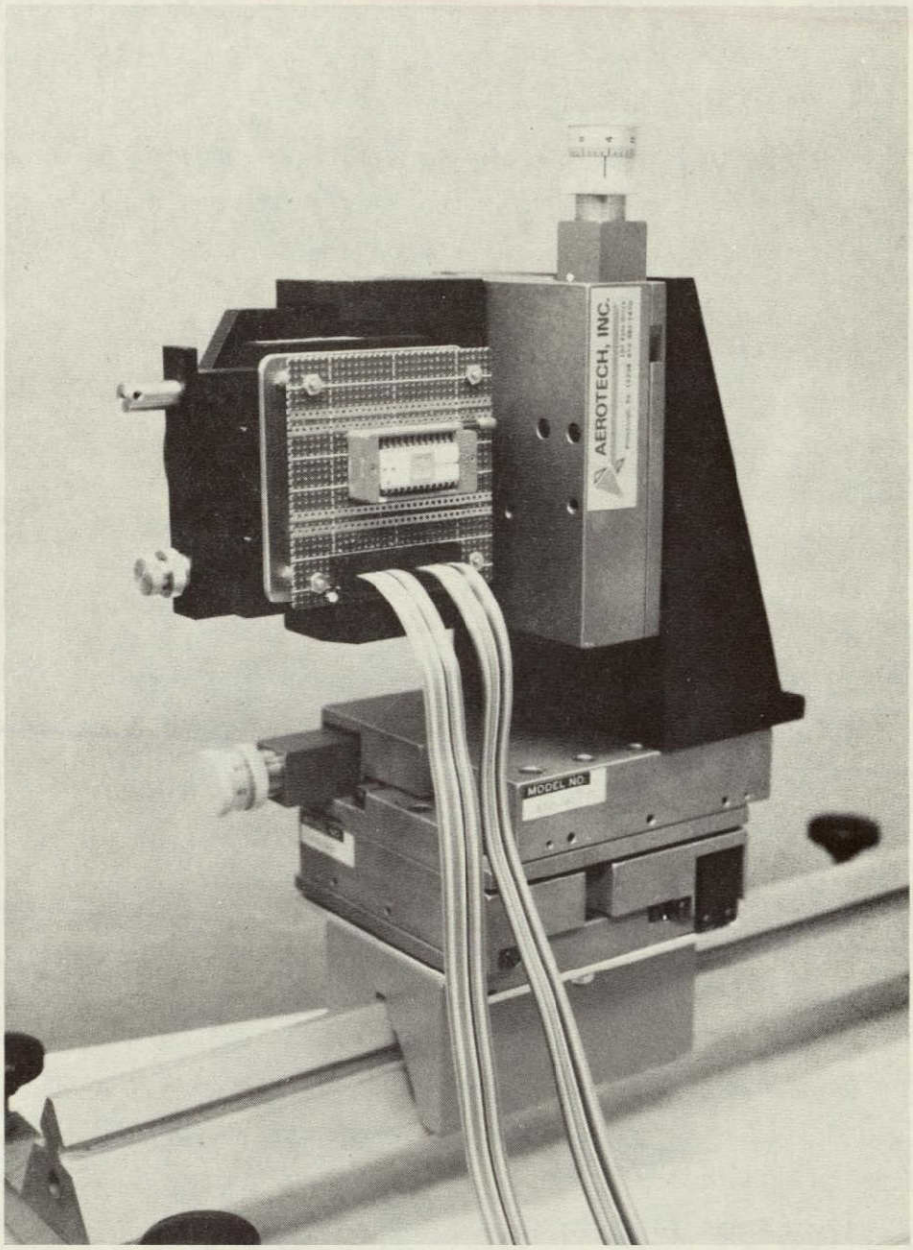

Figure 4-4. Test sample holder - positioner.

(picture element) is required to equal at least one modulation period. If the line scan time is τ_L and there are n pixels per line, then $f_m > n/\tau_L$. For this program n is approximately 500. If τ_L is 100 mS, then $f_m > 5$ KHz, If τ_L is 10 mS, then $f_m > 50$ KHz. The maximum frequency generated by the P. A. R. lock-in amplifier exceeds both of these frequencies but would provide better precision in the second case if it were higher.

The P. A. R. lock-in amplifier was modified to provide a maximum frequency of approximately 300 KHz, as a result of the preceding considerations. However, experiments with the CD4028 test device revealed that the lock-in amplifier did not reject switching noise as well at 300 KHz as it did when operated at 160 KHz. Apparently, the switching noise spectrum contains components that are within the frequency band of the lock-in amplifier when it is operated at 300 KHz. Further experiments revealed that there were frequencies between 160 KHz and 300 KHz at which the lock-in amplifier rejected the switching noise if the frequency of the State Superposition Test circuit was carefully controlled. Deviations from the specified frequency apparently introduced components into the switching noise spectrum which were within the frequency band of the lock-in amplifier. As a result of these problems, along with a tendency of the lock-in amplifier to be somewhat unstable with these modifications (the phase angle at which maximum signal was obtained would drift slowly) the modifications were not used and the lock-in amplifier was used at a modulation frequency of 160 KHz. As a result, the line scan time was set to be 100 mS.

4.3 Additions to the Optical Scanner Instrumentation

One of the major requirements of this program was to develop the capability of recording photoresponse data from devices and then later retrieving it so that it could be compared with similar data. The initial approach that was suggested for recording the photoresponse data was to connect the output from the optical scanner directly to the input of an analog-to-digital converter on a digital computer and then store the digitized data on magnetic discs. For various reasons that are discussed in Section 5.1, this approach was not used.

Instead, it was decided to record the photoresponse data on magnetic tape. These tapes would then be later digitized for use by the digital computer that would do the image processing of the photoresponse images. Because of bandwidth and resolution considerations, the photoresponse data was recorded by an FM recorder on magnetic tape along with various synchronization and calibration signals. An interface circuit was created to couple the optical scanner's outputs with the

FM recorder's inputs and to generate the required synchronization and calibration signals.

The recorder used was a Ampex Model FR1300 FM recorder with tape speeds of 7.5 ips (inches per second) to 60 ips. The photoresponse data was recorded at a tape speed of 60 ips which was necessary to provide enough resolution for the incoming data at a frequency of approximately 5 KHz. (500 pixels per line, at one line per 100 mS.) The data was recorded on Scotch Brand Magnetic Tape. Each tape is 2400 feet long. Each photoresponse image requires approximately 60 seconds, which uses 300 feet of tape. Therefore, 8 images could have been recorded on each tape, but only seven (or less) were recorded per tape.

The interface circuit provided seven channels of data to the FM recorder which has the capability of recording 10 channels of data. The seven channels are listed below:

Channel 1: Reflected Light Data (Analog)
Channel 2: Photoresponse Data (Analog)
Channel 3: "Line" Signal (Digital)
Channel 4: "Frame" Signal (Digital)
Channel 5: "Run" Signal (Digital)
Channel 6: "Clock" Signal (Digital)
Channel 7: Calibration (+5 volts)

Figure 4-5 is a block diagram of the interface circuit showing connections to the optical scanner and the FM recorder. Basically it gates the signals generated by the optical scanner to the FM recorder; generates several synchronization signals which are recorded by the FM recorder and also control the optical scanner's scan generators; and generates calibration signals which are recorded by the FM recorder.

The function of the interface circuitry can be best demonstrated by explaining how a single image would be recorded. The operator flips a switch which switches the "Run" signal from "low" (zero volts) to "high" (+5 volts). This signal is recorded primarily for the convenience of the person who later digitizes the tape from the FM recorder, as an indication that some meaningful data is about to follow. The "High" from the "Run" logic starts the clock pulse generator which runs at a fixed frequency (crystal controlled) of 5.013 KHz. The operator waits a fixed period of time and then flips a second switch which switches the "frame" signal from "low" to "high". This starts a clock pulse counter, the horizontal and vertical scan generators in the optical scanner and a line counter. As soon as the clock pulse counter starts, the "line" signal which it generates switches from "low" to "high". Similarly, the line counter generates the "frame" signal which switches from "low" to "high". These two signals indicate that a

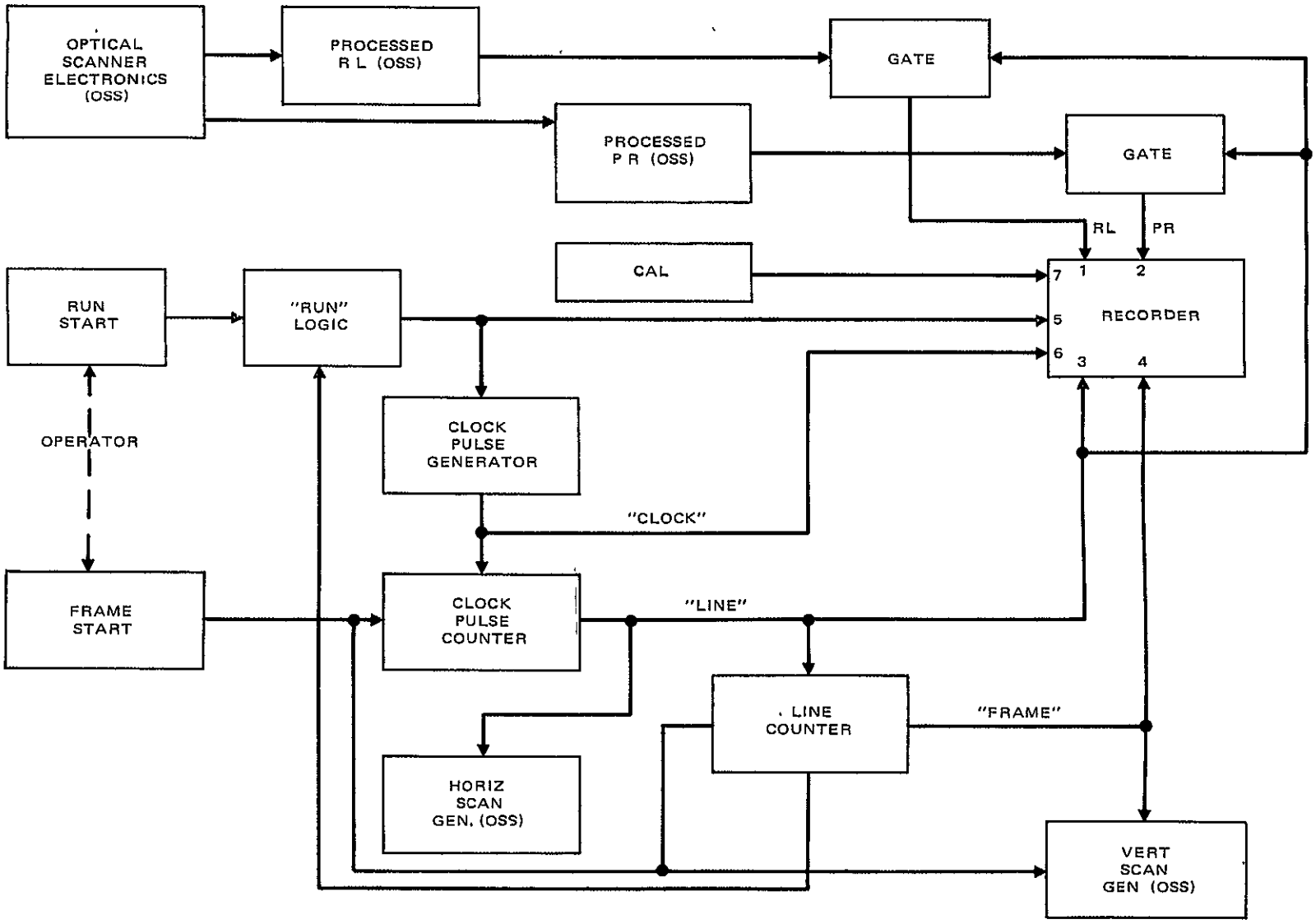

Figure 4-5. BLOCK DIAGRAM OF OPTICAL SCANNER/FM RECORDER INTERFACE

photoresponse image is now being started and the "line" signal turns on the gates that allow the reflected light and photoresponse signals to be transmitted to the recorder.

The clock pulse counter counts 512 clock pulses and then the "line" signal switches back to "low" indicating the end of a line in the image. This signal causes the gates that transmit the reflected light and photoresponse signals from the optical scanner to the FM recorder to turn off. Also, the line scan generator resets back to the beginning edge of the frame. The clock pulse counter counts a few more pulses while the line scan galvanometer driven mirrors stop ringing, then resets to zero and starts counting again. The "line" signal goes "high" again and the whole cycle repeats. The line counter counts 512 lines, at which point the "frame" and "run" signals go "low" indicating the end of a photoresponse image on the tape. The signals supplied by the interface to the FM recorder are shown in Figure 4-6.

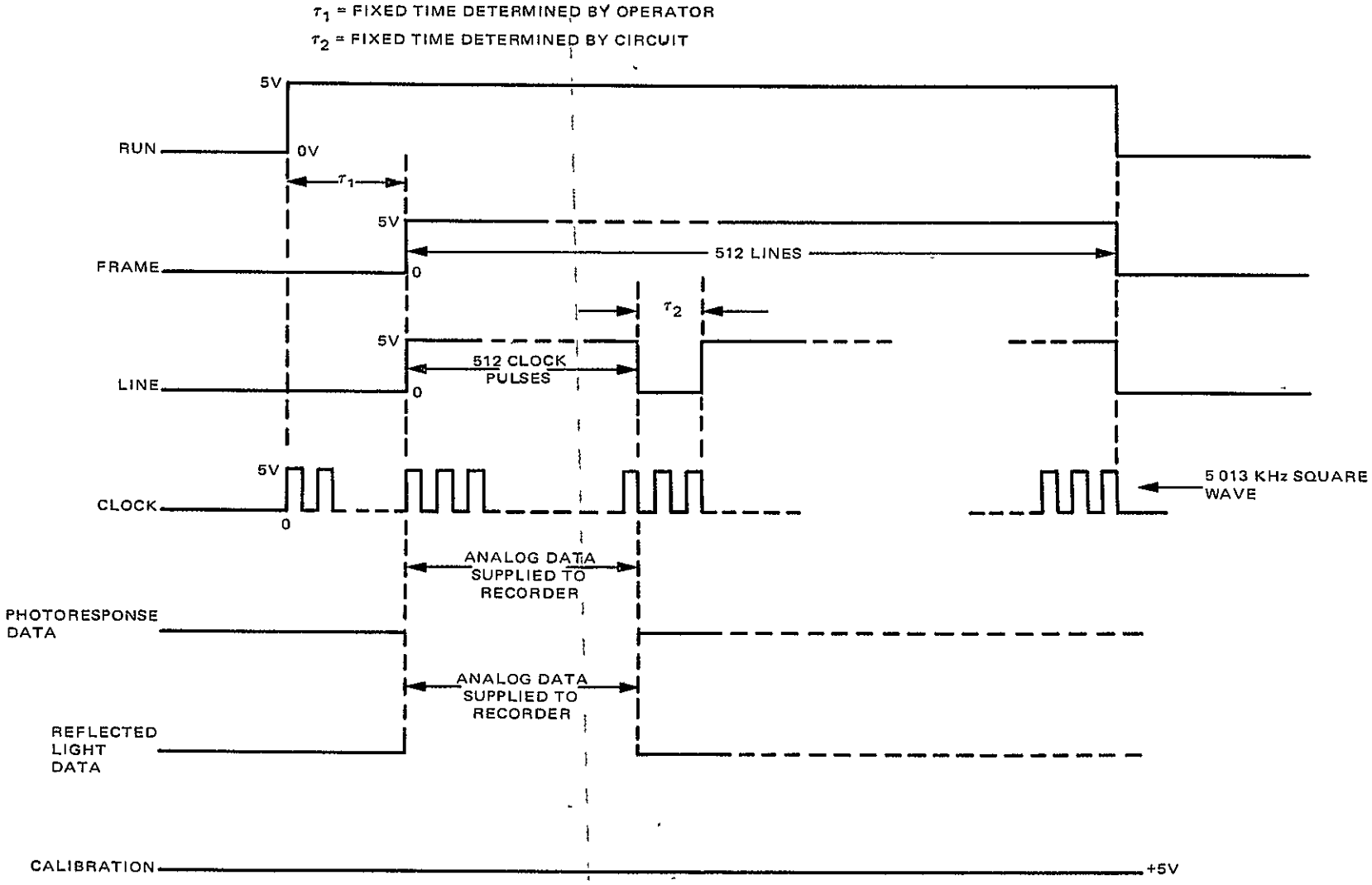

Figure 4-6. SIGNALS SUPPLIED TO FM RECORDER AS FUNCTION OF TIME

5.0 IMAGE PROCESSING OF PHOTORESPONSE DATA

5.1 Approach

The original proposed approach for doing image processing of the photoresponse data was for on-line, real time data capture and control. The output signals from the optical scanner were to be connected directly into an A/D (analog-to-digital) converter on a digital computer which would process and store the data on disc memory. Using this technique, the computer would control the optical scanner, collect the photoresponse data, eliminate non-critical data (idle time between images, scanner retrace times, etc.) and store formatted data on a bulk storage disc.

The approach that was used was to connect the output of the optical scanner to a FM recorder through an interface and to record the signals generated by the optical scanner along with synchronization signals generated by the interface. As they were needed, the images on the tapes from the FM recorder were then processed and stor on another tape in digital format. These tapes were then processed by the image processing hardware and software. This new approach accomplished the same goals as the original approach but there were many significant advantages to this approach. Some of the advantages include:

(1) less computer time and cost - the FM tapes were produced without the expenditure of time or cost of a computer or the use of computer personnel

(2) eliminates optical scanner/computer interface - using this approach there is no need for an elaborate interface between the optical scanner and a computer

(3) less image processing by computer - a large volume of data was collected without the need to computer process every image; only selected FM tapes were digitized and computer processed

(4) bulk processing of photoresponse images - once some photoresponse images are selected for analysis, the appropriate tapes are chosen and loaded; there is no need to wait for the production by the optical scanner of photoresponse images.

(5) this approach is an economical method that could be used to apply the developed techniques to do semiconductor screening.

The last advantage is perhaps the most important.

This new approach that was used, evaluates and demonstrates an economical method that could be used to apply the developed techniques without the need of a digital computer or image processing software. This approach only requires that the user have an FM recorder to record the photoresponse images which then can be processed

by a separate computer facility. Use of this approach in this program will evaluate its technical accuracy, and demonstrate that it is a valid method.

5.2 Image Processing Hardware and Software

Several existing Hughes Aircraft computing facilities were utilized in order to meet the needs of this program in the most time and cost effective manner. These facilities include:

(1) Flight Test Division Laboratory - for analog-to-digital data conversion,
(2) Simulation/Computing Center - for data reduction and reformatting
(3) Synthetic Aperture Radar Laboratory (SAR) - for image viewing, processing and printing.

In order to show how these facilities were utilized to provide the necessary data processing, the overall task of data processing will be broken down into four phases:

PHASE I	-	Data Collection
PHASE II	-	Data Conversion
PHASE III	-	Data Reduction & Formatting
PHASE IV	-	Data Correlation & Display

PHASE I - Data Collection

In Phase I, the output of the optical scanner is connected to a FM tape recorder through an interface so that the photoresponse data and reflected light signal can be recorded. Five additional signals are also generated by the interface logic and are also simultaneously recorded. These signals are (1) a run signal to denote that data following was significant and not tape start-up or "dead" time between images, (2) a frame signal to indicate the start of a new frame of data lines and pixels, (3) a line signal to indicate when the pixel clock is collecting significant data as opposed to retrace, (4) the pixel clock which is used to identify when the data was collected, and (5) a calibration signal used to later establish the correlation between extent of modulation and actual component bias voltage present during that recording period. These additional signals will be used in later phases to reduce the amount of data processed and to establish references for the analog-to-digital conversion.

PHASE II - Data Conversion

After a tape of images is collected, the tape must be converted from its analog state (FM) to a digital form. To perform this conversion, standard hardware and software was available at Hughes Flight Test Division. However, this equipment required additional signals for digitization, and an additional hardware circuit was designed. The added hardware circuit allowed for the generation of a burst of 4

convert commands whenever the recorded pixel clock switched from "low" to "high". This command input, when combined with existing equipment, resulted in the rapid digitization of a four word record (one word per remaining recorded signal) for each pixel clock. Calibration channel data was utilized to assure that digitized voltage levels would accurately represent the raw data. This feature was critical since digitized results from different FM tapes would later be subtracted and cross-correlated. The serially recorded component data was stored on a 9 track (9T) 800 BPI EBDC magnetic tape for transfer to the next phase of the data processing.

PHASE III - Data Reduction & Formatting

The simulation and Computing Center (SCC) Sigma 5 system was used to perform the majority of the required special purpose data manipulation. Because the SCC is active in a number of real-time signal processing and conditioning tasks, it has available to it a software library of digital data filter reformatting routines which were used extensively by this project. The Sigma 5 was used to read the 9T raw digital data tape and apply filtering to the data. The run channel was used to denote whether data was valid or not. Once the data is valid, the software scans for a frame pulse in order to start generating the 512 lines of pixels of data. The Sigma 5 also formats this data so that it is readable by existing SAR Lab routines. Throughout the above processing, digital software routines check to eliminate noise and check for data inconsistencies which could have been introduced during the capture or conversion phases.

PHASE IV - Data Correlation & Display

In this phase, as in previous phases, an attempt was made to define interfaces and data structures which would allow the use of existing software modules in order to accomplish the program goals. The equipment utilized in this phase was a Digital Equipment Corporation 11/70 system, a Comtal 800 display station, and a Dicomed high resolution film recorder. During this phase, the 9T image-format tape from the Sigma 5 was read and displayed on the Comtal. The Comtal allows one to store 512 lines of 512 pixels and then display this on a raster TV monitor. The Comtal also allowed for a set of registration symbols to be generated and displayed simultaneously with the component image. Using existing routines, each image was aligned to the registration marks and then stored in place of its non-aligned version. Also, using existing software, images were subtracted and the results enhanced to highlight any changed features. The final step in the data processing was to print hard copies of each image and subtraction results.

Figure 5.1 shows the overall hardware flow and the way in which the various facilities were integrated to provide the necessary processing. Figure 5.2 shows

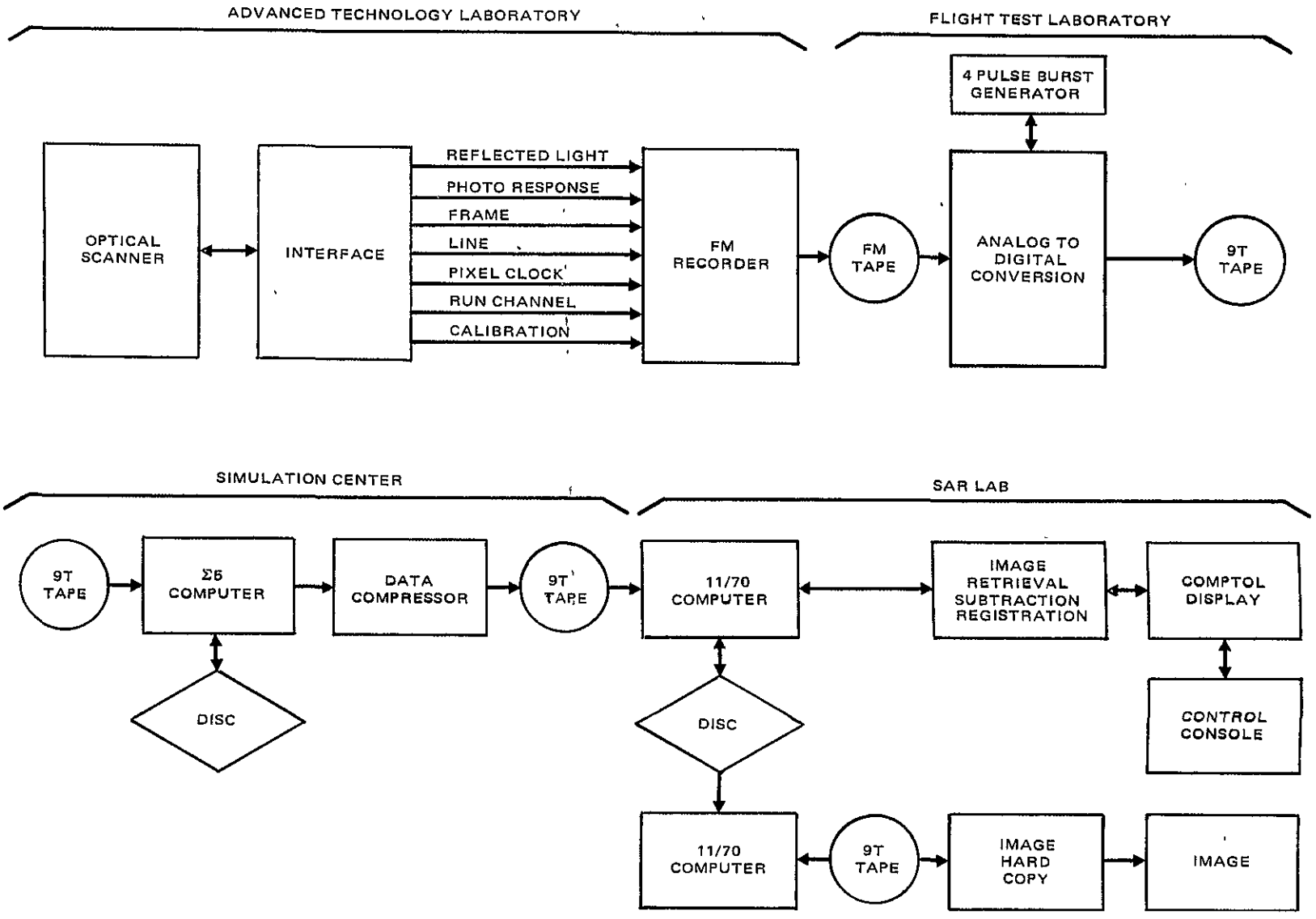

Figure 5.1. HARDWARE FLOW DIAGRAM

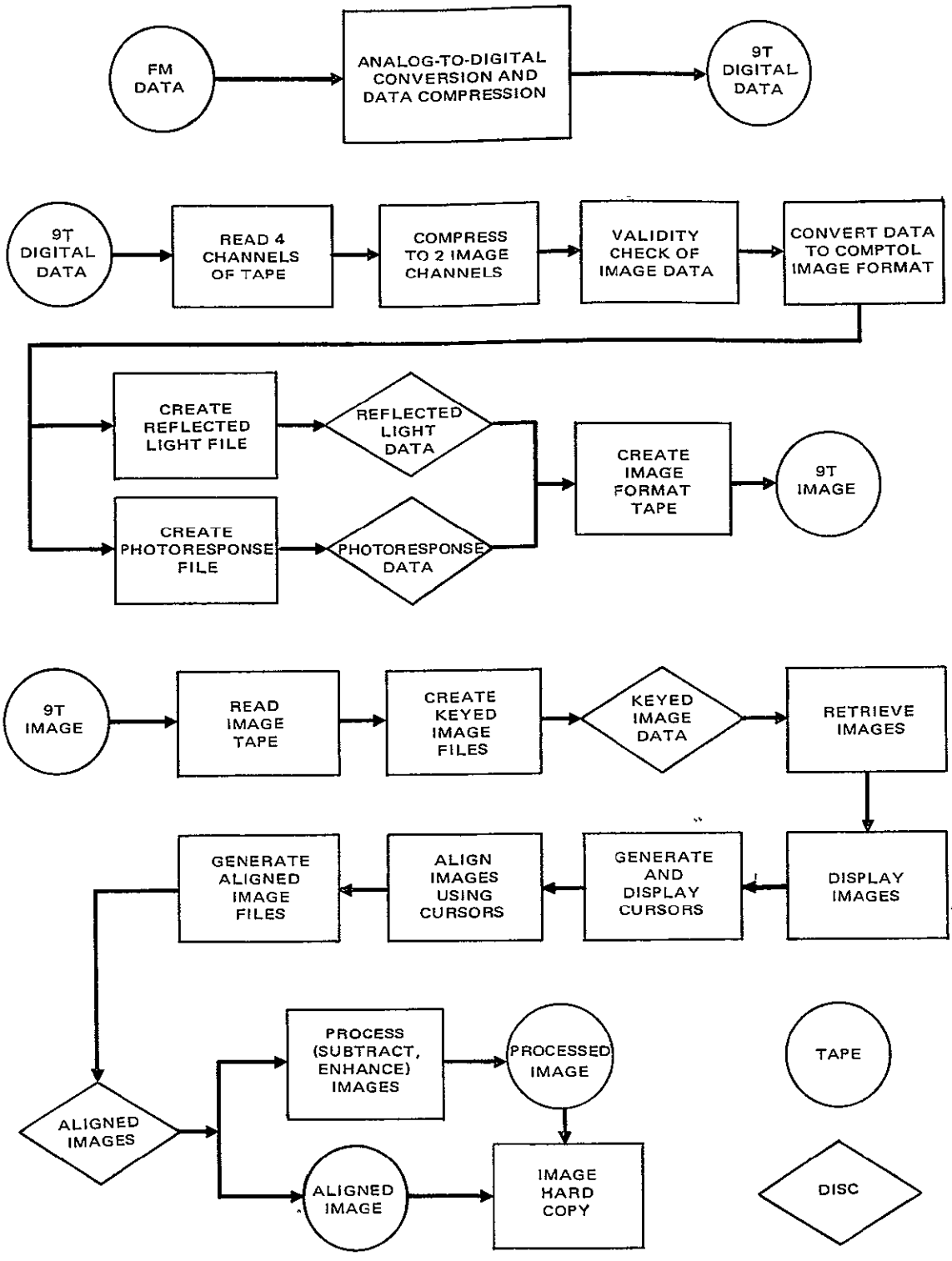

Figure 5.2. SOFTWARE FLOW DIAGRAM

a detailed diagram of the various software modules used during the phases of this program. Throughout the data processing phases, there were two goals which were maintained:

(1) use a modular structure, thus maximizing the use of existing routines, and

(2) design each phase so that it could be quickly debugged and verified through the use of a software simulation of the interface data to check the input and outputs of each phase.

5.3 Tests of Data Processing Approach

During the modification and development of the various software routines needed to do the image processing of the photoresponse data, additional software was created which was used to test the image processing software. The additional software provided a simulation of the appropriate data to check the inputs and outputs of each of the phases of the data processing. In this manner, much of the image processing software and hardware could be debugged and verified prior to any attempts at actual photoresponse image processing.

The real test of the entire image processing task was the actual display and comparison of some photoresponse images which had been produced by the optical scanner and recorded by the FM recorder. The initial test of the entire procedure, including all four phases of image processing was performed using photoresponse images from a simple test device. The device that was chosen was a 2N2222A transistor, since its photoresponse image is not complex. Three images were recorded from a single device: the first image was recorded, the second image was recorded after the device had been shifted by a significant amount and then the third image was recorded following attempts to manually re-position the device in its initial position.

The three recorded images were then digitized, processed, subtracted and displayed. Figures 5.3 through 5.5 show the first, second and third images, respectively. The only difference between the images is the position of the test device. These results show that the overall approach can at least reconstruct the photoresponse images from the optical scanner. Figure 5.6 shows the result of subtracting the first recorded image (Figure 5.3) from the second (Figure 5.4). Figure 5.7 shows the subtraction reversed; that is, the second image subtracted from the first. These results show that the subtraction routines function correctly. As expected, there are differences between the two images because the device was intentionally shifted. (Normally, attempts would be made to align the photoresponse images prior to the image subtraction, but this case was just an initial test of the procedure.) Two subtractions are necessary since negative results of subtractions appear the

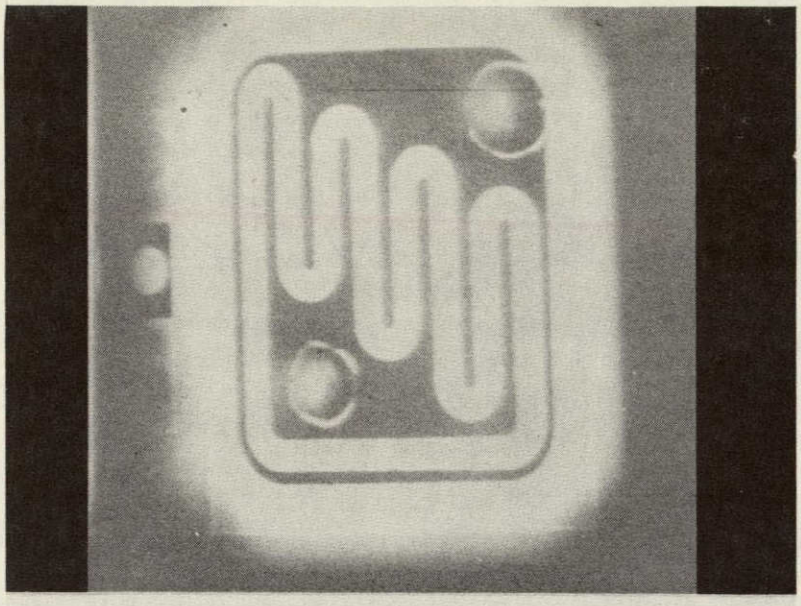

Figure 5.3. Initial photoresponse image from the 2N2222A transistor.

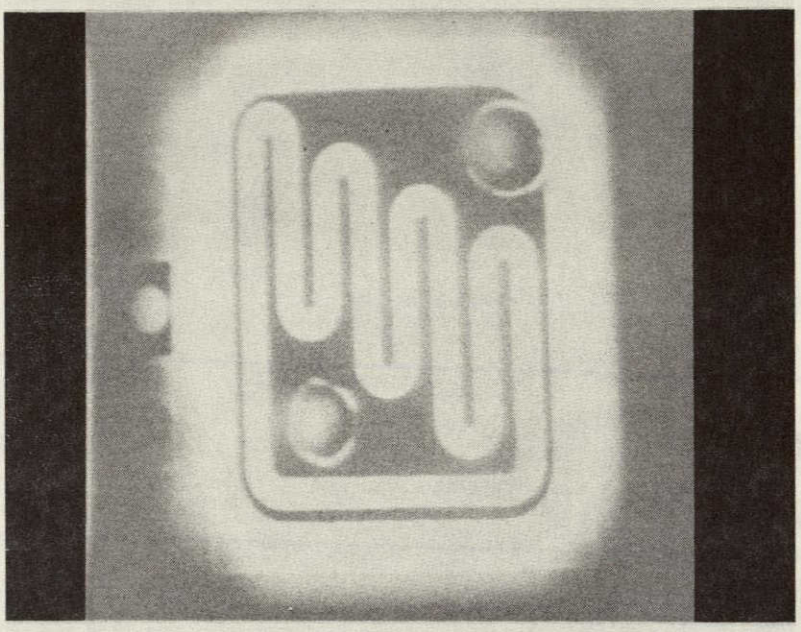

Figure 5.4. Photoresponse image from the same 2N2222A transistor that was used for Figure 5.3. The device was intentionally shifted downward for this image.

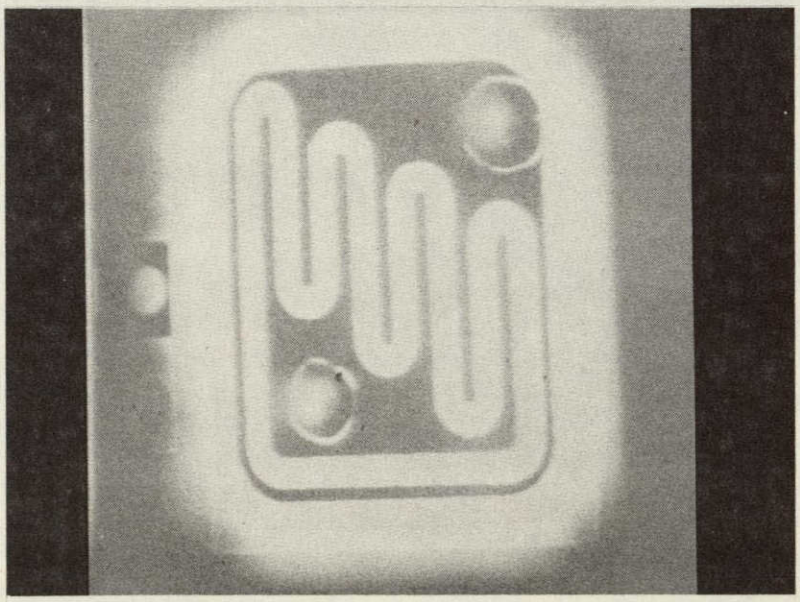

Figure 5.5. Photoresponse image of the 2N2222A transistor after attempts were made to manually re-align it with the position used for Figure 5.3.

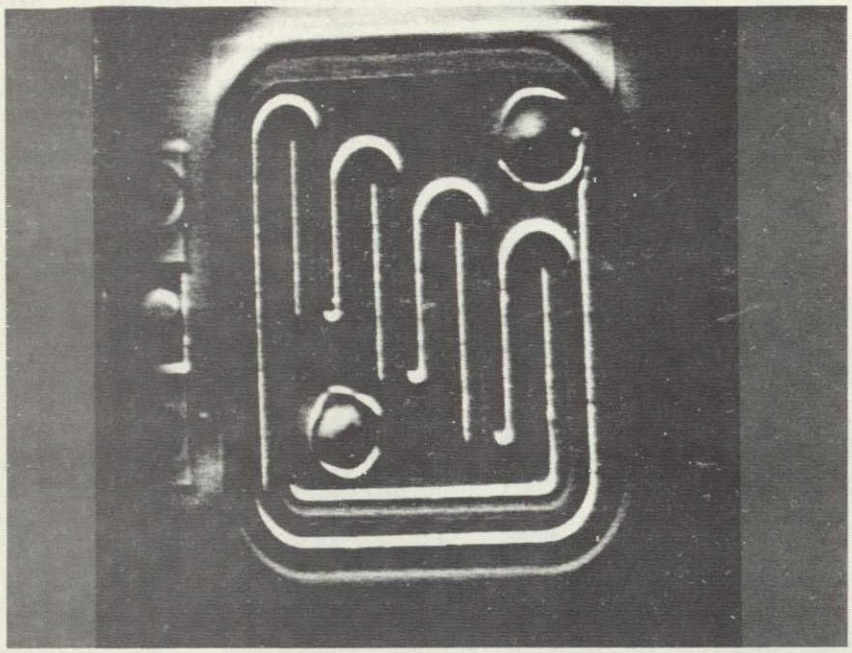

Figure 5.6. Image resulting from the subtraction of Figure 5.3 from Figure 5.4.

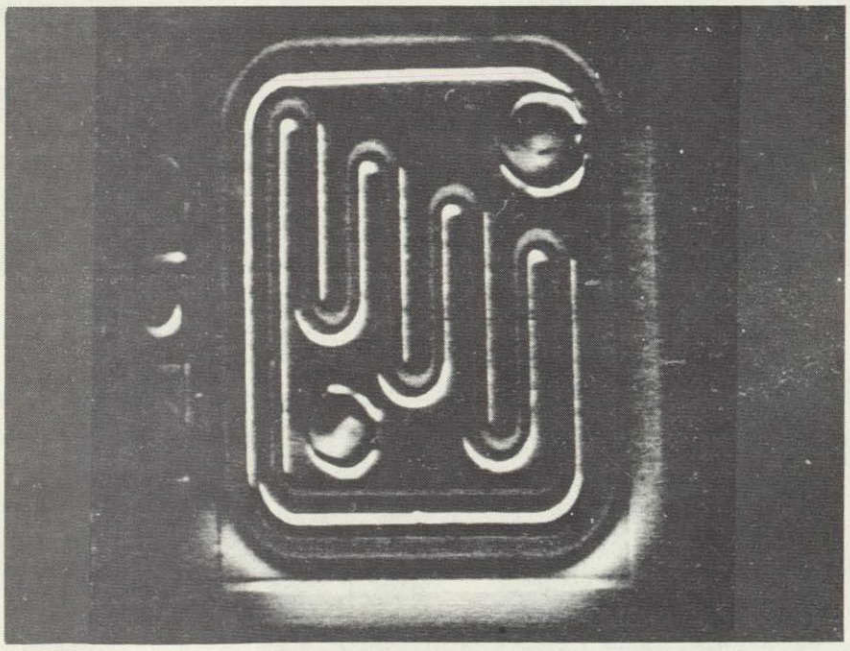

Figure 5.7. Image resulting from the subtraction of Figure 5.4 from Figure 5.3.

same as a subtraction where the result is zero. For example, if two aligned images of equal intensity are subtracted, the result would be a black image (zero difference). If two aligned images are subtracted and one image is more intense (brighter) than the other image, the result would again be a black image if the brighter image was subtracted from the other image (negative result). When the less intense image was subtracted from the brigher image, an image would result revealing that there was a difference between the images.

Figures 5.8 and 5.9 show the results of the subtractions of the first image (Figure 5.3) from the third (Figure 5.5) and vice versa. These results show that there is very little difference in the position of these images. This shows that devices can be positioned manually using the sample holder-positioner so that they are closely aligned.

The second test of the overall image processing procedure was performed using images recorded from two of the actual CD4028A test devices. Figure 5-10 shows the photoresponse from S/N 18 and Figure 5-11 shows the photoresponse from S/N 19. These results show that the software can reconstruct complex data that was produced by the optical scanner.

In order to align images from such complex devices, the images were first manually aligned using the precision sample holder-positioner. Particular care was used at this point to eliminate any rotation (θ_z) differences. When the images are then displayed at the image processing facility they are then more carefully aligned in the X-Y directions using cursors generated by the software. Each image is displayed simultaneously with the cursors and then stored in place of its non-aligned version. Figure 5-12 shows the cursors generated by the software. Figured 5-13 through 5-15 show a photoresponse image with the cursors superimposed on it, after the appropriate features on the photoresponse image have been aligned to the cursors. Of course, different shape cursors are created for each device type to align to a prominent feature on its photoresponse image.

Figures 5-16 and 5-17 show the results of the subtractions between Figures 5-10 and 5-11 after they had been aligned. It can be seen that the subtractions were fairly successful leaving only slight residues, some of which were real differences and some of which are results of minor misalignment which still remained. This shows that the subtraction routines work for complex photoresponse images.

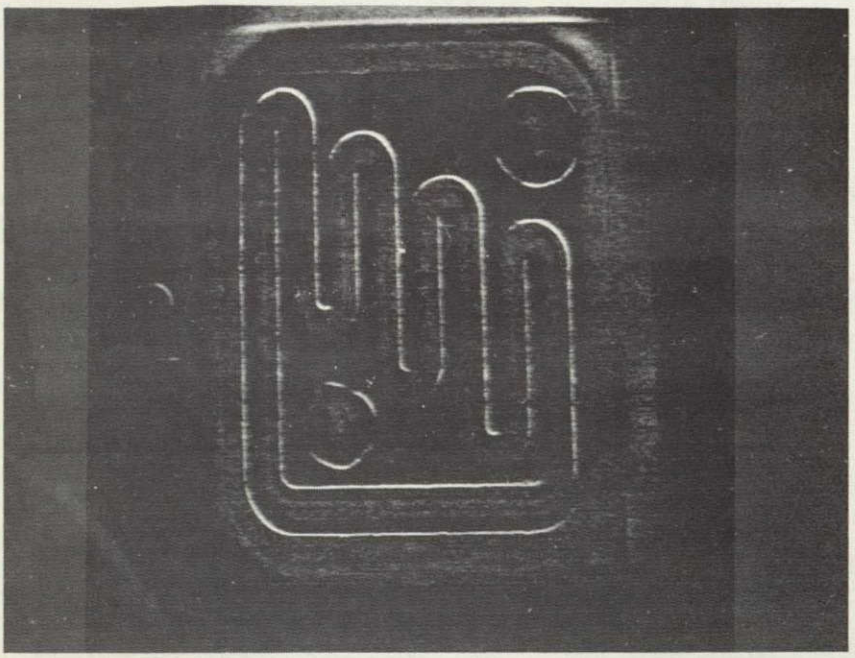

Figure 5.8. Image resulting from the subtraction of Figure 5.3 from Figure 5.5

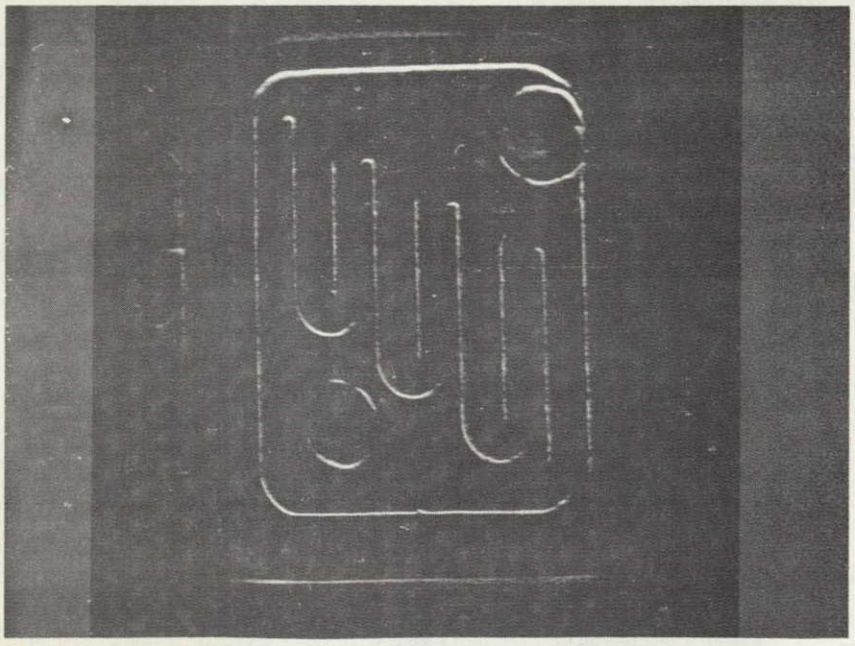

Figure 5.9. Image resulting from the subtraction of Figure 5.5 from Figure 5.3.

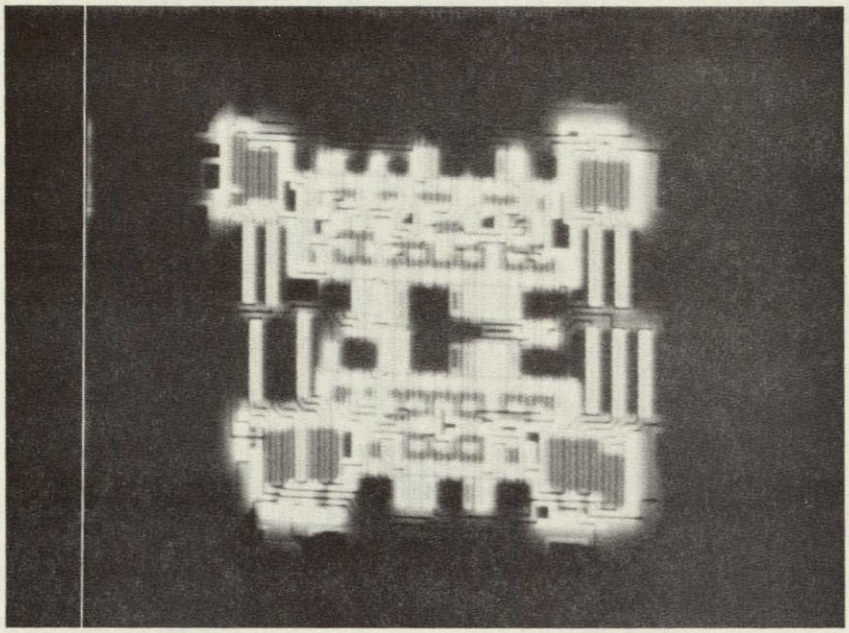

Figure 5.10. Photoresponse image from an actual complex test device (CD4028A test device S/N 18).

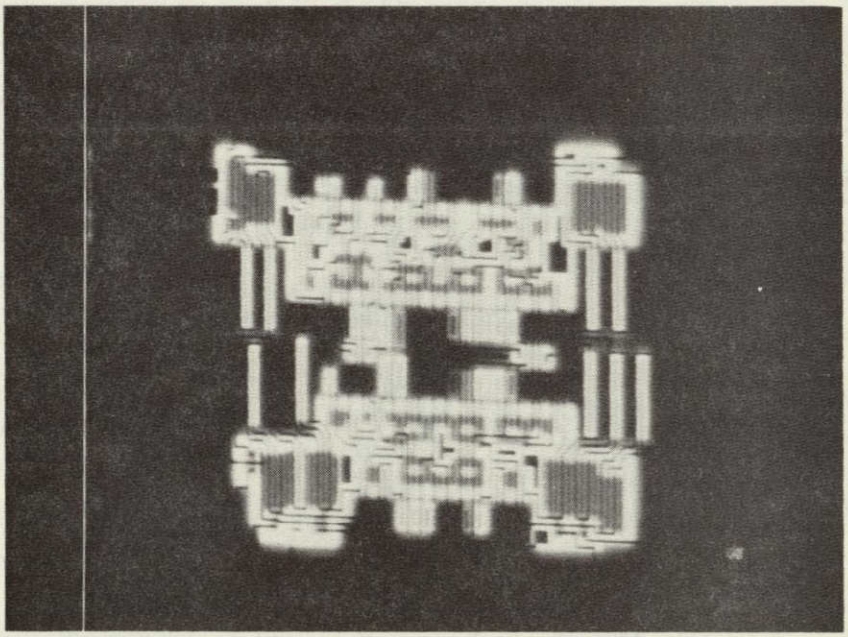

Figure 5.11. Photoresponse image from a second test device (CD4028A test device S/N 19).

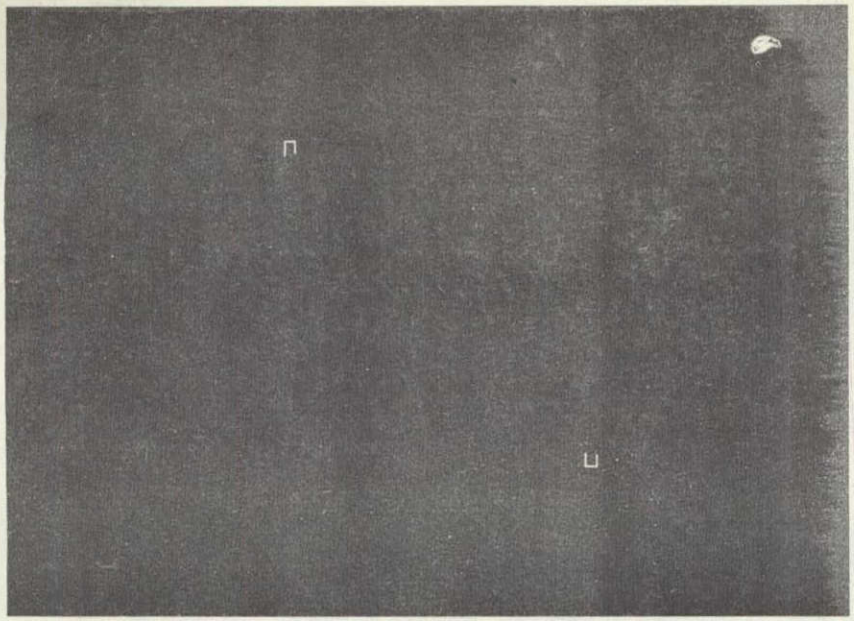

Figure 5.12. Cursors generated by the computer software for image alignment.

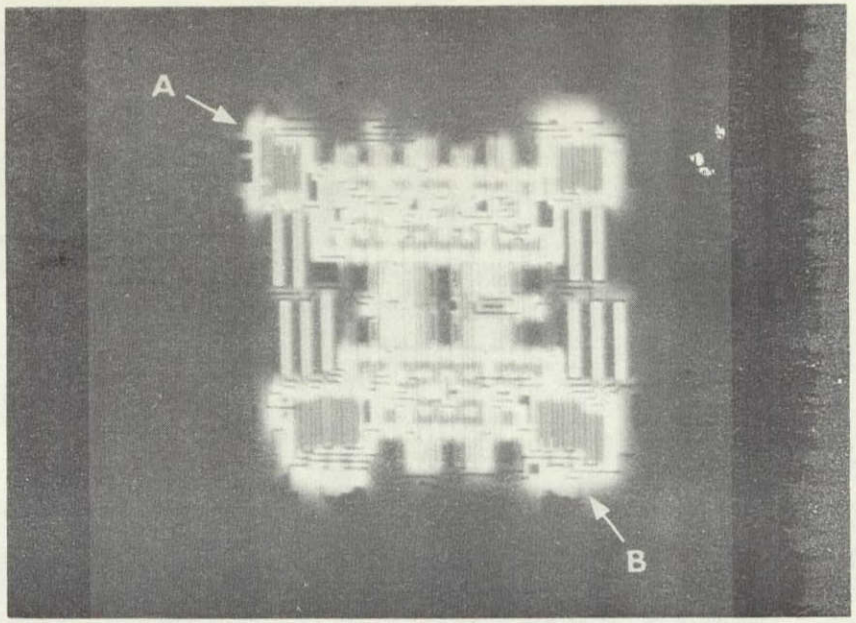

Figure 5.13. Cursors superimposed on a photoresponse image.

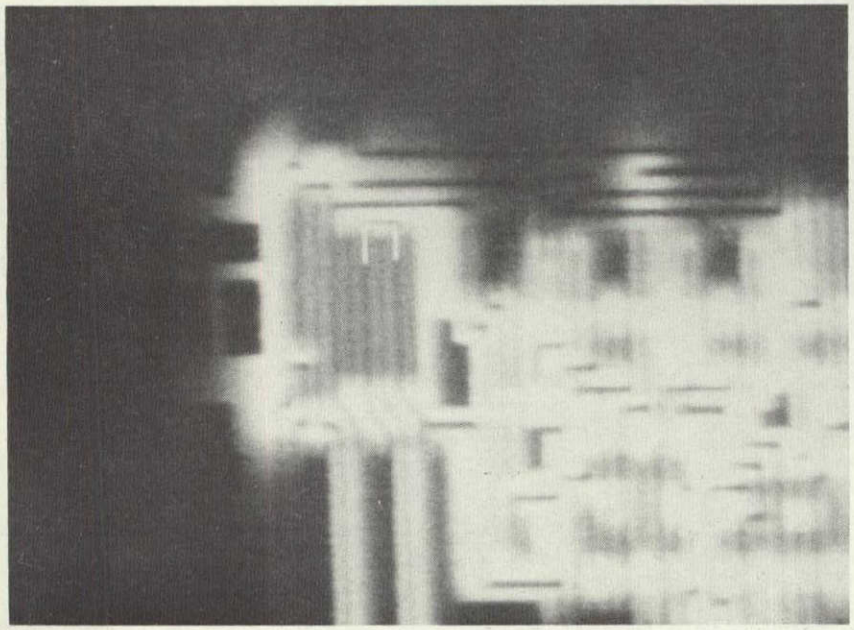

Figure 5.14. Enlarged view of area indicated by arrow A on Figure 5.13. Cursor aligned to image feature.

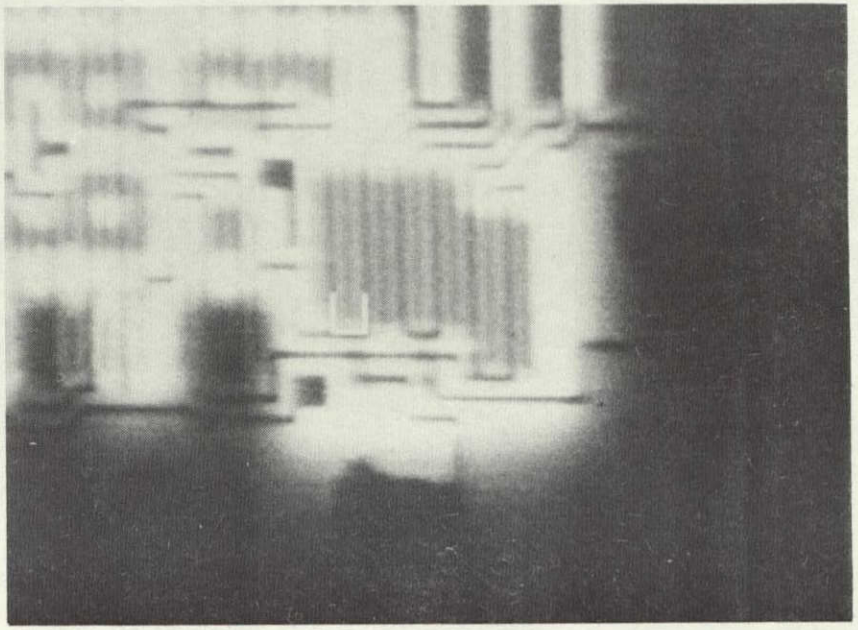

Figure 5.15. Enlarged view of area indicated by Arrow B on Figure 5.13. Cursor aligned to image feature.

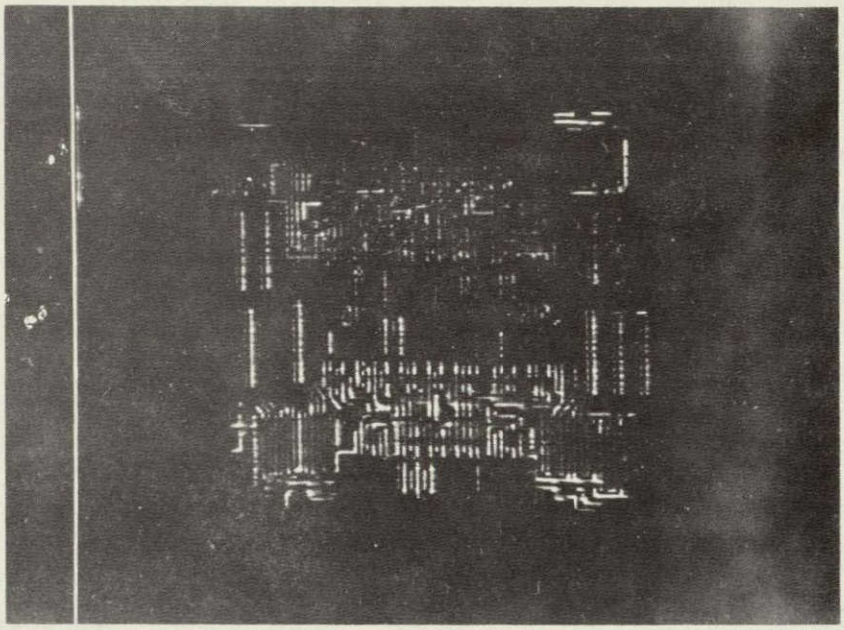

Figure 5.16. Image resulting from the subtraction of Figure 5.10 from Figure 5.11. The remaining bright areas are results of minor misalignments between the two images.

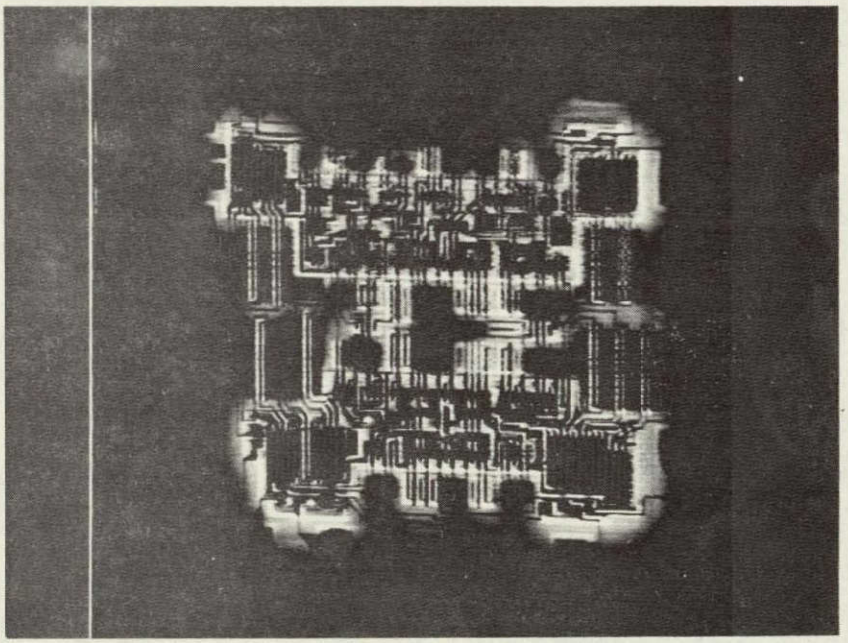

Figure 5.17. Image resulting from the subtraction of Figure 5.11 from Figure 5.10. The remaining bright areas are results of minor misalignments between the two images, plus some real differences.

6.0 TESTS ON THE CD4028A TEST DEVICE

6.1 CIRCUIT DESCRIPTION

The CD4028A is a fully static BCD-to-decimal decoder. A positive-true logic input BCD number (0-9) applied to the inputs DCBA causes the corresponding decimal output to go high while the other outputs remain low. The logic diagram of this microcircuit is shown in Figure 6-1. The circuit diagram is shown in Figure 6-2 with the individual MOSFET's labelled by numbers 1 to 120. Although not shown explicitly, the p-well is connected to the V^- terminal, and the n-substrate is connected to the V^+ terminal. The p-well/substrate junction is also omitted from the diagram.

Figure 6-3 is a micrograph of the CD4028A chip with the MOSFET's labelled on the gate electrodes.

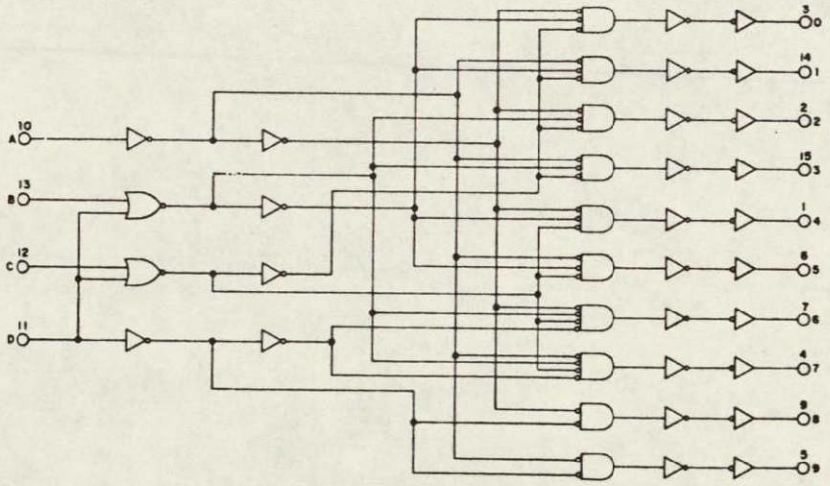

Figure 6-1. Logic diagram of the CD4028A microcircuit.

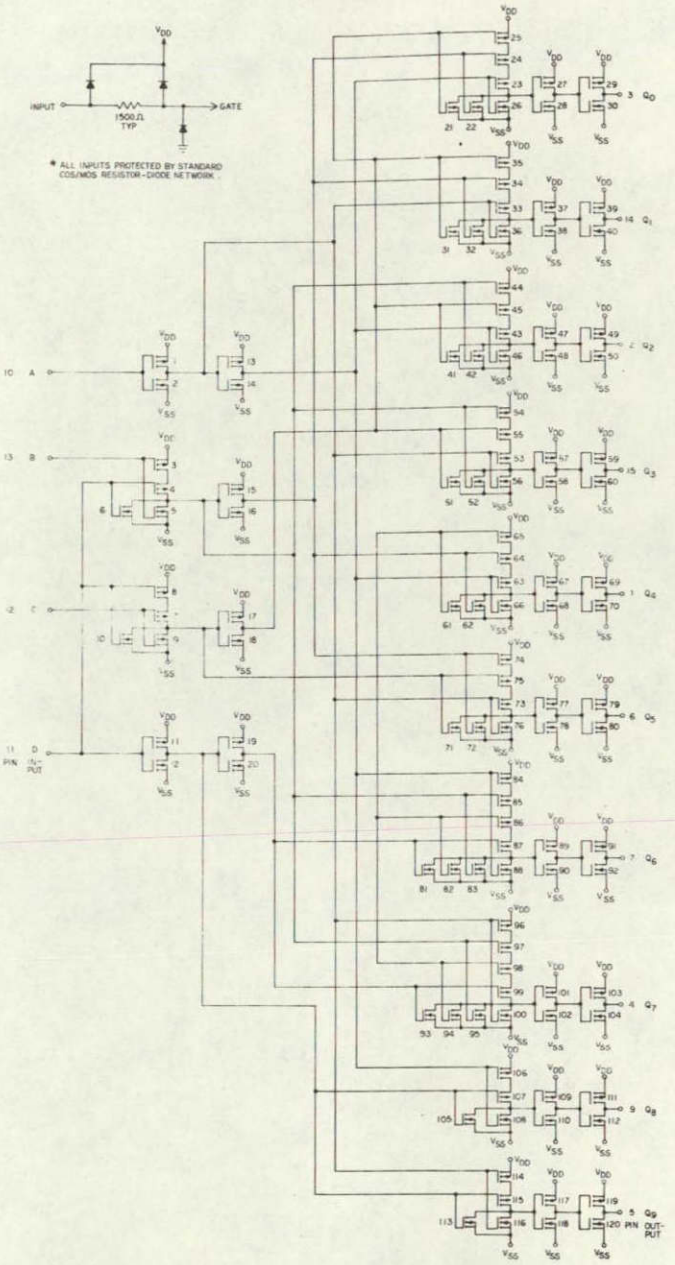

Figure 6-2. Circuit diagram of the CD4028A microcircuit.

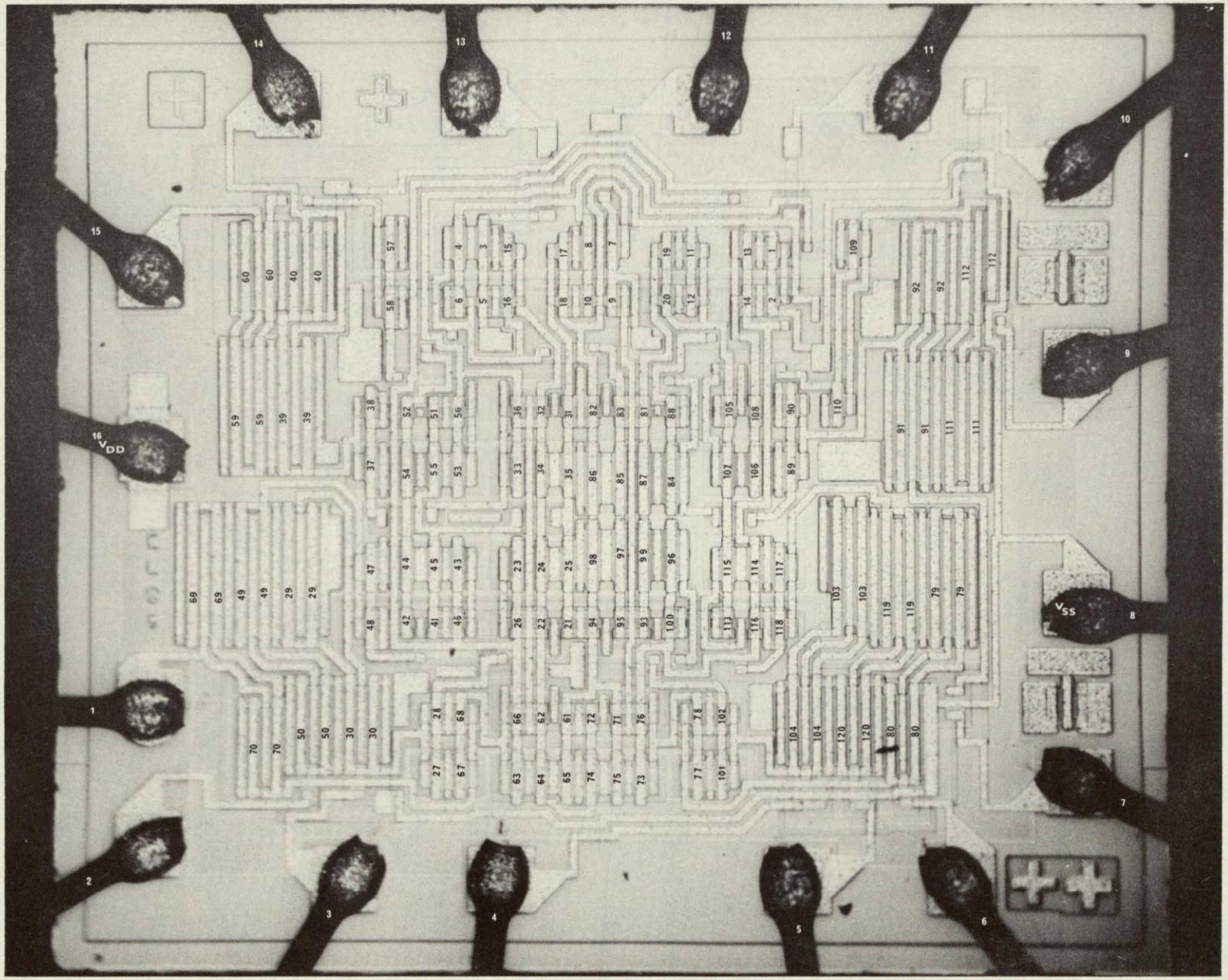

Figure 6-3. Micrograph of the CD4028A microcircuit chip. (1.70 mm x 1.50 mm)

6.2 STATE SUPERPOSITION TEST DEVELOPMENT

In the previous NASA funded optical scanner program, a state superposition program was developed for the CD4028A along with a test circuit to generate the appropriate logic sequences. The state superposition program consisted of the BCD input numbers 0 through 9. This sequence of four bit input words caused all circuit elements on a CD4028 chip to appear in the resulting photoresponse image. A conventionally clocked decade counter was used to generate the sequence of BCD input numbers. Since the duration of each input number was approximately the same, each output inverter driver was imaged with approximately the same intensity.

Also, experiments performed during the previous program revealed that a CD4029A binary/decade presettable up/down counter could not drive the CD4028A directly. A pulse generator was used to clock the CD4029A in the decade upcount mode. The test circuit that was used to drive the CD4028A test devices for the previous program is shown in Figure 6-4.

For this program, it was decided that it would be desirable to image all the devices connected directly to the inputs with approximately the same intensities. This was decided since some of the electrical tests that were devised monitor the characteristics of these transistors. With the previous state superposition program, some of the transistors connected directly to the inputs are imaged with far more intensity than the others simply because they are biased in the correct mode more often. In order to achieve more similar densities from these transistors, it was decided to repeat some of the BCD inputs, specifically the numbers 8 and 9. The circuit used to implement this sequence is shown in Figure 6-5. The input transistors' duty cycles obtained using the circuit developed for this program are shown with those previously obtained in Table 6-1. It can be seen that the duty cycles are not equal but at least the range of duty cycles has been decreased. (For this circuit, it is not possible to obtain equivalent duty cycles for the input transistors.) As a result, the p-channel FETs in the output inverter drivers no longer have exactly the same duty cycles. Instead of each p-channel FET having a duty cycle of 10%, eight have a duty cycle of 8.33% and 2 have a duty cycle of 16.66%.

CD4029B: Presettable Up/Down Counter

CD4050B: Non-inverting Hex Buffer

CD4028A: BCD-to-Decimal Decoder (DUT)

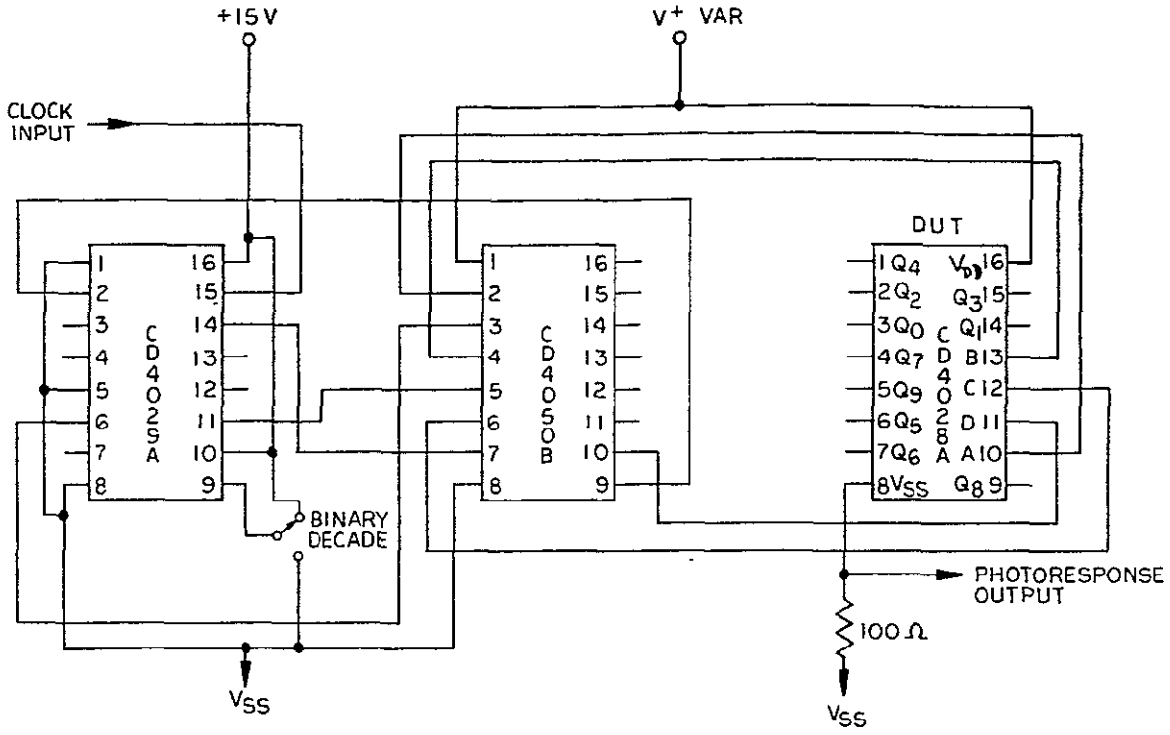

Figure 6.4 CD4028A microcircuit state superposition test circuit used in previous work.

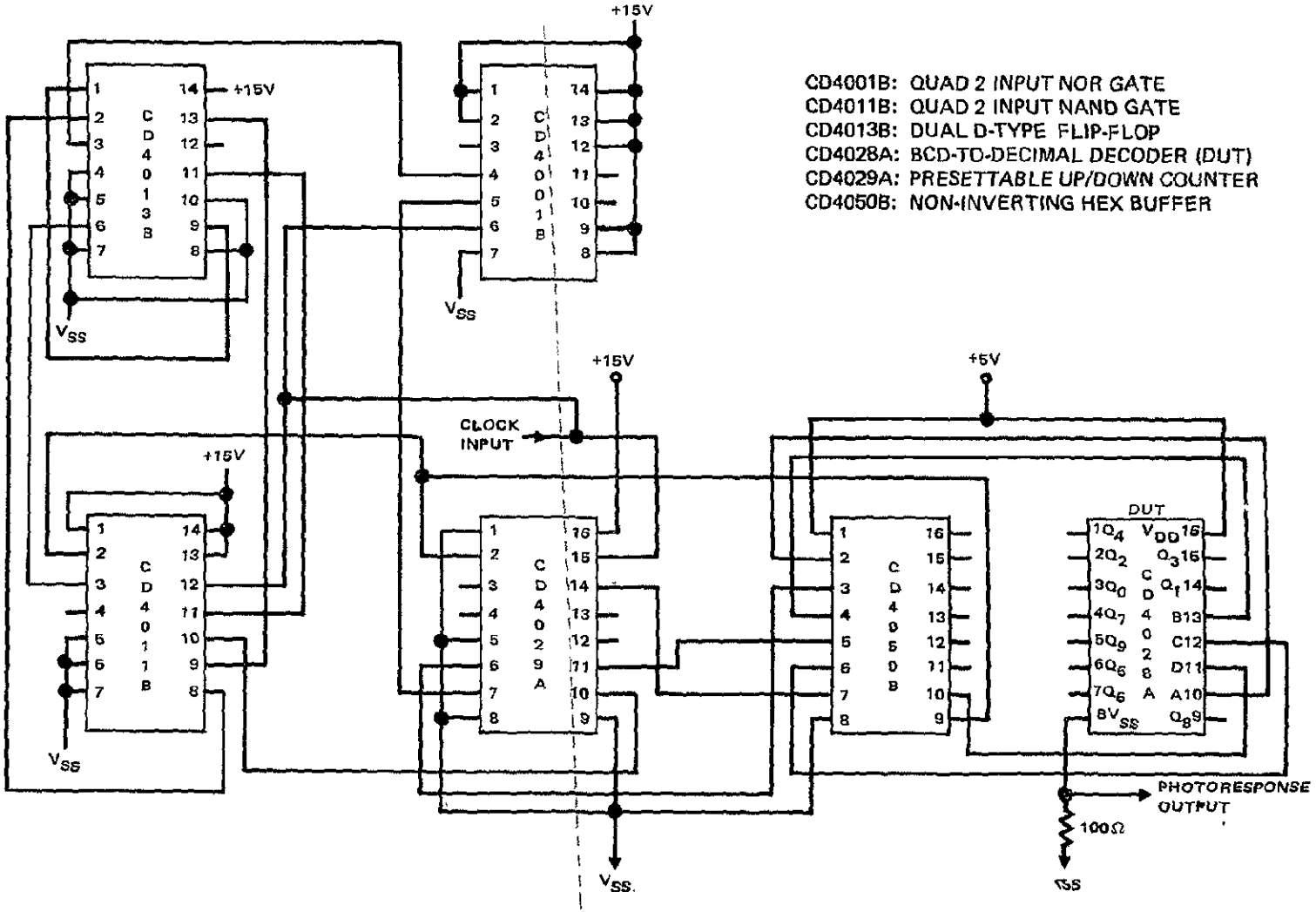

Figure 6-5. CD4028A MICROCIRCUIT STATE SUPERPOSITION TEST CIRCUIT DEVELOPED IN THIS PROGRAM

TABLE 6-1. Comparison of duty cycles for two state superposition programs

TRANSISTOR	DUTY CYCLE 1 (%)	DUTY CYCLE 2 (%)
1	50	50
2	50	50
3	40	33.3
4	20	33.3
5	40	33.3
6	40	33.3
7	40	33.3
8	20	33.3
9	40	33.3
10	40	33.3
11	20	33.3
12	80	66.7

Duty cycle 1 is the one achieved using the circuit from the previous program.

Duty cycle 2 is the one achieved using the circuit developed for this program.

6.3 Electrical Test Description and Results

6.3.1 Electrical Test Description

Electrical parameters were measured on each of the 25 CD4028A test devices prior to any life tests and also after each life test interval. The devices were also tested at these times to determine if they passed a logic funtion test (at V_{DD} = 3.0 volts and V_{DD} = 15.0 volts) and a noise immunity test (at V_{DD} = 5.0 volts, 10.0 volts and 15.0 volts). All of these tests were performed on the Tektronix S-3260 Automatic Test System.

The parameters that were measured on these devices include the following:

T_{PDHL}: propagation delay when switching from "high" to "low"

T_{PDLH}: propagation delay when switching from "low" to "high"

I_L : quiescent device current for each of the ten possible input conditions

I_{IL} : input leakage current with input "low"

I_{IH} : input leakage current with input "high"

V_{TH_N} : N-channel FET threshold voltage

V_{TH_P} : P-channel FET threshold voltages

I_O : output drive currents of both N-and P-channel--output FET's

6.3.2 Electrical Test Results

Tables 6-2a, b and c are computer printouts of the typical results of one of the electrical tests on CD4028A device S/N 1.

As a result of program requirements and the results of the electrical tests following each life-test interval, electrical parameters were measured on the test devices four times during test Runs 1 through 4. The various runs were performed at intervals as described below:

Run 1: Initial electrical parameters prior to any life testing

Run 2: Electrical parameters following 24 hours of life test

Run 3: Electrical parameters following an additional 100 hours of life test (total of 124 hours of life test)

Run 4: Electrical parameters following an additional 376 hours of life test (total of 500 hours of life test)

TABLE 6-2a. Computer Printout of Results of Electrical Parameter Tests of CD4028A Test Device S/N 1.

CD4028A CMOS BCD TO DECIMAL DECODER

SERIAL NUMBER: 1 TEMP: 25 C

PASS LOGIC FUNCTION TEST AT VDD= 15.0 VOLTS

PASS LOGIC FUNCTION TEST AT VDD= 3.00 VOLTS

PASS NOISE IMMUNITY TEST AT VDD= 5.00 VOLTS

PASS NOISE IMMUNITY TEST AT VDD= 10.0 VOLTS

PASS NOISE IMMUNITY TEST AT VDD= 15.0 VOLTS

PROPAGATION DELAY TEST TPDHL

INPUT	OUTPUT	5.0V	LIMIT	10.0V	LIMIT
IA	01	253.5NS	480.0NS MAX	78.00NS	180.0NS MAX
IB	01	232.0NS	480.0NS MAX	71.50NS	180.0NS MAX
IC	01	227.0NS	480.0NS MAX	70.50NS	180.0NS MAX
ID	01	215.5NS	480.0NS MAX	68.50NS	180.0NS MAX
IA	02	203.5NS	480.0NS MAX	63.50NS	180.0NS MAX
IB	02	235.0NS	480.0NS MAX	69.50NS	180.0NS MAX
IC	02	227.0NS	480.0NS MAX	66.50NS	180.0NS MAX
ID	02	217.0NS	480.0NS MAX	67.00NS	180.0NS MAX
IA	03	258.5NS	480.0NS MAX	77.00NS	180.0NS MAX
IB	03	217.5NS	480.0NS MAX	68.00NS	180.0NS MAX
IC	03	229.0NS	480.0NS MAX	68.50NS	180.0NS MAX
ID	03	239.5NS	480.0NS MAX	76.50NS	180.0NS MAX
IA	04	199.0NS	480.0NS MAX	63.50NS	180.0NS MAX
IB	04	216.5NS	480.0NS MAX	67.50NS	180.0NS MAX
IC	04	227.0NS	480.0NS MAX	67.50NS	180.0NS MAX
ID	04	237.0NS	480.0NS MAX	76.00NS	180.0NS MAX
IA	05	263.5NS	480.0NS MAX	78.00NS	180.0NS MAX
IB	05	243.5NS	480.0NS MAX	72.50NS	180.0NS MAX
IC	05	206.0NS	480.0NS MAX	64.50NS	180.0NS MAX
ID	05	243.0NS	480.0NS MAX	75.50NS	180.0NS MAX
IA	06	194.0NS	480.0NS MAX	62.50NS	180.0NS MAX
IB	06	233.5NS	480.0NS MAX	69.50NS	180.0NS MAX
IC	06	191.0NS	480.0NS MAX	60.50NS	180.0NS MAX
ID	06	235.0NS	480.0NS MAX	73.50NS	180.0NS MAX
IA	07	271.0NS	480.0NS MAX	79.00NS	180.0NS MAX
IB	07	236.0NS	480.0NS MAX	75.00NS	180.0NS MAX
IC	07	218.0NS	480.0NS MAX	69.50NS	180.0NS MAX
ID	07	199.5NS	480.0NS MAX	56.00NS	180.0NS MAX
IA	08	213.0NS	480.0NS MAX	69.00NS	180.0NS MAX
IB	08	246.0NS	480.0NS MAX	77.00NS	180.0NS MAX
IC	08	219.0NS	480.0NS MAX	70.50NS	180.0NS MAX
ID	08	205.5NS	480.0NS MAX	58.50NS	180.0NS MAX
IA	09	258.0NS	480.0NS MAX	75.50NS	180.0NS MAX
ID	09	158.0NS	480.0NS MAX	50.50NS	180.0NS MAX
IA	010	194.0NS	480.0NS MAX	62.50NS	180.0NS MAX
ID	010	151.5NS	480.0NS MAX	48.50NS	180.0NS MAX

TABLE 6-2b. Computer Printout of Results of Electrical Parameter Tests of CD4028A Test Device S/N 1.

PROPAGATION DELAY TEST TPDLH

INPUT	OUTPUT	5.0V	LIMIT	10.0V	LIMIT
TA	01	240.5NS	480.0NS MAX	126.5NS	180.0NS MAX
IB	01	270.5NS	480.0NS MAX	119.5NS	180.0NS MAX
IC	01	257.5NS	480.0NS MAX	116.0NS	180.0NS MAX
ID	01	282.5NS	480.0NS MAX	127.0NS	180.0NS MAX
IA	02	202.0NS	480.0NS MAX	89.50NS	180.0NS MAX
IB	02	281.5NS	480.0NS MAX	120.5NS	180.0NS MAX
IC	02	269.0NS	480.0NS MAX	117.5NS	180.0NS MAX
ID	02	295.5NS	480.0NS MAX	130.0NS	180.0NS MAX
IA	03	283.0NS	480.0NS MAX	124.0NS	180.0NS MAX
IB	03	198.5NS	480.0NS MAX	79.00NS	180.0NS MAX
IC	03	256.5NS	480.0NS MAX	113.0NS	180.0NS MAX
ID	03	265.5NS	480.0NS MAX	117.0NS	180.0NS MAX
IA	04	200.0NS	480.0NS MAX	85.00NS	180.0NS MAX
IB	04	208.5NS	480.0NS MAX	80.00NS	180.0NS MAX
IC	04	266.0NS	480.0NS MAX	113.0NS	180.0NS MAX
ID	04	274.5NS	480.0NS MAX	117.5NS	180.0NS MAX
IA	05	284.5NS	480.0NS MAX	124.5NS	180.0NS MAX
IB	05	276.5NS	480.0NS MAX	118.5NS	180.0NS MAX
IC	05	188.5NS	480.0NS MAX	70.00NS	180.0NS MAX
ID	05	282.0NS	480.0NS MAX	122.5NS	180.0NS MAX
IA	06	195.5NS	480.0NS MAX	87.50NS	180.0NS MAX
IB	06	287.5NS	480.0NS MAX	126.0NS	180.0NS MAX
IC	06	190.0NS	480.0NS MAX	70.00NS	180.0NS MAX
ID	06	287.5NS	480.0NS MAX	127.0NS	180.0NS MAX
IA	07	295.5NS	480.0NS MAX	130.5NS	180.0NS MAX
IB	07	219.0NS	480.0NS MAX	87.00NS	180.0NS MAX
IC	07	209.5NS	480.0NS MAX	77.00NS	180.0NS MAX
ID	07	224.0NS	480.0NS MAX	105.0NS	180.0NS MAX
IA	08	202.0NS	480.0NS MAX	92.50NS	180.0NS MAX
IB	08	218.0NS	480.0NS MAX	89.00NS	180.0NS MAX
IC	08	208.0NS	480.0NS MAX	79.00NS	180.0NS MAX
ID	08	223.5NS	480.0NS MAX	107.5NS	180.0NS MAX
IA	09	261.0NS	480.0NS MAX	120.5NS	180.0NS MAX
ID	09	151.0NS	480.0NS MAX	69.00NS	180.0NS MAX
IA	010	165.0NS	480.0NS MAX	80.00NS	180.0NS MAX
ID	010	143.5NS	480.0NS MAX	66.00NS	180.0NS MAX

QUIESCENT DEVICE CURRENT IL

CONDITION D C B A	MEASUREMENT	LIMIT
0 0 0 0	7.835UA	10.0UA MAX
0 0 0 1	7.820UA	10.0UA MAX
0 0 1 0	7.775UA	10.0UA MAX
0 0 1 1	7.645UA	10.0UA MAX
0 1 0 0	7.805UA	10.0UA MAX
0 1 0 1	7.820UA	10.0UA MAX
0 1 1 0	7.805UA	10.0UA MAX
0 1 1 1	7.730UA	10.0UA MAX
1 0 0 0	7.785UA	10.0UA MAX
1 0 0 1	7.780UA	10.0UA MAX

TABLE 6-2c. Computer Printout of Results of Electrical Parameter Tests of CD4028A Test Device S/N 1.

INPUT CURRENT TEST

INPUT	IIL	LIMIT	IIH	LIMIT
I1	2.[illegible]NA	-1[illegible].0UA MAX	-7.750NA	100.NA MAX
I0	-4.150[illegible]	-100.0NA MAX	-1.350NA	100.NA MAX
I8	3.[illegible]	-100.0NA MAX	-1.750NA	100.NA MAX
I9	-4.[illegible]	-100.0UA MAX	-3.050NA	100.NA MAX

OUTPUT DRIVE CURRENT

N-CHANNEL:

OUTPUT	VDD=5V	LIMIT	VDD=10V	LIMIT
O1	1.[illegible]MA	600.0UA MIN	2.52MA	1.200MA MIN
O2	1.61MA	600.0UA MIN	3.01MA	1.200MA MIN
O3	1.[illegible]MA	600.0UA MIN	2.03MA	1.200MA MIN
O4	1.35MA	600.0UA MIN	2.26MA	1.200MA MIN
O5	1.14MA	600.0UA MIN	1.75MA	1.200MA MIN
O6	1.67MA	600.0UA MIN	3.16MA	1.200MA MIN
O7	1.35MA	600.0UA MIN	2.27MA	1.200MA MIN
O8	1.23MA	600.0UA MIN	1.91MA	1.200MA MIN
O9	1.71MA	600.0UA MIN	3.37MA	1.200MA MIN
O10	1.38MA	600.0UA MIN	2.32MA	1.200MA MIN

P-CHANNEL:

OUTPUT	VDD=5V	LIMIT	VDD=10V	LIMIT
O1	-965.[illegible]	-370.0UA MIN	-1.92MA	-900.0UA MIN
O2	-967.[illegible]	-370.0UA MIN	-2.03MA	-900.0UA MIN
O3	-947.[illegible]	-370.0UA MIN	-1.95MA	-900.0UA MIN
O4	-989.[illegible]	-370.0UA MIN	-2.10MA	-900.0UA MIN
O5	-1.07[illegible]A	-370.0UA MIN	-2.29MA	-900.0UA MIN
O6	-869.[illegible]	-370.0UA MIN	-1.61MA	-900.0UA MIN
O7	-922.[illegible]	-370.0UA MIN	-1.77MA	-900.0UA MIN
O8	-884.[illegible]	-370.0UA MIN	-1.61MA	-900.0UA MIN
O9	-916.[illegible]	-370.0UA MIN	-1.74MA	-900.0UA MIN
O10	-862.[illegible]	-370.0UA MIN	-1.60MA	-900.0UA MIN

THRESHOLD VOLTAGE

ORIGINAL PAGE IS OF POOR QUALITY

N-CHANNEL

VTHN(1.000) = -2.24 V LIMITS: -700.MV TO -3.00 V

VTHN(2.000) = -2.21 V LIMITS: -700.MV TO -3.00 V

VTHN(3.000) = -2.25 V LIMITS: -700.MV TO -3.00 V

VTHN(4.000) = -2.23 V LIMITS: -700.MV TO -3.00 V

P-CHANNEL

VTHP(1.000) = 2.46 V LIMITS: 3.00 V TO 700.MV

VTHP(2.000) = 2.27 V LIMITS: 3.00 V TO 700.MV

VTHP(3.000) = 2.28 V LIMITS: 3.00 V TO 700.MV

VTHP(4.000) = 2.46 V LIMITS: 3.00 V TO 700.MV

Summaries of the electrical test results for the following parameters are presented in the table shown:

Table 6.3: Maximum and minimum values of all T_{PDHL} and T_{PDLH} times for each device at each run

Table 6.4: Average of the ten I_L values for each device at each run

Table 6.5: Average of the four V_{THN} values for each device at each run

Table 6.6: Average of the four V_{THP} values for each device at each run

Table 6.7: Average of the ten I_0 values for the N-channel FET's and the P-channel FET's at each run

The parameters I_{IH} and I_{IL} were not tabulated since the numbers were not very accurate due to the sensitivity of the test. These values were typically on the order of a few nanoamperes or less. All the devices I_{IH} and I_{IL} parameters were well within specified limits except for device S/N 2. At Runs 3 and 4, I_{IL} for this device was 100 microamperes which is far above the specified maximum of 100 nA.

All devices passed all function tests and noise immunity tests except device S/N 21 which failed all these tests at Runs 3 and 4.

The electrical tests can be summarized by stating that most parameters were fairly constant throughout the testing, except for the parameters of devices S/N 2 and S/N 21. The average power supply current $\overline{I_L}$, dropped for most devices from Run 1 to Run 2 but then stayed fairly constant throughout the rest of the tests. This has been attributed to the devices having been opened to ambient atmosphere for a long period prior to Run 1 and becoming somewhat leaky. Following Run 1 the devices were subjected to a 24 hour life test at 125°C which reduced the leakage currents back to the original levels.

CD4028A test devices S/N 2 and S/N 21 both failed several parametric tests at Runs 3 and 4. Examination of these devices revealed that the causes of these failures were not related to the life-testing to which they had been subjected. Rather, both had suffered mechanical damage to their internal bonds during handling. Device S/N 2 had one of its internal input leads squashed against the edge of the chip, causing a resistive short between this input and V_{DD}. Device S/N 21 had one of its internal output leads broken. Scanning electron micrographs of the two failed devices are shown in Figures 6.6 through 6.9

6.4 Life Tests

The CD4028A test devices were submitted to three life-test intervals. The initial life test interval was 24 hours long. Following this life test, the electrical parameters of the devices were measured and reviewed. Since there had

TABLE 6.3 CD4028: PROPAGATION DELAY TIMES

	RUN 1		RUN 2		RUN 3		RUN 4	
DEVICE S/N	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
1	296	143	295	140	304	148	301	148
2	269	129	268	126	274	133	273	135
3	250	123	250	120	257	127	252	128
4	238	116	239	114	247	121	245	121
5	227	113	226	111	235	118	232	117
6	267	130	267	126	275	133	272	134
7	307	142	305	139	311	146	307	146
8	279	139	277	136	287	144	284	143
9	259	131	259	129	267	137	263	137
10	277	137	275	130	282	139	277	138
11	282	137	281	133	292	142	287	141
12	272	128	271	125	277	133	271	132
13	284	133	283	130	289	138	283	137
14	266	128	264	124	274	132	270	131
15	281	135	279	133	285	140	280	140
16	257	124	255	121	260	129	255	128
17	250	119	247	117	256	125	252	123
18	188	93	186	90	(A)	(A)	192	98
19	174	90	173	87	181	94	178	93
20	154	78	152	75	158	83	155	81
21	232	116	230	113	(B)	(B)	(B)	(B)
22	260	128	259	124	268	132	263	131
23	266	130	265	128	273	137	268	135
24	278	132	276	129	282	137	277	135
25	253	128	251	124	258	132	252	132
Average	255	124	253	121	265	130	258	129
Standard Deviation	36	16	36	16	34	15	36	16

ALL VALUES ARE NANOSECONDS

(A) PARAMETERS WERE NOT MEASURED ON DEVICE S/N 18 AT RUN 3

(B) DEVICE S/N 21 FAILED AFTER RUN 2

TABLE 6.4 CD4028: AVERAGE POWER SUPPLY CURRENT ($\overline{I_L}$) .

DEVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	7.80	7.00	6.96	6.95
2	7.17	6.99	8.09	10.47
3	7.06	6.98	6.96	7.07
4	8.14	7.01	6.97	6.95
5	8.74	7.00	6.96	6.96
6	8.88	7.00	6.97	6.96
7	7.36	6.98	6.97	6.95
8	7.10	6.99	6.97	6.96
9	7.06	7.00	6.97	6.96
10	7.22	6.99	6.97	6.96
11	7.99	6.99	6.97	6.96
12	8.57	7.00	6.97	6.95
13	8.84	6.98	6.97	6.95
14	7.70	6.99	6.97	6.95
15	7.19	6.98	6.97	6.95
16	7.08	6.98	6.97	6.96
17	7.05	7.00	6.96	6.96
18	7.60	7.01	(A)	6.96
19	8.28	7.00	6.97	6.96
20	8.53	7.01	6.97	6.95
21	8.75	6.99	(B)	(B)
22	7.57	6.99	6.97	6.95
23	7.16	7.00	6.96	6.96
24	7.07	6.99	6.96	6.96
25	7.05	7.00	6.96	6.95
Average	7.72	6.99	6.97(C)	6.96(C)
Standard Deviation	0.66	0.009	0.004	0.02

ALL VALUES ARE MICROAMPERES

(A) PARAMETERS WERE NOT MEASURED ON DEVICE S/N 18 AT RUN 3

(B) DEVICE S/N 21 FAILED AFTER RUN 2

(C) DEVICE S/N 2 VALUES NOT INCLUDED IN THESE CALCULATIONS

TABLE 6.5 CD4028: AVERAGE N-CHANNEL FET THRESHOLD VOLTAGES ($\overline{V_{TH_N}}$)

DEVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	-2.32	-2.22	-2.23	-2.25
2	-2.28	-2.26	-2.26	-2.29
3	-2.23	-2.21	-2.23	-2.24
4	-2.18	-2.17	-2.18	-2.20
5	-2.17	-2.18	-2.18	-2.19
6	-2.27	-2.25	-2.26	-2.29
7	-2.26	-2.24	-2.25	-2.28
8	-2.24	-2.24	-2.24	-2.26
9	-2.20	-2.21	-2.23	-2.26
10	-2.20	-2.20	-2.21	-2.23
11	-2.26	-2.24	-2.25	-2.28
12	-2.24	-2.23	-2.24	-2.26
13	-2.28	-2.27	-2.27	-2.30
14	-2.24	-2.24	-2.25	-2.26
15	-2.25	-2.24	-2.25	-2.27
16	-2.26	-2.25	-2.26	-2.27
17	-2.07	-2.07	-2.08	-2.09
18	-2.11	-2.11	(A)	-2.12
19	-1.83	-1.82	-1.83	-1.84
20	-1.45	-1.44	-1.46	-1.47
21	-2.18	-2.18	-2.19	-2.20
22	-2.25	-2.24	-2.25	-2.27
23	-2.21	-2.23	-2.25	-2.27
24	-2.26	-2.25	-2.25	-2.27
25	-2.26	-2.25	-2.25	-2.27
Average	-2.18	-2.17	-2.18	-2.20
Standard Deviation	0.18	0.17	0.18	0.18

ALL VALUES ARE VOLTS

(A) PARAMETERS WERE NOT MEASURED ON DEVICE S/N 18 AT RUN 3

TABLE 6.6 CD4028: AVERAGE P-CHANNEL FET THRESHOLD VOLTAGES ($\overline{V_{TH_P}}$)

DEVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	2.37	2.38	2.37	2.37
2	2.31	2.31	2.09	1.87
3	2.28	2.27	2.28	2.27
4	2.27	2.27	2.27	2.27
5	2.30	2.30	2.30	2.30
6	2.30	2.30	2.30	2.30
7	2.40	2.40	2.40	2.40
8	2.29	2.29	2.29	2.29
9	2.36	2.36	2.36	2.36
10	2.40	2.40	2.40	2.40
11	2.37	2.37	2.38	2.37
12	2.35	2.35	2.35	2.35
13	2.34	2.34	2.34	2.34
14	2.28	2.28	2.28	2.28
15	2.39	2.39	2.39	2.39
16	2.30	2.30	2.30	2.30
17	2.43	2.43	2.44	2.43
18	1.89	1.89	(A)	1.89
19	1.92	1.92	1.92	1.92
20	1.84	1.84	1.84	1.84
21	2.28	2.28	2.28	2.29
22	2.31	2.30	2.30	2.30
23	2.37	2.37	2.37	2.37
24	2.37	2.37	2.37	2.37
25	2.27	2.27	2.27	2.27
Average	2.28	2.28	2.30(B)	2.28(B)
Standard Deviation	0.15	0.15	0.14(B)	0.16(B)

ALL VALUES ARE VOLTS

(A) PARAMETERS WERE NOT MEASURED ON DEVICE S/N 18 AT RUN 3

(B) DEVICE 2 NOT INCLUDED IN CALCULATION OF THESE VALUES

TABLE 6.7 CD4028: AVERAGE OUTPUT DRIVE CURRENT

	RUN 1		RUN 2		RUN 3		RUN 4	
DEVICE S/N	N	P	N	P	N	P	N	P
1	1.42	0.94	1.41	0.94	1.41	0.92	1.43	0.94
2	1.42	0.96	1.42	0.95	1.43	0.93	1.43	0.94
3	1.47	1.00	1.46	0.99	1.47	0.97	1.48	0.99
4	1.54	1.08	1.52	1.06	1.54	1.04	1.55	1.06
5	1.61	1.12	1.59	1.11	1.60	1.08	1.62	1.10
6	1.39	0.98	1.39	0.98	1.40	0.96	1.41	0.97
7	1.39	0.87	1.39	0.86	1.40	0.85	1.41	0.86
8	1.40	1.00	1.39	1.00	1.40	0.97	1.42	0.99
9	1.43	0.93	1.41	0.93	1.42	0.91	1.42	0.93
10	1.49	0.89	1.48	0.88	1.48	0.87	1.50	0.88
11	1.38	0.90	1.37	0.90	1.38	0.88	1.40	0.90
12	1.47	0.93	1.46	0.93	1.46	0.91	1.48	0.93
13	1.42	0.89	1.42	0.89	1.43	0.87	1.44	0.88
14	1.43	1.03	1.42	1.03	1.43	1.01	1.45	1.03
15	1.41	0.87	1.40	0.86	1.41	0.85	1.43	0.86
16	1.44	1.01	1.42	1.00	1.44	0.99	1.46	1.01
17	1.68	0.98	1.66	0.97	1.67	0.96	1.69	0.97
18	1.69	1.27	1.68	1.26	(A)	(A)	1.71	1.26
19	1.70	1.36	1.69	1.35	1.71	1.32	1.73	1.35
20	1.89	1.35	1.87	1.35	1.88	1.32	1.90	1.35
21	1.58	1.06	1.58	1.06	(B)	(B)	(B)	(B)
22	1.45	0.96	1.44	0.95	1.45	0.93	1.47	0.95
23	1.44	0.91	1.42	0.91	1.43	0.89	1.44	0.91
24	1.42	0.91	1.41	0.91	1.42	0.89	1.44	0.91
25	1.43	0.98	1.42	0.98	1.43	0.96	1.44	0.97
Average	1.50	1.01	1.49	1.00	1.48	0.97	1.51	1.00
Standard Deviation	0.13	0.13	0.12	0.13	0.12	0.12	0.13	0.14

ALL VALUES ARE MILLIAMPERES

(A) PARAMETERS WERE NOT MEASURED ON DEVICE S/N 18 AT RUN 3

(B) DEVICE S/N 21 FAILED AFTER RUN 2

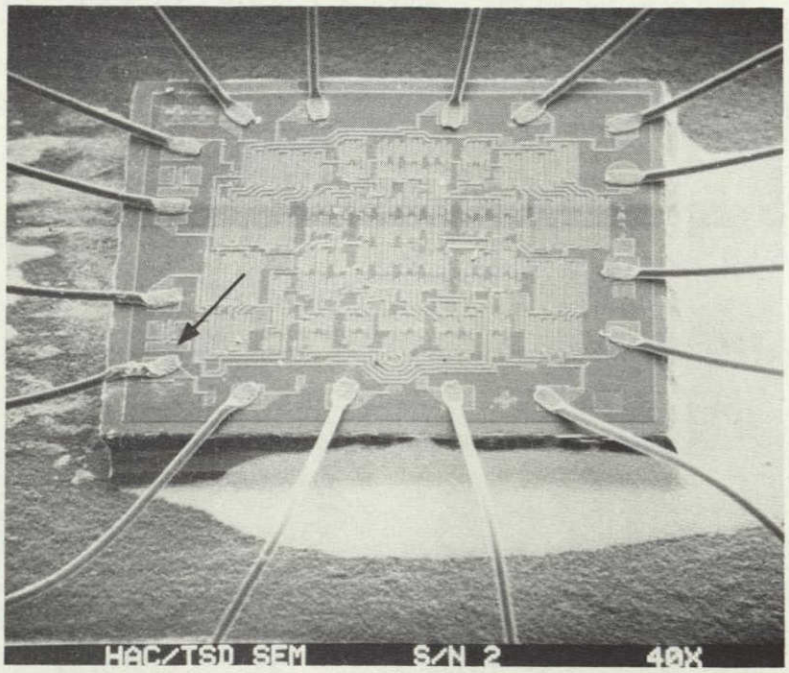

Figure 6.6. Scanning electron micrograph showing the overall chip and internal bonds of CD4028A test device S/N 2. The bond indicated by the arrow is shown in Figure 6.7.

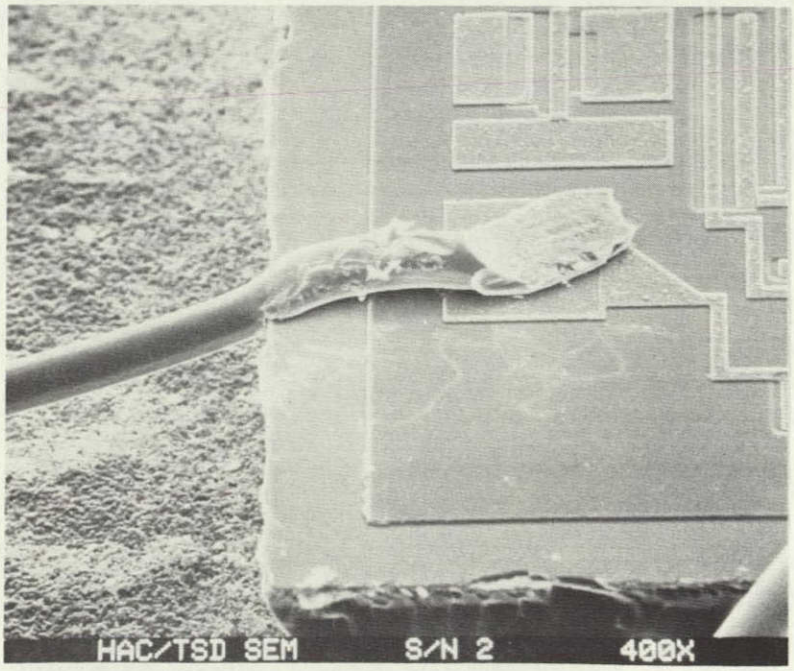

Figure 6.7. Scanning electron micrograph of one of the bonds in CD4028A test device S/N 2. It can be seen that it has been mechanically damaged and it is in contact with the edge of the chip.

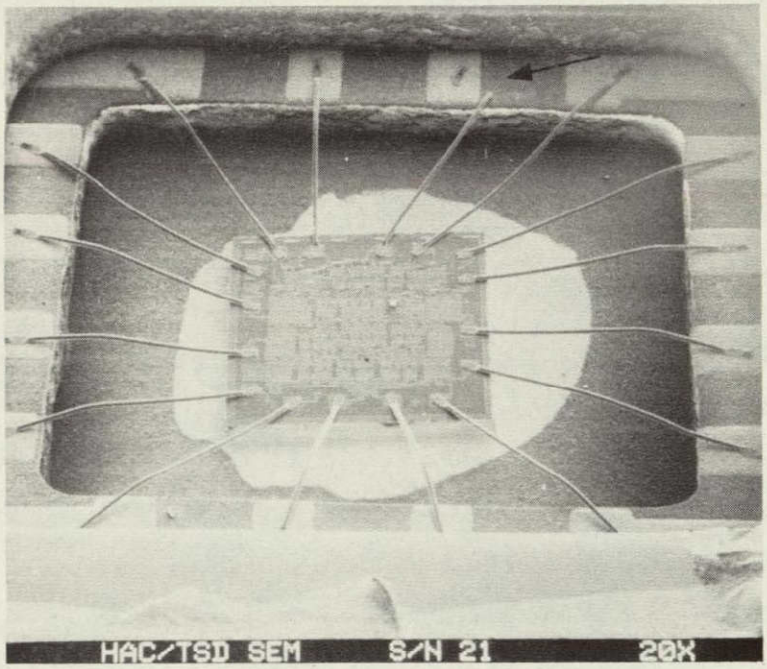

Figure 6.8. Scanning electron micrograph of the die cavity of CD4028A test device S/N 21. The bond indicated by the arrow is shown in Figure 6.9.

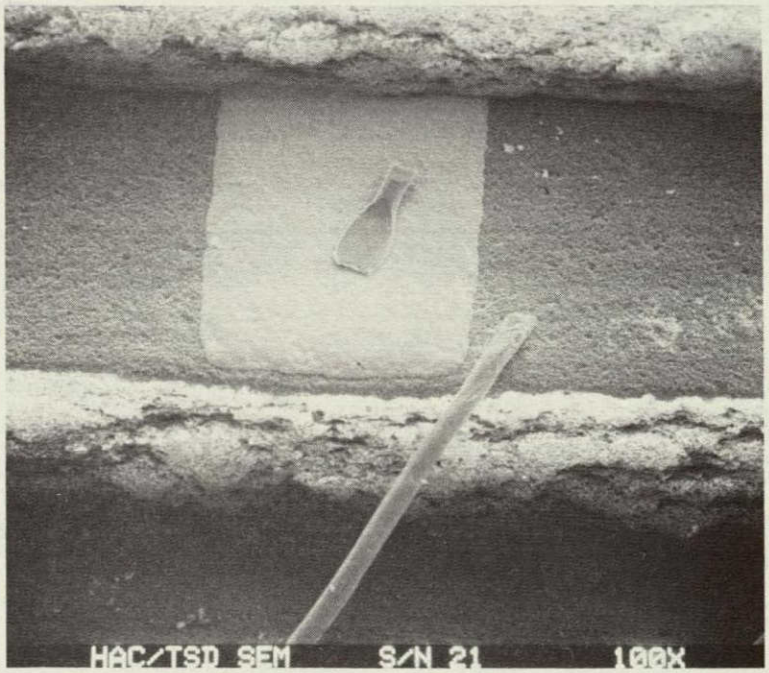

Figure 6.9. Scanning electron micrograph of a bond in CD4028A test device S/N 21. Mechanical damage has resulted in the bond having been broken.

been no significant changes in the electrical parameters, the next life test period was chosen to be 100 hours in duration. Review of the electrical parameters measured following this life test interval again revealed no significant changes. The third life test was chosen to be 376 hours long, which when added to the two previous intervals, totaled 500 hours of life test on each part. This was the maximum amount of life testing required for this program and also the maximum amount of time available within the limits of the program schedule. Unfortunately, there was still no significant change in the electrical parameters of the devices. (Devices S/N 2 and S/N 21 both failed several electrical parameters at Runs 3 and 4 but these failures were not related to the effects of the life-tests.)

The test devices were life-tested using the circuit shown in Figure 6-10. The parts were heated to 125°C during the life tests in ovens that were purged with dry nitrogen gas. Since the devices had been unlidded for optical access to the chip, the dry nitrogen gas was used to prevent the devices from being subjected to gases or water vapor which might contaminate the semiconductor chip.

6.5 Photoresponse Image Recording

Photoresponse images of all twenty-five CD4028A test devices were recorded on magnetic tape. These images were recorded prior to any life tests (Run 1), following 24 hours of life tests (Run 2), following an additional 100 hours of life tests (Run 3), and following an additional 376 hours of life test (Run 4). At each interval images from devices S/N 1 through S/N 7 were recorded serially on one magnetic tape, images from devices S/N 8 through S/N 14 were recorded on another tape, images from devices S/N 15 through S/N 21 were recorded on another tape, and images from devices S/N 22 through S/N 25 were recorded on another tape. Four tapes of serially recorded images were recorded at each test interval.

During the optical scanner examination of each device, the device was run with a power supply voltage of 5V. The test device was switched using the State Superposition test circuit described previously. The CD4029A counter in the test circuit was run with a clock frequency of 3.5 MHz. All circuits were fully operational under these conditions.

6.6 Correlation of Photoresponse Images with Electrical Test Results

Obviously, due to time and financial limitations not all of the photoresponse images from all of the test devices could be subtracted from each other in order to try to find differences that could be correlated with electrical test results

B Terminals are BCD (Binary Coded Decimal) inputs.

D Terminals are Decimal decoded outputs.

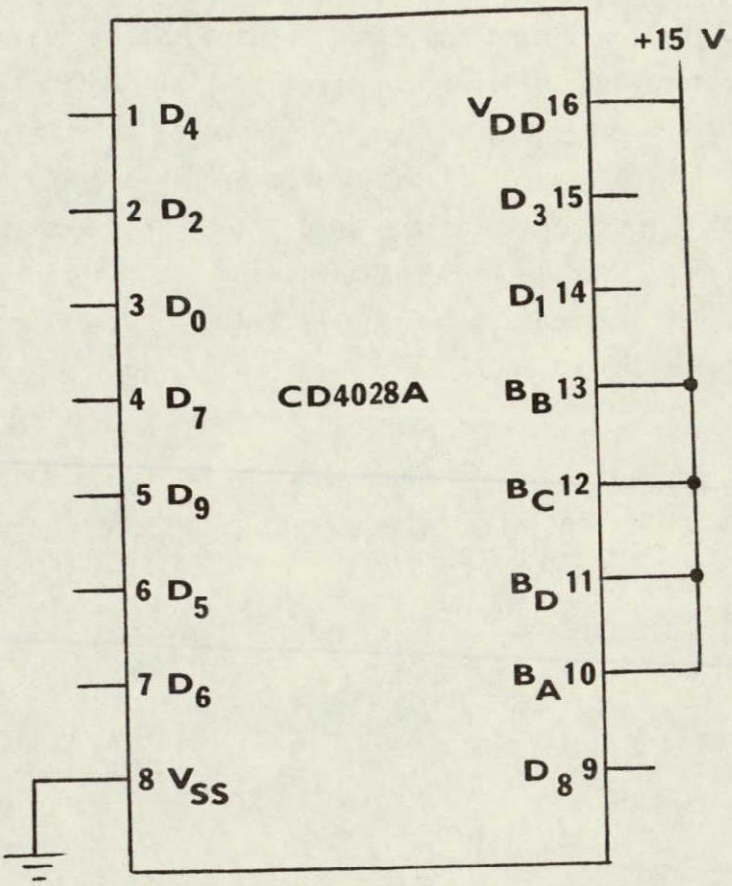

Figure 6-10. Life-test circuit for CD4028A. (Connections to all terminals except 8 and 16 are made through 47KΩ resistors.)

(or to try to find differences that could not be correlated with electrical test results). In order to attempt to pick some meaningful photoresponse images which would be analyzed, the electrical test results were reviewed.

Correlation 1

The first correlation that was to be attempted was to try to correlate differences in devices' electrical parameters with differences in photoresponse images. The electrical test data was reviewed in order to try to find devices whose electrical parameters were different from the others. If a device's electrical parameter differed from the average value for that parameter by more than two standard deviations, it was classified as "significantly different". (A simple criteria such as a parameter being outside of specification limits could not be used, since all of the devices initial electrical parameters were well within specification limits.) As a result of this criteria, two devices were quite consistently shown to be "mavericks". These two devices were S/N 19 and S/N 20. (Test device S/N 18 had two parameters which were "significantly different" from the average.) Table 6.8 lists the various tabulated parameters and shows which devices had parameters significantly different from the average. Except for devices S/N 18, S/N 19 and S/N 20, all other devices' parameters were less than two standard deviations from the average.

TABLE 6.8

Summary of Devices with "Significantly Different" Parameters

PARAMETER	S/N 18	S/N 19	S/N 20
T_{PD} (max)	N	D	D
T_{PD} (min)	N	D	D
$\overline{I}_L$	N	N	N
$\overline{V}_{TH_N}$	N	D	D
$\overline{V}_{TH_P}$	D	D	D
$\overline{I}_o$(N)	N	N	D
$\overline{I}_o$(P)	D	D	D

"D" indicates the devices parameter was more than 2 standard deviations from the average.

"N" indicates the devices parameter was less than 2 standard deviations from the average.

Devices S/N 19 and S/N 20 were chosen to represent devices whose electrical parameters were different from the average. (Device S/N 18 had only two parameters that were "significantly different" from the average.)

In order to perform comparisons several devices had to be chosen to represent a "normal" or average device. As previously noted, when the photoresponse images were recorded, the images from devices S/N 15 through S/N 21 were recorded on one tape. For ease of data handling and a reduced number of tapes that would have to be processed, the parameters from devices S/N 15, 16, 17 and 21 were reviewed to determine if they represented fairly average samples. It was found that their parameters were all fairly close to the average values of the parameters for the entire group. Therefore, these devices were used as "average" devices for purposes of comparisons.

Figures 6-11 through 6-16 are the photoresponse images of devices S/N 15, S/N 16, S/N 17, S/N 19, S/N 20 and S/N 21 recorded at Run 1. (These figures are photographs created at the image processing facility.) The image from device S/N 15 has some "noise" in its background from an undetermined cause.

The first subtractions that were performed were between images of "average" devices to determine if there were large differences between devices with similar parameters. Figures 6-17 and 6-18 show the results of subtractions between the images from devices S/N 15 and 16. It can be seen that there are no large differences except for some caused by a slight misalignment of the two images.

Figures 6-19 and 6-20 show the results of subtractions between the images from "average" devices S/N 16 and 17. Figure 6-19, which shows the results of subtracting the image from device S/N 16 from the image of device S/N 17, reveals some significant differences in the area of the device inputs. Another examination of the electrical data revealed that these two devices had quite a large difference (more than one standard duration) in their $\overline{V}_{THN}$ parameters and a considerable difference in their $\overline{V}_{THP}$ parameters (almost one standard deviation). Since these parameters measure threshold voltages on the devices inputs, it is apparent that there is a good correlation with the observed differences in the photoresponse images and the differences in the electrical parameters. Subtractions between the images from devices S/N 15 and S/N 17 are shown in Figures 6-21 and 6-22. Again the subtractions revealed differences in the areas of the device inputs which correlated well with a large difference in the devices' $\overline{V}_{THN}$ parameters.

Subtractions between the other "average" device images, the images from device S/N 21 and the image from device S/N 16 revealed virtually no differences. The results from the subtractions of these two images shown in Figures 6-23 and 6-24, show that there is virtually nothing left, indicating that the alignment between these two devices was also particularly good.

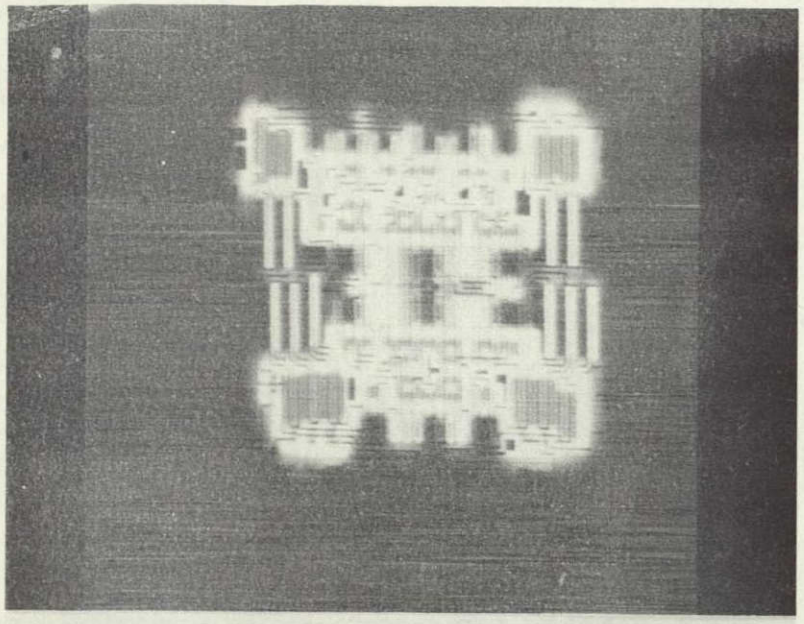

Figure 6.11. Photoresponse image from device S/N 15. The cause of the background noise was undetermined. Device S/N 15 was an "average" device.

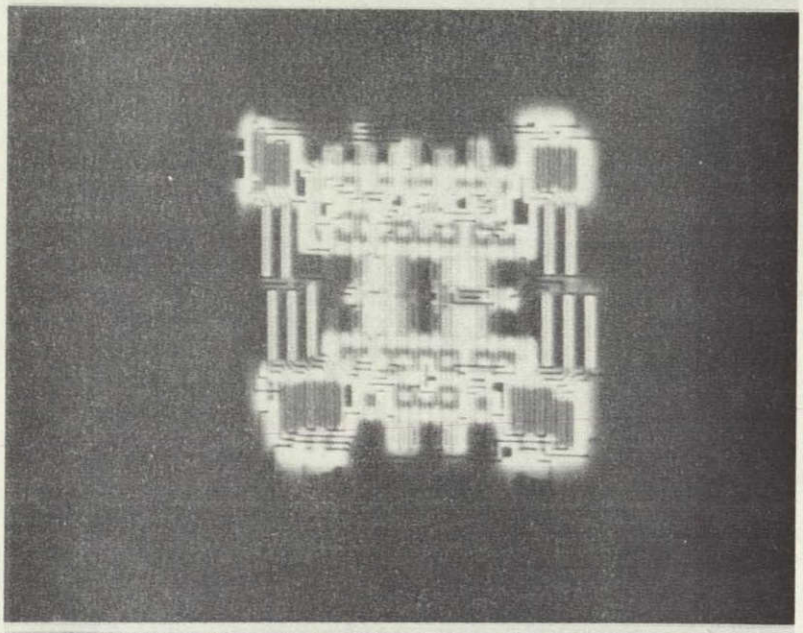

Figure 6.12. Photoresponse image from device S/N 16, an "average" device.

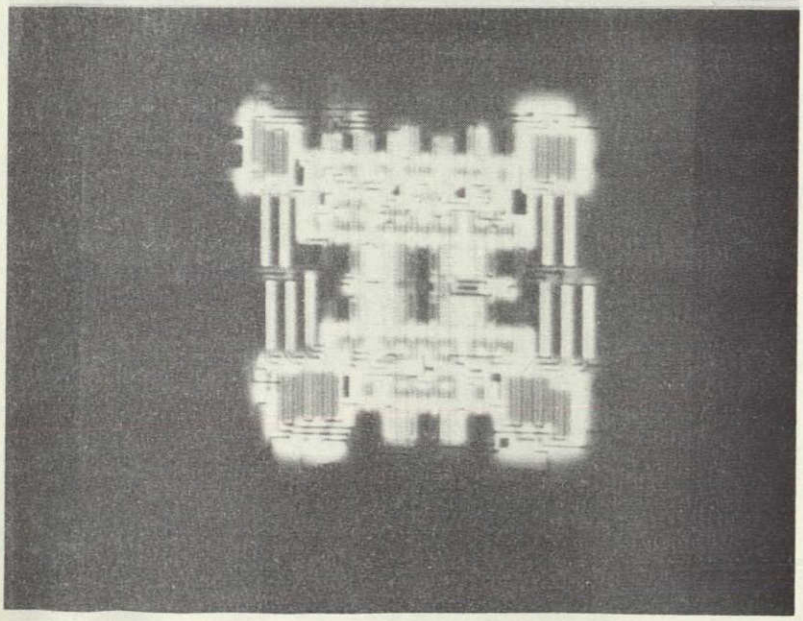

Figure 6.13. Photoresponse image from device S/N 17, an "average" device.

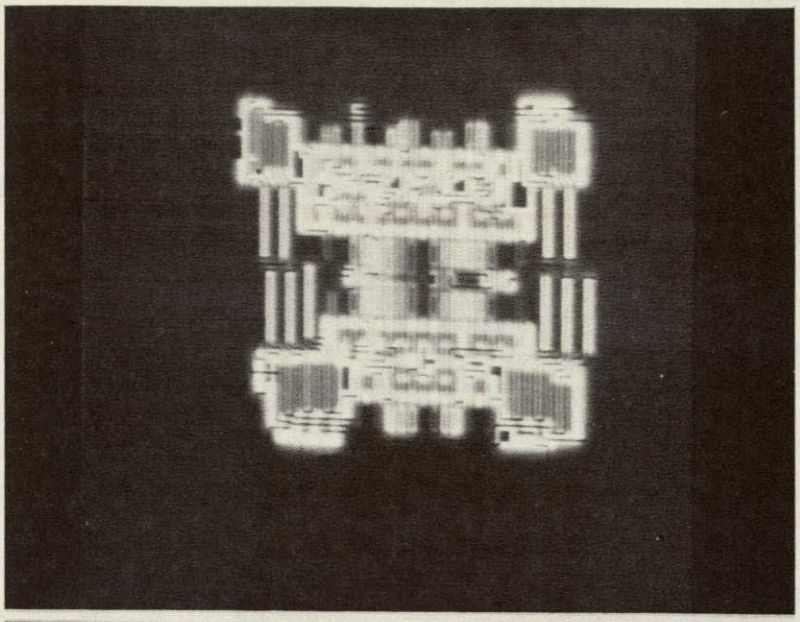

Figure 6.14. Photoresponse image from device S/N 19, a "significantly different" device.

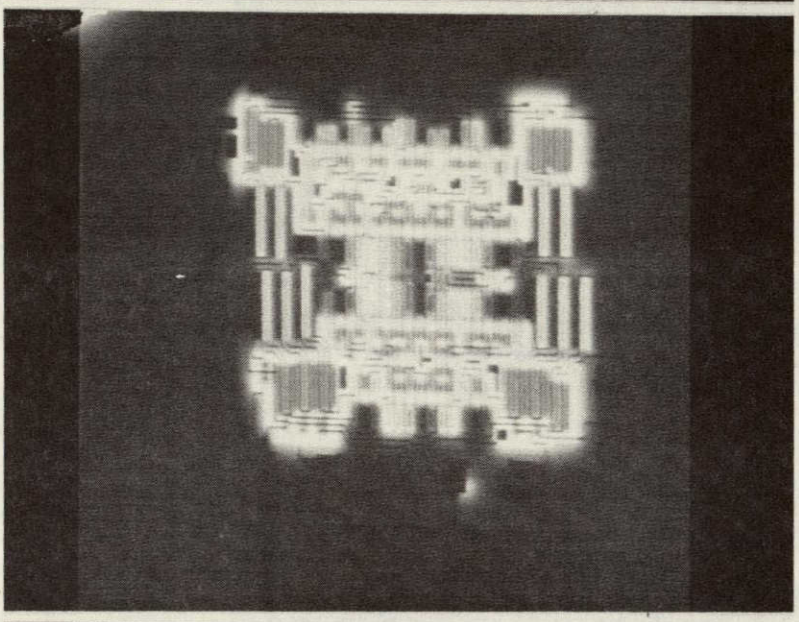

Figure 6.15. Photoresponse image from device S/N 20, a "significantly different" device.

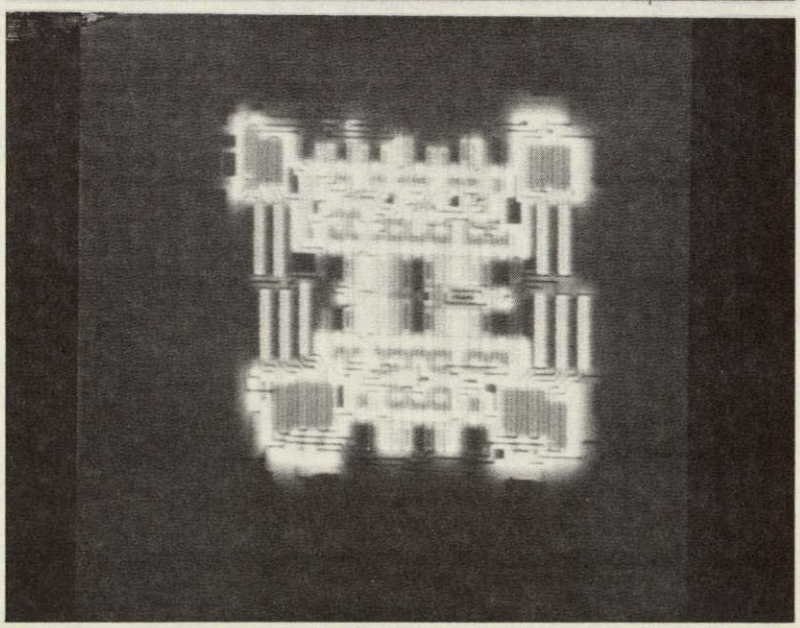

Figure 6.16. Photoresponse image from device S/N 21, an "average" device.

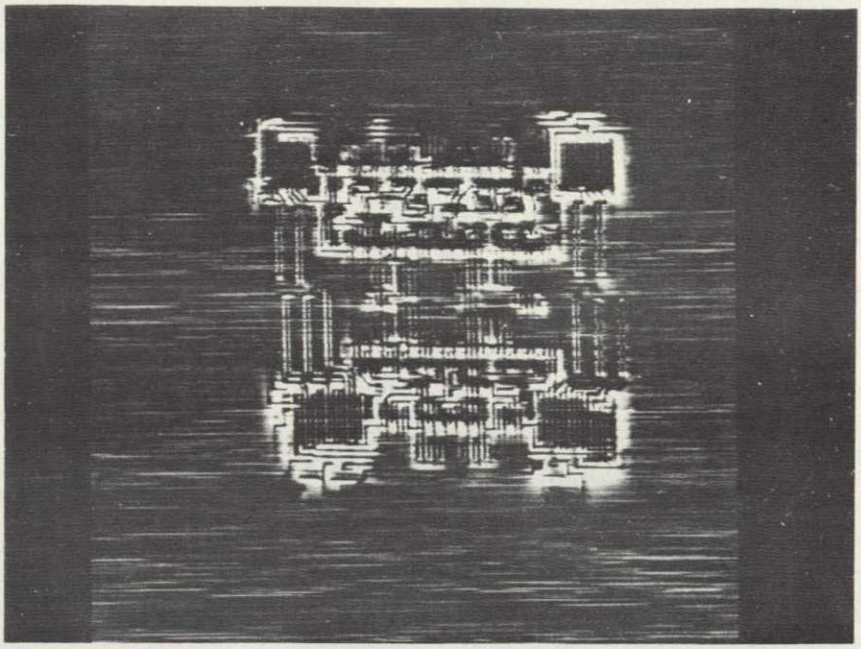

Figure 6.17. Image resulting from the subtraction of Figure 6.11 from Figure 6.12.

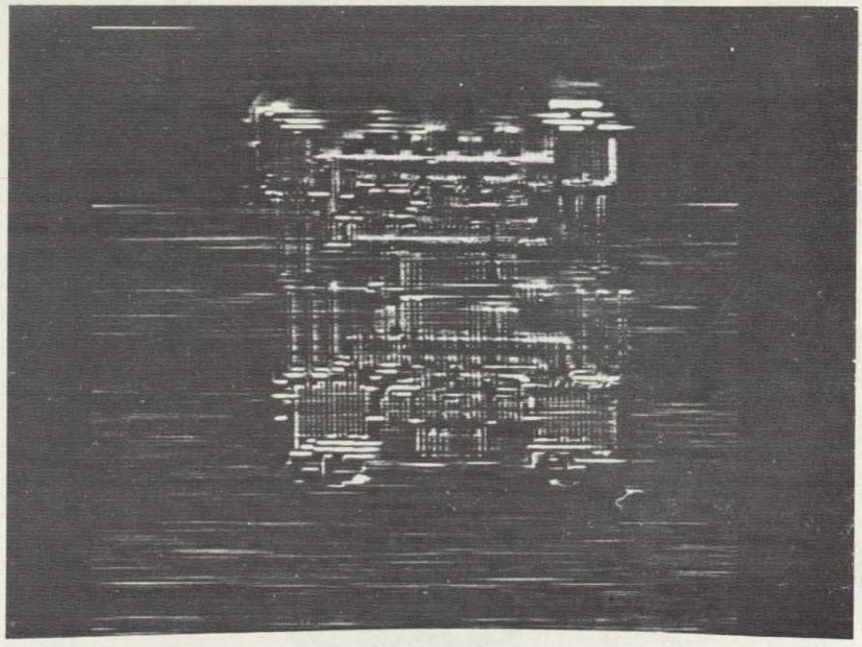

Figure 6.18. Image resulting from the subtraction of Figure 6.12 from Figure 6.11.

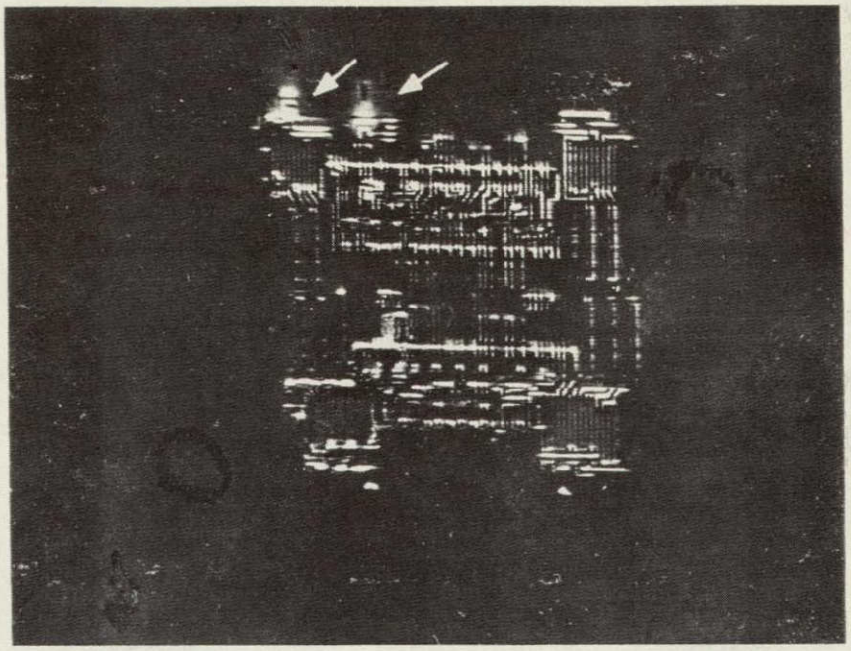

Figure 6.19. Image resulting from the subtraction of Figure 6.12 from Figure 6.13. Arrows indicate some significant results in the area of the device inputs.

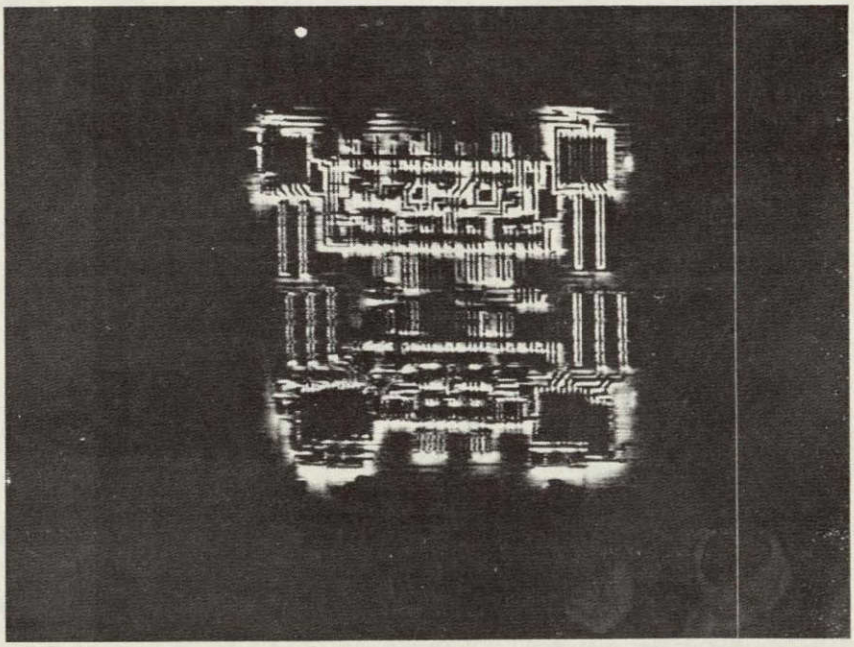

Figure 6.20. Image resulting from the subtraction of Figure 6.13 from Figure 6.12.

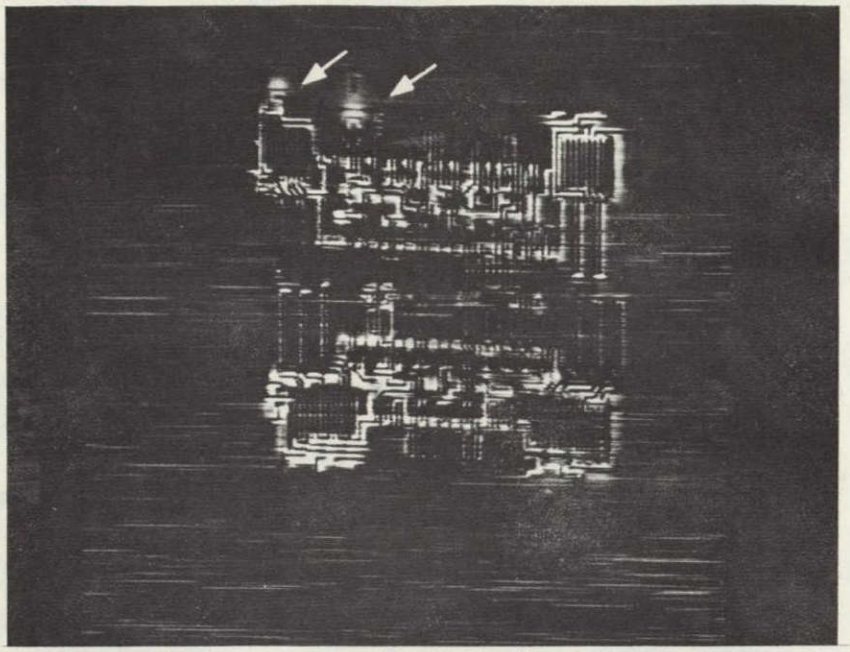

Figure 6.21. Image resulting from the subtraction of Figure 6.11 from Figure 6.13. Arrows indicate some significant results in the area of the device inputs.

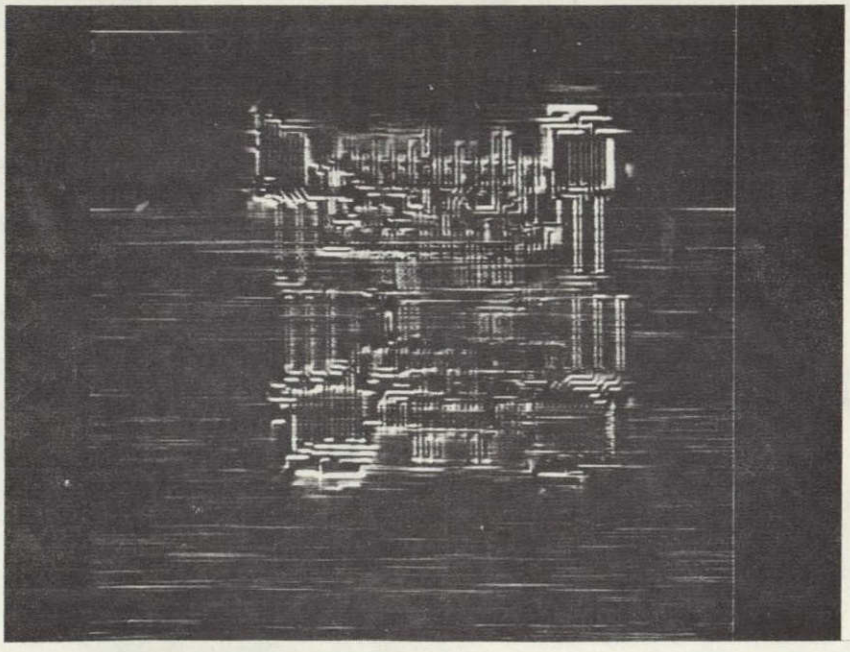

Figure 6.22. Image resulting from the subtraction of Figure 6.13 from Figure 6.11.

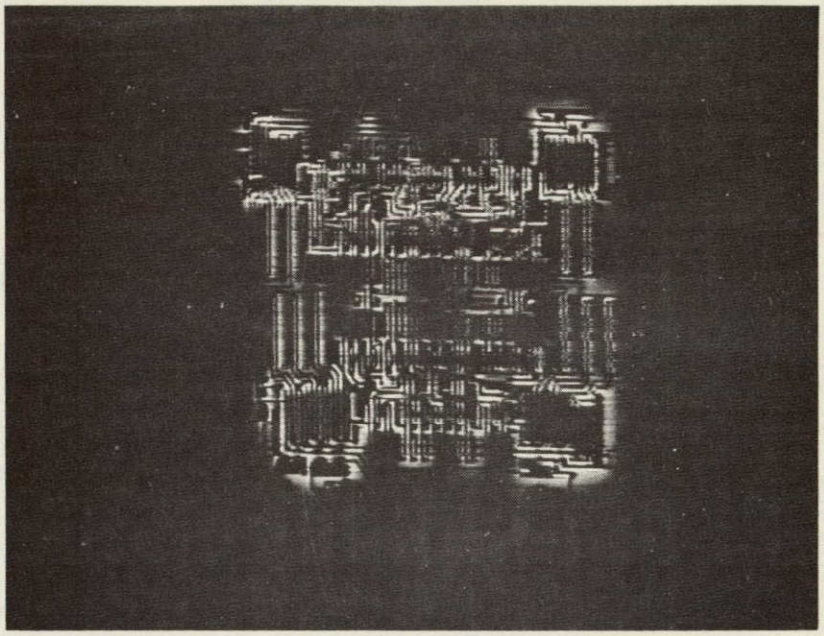

Figure 6.23. Image resulting from the subtraction of Figure 6.16 from Figure 6.12.

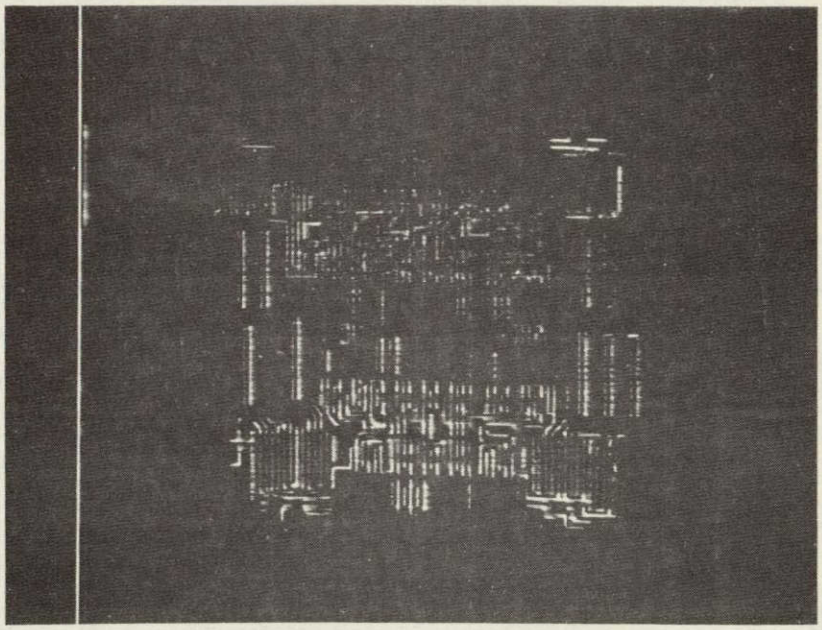

Figure 6.24. Image resulting from the subtraction of Figure 6.12 from Figure 6.16.

As a result of the subtractions between the devices that were chosen to represent "average" devices, the image from device S/N 16 was chosen to represent an average device. The image from device S/N 15 was rejected because of the "noise" in the background. The image from device S/N 17 was rejected because of its unique characteristics near the inputs. The images of devices S/N 16 and S/N 21 were shown to be almost exactly the same, so S/N 16 was chosen.

Subtractions between the image from device S/N 16 (an "average" device) and the image from device S/N 19 (a "significantly different" device) are shown in Figures 6-25 and 6-26. Figure 6-26 which is the result of the subtraction of the image of device S/N 19 from the image of device S/N 16, reveals the most differences. It can be seen that the image from device S/N 16 contained many more diffuse portions of response than did the image from device S/N 19. This can be correlated with the large differences in all of these devices' parameters.

Subtractions between the other image from a "significantly different" device, device S/N 20, and the image from device S/N 16 are shown in Figures 6-27 and 6-28. Again, when the "significantly different" device image was subtracted from the "average" device image many differences were revealed in the amount of diffuse response from the two devices. (This is the same result as obtained in the other "average" device - "significantly different" device subtraction.) However, in this case where the "average" device image was subtracted from the "significantly different" device image, a very unique area of photoresponse was noted on the significantly different device. The differences between these two devices images again correlates well with the large differences in their electrical parameters.

It has been shown that correlations could be formed between differences in devices' electrical parameters and differences in their photoresponse images. In some cases, these correlations were made between subtle differences in the images, but the differences in the electrical parameters were not large. None of the devices' electrical parameters were different enough that they were outside of specification limits.

Correlation 2

The second correlation that was to be attempted, was to try to correlate changes in the devices' electrical parameters following life tests with changes in the photoresponse images. The changes that were to be considered significant were those caused by inherent defects in the devices which caused the devices' electrical parameters to fail or degrade. Unfortunately, the only device parameter that changed was the average power supply current for the devices which dropped considerably between test Runs 1 and 2. This has been attributed to the devices having been opened

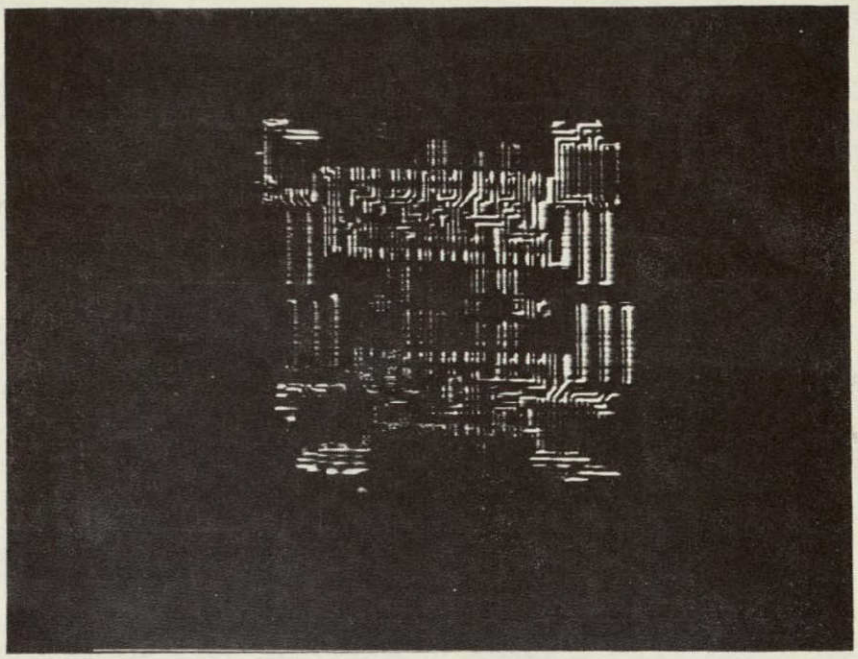

Figure 6.25. Image resulting from the subtraction of Figure 6.12 from Figure 6.14.

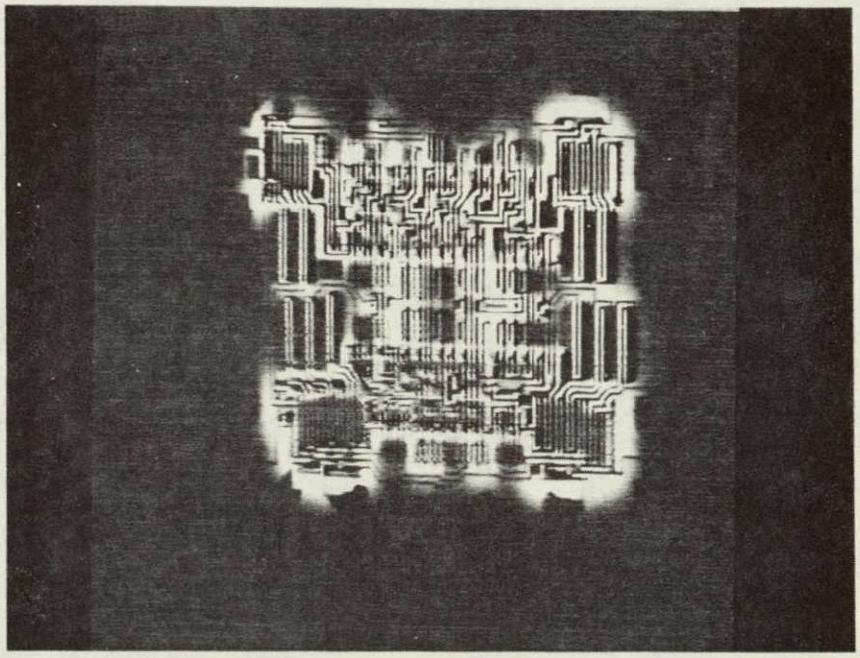

Figure 6.26. Image resulting from the subtraction of Figure 6.14 from Figure 6.12.

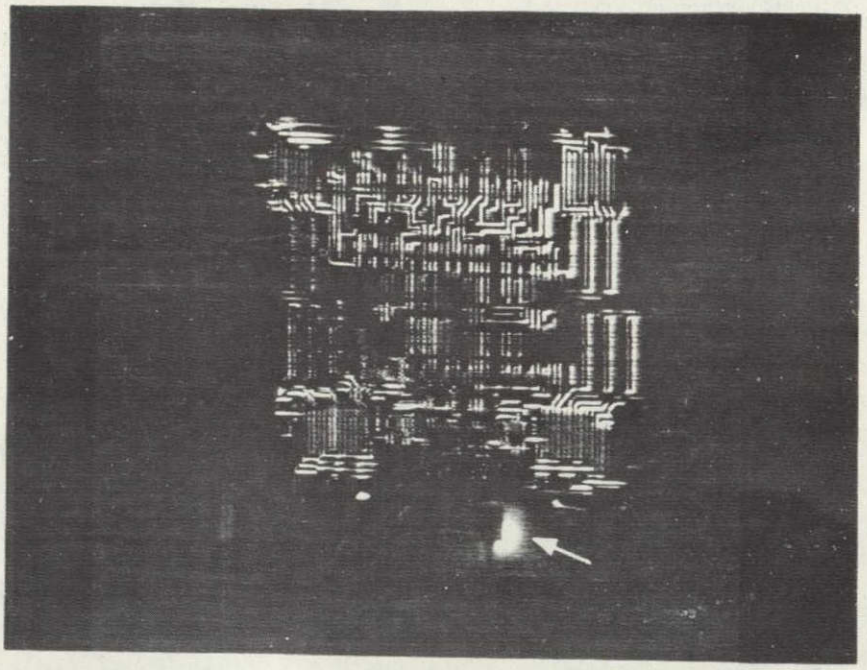

Figure 6.27. Image resulting from the subtraction of Figure 6.12 from Figure 6.15. The arrow indicates a very unique area of difference.

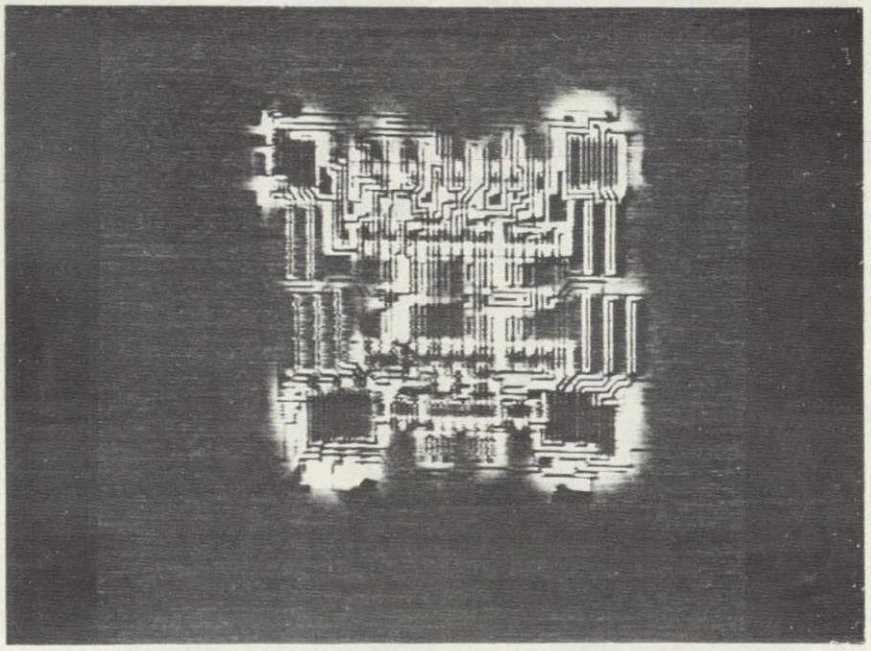

Figure 6.28. Image resulting from the subtraction of Figure 6.15 from Figure 6.12.

to ambient atmosphere for a long period prior to Run 1 and becoming somewhat leaky. Following Run 1 the devices were subjected to a 24 hour life test at 125°C which reduced the power supply currents back to a consistently lower level.

Comparisons of images from devices from Runs 1 and 2 revealed very little difference in their photoresponse images even in the case of devices whose power supply currents decreased appreciably. Apparently, the ambient contamination produced a small effect over many areas, causing an appreciable change in the power supply currents but a small change in the photoresponse images. The only correlation that could be made between changes in device parameters and changes in photoresponse images was that neither changed appreciably, except for the devices' power supply currents. But this change has been attributed to an effect that was not inherent in the devices and is therefore not considered significant.

Correlation 3

It was hoped that a correlation could be made between devices whose parameters degraded or failed and unique elements in their initial photoresponse images. This correlation could not be made since none of the devices' parameters failed or degraded.

7.0 TESTS ON THE CD4034A TEST DEVICE

7.1 CIRCUIT DESCRIPTION

The CD4034A is a fully static eight-stage parallel/serial bilateral bus register. It is a very versatile microcircuit that can be operated in any one of several modes. Depending on inputs to the control terminals, it can operate as a serial-input shift register, a data-recirculating register, or as a parallel-load register. The parallel load can be performed either asynchronously or synchronously (i.e., controlled by the clock input). Each stage has two parallel input/output data lines, which are labelled A and B, whose functions are selected by two control inputs: A/B and A-enable. The A/B control selects either the A or the B data lines as inputs; the non-selected lines then serve as outputs. The A-enable control must be high to enable the A data lines. A low input on the A-enable control and a high input on the A/B control puts the microcircuit in the data-recirculating mode.

The logic diagram for the CD4034A microcircuit is shown in Figure 7-1. The circuit diagram is shown in Figure 7-2 with the individual MOSFET's labelled. The connections of the p-well to the V^- terminal and of the n-substrate to the V^+ terminal are not shown explicitly. Also omitted from this diagram is the p-well/substrate junction. A micrograph of the CD4034A chip is shown in Figure 7-3 with the MOSFET labels on the gate metallizations.

7.2 STATE SUPERPOSITION TEST DEVELOPMENT

The CD4034A is basically a simple type of circuit, an eight-stage register, which is complicated by an elaborate set of control functions. The State Superposition Program developed for this device on the previous program was reviewed and it was decided to use the same one for this program. The operation of the test device and the flow of the State Superposition Program are described below.

Each stage in the register can be either in a high or low state. The data flow into a register stage proceeds along three paths: through one of the two

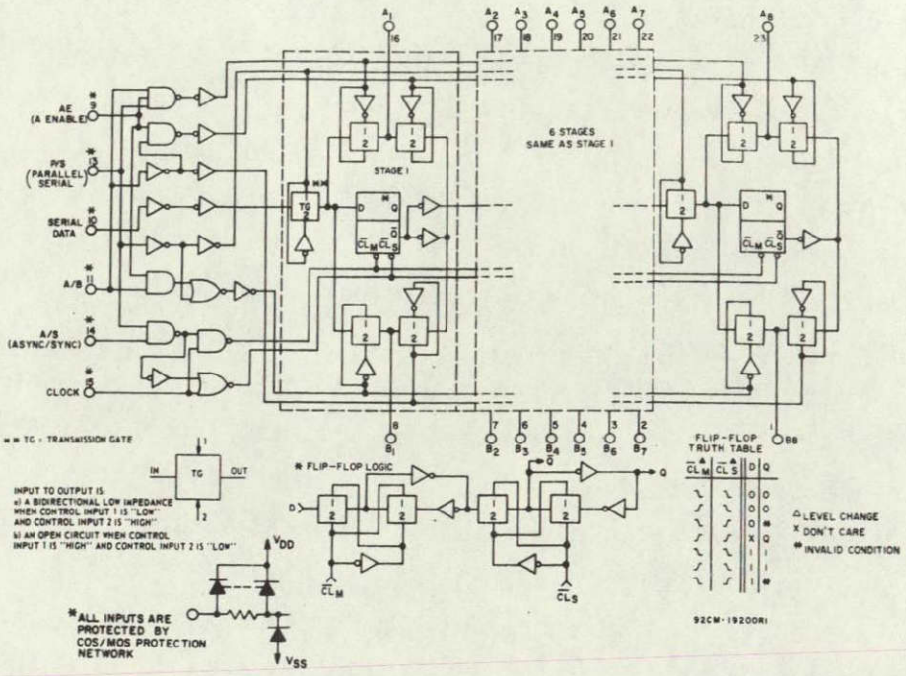

Figure 7-1. Logic diagram of the CD4034A microcircuit.

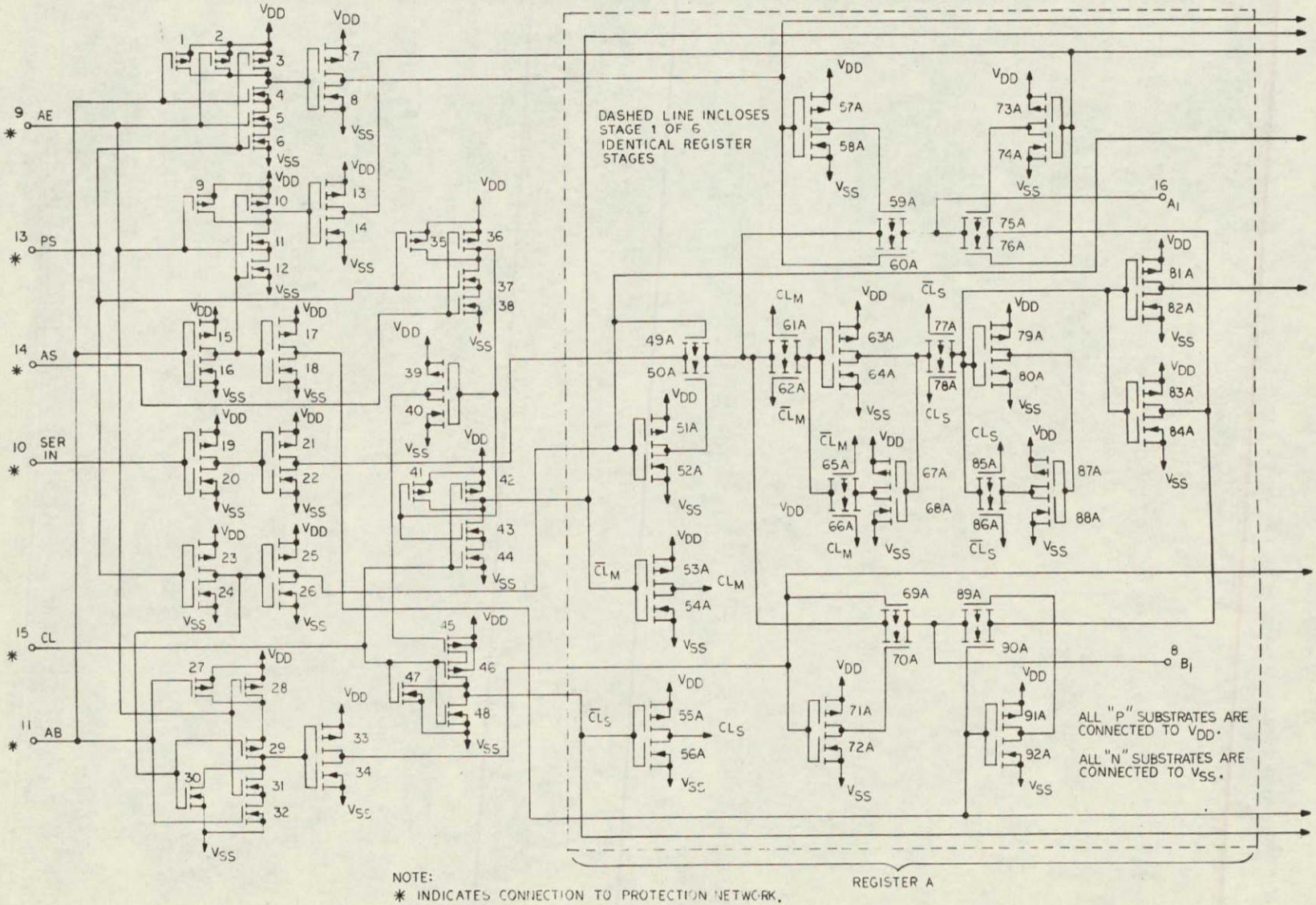

Figure 7-2. Circuit diagram of the CD4034A microcircuit.

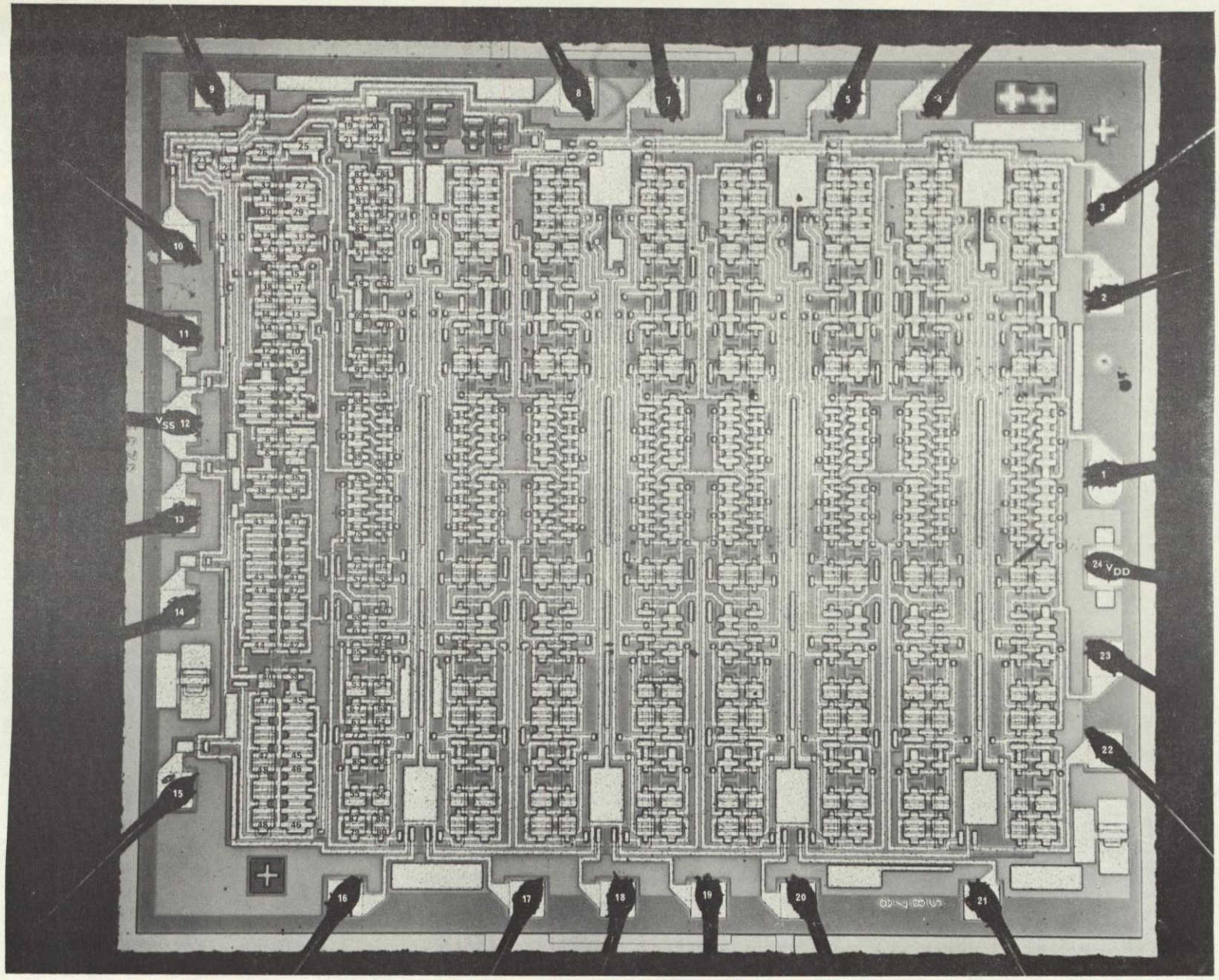

Figure 7-3. Micrograph of the CD4034A microcircuit chip.
(2.80 mm x 2.55 mm)

selectable parallel inputs, or through the serial transfer input from the previous stage. These paths can be exercised by using them to alternately load ones and zeros into each stage. The sequence of operations chosen for the State Superposition Program is as follows:

1. Do an asynchronous parallel load of ones into the even-numbered A inputs and zeros into the odd-numbered A inputs.
2. Do the above operation with complemented input data.
3. Do operations 1 and 2 synchronously (i.e., under control of clock input).
4. Do operations 1, 2 and 3 into the B inputs.
5. Do a serial input load of alternating ones and zeros for eight cycles of the clock.

The input and control signals required to carry out this sequence of operations can be derived from a clock square wave signal divided down by a four-stage counter or frequency divider. A timing diagram of the input and control signals to be applied to the DUT is shown in Figure 7-4.

In addition to generating the signals in the timing diagram, the State Superposition test circuit must perform two additional functions: it must generate a clock signal that lags the input data so that the data signals are properly set up when the clock pulse loads them in (during synchronous loading operations), and it must disconnect the A or B terminals from the data sources when these terminals are selected as outputs. This latter function is implemented with transmission gates that are turned on only when the terminals to which they are connected are selected as inputs. The State Superposition test circuit that performs all these functions is shown in Figure 7-5. The following CMOS microcircuits are used in it:

CD4016 - quad transmission gate
CD4024 - seven stage binary counter (only four stages employed)
CD4011 - quad two input NAND gate
CD4049 - hex inverting buffer/converter
CD4050 - hex non-inverting buffer/converter

7.3 ELECTRICAL TEST DESCRIPTION AND RESULTS

7.3.1 Electrical Test Description

As in the case of the CD4028A test devices, electrical parameters were measured on each of the 25 CD4034A test devices prior to any life tests and

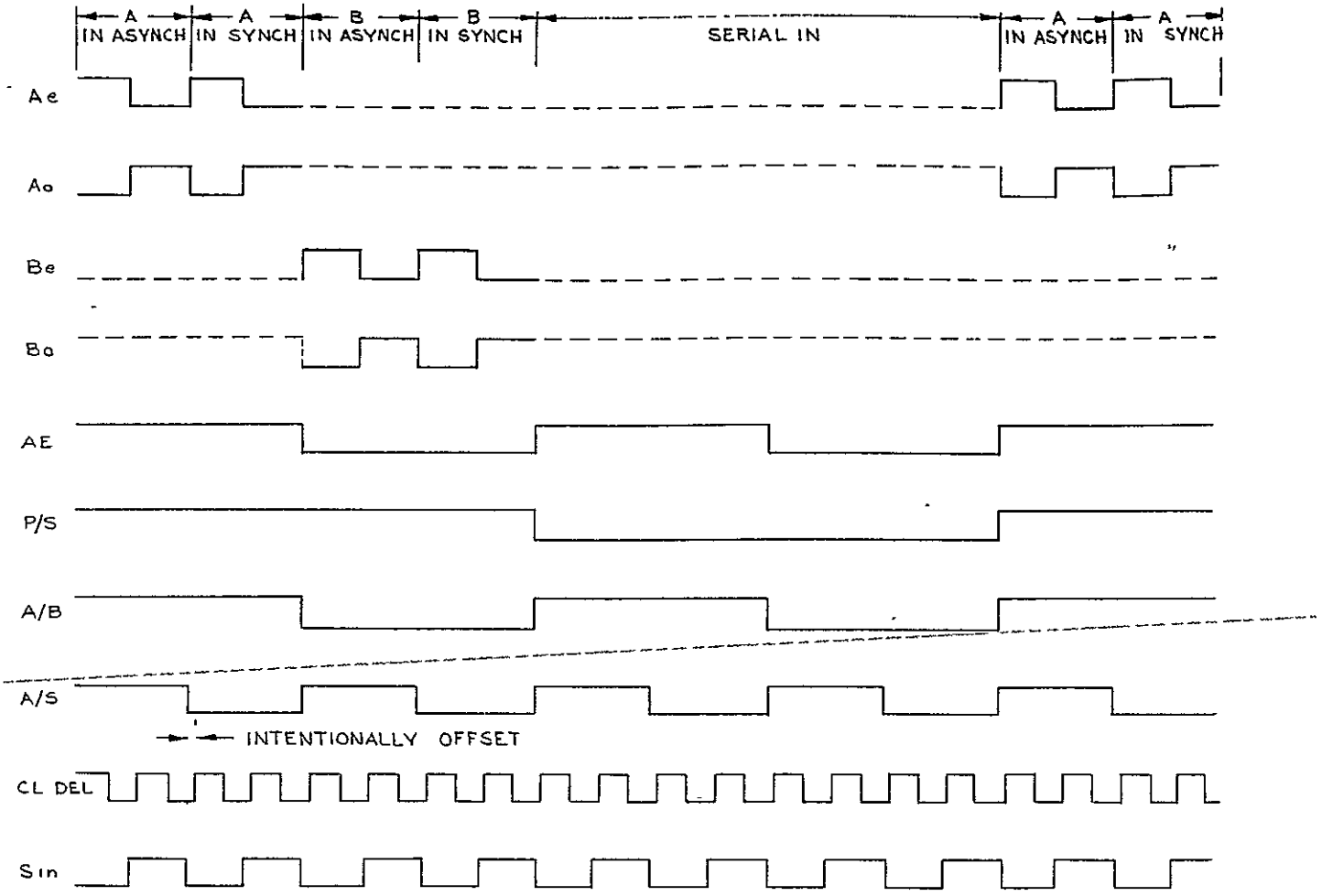

Figure 7-4. Timing diagram of signals applied to the CD4034A by the state superposition test circuit.

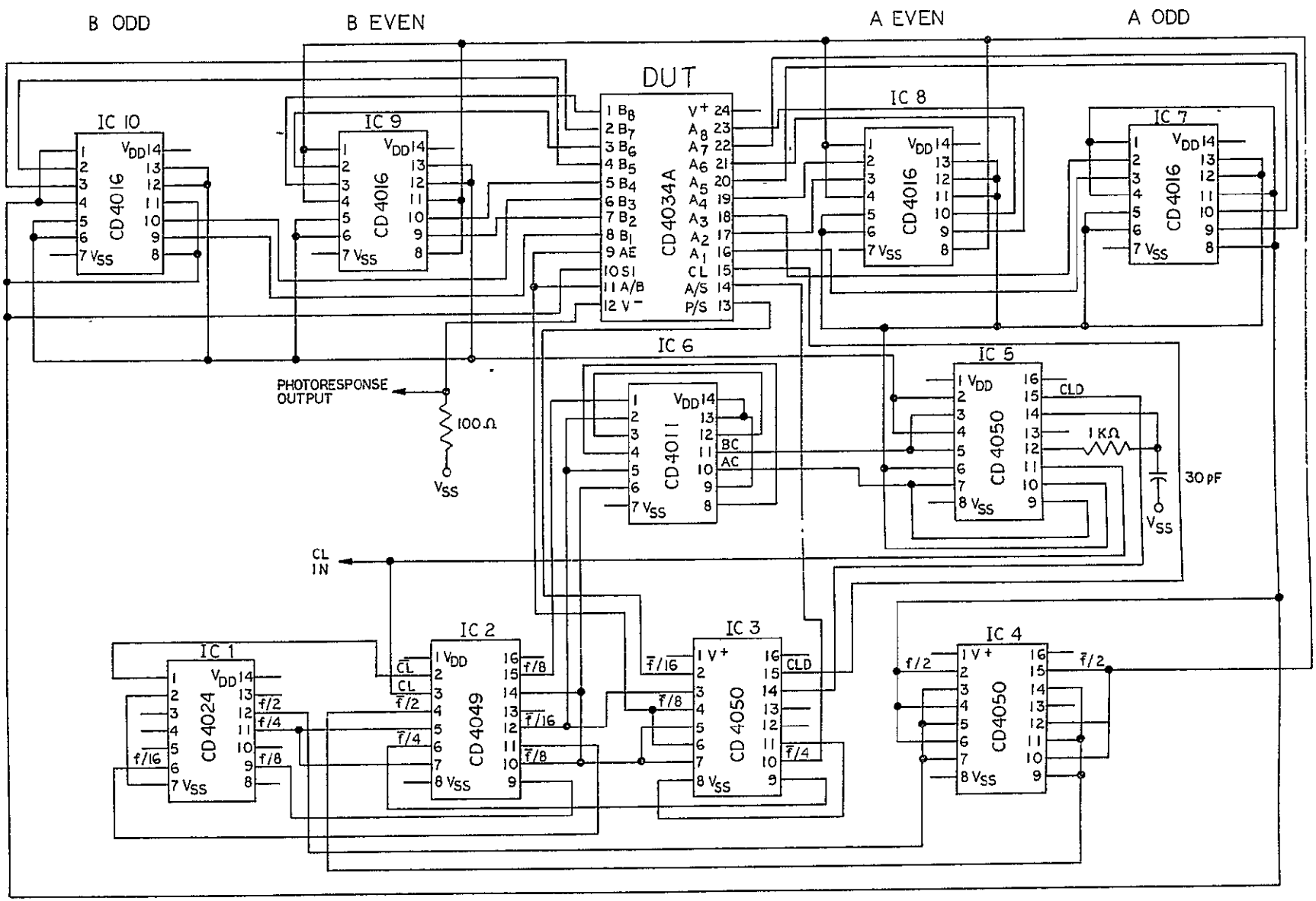

Figure 7-5. Circuit diagram of the state superposition test circuit for the CD4034A microcircuits.

also after each life test interval. The devices were also subjected to a functional test (at both 5.0 and 15.0 volts) and a truth table test (also at both 5.0 and 15.0 volts). All of these tests were performed on the Tektronix S-3260 Automatic Test System.

The parameters that were measured on the devices include the following:

T_{PLH}: propagation time for switching from "low" to "high"

T_{PHL}: propagation time for switching from "high" to "low"

V_{OL}: output voltage when output should be "low"

V_{OH}: output voltage when output should be "high"

I_{IH}: input leakage current with input "high"

I_{IL}: input leakage current with input "low"

V_{ICP}: positive input clamping voltage

V_{ICN}: negative input clamping voltage

I_{SS}: power supply current for various input conditions

V_{TH_N}: N-channel FET threshold voltages

V_{TH_P}: P-channel FET threshold voltages

7.3.2 Electrical Test Results

Tables 7-1a and b are computer printouts of the typical results of one of the electrical tests on CD4034A device S/N 1.

As in the case of the CD4028A test devices, electrical parameters were measured on the CD4034A test devices four times during test Runs 1 through 4. These runs were performed at the same intervals as Runs 1 through 4 for the CD4028A test devices.

Run 1: Measurement of initial electrical parameters

Run 2: Electrical parameters following 24 hours of life test

Run 3: Electrical parameters following an additional 100 hours of life test

Run 4: Electrical parameters following an additional 376 hours of life test

TABLE 7-1a. Computer Printout of Electrical Parameter Test Results for CD4034A Test Device S/N 1.

CD4034A BI-DIRECTIONAL SERIAL-PARALLEL BUS DRIVER SPEC NUMBER: 932626
11:18:35 TEMP: 25 SN: 1

PASSED FUNCTIONAL TEST VDD=5.00 V
PASSED FUNCTIONAL TEST VDD=15.0 V
PASSED TRUTH TABLE TEST VDD=5.00 V
PASSED TRUTH TABLE TEST VDD=15.0 V

PIN	PTN	TPLH2 TPLH1 MAX 1300NS	TPHL2 TPHL1 MAX 1100NS	TPLH4 TPLH3 MAX 1300NS	TPHL4 TPHL3 MAX 1100NS
CLK	A1	460.NS	460.NS	765.NS	475.NS
CLK	A2	460.NS	460.NS	735.NS	470.NS
CLK	A3	465.NS	460.NS	745.NS	490.NS
CLK	A4	460.NS	460.NS	750.NS	480.NS
CLK	A5	460.NS	460.NS	780.NS	490.NS
CLK	A6	460.NS	460.NS	785.NS	495.NS
CLK	A7	460.NS	460.NS	725.NS	465.NS
CLK	A8	460.NS	460.NS	745.NS	470.NS
CLK	B8	775.NS	495.NS	780.NS	490.NS
CLK	B7	740.NS	485.NS	740.NS	480.NS
CLK	B6	785.NS	505.NS	775.NS	500.NS
CLK	B5	725.NS	475.NS	725.NS	465.NS
CLK	B4	750.NS	485.NS	740.NS	480.NS
CLK	B3	805.NS	510.NS	790.NS	500.NS
CLK	B2	760.NS	480.NS	760.NS	475.NS
CLK	B1	745.NS	465.NS	720.NS	460.NS

PIN	VOL1 MAX 0.5V	VOL2 MAX 1.25V	VOH1 MIN 4.5V	VOH2 MIN 11.25V
B8	148.MV	350.UV	4.81 V	12.5 V
B7	145.MV	450.UV	4.82 V	12.5 V
B6	142.MV	-250.UV	4.81 V	12.5 V
B5	138.MV	450.UV	4.82 V	12.5 V
B4	141.MV	-150.UV	4.82 V	12.5 V
B3	142.MV	850.UV	4.82 V	12.5 V
B2	140.MV	-350.UV	4.82 V	12.5 V
B1	138.MV	900.UV	4.82 V	12.5 V
A1	140.MV	-100.UV	4.82 V	12.5 V
A2	140.MV	600.UV	4.82 V	12.5 V
A3	138.MV	-300.UV	4.82 V	12.5 V
A4	136.MV	350.UV	4.82 V	12.5 V
A5	136.MV	300.UV	4.82 V	12.5 V
A6	138.MV	-300.UV	4.82 V	12.5 V
A7	137.MV	250.UV	4.82 V	12.5 V
A8	135.MV	-50.0UV	4.81 V	12.5 V

TABLE 7-1b. Computer Printout of Electrical Parameter Test Results for CD4034A Test Device S/N 1.

PIN	IIH MAX 1NA	IIL MAX -1NA	VICP MAX 1.5V	VICN MAX -6V
CLK	-606.PA	-9.25NA	830.MV	-2.34 V
AE	100.PA	-1.35NA	825.MV	-2.39 V
PS	900.PA	217.PA	830.MV	-2.38 V
A8	-50.0PA	-66.7PA	830.MV	-2.40 V
AS	-650.PA	-213.PA	830.MV	-2.34 V
SER	1.10NA	-373.PA	840.MV	-2.40 V
A1	550.PA	-177.PA		
A2	-650.PA	-66.7PA		
A3	< 1PA	-193.PA		
A4	1.25NA	-233.PA		
A5	-150.PA	133.PA		
A6	-1.15NA	-217.PA		
A7	-450.PA	-157.PA		
A8	950.PA	-73.3PA		
B8	-300.PA	90.0PA		
B7	-850.PA	-100.PA		
B6	900.PA	-173.PA		
B5	450.PA	-26.7PA		
B4	-900.PA	36.7PA		
B3	150.PA	-26.0PA		
B2	950.PA	23.3PA		
B1	-350.PA	-56.7PA		

MAXIMUM ISS: 1.0
ISS: -74.0NA
ISS: -110.NA
ISS: -79.1NA
ISS: -55.5NA
ISS: -68.5NA
ISS: -56.5NA
ISS: -59.5PA
ISS: -94.5NA

VTH(34)	-1.85 V
VTH(38)	-1.85 V
VTH(32)	-1.7 V
VTH(10)	-1.7 V
VTH(11)	-1.59 V
VTH(33)	3.15 V
VTH(36)	3.14 V
VTH(39)	3.11 V
VTH(35)	3.09 V
VTH(9)	3.11 V

Summaries of the electrical test results are presented in the following tables for the parameters listed:

Table 7.2: Maximum and minimum values of all T_{PHL} and T_{PLH} times for each device at each run

Table 7.3: Maximum V_{OL} for each device at each run

Table 7.4: Peak I_{SS} for each device at each run

Table 7.5: Average of the four V_{TH_N} values for each device at each run

Table 7.6: Average of the four V_{TH_P} values for each device at each run

Parameter V_{OH1} was not tabulated. V_{OH1} varied from 4.82 V to 4.89V for all devices during all runs except for device S/N 7 which was a functional failure. The values of V_{OH1} for device S/N 7 are shown below.

Run 1	Run 2	Run 3	Run 4
110MV	90MV	85MV	80MV

These values are all far below the minimum specified value of 4.5V for V_{OH1}.

Parameters V_{OL2} and V_{OH2} were not tabulated or correlated. These parameters were measured with V_{DD} = 15.0V. Since the photoresponse images were recorded with V_{DD} = 5.0V, there would be little or no correlation between these parameters and the photoresponse images.

Parameters I_{IH} and I_{IL} were not tabulated since the values varied considerably from run to run. This was due to the sensitivity of the test with typical values for these parameters being on the order of hundreds of picoamperes or less. All of the devices' I_{IH} and I_{IL} parameters were less than 45nA which is the limit specified in military specification MIL-M-38510/57. The limit that was specified on the test program and on the printouts was incorrectly specified as 1.0 nA.

Parameters V_{IC_P} and V_{IC_N} were not tabulated for the devices since there was not much of a spread in these values. All values of V_{IC_P} and V_{IC_N} were well within specified limits. V_{IC_N} values ranged from 2.3V to 2.5V and V_{IC_P} values ranged from 815MV to 850MV. (This parameter is basically a test of the input protection circuitry on each input. Unless these parameters are outside of specification limits, slight differences in their values from device to device will cause no difference in the operation of the different devices. Also, slight differences in these values would be extremely difficult to correlate with changes in photoresponse images.)

TABLE 7.2.CD4034: PROPAGATION DELAY TIMES

DEVICE S/N	RUN 1		RUN 2		RUN 3		RUN 4	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
1	460	805	455	765	500	795	500	835
2	520	675	515	630	565	670	570	700
3	470	585	465	560	510	590	515	610
4	430	505	425	525	475	525	475	530
5	440	535	435	525	480	550	480	560
6	445	520	445	515	485	535	485	545
7	630	840	625	845	670	880	675	880
8	460	585	455	560	495	590	505	610
9	435	500	430	495	475	520	475	520
10	465	525	455	510	500	545	505	555
11	430	500	425	490	465	520	470	525
12	430	500	425	490	470	515	475	520
13	445	525	440	515	480	535	485	545
14	445	495	440	490	480	510	485	515
15	435	540	430	525	470	540	475	545
16	435	510	430	495	470	515	475	520
17	435	495	425	485	470	515	475	520
18	435	505	430	495	475	530	475	530
19	485	550	480	545	525	555	525	575
20	460	565	455	555	500	585	500	590
21	445	535	440	520	485	555	485	560
22	485	635	475	610	520	635	525	665
23	475	575	475	575	515	590	515	600
24	450	535	445	525	485	555	490	565
25	495	600	490	595	535	610	540	620
Average	462	566	456	554	500	578	503	590
Standard Deviation	41	88	41	84	42	87	43	92

ALL VALUES ARE NANOSECONDS

C-2

TABLE 7.3.CD4034: MAXIMUM V_{OL} (OUTPUT "LOW" VOLTAGE)

DEVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	148	146	149	146
2	176	174	174	174
3	166	165	164	164
4	144	143	142	142
5	141	140	139	139
6	153	153	151	152
7	(4.97V)(A)	(4.97V)(A)	(5.00V)(A)	(5.00V)(A)
8	165	163	162	162
9	147	145	144	144
10	159	156	155	155
11	143	142	141	140
12	144	143	142	142
13	147	146	146	146
14	153	152	150	150
15	148	146	145	145
16	153	151	150	150
17	144	141	141	141
18	141	139	139	139
19	175	174	172	173
20	146	145	144	145
21	149	147	147	146
22	168	165	165	164
23	152	154	152	152
24	146	145	144	144
25	165	164	163	164
Average	153(B)	152(B)	151(B)	151(B)
Standard Deviation	10(B)	10(B)	10(B)	10(B)

ALL VALUES ARE MILLIVOLTS UNLESS OTHERWISE NOTED

(A) DEVICE S/N 7 WAS A FAILED DEVICE

(B) PARAMETERS FROM DEVICE 7 NOT INCLUDED IN CALCULATIONS

TABLE 7.4.CD4034: PEAK POWER SUPPLY CURRENTS (I_{SS})

DEVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	116	98	110	85
2	59	59	47	47
3	59	58	59	51
4	60	58	60	40
5	63	58	50	50
6	62	54	53	39
7	61	60	45	37
8	62	57	50	43
9	63	56	51	50
10	63	57	50	44
11	64	61	45	42
12	64	59	43	53
13	64	61	49	55
14	64	62	47	51
15	65	58	50	53
16	63	57	53	46
17	63	58	54	46
18	58	56	45	37
19	58	68	53	47
20	53	55	49	44
21	54	56	57	45
22	61	57	54	38
23	57	57	61	43
24	56	56	56	52
25	58	58	60	52
Average	62.8	59.8	54.0	47.6
Standard Deviation	11.3	8.3	12.5	9.3

ALL VALUES ARE NANOAMPERES

TABLE 7.5.CD4034: AVERAGE N-CHANNEL FET THRESHOLD VOLTAGES ($\overline{V_{TH_N}}$)

DEVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	-1.66	-1.61	-1.62	-1.64
2	-2.20	-2.17	-2.17	-2.19
3	-2.15	-2.12	-2.12	-2.14
4	-2.30	-2.29	-2.32	-2.33
5	-2.31	-2.30	-2.31	-2.34
6	-2.38	-2.34	-2.37	-2.40
7	-3.00	-3.01	-2.97	-3.02
8	-2.13	-2.10	-2.10	-2.12
9	-2.31	-2.28	-2.33	-2.34
10	-2.35	-2.33	-2.37	-2.37
11	-2.30	-2.28	-2.32	-2.32
12	-2.30	-2.31	-2.33	-2.34
13	-2.38	-2.35	-2.35	-2.39
14	-2.32	-2.30	-2.34	-2.34
15	-2.32	-2.30	-2.35	-2.35
16	-2.35	-2.33	-2.37	-2.38
17	-2.29	-2.27	-2.31	-2.32
18	-2.29	-2.27	-2.31	-2.31
19	-2.46	-2.43	-2.44	-2.48
20	-2.34	-2.29	-2.32	-2.36
21	-2.32	-2.29	-2.34	-2.35
22	-2.15	-2.12	-2.14	-2.16
23	-2.33	-2.31	-2.31	-2.35
24	-2.31	-2.28	-2.33	-2.34
25	-2.36	-2.33	-2.34	-2.36
Average	-2.30	-2.28	-2.30	-2.32
Standard Deviation	0.20	0.21	0.21	0.21

ALL VALUES ARE VOLTS

TABLE 7.6.CD4034: AVERAGE P-CHANNEL FET THRESHOLD VOLTAGES ($\overline{V_{TH_P}}$)

EVICE S/N	RUN 1	RUN 2	RUN 3	RUN 4
1	3.12	3.12	3.12	3.12
2	2.51	2.50	2.51	2.51
3	2.41	2.41	2.41	2.41
4	2.25	2.24	2.24	2.25
5	2.28	2.28	2.28	2.28
6	2.17	2.17	2.17	2.17
7	2.28	2.29	2.29	2.29
8	2.41	2.41	2.41	2.42
9	2.20	2.20	2.20	2.20
10	2.21	2.21	2.22	2.21
11	2.23	2.23	2.23	2.23
12	2.20	2.20	2.20	2.20
13	2.18	2.18	2.18	2.18
14	2.17	2.17	2.17	2.17
15	2.26	2.26	2.26	2.26
16	2.21	2.21	2.21	2.21
17	2.21	2.21	2.21	2.21
18	2.25	2.25	2.25	2.25
19	2.17	2.17	2.17	2.17
20	2.27	2.27	2.27	2.27
21	2.22	2.22	2.22	2.22
22	2.48	2.47	2.47	2.48
23	2.37	2.37	2.37	2.37
24	2.26	2.26	2.26	2.26
25	2.37	2.37	2.37	2.37
Average	2.31	2.31	2.31	2.31
Standard Deviation	0.19	0.19	0.19	0.19

ALL VALUES ARE VOLTS

The electrical tests can be summarized by stating that there was very little change in most of the significant electrical parameters for the CD4034A test devices. The values for the peak power supply currents for the devices showed the most change. The average of the peak power supply currents decreased throughout the life-testing from a value of 62.8 nanoamperes at the initial test prior to life-testing, down to 47.6 nanoamperes following 500 hours of life testing. Figure 7-6 is a graph of the average of the peak power supply current of the test devices plotted as a function of accumulated life-test time. The only parameters that were outside of specified limits were those of device S/N 7 which was included in all testing even though it had failed initial electrical tests.

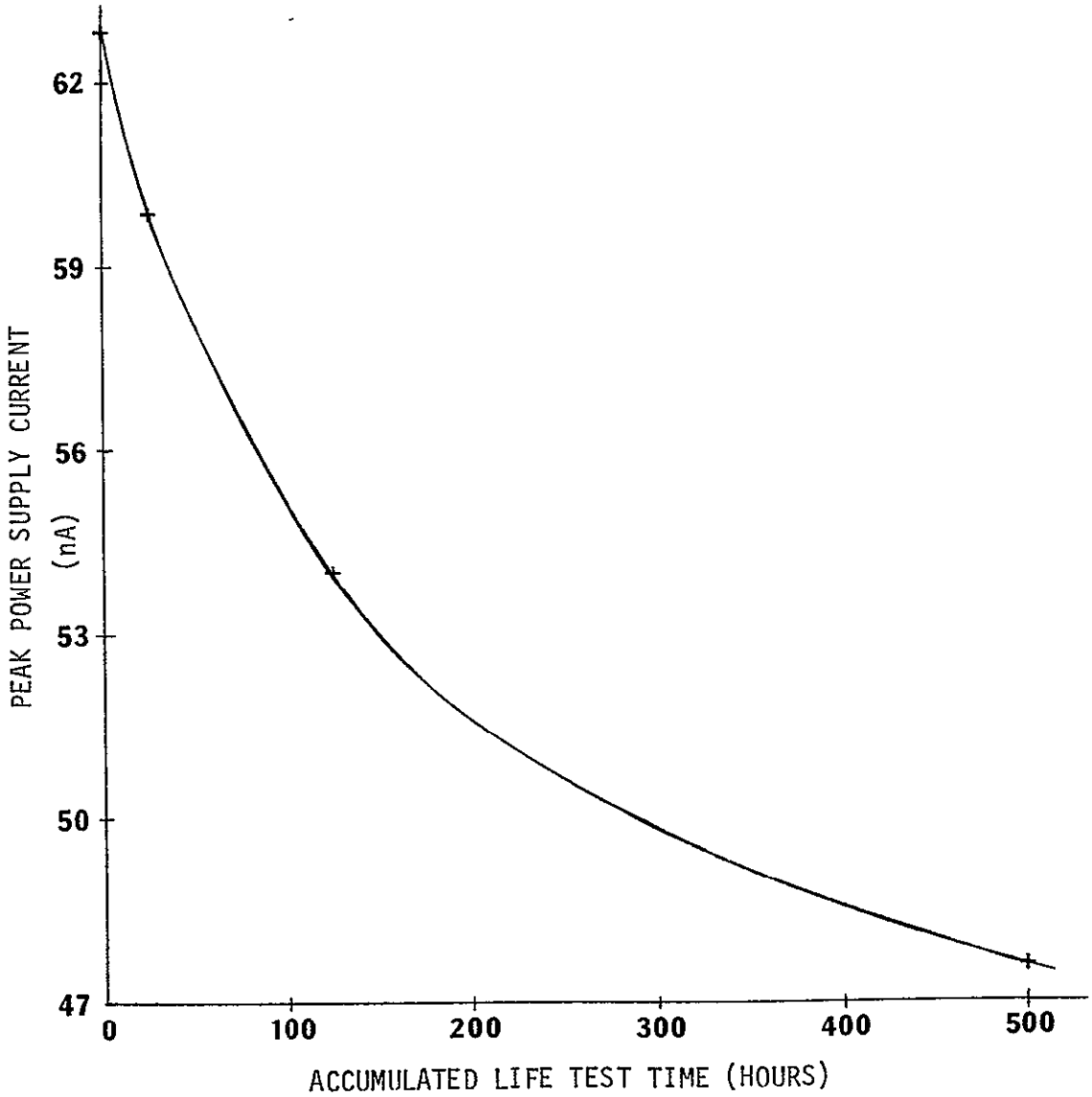

FIGURE 7.6 GRAPH OF PEAK POWER SUPPLY CURRENT AS A FUNCTION OF ACCUMULATED LIFE TEST TIME.

7.4 LIFE-TESTS

The CD4034A test devices were subjected to three life-test intervals. The initial life test interval was 24 hours long. Review of the devices' electrical parameters following this interval, revealed no significant change from the initial parameters. The next life test period was chosen to be 100 hours long in order to try to obtain some significant changes in electrical parameters. Again, the electrical parameters showed no significant changes after this life test interval. The third life test which was 376 hours long, resulted in a total of 500 hours of life testing on the test devices. This was the maximum amount of life testing required for this program and also the maximum amount of time available within the limits of the program schedule. Unfortunately, as in the case of the CD4028A test devices, there was still no significant change in the electrical parameters of the CD4034A test devices.

The test devices were life-tested using the circuit shown in Figure 7-7. The devices were heated to 125^{o}C during the life tests in ovens that were purged with dry nitrogen gas.

7.5 PHOTORESPONSE IMAGE RECORDING

Photoresponse images of all twenty-five CD4034A test devices were recorded on magnetic tape. These images were recorded prior to any life tests (Run 1), following 24 hours of life tests (Run 2), following an additional 100 hours of life test (Run 3) and following an additional 376 hours of life test (Run 4). At each run, four tapes of serially recorded images were recorded. Devices S/N 1 through S/N 7 were recorded on one magnetic tape, devices S/N 8 through S/N 14 were recorded on a second magnetic tape, devices S/N 15 through S/N 21 were recorded on a third tape and devices S/N 22 through S/N 25 were recorded on a fourth tape.

During the optical scanner examination of each device, the device was run using a power supply voltage of 5V. The test device was switched using the State Superposition test circuit described previously. The test circuit was run at a frequency of 3.5 MHz.

One of the improvements of this program over the last one, was the addition of a 2.5X microscope lens to the optical scanner setup. Using this lens it was possible to obtain a single photoresponse image that covered the entire CD4034A chip. In the previous program, it was necessary to cover the CD4034A chip with two overlapping photoresponse images in order to image all the elements.

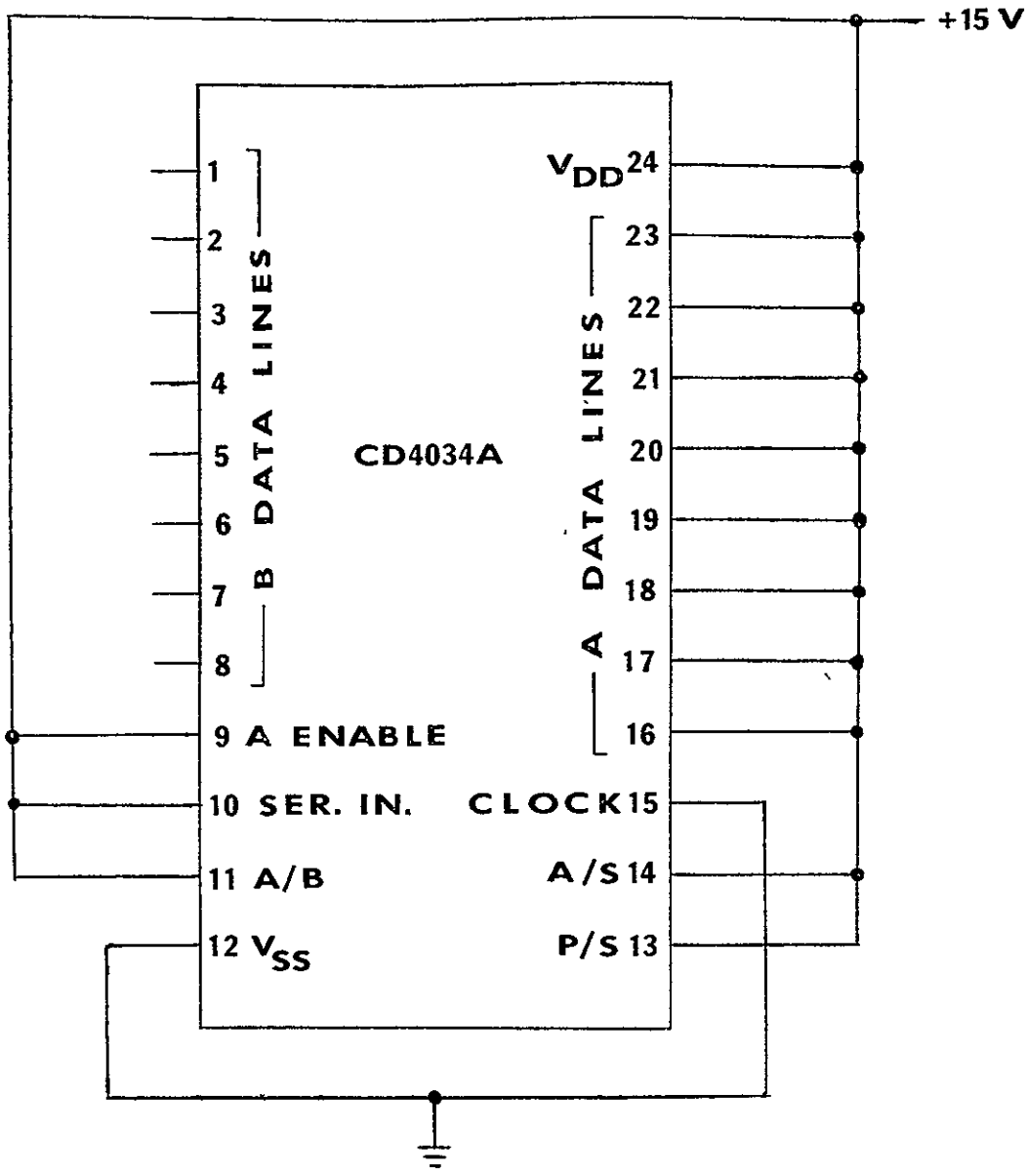

Figure 7-7. Life-test circuit for CD4034A. (Connections to all terminals except 12 and 24 are made through 47KΩ resistors.)

7.6 CORRELATION OF PHOTORESPONSE IMAGES WITH ELECTRICAL TEST RESULTS

As in the case of the CD4028A test devices, due to time and financial limitations not all of the photoresponse images from all of the CD4034A test devices could be subtracted from each other in order to try to find differences that could be correlated with electrical test results. The electrical test results were reviewed in order to attempt to pick some meaningful photoresponse images which would be analyzed.

Correlation 1

The first correlation that was to be attempted was to correlate differences in devices' electrical parameters with differences in photoresponse images. The electrical test data was reviewed in order to find devices whose electrical parameters were "significantly different" from the others. As in the case of the CD4028A test devices, if a device's electrical parameter varied from the average value for that parameter by more than two standard deviations, it was classified as "significantly different". Device S/N 7 was automatically included in the class of "significantly different" devices since it had failed initial electrical tests. As a result of this definition, two devices (other than device S/N 7) were shown to be "mavericks". These two devices were S/N 1 and S/N 2. Table 7.7 lists the various tabulated parameters and shows which devices had parameters significantly different from the average or outside of specification limits. Except for devices S/N 1, S/N 2 and S/N 7 all other devices' parameters were less than two standard deviations from the average and within specification limits.

TABLE 7.7

Summary of Devices with "Significantly Different" or Failed Parameters

PARAMETER	S/N 1	S/N 2	S/N 7
T_{pd} (max)	D	N	D
T_{pd} (min)	N	N	D
V_{OL}	N	D	F
I_{SS}	D	N	N
$\overline{V}_{TH_N}$	D	N	D
$\overline{V}_{TH_P}$	D	N	N

"D" indicates the device's parameter was more than 2 standard deviations from the average.

"F" indicates the device's parameter was outside of specification limits

"N" indicates the device's parameter was less than 2 standard deviations from the average.

Devices S/N 1, S/N 2 and S/N 7 were chosen to represent devices whose electrical parameters different from the average. Device S/N 7 was, of course, considerably different from the average since several of its electrial parameters failed to meet specification requirements.

In order to perform comparisons some devices were chosen to represent "average" devices. As noted previously, the images from devices S/N 1 through S/N 7 were recorded on one magnetic tape. For ease of data handling and a reduced number of tapes that would have to be processed, the parameters from devices S/N 3, S/N 4, and S/N 5 and S/N 6 were reviewed to determine if they represented fairly average samples. Two of the electrical parameters of device S/N 3 were about one standard deviation away from the average, so this device was rejected as an "average: device. Devices S/N 4, S/N 5 and S/N 6 were to be used as examples of "average" devices.

When the images for the devices that were chosen to represent "average" devices were displayed, it was discovered that the image for device S/N 4 was not usable. Unfortunately, it could not be recorded again since the device had already been submitted for its initial life-test. Figures 7.8 through 7.12 are the photoresponse images of devices S/N 1, S/N 2, S/N 5, S/N 6 and S/N 7 recorded at run 1. (These figures are photographs created at the image processing facility.)

The first subtractions that were performed were between images of the two "average" devices to determine if there were differences between devices with similar parameters. Figures 7.13 and 7.14 show the results of the subtractions between the images of devices S/N 5 and S/N 6. It can be seen that there are no differences except for some slight misalignment between the two devices. As a result, either device could be used to represent an "average" device.

Subtractions between images from an "average" device, S/N 5, and a "significantly different" device, S/N 1, are shown in Figures 7.15 and 7.16. It can be seen that there were major differences between the images of these devices. The large bright areas in these figures are concluded to be correlated with the large differences in the maximum propagation delay time parameters (T_{PD}) for these devices. The previous program revealed that CMOS devices exhibited anomalous areas in their photoresponses as their maximum operating frequencies were approached. Apparently, the large T_{PD} for device S/N 1 caused it to exhibit these anaomalous areas in its photoresponse image. Subtractions between this device's image and the image for the faster device S/N 5, clearly revealed

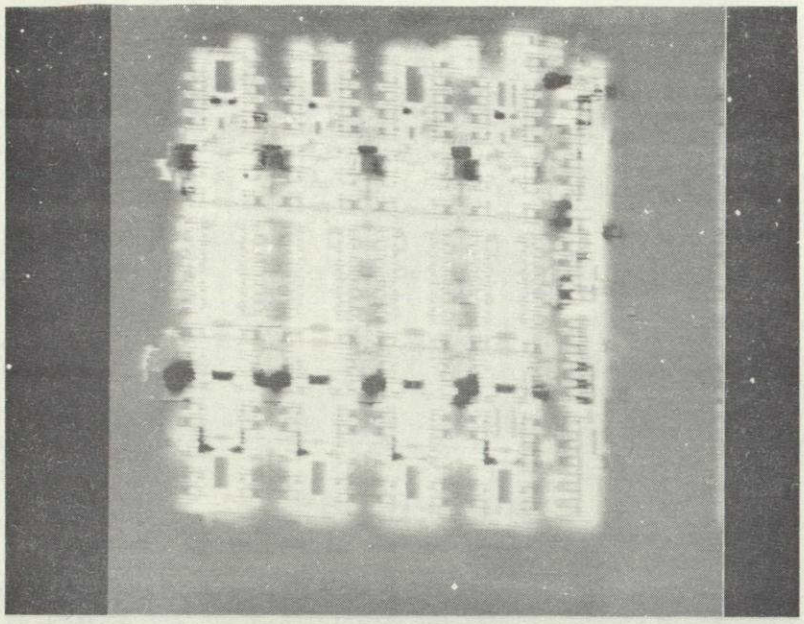

Figure 7.8. Photoresponse image from device S/N 1, a "significantly different" device.

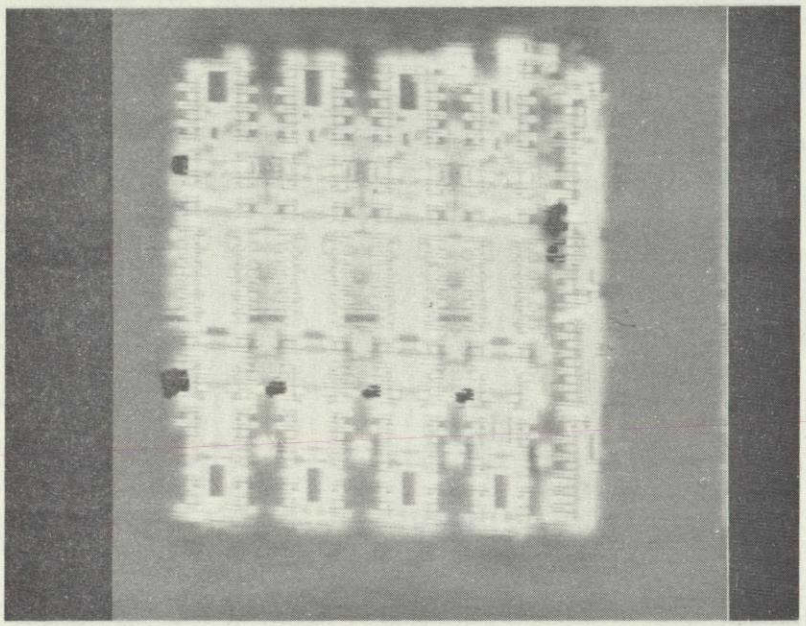

Figure 7.9. Photoresponse image from device S/N 2, a "significantly different" device.

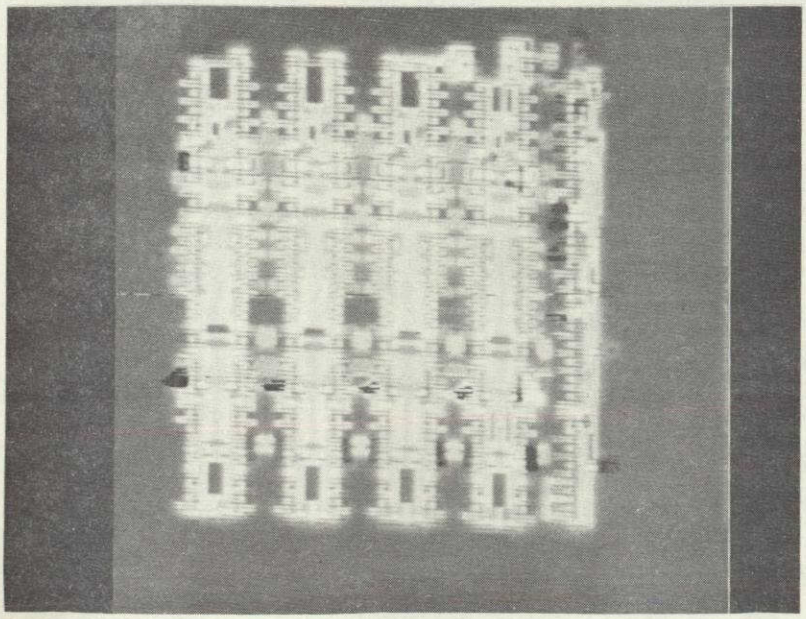

Figure 7.10. Photoresponse image from device S/N 5, an "average" device.

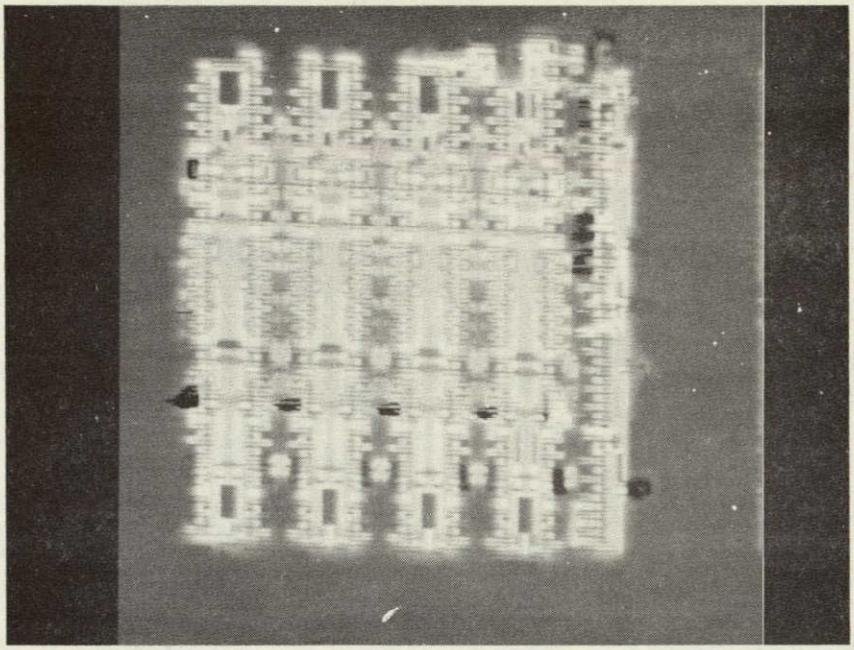

Figure 7.11. Photoresponse image from device S/N 6, an "average" device.

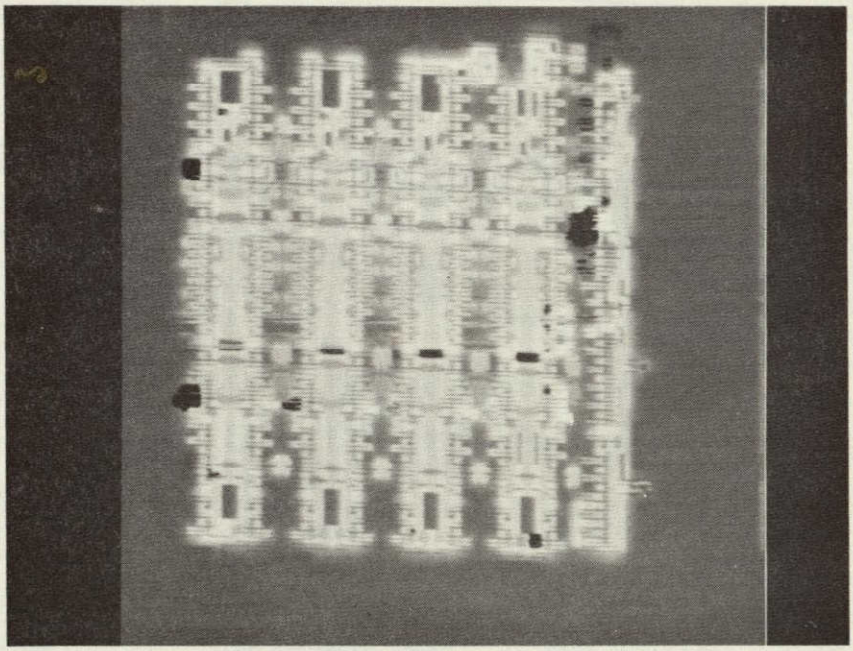

Figure 7.12. Photoresponse image from device S/N 7, a failed device.

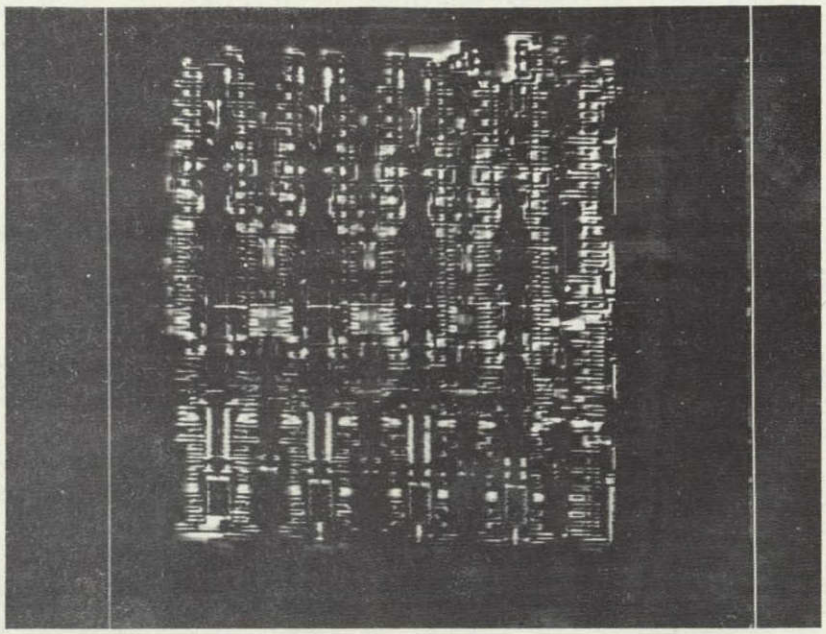

Figure 7.13. Image resulting from the subtraction of Figure 7.10 from Figure 7.11.

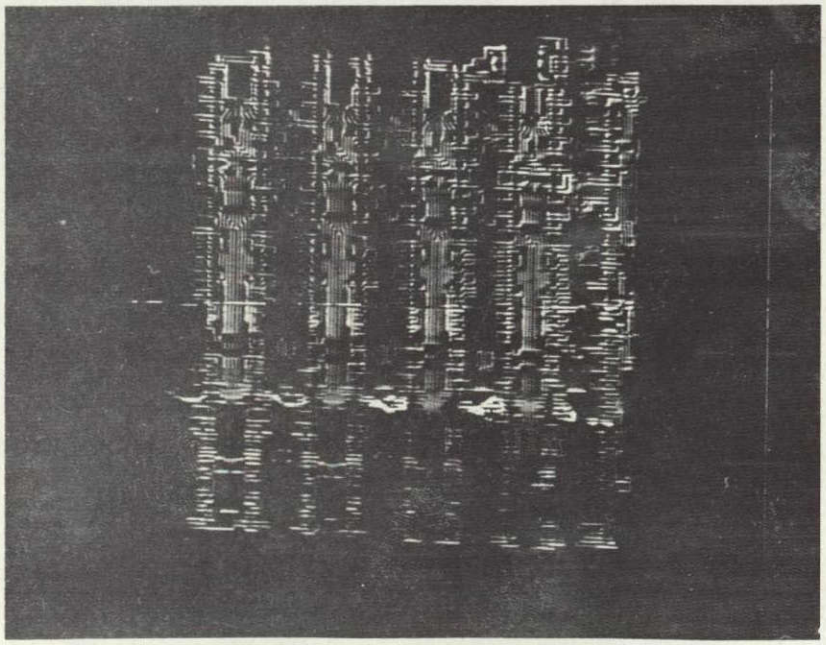

Figure 7.14. Image resulting from the subtraction of Figure 7.11 from Figure 7.10.

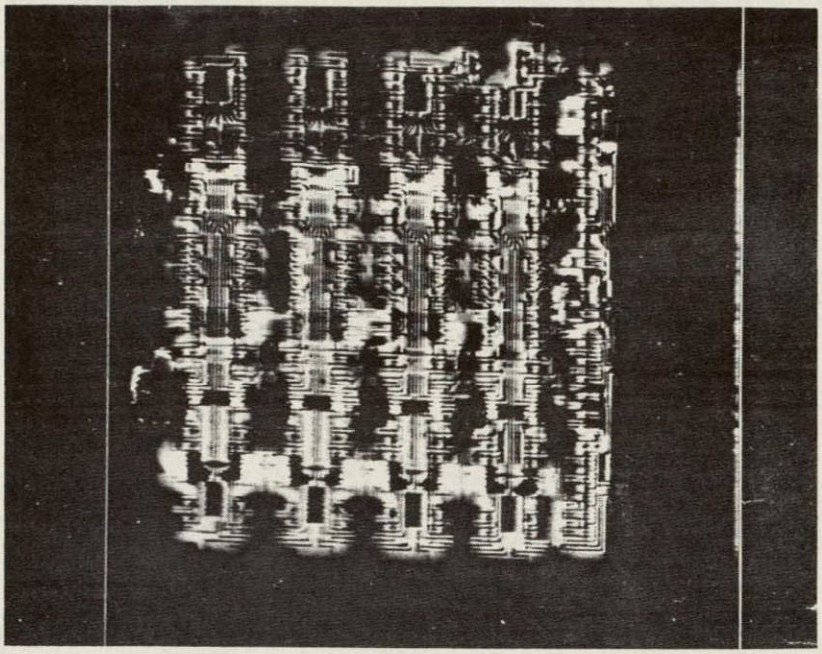

Figure 7.15. Image resulting from the subtraction of Figure 7.10 from Figure 7.8.

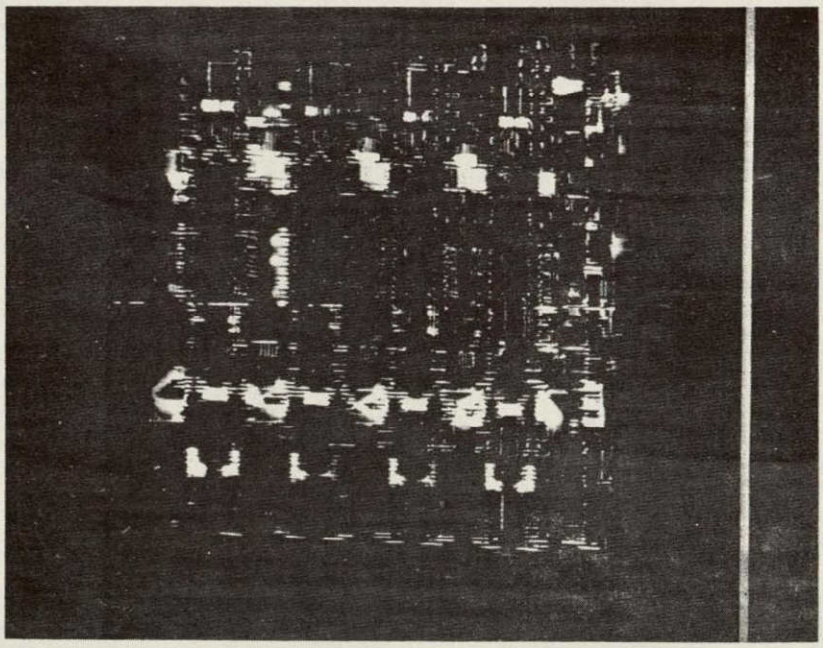

Figure 7.16. Image resulting from the subtraction of Figure 7.8 from Figure 7.10.

these differences. Also, there appeared to be a slight overall intensity difference (best observed in Figure 7.15) which can be correlated with the large difference in the I_{SS} parameter for these devices, since this is the only other parameter which is a result of the overall operation of the entire device.

Subtractions between images from device S/N 2, a "significantly different" device and device S/N 5, an "average" device are shown in Figures 7.17 and 7.18. Differences between these devices' images were observed. However, there is no definite basis for a correlation between the observed differences in the images and the measured differences in these devices' V_{OH} and V_{OL} parameters.

Subtractions between images from the failed device S/N 7, and the "average" device S/N 5, are shown in Figures 7.19 and 7.20. Many differences between the devices were revealed by the subtractions. Since so many differences were found between these device's images, no attempt was made to directly correlate all the differences to device S/N 7's failure. It was concluded that it was sufficient to note that there were many differences between the two images.

Correlation 2

The second correlation that was to be attempted was to try to correlate changes in the devices' electrical parameters following life tests with changes in the photoresponse images. The changes that were to be considered significant were those caused by inherent defects in the devices which caused the devices' electrical parameters to fail or degrade. Unfortunately, none of the devices' parameters changed significantly through a total of 500 hours of life tests. Subtraction between a device's images from Runs 1 to 4 revealed little or no change for several devices for which this comparison was performed. For some devices, there was a slight change in overall image intensity between Runs 1 and 4 which can be correlated with the tendency for the power supply current (I_{SS}) to drop from Run 1 to Run 4. As in the case of the CD4028A test devices, the only general correlation that could be made between the devices' photoresponse images and their electrical parameters was that neither changed significantly as a result of the life tests.

Correlation 3

It was hoped that a correlation could be made between devices whose parameters degraded or failed and unique elements in their initial photoresponse images. This correlation could not be made since none of the devices' parameters failed or degraded.

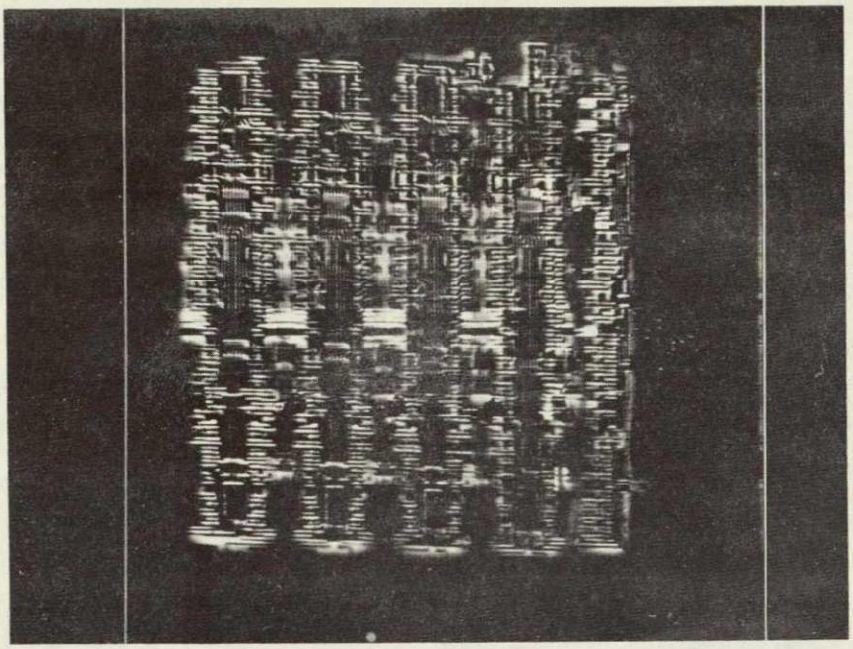

Figure 7.17. Image resulting from the subtraction of Figure 7.10 from Figure 7.9.

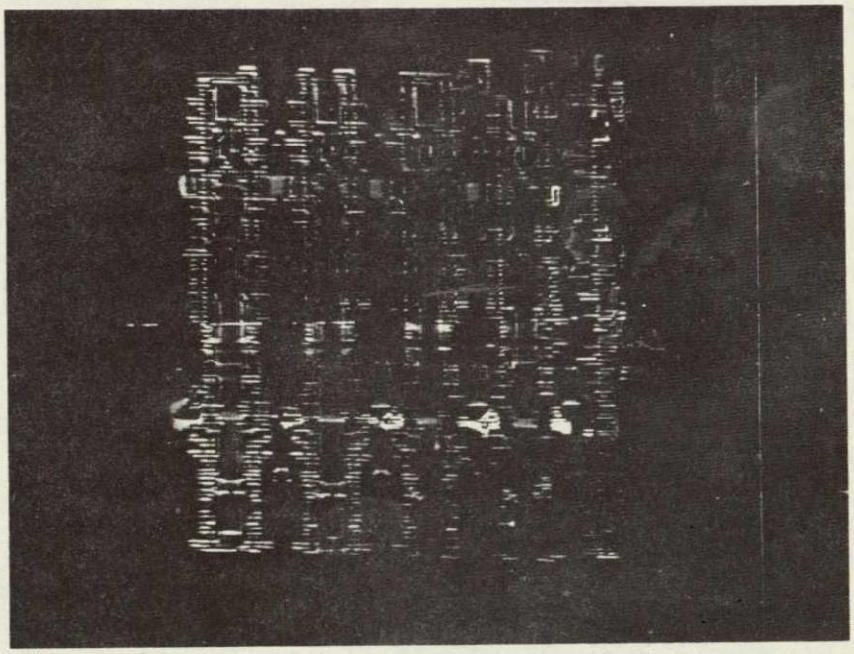

Figure 7.18. Image resulting from the subtraction of Figure 7.9 from Figure 7.10.

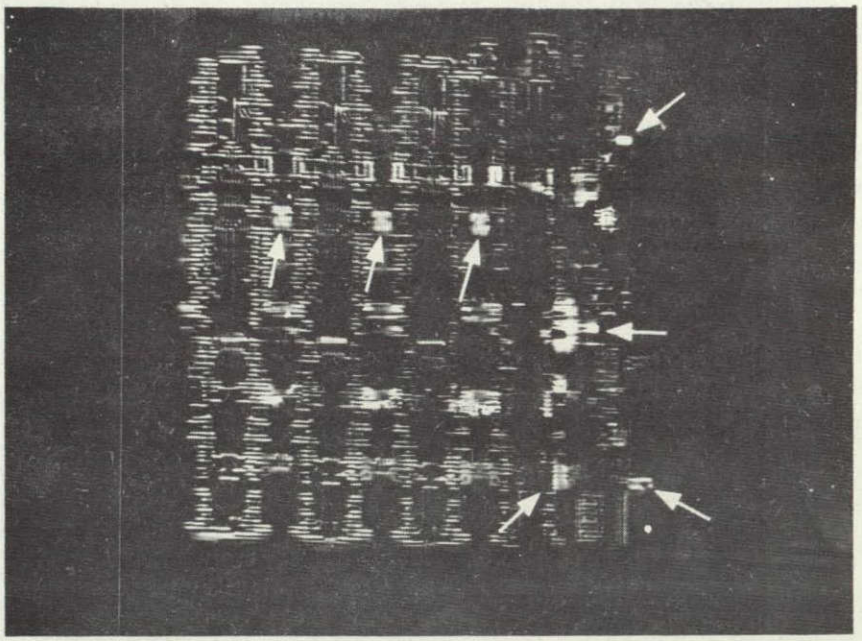

Figure 7.19. Image resulting from the subtraction of Figure 7.10 from Figure 7.12. Arrows indicate some of the significant differences revealed in this image.

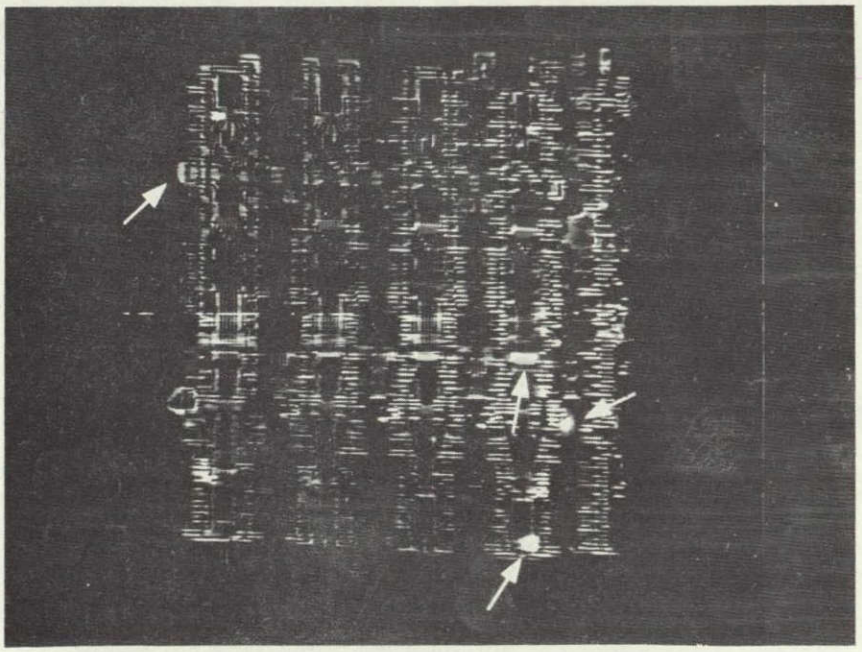

Figure 7.20. Image resulting from the subtraction of Figure 7.12 from Figure 7.10. Arrows indicate some of the significant differences revealed in this image.

8.0 CONCLUSIONS

To best review and evaluate the results of this prog[illegible] to recall the overall purpose with which it was undertaken. The purpose of this program was to investigate a new approach for the development of the optical scanner as a screening inspection instrument for microcircuits. The new approach was to compare quantitative differences in the photoresponse images and to correlate them with electrical parameter differences in test devices. There were four major tasks that were completed in order to implement and investigate this approach:

(1) The existing optical scanner instrumentation was modified so that the photoresponse data could be recorded and subsequently digitized.

(2) A method was developed to apply digital image-processing techniques to the digitized photoresponse data in order to do quantitative comparisons of the data.

(3) Electrical tests were performed and photoresponse images were recorded before and following life test intervals on two groups of test devices.

(4) Correlations were made between differences in the photoresponse data and differences or changes in the electrical parameters of the test devices.

The first task, to modify the existing optical scanner instrumentation for recording and subsequently digitizing the photoresponse data, actually was composed of two objectives:

(1) To provide quantitatively significant data.

(2) To provide a means of recording and digitizing this data.

This task was successfully completed by modifications and additions to the previously existing instrumentation. The new laser that was incorporated into the system greatly increased the stability and useful signal level of the signal generated by the instrumentation. The addition of a FM magnetic tape recorder along with an interface designed to provide the appropriate logic signals created the means for recording the photoresponse signals. The resulting magnetic tapes were digitized so that they could then be analyzed using procedures developed in the next task.

The second task of the program, the development of a method to apply digital image-processing techniques to the digitized photoresponse data, was accomplished by the modification and subsequent application of some established image processing software routines and hardware facilities. After the recorded photoresponse data had been digitized, the software applied algorithms to reduce the data to an array representative of each photoresponse image from each device. The data was then reformatted so that it could be processed by the facility which was used to display and photograph both the recorded data as well as the data resulting from image subtractions and other image processing routines.

The third task of the program, to perform electrical tests on test devices and record their photoresponse images before and following life test intervals was the most straightforward of the tasks. Prior to any life testing, the electrical parameters and photoresponse images from a group of twenty-five CD4028A test devices and a group of twenty-five CD4034A test devices were measured and recorded. All of the electrical parameters of all of the CD4028A test devices were within specification limits. One of the CD4034A test devices failed several electrical parameter tests, but all of the other devices' parameters were within specification limits. Following three intervals of life-tests which totalled 500 hours for each test group, there was very little or no change in the electrical parameters of the test devices. Two of the CD4028A test devices failed during the testing, but both failures were discovered to be a result of mechanical damage incurred during handling. These failures were disregarded, since the only change that was considered to be significant for the purposes of this program was electrical parameter degradation or failure resulting directly from the life tests.

The fourth task, correlation of changes or differences in electrical parameters of the test devices with differences in their photoresponse images, consisted of three specific parts:

(1) Correlation of differences in the initial electrical parameters from device to device with differences in the initial photoresponse images.

(2) Correlation of changes in electrical parameters of each device following life tests with differences in its photoresponse images.

(3) For any device which failed at some point in the life test (or whose electrical parameters significantly degraded) determine if there is anything unique in its initial photoresponse image which can be correlated with its subsequent failure.

The extent to which these various correlations could be made would be the test of this new approach for the development of the optical scanner as a screening inspection instrument.

Some correlations were made between differences in initial electrical parameters and differences in photoresponse images for both the CD4028A and CD4034A test device groups. The most obvious correlation was made for the one CD4034A test device which was a parametric failure at the initial electrical test. Subtractions of this device's photoresponse image from photoresponse images of other devices whose specifications were all within specification limits revealed many obvious differences. The other correlations between differences in initial electrical parameters and differences in photoresponse images were not made from observations of obvious differences in photoresponse images for the other test devices. Rather, these correlations were made through comparisons of subtle differences in the images that resulted from the subtraction of two photoresponse images. However, this did demonstrate that the new approach of quantitative analysis was successful. Many of the differences that were revealed by the subtraction of two images were virtually undetectable by visual comparison of the two images.

Initially, it would appear to be a somewhat negative result that the differences in the device's electrical parameters could only be related to subtle differences in their photoresponse images (except for the one CD4034A test device which failed several initial parametric tests). Even though there were differences in their electrical parameters, these devices were all fully functional and their electrical parameters were all within specification limits. Therefore, an effective screening inspection technique using the optical scanner should not reveal large differences between these devices. The results of this program did not conflict with this requirement. Also, an effective screening inspection technique using the optical scanner should reveal large differences between a device whose electrical parameters are outside of specification limits and one whose parameters are acceptable. The results of the comparison of the optical scanner examinations of the one CD4034A test device whose parameters were unacceptable with other test devices revealed significant differences as required.

The other correlation between electrical parameter changes following life tests and photoresponse image differences could not be made. Except for two CD4028A devices that weremechanically damaged during handling, there were no significant changes in electrical parameters for any of the test devices following a total of 500 hours of life testing. The only correlation that could be made was that there were also no significant changes in the photoresponse images

following the life tests.

The other endeavor of the program, to analyze the initial photoresponse images from the test devices in order to determine if they contained information which could be used to predict future device degradation or failure, could not be investigated. Since none of the test devices failed or degraded as a result of inherent defects during the life tests, there was no possibility of analyzing the initial photoresponse images for indications which could have been used to predict the failures.

In summary, it was shown that it is possible to implement a method to perform quantitative analysis of the optical scanner photoresponse images using digital image-processing techniques. Some correlations were made between the test devices' electrical behavior and the differences in the photoresponse images as a result of the new approach that was implemented. Unfortunately, no significant correlations between devices failed or degraded electrical parameters and photoresponse differences could be made except in the extreme case of one device which failed several electrical tests from the beginning of the program. This was due to the fact that the devices electrical parameters did not fail or degrade due to inherent problems during the life tests.

The results of this program suggest that additional studies be performed using new groups of test devices which would be subjected to either longer life test durations or life tests of more severe test conditions. Since it was shown that correlations could be made between subtle differences in device electrical parameters using the quantitative analysis approach, it should be possible using minimal effort to correlate failed or degraded electrical parameters with changes in photoresponse images. At this point, evaluation of the initial photoresponse images can be performed to determine if there is information in the initial photoresponse image of a device that can be used to predict the failure of the device. If this information does indeed exist, then an extremely valuable screening inspection instrument and technique would be the result. The major developmental effort at that point would be to expand the capabilities of the instrument to include all technologies since CMOS microcircuits have been the main technology investigated up to this point. Also, additional techniques still need to be developed and evaluated for some of the more specialized microcircuit types, such as memories. Once all of these problems were solved and the required techniques were developed, the result would be semiconductor devices whose reliability was greatly improved through the application of the optical scanner as a screening inspection instrument.