CORRELATOR COMPUTER INTERFACE AND MODULE IMPLEMENTATION– MARK III PROCESSOR

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INTRODUCTION

This paper briefly describes two hardware aspects of the Mark III Processor treated in the previous paper by Alan Whitney. The first area concerns the choice of interface to the controlling minicomputer and the second area concerns the implementation of the correlator module.

COMPUTER INTERFACE

At the outset of the hardware design associated with the Mark III Processor, it became obvious that one of the major functions which would have to be designed was a large computer-to-correlator module I/O bus or module selector to facilitate communications with the 90 independent correlator modules. Another outstanding design task identified was the mechanical packaging of the correlator circuitry. Our investigation of CAMAC (Computer Automated Measurement and Control)-IEEE Std 583-1975, convinced us that both of these functions were available to us without the burden of engineering through the use of the standard. Another benefit was that CAMAC provides independence from the host computer, which in our case had not yet been specified. The connecting link to the host computer, of course, must be computer-specific; this link, the branch driver, is available for most popular minicomputers. In our case, an HP1000 minicomputer was selected; although a branch-driver of American manufacture was not available, a unit of European manufacture was.

As with most human endeavors, perfection does not exist or in any event last very long. We have deviated from the CAMAC standard in our processor development in two areas. The first area is power. We require +5 volts at 80 amperes per crate complement of 15 correlator modules. Consequently, we have converted the +6-volt bus to +5-volt use and in addition have defined two adjacent buses for +5-volt use in order to increase current-carrying capacity into each module. The second area involves the physical size of the correlator modules and the crates into which they are plugged. Our final correlator circuit design is comprised of 340 elements, mostly dual in-line package integrated circuits. In order to accommodate this population, our module is 3.5 inches taller, 5.3 inches deeper, and 1.5 times as wide as a standard single-width CAMAC module. In each of the six crates required for our system, we accept 15 modules in the first 22.5 slots. We mate with the standard

CAMAC dataway (backplane) by means of an auxiliary connector edge board offset by one-half a module width in alternate modules. Procurement of the special CAMAC hardware did not require generation of engineering drawings and the costs were very reasonable.

MODULE IMPLEMENTATION

The circuit design of the Mark III correlator module represents a conservative approach in that no custom LSI was undertaken; it was felt that the risks in project time and funding were not warranted even though a reduction in number of circuit elements might have resulted. The majority of the circuits used are low-power Schottky TTL types, with the balance being NMOS RAM's, TTL RAM's, and several PROM's used as sequence controllers. Power consumption is about 26 watts per module.

As mentioned previously, the component count had reached 340 at the end of the design phase. A normal single-width CAMAC module holds in the order of 80 to 90 IC's using printed circuitry as an interconnection media. Multiple CAMAC modules and a single "large" CAMAC module were considered as possible packaging forms for the correlator. The "large" CAMAC module approach was chosen because of the difficulty in partitioning the correlator with minimum interconnections, the fabrication economy of a single large planar assembly, and the desire to minimize the number of modules (thereby staying within the hardware capacity of a single CAMAC branch which requires only two HP I/O slots). Wrapped-wire interconnections were used in order to allow easy modifications during the development phase and were also utilized in the production phase to avoid the high costs and risks associated with multi-layer printed-circuit boards. Another benefit of the wrapped-wire approach is increased component density; our "large" CAMAC module holds four times the IC's in three times the volume of a printed-circuit single-width module.

Our experience in the production and checkout of correlator modules has been positive. The bulk of the fabrication is accomplished by contract machine wrapping, leaving component population of the panel as the major in-house task, along with checkout. Checkout of each module is averaging four hours. Approximately half the modules work when plugged in; the balance have some combination of wiring or population problem.

The cost of the materials and services for each module is under $1000, with the allocation roughly equal among the basic wrapped-wire panel, wiring services, and integrated circuits.