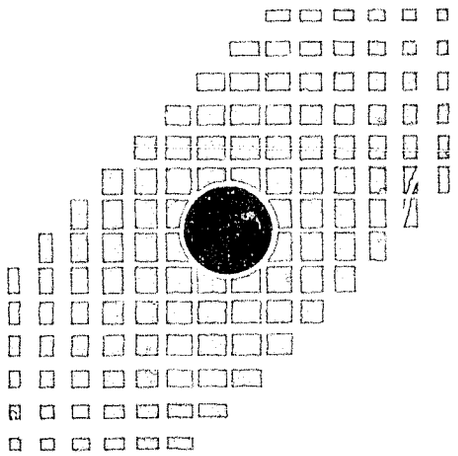
SCHOOL OF ENGINEERING
DUKE UNIVERSITY
DURHAM, NC 27706

CENTER FOR SOLID-STATE POWER CONDITIONING AND CONTROL



RESEARCH ON DESIGN FEASIBILITY OF HIGH-POWER LIGHT-WEIGHT DC-TO-DC CONVERTERS FOR SPACE POWER APPLICATION

Sixth Semiannual Status Report
May 31, 1980

Prepared for

National Aeronautics and Space Administration
Lewis Research Center
Research Grant No. NSG-3157

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1. BACKGROUND

Due to the anticipated future power requirements of larger spacecraft, the need to develop light-weight high-power dc-to-dc conversion systems has been established. In order to respond to this need, research into the development of such light-weight high-power converters was begun for NASA Lewis Research Center on July 1, 1977 in the Department of Electrical Engineering at Duke University.

Research has been directed toward the development of a 10-kilowatt module, which would then be paralleled with nine other such modules to provide regulated outputs for up to a 100-kilowatt system. The original design goals called for a system which would supply a regulated +500 V and -500 V with respect to the neutral of a 3-wire dc distribution system from an unregulated dc source ranging from 120 V to 240 V. However, with NASA Lewis Research Center agreement, in recognition of the types of stresses that these initially selected target values would place on the components of a dc-to-dc converter such that many of the required electrical components are simply unavailable in the types of ratings necessary to sustain such design goals, the requirements for the output voltage have been changed to +400 V and -400 V, while the acceptable input voltage range has been modified to 110 V through 180 V. A design goal which has remained unchanged throughout the course of this research is the selection of 100 kilohertz as the converter switching frequency, serving to effect significant reduction in the physical size and weight of the converter by reducing the size and weight of the converter's energy storage elements.

The development toward a 10-kilowatt module has proceeded thus far in two phases, each phase being so directed as to push the limits of present-day technology. The first goal of constructing and testing a one-kilowatt two-winding energy-storage converter has been completed, and work is continuing at

this power level in order to improve the converter performance through better understanding of the phenomena associated with such a high-frequency high-power converter. Alongside, and in primary focus at this time, is work on the second phase consisting of the development of a 5.0-kilowatt module, consisting of two 2.5-kilowatt submodules whose outputs are to be connected in series, each 5.0-kilowatt submodule forming one half of the eventual 10-kilowatt module. This report, which covers the period of December 1, 1979 through May 31, 1980 is principally concerned with the progress as well as the problems associated with the present 2.5-kilowatt converter, and with factors affecting the development of future higher-power modules.

2. PERSONNEL

During the period covered by this report, the following personnel were associated with the research project:

Faculty: Dr. Thomas G. Wilson, Principal Investigator; Dr. Harry A. Owen, Jr., Associate Investigator; and Dr. Rhett T. George, Jr., all part-time.

Graduate Research Assistants: Mr. Thomas H. Sloane, Mr. Paul M. Wilson, and Mr. Ronald C. Wong, all one-half time. Mr. Sloane and Mr. Wilson are doctoral candidates in Electrical Engineering, and Mr. Wong is a candidate for the M.S. degree in Electrical Engineering.

3. DOCUMENTATION

(1) A paper entitled "Predicting Performance of Power Converters Operating with Switching Frequencies in the Vicinity of 100 kHz," David D. Bahler, Harry A. Owen, Jr., and Thomas G. Wilson, was published as a part of the proceedings of the 1978 Power Electronics Specialists Conference, PESC-78, IEEE Publication 78CH1337-5AES, pp. 148-157 (June 1978).

(2) A paper entitled "Switching Transients in High-Frequency High-Power Converters Using Power MOSFET's," Thomas H. Sloane, Harry A. Owen, Jr., and Thomas G. Wilson, was published as a part of the proceedings of the 1979 Power Electronics Specialists Conferences, PESC-79, IEEE Publication 79CH1461-3AES, pp. 244-255 (June 1979).

(3) A paper entitled "A DC Model for Power Switching Transistors Suitable for Computer-Aided Design and Analysis," Paul M. Wilson, Rhett T. George, Jr., Harry A. Owen, Jr., and Thomas G. Wilson, was published as a part of the proceedings of the 1979 Power Electronics Specialists Conference, PESC-79, IEEE Publication 79CH1461-3AES, pp. 428-436 (June 1979).

(4) A paper entitled "Modeling Switching-Time Effects in High-Frequency Power Conditioning Networks," Harry A. Owen, Jr., Thomas H. Sloane, Ben H. Rimer, and Thomas G. Wilson, was published in the proceedings of an International Symposium sponsored by the European Space Agency and the University of Bologna, SPACECAD 79, Bologna, Italy, 19-21 Sept. 1979, (ESA SP-146, Nov. 1979), pp. 325-337.

(5) A paper entitled "Switching-Interval Modelling in Very High Frequency High Power MOSFET Converters," Harry A. Owen, Jr., Thomas H. Sloane, Ben H. Rimer, and Thomas G. Wilson, was prepared and presented at the Seventh National Solid-State Power Conversion Conference, POWERCON 7, in March 1980 in San Diego, Calif., and was published in the Proceedings of the Seventh National Solid-State Power Conversion Conference, pp. G1-1 to G1-13 (March 1980).

4. RESEARCH SUMMARY

4.1 Overview

During the period documented by this report, two advances in semiconductor technology have enabled project personnel to operate light-weight dc-to-dc converters with 100-kilohertz switching frequencies at substantially higher power levels than were previously possible with available power switching transistors. In addition, the amount of power processed per power switching transistor has also increased substantially. First, eight of the new International Rectifier IRF350 HEXFET's with ratings of 11 A and 400 V were operated in parallel to provide a converter output power of approximately 2000 W. Second, a recently developed bipolar power switching transistor, the International Rectifier HPT540, was operated in conjunction with a newly developed turn-off snubber circuit to provide converter output power levels approaching 1000 W.

In parallel with these advances in power levels at the 100-kilohertz conversion frequency, work continued on a study of the interrelationships between mass, switching frequency, and efficiency. Converters were constructed for operation at a maximum output power level of 200 W, and a comparison was made for operation under similar input/output conditions for conversion frequencies of 20 kilohertz and 100 kilohertz. The effects of nondissipative turn-off snubber circuitry were also included in that study.

Finally, the computerized instrumentation system advanced to the point where the measurement of pertinent converter operating conditions as well the recording of converter waveforms can be routinely performed. This system has been operated reliably at converter output power levels of up to 2000 W, and has proven to

be of great assistance to project personnel involved with the operation of these higher-power converters.

4.2 2.5-Kilowatt Converter Developments

4.2.1 Converter without Snubber Circuit

The approach being employed in the development of the 5-kW converter is to use a circuit configuration involving two submodules, each capable of supplying up to 2.5 kW of output power, which are to be incorporated into a single 5-kW module. Figure 1 is a schematic of the 5-kW module which may be viewed as two individual voltage-or-current step-up energy-storage converters connected together with parallel inputs and series outputs. In this manner the input voltage of each submodule corresponds to the input voltage design range of 110 V to 180 V for the module, while the output voltage of each submodule is 200 V, resulting in an output voltage of 400 V when the submodules outputs are added in series in the 5-kW module. Each of the power switches represented by a single FET symbol in Fig. 1 is composed of a parallel configuration of eight FET's as seen in Fig. 2 which is a complete schematic of a 2.5-kW submodule.

The resistors in series with each FET gate lead in Fig. 2 are present to dampen out any high-frequency oscillations that may occur in parasitic resonant circuits in the gate and drain circuits. A MOS clock driver, the DS0026, is used as the gate drive with the four drivers in two packages paralleled to provide enough power to drive the eight individual gate resistors and the effective input capacitance of the eight FET's. Transistor inverter Q9 is used so that if the pulse-width modulator inadvertently is disconnected or undergoes a loss of power, the duty ratio becomes 0% rather than 100%.

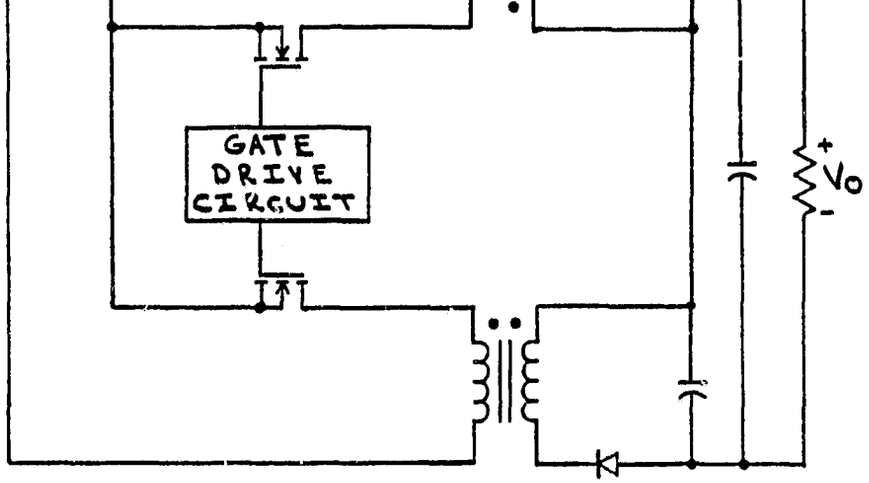


Fig. 1 5-kW module composed of two voltage-or-current step-up converters with parallel inputs and series outputs.

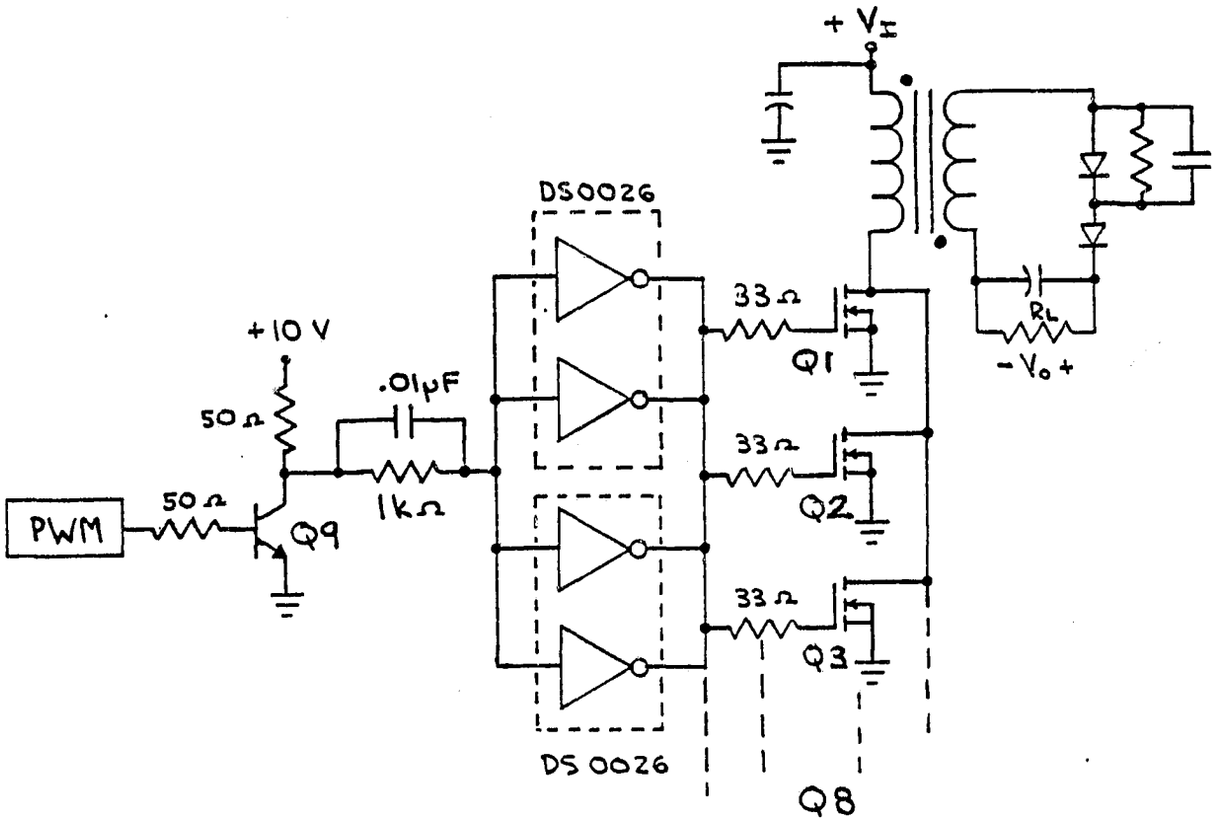


Fig. 2 2.5-kW submodule with drive circuitry and 8 parallel FET's as the controlled switch.

Major concerns in the design and implementation of the power stage are the voltage stresses imposed on the FET's and the diode during the turning-on and turning-off periods when a large di/dt exists in the circuit. Specifically, during the turning-off of the FET's and during the diode turning-off transitions, large spikes of voltage superimposed on the eventual blocking voltage are present. Close attention to minimizing circuit path lengths results in minimal stray circuit inductance in the drain and secondary circuits which reduces these inductively produced voltages. A different effect is produced by the effect of stray circuit inductance between the FET source pins and the return path of the gate drive. This inductance has the effect of causing a voltage that opposes the gate drive voltage. This negative feedback decreases the effective amplitude of the gate drive, increasing the transition times from the off-state to the on-state and vice-versa, thus decreasing the di/dt and lowering the induced voltage spike [1]. The stray circuit inductance that exists between the power source and the input to the converter is bypassed by an electrolytic filter capacitor connected to the circuit by a sandwich type of bus. At the converter-circuit end of this bus, a small capacitor with low ESR and low ESL is used to aid in reducing any remaining small induced voltages due to the reactance arising from the length of the sandwich-type bus. A similar arrangement is used for the output filter capacitor.

Typically, the stray circuit inductances in the primary and secondary loops are much smaller in magnitude than the respective leakage inductances in the primary and secondary of the energy-storage reactor. That is, the degree of coupling between primary and secondary windings of the energy-storage reactor is the dominant parameter in determining both the total primary loop and the total secondary loop stray inductances. Using a winding technique which maximizes the

coupling between the primary and secondary windings will decrease the total stray inductance in both the primary and secondary loops,which for the same di/dt during switching results in lowering voltage stresses on both the FET's and the secondary diode.

A true bifilar-wound core has excellent coupling but this winding technique may only be used in reactors with a 1:1 turn ratio. When a turn ratio other than 1:1 is required, use of a semi-bifilar method as shown in Fig. 8 of the November 30, 1979 Semiannual Status Report is required which results in poorer coupling than use of a true bifilar winding method. Experience with the reactor in the 1-kW module has shown that a 1:2 turn ratio, with its larger leakage inductances compared to a 1:1 turn ratio, places lower total voltage stress on the FET's. With the 1:2 turn ratio, a larger spike may exist, but since the secondary voltage is halved when reflected to the primary side because of the 1:2 turn ratio, the peak voltage stress on the FET's is less than with the 1:1 turn-ratio reactor.

The turn ratio of 1:2 was used as a design parameter in the energy-storage reactor design program DC2DC which resulted in several possible designs presented in Appendix A of the November 30, 1979, Semiannual Status Report. Of the possible designs obtained in the computer run, those with more than a one-core stack were discarded because of the desire to limit the number of magnetic energy-storage elements in the 5-kW module to two. The design chosen to initially investigate requires an Arnold Engineering A-127259 core wound with 11 turns on the primary and 22 turns on the secondary. Other designs either did not have enough turns to completely encircle the toroid, resulting in increased leakage inductance, or the core would not stay in the continuous mmf mode over the entire operating range. The core used has a relative permeability of 147, a cross-sectional area

of 733 mm^2, and a mean magnetic path length of 25 cm. Two A-127259 cores were purchased from Arnold Engineering and wound using different methods and used in the converter. When the currents measured using these cores were compared with the currents as predicted by the evaluation section of the program DC2DC, large discrepancies were apparent. Subsequent experiments including a reactance measurement at 400 Hz, measurement on a General-Radio bridge at 1000 Hz, and a di/dt measurement with a square-wave of voltage applied, all verified that the relative permeability of the cores received from Arnold Engineering was not 147 but approximately 50. Three and a half weeks after these defective cores were first used, two replacement cores were received from Arnold Engineering. When these cores were wound and placed in the converter, the circuit operation was as predicted by the reactor design program DC2DC.

Use of a 1:2 turn ratio for the reactor does place increased voltage stress on the secondary diode because of the doubling of the primary voltage when reflected to the secondary. Two Motorola MR1386 600-V 20-A diodes were placed in series on separate heat sinks to achieve the necessary blocking voltage. During operation at modest power levels it was observed that the reverse voltage across the two diodes was not shared equally between them since the diodes did not have identical reverse leakage currents and the junction and stray circuit capacitances associated with the individual diodes were different. During the switching intervals the diodes share the reverse voltage in inverse relation to their junction and parallel circuit capacitances which have a low impedance during the switching interval relative to the diode dc resistance. However, during the blocking interval the voltage is distributed across the diodes according to their individual dc blocking characteristics. In this instance neither the transient nor the blocking voltages were being distributed equally.

To force equal sharing of these voltages an RC combination was added to the diode with the larger blocking and transient voltages, as seen in Fig. 2. The resistor is used to achieve sharing while the diodes are blocking and the capacitor functions to compensate during the switching intervals.

Eight International Rectifier IRF350 devices rated at 400 V, 11 A, and 150 W are configured in a parallel combination to form the controlled power switch. These eight FET's are mounted in a circular arrangement on a water-cooled heat sink identical to the one used in the 1-kW module shown in Figs. 1 and 2 in the November 30, 1979 Semiannual Status Report. During operation at power levels of 2 kW the copper plate on which the FET's are mounted remains cool while the temperature of the top of the case of the FET's rises to an estimated 65° C. At this case temperature the individual FET's can safely dissipate 100 W as seen from Fig. 11 in the International Rectifier IRF350 data sheet. If all eight FET's are at the same case temperature and share the dissipated power equally, then the eight FET's in parallel may safely dissipate 800 W. As data presented in Table 1 indicates, at 2 kW of output power, 607 W of power is dissipated in the various components that comprise the power stage. Calculation of power loss in the output capacitor, in the output diodes, and in the reactor results in approximately 75 W of loss which leaves the eight parallel FET's to dissipate the remaining 532 W. Consequently, knowing that the power is not distributed equally among the parallel FET's and to allow some reasonable margin, eight FET's are used to achieve an estimated 800 W of power handling capability to dissipate the 532 W estimated to be lost in the controlled switch. International Rectifier has generously supplied the research group with fourteen IRF350 power FET's with maximum drain-to-source voltages ranging from 340 V to 390 V, and it is eight of these that are presently used in the 2.5-kW submodule.

The submodule is located on a bench with a copper sheet located just under the benchtop to which all instrumentation is attached through the use of low-impedance copper strips. In this manner a good uniform ground is assured, providing a means of obtaining accurate measurements. Used as the input power supply is a Hewlett-Packard Model 6477C, with an output rating of 0 V to 220 V at 50 A. This unit initially was received in faulty condition, necessitating its return to Hewlett-Packard for repairs which took one month. Operation of the converter has been obtained in an open-loop mode with output power levels of up to 2.2 kW momentarily and up to 2 kW for periods of 3 and 4 minutes. Continuous operation at these power levels was prevented by an increase in case temperature of individual FET's above 65° C to a level where individual FET's may have been dissipating more power than allowed by the specifications at the elevated case temperature. Table 1 presents data taken at the 2 kW output power level.

Table 1. Data for the 2.5-kW Converter Without Snubber

Input voltage	75 V	Output voltage	152 V
Input current	34.8 A	Output current	13.2 A
Input power	2608 W	Output power	2001 W
Duty ratio	0.5	Load	11.25 Ω

Efficiency 77%

Figures 3, 4 and 5 are oscillograms taken under the operating conditions given in Table 1. Figure 3 shows two cycles of total source current along with drain-to-source voltage, while Fig. 4 is an expanded view of the turning-on

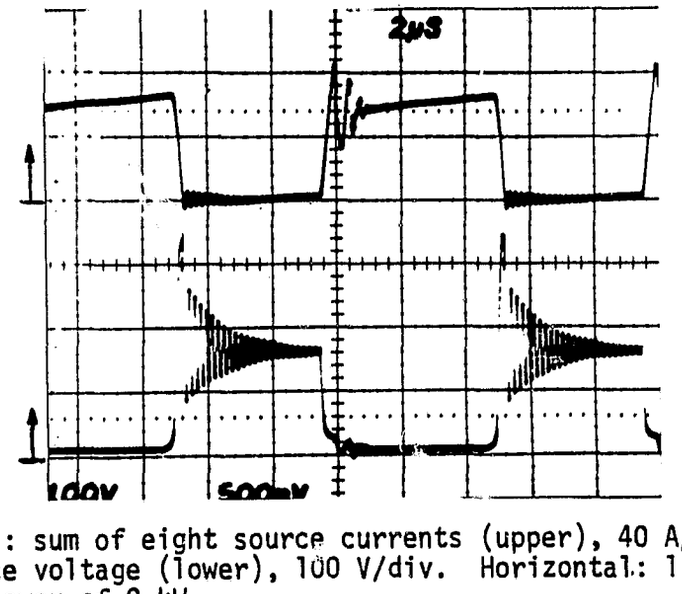


Fig. 3 Vertical: sum of eight source currents (upper), 40 A/div.; drain-to source voltage (lower), 100 V/div. Horizontal: 1 microsecond/div. Output power of 2 kW.

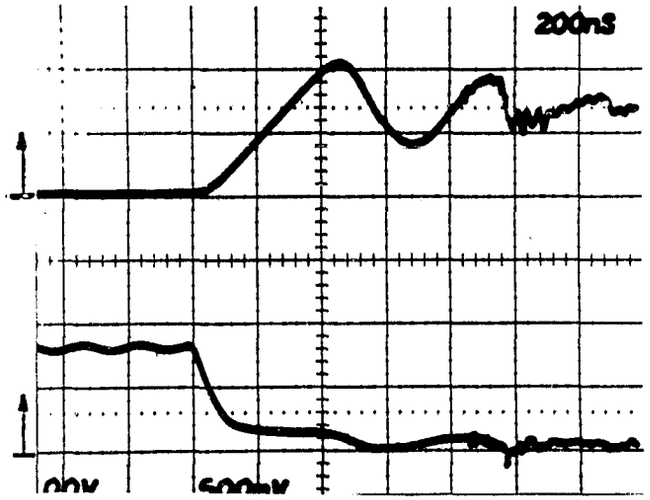


Fig. 4 Turning-on as expanded from Fig. 3, same vertical scale factors as Fig. 3. Horizontal: 200 nanoseconds/div.

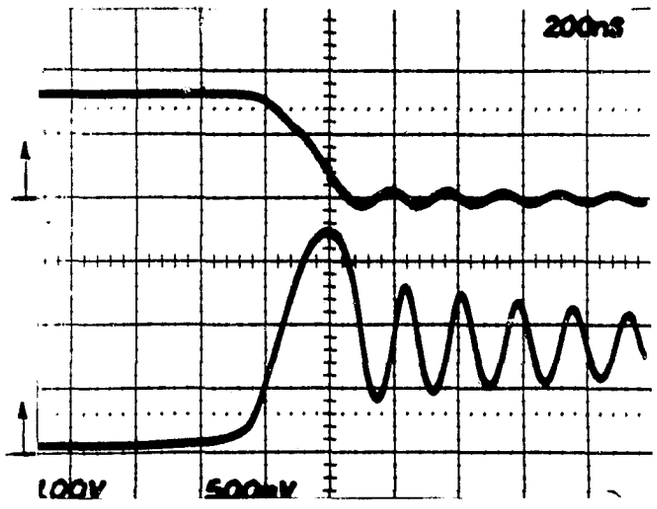


Fig. 5 Turning-off as expanded from Fig. 3, same vertical scale factors as Fig. 3. Horizontal: 200 nanoseconds/div.

waveforms and Fig. 5 an expanded view of the turning-off waveforms. The peak source current is seen to be approximately 80 A, which is much less than the 200-ampere capability of eight IRF350's in parallel. This emphasizes that the number of FET's needed is based on the amount of power each FET may safely dissipate, and not on their maximum current handling capability. Examination of Figs 3, 4 and 5 reveals that substantial power loss occurs only during the turning-off interval. This is best seen in Fig. 5 where large positive values of current and voltage occur simultaneously. This qualitative deduction is verified by a study of a representative power waveform generated using the Biomation Waveform Recorder and the computer program BIOV1 as shown in Fig. 21 in section 4.5.2 of this report.

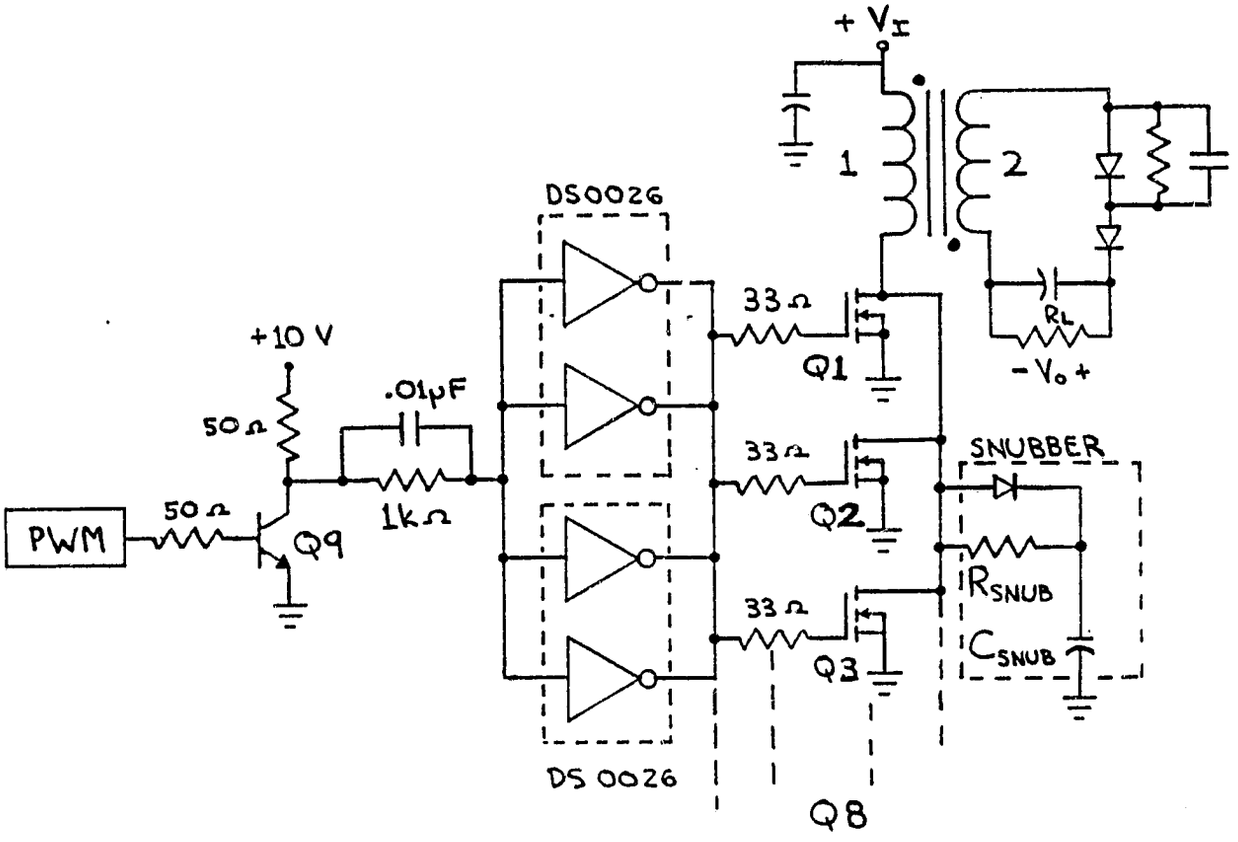


Fig. 6 Same as Fig. 2 with turn-off snubber circuitry added with C_{SNUB}=.02 μF and R_{SNUB}=66 Ω.

4.2.2 Converter with Turn-off Snubber

To decrease the power dissipated in the FET's which will lower the operating temperature allowing longer operating periods and higher output power, a dissipative turn-off snubber was designed and added to the circuit as shown in Fig. 6. A description of the basic operation of the snubber begins with the capacitor C_{SNUB} discharged through the resistor R_{SNUB} during the on-time of the FET's. When gate drive is removed from the FET's, primary current which has been flowing through the FET's is partially diverted through the snubber diode into the snubber capacitor. Eventually the snubber capacitor voltage rises sufficiently so that the primary voltage reflected to the secondary causes the forward biasing of the secondary diodes and reactor current flow shifts from the primary to the secondary as required to maintain a continuous core mmf. The data presented in Table 2 corresponds to the operation with the turn-off snubber at an output power level of approximately 2 kW.

Table 2. Data for the 2.5-kW Converter with Turn-off Snubber

Input Voltage	73.1 V	Output Voltage	150.5 V
Input Current	34.7 A	Output Current	13.0 A
Input Power	2536 W	Output Power	1961 W
Duty Ratio	0.5	Load	11.25 Ω

Efficiency 77%

Figure 7 is an oscillogram of two switching cycles while Fig. 8 is an expanded picture of the turning-on interval and Fig. 9 an expanded picture of the turning-off interval. As can be seen in Figs. 7 and 9 during the turning-off interval after the source current has reached zero, the drain-to-source

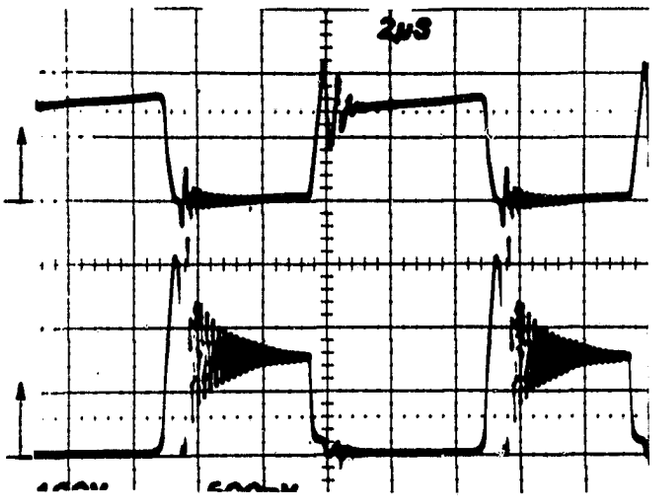


Fig. 7 Same waveform variables and scale factors as Fig. 3; snubber used as shown in Fig. 6.

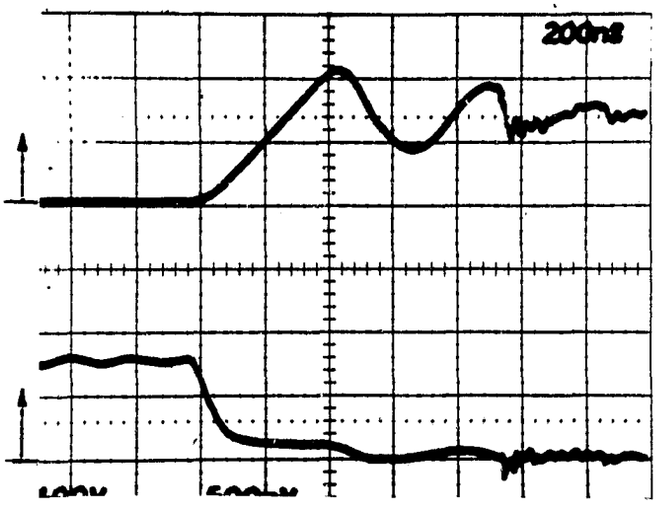


Fig. 8 Same waveform variables and scale factors as Fig. 4; snubber used as shown in Fig. 6.

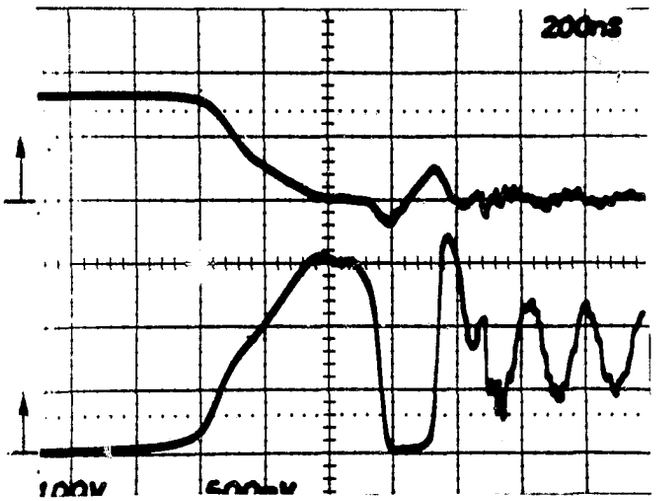


Fig. 9 Same waveform variables and scale factors as Fig. 5; snubber used as shown in Fig. 6.

voltage undergoes a large transient and eventual ringing upwards to produce the maximum voltage stress. It is this voltage overshoot which is present with or without the snubber and the absolute maximum drain-to-source voltage rating of 340 V for the particular IRF350's in use that limits the output power to 2 kW. At the 2-kW level the presence of the snubber had little effect on the efficiency, but a significant portion of the turning-off power loss was moved from the FET's to the snubber resistor allowing cooler operation of the FET's. Longer converter operating times of 15 minutes were possible, as contrasted to the 2 to 3 minutes maximum operating time without the snubber. Higher output power levels can be achieved by using the IRF350's specified with a maximum drain-to-source voltage of 400 V, and these FET's will be used as further experience is gained in the operation and performance of the 2.5-kW submodule.

4.3 Continuation of Study of Reactor Mass Versus Switching Frequency

An initial study of the variation of the magnetic reactor mass (core mass plus copper mass) with respect to different switching frequencies was carried out in the previous research period and the results reported in Section 4.4 of the November 30, 1979 Semiannual Status Report. In that study, a computer-aided approach based on commercially available powder permalloy cores was made to design magnetic reactors for switching frequencies from 10 kHz up to 100 kHz. It showed, for example, that the mass of the reactor can be reduced by approximately seventy percent if the switching frequency is increased from 20 kHz to 100 kHz. However, the benefit gained by the reduction in mass is compromised by the increase in switching loss associated with the higher switching frequency. As a result, a preliminary trade-off study of power loss versus mass has been initiated in the present reporting period.

To study the trade-off between the increase in power loss and the reduction in mass, two magnetic reactors were designed for operation, respectively, in a 20-kHz and a 100-kHz switching environment. The two magnetic reactors were designed for constant-frequency operation in a voltage-or-current step-up (buck-boost) converter with an input voltage range of 60 V to 120 V, an output voltage of 125 V, and a maximum output power of 200 W. Both of these magnetic reactors have a one-to-one primary-to-secondary turn ratio, and they were each wound bifilar to reduce the leakage inductance in the individual windings. Table 3 gives detailed information on the two magnetic reactors. As shown from the table, the mass of the magnetic reactor designed for switching at 100 kHz is 0.335 kg smaller than that of the magnetic reactor designed for switching at 20 kHz.

TABLE 3. Specification of the Two-winding Voltage-or-current Step-up Converter for Comparison of the Power Loss at Different Switching Frequencies.

	20-kHz	100-kHz
Magnetic Core	2-core stack of Magnetics 55108	2-core stack of Magnetics 55584
Turn Ratio	1:1	1:1
Number of Turns in the Primary	24	14
Mass of Reactor (Copper and Core Mass)	0.4535 kg	0.1185 kg
Input Voltage Range	60 V to 120 V	
Output Voltage	125 V	
Maximum Output Power	200 W	

Using the magnetic reactor designed for switching at 20 kHz, three International Rectifier IRF330 HEXFET's individually rated at 400 V and 8 A peak current, a Motorola MR1386 600-V diode rated at 20 A, and two high-voltage capacitors, a dc-isolated two-winding voltage-or-current step-up converter was built and various data were collected for the input voltage range of 60 V to 120 V. Then the magnetic reactor designed for a switching frequency of 20 kHz was replaced by the magnetic reactor designed for switching at 100 kHz, and the rest of the converter was left unchanged. Data were collected for the converter operated at 100 kHz over an identical range of operating conditions for which data had been collected for the 20-kHz converter. Table 4 displays the data for comparison of the power loss at the two different switching frequencies.

TABLE 4. Comparison of Power Loss at Different Switching Frequencies

Switching at 20 kHz

Input Voltage (V)	Input Power (W)	Output Power (W)	Power Loss (W)	Efficiency (%)
60	216	200	16	93
80	220	200	20	91
100	220	200	20	91
120	221	200	21	90

Switching at 100 kHz

Input Voltage (V)	Input Power (W)	Output Power (W)	Power Loss (W)	Efficiency (%)
60	253	200	53	79
80	255	200	55	78
100	256	200	56	78
120	262	200	62	76

The converter switching at 100 kHz obviously has higher power loss than its counterpart switching at 20 kHz. This higher power loss can be attributed to higher core loss and higher switching loss from the semiconductor devices. The experimentally observed switching waveforms indicate that there is substantial turning-off loss which is the principal contribution to the higher power loss associated with the converter switching at 100 kHz. Figure 10 shows the turning-off waveform of the drain currents of two of the three IRF330's and the common drain-to-source voltage for the converter switching at 100 kHz at an input voltage of 100 V. To obtain an estimate of the turning-off power loss, these waveforms were then approximated by piecewise-linear waveforms as shown in Fig. 11.

The energy loss per transistor associated with each turning-off process can be estimated by finding the time integral of the v_{DS} i_D product using Fig. 11, and this is found to be 1.38×10^{-4} joules. As a result, the total turning-off loss

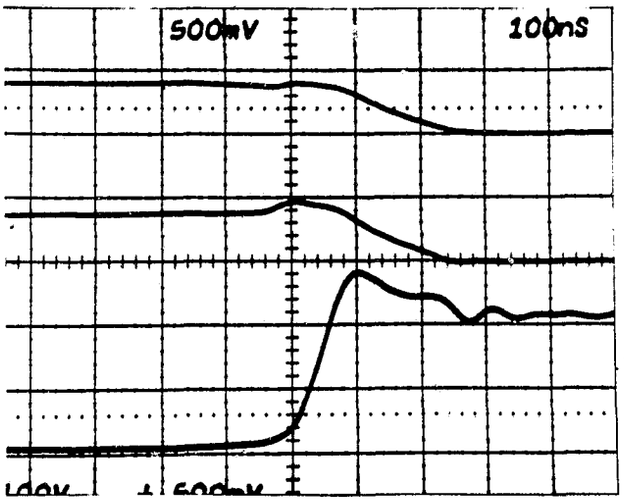


Fig. 10 Turning-off waveforms for two of the three paralleled IRF 330's. Vertical Scales are i_{D1}(upper), 5 A/div; i_{D2} (middle), 5 A/div; v_{DS}(lower), 100 V/div. Horiz. Scale is 100 ns/div.

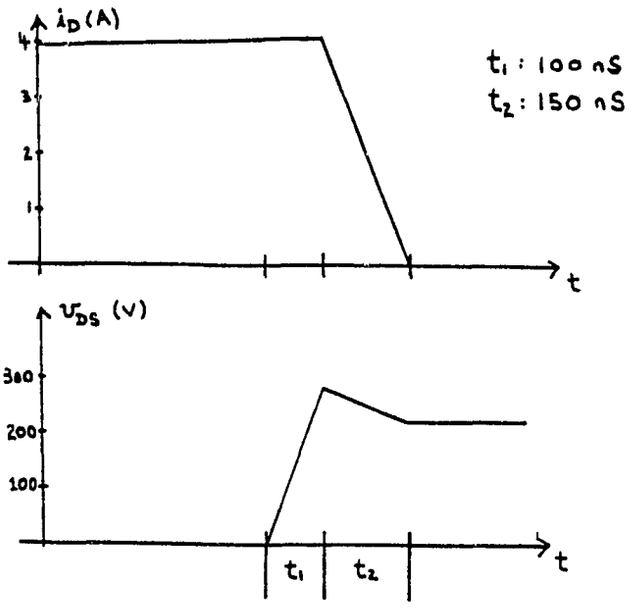


Fig. 11 Piecewise-linear approximation of the waveforms in Fig. 10 with only one drain current.

for three transistors switching at 20 kHz would be

$$1.38 \times 10^{-4} \times 20 \times 10^{3} \times 3 = 8.28 \text{ W}$$

The total turning-off loss for three transistors switching at 100 kHz would then be

$$1.38 \times 10^{-4} \times 100 \times 10^{3} \times 3 = 41.4 \text{ W}$$

Recall from Table 4 that the total power loss for the converter switching at 100 kHz at an input voltage of 100 V was 56 W, thus a turning-off loss of 41.4 W accounts for 74% of the total power loss in the circuit. To reduce this turning-off loss, an LC nondissipative snubber was designed [2] and implemented for the converter switching at 100 kHz. Figure 12 shows the circuit diagram of the converter with the nondissipative snubber.

The addition of the snubber to the circuit increases the mass of the 100-kHz converter by 0.0985 kg, so that the total mass of the magnetic reactor for switching at 100 kHz and the snubber ciruit is 0.217 kg, and compared to the mass of the magnetic reactor for switching at 20 kHz, it is 0.236 kg lighter. Table 5 shows the data obtained from the converter switching at 100 kHz with the snubber circuit.

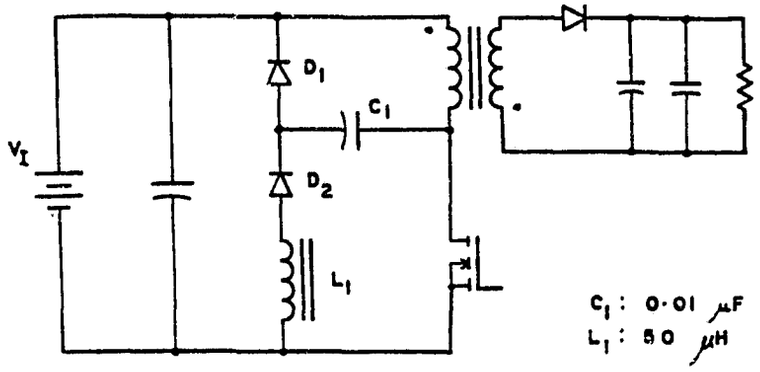


Fig. 12 Voltage-or-current step-up converter with an LC nondissipative snubber.

TABLE 5. Power Loss for the Converter Switching at 100 kHz with the Snubber Circuit.

Input Voltage (V)	Input Power (W)	Output Power (W)	Power Loss (W)	Efficiency (%)
60	235	200	35	85
80	232	200	32	86
100	238	200	38	84
120	242	200	42	83

With the nondissipative snubber, the efficiency of the converter switching at 100 kHz is definitely improved. Compared to the 20-kHz converter, the 100-kHz converter without the snubber circuit has a reduction of 0.335 kg in mass but an increase of 35 W to 41 W in power loss over the range of operating condition. Compared to the 20-kHz converter, the 100-kHz converter with the snubber circuit has a reduction of 0.236 kg in mass but an increase of 12 W to 21 W in power loss. In the next research period, a nondissipative snubber will be implemented in a higher-power converter such as a 1-kW unit to study the trade-off of power loss versus mass in a higher output power environment. At this moment, the mass of the snubber (0.0985 kg) is very close to the mass of the magnetic reactor designed for switching at 100 kHz (0.1185 kg), thus negating some of the mass reduction gained over the magnetic reactor designed for switching at 20 kHz. It is expected that at higher power levels the mass of the snubber circuit will decrease to a fraction of the mass of the energy-storage magnetic reactor, and the power loss versus mass trade-off ratio should improve substantially.

4.4 Bipolar Junction Power Transistor Investigations

4.4.1 Investigation of Motorola Power Darlingtons

During the current reporting period, three different bipolar junction power switching transistors were investigated as potential candidates for the controlled power switch of the converter. These transistors were the Motorola MJ10016 Power Darlington, the Motorola MJ10023 Power Darlington, and the International Rectifier HPT540 Power Transistor. Quantities sufficient for research purposes of each of these devices were made available free of charge to project personnel by the respective manufacturers.

As reported in the Fifth Semiannual Status Report (November 30, 1979), the Motorola MJ10016 Power Darlington had come to the attention of project personnel as a transistor with a large reverse bias safe operating area (RBSOA), fairly fast switching times (inductive crossover time 0.36 μsec typical), and the added advantage of reduced base-drive requirements. Almost simultaneously upon the arrival of the sample MJ10016's, Motorola announced a new type of power Darlington, the MJ10023. The MJ10023 is a single-chip version of the MJ10016, which was constructed with a separate silicon chip for each transistor in the Darlington configuration, the MJ10023 purportedly possessing faster switching times than the MJ10016, but with lowered current and voltage ratings. For reference, some major characteristics of the two devices are given in Table 6.

TABLE 6. Major Characteristics of the MJ10016 and MJ10023 Transistors

CHARACTERISTIC	MJ10016	MJ10023
$V_{CEO(SUS)}$	500 V	400 V
I_C - continuous	50 A	40 A
I_C - peak	75 A	60 A
Power Diss. at T_{CASE}= 25°C	250 W	250 W
Current Fall time	1.0 μs (max)	0.9 μs (max)
$h_{FE,MIN}$	50 at I_C = 10 A	50 at I_C = 10 A
Case Construction	modified TO3	modified TO3

Although the peak current and sustaining voltage ratings of these two devices would be sufficient to operate the 1-kilowatt converter under full-load conditions, the heat generation from switching, coupled with probable entry into reverse-bias second breakdown at high current levels, necessitates the paralleling of more than one device in order to achieve high output power from the converter. However, when two or more of either of the power Darlingtons were paralleled, severe oscillations in the collector and emitter currents of the paralleled transistors resulted. This oscillatory phenomenon is depicted by the smeared emitter current trace in Fig. 13, where two of the emitter currents of four paralleled MJ10016's are shown in the lower trace. Similar oscillations were found to occur during continuous conduction when two or more MJ10023's were paralleled.

Although the exact mechanism by which the oscillations are produced has not been found, the oscillatory phenomenon appears to be related to the rate of rise of base current, di_B/dt. The oscillations can be diminished in amplitude or even completely eliminated by decreasing di_B/dt at turn-on. Thus, in order to

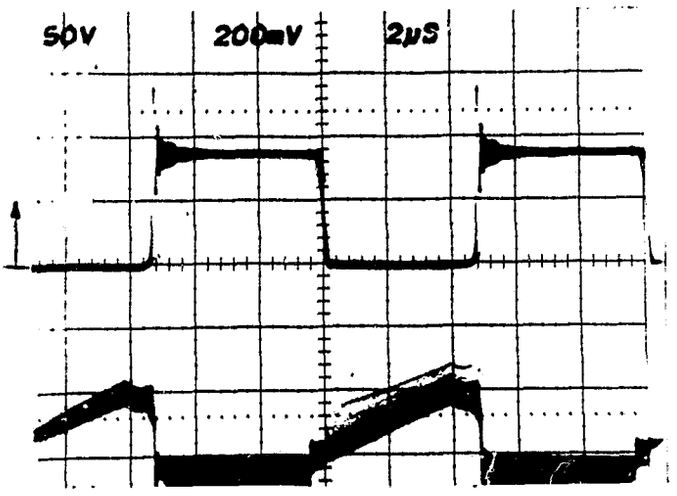


Fig. 13 Oscillatory phenomenon associated with paralleled Darlington transistors. Vertical: Collector-to-emitter voltage (upper), 100 V/div; Two emitter currents (lower), 2 A/div. with ac-coupled current probe.

operate the converter without collector current oscillations, one possibility tried was to add ferrite beads with inductances on the order of 1.0 μH to the emitter of each paralleled transistor. The purpose of the ferrite beads was simply to slow down the rate of rise of base current at turn-on. This technique completely eliminated the oscillations when up to four MJ10023's were paralleled, and limited the oscillations to a portion of the duty cycle range when four MJ10016's were paralleled.

4.4.2 Paralleling of Bipolar Power Transistors

The aforementioned paralleling of power Darlingtons was accomplished as described below. Because the on-resistance of BJT's possesses a negative temperature coefficient, extreme caution must be taken to avoid overheating any single bipolar transistor and creating the possibility of thermal runaway. The Motorola power Darlingtons were paralleled as follows: out of the sample of transistors available, the ones with the most closely matched DC characteristics were initially selected for paralleling. This was normally sufficient to insure good current sharing. The individual emitter currents (as opposed to collector currents due to the common collector connection of the water-cooled heat sink) were then examined with the converter running to determine if in fact one transistor was being stressed much more heavily than the others. Because the particular inductances of the ferrite beads varied slightly from bead to bead, any major imbalance in the emitter currents at this point during the switching intervals could usually be corrected by the selection of the proper bead. Thus, once a group of transistors had been matched with respect to their DC characteristics, the process of paralleling became a task of matching the proper transistor with the proper ferrite bead.

The converter was run using both a set of four paralleled MJ10016's and a set of four paralleled MJ10023's at output powers in excess of 500 W and with efficiencies in excess of 85%. Data for each run using the two types of power Darlingtons is shown in Table 7.

TABLE 7. Converter Operation with Motorola Darlingtons

Transistor Type:	MJ10016	MJ10023
V_I	90 V	71 V
I_I	7 A	9 A
P_I	630 W	640 W
V_O	255 V	172 V
I_O	2.1 A	3.2 A
P_O	540 W	545 W
Efficiency	86%	85.1 %

The data shown in Table 7 is not meant to represent identical operating conditions. The two runs were made on separate occasions and it is only coincidental that the output and input powers are similar. In addition, the MJ10023 does turn out to be a faster transistor, with correspondingly higher efficiencies than the MJ10016 when utilized under identical operating conditions.

Research involving the use of the Motorola Darlingtons has not been completed. The oscillatory phenomenon observed in conjunction with the use of these transistors in parallel is yet to be understood, and the best possible means to circumvent this oscillatory phenomenon has yet to be devised. In fact, research on these Motorola Darlingtons was only temporarily set aside due to the arrival of the International Rectifier HPT540, which at the time seemed a more promising candidate for the controlled power switch.

4.4.3 Alternative to Paralleling

While many types of objections might be raised to the current method of paralleling power transistors, one in particular stands out from the experimental viewpoint. Because the behavior of the switching characteristic may be changed by a slight change in the emitter lead inductance, the insertion of a current probe into the emitter lead of a power transistor will alter its current sharing in relation to an unprobed transistor. At higher output powers and correspondingly larger di/dt's, this may lead to failure of unprobed transistors. An alternative which depends far less on individual transistor characteristics involves alternately switching paralleled power transistors. For example, if two transistors are to be paralleled, and the energy storage elements have been designed for 100 kHz, each transistor is alternately switched at an effective rate of 50 kHz, as shown in Figure 14. This might become particularly useful when large capacity devices (such as the HPT540) are utilized which can handle large currents, but the 50% reduction in duty cycle for alternate switching will help reduce the possibility of thermal complications prevalent with BJT's switching at 100 kHz.

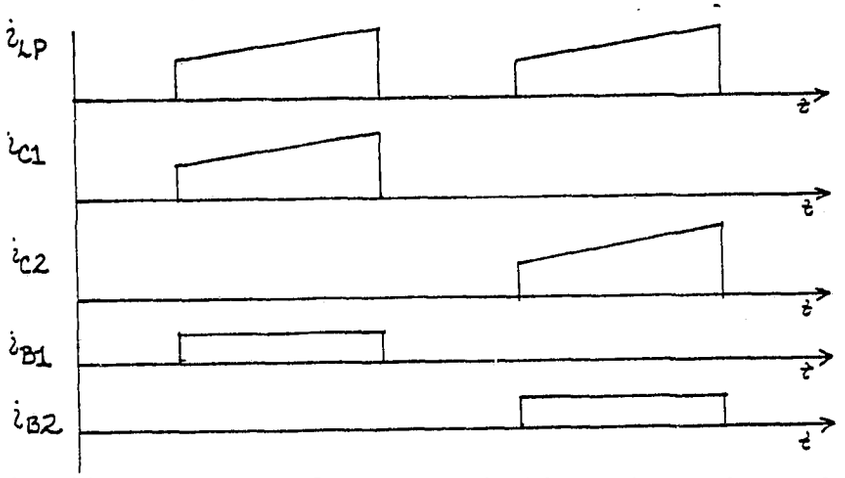


Fig. 14 Illustration of alternate switching scheme. i_{LP} refers to total primary inductor current composed of the sum of i_{C1} and i_{C2}, the collector currents of two paralleled transistors. Base currents i_{B1} and i_{B2} are shown to illustrate the necessary drive conditions.

4.4.4 The International Rectifier HPT540

In early March, International Rectifier, Inc. announced the production of new high-power switching transistors, the HPT540 and HPT545. The research project here at Duke University was provided with two samples of the HPT540, courtesy of International Rectifier. For reference, some major characteristics of this device are shown in Table 8.

TABLE 8. Major Characteristics of the HPT540

$V_{CEO(SUS)}$	400 V
I_C - continuous	50 V
I_C - peak	75 A
Power Diss. at T_{CASE} = 25°	300 W
Current Fall time	$\leq$ 0.2 μs @ I_C = 50 A
$h_{FE,MIN}$	8 @ I_C = 50 A
Case Construction	Similar to JEDEC TO-208AD (TO-83)

Although the current and voltage ratings of this device are identical to those of the MJ10016, the HPT540 posesses superior switching speeds, and the stud-type case affords lower thermal resistance both junction-to-case and case-to-sink.

4.4.5 RC Snubbers for use with Power BJT's

One problem that still restricts the use of power BJT's in the present 1-kilowatt converter is the presence of reverse-bias second breakdown. The paralleling of devices avoids second breakdown by reducing the peak current flowing through each individual transistor, but this is wasteful of available current carrying ability. One area which has received some attention during the current reporting period has been the development of suitable turn-off snubber circuitry for use with bipolar transistors. In particular, work with

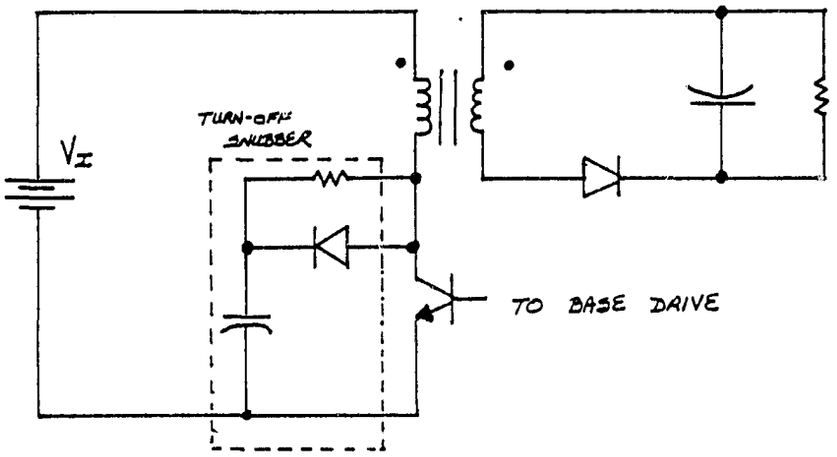


Fig. 15 Illustration of simple dissipative turn-off snubber circuit (entire converter shown for clarity) originally used in conjunction with the International Rectifier HPT540.

dissipative RC snubbers has been started in an effort to shape the turn-off trajectory to stay out of the high-voltage high-current portion of the v_{CE}-i_C plane where repetitive switching may bring on reverse-bias second breakdown. A point to be noted is that manufacturers normally specify both forward and reverse safe operating areas under single-pulse testing. Thus, there is usually no good way of knowing what the secondary breakdown limits will be under 100 kHz repetitive switching unless the device is exercised to destruction.

The initial snubber circuit tried was the simple RC snubber shown in Fig. 15 used in conjunction with the HPT540. This circuit was found to sufficiently shape the turn-off trajectory, but it has at least one distinct disadvantage. Because the energy stored in the snubber capacitor during the off-time of the power switch is routed through the collector at turn-on, the turn-on current stress is increased in the power switch. The circuit shown in Fig. 16 contains an alternative to this type of RC snubber. The entire base drive, converter, and RC snubber have been shown for reference purposes. The operation of this actively-switched snubber circuit is as follows: Transistors Q1 and Q2 are turned on and

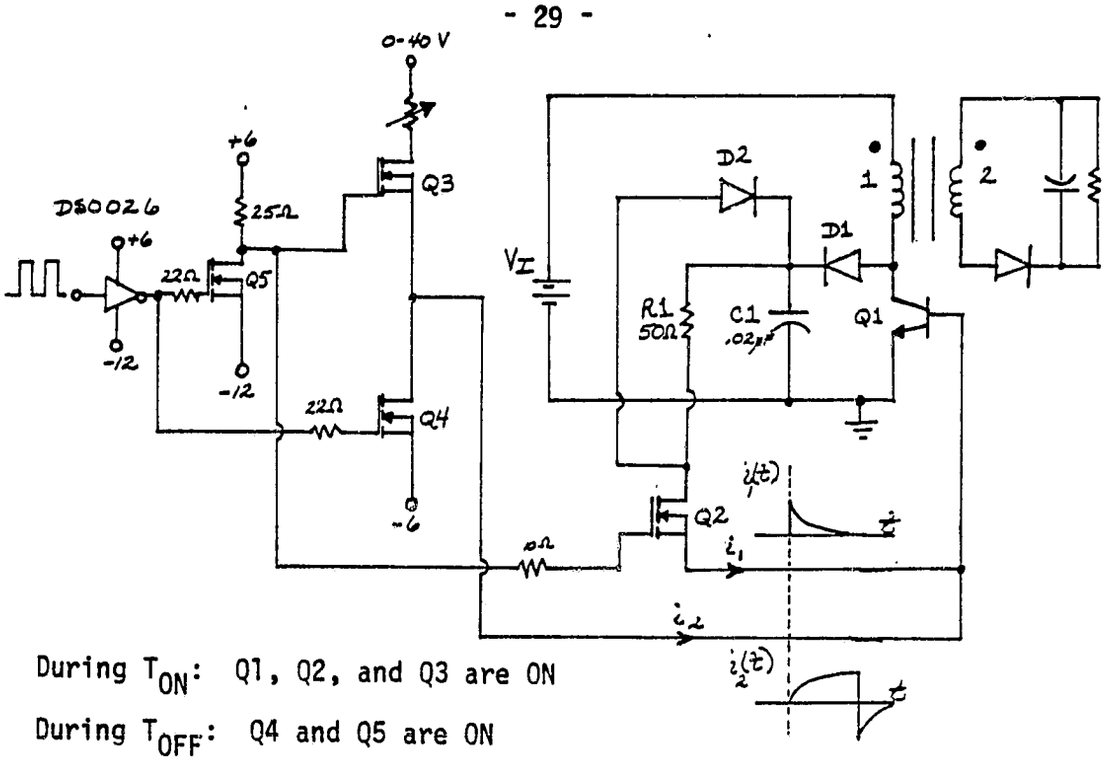
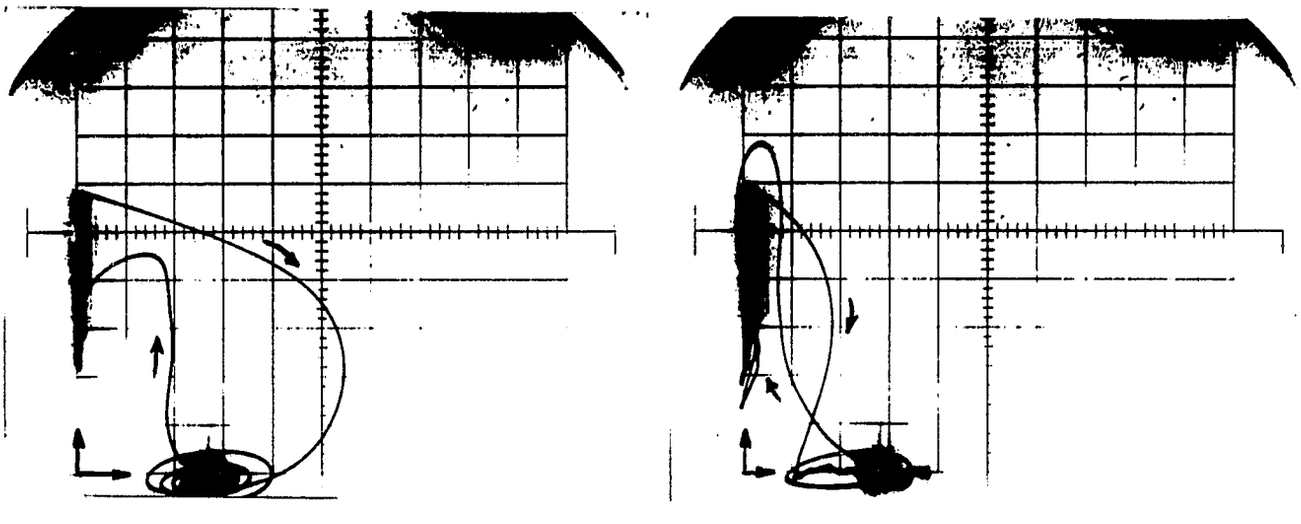


Fig. 16 Circuit diagram for actively switched snubber, base drive, and converter.

off at the same time. As with the simple RC snubber, capacitor C1, through diode D1, helps limit the rate of rise of collector-emitter voltage at turn-off. In addition, diode D2 was added to insure that the drain-to-source voltage of Q2 is clamped to the capacitor voltage, V_{C1}. During the off-time, C1 is essentially charged to the input voltage plus the output voltage reflected through the transformer turn ratio. When Q1 and Q2 are turned on, C1 is discharged through R1, Q2, and the base-emitter junction of Q1. This circuit holds two distinct advantages over the simple RC snubber shown in Fig. 15. First of all, the energy stored in the snubber capacitor is not routed to the collector of the power switch. This avoids the increased current stress at turn-on mentioned earlier. Secondly, neglecting stray inductances, the base current initially supplied at



(a) (b)

Fig. 17 Collector current (vertical) vs. collector-to-emitter voltage (horizontal) switching trajectories for converter operation both with and without the actively-switched snubber at P_O = 300W. Scale factors are collector current, 2 A/div, and collector-to-emitter voltage, 50 V/div. (a) operation without snubber (b) operation with actively-switched snubber.

turn-on is $V_{C1}/R1$, thus rapidly turning on the transistor. Thus, the need for a separate high-voltage high-resistance base drive to provide a current source at turn-on is eliminated by utilizing the stored energy of the snubber. In essence, the actively-switched snubber improves the turn-on trajectory as well as shaping the turn-off trajectory, as shown in Figs. 17(a) and (b) which show switching trajectories under approximately identical converter operating conditions for the HPT540 switching both with and without the actively-switched snubber. An invention disclosure is currently being prepared for submission to NASA concerning the possible patentability of this actively-switched snubber.

4.4.6 High Power Operation with the HPT540

Combining the actively-switched snubber with many of the techniques developed for high power operation using power field-effect transistors and documented in the Fifth Semiannual Status Report (November 30, 1979), an output power of nearly one kilowatt was obtained using one HPT540 as the main power switch. Specifically, the techniques employed include the use of a one-to-two transformer turn ratio, a series pair of 600-V diodes, and a water-cooled heat sink specifically designed to accomodate up to two HPT540 transistors. With this combination, the BJT-switched converter was operated at approximately 930 W output for 12 minutes. Transistor collector waveforms for full-cycle switching, turn-on, turn-off, and i_C vs v_{CE} are shown in Figs. 18(a) through (d), respectively. Data for this run is shown below in Table 9.

TABLE 9. Data for 1 Kilowatt Converter Utilizing HPT540 and Actively Switched Snubber.

V_I	69 V	V_O	202 V
I_I	17.7 A	I_O	4.6 A
P_I	1220 W	P_O	930 W
Duty Ratio	.64	Load	46.9 Ω

Efficiency 76%

Note from Table 9 that 290 watts is being lost, which is believed to be primarily associated with the transistor and snubber circuitry. The snubber will dissipate $1/2\ CV^2f$ watts, where C = C1, V = V_{C1}, and f is the switching frequency. For V_{C1} = 170 V and C = 0.02 μF, as was the case, the snubber accounts for 29 watts of the total loss. Therefore, allowing for losses in the magnetic core and in the diode, a conservative estimate for the power loss in the transistor is in the range of 230 to 250 watts. However, at T_{CASE} = 62.5°C, the specified power

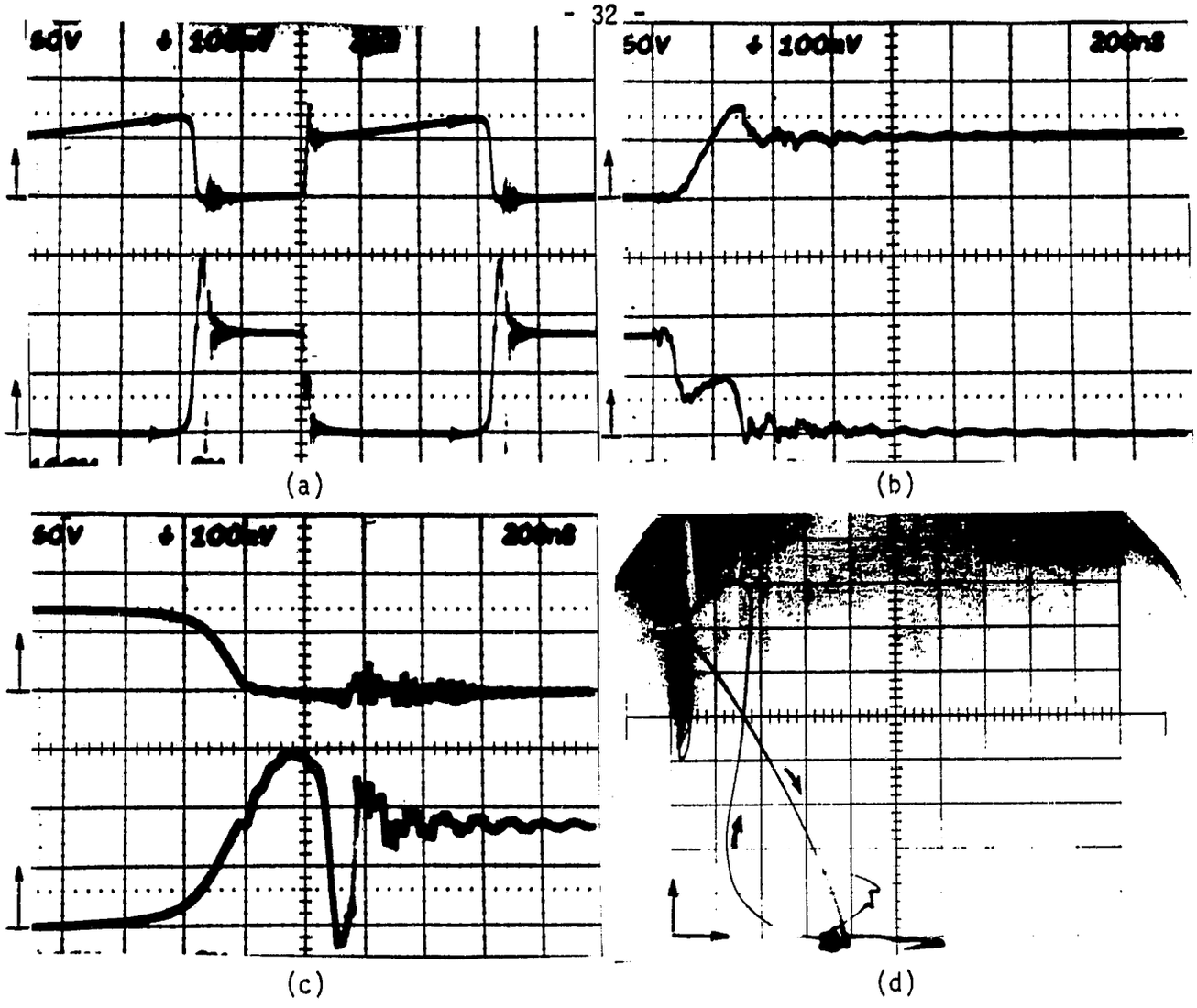


Fig. 18 Collector current i_C and collector-to-emiter voltage v_{CE} waveforms for converter operation with HPT540 at P_O=930 W. (a) Full-cycle switching with vertical scales: i_C (upper), 20 A/div; v_{CE}(lower), 100 V/div. Horizontal scale is 2.0 μs/div. (b) and (c) Turning-on and turning-off intervals, respectively, with same waveforms and vertical scales as (a), but with horizontal scale 200 ns/div. (d) i_C vs. v_{CE} with i_C (vertical), 4 A/div; v_{CE} (horizontal), 50 V/div.

dissipation capability of the HPT540 drops to 225 W. The actual case temperature was not known exactly during the operation of the converter, but it was estimated to be at least 60°C. The point here is that operation under the conditions shown in Table 9 was either at or slightly above the limits specified for the HPT540 by the manufacturer, and thus higher operating powers or very long operation times were simply not attempted.

4.5 Instrumentation and Measurement System

4.5.1 Test benches and ground plane

The November 30, 1979 Semiannual Status Report discussed in some detail the need for establishing a well-defined ground plane for all converter circuit measurements. It also described the techniques employed in constructing such a ground. During the present reporting period the grounding system has been used extensively and has proved to be extremely effective in eliminating stray coupling effects up to the highest converter power levels so far attained.

In order to avoid the not insignificant delays in changing the experimental setup from measurements using a converter with power FET's as the active switching devices to one with BJT's, which require quite different base drives and a different heat sink arrangement, a second test-bench was fabricated. In this way, one converter can be worked on and readied while data is being taken on the other. The basic system and approach to grounding remain the same although certain refinements have been incorporated. The two test stations have a common ground and measurements may be made at either station under control of the PDP-11/03 computer.

4.5.2 Computer-aided measurement and analysis of converter operating data.

The instrumentation for the high-power converters has been designed from the outset to incorporate features to aid in data recording and reduction, and to enhance the safety of the personnel. Programmable computer control was selected for the instrumentation system to provide for the greatest flexibility. For interconnections, the IEEE-488 instrument bus standard was chosen. Selection of appropriate instruments and connection to a computer then followed.

The original plan called for integration of the instrumentation system with the Digital Equipment Corporation (DEC) PDP-11/45 computer located in the

Department of Electrical Engineering Minicomputer Laboratory. Shortly afterward, a DEC LSI-11 microcomputer became available on loan to the research project and the instrumentation plan was shifted to this computer system which could be located directly in the research laboratory. A good deal of experience with the use of the IEEE 488 instrument bus was gained with this setup using the IEEE 488 bus-compatible instruments acquired for this work. The present instrumentation system is centered around a DEC PDP-11/03 laboratory computer system which was contributed by the Digital Equipment Corporation for use in the program of instruction and research in power electronics at Duke University. The computer has other ports for connecting the Biomation 8100 digitizing data recorder and ancillary computer equipment such as a line printer and graphics terminal.

The philosophy of the instrumentation design has not changed, but the implementation is evolutionary with changes and refinements. Two Hewlett-Packard 3438-A digital multimeters, one replacing an HP 3437-A system voltmeter, are used with computer-controlled relays so that one multimeter measures alternately the input voltage and current while the other measures the output voltage and current. Current readings are taken across 50-mV ammeter shunts while voltage measurements are made directly. The auto-ranging feature of the digital multimeters is employed. The computer program reads each meter, records that reading or the average of a selected number of consecutive readings, and then sets the relays for the next measurement. The program computes input power, output power, efficiency, and power dissipated in the converter. Raw and computed data may be viewed on a video display, preserved on a hard copy by printer, and stored on a magnetic computer storage disk.

One of the major challenges in the instrumentation has been the reduction of electromagnetic interference (EMI) to a level where digital instrument operation and proper IEEE bus data transmission are unaffected. The voltage

and current switching waveforms presented in the section on converter operation illustrate the high rates of change in voltage and current during the turning-on and turning-off intervals which account for a considerable amount of power extending through the spectrum up to several hundred megahertz.

At the outset, the EMI from the converter caused malfunctioning of the digital meters at power levels of one hundred to two hundred watts. At levels a little over two hundred watts, the EMI affected the signals on the IEEE bus, causing the relay unit to malfunction and occasionally causing failure of the computer. The computer malfunction was generally one of two kinds, a false interrupt, or an invalid operation address. The computer malfunctions seemed to result from EMI entering via the IEEE bus. While there is a reasonable chance that radiated EMI may be significant, the direct-wire connections from converter to digital meters to IEEE-bus were viewed as the prime source of interference difficulties.

As described in connection with the discussion of Figs. 30 and 31 of the November 30, 1979 Semiannual Status Report, the signal lines first were singly filtered with a balanced pi-section low-pass LC filter housed in a shielded and well-grounded box. With this arrangement, satisfactory operation to nearly four hundred watts was obtained, but malfunctions occured above this level. Cascade filtering was then employed with two pi sections in separate housings, one close to the converter, the other near the instrumentation. The signal lines were changed from twisted pair to shielded pair and the grounding system was enlarged. The present measurement system has operated satisfactorily at power levels to two kilowatts with no difficulties having been encountered. It appears that this filtering technique will control the EMI, allowing proper instrument functioning at 5 and 10 kilowatts. The system will be carefully monitored, however, as it is used with higher-power converters.

In addition to the recording of data and the controlling of certain converter functions by the computer through the IEEE 488 bus system, the PDP-11/03 computer also is being used in conjunction with the Biomation 8100 digital transient recorder. Two major objectives of this work are: (1) to assist in the identification and quantification of losses throughout the converter under investigation, and (2) to record wide-band waveforms in a form which will permit a variety of analyses to be made on converter performance. An especially useful capability of such a facility, which has not yet been implemented, would be the analysis of waveforms acquired just before a converter failure by using the Biomation pretrigger mode of waveform acquisition. The basic system is now in regular use using an interactive program. Some of the features of the system are illustrated in the remainder of this section.

Waveforms of drain current and drain-to-source voltage in the 2.5-kW converter module using HEXFET transistors are used to illustrate the use of the program. The program is constructed to produce documentation on the line printer during the progress of the program to simplify laboratory record keeping. The output shown in Fig. 19 occurs after the program user has entered interactively the Biomation 8100 setup data and two digitized waveforms have been retrieved.

In this example, the waveforms correspond to drain-to-source voltage and drain current. Run and waveform captions, date and time, sample interval, probe attenuation or current sensitivity, input range, offset and type of coupling are entered by the user and are stored in memory. If the user chooses to save the waveform permanently, the setup data also are saved on disk with the waveform samples.

The program output of Fig. 20 was obtained from the array print feature. In this example, the first 500 nanoseconds of the waveforms stored in arrays 1 and 2 are printed along with the time corresponding to the sample interval set up for the

```
BIOMATION RUN CAPTION:  8-HEXFET CONV. 2KW RUN 3


DATE: 04-JUN-80
TIME:09:43:13


SAMPLE INTERVAL:  1.000E-08 SEC.
CHANNEL A:VDS
PROBE ATTEN. RATIO= 100
INPUT RANGE=  2.00 V
OFFSET = -0.80
DC-COUPLED

BIOMATION RUN CAPTION:  8-HEXFET CONV. 2KW RUN 3


DATE: 04-JUN-80
TIME:09:44:00


SAMPLE INTERVAL:  1.000E-08 SEC.
CHANNEL B:ID
CURRENT PROBE SENS. =  40 A/V
INPUT RANGE =  2.00 V
OFFSET =  0.00
DC-COUPLED
```

Fig. 19 Output from the program BIOV1 documenting the retrieval of waveforms of drain-to-source voltage and drain current with identifying names VDS and ID, respectively.

Biomation 8100. The print feature is useful for getting the offset value to be removed from an ac-coupled signal such as obtained from a current probe.

To obtain the value of offset introduced into the drain-to-source voltage by the Biomation 8100, a calibration run is made with the voltage probe short-circuited. After removing the offsets introduced by ac coupling and by the Biomation 8100, the waveforms of current and voltage may be multiplied to obtain an estimate of the instantaneous power dissipated in the transistors. The waveform display feature of the program is illustrated in Fig. 21 using an oscilloscope-type grid for the plot background.

SAMPLE INTERVAL = 1.000E-08 SECONDS.
START TIME = 0.000E-01 SECONDS.
STOP TIME = 5.000E-07 SECONDS.
TOTAL RECORD LENGTH = 1.001E-05 SECONDS.

TIME	DATA(1,J)	DATA(2,J)
0.0000E-01	-3.9062E+01	-3.9375E+01
1.0000E-08	-3.9062E+01	-3.9375E+01
2.0000E-08	-3.9062E+01	-3.9375E+01
3.0000E-08	-3.9062E+01	-3.8750E+01
4.0000E-08	-3.7500E+01	-3.8750E+01
5.0000E-08	-3.5937E+01	-3.8750E+01
6.0000E-08	-3.4375E+01	-3.8750E+01
7.0000E-08	-3.2812E+01	-3.8750E+01
8.0000E-08	-2.8125E+01	-3.8750E+01
9.0000E-08	-2.6562E+01	-3.8750E+01
1.0000E-07	-2.5000E+01	-3.8750E+01
1.1000E-07	-2.5000E+01	-3.8750E+01
1.2000E-07	-2.5000E+01	-3.8750E+01
1.3000E-07	-2.5000E+01	-3.8750E+01
1.4000E-07	-2.6562E+01	-3.8750E+01
1.5000E-07	-2.8125E+01	-3.9375E+01
1.6000E-07	-2.9687E+01	-3.9375E+01
1.7000E-07	-3.1250E+01	-3.9375E+01
1.8000E-07	-3.4375E+01	-3.9375E+01
1.9000E-07	-3.5937E+01	-3.9375E+01
2.0000E-07	-3.7500E+01	-3.9375E+01
2.1000E-07	-3.9062E+01	-3.9375E+01
2.2000E-07	-3.9062E+01	-3.8750E+01
2.3000E-07	-4.3750E+01	-3.8750E+01
2.4000E-07	-5.1562E+01	-3.8125E+01
2.5000E-07	-6.2500E+01	-3.7500E+01
2.6000E-07	-7.5000E+01	-3.6250E+01
2.7000E-07	-8.7500E+01	-3.5625E+01
2.8000E-07	-1.0000E+02	-3.5000E+01
2.9000E-07	-1.0781E+02	-3.3125E+01
3.0000E-07	-1.1406E+02	-3.0625E+01
3.1000E-07	-1.2500E+02	-3.0000E+01
3.2000E-07	-1.3125E+02	-2.8125E+01
3.3000E-07	-1.3750E+02	-2.5625E+01
3.4000E-07	-1.3906E+02	-2.3125E+01
3.5000E-07	-1.4219E+02	-2.2500E+01
3.6000E-07	-1.4375E+02	-2.0000E+01
3.7000E-07	-1.4531E+02	-1.8125E+01
3.8000E-07	-1.4688E+02	-1.5625E+01
3.9000E-07	-1.4688E+02	-1.3125E+01
4.0000E-07	-1.4844E+02	-1.3125E+01
4.1000E-07	-1.5000E+02	-1.0000E+01
4.2000E-07	-1.5000E+02	-8.1250E+00
4.3000E-07	-1.5156E+02	-5.6250E+00
4.4000E-07	-1.5156E+02	-5.0000E+00
4.5000E-07	-1.5156E+02	-3.1250E+00
4.6000E-07	-1.5156E+02	-6.2500E-01
4.7000E-07	-1.5313E+02	1.8750E+00
4.8000E-07	-1.5313E+02	4.3750E+00
4.9000E-07	-1.5313E+02	5.0000E+00
5.0000E-07	-1.5469E+02	7.5000E+00

v_{DS} = DATA(1,J)

i_D = DATA(2,J)

Fig. 20 Output from the program BIOV1 using the array print option to obtain the values of the raw data obtained from the Biomation 8100 over the first 500 nanoseconds.

The program permits the user to choose one of six programmed oscilloscope grids or to construct a custom grid. The waveforms displayed are the drain-to-source voltage, the total drain current and the product of the two waveforms for an eight-HEXFET converter run with an output power of approximately 2 kW in Fig. 21. The calibration data which documents the display are shown in Fig. 22.

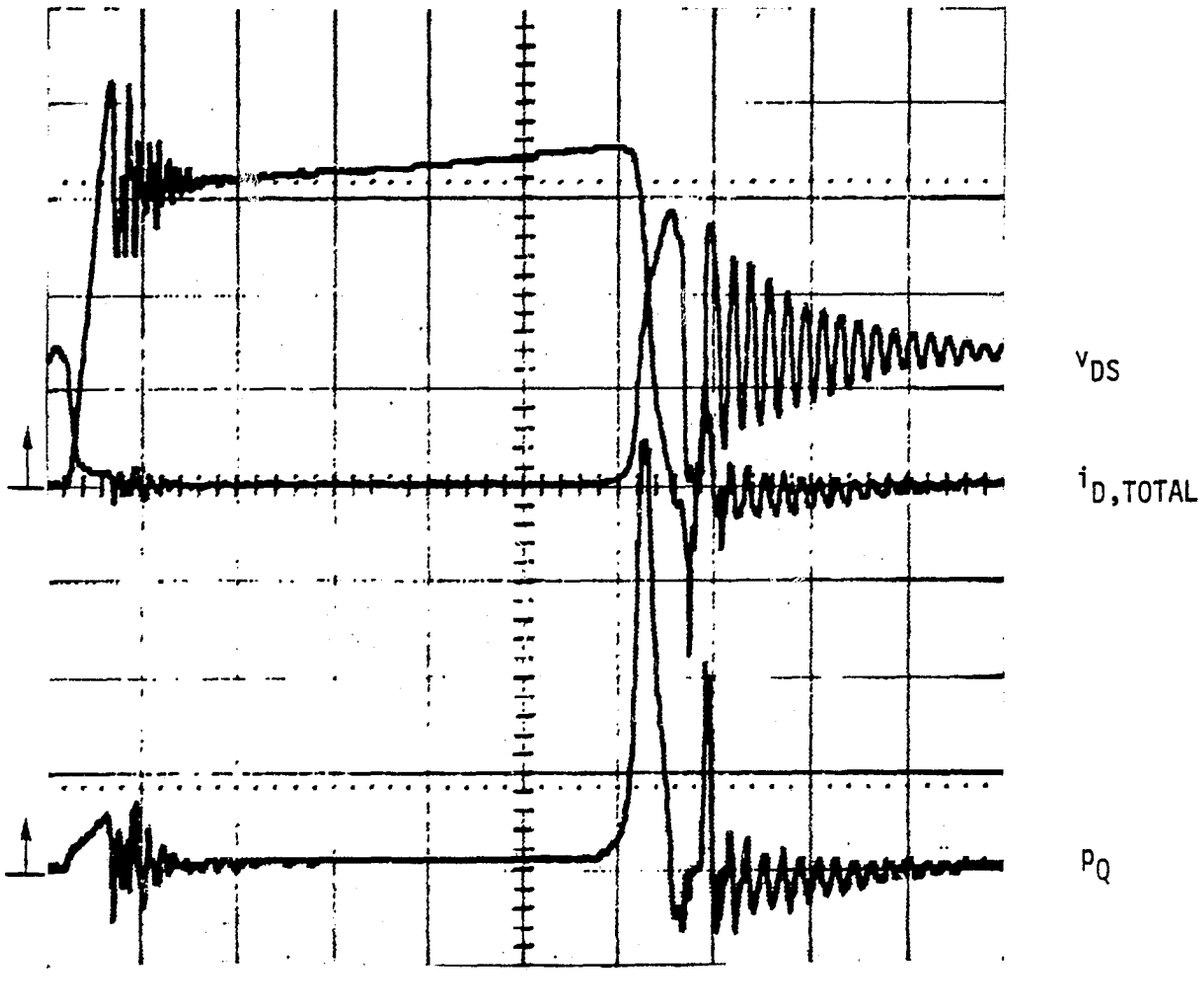


Fig. 21 Waveforms of total drain current i_D, drain-to-source voltage v_{DS} and transistor power loss p_Q plotted by the program BIOV1. Vertical deflection factors: i_D, total, 20 A/div.; v_{DS}, 100 V/div.; p_Q, 2000 W/div. Horizontal time scale: 1 microsecond/div.

```
DATE: 04-JUN-80
TIME: 16:00:14


SAMPLE INTERVAL=  1.000E-08 SEC.
START TIME=  0.000E-01 SEC.
STOP TIME=  1.000E-05 SEC.
TOTAL RECORD LENGTH=  1.000E-05 SEC.
FOR Y-AXIS VARIABLE NO. 1
VERTICAL DEFLECTION FACTOR=  1.000E+02 UNITS/MAJ. DIV.
VERTICAL OFFSET=  0.000E-01 UNITS



DATE: 04-JUN-80
TIME: 16:00:14


SAMPLE INTERVAL=  1.000E-08 SEC.
START TIME=  0.000E-01 SEC.
STOP TIME=  1.000E-05 SEC.
TOTAL RECORD LENGTH=  1.000E-05 SEC.
FOR Y-AXIS VARIABLE NO. 2
VERTICAL DEFLECTION FACTOR=  2.000E+01 UNITS/MAJ. DIV.
VERTICAL OFFSET=  0.000E-01 UNITS



DATE: 04-JUN-80
TIME: 16:00:14


SAMPLE INTERVAL=  1.000E-08 SEC.
START TIME=  0.000E-01 SEC.
STOP TIME=  1.000E-05 SEC.
TOTAL RECORD LENGTH=  1.000E-05 SEC.
FOR Y-AXIS VARIABLE NO. 3
VERTICAL DEFLECTION FACTOR=  2.000E+03 UNITS/MAJ. DIV.
VERTICAL OFFSET= -8.000E+03 UNITS
```

Fig. 22 Output from the program BIOV1 which documents the waveforms plotted by the program in Fig. 21.

A final illustration of some of the program capabilities makes use of the computed averages feature. The user enters the array on which the averaging procedures are to be performed and is queried on the method of entering the start and stop times over which the averaging is to take place. The start and stop times may be entered at the keyboard or by means of a lighted cursor

on the graphic terminal. If the waveform to be processed has been displayed, the cursor method provides a convenient means of choosing the start and stop times for separating the various time intervals of interest during a switching cycle. Performing the averaging on the instantaneous power data stored in array 3 and displayed as the bottom waveform in the previous illustration, estimates of the average power over the turning-on, on-time, and turning-off intervals are obtained by noting the value of the average of the sum of the samples for these three cases as shown in Fig. 23.

The sources of error in the data processing procedures in the program are essentially the same as those in the use of regular instruments. The resolution of the Biomation 8100 is 1 part in 256. To begin to approach this resolution in practice requires adjustment of the input range (attenuation) and offset of the Biomation 8100 to obtain the maximum excursion over the digitizer range. Use of the shorted-voltage-probe data obtained immediately before or after taking the drain-to-source voltage provides an excellent estimate of the offset to be removed from that waveform. To obtain the offset for an ac-coupled current probe, one must choose carefully a point on the current waveform known from circuit behavior to be zero. Using the array print feature of the program, that section of the waveform may be printed out to obtain the value of the Biomation 8100 data at the chosen point which is then subtracted from the entire array as the offset. As an aside, whenever a current probe is operated near its maximum rated value, the waveform may display a droop or sag, making it impossible to obtain a good estimate of the instantaneous power product. The current waveform should be inspected carefully and another probe with higher current rating or a wide-bandwidth current shunt should be used if the droop effect is noted. To obtain the current waveform in Figure 21, the combination of a 40:1 current trans-

```
SUMS AND AVERAGES FOR ARRAY DATA (3,J)

START TIME =  1.333E-08 SEC,
STOP TIME=  6.800E-07 SEC.
AVERAGING INTERVAL =  1.000E-05 SEC.
NO. OF SAMPLES USED = 1001
MINIMUM VALUE OF N SAMPLES =  0.0000E-01
MAXIMUM VALUE OF N SAMPLES =  1.1424E+03
SUM OF N SAMPLES =  3.1866E+04
AVERAGE OF N SAMPLES =  3.1834E+01                    P_Q, turning-on loss
SUM OF SQUARES OF N SAMPLES =  2.4499E+07
AVERAGE OF SQUARES OF N SAMPLES = 2.4475E+04
TOTAL RMS OVER N SAMPLES =  1.5644E+02
SUM OF SQUARES OF AC COMPONENT OVER N SAMPLES = 2.2538E+07
AVERAGE OF SQUARES OF AC COMPONENT OVER N SAMPLES = 2.2516E+04
RMS OF AC COMPONENT OVER N SAMPLES =  1.5005E+02

SUMS AND AVERAGES FOR ARRAY DATA (3,J)

START TIME =  6.800E-07 SEC,
STOP TIME=  5.813E-06 SEC.
AVERAGING INTERVAL =  1.000E-05 SEC.
NO. OF SAMPLES USED = 1001
MINIMUM VALUE OF N SAMPLES = -1.0207E+03
MAXIMUM VALUE OF N SAMPLES =  1.3963E+03
SUM OF N SAMPLES =  9.8039E+04
AVERAGE OF N SAMPLES =  9.7941E+01                    P_Q, on-time loss
SUM OF SQUARES OF N SAMPLES =  3.6238E+07
AVERAGE OF SQUARES OF N SAMPLES = 3.6202E+04
TOTAL RMS OVER N SAMPLES =  1.9027E+02
SUM OF SQUARES OF AC COMPONENT OVER N SAMPLES = 2.1964E+07
AVERAGE OF SQUARES OF AC COMPONENT OVER N SAMPLES = 2.1943E+04
RMS OF AC COMPONENT OVER N SAMPLES =  1.4813E+02

SUMS AND AVERAGES FOR ARRAY DATA (3,J)

START TIME =  5.813E-06 SEC,
STOP TIME=  6.547E-06 SEC.
AVERAGING INTERVAL =  1.000E-05 SEC.
NO. OF SAMPLES USED = 1001
MINIMUM VALUE OF N SAMPLES =  2.2053E+02
MAXIMUM VALUE OF N SAMPLES =  8.9491E+03
SUM OF N SAMPLES =  2.2878E+05
AVERAGE OF N SAMPLES =  2.2856E+02                    P_Q, turning-off loss
SUM OF SQUARES OF N SAMPLES =  1.3396E+09
AVERAGE OF SQUARES OF N SAMPLES = 1.3382E+06
TOTAL RMS OVER N SAMPLES =  1.1568E+03
SUM OF SQUARES OF AC COMPONENT OVER N SAMPLES = 1.2388E+09
AVERAGE OF SQUARES OF AC COMPONENT OVER N SAMPLES = 1.2376E+06
RMS OF AC COMPONENT OVER N SAMPLES =  1.1125E+03
```

Fig. 23 Output of the program BIOV1 illustrating use of the computed averages option to obtain an estimate of the transistor loss during the turning-on, on-time and turning-off intervals.

former constructed using a powder permalloy core and a 10-A current probe was used. The sag effect is illustrated in the off-time portion of the waveform. Upon receipt of a 100-A current probe currently on order, this measurement problem should be eliminated.

5. FUTURE WORK

During the next reporting period, several approaches will be taken towards the development of a light-weight dc-to-dc converter operating at an output power of 5.0 kilowatts and with a conversion frequency of 100 kilohertz. First and foremost, the present 2.5-kilowatt design utilizing power HEXFET's will be upgraded to the point where full output power can be reliably obtained over a wide range of input voltage. In parallel with this effort, a second 2.5-kilowatt unit will be constructed, and the task of connecting the two converters for series output will be undertaken. An important portion of this last effort will lie in the design of a suitable drive scheme for the two halves of the 5.0-kilowatt module. In addition, because the bipolar junction transistor remains a viable candidate for the controlled power switch in a high-frequency high-power dc-to-dc converter, a converter employing BJT's will be constructed with an output power of 2.5 kilowatts as the target goal, allowing comparisons for operation with both BJT's and FET's at that power level.

Work will continue on a study of the interrelationships between switching frequency, mass, and efficiency, particularly at higher output power levels. The effects of snubber circuitry at these increased power levels will also be included in this comparison. Attention will be given to the optimization of the energy-storage reactor with respect to mass and efficiency, and the use of ferrites at 100 kilohertz will be examined. Finally, with the computer-controlled instrumentation

system on-line and fully operational at high power levels, the waveform recording portion of this system and the analysis software will be used to investigate the feasibility of determining power losses in the various components of the test converters.

6. REFERENCES

[1] T.H. Sloane, H.A. Owen, Jr., and T.G. Wilson "Switching Transients in High-Frequency High Power Converters Using Power MOSFET's," PESC-79 Record, IEEE Power Electronics Specialists Conference - 1979, IEEE Publication 79CH1461-3 AES, pp. 244-255 (June 1979).

[2] W. Shaughnessy, "Modelling and Design of Non-Dissipative LC Snubber Networks," Proceedings of the Seventh National Solid-State Power Conversion Conference, Powercon 7, March 1980.