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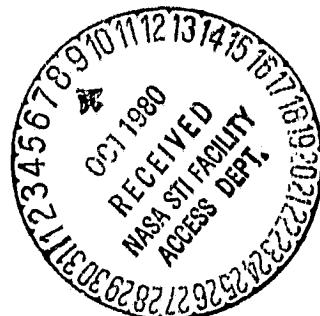
TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION

FINAL REPORT

A MICROPROCESSOR-BASED CARDIOTACHOMETER

Prepared for the NASA Johnson Space Center
Cardiovascular Research Laboratory

October 31, 1979



Contract NAS9-14880
Project 0100-20

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TABLE OF CONTENTS

	<u>Page</u>
I. INTRODUCTION	1
II. GENERAL DESCRIPTION	3
III. HARDWARE DESCRIPTION	5
IV. SOFTWARE DESCRIPTION	9
Heart Rate Monitor Routine	9
D/A Setup Routine	11
D/A Ramp Routine	11
V. APPENDIX A - FLOW CHARTS	13
Start Routine	14
Input Routine	15
Count Routine	16
Check Routine	17
Output Routine	18
Err1 (Underrange) Routine	19
Err2 (Overrange) Routine	19
D/A Setup Routine	20
D/A Ramp Routine	21
Input 2 Routine	22
VI. APPENDIX B - ASSEMBLY PROGRAM LISTING	23
VII. APPENDIX C - PROGRAM EXECUTION TIMES	30
VIII. APPENDIX D - WIRE WRAP LISTS	32
IX. APPENDIX E - COMPONENT LOCATION LAYOUT DRAWINGS	40
X. APPENDIX F - CIRCUIT DIAGRAMS	45
XI. APPENDIX G - SAMPLE OUTPUT	58

INTRODUCTION

In the early development of the Cardiopulmonary Data Acquisition System (CDAS) for the NASA/JSC Cardiovascular Laboratory, one of the main requirements was a device which would provide reliable measurements of instantaneous heart rate during treadmill and ergometer stress testing. Cardiotachometers which were commercially available generally were not designed to handle the rather large amount of noise, baseline wandering, and amplitude changes that are frequently seen in the electrocardiogram (ECG) during exercise testing. In addition, most commercial units were not reliable enough for research use and generally would be difficult to interface with the existing laboratory instrumentation and computers. As a result, the development of a completely new cardiotachometer was undertaken so that highly accurate and reliable measurements could be made of the heart rate of test subjects.

In summary, the principle requirements for the new cardiotachometer were as follows:

- (1) Reliable heart rate measurements during either rest or exercise stress testing.
- (2) Accurate heart rate measurements over the range of 30 to 250 beats/minute.
- (3) Analog output for interfacing with an FM tape recorder and a micro-computer analog to digital (A/D) converter.
- (4) Instantaneous (beat to beat) updates on the system output were also desirable so that occasional noise artifacts or ectopic beats could be more easily identified except that occasional missed beats caused by switching ECG leads should not cause a change in the output.

The first unit developed for this task utilized discrete transistors and small and medium-scale integration integrated circuits (IC's) for all of the logic and digital-to-analog (D/A) conversion required. This original system has been in use for about 3 years and has been fairly reliable, but its accuracy and noise immunity sometimes were not satisfactory. In addition, modifications to this system were difficult to make since any logic modifications would require wiring changes and hardware additions. As a result, a completely new cardiotachometer was developed, using an improved analog filter and R-wave detector and an Intel 8080A microprocessor to handle all of logic and arithmetic necessary. By using the microprocessor, all of the above requirements could more easily be met and future hardware modifications could be minimized if functional changes were needed.

GENERAL DESCRIPTION

In the implementation of the new cardiotachometer, a new approach was used to calculate heart rate. Instead of using the discrete transistor D/A converter to invert and display the count as was used before, a 16 bit precision software math routine is used, together with a monolithic 8-bit D/A converter. Also the previous model used 8 bit wide counters while the new one uses 16 bit wide registers. Thus accuracy and resolution is greatly increased. The interface hardware was built around an 8255 programmable peripheral interface IC. To this IC was added a D/A IC, switches with debounce circuits, light emitting diodes (LED's) with drivers, and a single bit A/D consisting of a special filter, automatic gain controller (AGC), and pulse detector. Also a calibration circuit was used consisting of an 8253 programmable interval timer, opto-isolators, and a digital multiplexer.

By using a microprocessor based system, future modifications can be added easily. Such modifications could be software digital filtering, a continuously updated averaging heart rate output, or other similar features.

A summary of the characteristics of the new cardiotachometer is given in Table 1.

TABLE 1
DEVICE OPERATIONAL SPECIFICATIONS

Input	-Single lead ECG
Output	-Analog voltage 0-3VDC representing 0-300 beats/min. (BPM)
Accuracy	-Better than 2% of reading over entire range Typically better than 1% over the range 30-230 BPM
Output Resolution	-1.13 BPM
Internal Resolution	-0.45 msec. in R-R interval measurement
Under & Over Range Indications	-LED illuminates and output drops to 0 when heart rate drops below 30 BPM or increases above 300 BPM
Calibration	-60 BPM or 180 BPM pulses obtained by dividing CPU crystal-controlled clock pulses can be switched to the system analog input for calibration and troubleshooting. Accuracy: ± 1 msec.

HARDWARE DESCRIPTION

The Central Processing Unit (CPU) board consists of the following:

8080A - CPU

8228 - System controller

8224 - System clock generator

74LS138 - Memory decoder

2708 - 1K x 8 bit Erasable Programmable Read-Only Memory (EPROM)

2111-1 - 256 x 4 bit static RAM (2 ea)

C6136P - -5VDC 50 MA regulator

7404 - Hex inverter

18.432 MHz - crystal

The 8080A chip set is configured as a 2 MHz system using isolated I/O-linear select. This allows up to 14 devices to be selected without a decoder chip.

The memory is configured by using a 2708 EPROM and two 2111-1 RAM's. This gives 1K of ROM and 256 bytes of RAM's. Due to using wire-wrap techniques and the availability of 2716 2Kx8 and 2732 4Kx8 EPROMS and 2114-1 1Kx4 static RAM's, the memory could be expanded up to 8K of ROM and 2K of RAM. Only minor changes in the wire-wrapping would be needed.

The 8224 system clock chip uses an 18.432 MHz crystal which gives a system clock frequency of 2.048 MHz.

The Input/Output (I/O) board consists of the following:

8255 - Programmable peripheral interface

8253 - Programmable interval timer

DAC-IC8BC - 8 bit D/A converter

LM1458 - Dual 741 op-amps

SN7404 - Hex inverter

SN7406 - LED Drivers

74153 - 4 to 1 digital multiplexer

6N138 - Opto-isolators

74123 - Dual one-shot multivibrators

The 8255 is the main IC for interfacing inputs and outputs to the CPU-Memory board. Port A (PA0-PA7) are used to feed the 8-bit output to the D/A converter and half of a LM1458 op amp to produce a 0-3VDC analog signal. This signal represents heart rate (0-300 BPM).

Port B (PB0-PB7) is not used at the present time.

Port C (PC0-PC7) is split via software control to use (PC0-PC3) as input and (PC4-PC7) as output. All outputs used are latched outputs so no refreshing is required.

Port C inputs (PC0-PC3) are not latched.

The 8253 is configured via software as a rate generator (mode 2) for constant output, and has three separate 16-bit timers.

Timer 0 is used to divide the main CPU clock via 2048 to produce a 1KHZ signal.

Timer 1 is used to divide the 1KHZ output from timer 0 to produce the Low Cal

signal. This signal is fed to half of the 74123 to produce a 10 msec. wide 60 BPM Low Cal signal. Timer 2 is used to divide the 1KHZ output from timer 0 to produce the High Cal signal. This signal is fed to the other half of the 74123 to produce a 10 msec. wide 180 BPM High Cal signal.

These two signals plus the TTL pulses from the conditioned ECG input signal are fed to a 74153 4-input, 1 output digital multiplexer. This multiplexer is controlled from the main CDAS computer via two 6N138 opto-isolators. Control codes are:

00 input to the 6N138's connects the ECG input to the cardiotachometer peripheral interface input.

01 input to the 6N138's connects the 60 BPM Low Cal pulses to the input.

10 input to the 6N138's connects the 180 BPM High Cal pulses to the input.

11 input to the 6N138's disconnects the cardiotachometer input for the Standby mode.

The raw ECG signal is specially conditioned by 3 circuits which were developed from a modified Skylab type cardiotachometer to produce a 10 msec. pulse which represents the R-wave of the ECG. The ECG is first sent to a 10 HZ-30HZ bandpass filter. The output of the filter is then sent to the automatic gain control (AGC) circuit. The AGC circuit outputs a pulse with constant amplitude even with varying ECG input amplitudes. This output is then sent to the pulse detector.

The pulse detector outputs a 10 msec. wide pulse. The pulse detector also incorporates a pulse width controller. This circuit produces a constant pulse

width output even with changes in the ECG input. This allows the 8080 CPU to do all of its calculations and displaying during the pulse. The output, along with the 60 BPM Low Cal, 180 BPM High Cal, and 0 BPM Standby signals, is then fed to the 74153 digital multiplexer. The multiplexer output is then fed to the PC0 input of the 8255 peripheral interface.

PC1 and PC2 are also inputs which are connected to two SPDT push button switches via 7404 debounce circuits. Switch 1, connected to PC1, causes the CPU to select a D/A setup routine. This routine outputs via the D/A either a 0 or full scale signal each time switch 1 is pushed. This allows for adjustments of the D/A for zero and full scale values. Switch 2, connected to PC2, causes the CPU to select a ramp routine. This allows for checking D/A linearity and missing code conditions, and checks other functions of the microprocessor as well.

The front panel LED's are connected to other 8255 port C outputs via 7406 LED drivers as follows: ECG LED to PC0, Underrange LED to PC4, and OVERRANGE LED to PC5. PC3, PC6, and PC7 are not used at present.

SOFTWARE DESCRIPTION

Heart Rate Monitor

Refer to the flowcharts and program listing for this discussion. The program starts at address 0000. None of the interrupts are used. The stack pointer is set and then the initialize routine initializes the 8255, 8253 timers, ectopic flag, pause flag, misbeat reference storage area, and the ectopic reference storage area.

It next calls the input routine from the start routine and waits for either a ECG/Cal input or for switch 1 to be pushed. If switch 1 is pushed, the program jumps to the D/A setup routine. If an ECG/Cal pulse is present, it returns and waits for the ECG/Cal pulse to end.

When the pulse has ended the program enters the Count routine, where the HR counter is initialized and then a timing loop is entered. The program loops until either the count reaches the under range count or there is another ECG/Cal/Switch input.

If the count reaches the underrange count, it then jumps to the underrange routine ERR1. The D/A is set to 0 VDC and the underrange LED is turned on. The program then jumps to start.

If an ECG/Cal pulse is detected, the program then enters the Check routine. There it first determines if the ectopic flag, ECTFLG, was set on the previous beat. If so, the Pause flag is then set, since there may be a compensatory

pause (longer than normal R-R interval) following a premature beat. If ECTFLG was not set, then the current R-R interval count is compared with the missed beat reference value (MISBEAT), which is a number equal to slightly less than twice the previous normal R-R interval count. If the current count is greater, then the program simply assumes that one or more beats have been missed due to an ECG dropout, lead change, or similar temporary problem.

MISBEAT is then reset and the program jumps back to Start. Nothing is changed on the output, and this procedure therefore keeps a short signal dropout from causing an erroneous heart rate from being output.

If there was no missed beat condition or if the Pause flag was set, then the current count is compared with the ectopics reference count, ECT. This number is approximately 3/4 of the previous normal R-R interval count. If the current count is less, then the current beat is probably an ectopic and therefore the ectopic flag ECT is set before continuing.

Next, the count is checked for an overrange condition. If the count is less than that corresponding to a heart rate of 300, the program jumps to ERR2. There, the D/A converter is set to 0 VDC, the overrange LED is turned on, and the program jumps back to start.

If it is not overranged then ECTFLG is checked. If ECTFLG is set, the program goes to the output routine. If not set, the pause flag is checked. If the pause flag is set the program goes to the output routine. If the pause flag is not set then a new MISBEAT reference count and ECT reference count are calculated and stored and then the program goes to the output routine.

The MISBEAT reference and ECT reference are variable indicators, based on the previous normal R-R interval count, which are used to determine if a missed beat or ectopic has happened.

The program then goes to the Output routine. The count is divided by a constant. The result is an eight bit number which is sent to the D/A and outputed. Both under and overrange LEDS are turned off and the pause flag is reset. The program then goes back to Start for the next heart beat.

D/A Setup Routine

In the Heart Rate Monitor Program if the Input routine detects switch 1 it then jumps to the setup routine.

The setup routine first outputs a 00 to the D/A converter. This sets the D/A to zero volts output. This allows for adjustment of the D/A zero.

When switch 1 is pushed again a FF is sent to the D/A. This is the full scale condition and allows for adjustment of the full scale value (normally 3 volts) on the D/A.

Each time switch 1 is pushed either a zero or full scale output appears on the output of the D/A.

D/A Ramp Routine

If switch 2 is pushed during the setup routine, the program jumps to the D/A Ramp routine. This routine first outputs a zero to the D/A. It then enters

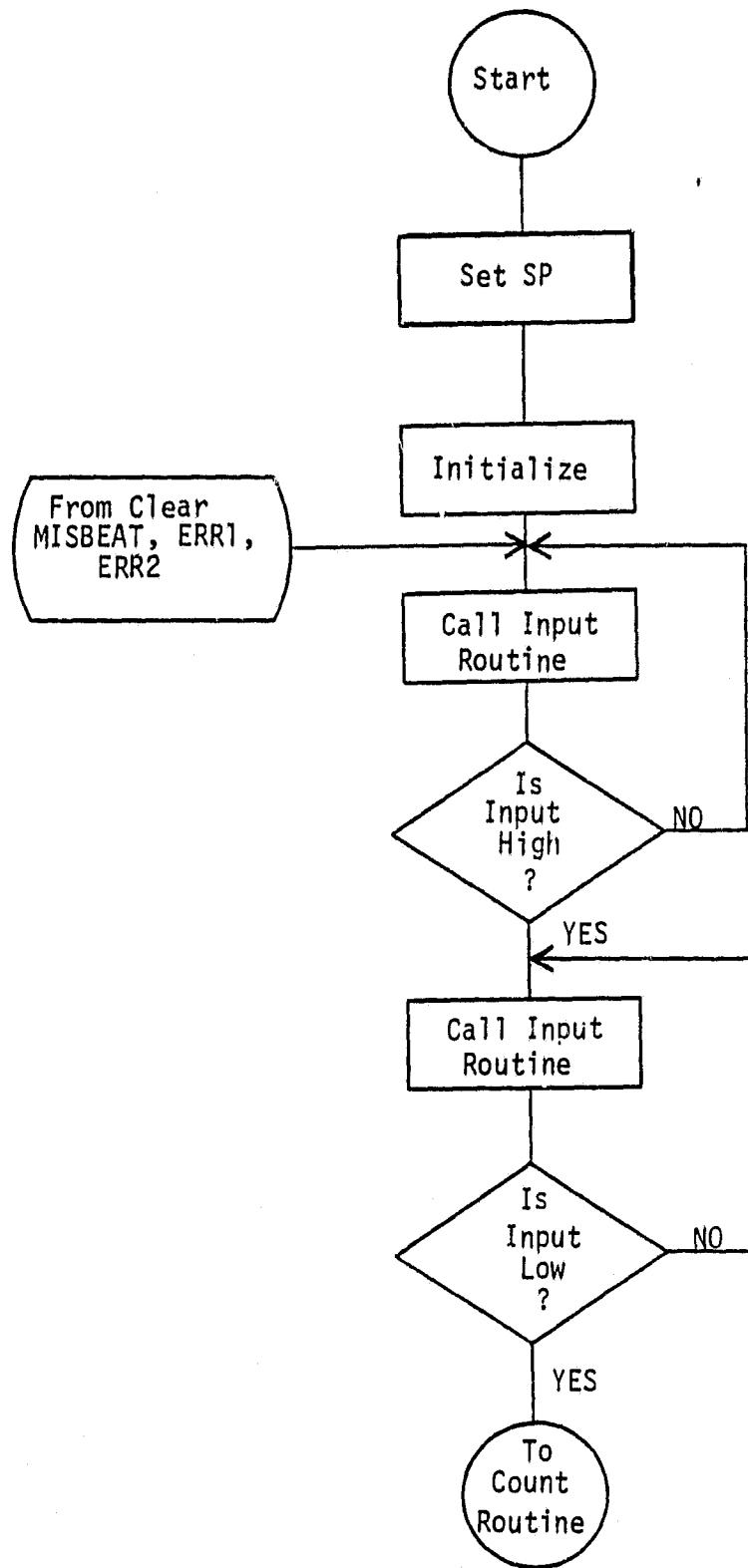
a wait loop. Upon completion of the wait period the D/A is updated by one count and the routine jumps back to the wait loop,

This routine allows for checking that the D/A responds correctly and if the 8255 outputs a wrong code.

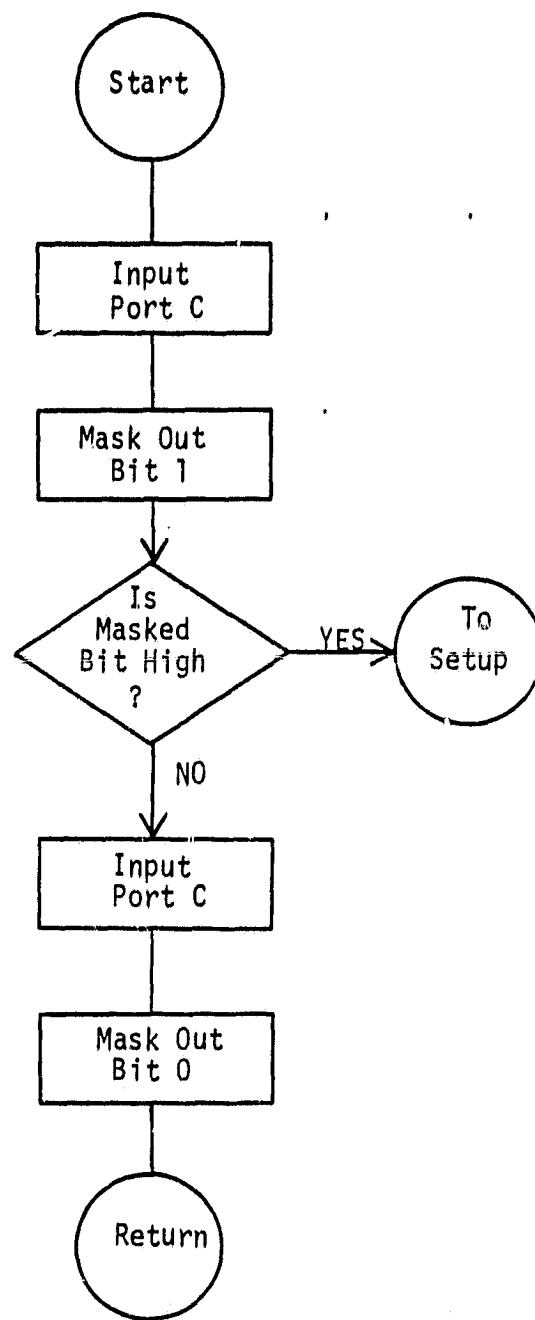
Pressing the reset switch at any time returns the program to the beginning of the Heart Rate Monitor routine.

APPENDIX A

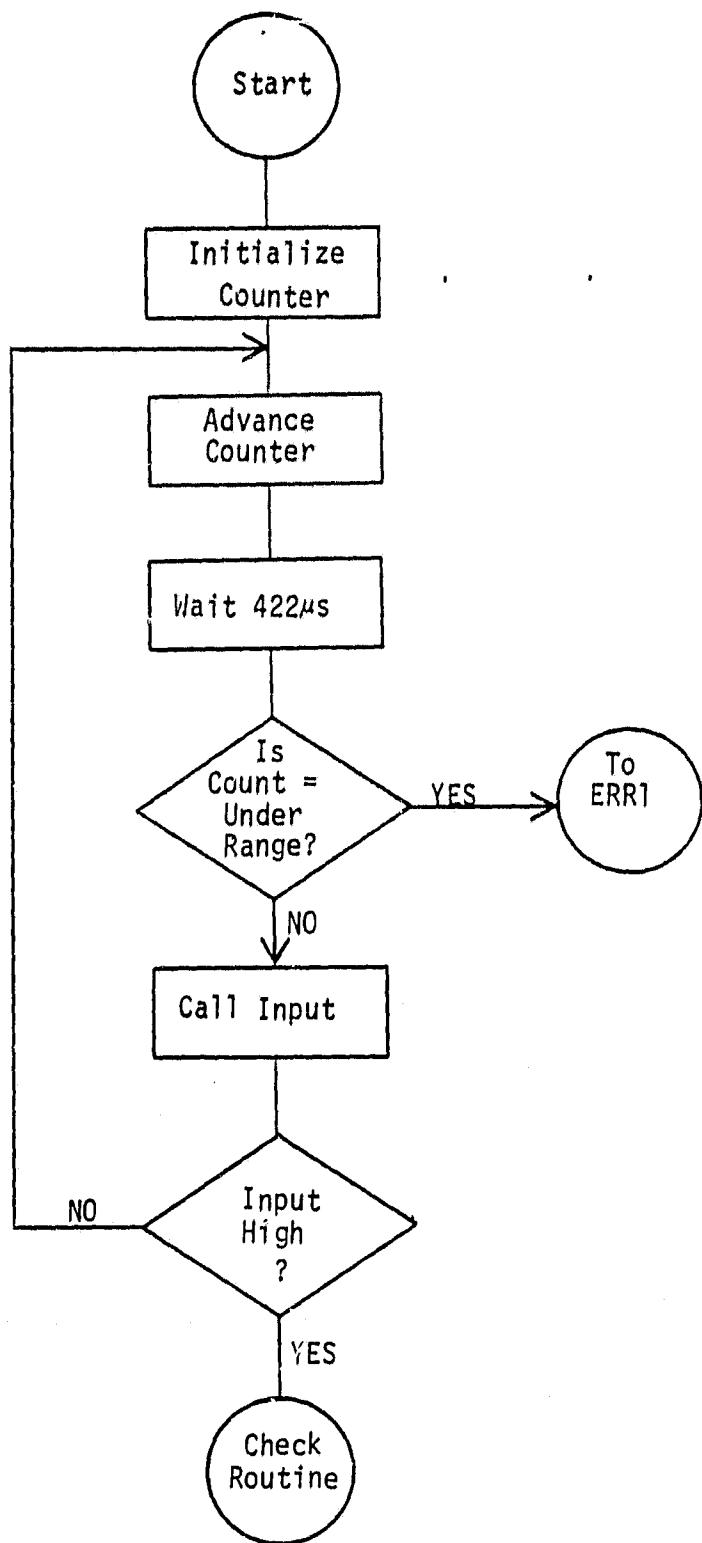
START ROUTINE



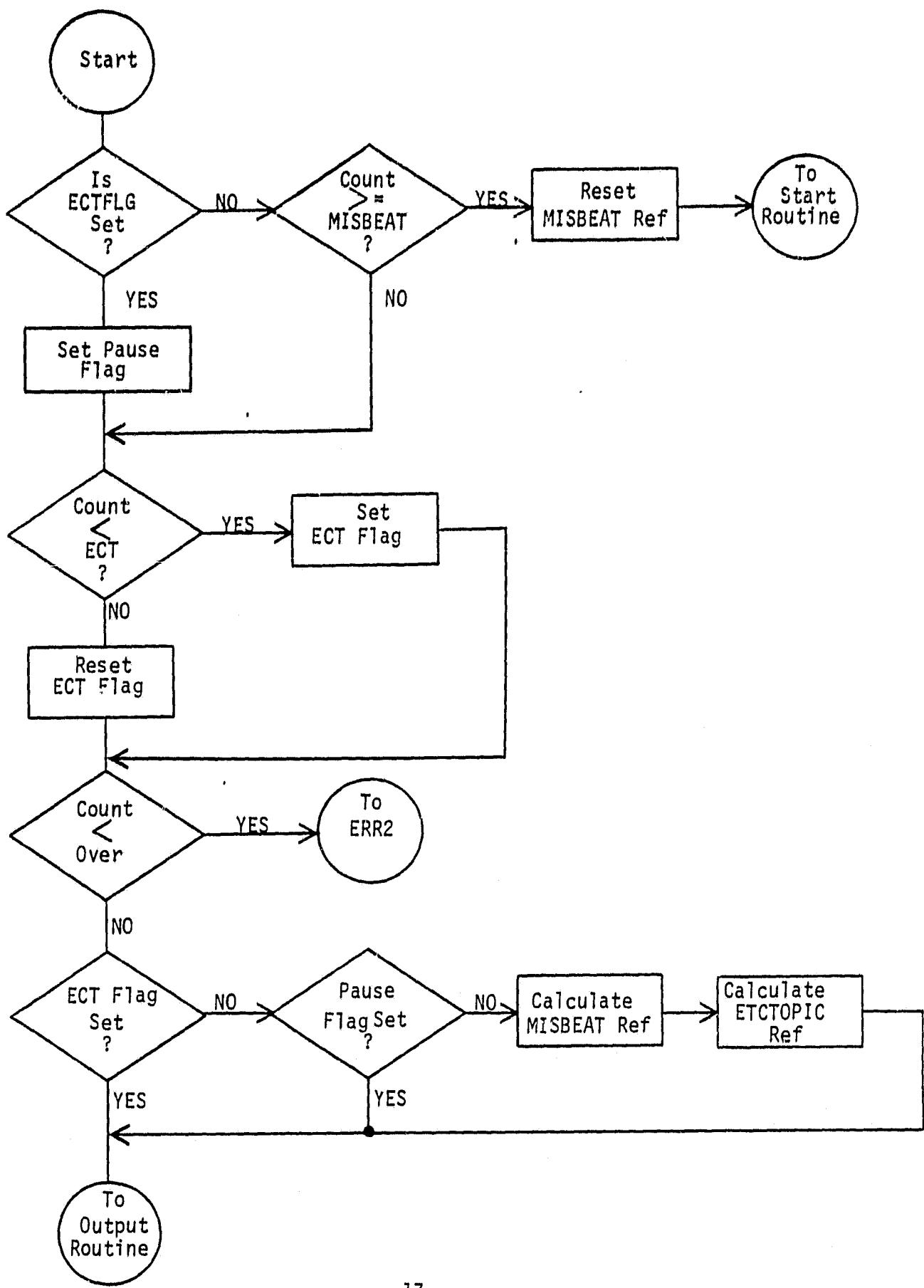
INPUT ROUTINE
(For Switch 1 and ECG/Cal Pulses)



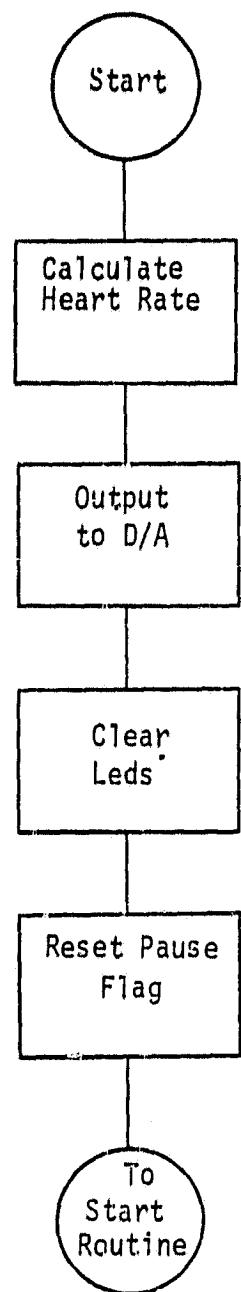
COUNT ROUTINE



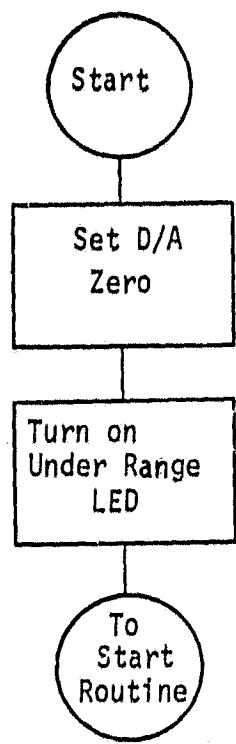
CHECK ROUTINE



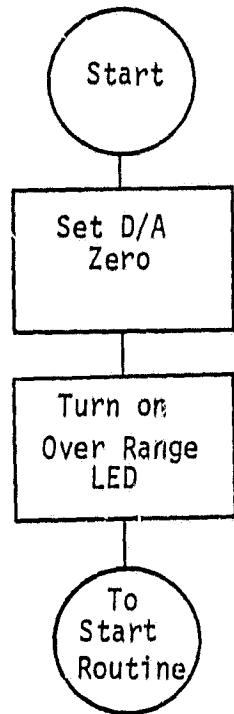
OUTPUT ROUTINE



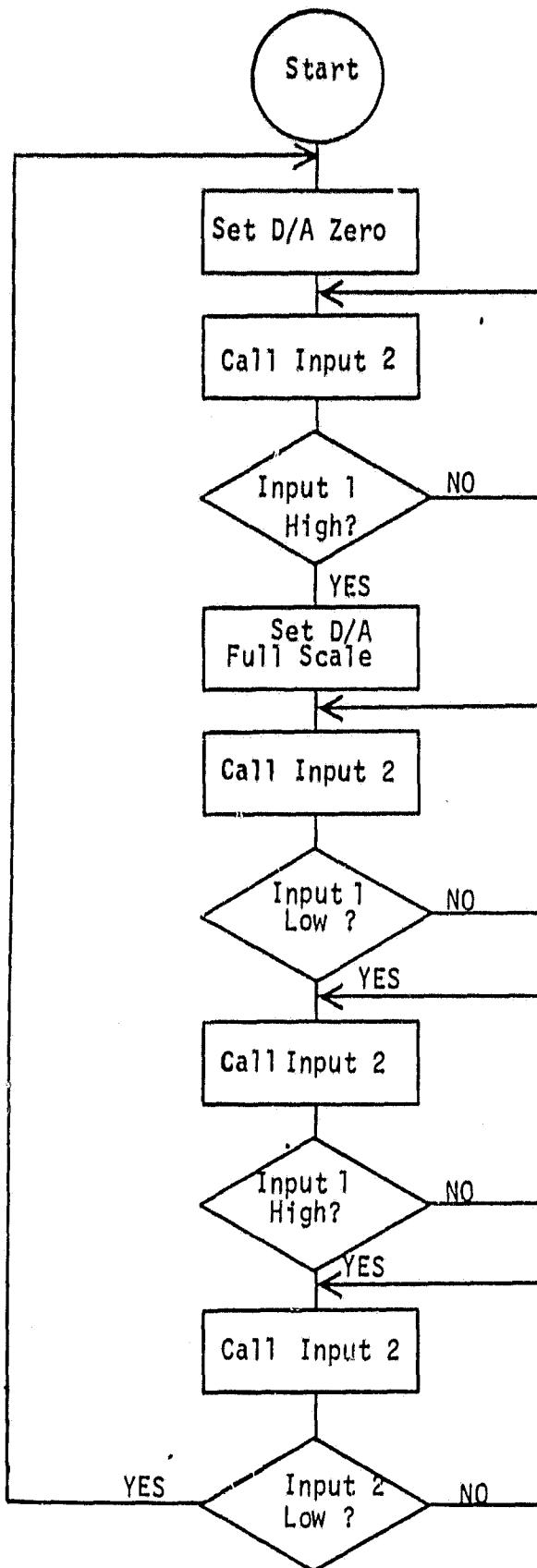
ERR 1 (Underrange)



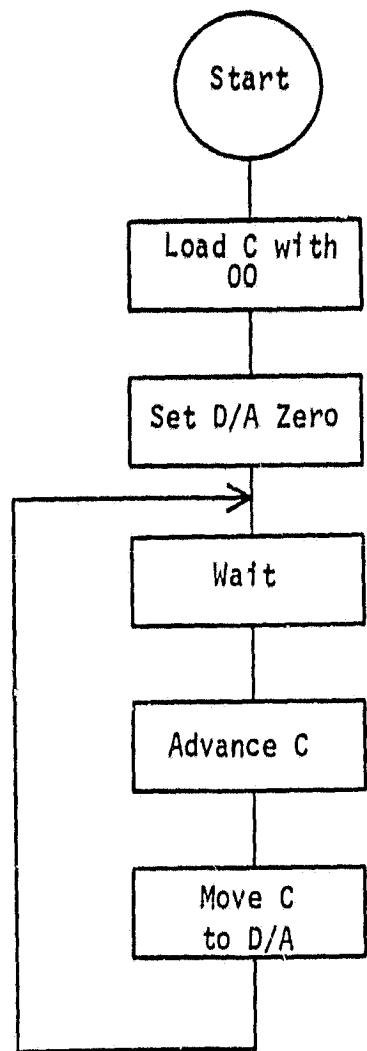
ERR 2 (Overrange)



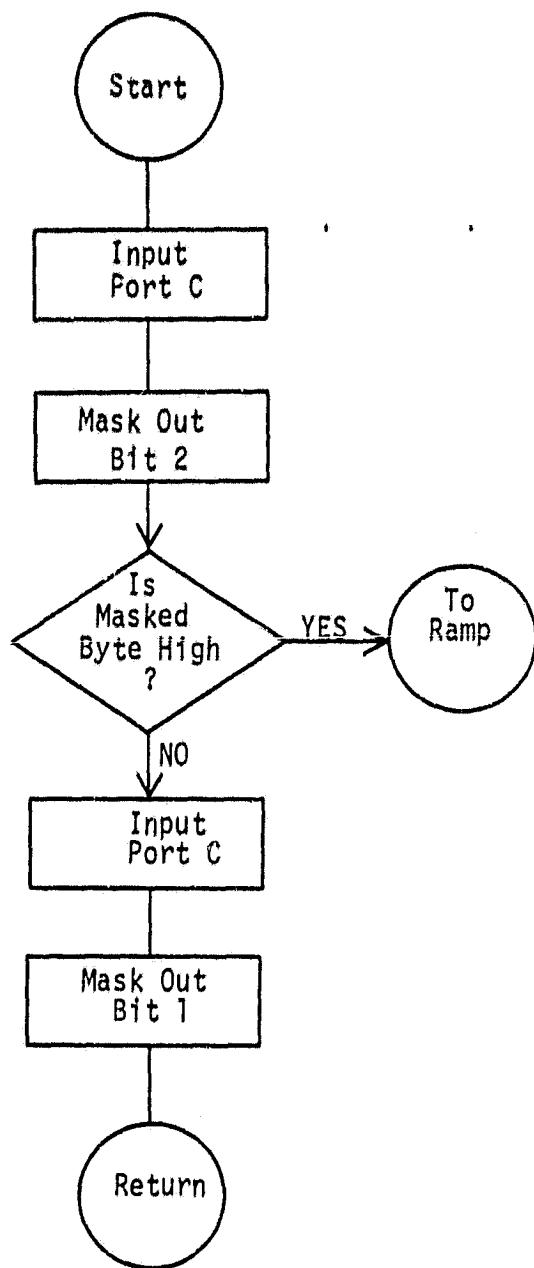
D/A SETUP ROUTINE



D/A RAMP ROUTINE



**INPUT 2 ROUTINE
(For Switch 2)**



APPENDIX B

0000	31FF1C	BEGIN:	LXI SP	;SET UP STACK POINTER
0003	CDCA00		CALL INIT	;INITIALIZATION ROUTINE
0006	CDOA01	START:	CALL INPUT	
0009	CA0600		JZ START	
000C	CDOA01	S1:	CALL INPUT	;WAIT FOR R-WAVE
000F	C20C00		JNZ S1	;TO END THEN GO
0012	110000	COUNT:	LXI D,E	;INITIALIZE HR COUNTER
0015	13		C1: INX D,E	
0016	011301	TIMER:	LXI B,C	
0019	0D		T1: DCR C	
001A	79		MOV A,C	
001B	FE00		CPI A,00	;SEE IF C IS ZERO
001D	C21900		JNZ T1	;IF NOT GOTO T1
0020	05		DCR B	
0021	78		MOV A,B	
0022	FE00		CPI A,00	;SEE IF B IS ZERO
0024	C21900		JNZ T1	;IF NOT GOTO T1
0027	EB	UNDER:	XCHG	;SWAP D,E WITH H,L
0028	11F813		LXI D,E	;LOAD UNDER RANGE CODE
002B	CD1801		CALL HILO	;CHECK FOR UNDER RANGE
002E	CD3E01		JC ERR1	;IF SO GOTO ERR1
0031	EB		XCHG	;SWAP D,E WITH H,L
0032	CDOA01	C2:	CALL INPUT	;LOOK FOR NEXT R-WAVE
0035	CA1500		JZ C1	;IF NOT GOTO C1
0038	3A041C	MISBT:	LDA ECTFLG	;LOAD ECTOPIC FLAG
003B	FEFF		CPI A,FF	;SEE IF SET
003D	C27401		JNZ MISCNT	;IF FLAG NOT SET JMP
0040	3E01		MVI A,01	;IF FLAG SET THEN
0042	32041C		STA PAUSE	;SET PAUSE FLAG
0045	2A021C	ECT:	LHLD	;LOAD ECTOPIC REF INTO H,L
0048	EB		XCHG	;SWAP D,E WITH H,L
0049	CD1801		CALL HILO	;CHECK FOR ECTOPIC BEAT
004C	D25A00		JNC FLAG1	;IF SO GOTO FLAG1
004F	3A041C		LDA ECTFLG	;GET ECTOPIC FLAG
0052	3E00		MVI A,00	;RESET ECTOPIC FLAG
0054	32041C		STA ECTFLG	;STORE ECTOPIC FLAG
0057	C36100		JMP OVER	
005A	3A041C	FLAG1:	LDA ECTFLG	;GET ECTOPIC FLAG
005D	2F		CMA	;COMPLIMENT FLAG
005E	32041C		STA ECTFLG	;STOR ECTOPIC FLAG
0061	00	OVER:	NOP	;SWAP D,E WITH H,L
0062	11C001		LXI D,E	;LOAD OVER RANGE CODE
0065	CD1801		CALL HILO	;CHECK FOR OVER RANGE
0068	D24901		JNC ERR2	;IF SO GOTO ERR2
006B	EB		XCHG	;SWAP D,E WITH H,L
006C	00		NOP	
006D	3A041C	FLGCK:	LDA ECTFLG	;GET ECTOPIC FLAG
0070	FEFF		CPI A,FF	
0072	CA8D00		JZ DIVIDE	;IF NOT SET GOTO DIVIDE
0075	3A051C		LDA PAUFLG	;GET PAUSE FLAG
0078	FE01		CPI A,01	
007A	CA8D00		JZ DIVIDE	;IF NOT SET GOTO DIVIDE
007D	0E1C	HRREF:	MIV C,1.75	;MISBT CONSTANT

007F	CD5401	CALL MULT	;CALCULATE NEW MISBT
0082	22001C	SHLD	;STORE NEW MISBT REF
0085	0E0C	MIV C,.75	;ECTREF CONSTANT
0087	CD5401	CALL MULT	;CALCULATE NEW ECTREF
008A	22021C	SHLD	;STORE NEW ECTREF
008D	010507	DIVID:	LXI B,C ;THIS ROUTINE IS
0090	7A	MOV A,D	;AN UNSIGNED 16-BIT
0091	2F	CMA	;DIVIDE ROUTINE
0092	57	MOV D,A	
0093	7B	MOV A,E	
0094	2F	CMA	
0095	5F	MOV E,A	
0096	13	INX D,E	
0097	210000	LXI H,L	
009A	3E17	MVI A,17	
009C	E5	DVO:	PUSH H,L ;REGISTERS H,L USED
009D	19		DAD D,E ;TO STORE DATA
009E	D2A200		JNC DV1 ;TEMPORARILY
00A1	E3		XTHL
00A2	E1	DV1:	POP H,L
00A3	F5		PUSH PSW
00A4	79		MOV A,C
00A5	17		RAL
00A6	4F		MOV C,A
00A7	78		MOV A,B
00A8	17		RAL
00A9	47		MOV B,A
00AA	7D		MOV A,L
00AB	17		RAL
00AC	6F		MOV L,A
00AD	7C		MOV A,H
00AE	17		RAL
00AF	67		MOV H,A
00B0	F1		POP PSW
00B1	3D		DCR A
00B2	C29C00		JNZ DVO
00B5	B7	CLEAN:	ORA A
00B6	7C		MOV A,H
00B7	1F		RAR
00B8	57		MOV D,A
00B9	7D		MOV A,L
00BA	1F		RAR
00BB	5F		MOV E,A
00BC	79	OUTD/A:	MOV A,C ;PUT RESULT IN A
00BD	3C		INR A ;ADD ONE TO A
00BE	D304		OUT D/A ;LOAD PORT A-D/A
00CO	3E00	CLEAR:	MVI A,00
00C2	D306		OUT LEDS ;LOAD PORT B-LEDS
00C4	32051C		STA PAUFLG ;SET PAUSE FLAG TO 00
00C7	C30600		JMP START

00CA	3E81	INIT:	MVI A,81	;LOAD MODE 0 &
00CC	D307		OUT PPI	;OUTPUT TO PPI-8255
00CE	3E34		MVI A,34	;LOAD MODE 2 &
00DO	D30B		OUT ITO	;OUTPUT TO COUNTER 0-8253
00D2	3E74		MVI A,74	;LOAD MODE 2 &
00D4	D30B		OUT IT1	;OUTPUT TO COUNTER 1-8253
00D6	3EB4		MVI A,B4	;LOAD MODE 2 &
00D8	D30B		OUT IT2	;OUTPUT TO COUNTER 2-8253
00DA	3E00		MVI A,FF	;LOAD COUNTER 0
00DC	D308		OUT ITO	;DIVIDE BY 2047
00DE	3E08		MVI A,07	
00E0	D308		OUT ITO	
00E2	3EE8		MVI A,E8	;LOAD COUNTER 1
00E4	D309		OUT IT1	;DIVIDE BY 1000
00E6	3E03		MVI A,03	
00E8	D309		OUT IT1	;60 BPM CAL SIGNAL
00EA	3E4D		MVI A,4D	;LOAD COUNTER 2
00EC	D30A		OUT IT2	;DIVIDE BY 333
00EE	3E01		MVI A,01	
00FO	D30A		OUT IT2	;180 BPM CAL SIGNAL
00F2	3EFF		MVI A,FF	;INITIALIZE MISBT REFERENCE
00F4	32001C		STA	;TO FFFF
00F7	32011C		STA	
00FA	00		NOP	
00FB	3E00		MVI A,00	
00FD	32021C		STA	;INITIALIZE ECTOPIC
0100	32031C		STA	;REFERENCE TO 0000
0103	32041C		STA	;SET ECTOPIC FLAG TO ZERO
0106	32051C		STA	;SET PAUSE FLAG TO ZERO
0109	C9		RET	
010A	DB06	INPUT:	IN PORTC	;CHECK IF SWITCH 1
010C	0602		MVI B,02	;WAS PUSHED
010E	A0		ANA B	
010F	C29401		JNZ SETUP	;IF SO GOTO STEP
0112	DB06		IN PORT C	
0114	0601		MVI B,01	;CHECK FOR ECG OR
0116	A0		ANA B	;CAL SIGNAL
0117	C9		RET	
0118	C5	HILO:	PUSH B,C	;THIS ROUTINE COMPARES
0119	47		MOV B,A	;H,L WITH D,E
011A	E5		PUSH H,L	
011B	7A		MOV A,D	
011C	B3		ORA A	;IF H,L IS LESS
011D	CA3901		JZ HILO1	;THAN D,E THEN
0120	23		INX H,L	;CARRY IS SET 0
0121	7C		MOV A,H	
0122	B5		ORA L	;IF H,L IS GREATER
0123	CA3901		JZ HILO1	;THAN OR EQUAL

0126	E1	POP H,L	;TO D,E THEN CARRY
0127	D5	PUSH D,E	;IS SET 1
0128	3EFF	MVI A,FF	
012A	AA	XRA D	
012B	57	MOV D,A	
012C	3EFF	MVI A,FF	
012E	AB	XRA E	
012F	5F	MOV E,A	
0130	13	INX D,E	
0131	7D	MOV A,L	
0132	83	ADD E	
0133	7C	MOV A,H	
0134	8A	ADC D	
0135	D1	POP D,E	
0136	78	MOV A,B	
0137	C1	POP B,C	
0138	C9	RET	
0139	E1	HIL01: POP H,L	
013A	78	MOV A,B	
013B	C1	POP B,C	
013C	37	STC	
013D	C9	RET	

013E	3E00	ERR1: MVI A,00	;SET D/A TO ZERO
0140	D304	OUT D/A	;AND TURN ON UNDER
0142	3E10	MVI A,10	;RANGE LED
0144	D306	OUT LEDS	
0146	C30600	JMP START	

0149	3E00	ERR2: MVI A,00	;SET D/A TO ZERO
014B	D304	OUT D/A	;AND TURN ON OVER
014D	3E20	MVI A,20	;RANGE LED
014F	D306	OUT LEDS	
0151	C30600	JMP START	

0154	D5	MULT: PUSH D,E	;THIS ROUTINE MULTIPLIES
0155	EB	XCHG	;2 UNSIGNED 8 BIT
0156	29	DADH	;NUMBERS AND
0157	29	DADH	;PRODUCES AN
0158	29	DADH	;UNSIGNED 16 BIT
0159	29	DADH	;RESULT
015A	EB	XCHG	
015B	0600	MVIB,00	
015D	1E09	MVI E,09	
015F	79	MOV A,C	
0160	1F	RAR	
0161	4F	MOV C,A	
0162	1D	DCR E	
		MULTO:	

;REGISTER D IS
;MULTIPLICAND

;REGISTER C IS
;MULTIPLIER

0163	CA7001	JZ DONE	;REGISTER B IS
0166	78	MOV A,B	;MSB RESULT
0167	D26B01	JNC MULT1	
016A	82	ADD D	;REGISTER C IS
016B	1F	MULT1: RAR	;LSB RESULT
016C	47	MOV B,A	
016D	C35F01	JMP MULT0	
0170	60	MOV H,B	
0171	69	MOV L,C	
0172	D1	POP D,E	
0173	C9	RET	
0174	2A001C	MISCNT: LHLD HR REF	;LOAD HR RE
0177	EB	XCHG	
0178	CD1801	CALL HILO	
017B	D20045	JNC ECT	
017E	3EFF	MVI A,FF	
0180	32001C	STA	
0183	32011C	STA	
0186	31FFIC	LXI SP	
0189	C30600	JMP START	
018C	000000	NOP	
018F	000000	NOP	
0192	0000	NOP	

8080 MICRO CARDIOTACHOMETER SOFTWARE

ZERO & FULL SCALE PROGRAM

0194	3E00	STEP: MVI A,00	;THIS ROUTINE
0196	D304	OUT D/A	;ALLOW ADJUSTMENT
0198	CDD501	L1: CALL IN2	;OF THE D/A FOR
019B	CA9801	JZ L1	;ZERO AND FULL
019E	3EFF	MVI A,FF	;SCALE OUTPUT
01A0	D304	OUT D/A	
01A2	CDD501	L2: CALL IN2	
01A5	C2A201	JNZ L2	
01A8	CDD501	L3: CALL IN2	
01AB	CAA801	JZ L3	
01AE	CDD801	L4: CALL IN2	
01B1	C2AE01	JNZ L4	
01B4	C39401	JMP STEP	

RAMP PROGRAM

01B7	0300	RAMP: MVI C,00	
01B9	79	MOV A,C	
01BA	D304	OUT D/A	
01BC	CDDD01	T1: CALL IN3	
01BF	1B	DCX D,E	
01C0	7A	MOV A,D	
01C1	FE00	CPI A,00	
01C3	C2BC01	JNZ T1	
01C6	CDDD01	T2: CALL IN3	

01C9	1B	DCX D,E
01CA	78	MOV A,E
01CB	BA	CMP D
01CC	C2C601	JNZ T2
01CF	79	MOV A,C
01D0	D304	OUT D/A
01D2	C3B701	JMP RAMP

SUBROUTINE FOR STEP & RAMP PROGRAMS

01D5	DB06	IN2: IN PORTC
01D7	0604	MVI B,04
01D9	A0	ANA B
01DA	C2B701	JNZ RAMP
01DD	DB06	IN3: IN PORT C
01DF	0602	MVI B,02
01E1	A0	ANA B
01E2	C9	RET

*

APPENDIX C

8080 MICRO CARDIOTACHOMETER SOFTWARE

REAL-TIME HEART RATE PROGRAM
EXECUTION TIMES

<u>OPERATION</u>	<u>TIMES</u>
START-UP NO SIGNAL IN	144.6 μ s
DELAY TIMER ROUTINE	422.08 μ s
EACH COUNT OF D,E REGISTER	584.26 μ s
UNDER RANGE LED & ZERO OUTPUT	21.98 μ s
OVER RANGE LED & ZERO OUTPUT	21.98 μ s
UNDER RANGE <30 BPM	2.307 sec.
OVER RANGE >300 BPM	187.07 ms
16 BIT DIVISION ROUTINE	1.74 ms
OUTPUT & CLEAR ROUTINE	23.94 μ s
CALCULATE & DISPLAY TIME	1.77 ms
OPERATING SPEED RANGE	>187.07 ms to <2.307 sec.

APPENDIX D

WIRE WRAP LIST
CPU-MEMORY

+5VDC

C20 to +5
A1 to A2 to A3 to
A4 to A6 to +5
A27 to A28 to +5
B10 to +5
B18 to +5
B36 to +5
D22 to +5
D32 to +5
J1 to +5
J16 to +5
J29 to +5
A23 to +5

-5VDC

A44 to J32 to
J19 to C11 to
25

+12VDC

1 to 7 to
A34 to B17 to
E12 to J21 to
J34

-12VDC

24 to 30 to A45

GND

A17 to GND
A25 to GND
A42 to GND
A46 to GND
B5 to GND
B44 to B45 to GND
C2 to GND
C13 to GND
C30 to GND
C40 to GND
D25 to GND
D35 to GND
G14 to GND
G27 to GND
G40 to GND
J7 to GND
J22 to GND
J35 to GND

WIRE WRAP LIST
CPU-MEMORY

SIGNALS

B1 to A36 to A16 to 27
 B2 to A37 to C14
 B3 to B4 to 2
 A5 to A11 to 3
 B6 to A12
 A15 to 26
 A7 to A8
 B7 to B11
 B8 to B12
 B24 to C15
 A13 to E18
 A10 to C12 to 40
 A14 to C19
 B16 to E19
 C10 to J14
 C9 to J12
 C8 to G12
 C7 to G10
 C3 to G6
 C4 to J10
 C5 to J8
 C6 to G8
 E20 to G2
 C17 to G4
 C18 to G3
 B34 to J6
 J2 to 41
 J4 to 42

DATA

G13 to G24 to G37 to D29 to 23 (D0)
 J13 to G25 to G38 to D28 to 22 (D1)
 G11 to G26 to G39 to D27 to 21 (D2)
 G9 to J27 to J40 to D26 to 20 (D3)
 G5 to J26 to J39 to D39 to 43 (D4)
 J11 to J25 to J38 to D38 to 44 (D5)
 J9 to J24 to J37 to D37 to 45 (D6)
 G7 to J23 to J36 to D36 to 46 (D7)

ADDR

E16 to G23 to G36 to C25 to C35 to 19 (A0)
 E15 to G22 to G35 to C24 to C34 to 18 (A1)
 E14 to G21 to G34 to C23 to C33 to 17 (A2)
 E12 to G20 to G33 to C22 to C32 to 40 (A3)
 E11 to G19 to G32 to D23 to D33 (A4)
 E10 to G18 to G31 to C26 to C37 (A5)
 E9 to G17 to G30 to C27 to C38 (A6)
 E8 to G16 to G29 to C28 to C39 (A7)
 E7 to J17 to J30 (A8)
 E6 to J18 to J31 (A9)
 C1 to A18 (A10)
 E1 to A19 (A11)
 E4 to A20 (A12)
 E3 to A21 (A13)
 E2 to A22 (A14)
 (A15)

CONTROL-SIGNALS

B19 to B27 to J20	{ CS0 }
B20 to B28 to J33	{ CS1 }
A24 to D30 to D40	{ CS7 }
D24 to D34 to J5	{ MEMR }
C30 to C40 to J3	{ MEMW }
J6 to B34	
J4 to 42	{ RD }
J2 to 41	{ WR }

WIRE WRAP LIST
INTERFACE BOARD

GROUND-BLK

AC14 to GND
AA33 to GND
AD22 to GND
AH7 to GND
AH15 to GND

AA6 to +5
AC22 to +5
AE15 to +5
AE9 to AF4 to +5
AJ1 to AJ9 to +5

+12VDC-WHITE

AE1 to GA7
AG5 to B43
AE1 to AE5

-12VDC-GREEN

AD4 to AD8 to
AB50 to AF10
to GA30

8255 & 8253 SIGNALS

GA40 to AH3 to AC25
GA41 to AA16 to AC23
GA42 to AC16 to AC24
GA28 to AA15

8255 & 8253 SIGNALS

GA23 to AA14 to AA29
GA22 to AA13 to AA28
GA21 to AA12 to AA27
GA20 to AA11 to AA26
GA43 to AA10 to AA25
GA44 to AA9 to AA24
GA45 to AA8 to AA23
GA46 to AA7 to AA22
GA19 to AC12 to AC27
GA18 to AC13 to AC26
GA17 to AH1
AH2 to AC15

DEBOUNCE SWITCHES

GB23 to AH5 to AJ7
GB46 to AJ6 to AH6 to AC6
GB22 to AJ3 to AJ4
GB45 to AJ2 to AJJ to AC5

ECG LED

AH13 to BA16
AH14 to BC7
BD7 to 5B21 (LED1 out)

LEDS 2 & 3

LED2 under
LED3 over

UNDER LED

AC8 to AH9
AH10 to BC5
BD5 to 5B44 (LED2 out)

OVER LED

AC9 to AH11
AH12 to BC6
BD6 to GB20 (LED3 out)

WIRE WRAP LIST

INTERFACE GROUP

FILTER CIRCUIT

SIGNAL GND
AG30 to GND
AE27 to GND
AG34 to GND
AD30 to GND
AF33 to GND
AD37 to GND

SIGNALS

AD24 to AD25 to AG29
AD26 to AD27 to AF28
AF29 to AD28
AE28 to AE29 to AE31 to AG32
AD29 to AD33 to AG33
AE33 to AE34 to AE30 to AD31
AD34 to AD35
AE35 to AE36 to AE38 to AF31
AD36 to AD37 to AF32
AD38 to AE39 to AE37

INPUT

AD40

OUTPUT

AE25 to AF27

OUTPUT2

AE24 to AG28

PULSE DETECTOR

SIGNALS

AH32 to AH33 to AG26
AJ36 to AJ37 to AJ38 to AF24
AF23 to AJ31
AH30 to AH31
AJ30 to AJ27 to AJ44
AH44 to AH28
AH45 to AJ39
AH40 to AH41
AJ40 to AJ39

PULSE DETECTOR

GNDS
AJ17 to GND AJ24 to AJ26 to GND
AJ21 to GND
AJ32 to GND
AH37 to GND
AJ41 to GND
AH37 to GND

+12VDC

AJ19 to AG23 to AG27 to AG31 to AG38

-12VDC

AF22 to AF26 to AF30 to AF34 to AH39

SIGNALS

AJ18 to AJ19 to AG21
AH19 to AH21 to AH22
AH20 to AG22
AJ20 to AD47
AD50 to AB43
AJ22 to AF19
AH24 to AH27 to AH28 to AF20
AH26 to AH35 to AH36 to AF21 to AF25
AJ28 to AH29 to AG25
AJ29 to AG24

LSI-11 INTERFACE

GNDS

BB4 to GND
BB8 to GND
BA17 to BB11 to GND
BA12 to GND

WIRE WRAP LIST
INTERFACE BOARD

D/A

AC17 to AE10
AC18 to AE11
AC19 to AE12
AC20 to AE13
AA20 to AD13
AA19 to AD12
AA18 to AD11
AA17 to AD10

SIGNAL GND

AG4 to GND
AG7 to AG8 to AG4
AD6 to AD7 to
AD3 to GND
AG1 to AG4

SIGNAL

AF1 to AF2 to AF3 to
AD2 to AD9 to AC43
AD1 to AG3 to AC50 to
GB18
AE8 to AG6
AG10 to AE6
AG2 to AA47
AF6 to AF5 to AF8
AF7 to AE7

AGC CIRCUIT

+12VDC

AD43 to AE43
AF38 to AF34
AG35 to AG31
AD50 to AE50

CIRCUIT

AG40 to AG41 to AG42 to AF36
AF41 to AF43 to AG46
AG44 to AF37
AG43 to BB44 to AF35
AF45 to AF47
BA44 to BA45
BB45 to BB46
BA46 to BA47 to BA48 to AG38
BA49 to BA50 to AG37
BB49 to AG36 to AG45

SIGNAL GND

AF44 to GND
AG46 to GND
BB47 to BB48 to GND
BB50 to GND

OUTPUT

BB44 to AJ35

INPUT

AF27 to AF40

INPUTS

AJ33 to AJ35

OUTPUTS

AH17 to AH18 to AG20 to BA15

LSI-11 INTERFACE

+5VDC

BB1 to +5

BB5 to +5

BB10 to +5

BD3 to BD4 to +5

SIGNALS

BD1 to BD2 to GB42

BA3 to GB43 (CSR0)

BA7 to GB19 (CSR1)

BC1 to BA2

BC2 to BA6

BB3 to BC3 to BB12

BB7 to BC4 to BA11

INPUTS

AG20 to BA15 (ECG)

AE18 to BA14 (LOW CAL)

AD19 to BA13 (HIGH CAL)

OUTPUTS

BA16 to AC7

WIRE WRAP LIST
INTERFACE BOARD

CALIBRATION CIRCUIT

+5VDC

AA32 to +5
AC32 to +5
AC30 to +5
AE15 to +5
AD16 to AD17 to +5
AE19 to AE20 to +5
AF11 to AF13 to +5

GNDs

AD22 to GND

SIGNALS

GA26 to AA30
AA31 to AC28 to AC31
AC29 to AE22
AC33 to AD15
AG11 to AG12 to AE16
AG13 to AG14 to AD21
AF12 to AE17
AF14 to AD20

OUTPUTS

AE18 to BA14 (LOW CAL)
AD19 to BA13 (HIGH CAL)

APPENDIX E

TF 1

D0	D1	D2	D3	A0	A1	A2	7'	24	1
23	22	21	20	19	18	17			

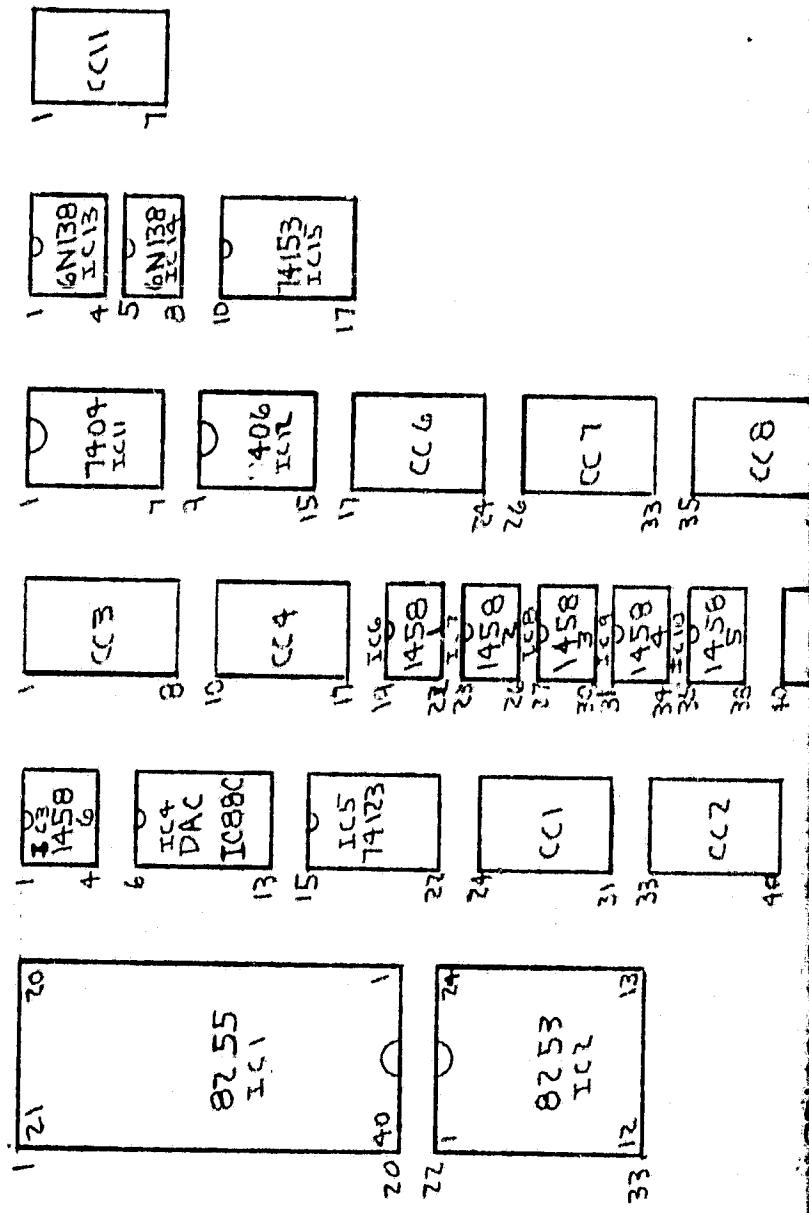
TF 3

SW1	SW2	LED1	LED2	IN1	IN2	AN	SND
23	22	21	20	19	18	17	

TF 4

A B C D E F G H J A B C D

FOLDOUT FRAME

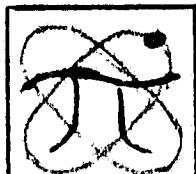


FOLDOUT FRAME

2

1458

- (1) PULSE DETECT OUT
- (2) PULSE DETECT IN
- (3) FILTER OUT
- (4) FILTER IN
- (5) AGC
- (6) D/A OUT



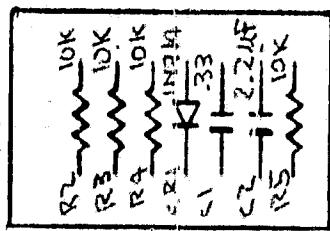
TECHNOLOGY INCORPORATED
LIFE SCIENCES DIVISION
HOUSTON, TEXAS 77058

DRAWN BY M.H. UTLEY	DATE 9-30-79	TITLE 8080A-BASED CARDIOTACHOMETER COMPONENT LAYOUT INTERFACE BOARD
DESIGN ENG. J.A. DONALDSON	11-14-79	
PROJ. ENGI. W.G. CROSIER	11-14-79	DWG. NO. MPCT-2009-L

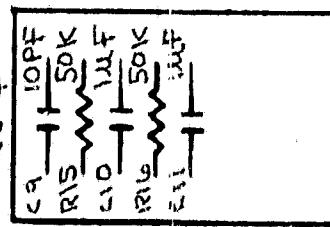
SHEET

1 OF 2

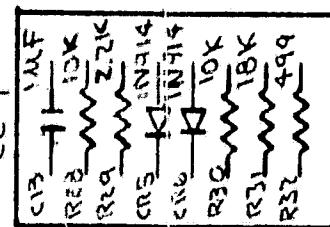
CC 1



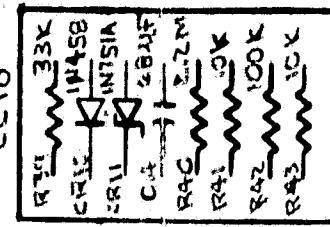
CC 4



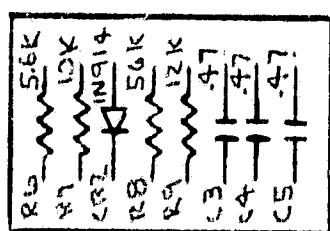
CC 7



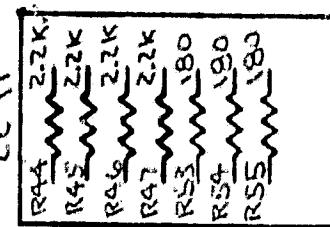
CC 10



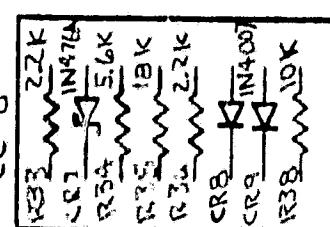
CC 2



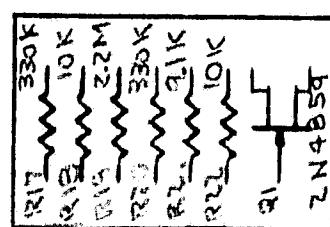
CC 11



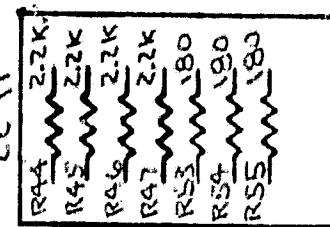
CC 8



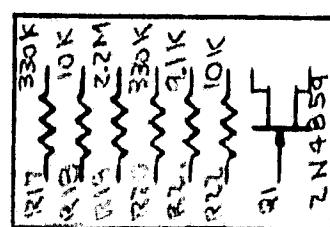
CC 5



CC 9

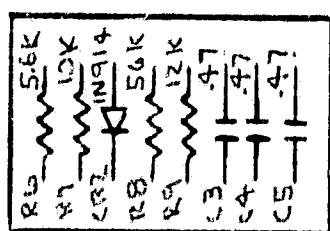


CC 6



WOLDOUT FR 111

CC 3



WOLNICH MP 1977

J



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LIFE SCIENCES DIVISION
HOUSTON, TEXAS 77058

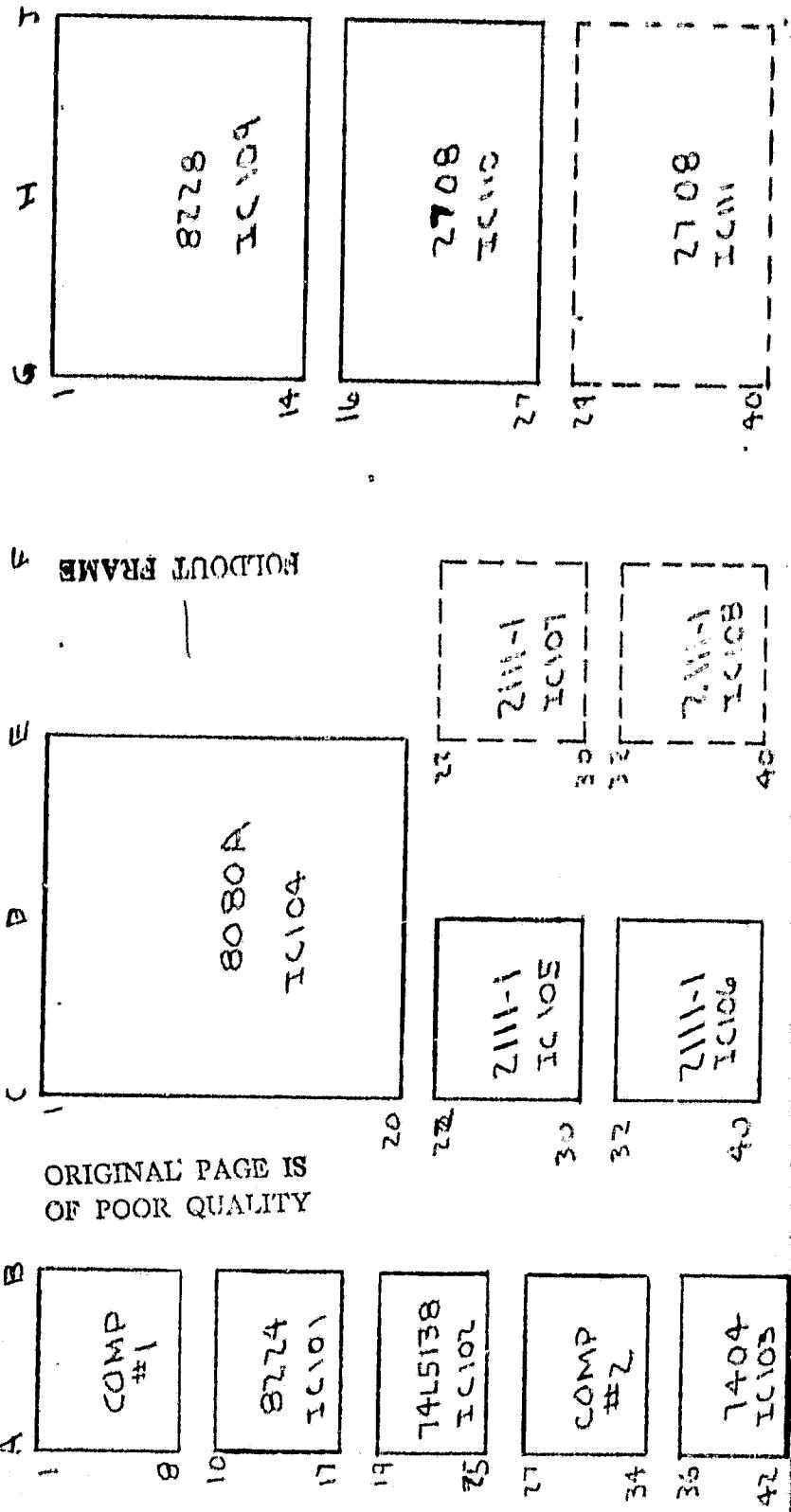
DRAWN BY M. H. UTLEY	DATE 9-28-79	TITLE 8080 A - BASED CARDIOTACHOMETER COMPONENT LAYOUT -INTERFACE BOARD
DESIGN ENG J.A. DONALDSON	11-14-79	DWG. NO. MPCT-2009-L
PROT. ENG, W. G. CROSLER	11-14-79	SHEET 2 OF 2

+12 •1 24•-12

RESET-H • •-5
M RESET-L • •OSC
• • INT
• • RESET
• •
+12 • •-12

CPU C
CPU D
CPU E
CPU F
CPU G
CPU H

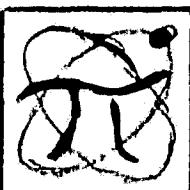
A2 • •A3
A1 • •WR
A0 • •RD
D3 • •D4
D2 • •D5
D1 • •D6
D0 •23 46•D7



ORIGINAL PAPER IS

POLYDOUT FRAME
2

NOTES: (1) DASHED LINES INDICATE LOCATIONS FOR IC'S TO BE ADDED LATER FOR FUTURE EXPANSION, IF NECESSARY.



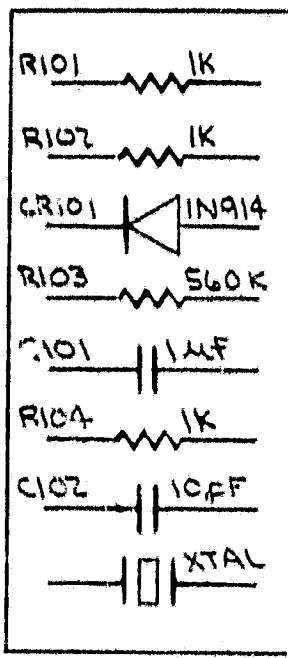
TECHNOLOGY INCORPORATED
LIFE SCIENCES DIVISION
HOUSTON, TEXAS 77058

DRAWN BY M.H.UTLEY	DATE 10-17-79	TITLE BOBORA-BASED CARTRIDGE TACHOMETER COMPONENT LAYOUT CPU BOARD
DESIGN ENG J.A.DONALDSON	11-14-79	DWG. NO. MPCT-2011-L
PROB. ENG W.G.CROSIER		SHEET 1 OF 2

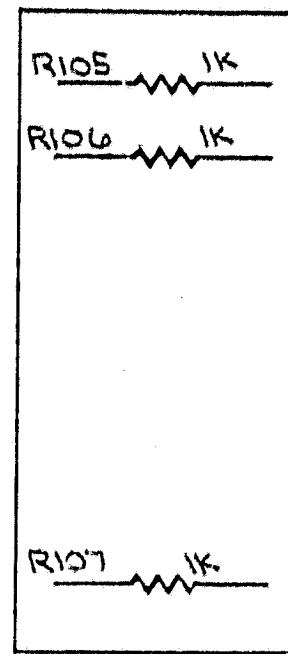
COMP
#

59

44

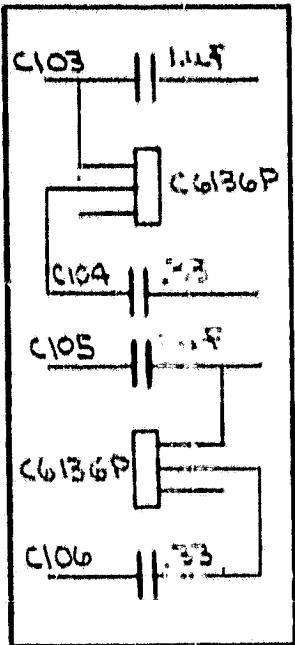


COMP 1



COMP 2

BUILDOUT FRAME



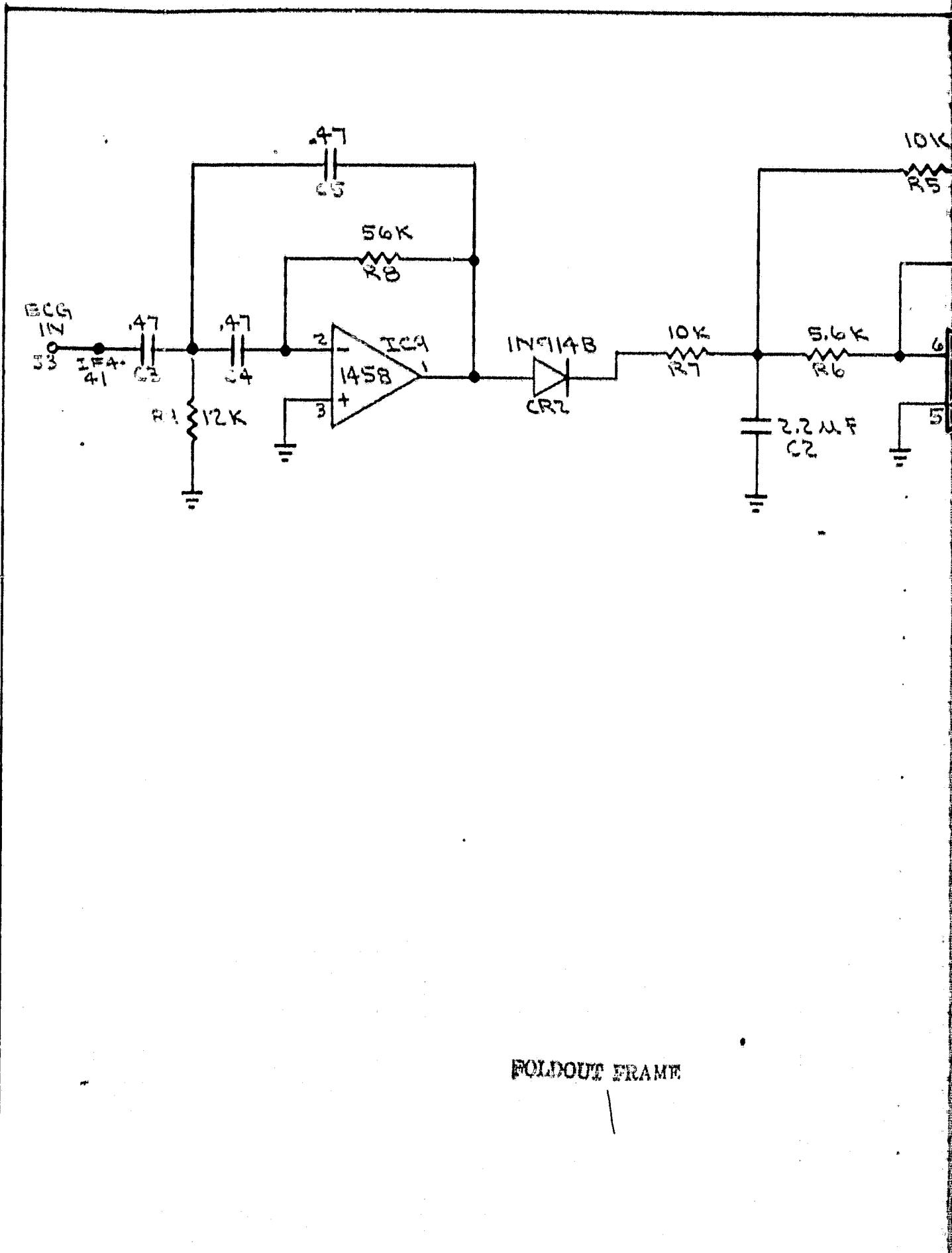
COMP 3

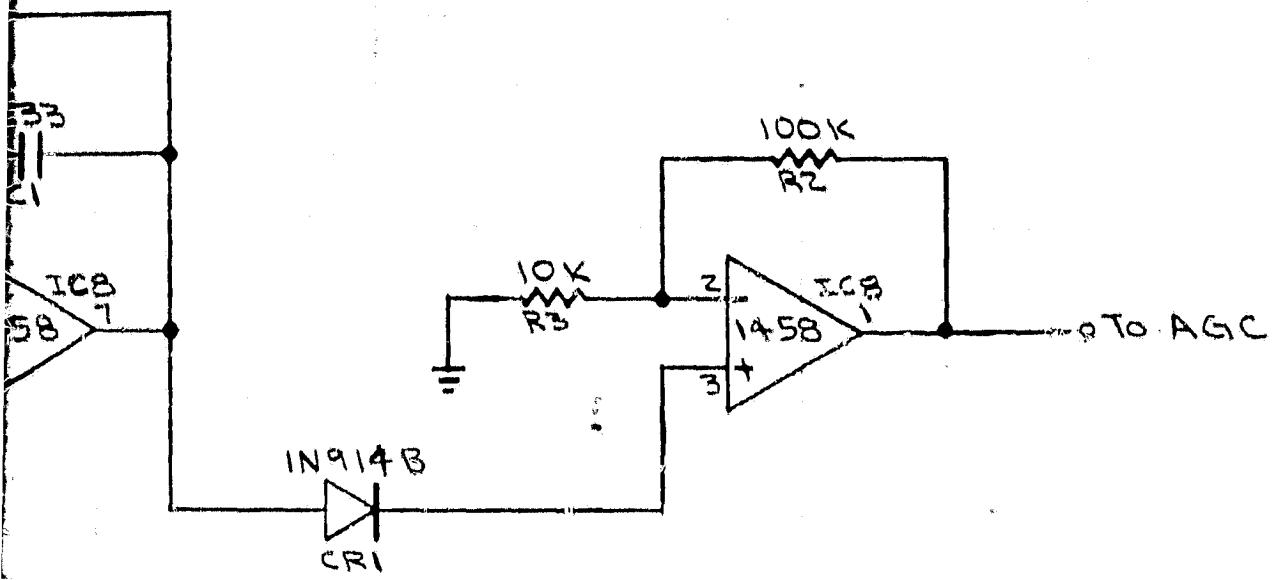
FOLDOUT FRAME

2

	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058		
DRAWN BY M.H.UTLEY	DATE 10-16-79	TITLE 2080 A - SF-560 CARDIOTACHOMETER COMPONENT LAYOUT CPU BOARD	
DESIGN ENG. J.A. DONALDSON	11-14-79	DWG. NO. MPCT-2011-L	
PROJ. ENG. W.G. CROSIER	11-14-79	SHEET 2 OF 2	

APPENDIX F

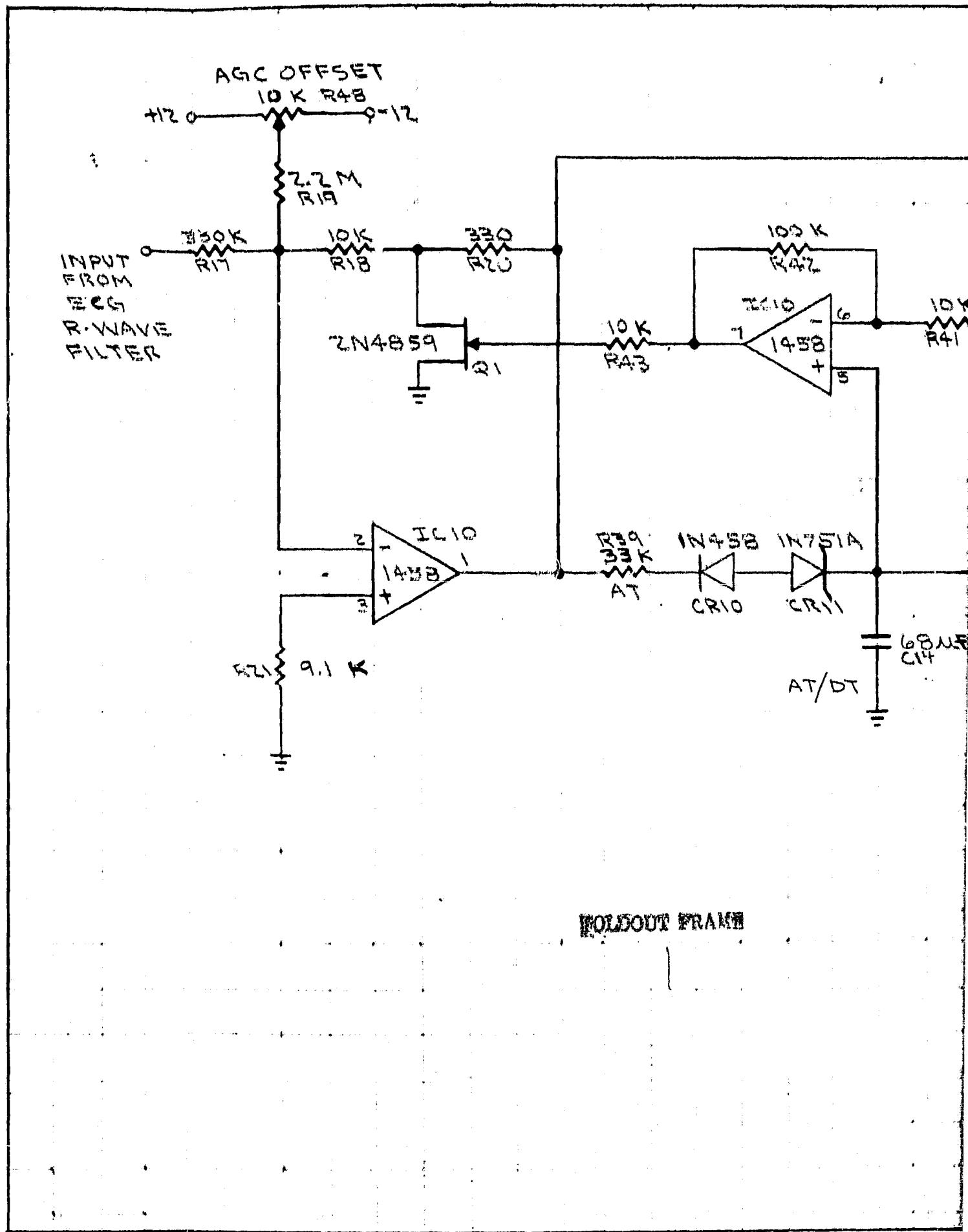


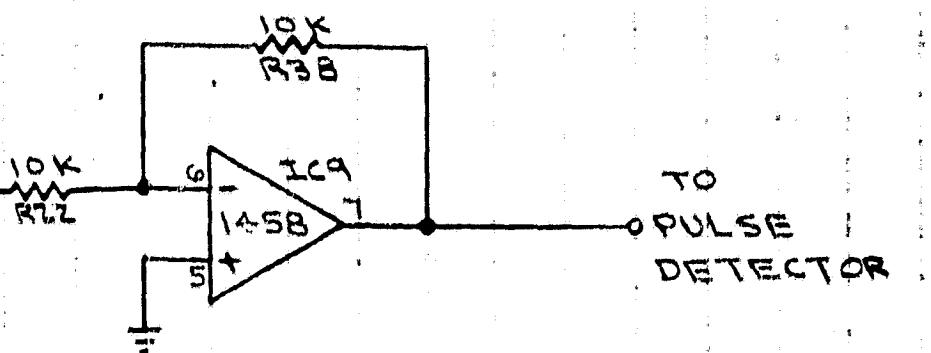


FOLDOUT FRAME

2

	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058		
DRAWN BY M. H. UTLEY	DATE 9-29-79	TITLE BOB0A - BASED CARDIOTACHOMETER ECG - R - WAVE FILTER	
DESIGN ENG. J. A. DONALDSON	11-14-79		
PROJ. ENG W. G. CROSIER	11-14-79	DWGS. NO MPCT - ZOO1-5	
		SHEET 1 OF 1	



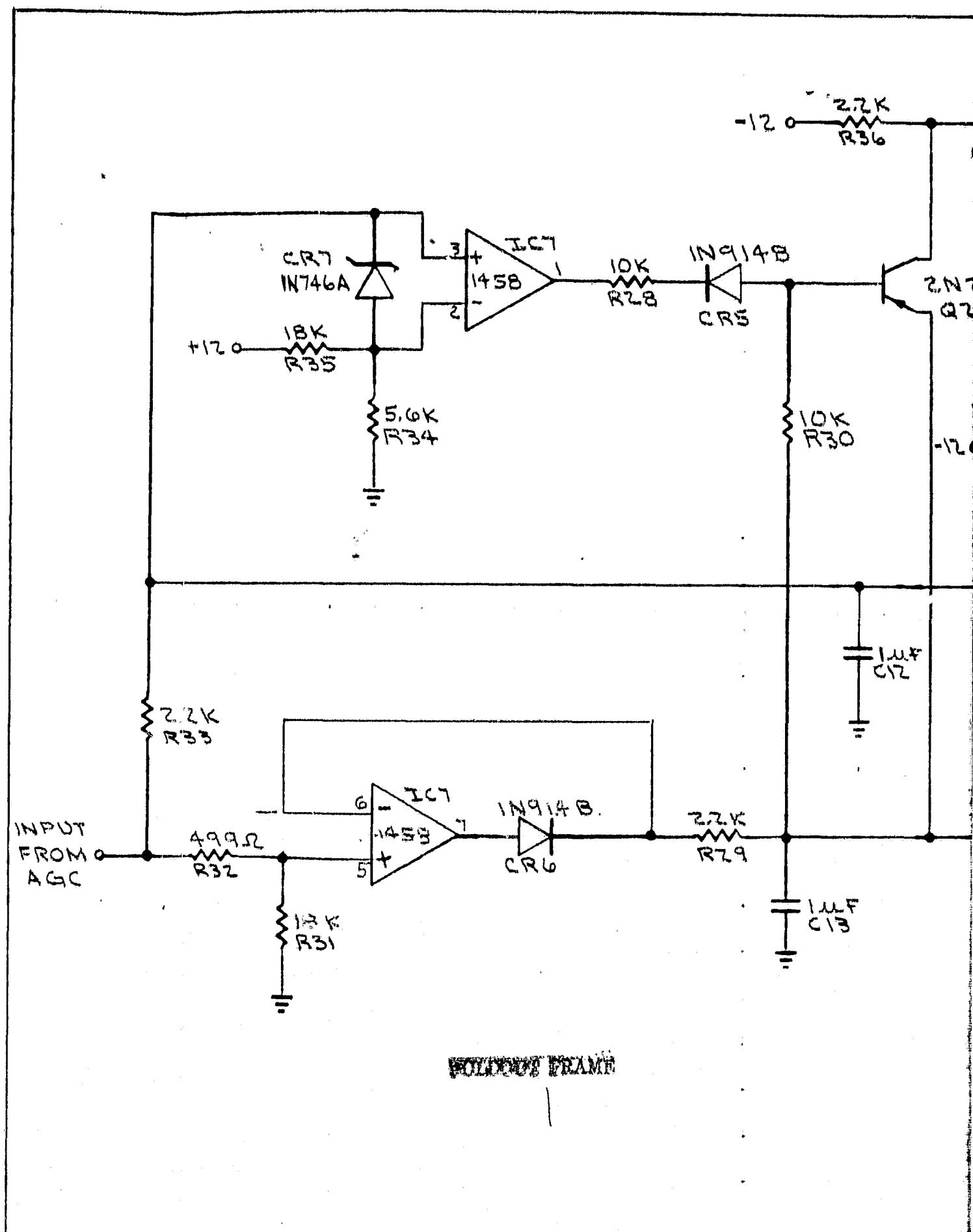


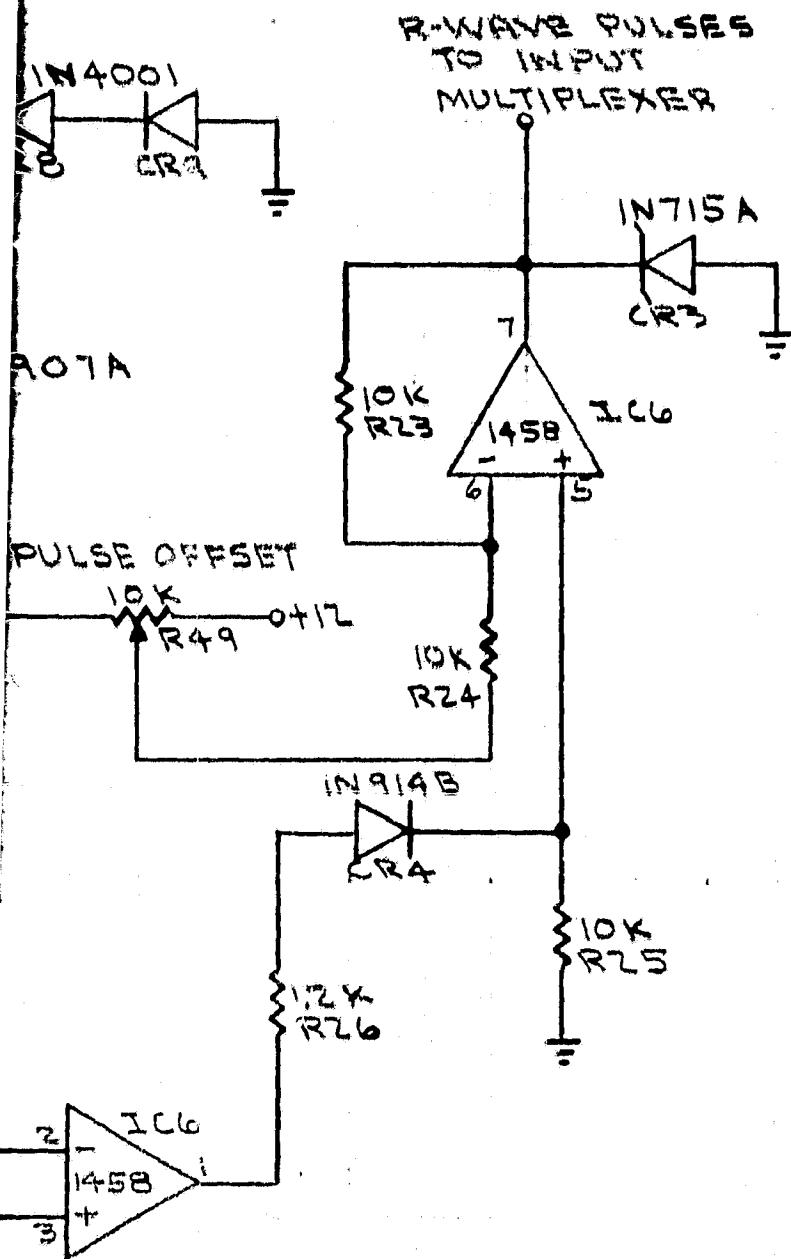
R40
2.2 M
DT

FOLDOUT FRAM

2

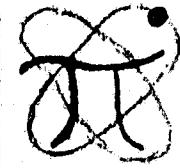
	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058	
DRAWN BY M. H. UTLEY	DATE 9-26-79	TITLE BOBOPA - BASED CARDIOTACHOMETER AUTOMATIC GAIN CONTROL
DESIGN ENG. J. A. DONALDSON	11-14-79	PROJ. ENG.
		DWG. NO. MPCT-2002-5
		SHEET 1 OF 1





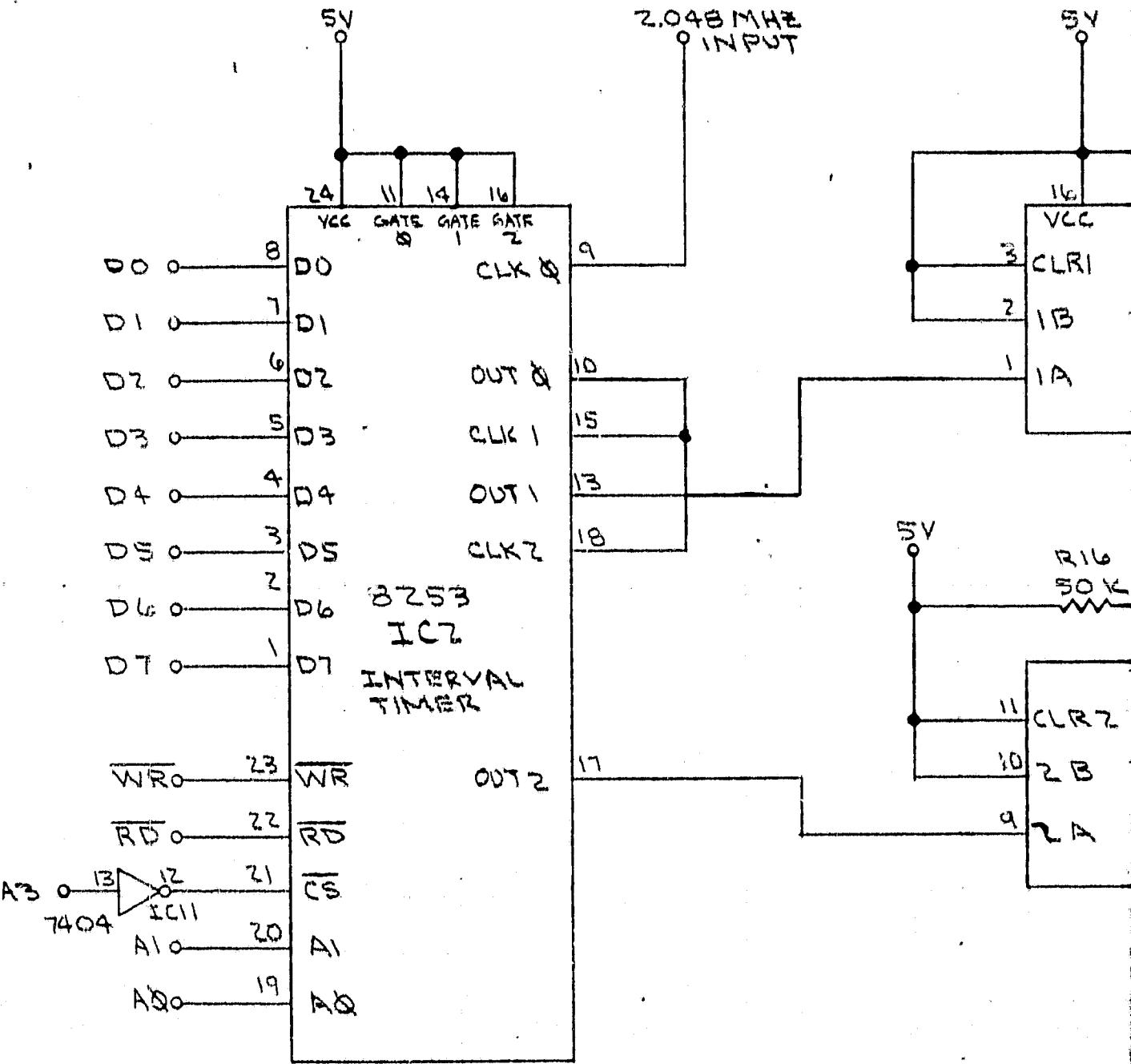
BOLDOUT FRAME

2

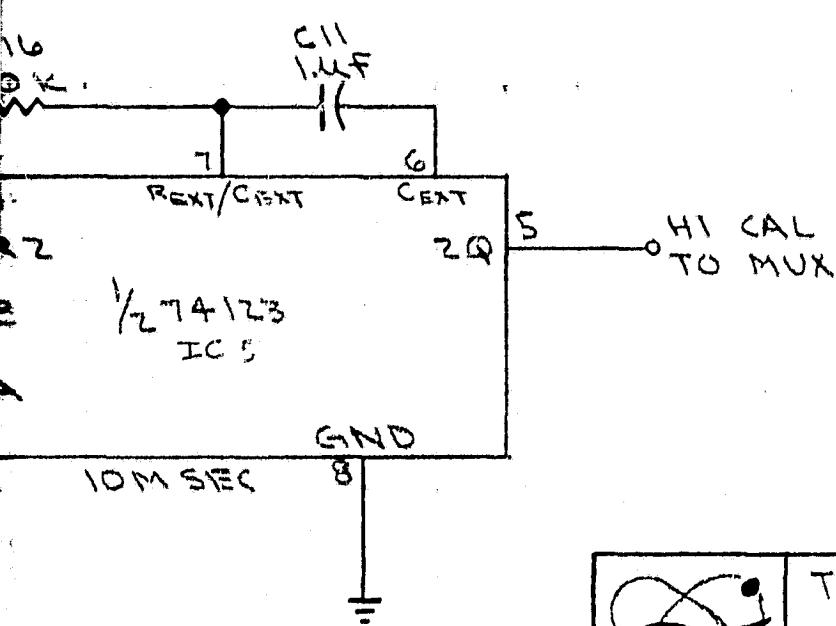
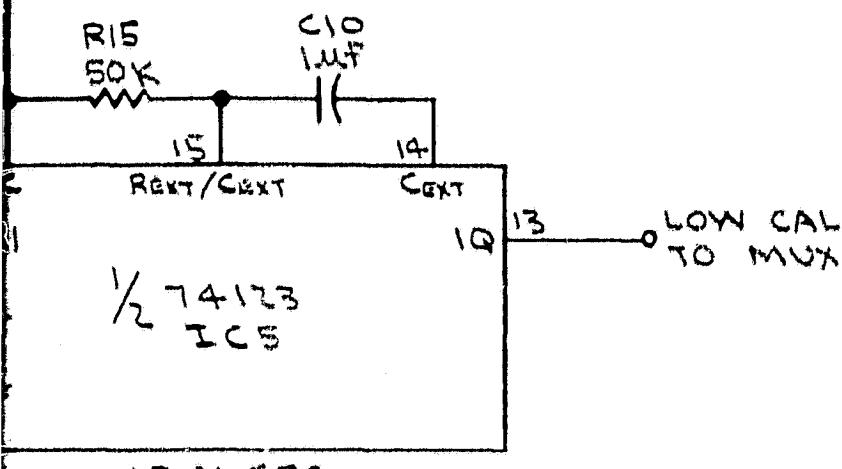


TECHNOLOGY INCORPORATED
LIFE SCIENCES DIVISION
HOUSTON, TEXAS 77058

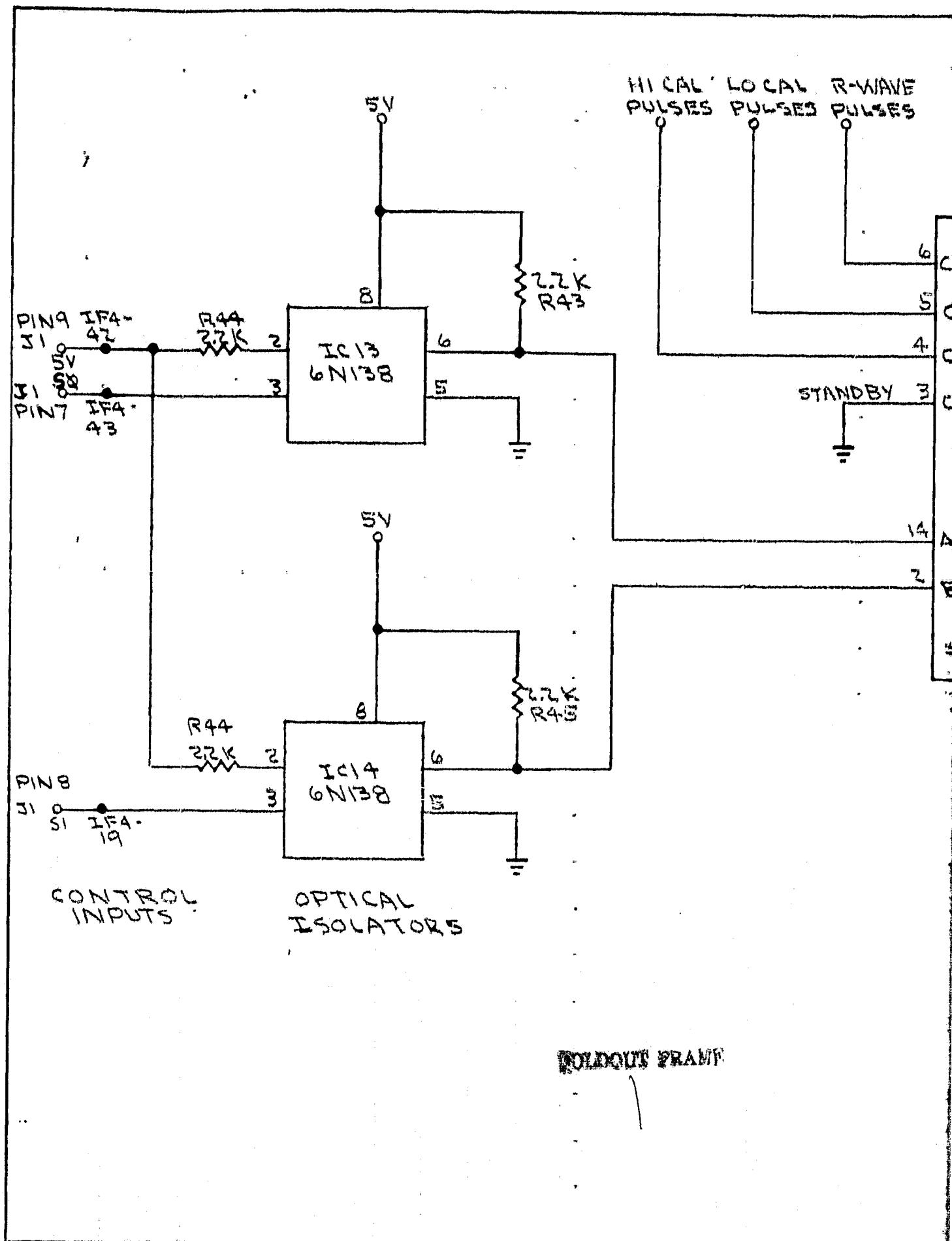
DRAWN BY M. H. UTLEY	DATE 9-21-79	TITLE BOBOSA - BASED CARDIOTACHOMETER PULSE DETECTOR
DESIGN ENG J. A. DONALDSON	11-14-79	DWG. NO MPCT - 2.003 - S
PROJ. ENG W. G. CROSIER	11-14-79	SHEET 1 OF 1

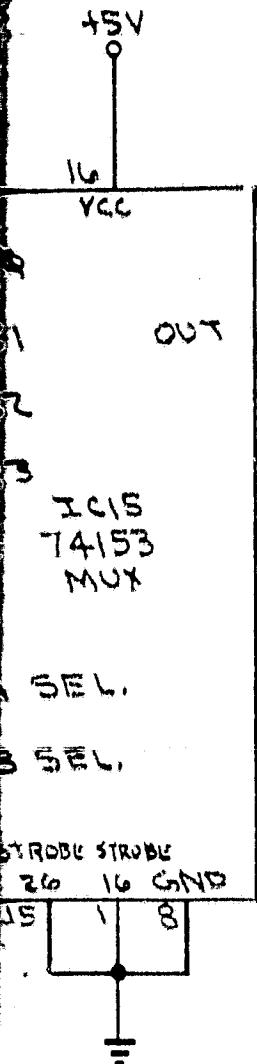


VIDEO RAM



	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058		
DRAWN BY M.H. UTLEY	DATE 10-13-79	TITLE 8080 A - BASED CARDIOTACHMETER LO-HI CAL PULSE GENERATOR	
DESIGN ENG. J.A. DONALDSON	11-14-79	DRAWG. NO. MAPCT-2004-5	
PROS. ENG. W.G. CROSIER	11-14-79	SHEET 1 OF 1	





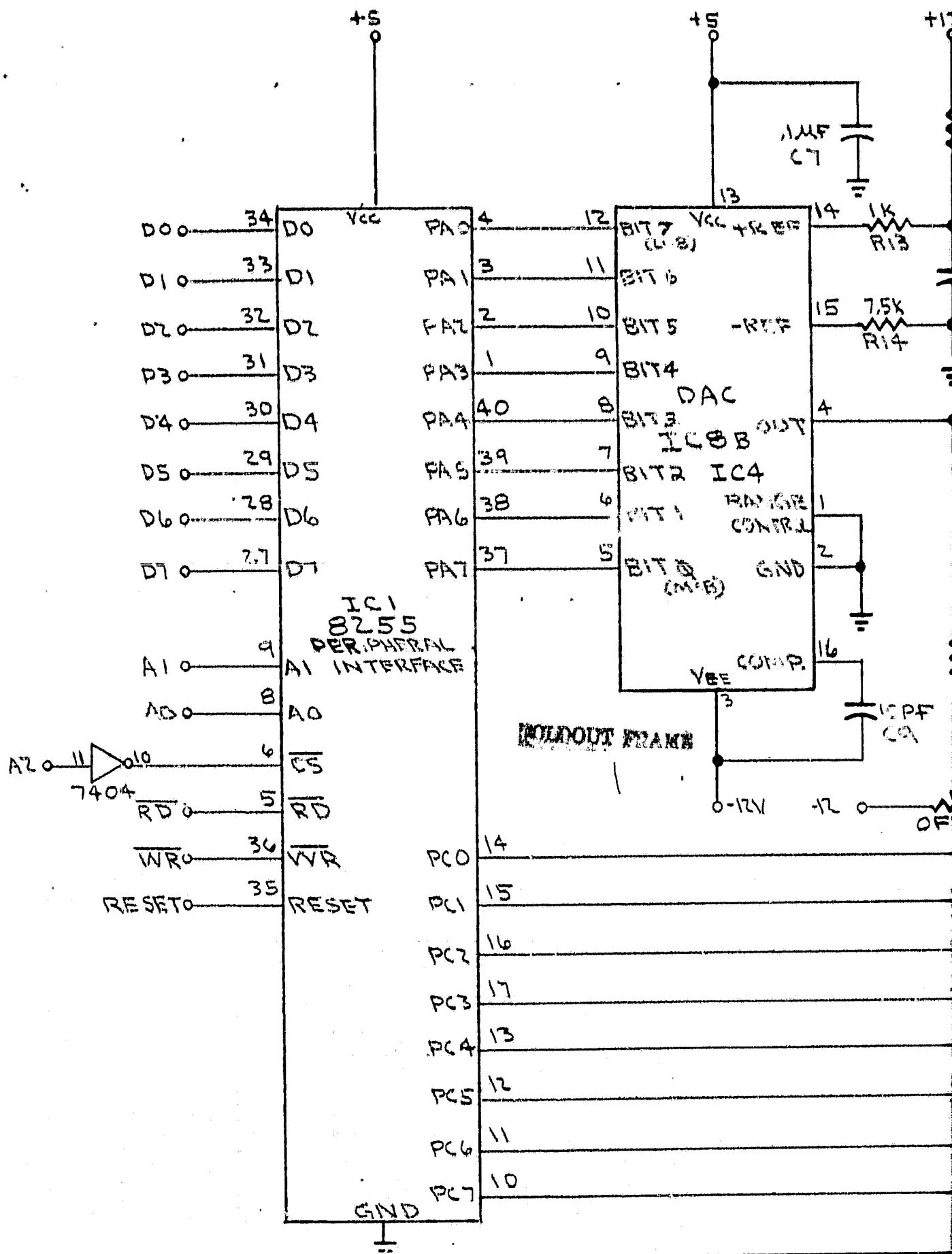
OTO DIGITAL INTERFACE
8255 - PIN PLD

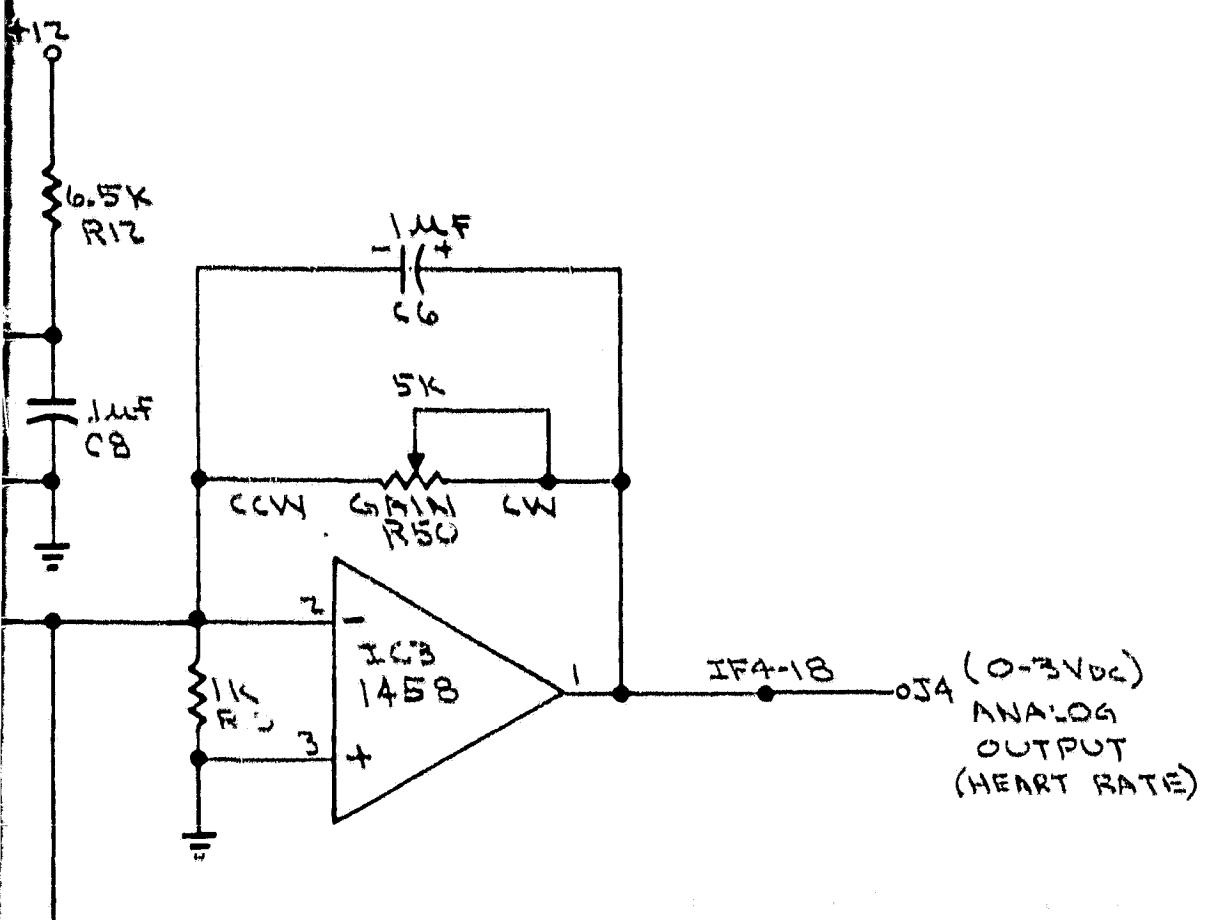
CONTROL INPUTS		74153
S ₂	S ₁	OUTPUT
0	0	ECG
1	0	LO CAL
0	1	HI CAL
1	1	STAND BY

BOLDOUT FRAM:

J

	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058		
DRAWN BY M.H. UTLEY	DATE 10-12-79	TITLE 8030 A - BASED CARDIOTACHOMETER COMPUTER CONTROL & INPUT MULTIPLEXER	
DESIGN ENGI. J.A. DONALDSON	11-14-79	DWG. NO. MPCT-2005-S	
PROJ. ENG. W.G. CROISIER	11-14-79	SHEET 1 OF 1	





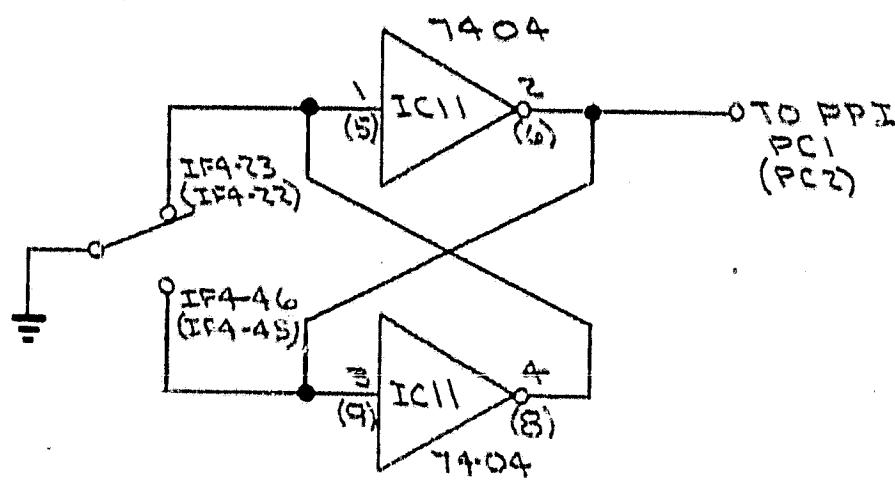
PULLDOWN FRAME

2

- ECG/CAL IN
 - SW1 IN
 - SW2 IN
 - SPARE IN
 - LED2 OUT (UNDER)
 - LED3 OUT (OVER)
 - SPARE OUT
 - SPARE OUT
- R51
10K
OFFSET → +12

	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058		
DRAWN BY M.H.UTLEY	DATE 10-6-79	TITLE 8080 A - BASED CARDIOTACHOMETER DIGITAL I/O AND ANALOG OUTPUT INTERFACE	
DESIGN ENG J.A. DONALDSON	11-14-79	DRAW. NO. MPCT-2006-S	
		SHEET 1 OF 1	

UNDER RANGE PC4



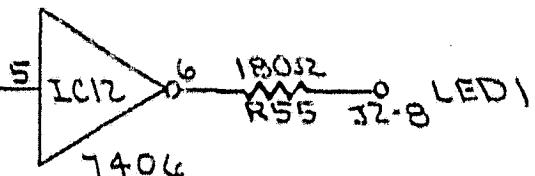
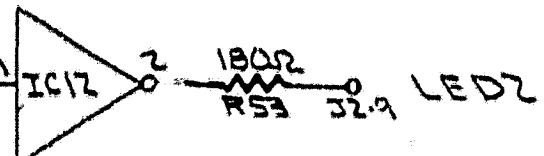
OVER RANGE PC5

ECG/CAL PC0

SYSTEM CALIBRATE 1 & 2
IN PUT & DEBOUNCE

LED

POT/DOUT FRAM



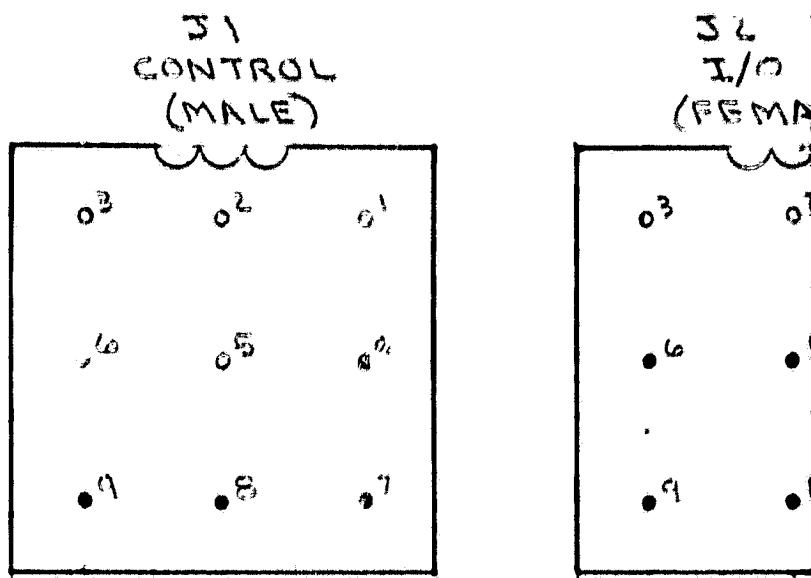
D OUTPUT DRIVERS

~~NO LOAD FLAME~~

3

		TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058		
DRAWN BY M.H. UTLEY	DATE 10-13-79	TITLE 8080A - BASED CARTIOTACHOMETER CAL. 1F2, INPUT OF BOUNCE AND LED OUTPUT DRIVERS		
DESIGN ENG. J.A. DONALDSON	11-14-79	DRAWG. NO. MPCT-2007-5		
PROJ. ENG W.G. CROSTIER	11-14-79	SHEET 1 OF 1		

EXTERNAL VIEW
PIN SIDE - VANEEL C.G.



(1) SPARE

(2) SPARE

(3) SPARE

(4) GND

(5) SPARE

(6) SPARE

(7) IN1 (CSR 0)

(8) IN2 (CSR 1)

(9) +5V_H

(1) SPARE

(2) SPARE

(3) SPARE

(4) RES

(5) GND

(6) LED

(7) GND

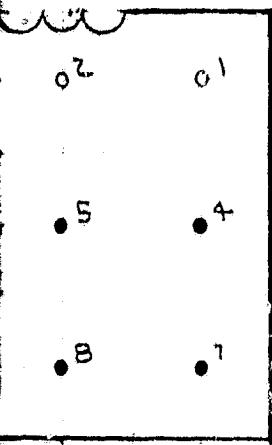
(8) LED

(9) LED

FOLDOUT FRAME

CONNECTOR

10
FEMALE)



PART

PART

PART

ESRT

PART

ED 3 (OVER RANGE)

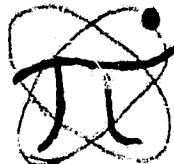
ND

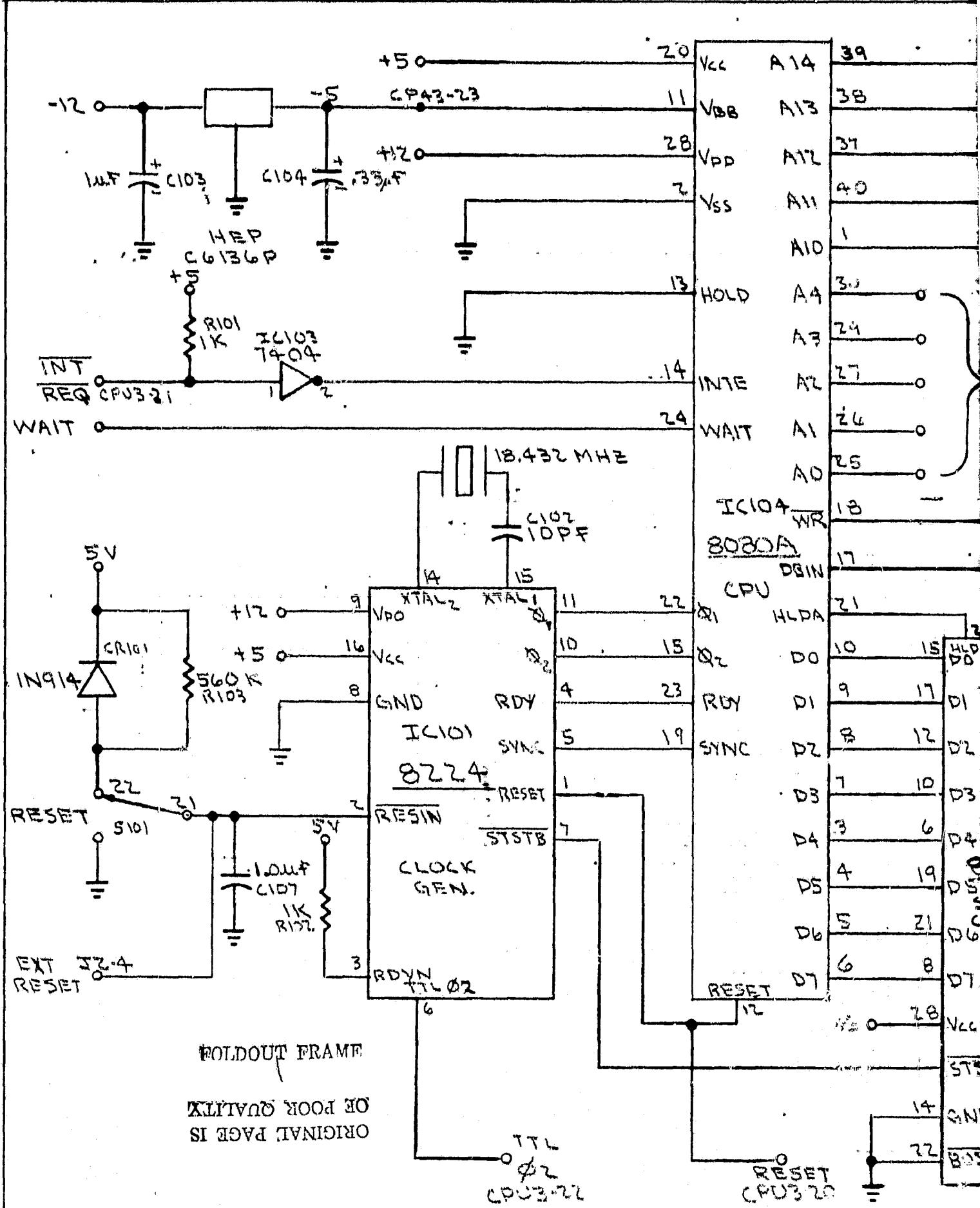
ED 1 (ECG/CAL)

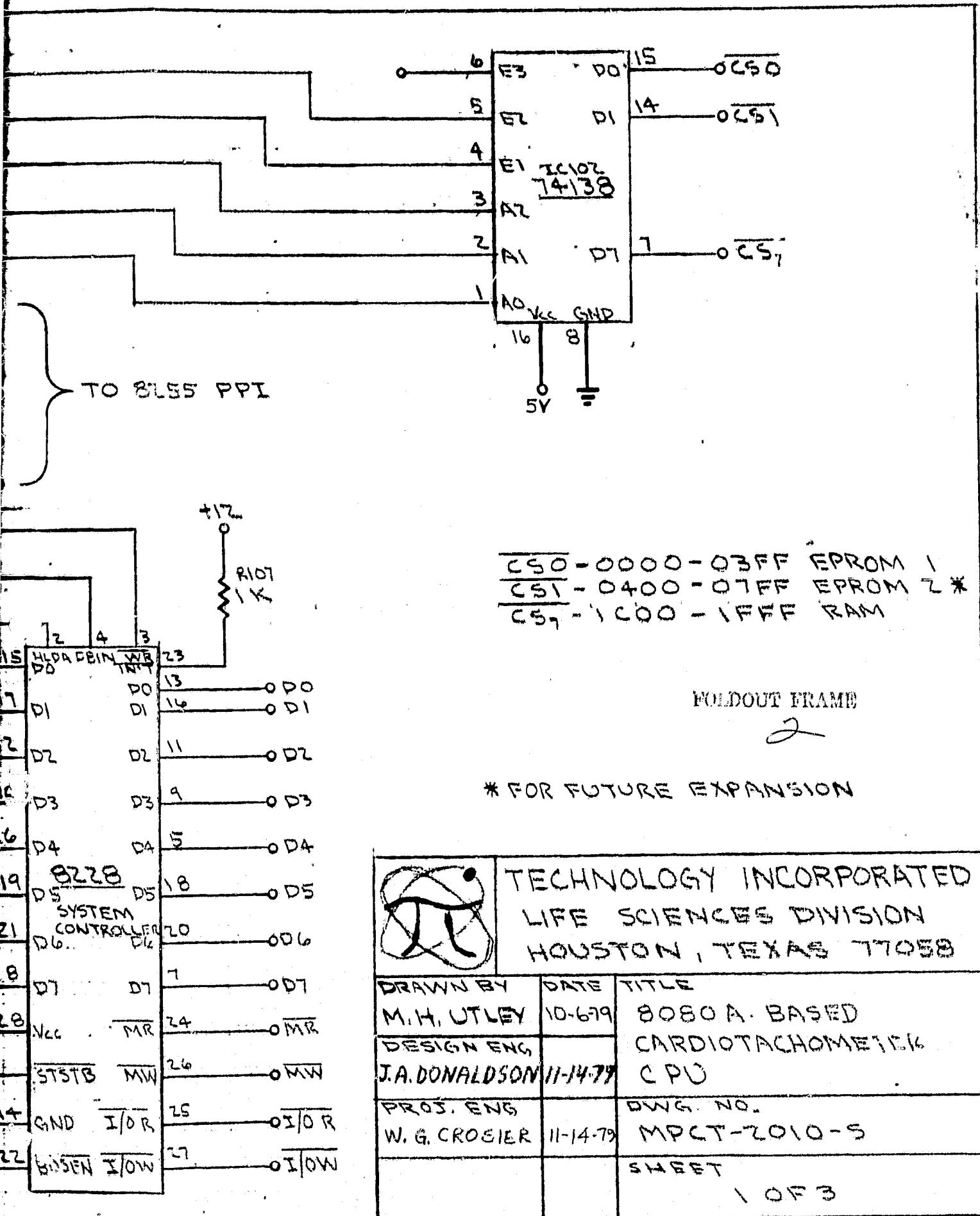
ED 2 (UNDER RANGE)

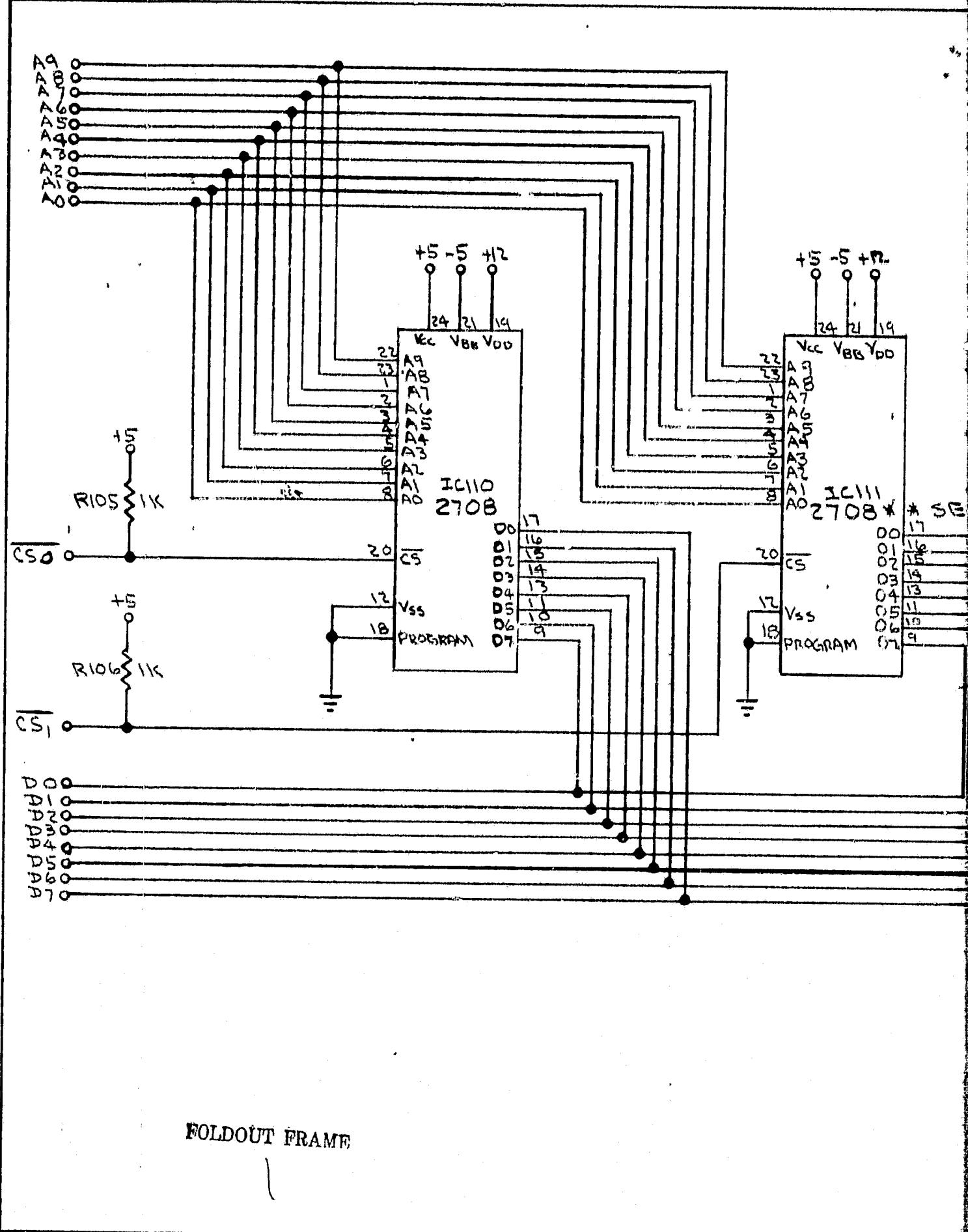
SOLIDOUT FRAME

2

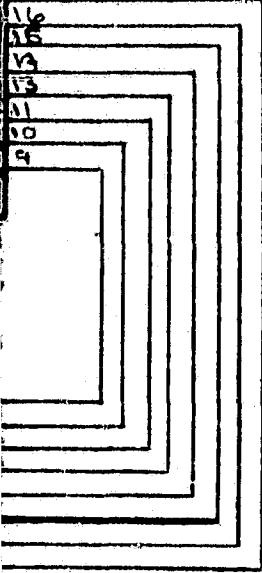
		TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058
DRAWN BY M. H. UTLEY	DATE 9-24-79	TITLE BOB0A-BASED CARDIOTACHOMETER CONTROL-I/O CONNECTOR
DESIGN ENG. J.A. DONALSON	11-14-79	PWG. NO. MPCT-2008-1
PROJ. ENG.		SHEET 1 OF 1







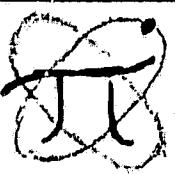
* SEE NOTE 1

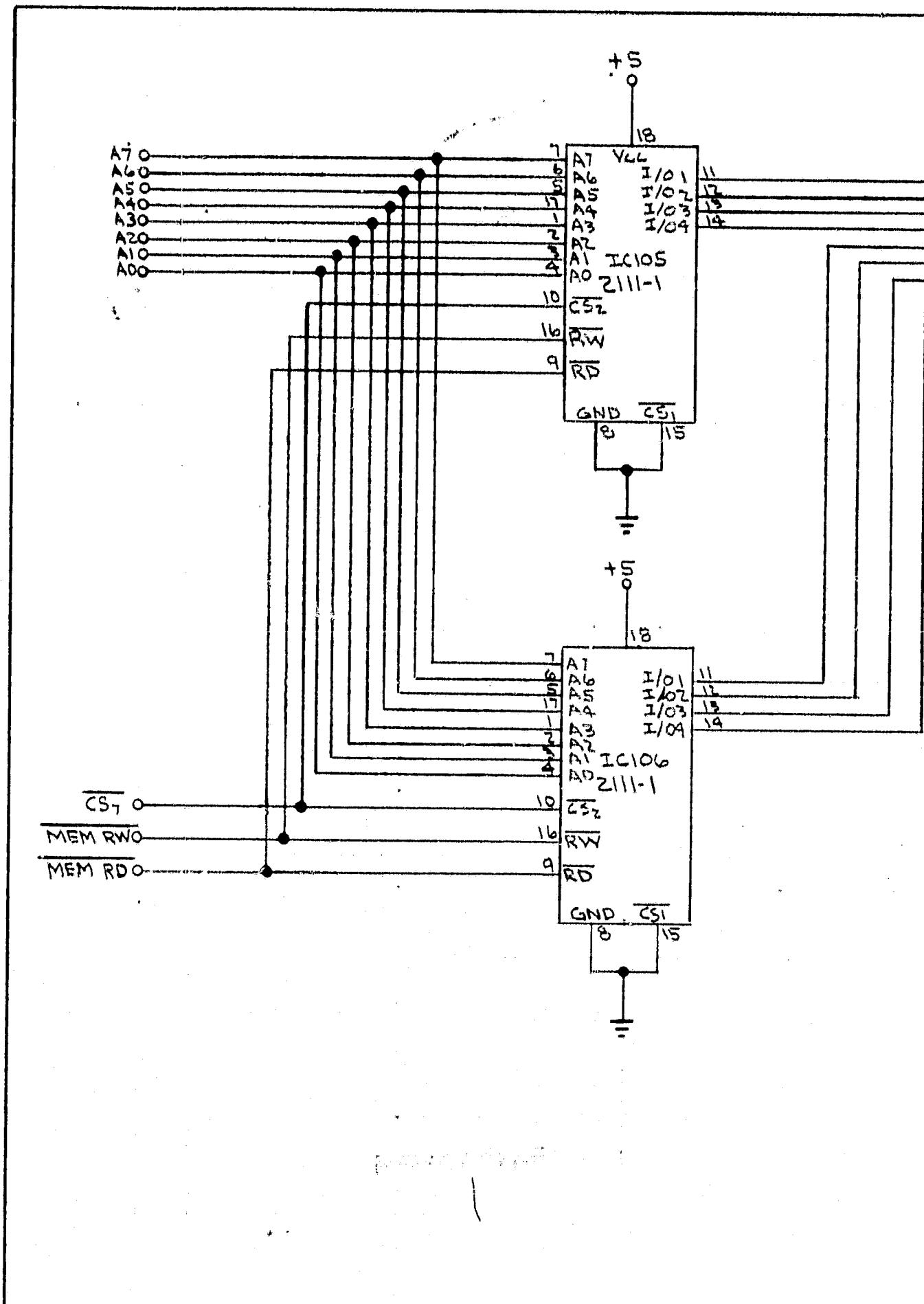


NOTES: (1) FOR FUTURE EXPANSION.

FOLDOUT FRAME

2

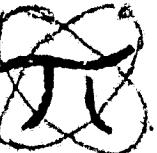
		TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058
DRAWN BY M.H. UTLEY	DATE 10-10-79	TITLE BOBOSA -BASED CARDIOTACHOMETER CPU
DESIGN ENG. J.A. DONALDSON	11-14-79	PROJ. ENG. W.G. CROSIER
		DING. NO. MPCT-2010-S
		SHEET 2 OF 3

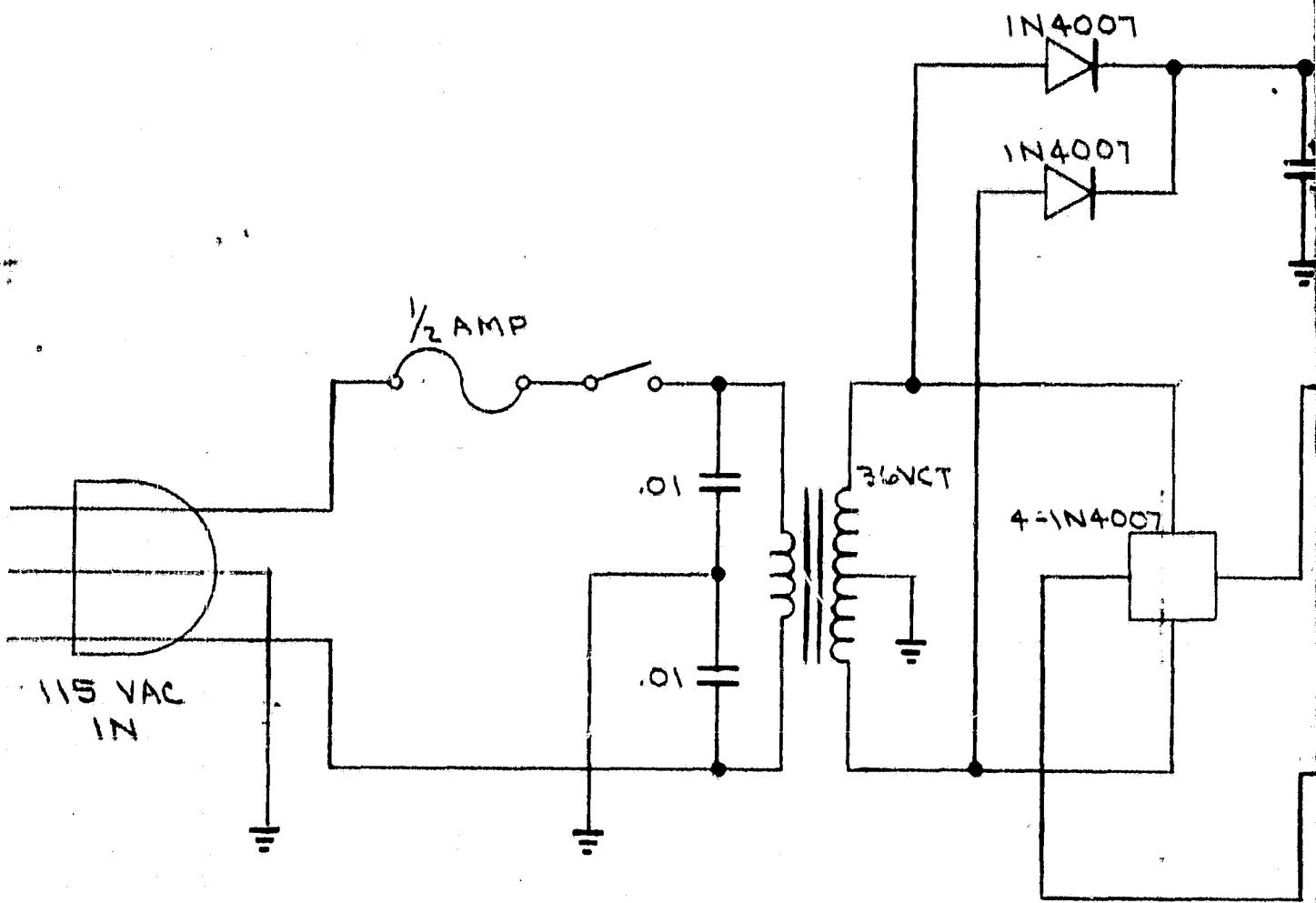


000
001
002
003
004
005
006
007

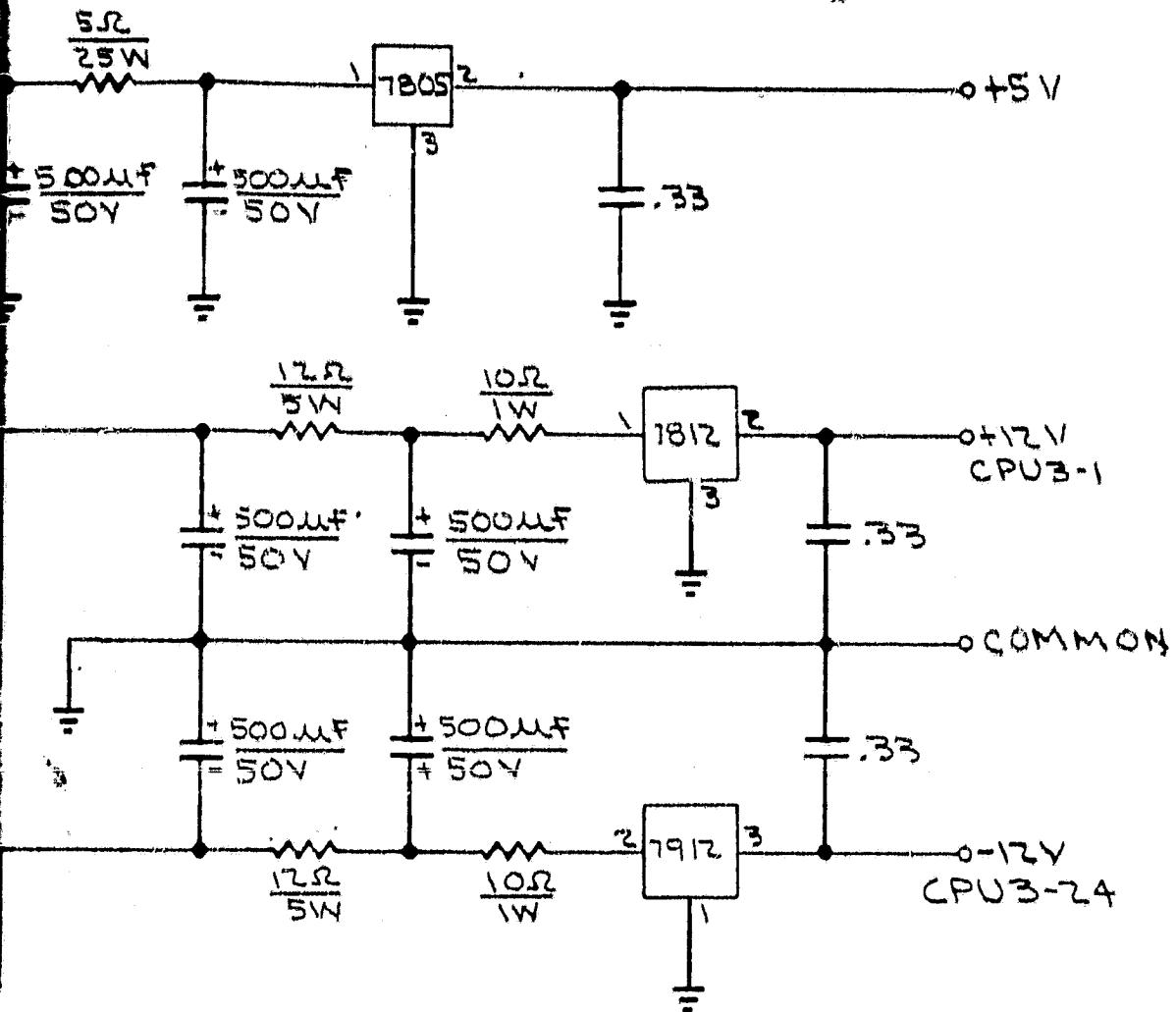
FULLDRAWN PRINT



	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058	
DRAWN BY M.H. UTLEY DESIGN ENG. J.A. DONALDSON	DATE 10-10-79 11-14-79	TITLE 8080 A-BASED CARDIOTACHOMETER CPU
PROJ. ENG. W.G. CROSIER		DWG. NO. MPCT-2010-S
		SHEET 3 OF 3



FOLDOUT FRAME



FOLDOUT FRAME

2

	TECHNOLOGY INCORPORATED LIFE SCIENCES DIVISION HOUSTON, TEXAS 77058	
DRAWN BY M.H. UTLEY	DATE 10-13-79	TITLE 8080A - BASED CARDIOTACHOMETER
DESIGN ENGI. J.A. DONALDSON	11-14-79	POW. & SUPPLY
PROJ. ENG W.G. CROISIER	11-14-79	DWG. NO. MPCT-2012-5
		SHEET 1 OF 1

APPENDIX G

APPENDIX C
SAMPLE OUTPUT

