APPLICATION OF A MICROPROCESSOR TO A SPACECRAFT ATTITUDE CONTROL

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The space-qualified TDRSS attitude control system (ACS) microprocessor development work spanned three main design areas: hardware and instruction set, ACS firmware, and hardware/firmware verification testing.

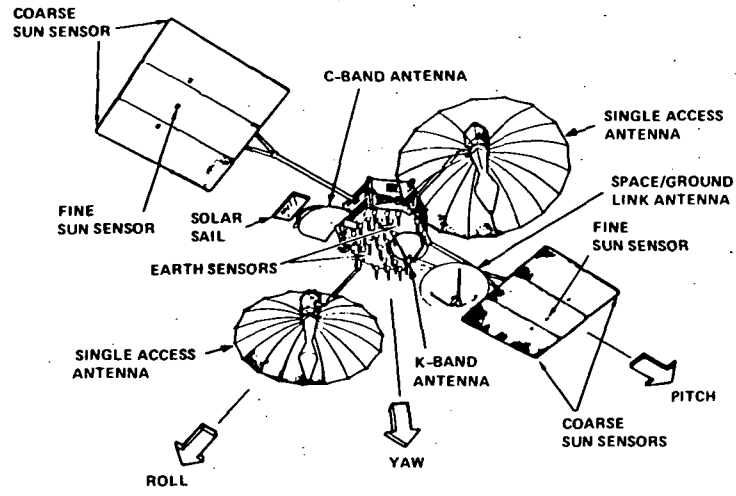
The Control Processor Electronics (CPE) hardware utilizes two parallel AM2901 4-bit microprocessors, with a microprogrammed instruction set tailored to the TDRSS controls application. Fourteen special purpose I/O instructions interface with the ACS hardware, each transferring data for one sensor while meeting timing and data-handling requirements. The ACS firmware resides in 5120 bytes of ROM with 1024 bytes of RAM for scratch data storage. The 16-bit add, subtract, and divide operations are overflow-protected and multiplies are done in hardware.

The firmware includes data processing for five sensors, four attitude control laws, and telemetry and commands. The main design limitations were: 16-bit word length, 1024 8-bit byte RAM, and computation speed/task sharing tradeoffs. It performed ACS computations quickly and without significant data degradation. The word length limitation motivated the careful selection of control filter topology and sacrifice of dynamic range in favor of null performance.

The flight program design was tested with three tools: Varian V-73 minicomputer, CDC Cyber computer, and the CPE development station. The V-73 simulation tested source (assembly) programs prior to development station availability. The CDC Cyber simulation was used primarily for accuracy analysis. The development station included commercial versions of the flight hardware which were run at full speed. All formal verification tests were run on the development station to verify timing, accuracy, and interface requirements.

From this development experience, additional hardware and software requirements were identified:

- Rapid Memory Examine/Change
- Floating point hardware
- High level language



TDRSS SPACECRAFT CONFIGURATION

TRACKING AND DATA RELAY SATELLITE (TDRSS) MISSION:

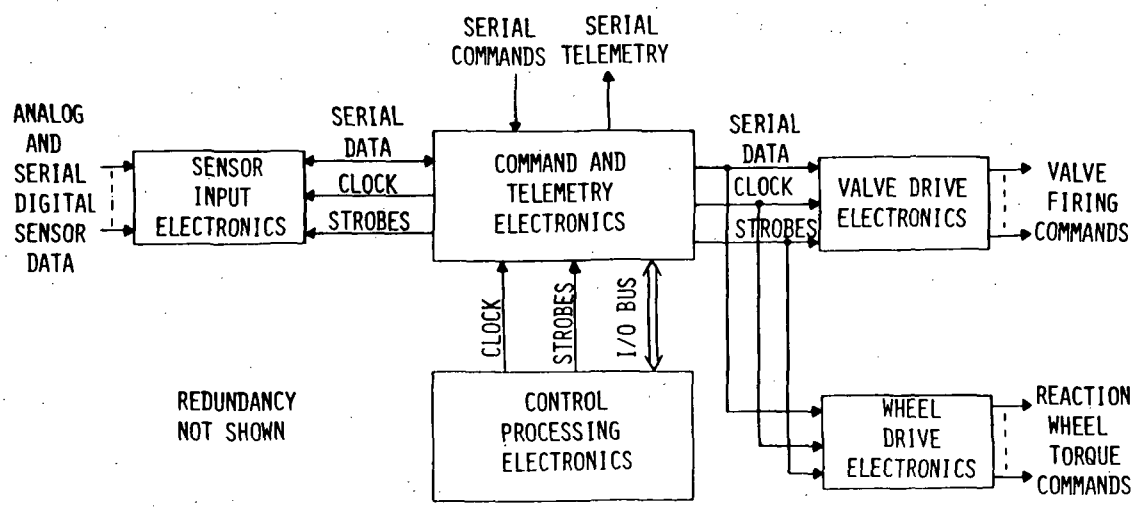
- COMMERCIAL COMMUNICATION FOR WESTERN UNION
- SATELLITE TRACKING AND DATA RELAY FOR NASA

- TDRSS IS ONE RECENT TRW APPLICATION OF THE USE OF A MICROPROCESSOR TO PERFORM SPACECRAFT ATTITUDE CONTROL SYSTEM COMPUTATIONS
- DEVELOPMENT WORK SPANNED THE FOLLOWING AREAS:
  - HARDWARE DESIGN OF THE CONTROL PROCESSING ELECTRONICS (CPE), A SPECIAL-PURPOSE MICROCOMPUTER BASED ON THE AMD 2901 BIT-SLICE MICROPROCESSOR
  - DEFINITION OF THE INSTRUCTION SET
  - DESIGN AND CODE THE FIRMWARE FLIGHT PROGRAM
  - VERIFICATION TESTING OF THE FIRMWARE

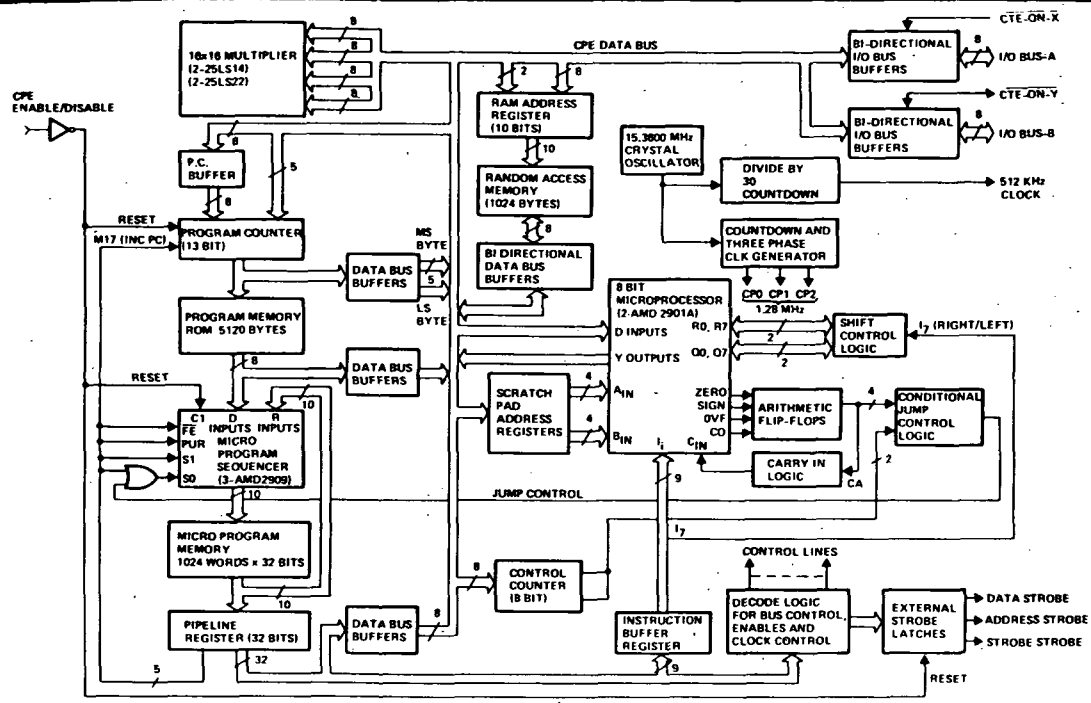
TDRSS ATTITUDE CONTROL HARDWARE

- CONTROL ELECTRONICS ASSEMBLY
- SENSORS
  - EARTH SENSOR
  - COARSE SUN SENSORS
  - FINE SUN SENSORS
  - GYROS
  - REACTION WHEEL TACHOMETERS
  - SOLAR ARRAY DRIVE RESOLVERS
- ACTUATORS
  - THRUSTERS
  - REACTION WHEELS

TDRSS CONTROL ELECTRONICS ASSEMBLY



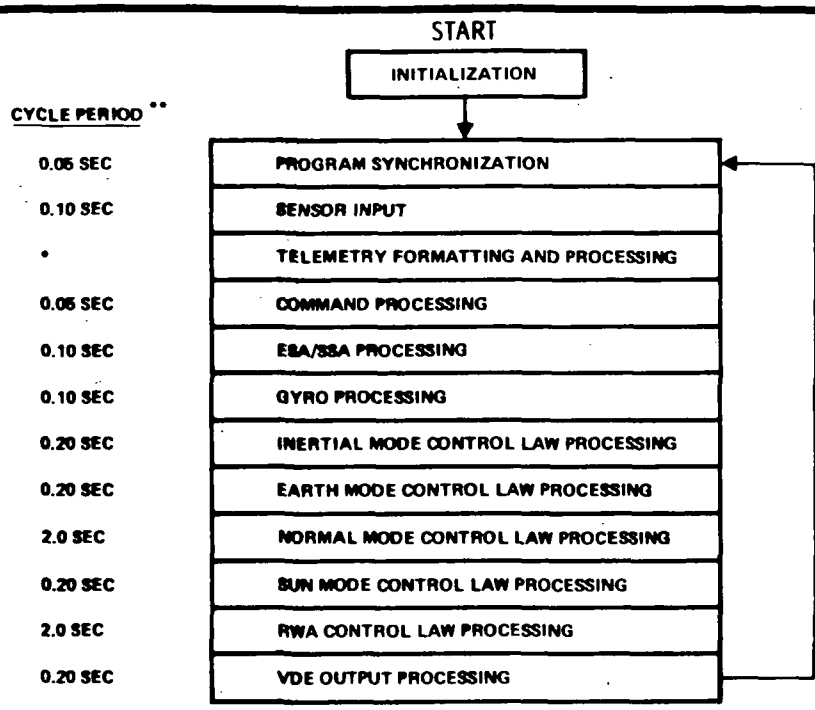
CPE BLOCK DIAGRAM



CPE INSTRUCTION SET

- SPECIFIED BY CPE CONTROL FIRMWARE DESIGNERS TO BE OPTIMUM FOR TDRSS APPLICATION
- INSTRUCTION SET MICROPROGRAMMED BY HARDWARE DESIGNERS
- 108 TOTAL INSTRUCTIONS INCLUDING:
  - SINGLE- OR MULTIPLE-BIT SET, RESET AND TEST
  - 16-BIT FRACTIONAL FIXED-POINT ARITHMETIC
  - 16-BIT ADD, SUBTRACT AND DIVIDE CLAMPED AT ± 1.0 WHEN OVERFLOW OCCURS
  - MULTI-BIT LOGICAL AND ARITHMETIC SHIFTS (SINGLE AND DOUBLE-PRECISION)
  - FOURTEEN INPUT/OUTPUT INSTRUCTIONS DEDICATED TO PARTICULAR SENSORS OR ACTUATORS WITH ALL HARDWARE TIMING BEING TAKEN CARE OF IN THE MICROCODE. FOR EXAMPLE, INSS INSTRUCTION INPUTS ALL DATA ASSOCIATED WITH THE COARSE AND FINE SUN SENSORS TO PAGE 0 OF RAM; OUWTQ OUTPUTS TORQUE COMMANDS TO THE REACTION WHEELS FROM PAGE 0 OF RAM.

PROGRAM STRUCTURE



*TELEMETRY BIT RATES OF 250, 1000, AND 4000 BITS/SECOND ARE SELECTABLE FOR THE 512 BIT MAIN FRAME. THESE PRODUCE TELEMETRY CYCLE TIMES OF 2.048, 0.512, AND 0.128 SECONDS RESPECTIVELY.

**EXECUTION FREQUENCY (NOT EXECUTION TIME) FOR EACH PROGRAM MODULE.

FIRMWARE DEVELOPMENT/VERIFICATION PHILOSOPHIES

DESIGN SCOPE -

- MICROPROCESSOR DEDICATED TO ATTITUDE CONTROL FUNCTION
- INSTRUCTION SET TAILORED TO CONTROL NEEDS (ARITHMETIC LIMITING, CONTROL HARDWARE I/O)

DESIGN PERSONNEL

- FIRMWARE DESIGNED CODED, AND TESTED BY CONTROL SYSTEMS ENGINEERS
  - IMPROVED COMMUNICATION FOR MECHANIZATION OF CONTROLS REQUIREMENTS IN FIRMWARE
  - INTERACTION IMPROVED FOR ACHIEVING ADEQUATE PERFORMANCE IN THE FIRMWARE

INDEPENDENT VERIFICATION

- ACHIEVED BY SWAPPING MODULE RESPONSIBILITY AT VERIFICATION TIME
- VERIFICATION TEST PLAN INDEPENDENT OF MODULE DESIGNERS
- REVIEW OF TEST RESULTS BY CONTROL LOOP ANALYSTS

CONSTRAINTS AND THEIR EFFECTS ON FIRMWARE DESIGN

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16 BIT WORD LENGTH MAXIMUM, 8-BIT BYTES

- CAREFUL MAGNITUDE SCALING FOR COMPUTATIONS
- QUANTIZATION EFFECTS ON CONTROL FILTER TOPOLOGIES
- LOW LEVEL PERFORMANCE/DYNAMIC RANGE TRADEOFFS

1024 8-BIT BYTES ADDRESSABLE IN RAM

- ATTITUDE CONTROL FILTER COMPLEXITY
- FILTER STATE ACCURACY/MULTIPLE PRECISION ARITHMETIC

DATA PROCESSING

- COMPUTATION COMPLEXITY/TIME DELAYS
- COMPUTATION COMPLEXITY/TASK SHARING

FILTER IMPLEMENTATION TOPOLOGIES

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WORD LENGTH EFFECTS -

- ACCURACY, QUANTIZATION

FILTER TOPOLOGIES -

- POLYNOMIAL FORM (REJECTED)
- CASCADED FORM (ACCEPTED)

OTHER ALTERNATIVE FORMS

- PARALLEL FORM
- MATRIX FORM
- DFT, FFT

SCALING CONSIDERATIONS

- TOPOLOGY AND GAIN DISTRIBUTION FOR INTERMEDIATE STATES
- DYNAMIC RANGE, ETC.

FIRMWARE DEVELOPMENT & VERIFICATION TOOLS

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- VARIAN V-73 MINICOMPUTER
  - 8 AND 16 BIT ARITHMETIC
  - FORTRAN FUNCTIONS SIMULATING INDIVIDUAL CPE INSTRUCTIONS
  - PROVIDES INTERFACE IN ENGINEERING UNITS FOR MAXIMUM VISIBILITY
  - INPUT SAME AS ASSEMBLER INPUT
- CYBER 74 TIMESHARE
  - SCIENTIFIC SIMULATION OF ARITHMETIC INSTRUCTIONS
  - PROVIDES TOOL FOR CONTROL LOOP DESIGNERS
    - ASSESS LIMITED WORD LENGTH EFFECTS
    - FILTER DESIGN
  - RESIDENCE FOR CONTROLLED CPE SOURCE PROGRAM
  - RESIDENCE FOR CPE ASSEMBLER PROGRAM

FIRMWARE DEVELOPMENT & VERIFICATION TOOLS (CONTINUED)

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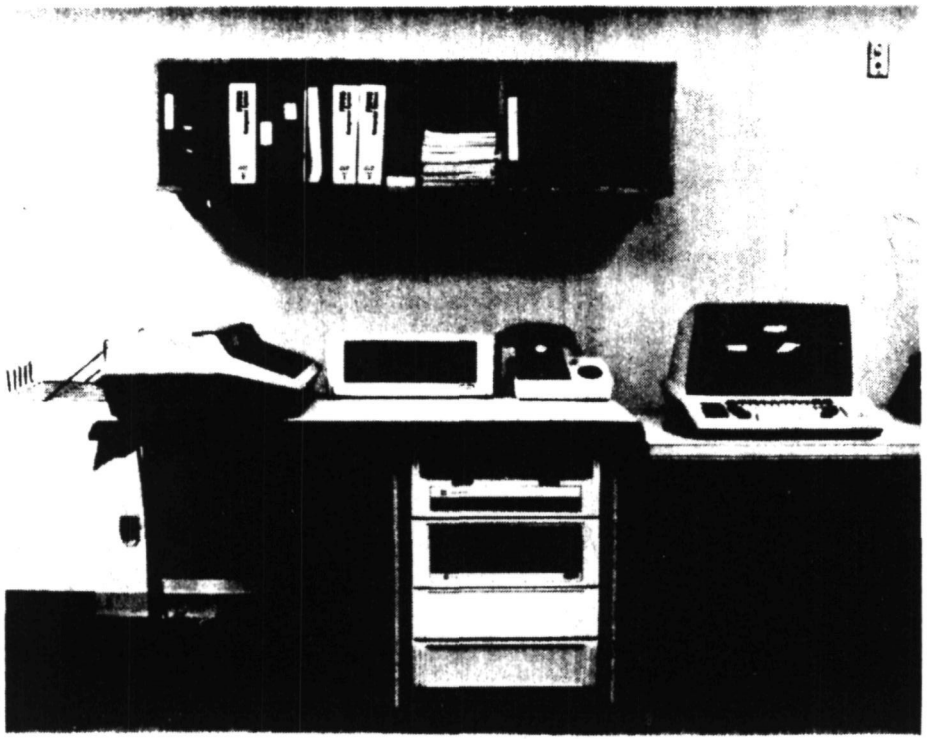
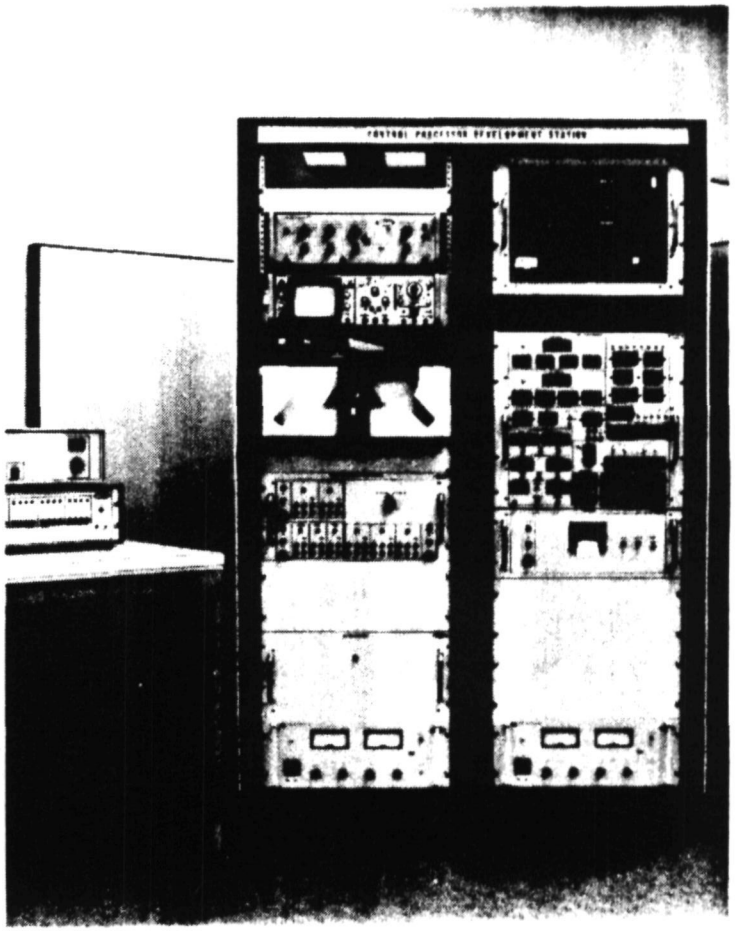
- TI 990/10 MINICOMPUTER
  - VERIFICATION TOOL
  - USED AS DRIVER FOR VERIFICATION TESTS
  - DATA COLLECTION AND PRINTOUT
  - PROVIDES DYNAMICS SIMULATION FOR DYNAMIC ENVIRONMENT
- CPE DEVELOPMENT STATION
  - BREADBOARD CPE
  - FRONT PANEL FOR PROGRAM ENTRY, EDIT, AND EXECUTION
- INTERFACE BOX
  - HARDWARE LINK OF TI 990/10 AND BREADBOARD CPE
  - GROUND STATION COMMAND SIMULATOR

DEVELOPMENT STATION EQUIPMENT



TF 990/10 AND PROM PROGRAMMER



INTERFACE BOX AND CONTROL
PROCESSOR DEVELOPMENT STATION

REVIEWING THE FIRMWARE DESIGN

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DESIGN IMPROVEMENT, FUTURE DESIGNS ARE ENHANCED BY DESIGN REVIEW AT SIGNIFICANT MILESTONES -

- INITIAL DESIGN
- COARSE PROGRAM FLOWS
- DETAILED PROGRAM FLOWS
- CODE CHECKOUT, MODULE LEVEL
- TOTAL INTEGRATED PROGRAM VERIFICATION
- SUBSYSTEM TESTING
- SPACECRAFT OPERATIONS DESIGN
- FLIGHT EXPERIENCE

DESIGN REVIEW AREAS -

- HARDWARE DESIGN
- MICROCODE DESIGN
- INSTRUCTION SET DESIGN
- GROUND STATION COMMANDS SET
- TELEMETRY DATA AVAILABLE
- PROGRAM STRUCTURE
- DESIGN PHILOSOPHIES

REVIEWING THE FIRMWARE DESIGN

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SOME DESIGN IMPROVEMENTS UNCOVERED -

- RAM MEMORY LOAD AND MOVE DATA INSTRUCTION
- EXECUTIVE PROGRAM AND SUBROUTINES STRUCTURE
- GROUND COMMANDS TAILORED TO SPACECRAFT OPERATIONS
- MICROPROCESSOR DEVELOPMENT STATION SOFTWARE CHECKOUT FEATURES
  - RAM
  - SCRATCHPAD VISIBILITY
  - RAPID MEMORY EXAMINE/CHANGE
- CONTROL FILTER STATES WORD LENGTH $\geq$ 24 BITS
- FLOATING POINT HARDWARE
- HIGH LEVEL LANGUAGE