AN EXPERIMENTAL DISTRIBUTED MICROPROCESSOR IMPLEMENTATION WITH A SHARED MEMORY COMMUNICATIONS AND CONTROL MEDIUM

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An experimental distributed microprocessor subsystem is currently under development at the Naval Air Development Center as a vehicle to investigate distributed processing concepts with respect to replacing larger computers with networks of microprocessors at the subsystem or node level. Major benefits being exploited include increased performance, flexibility, system availability, and survivability by use of multiple processing elements with reduced cost, size, weight and power consumption.

This paper concentrates on defining the distributed processing concept in terms of control primitives, variables, and structures and their use in performing a decomposed DFT (Discrete Fourier Transform) application function. The DFT was chosen as an experimental application to investigate distributed processing concepts because of its highly regular and decomposable structure for concurrent execution. The design assumes interprocessor communications to be anonymous. In this scheme, all processors can access an entire common database by employing control primitives. Access to selected areas within the common database is random, enforced by a hardware lock, and determined by task and subtask pointers. This enables the number of processors to be varied in the configuration without any modifications to the control structure. Decompositional elements of the DFT application function in terms of tasks and subtasks are also described.

The experimental hardware configuration consists of IMSAI 8080 chassis which are independent, 8-bit microcomputer units. These chassis are linked together to form a multiple processing system by means of a shared memory facility. This facility consists of hardware which provides a bus structure to enable up to six microcomputers to be interconnected. It provides polling and arbitration logic so that only one processor has access to shared memory at any one time. For discussion purposes, five of the processors are designated as slaves and one as a master where each slave contains an identical copy of a control executive and application program tasks. In actual operation, the slave processors cooperate to compute the DFT where the master provides external input, output, and control functions. With this implementation, commands to perform a DFT iteration are provided through the master.

It is expected that this concept will be tested and demonstrated on a laboratory model by the end of 1980. Evaluations will concentrate on areas such as performance comparisons based on varying the number of processors and bus contention factors as a function of local processing and common data base access times. Future work will focus on fault tolerant techniques that can be directly implemented and evaluated on the baseline laboratory model.

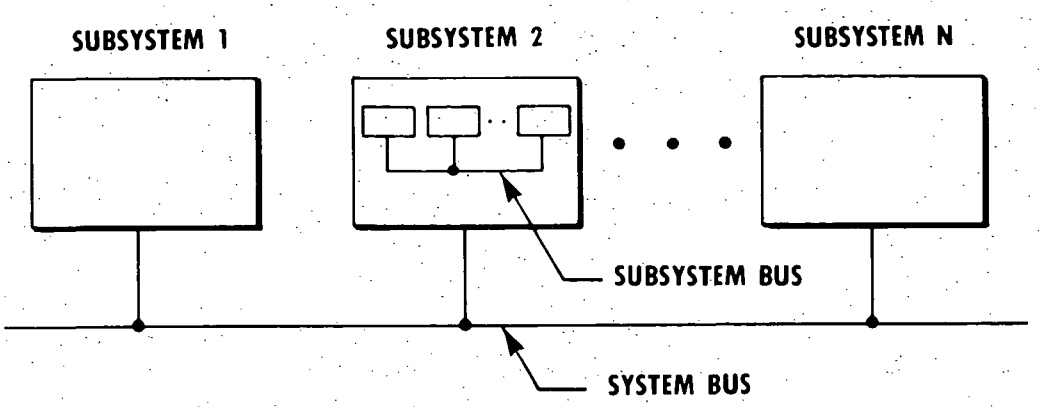
MOTIVATION

- AVIONIC PROCESSING SYSTEMS ARE BECOMING MORE DISTRIBUTED IN ORDER TO EXPLOIT THE FOLLOWING MAJOR BENEFITS:
  - INCREASED SYSTEM-WIDE REAL TIME PERFORMANCE
  - EASE OF ADAPTABILITY TO INTEGRATION AND CHANGE
  - HIGH SYSTEM AVAILABILITY
  - DECREASED SYSTEM VULNERABILITY
- BECAUSE OF REDUCED SIZE, WEIGHT, POWER CONSUMPTION AND COST ADVANTAGES, MICROPROCESSOR TECHNOLOGY WILL IMPACT AVIONIC PROCESSING SYSTEMS IN THE FOLLOWING AREAS:
  - INTERFACE AND HARDWIRED LOGIC REPLACEMENT APPLICATIONS
  - ➡ REPLACING LARGER COMPUTERS WITH NETWORKS OF SMALLER COMPUTERS

MICROPROCESSOR TECHNOLOGY AND DISTRIBUTED PROCESSING

- REASONABLE COST-PERMITS EXPERIMENTING WITH CONCEPTS WHICH WOULD OTHERWISE BE PAPER STUDIES
- REDUCED SIZE, POWER, AND WEIGHT PERMITS APPLICATIONS THAT WOULD OTHERWISE NOT BE FEASIBLE
- LIFE CYCLE COSTS OFTEN MUCH LOWER THAN FORMER SOLUTIONS TO SAME PROBLEM

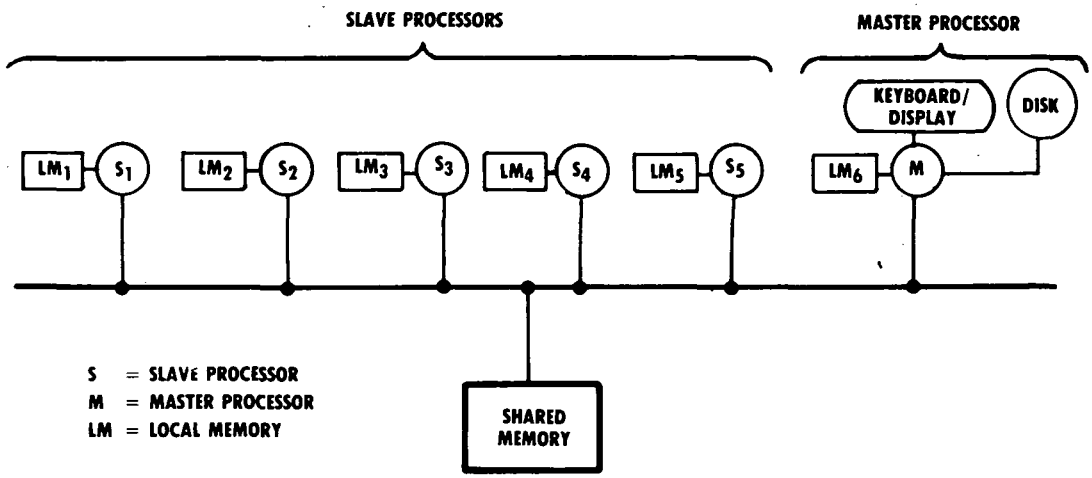
GLOBAL/LOCAL DISTRIBUTION



APPROACH

- EXPERIMENTAL INVESTIGATION
- LABORATORY MODEL
- OFF-THE-SHELF HARDWARE (MICROPROCESSORS ARE INEXPENSIVE)
  - MULTIPLE PROCESSORS
  - SHARED MEMORY FACILITY INTERCONNECT
- EXPERIMENTAL CONTROL STRUCTURE
  - LOCAL KNOWLEDGE OF EXISTANCE OF OTHER PROCESSORS NOT REQUIRED
  - GLOBAL CONTROL AND TASK SCHEDULING VIA HIGHLY RELIABLE SHARED MEMORY
- EXPERIMENTAL WELL-KNOWN APPLICATION-DFT
- DEMONSTRATE CONCEPT FEASIBILITY
- PERFORM TRADE-OFF ANALYSES
- IDENTIFY AND IMPLEMENT FAULT-TOLERANT CONCEPTS

EXPERIMENTAL HARDWARE CONFIGURATION



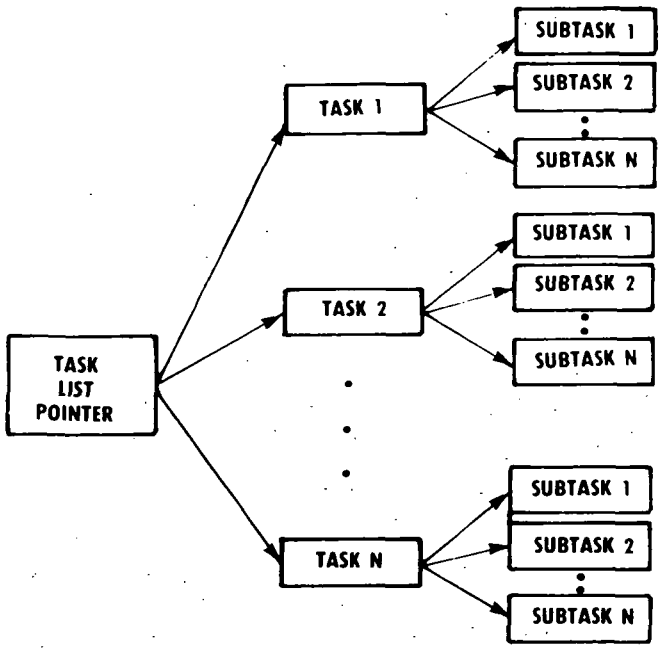
SHARED MEMORY FACILITY CONSTRAINTS

- SIX PROCESSORS MAXIMUM
- ROUND-ROBIN POLLING SCHEME
- ONE BYTE ACCESSED PER POLL
- FIXED LOCK-OUT TIME IN FLAG BLOCK

ASSUMPTIONS

- MASTER PROCESSOR PERFORMS INTERFACE AND DISPLAY FUNCTIONS
- SLAVE PROCESSORS PERFORM APPLICATION FUNCTION CONCURRENTLY AS DIRECTED BY MASTER PROCESSOR
- LOCAL MEMORY
  - EACH SLAVE PROCESSOR CONTAINS IDENTICAL COPY OF PROGRAMS
  - CONTROL EXECUTIVE
  - APPLICATION TASKS
- SHARED MEMORY
  - COMMON TO ALL PROCESSORS
  - CONTROL VARIABLES
  - APPLICATION DATA
  - ACCESSED BY CONTROL PRIMITIVES
  - ACCESS RIGHTS ENFORCED BY SEMAPHORES
- VARYING NUMBER OF PROCESSORS DOES NOT AFFECT CONTROL STRUCTURE

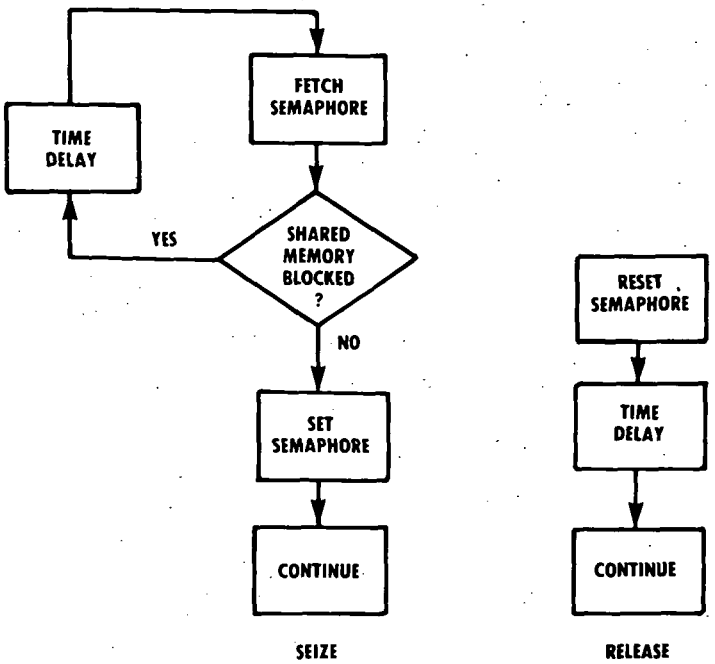
TASK STRUCTURE



SYSTEM CONTROL: SEMAPHORES

- ENFORCES ACCESS RIGHTS TO SHARED MEMORY
- USED TO INDICATE CONDITIONS
  - SHARED MEMORY BLOCKED
  - SHARED MEMORY AVAILABLE
  - ITERATION IN PROGRESS
  - ITERATION COMPLETED

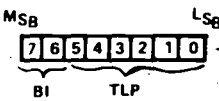
CONTROL PRIMITIVES



CONTROL VARIABLES

BI/TLPt

FORMAT:



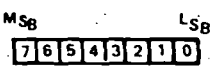
– BI IS A 2-BIT SEMAPHORE AND INDICATES THE FOLLOWING CONDITIONS:

SEMAPHORE B	SEMAPHORE I	CONDITION
0	0	SHARED MEMORY BLOCKED AND ITERATION COMPLETED
0	1	SHARED MEMORY BLOCKED AND ITERATION IN PROGRESS
1	0	SHARED MEMORY AVAILABLE AND ITERATION COMPLETED
1	1	SHARED MEMORY AVAILABLE AND ITERATION IN PROGRESS

– TLP IS A 6-BIT TASK LIST POINTER THAT CAN POINT TO ANY ONE OF 64 TASKS

• TSt

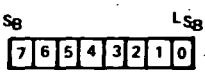
– FORMAT:



–TSt IS AN 8-BIT WORD USED TO ASSOCIATE CORRESPONDING DATA WITH A TASK AND CAN TAKE ON 256 VALUES

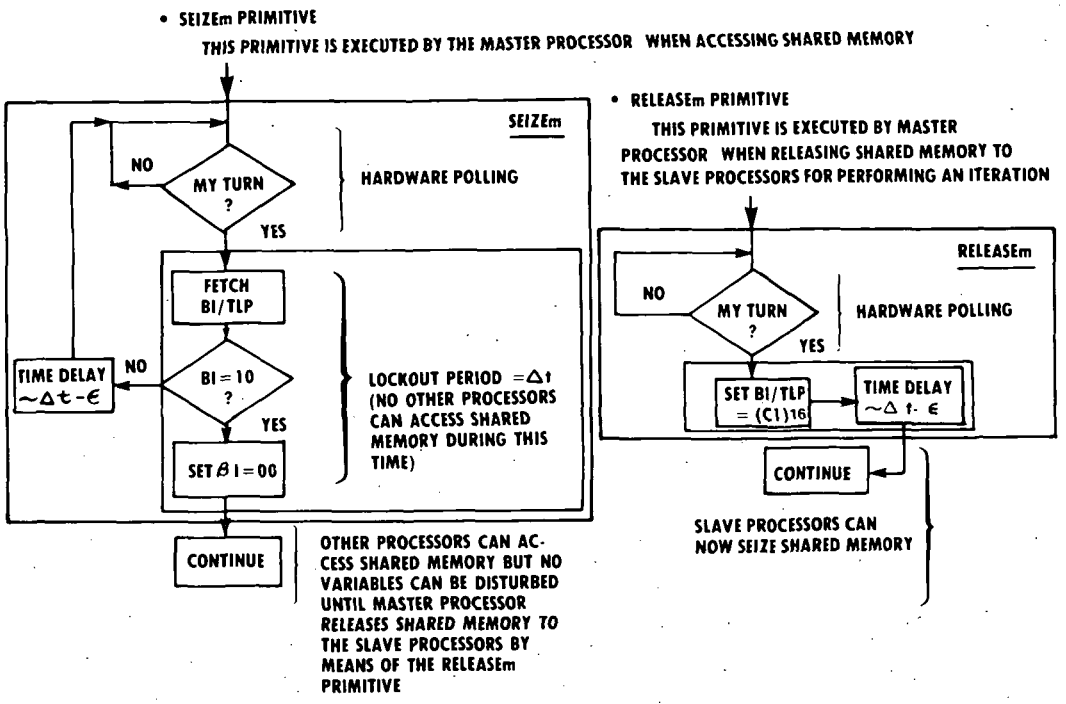
• CTCt

– FORMAT:

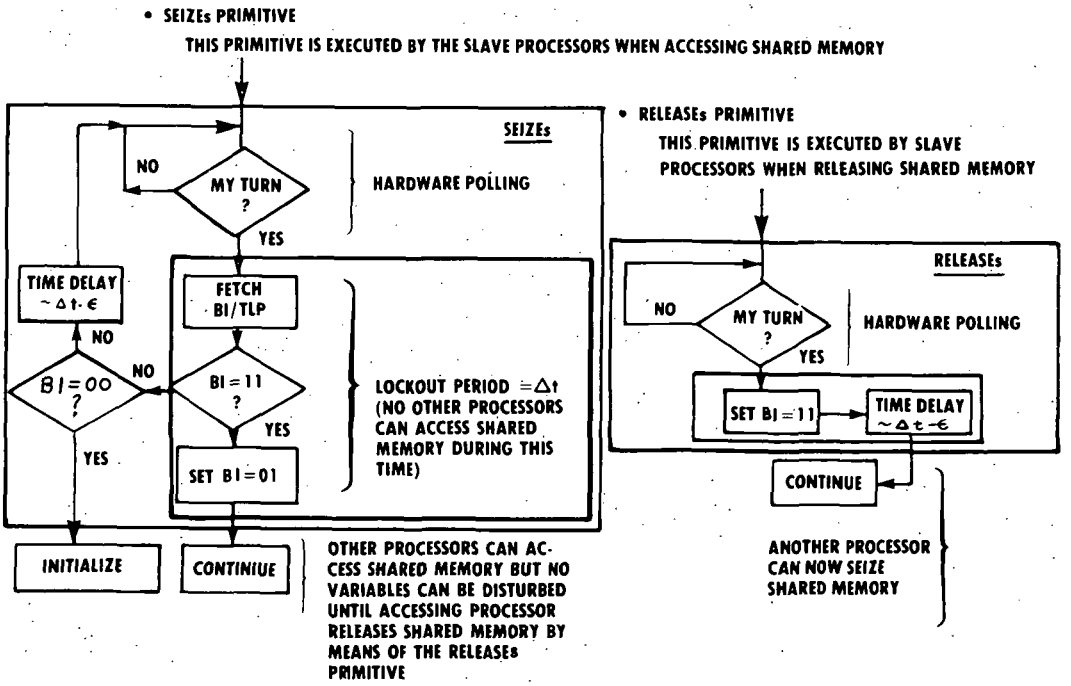


– CTC IS AN 8-BIT CUMULATIVE TASK COUNTER. ONE CTC IS REQUIRED FOR EACH TYPE OF TASK BEING PERFORMED, i. e., THE NUMBER OF CTC s ARE EQUAL TO THE NUMBER OF TASKS POINTED TO BY TLP.

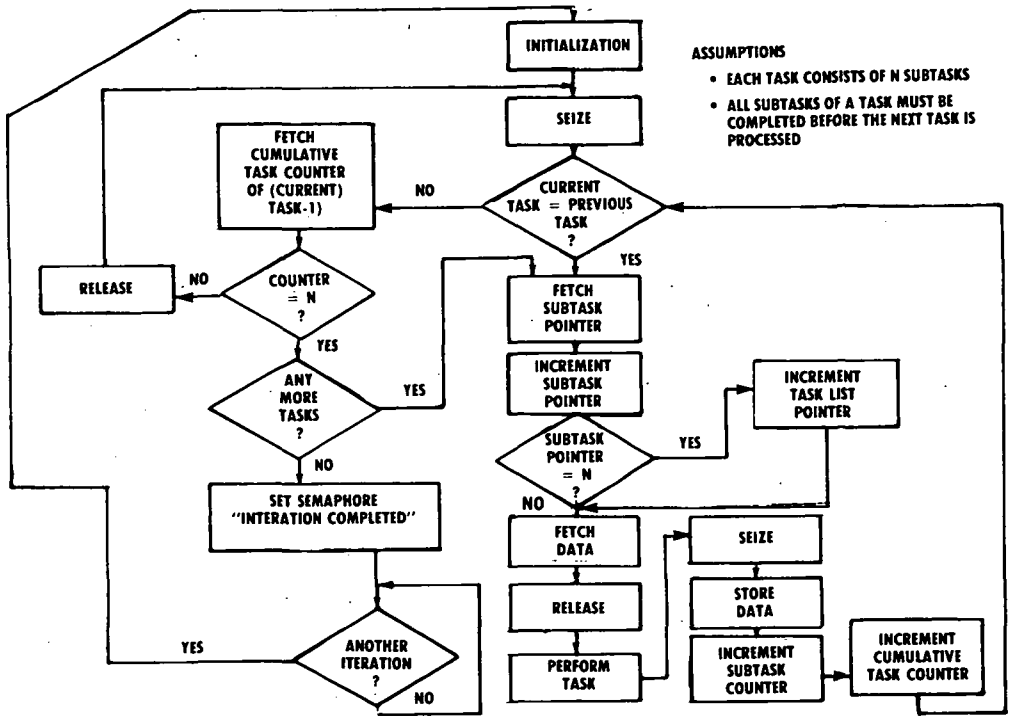
MASTER PROCESSOR CONTROL PRIMITIVES



SLAVE PROCESSOR CENTROL PRIMITIVES



TASK EXECUTION CONTROL



DFT APPLICATION

A DFT CAN BE DEFINED IN THE FOLLOWING MATRIX FORM:

$G = WF$

IF WE LET:

- $n = 0,1,2, \ldots, N-1$ = MATRIX ROW NUMBER AND FREQUENCY STEP
- $k = 0,1,2, \ldots, k-1$ = MATRIX COLUMN NUMBER AND TIME STEP
- $N = k$ BUT MAINTAINING n AND k NOTATIONS TO DISTINGUISH ROWS FROM COLUMNS

THEN:

- W IS AN $N \times k$ MATRIX CONSISTING OF THE TERMS

$$W^{n,k} = e^{(-2\pi j/N)(nk \text{ MOD } N)}$$

$$= \cos\left[\left(\frac{2\pi}{N}\right)(nk \text{ MOD } N)\right] - j \sin\left[\left(\frac{2\pi}{N}\right)(nk \text{ MOD } N)\right]$$

- F IS A $k \times 1$ MATRIX REPRESENTING THE FUNCTION $F(tk)T/2\pi k$ OVER THE TIME SPAN T
- G IS AN $N \times 1$ MATRIX WHERE $Gn = T/2\pi k \sum_{k=0}^{K-1} W^{n,k} F(tk)$

IN EXPANDED FORM, $G = WF$ CAN BE WRITTEN AS:

$$\begin{pmatrix} G0 \\ G1 \\ G2 \\ \vdots \\ GN-1 \end{pmatrix} = \begin{pmatrix} W^{0,0} & W^{0,K-1} & W^{0,2} & W^{0,K-1} \\ W^{1,0} & W^{1,K-1} & W^{1,2} & W^{1,K-1} \\ W^{2,0} & W^{2,K-1} & W^{2,2} & W^{2,K-1} \\ \vdots & & & \vdots \\ W^{N-1,0} & W^{N-1,K-1} & W^{N-1,2} & W^{N-1,K-1} \end{pmatrix} \begin{pmatrix} Fto\ T/2\ \pi\ K \\ Ft1\ T/2\ \pi\ K \\ Ft2\ T/2\ \pi\ K \\ \vdots \\ FtK-1\ T/2\ \pi\ K \end{pmatrix}$$

SINCE:

$$Gn,k\ (REAL) = \cos\left[\left(\frac{2\pi}{N}\right)(nk \text{ MOD } N)\right] F(tk)\ T/2\ \pi k$$

$$Gn,k\ (IMAGINARY) = -j\left\{\sin\left[\left(\frac{2\pi}{N}\right)(nk \text{ MOD } N)\right\}F(tk)\ T/2\ \pi k\right.$$

$\omega n = n\Delta\omega$ WHERE $\Delta\omega = \frac{2\pi K}{NT}$

$$|Gn| = \sqrt{\left[\sum_{k=0}^{K-1} Gn,k\ (REAL)\right]^2 + \left[\sum_{k=0}^{K-1} Gn,k\ (IMAGINARY)\right]^2}$$

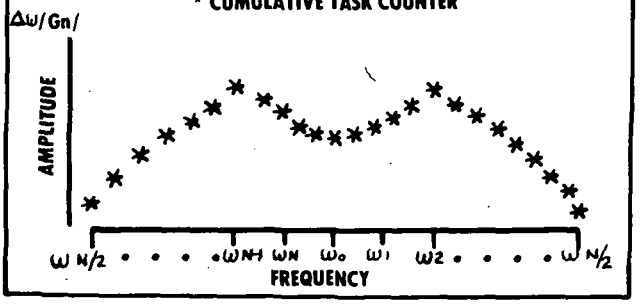
THE AMPLITUDE/FREQUENCY VALUES CAN BE OBTAINED AS FOLLOWS:

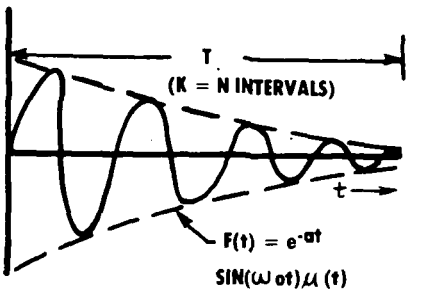
$$AMP(\omega_n) = \Delta\omega |Gn|$$

INPUT/OUTPUT

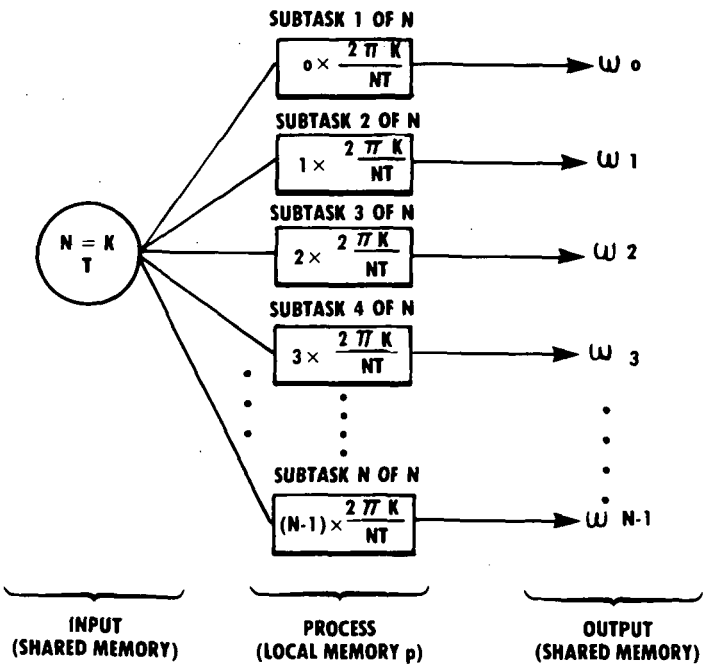
SLAVE PROCESSOR	TASK/SUBTASK COMPLETIONS		
	TASK 1	TASK 2	TASK 3
1	X	X	X
2	X	X	X
3	X	X	X
4	X	X	X
5	X	X	X
CTC*	X	X	X

* CUMULATIVE TASK COUNTER

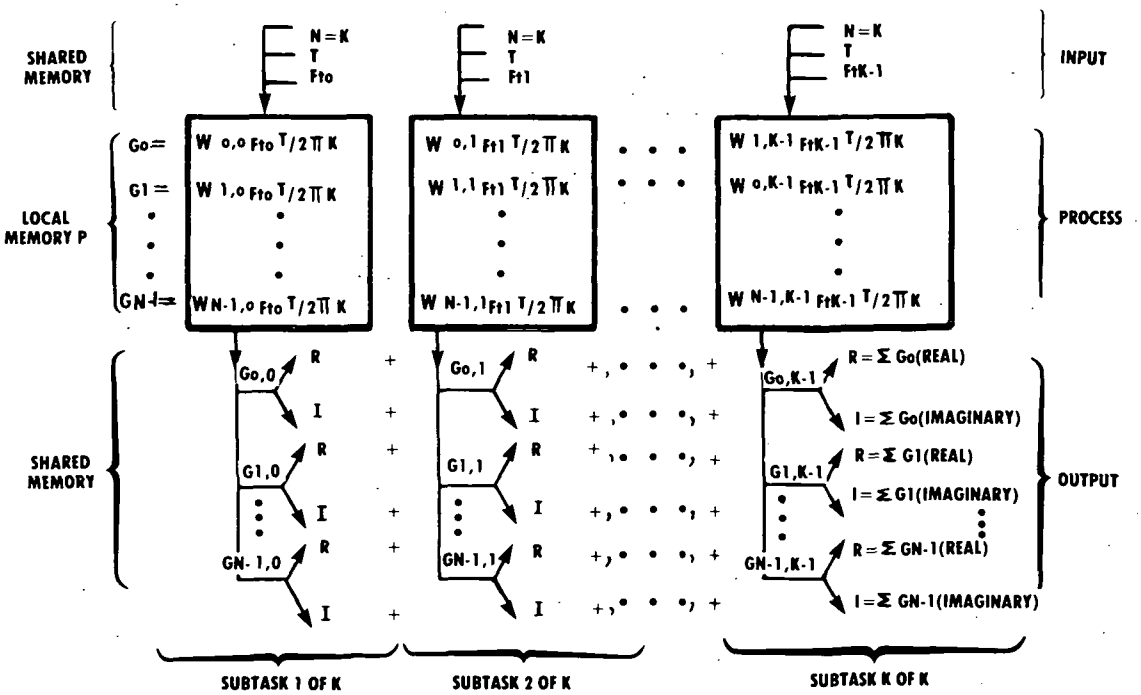




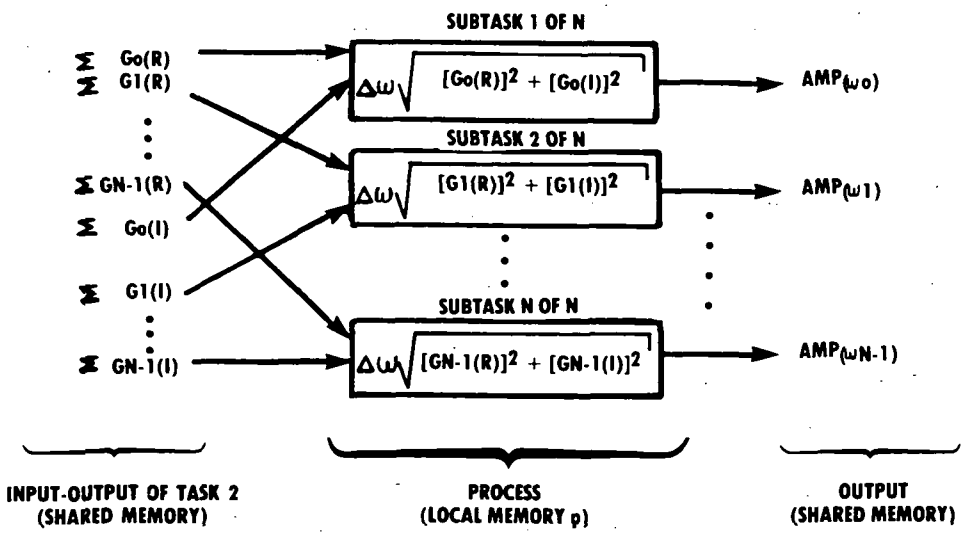
DFT DECOMPOSITION FOR TASK 1



DFT DECOMPOSITION FOR TASK 2



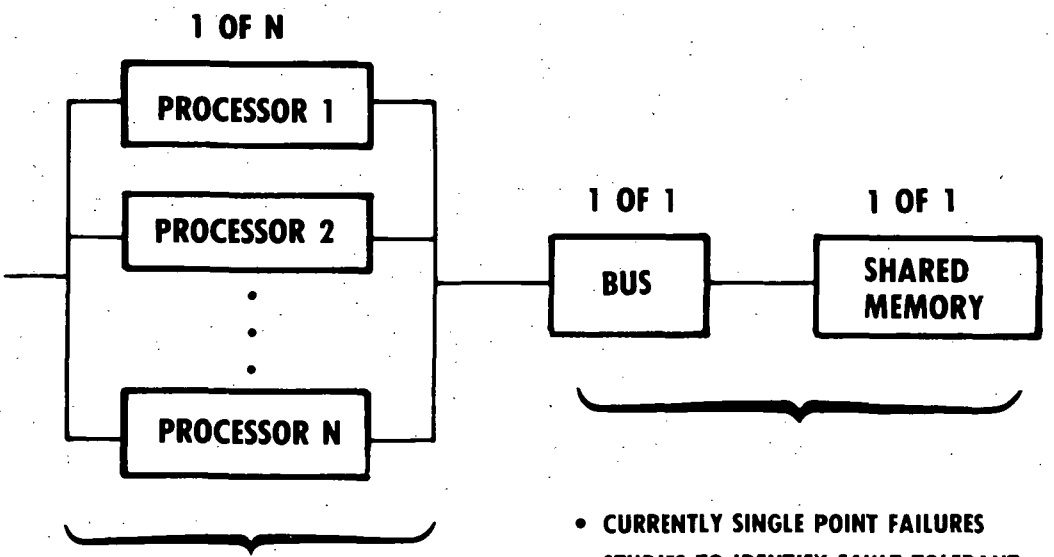
DFT DECOMPOSITION FOR TASK 3



STATUS

- IMPLEMENTATION
- GCSS SIMULATION
- LABORATORY EVALUATION
- FAULT TOLERANT STUDIES
  - PROCESSOR
  - SHARED MEMORY
  - BUS

RELIABILITY MODEL



- TAKE ADVANTAGE OF MULTIPLE PROCESSORS
- OPTIMIZE EXISTING CONTROL STRUCTURE FOR FAULT-TOLERANCE PURPOSES

- CURRENTLY SINGLE POINT FAILURES
- STUDIES TO IDENTIFY FAULT TOLERANT SCHEMES
- POSSIBLE IMPLEMENTATION OF HIGHLY RELIABLE SHARED MEMORY WOULD BE DUPLEXED CONFIGURATION EACH WITH SINGLE ERROR CORRECTION AND DOUBLE ERROR DETECTION