A HIGH PERFORMANCE MULTIPLIER PROCESSOR FOR USE WITH AEROSPACE MICROCOMPUTERS

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An MC68000-based microcomputer including a hardware multiplier processor has been designed and prototyped for a re-entry vehicle navigation and control application. In this paper, the microcomputer is discussed with emphasis on the multiplier processor architecture, software control and theory of operation.

The MC68000 CPU of the microcomputer cannot satisfy the real-time multiply processing requirements of a high accuracy RV navigator. The standalone CPU thru-put for multiply intensive applications is increased approximately seven times by the addition of a board level Hardware Multiplier Processor (HMP). Although the HMP was designed for the MC68000 microcomputer, it can be used with any 16 or 32 bit CPU with minimal modifications.

The memory mapped HMP performs 16 and 32 bit multiplications and can optionally add or subtract the full product to previous accumulator contents. The circuitry is sufficiently fast to allow the MC68000 running at 8 MHz to write single or double precision variables to the HMP using memory to memory transfers and perform an operation with no wait states introduced or overhead time for command passing.

The result of multiply and accumulate operations may be transferred in its entirety or scaled by $2^{\pm 30}$ and rounded automatically prior to transfer to the destination location specified by the CPU. Worst case CPU wait times introduced are: 3.3 μsec for double precision scale by 2^{-14} and round to single precision; and 6.3 μsec for quadruple precision scale by 2^{-30} and round to double precision.

The Hardware Multiplier Processor incorporates Serial/Parallel Hardware Multiplier ICs, a translation PROM and address controlled logic to implement previously mentioned arithmetic functions. The use of serial arithmetic circuitry yields a processor of small physical size, low power and significant flexibility. The computation time of the HMP is shorter than most of the general memory addressing modes of the host CPU. The nine least significant CPU address bits in conjunction with the translation PROM control all HMP functions. The translation PROM provides the function related serial clock count to the clock control logic which in turn controls all HMP timing.

SANDIA AEROSPACE COMPUTER VERSION 4
(SANDAC IV)

ARCHITECTURE

MC68000 CPU
- 32 BIT DATA AND ADDRESS REGISTERS
- 56 INSTRUCTIONS
- 14 ADDRESSING MODES
- MEMORY MAPPED I/O

16 BIT DATA BUS
16 M BYTE ADDRESS SPACE
HARDWARE MULTIPLIER PROCESSOR (HMP)
VECTORED INTERRUPTS

POWER REQUIREMENTS

+5V @ 3A TYPICAL

PHYSICAL

EXPANDABLE MODULAR CONSTRUCTION
STACKABLE PIN-SOCKET INTERMODULE BUS
17.8 CM x 15.9 CM x 1.27 CM MODULES

SANDAC IV CPU MODULE

MC68000 CPU
16K BYTE EPROM MEMORY
16K BYTE NON-VOLATILE CMOS RAM
POWER MONITOR & RESET CIRCUIT

SANDAC IV I/O MODULE

4 CHANNEL OPTO-ISOLATED USART SERIAL I/O
8 CHANNEL PRIORITY INTERRUPT CONTROLLER
5 CHANNEL PROGRAMMABLE 16 BIT TIMER/COUNTER
16 BIT MEMORY MAPPED (4K WORD) I/O

SANDAC IV HMP MODULE

MEMORY MAPPED REGISTERS AND FUNCTIONS

SINGLE PRECISION (16 BIT) AND DOUBLE PRECISION (32 BIT) FUNCTIONS

MULTIPLY WITH OPTIONAL ADD OR SUBTRACT TO PREVIOUS ACCUMULATOR CONTENTS

SCALE $2^{\pm N}$ AND ROUND

OVERFLOW DETECTION RELATING TO ACCUMULATION

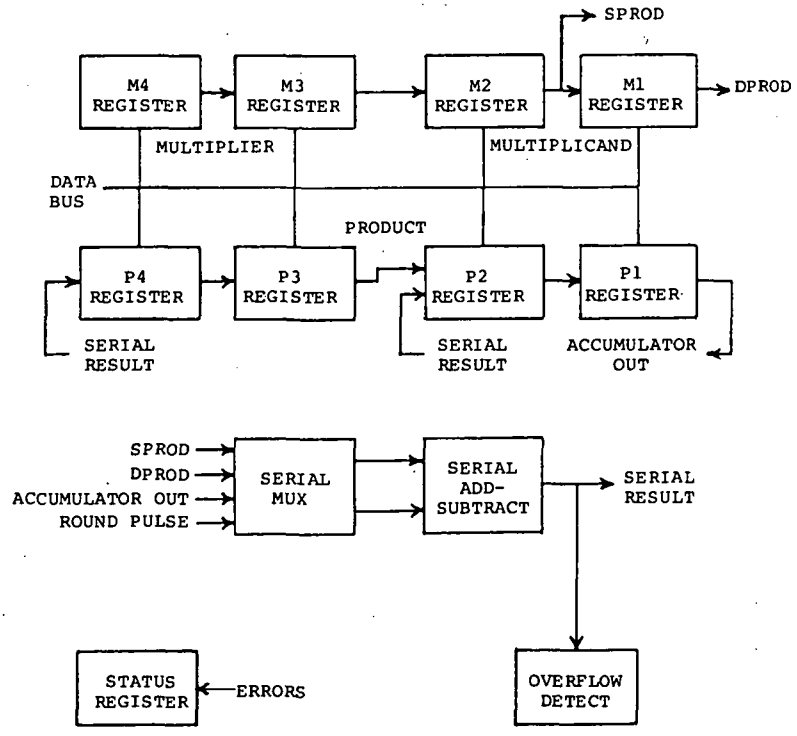
ADDRESSING ERROR DETECTION

CONTROL FUNCTIONS DERIVED FROM LATCHED ADDRESS BITS

HOST CPU ALLOWED TO PROCEED IN PARALLEL WITH HMP

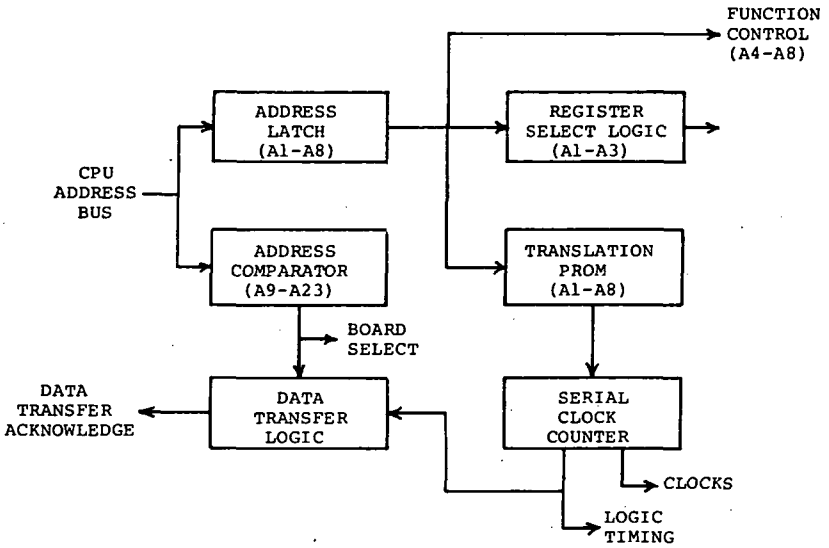
AUTOMATIC HOLD-OFF OF HOST CPU IF HMP BUSY

HARDWARE MULTIPLIER PROCESSOR
BLOCK DIAGRAM



HARDWARE MULTIPLIER PROCESSOR

CONTROL BLOCK DIAGRAM



EXAMPLE HMP ADDRESS MAPPED FUNCTIONS

ADDRESS (HEX)	FUNCTION
FE00	READ-CLEAR STATUS REGISTER
FE02	READ/WRITE P4
FE04	READ/WRITE P3
FE06	READ/WRITE P2
FE08	READ/WRITE P1
FE0A	READ/WRITE M4
FE0C	READ/WRITE M3
FE0E	WRITE M2
FE0E	READ STATUS REGISTER
FE1E	WRITE M2, S.P. MULTIPLY & ADD
FE3E	WRITE M2, CLEAR ACCUM., S.P. MULT. & ADD
FE5E	WRITE M2, S.P. MULTIPLY & SUBTRACT
FE7E	WRITE M2, CLEAR ACCUM., S.P. MULT. & SUB.
FE8E	WRITE M2
FE90	WRITE M1, D.P. MULTIPLY & ADD
⋮	⋮

EXAMPLE HMP ADDRESS MAPPED FUNCTIONS

ADDRESS (HEX)	FUNCTION
FF00	D.P. P REG x 2^{-14} & S.P. ROUND
⋮	⋮
FF1A	D.P. P REG x 2^{-1} & S.P. ROUND
FF1C	D.P. P REG x 2^{0} & S.P. ROUND
FF1E	D.P. P REG x 2^{1} & S.P. ROUND
⋮	⋮
FF38	D.P. P REG x 2^{14} & S.P. ROUND
FF80	Q.P. P REG x 2^{-30} & D.P. ROUND
⋮	⋮
FFBA	Q.P. P REG x 2^{-1} & D.P. ROUND
FFBC	Q.P. P REG x 2^{0} & D.P. ROUND
FFBE	Q.P. P REG x 2^{1} & D.P. ROUND
⋮	⋮
FFF8	Q.P. P REG x 2^{30} & D.P. ROUND

FUNCTION EXECUTION TIME

FUNCTION	EXECUTION TIME
S.P. MULTIPLY & ACCUMULATE	2.38 μs
D.P. MULTIPLY & ACCUMULATE	4.38 μs
D.P. SCALE 2^{-14} & S.P. ROUND	3.31 μs
D.P. SCALE 2^{0} & S.P. ROUND	2.44 μs
D.P. SCALE 2^{14} & S.P. ROUND	1.56 μs
Q.P. SCALE 2^{-30} & D.P. ROUND	6.31 μs
Q.P. SCALE 2^{0} & D.P. ROUND	4.44 μs
Q.P. SCALE 2^{30} & D.P. ROUND	2.56 μs

SANDAC IV BENCHMARK EQUATION

$$A_{11} = B_{11}C_{11} + B_{12}C_{21} + B_{13}C_{31} + K$$

NOTE: ALL TERMS ARE 32 BIT FIXED POINT.

CONFIGURATION	EXECUTION TIME
MC68000 CPU @ 8 MHZ (SUBROUTINE SOLUTION)	235 μs
MC68000 CPU @ 8 MHZ + HMP (HMP SOLUTION)	31 μs

BENCHMARK EQUATION MACRO INSTRUCTION SOLUTION

$$A_{11} = B_{11}C_{11} + B_{12}C_{21} + B_{13}C_{31} + K$$

SOURCE CODE:

```
LQPP K              /LOAD Q.P. CONSTANT
DPMA B11, C11       /D.P. MULTIPLY & ADD
DPMA B12, C21       /D.P. MULTIPLY & ADD
DPMA B13, C31       /D.P. MULTIPLY & ADD
DPSRM 0, A11        /QUAD P. SCALE, ROUND & MOVE
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BENCHMARK EQUATION MACRO EXPANSION

$$A_{11} = B_{11}C_{11} + B_{12}C_{21} + B_{13}C_{31} + K$$

ASSEMBLER EXPANSION:

MACRO	MC68000 MNEMONICS	COMMENT
LQPP #0, K		/LOAD Q.P. CONSTANT
	MOVE.L 0, FE02	
	MOVE.L K, FE06	
DPMA B_{11}, C_{11}		/D.P. MULTIPLY & ADD
	MOVE.L B_{11}, FE0A	
	MOVE.L C_{11}, FE8E	
DPMA B_{12}, C_{21}		/D.P. MULTIPLY & ADD
	MOVE.L B_{12}, FE0A	
	MOVE.L C_{21}, FE8E	
DPMA B_{13}, C_{31}		/D.P. MULTIPLY & ADD
	MOVE.L B_{13}, FE0A	
	MOVE.L C_{31}, FE8E	
DPSRM 0, A_{11}		/QUAD P. SCALE, ROUND & MOVE
	MOVE.L FFBC, A_{11}	

SUMMARY

EFFECTIVELY EXPANDS HOST CPU INSTRUCTION SET

EASY INCORPORATION INTO ANY 16 BIT SYSTEM

HIGH PERFORMANCE DUE TO SIMULTANEOUS DATA & COMMAND TRANSFER BY HOST CPU

SERIAL ARITHMETIC APPROACH REDUCES COMPONENT COUNT

EQUATION EXECUTION TIME PRIMARILY DEPENDENT ON CPU MEMORY ACCESS TIME

STRAIGHT FORWARD SOFTWARE CONTROL

SINGLE μP CPU PLUS HMP PROVIDES PERFORMANCE COMPARABLE TO BIPOLAR BIT-SLICE DESIGNS