APPLICATION OF ADVANCED ELECTRONICS TO A FUTURE SPACECRAFT COMPUTER DESIGN

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Over the past two and one half years at Martin Marietta, an Independent Research and Development task* has been conducting an extensive investigation on advanced spacecraft computer systems. The task objectives are to quantitatively determine how recent advancements in hardware and software** technology can be used to obtain major improvements in spacecraft computer system capabilities. This paper describes the major hardware aspects which have been investigated and what results have been obtained.

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* This work was conducted by the Denver Division of Martin Marietta Corporation under Independent Research and Development Project Authorization D-80D.

** Related paper, "Application of Software Technology to a Future Spacecraft Computer Design, in Microprocessor Software Technology Session.

During 1978 several architecture trade studies were conducted to arrive at a decision on what characteristics a future spacecraft computer should have. The architecture trade studies went through two phases; the implementation independent phase and the chip set dependent phase. Some of the major factors which were included during the first phase were:

- Data types and precision,
- Processing throughput,
- Input and output,
- Address space,
- Instruction types,
- Multiprogramming features, and
- Test support equipment.

In general terms, a modern minicomputer-like architecture with a 250,000 operations per second performance and the lowest possible power consumption was desired. It was noticed almost immediately that in some cases it was difficult to define certain architecture features because they appeared to be application dependent. For example, input and output (I/O) appears to vary depending on the spacecraft data bus. To allow for this variation but not impede progress it was decided to use memory mapped I/O. This approach, insures that sufficient flexibility is maintained in the architecture for most applications. In a related area a slightly different approach was taken I/O is normally handled in one of two ways, register transfers or direct memory access (DMA). If the direct memory access was imbedded in each I/O controller than each application, each would be burdened with the nonrecurring cost of DMA. To avoid this situation we incorporated a generalized Direct Memory Processor which can buffer and transfer data between a memory mapped I/O controller and main memory, Hence there is only a one time nonrecurring design cost associated with this feature of the computer.

In 1978 integrated circuits technology was reviewed. Of particular interest in this area was the feasibility of using Complementary Metal Oxide Semiconductor/Silicon on Saphire (CMOS/SOS) parts. The primary reason for interest in CMOS/SOS was the favorable speed/power ratio which is important in spaceborne applications. The candidate CMOS/SOS chip sets which were

investigated include: custom devices developed by NASA Marshall Space Flight Center and Air Force Space Division (formerly SAMSO); parts developed under the Space Division Advanced Computer Technology program (ACT-I); 290X parts under development at Raytheon; and a microprocessor chip set being developed at RCA under contract to the Air Force Avionics Laboratory at Wright Patterson (AFWAL). We elimated the use of custom parts early in our selection process because of their high cost. The ACT and Raytheon parts were eliminated because a comprehensive family of support components was not available. It was felt, therefore, that the best potential CMOS/SOS technology for use in spaceborne applications was the AFWAL/RCA microprocessor chip set. In addition to being a comprehensive family of LSI devices, the units are being produced in a radiation hardened process with high reliability screening. Recently the Global Positioning System (GPS) program has selected this chip set for use giving further evidence that our decision to base our design on the AFWAL/RCA chip set was appropriate.

The LSI devices available in the RCA chip set are: the TCS 129 General Processing Unit (GPU), the TCS 196 Multiplier, the TCS 09X Gate Universal Array (GUA), the TCS 150 Random Access Memory (RAM), the TCS 075 Read Only Memory, and the TCS 158 Microprogram Controller Unit. The GPU forms the foundation for the entire chip set. It is an eight bit wide arithmetic and logic slice that can be cascaded to form an arbitrarily wide data word. The TCS 196, unlike other multiplier chips presently available, is also a cascadable device. All of the partial product logic is included on the TCS 196 to form an N x M multiplier without the need for supporting hardware logic. The purpose of the TCS 09X GUA is to provide the logic and circuitry which in most other chip set families is found in small and medium scale integrated circuits. These arrays are fixed regular patterns of transistors and routing paths. By defining transistor interconnection, the GUA is customized with logic in much the same way that Read Only Memory is customized with data. Some of the benefits associated with GUAs are improved speed and real estate requirements; disadvantages include higher nonrecurring cost and greater design risk. Martin Marietta has thus far designed three Gate Universal Arrays and testing has shown that the devices are functionally correct and exceed performance expections.

Once the first phase of the architecture analysis was completed, the factors associated with use of the CMOS/SOS microprocessor chip set had to be taken into account. Some of these factors were:

- Number of user available registers,
- High speed arithmetic support hardware,
- Instruction decoding,
- Data formatting and deformatting,
- Memory volatility, and
- Interrupt handling.

It is important to mention at this time that software* analysis as well as circuit analysis played a significant part at this time in determining what the final characteristics of the computer would be. For example the fact that we desired a modern minicomputer-like architecture implied that multiple general purpose registers were required. The number of registers however could only be determined by coding application programs, measuring the resulting throughput, and performing the physical circuit design to determine what the impact was in terms of hardware cost and complexity.

Throughout the first half of 1979 we performed many paper emulations in which we wrote application programs, wrote microprograms, and prepared circuit layouts. These paper emulations allowed us to determine specific advantages and disadvantages inherent in different architectures implemented with the CMOS/SOS microprocessor chip set. In midyear we chose the "best" architecture for implementation. Best is a subjective term which in some cases such as performance and power consumption can be determined quantitatively, but in other cases such as flexibility and risk it can only be measured qualitatively.

After the selection process was completed, detailed design began with the goal of having an operational demonstration unit in 1980. The most challenging part of the detailed design was the many unknowns associated with using a microprocessor chip set which was still under development at that time. Our three primary concerns were internal device performance, off-chip drive

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* Op. Cit.

capability, and Gate Universal Array layout. The first concern was handled by derating devices a minimum of 100% using the limited test data available. Testing at Martin Marietta has since shown that all devices are much better than were originally anticipated. Our second concern, off-chip drive capability, was caused by the capacitance loading problems associated with CMOS technology. This problem becomes particularly severe in the area of the main memory interface. To eliminate the concern we incorporated a bulk hardened signal level converter to drive the memory bus at TTL levels. The addition of the signal level converter causes an added latency along the bus but this is a much better situation than that which would have occurred if an attempt had been made to fanout the CMOS signals. Our remaining concern, GUA design, was handled very conservatively. TTL circuit equivalents were built for each array, extensive software logic simulations were conducted, and the entire data submittal package was independently verified before shipment to RCA. As a result of this effort, no Martin Marietta caused problems have been found in any of the three designs which we have completed. There were some issues in the testing area which arose because of Martin Marietta's and RCA's lack of experience with the chip set. These have since been resolved by modifying our software so that test vector data is automatically generated during the logic simulation.

Throughout 1980 efforts have been directed toward fabrication of a breadboard unit which demonstrates the primary computer modules: the central processor module, the priority interrupt controller, the memory bus driver/receiver, and an 8K RAM memory bank. Additionally an operator control panel, a writable control store, a programmable read only memory bank, and a serial I/O port were implemented to facilitate development. The resulting computer has been operational for several months and many of the major design goals have already been demonstrated. Functionality, performance and power consumption meet our expectations.

In 1980 concurrent with our breadboard fabrication we took the first step towards producing a qualified flight unit. This step was the fabrication and testing of mockup printed circuit boards using leadless carrier packaging technology. Although the Orlando Division of Martin Marietta has over three years experience in the use of leadless carriers, we felt it was necessary to

perform some specific tests to eliminate the controversy surrounding the use of this technology in spaceborne applications. As a result of qualification level thermal and vibration tests, we have found that leadless carriers mounted on polyimide daughter boards which are in turn properly mounted on larger mother boards is an appropriate packaging approach.

In 1981 we intend to extend our work by taking the primary hardware modules now in wire wrap form and converting these to printed circuit boards. This effort will have two major benefits. First, it will allow us to show what performance margins exist at the system level. Performance margin cannot be demonstrated on the breadboard because of the high capacitance associated with the wire wrap technique. The second major benefit to design and fabricating the printed circuit boards is that we will be able to perform thermal and vibration qualification level testing on a unit which much more closely resembles the final flight unit.

Although the AFWAL/RCA CMOS/SOS microprocessor chip set was originally considered to be a high risk item, the fact that parts have been produced, tested and used in our computer system and the GPS program indicate that these parts will have a favorable future. The results we have obtained show that a CMOS/SOS computer can obtain the same performance levels as presently available bipolar spacecraft computer but at approximately 15% of their power consumption.

BACKGROUND

OBJECTIVES:*

QUANTITATIVELY DETERMINE HOW RECENT ADVANCEMENTS IN HARDWARE AND SOFTWARE** TECHNOLOGY CAN BE USED TO OBTAIN IMPROVEMENTS IN SPACECRAFT COMPUTER CAPABILITIES.

CMOS/SOS INTEGRATED CIRCUITS
SEMI-CUSTOM LSI DEVICES
LEADLESS CARRIER PACKAGING
MICROPROGRAMMING
PASCAL, HAL, ADA, HIGER ORDER LANGUAGE

*THIS WORK WAS CONDUCTED BY THE DENVER DIVISION UNDER INDEPENDENT RESEARCH AND DEVELOPMENT PROJECT AUTHORIZATION D-80D

**RELATED PRESENTATION, "APPLICATION OF SOFTWARE TECHNOLOGY TO A FUTURE SPACECRAFT COMPUTER DESIGN", IN SESSION III: MICROPROCESSOR SOFTWARE TECHNOLOGY

BACKGROUND

APPROACH:

1978 REVIEW AVAILABLE STATE OF THE ART TECHNOLOGY
DEFINE CANDIDATE ARCHITECTURES

1979 PERFORM DESIGN OF ARCHITECTURES AND USE "PAPER EMULATION" TO OBTAIN QUANTITATIVE RESULTS
SELECT "BEST" ARCHITECTURE

1980 DEMONSTRATE SYSTEM USING BREADBOARD

1981 BUILD AND TEST BRASSBOARD

AVAILABLE CMOS/SOS INTEGRATED CIRCUITS

MSFC AND SAMAO CUSTOM DEVICES

SAMSO ADVANCED COMPUTER TECHNOLOGY PROGRAM

RAYTHEON 290X RESEARCH PROGRAM

AIR FORCE MATERIALS LAB/RCA MICROPROCESSOR CHIP SET

CONCLUSION:

OF AVAILABLE CMOS/SOS TECHNOLOGY AFML/RCA MICROPROCESSOR CHIP SET HAS BEST POTENTIAL FOR USE IN SPACEBORNE APPLICATIONS

AFML/RCA CMOS/SOS MICROPROCESSOR CHIP SET

GPU TCS 129
- General Processing Unit
- 8-bit Parallel Slice
- Concatenatable
- Fully Static
- <125-ns Register-to-Register Add

RAM TCS 150
- Random-Access Memory
- 256x4-bit Organization
- <125-ns Access Time

ROM TCS 075
- Read-Only Memory
- Fully Static 1024 bits
- Mask-Programmable
- <100-ns Cycle Time

MUL TCS 196
- 8x8-bit Multiplier
- Expandable
- Completely Asynchronous
- Latched Input Operands

GUA TCS 093
- Gate Universal Array
- Customized Logic
- 632 Gate-Level Complexity
- 64 Pads
- Proven Cell Library
- 100-Mhz High-Speed Divider
- 452, 300 and 182 GUAs Also Available

"2910" Controller TCS 158
- Microprogram Controller
- Functional Equivalent to Am2910

GATE UNIVERSAL ARRAYS

FIXED REGULAR PATTERN OF TRANSISTORS AND ROUTING PATHS. BY DEFINING INTERCONNECTIONS AMONG DEVICES, GUAs MAY BE CUSTOMIZED WITH LOGIC VERY SIMILAR TO THE WAY READ ONLY MEMORY IS CUSTOMIZED WITH DATA.

MARTIN MARIETTA HAS DESIGNED THREE GUAs:

TCS 092-843, GPU CONTROLLER

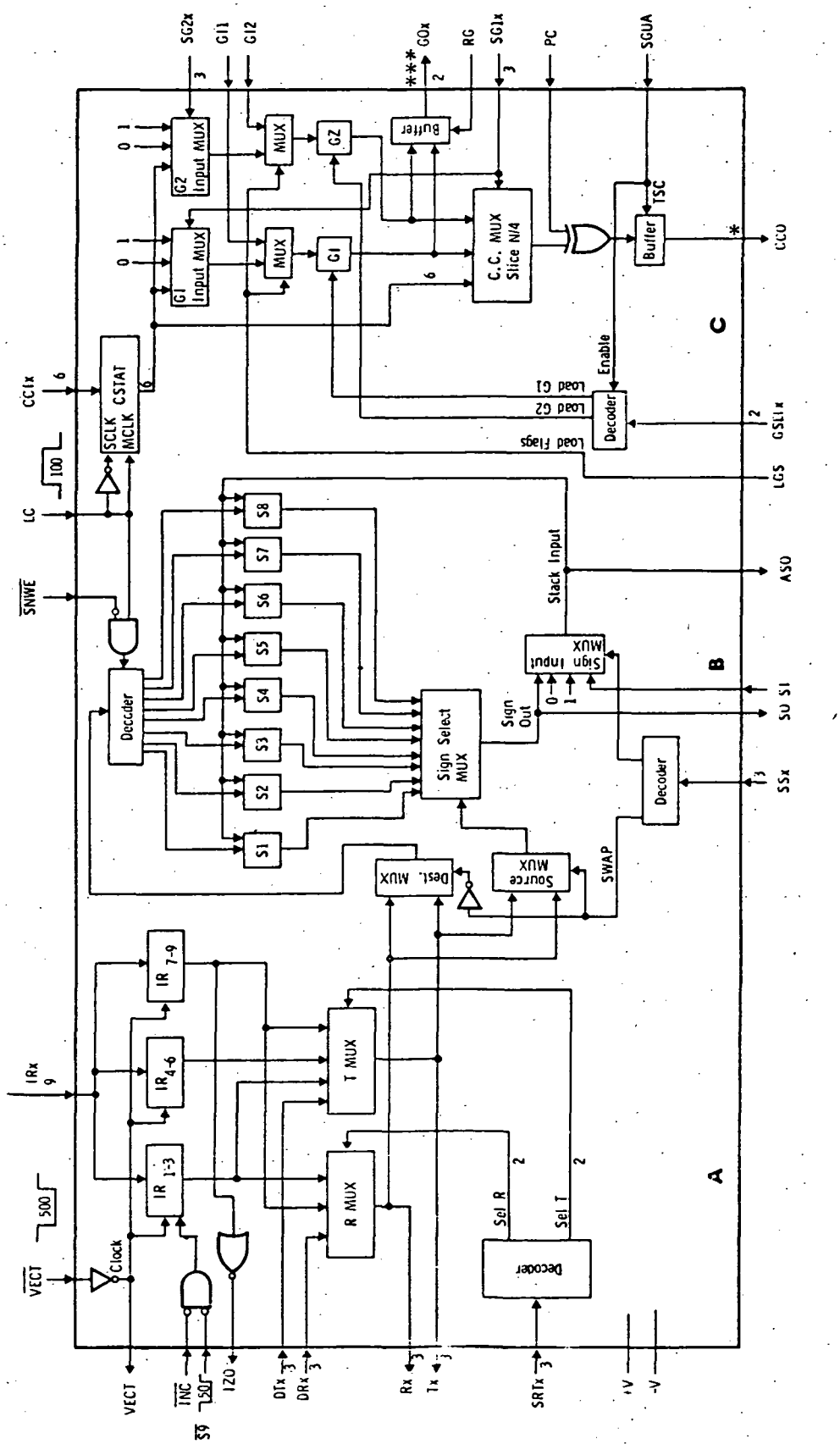
TCS 092-844, MEMORY CONTROLLER

TCS 093-845, SSI FUNCTIONS

TCS 092-843

FUNCTION:	GPU CONTROLLER
UTILIZATION:	368 INTERNAL CELLS
	62 I/O CELLS
	2 LOW Z CELLS
CIRCUITS:	A - REGISTER ADDRESS DECODE/ENCODE
	B - SIGN BIT FILE
	C - CONDITION CODE MUX

TCS 092-843 BLOCK DIAGRAM



MAC-16 COMPUTER DESIGN GOALS

LOW POWER (< 20 WATTS)

HIGH PERFORMANCE (> 250 KOPS)

MINICOMPUTER-LIKE INSTRUCTION SET ARCHITECTURE

FIXED POINT AND FLOATING POINT ARITHMETIC

PRIVILEGED AND USER MODE EXECUTION

MULTIPLE LEVEL INTERRUPT HANDLING

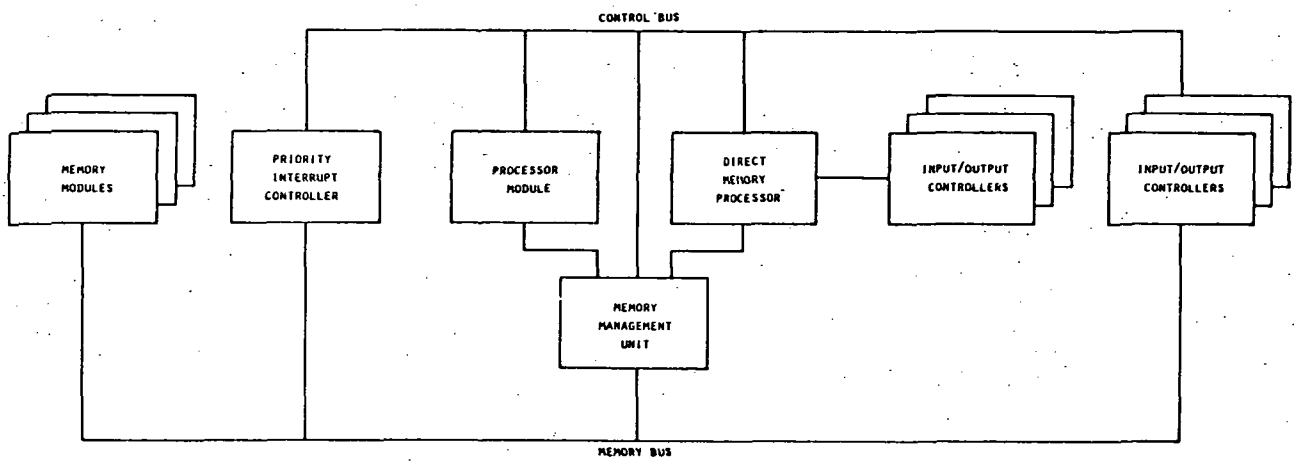
MEMORY MAPPED INPUT AND OUTPUT

DIRECT MEMORY ACCESS

MAC-16 COMPUTER PRIMARY HARDWARE MODULES

SP-D32:	CENTRAL PROCESSOR MODULE
PIC-16:	PRIORITY INTERRUPT CONTROLLER
MMU-A:	MEMORY BUS DRIVER/RECEIVER
MMU-B:	BASIC MEMORY MANAGEMENT UNIT
MMU-C:	EXTENDED MEMORY MANAGEMENT UNIT
RAM-8E:	HIGH SPEED 8K RANDOM ACCESS MEMORY
RAM-16E:	16K RANDOM ACCESS MEMORY
PROM-8:	8K PROGRAMMABLE READ ONLY MEMORY
DMP-8:	DIRECT MEMORY PROCESSOR

MAC-16 COMPUTER ARCHITECTURE



SP-D32 CENTRAL PROCESSOR PRINCIPLE ELEMENTS

FIXED POINT PROCESSOR

FLOATING POINT PROCESSOR

MICROPROGRAM CONTROL LOGIC

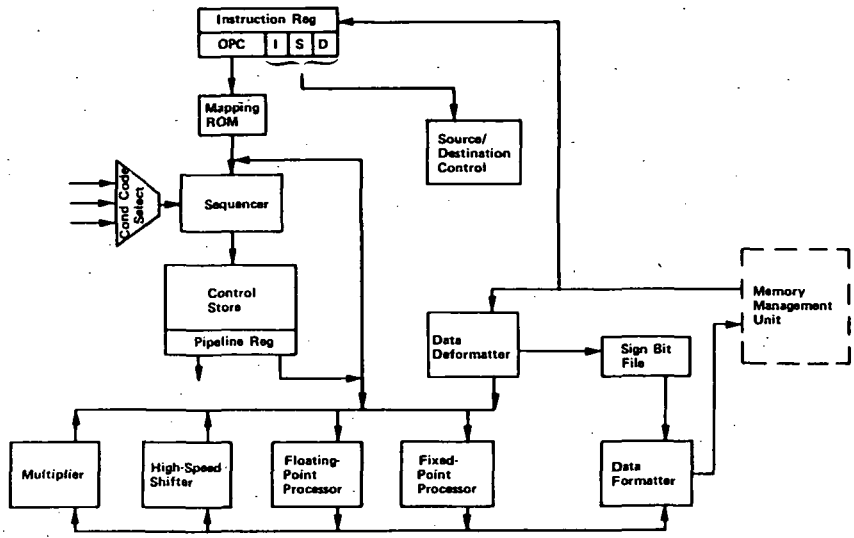
MULTIPLIER CIRCUIT

HIGH SPEED SHIFTER

DATA FORMAT AND DEFORMAT LOGIC

MEMORY INTERFACE

SP-D32 CENTRAL PROCESSOR MODULE OVERVIEW



SPACECRAFT CENTRAL PROCESSOR COMPARISON

	AUTONETICS DF224	LITTON 4516E	TELEDYNE MECA-43	IBM NSSC-II	ITEK ATAC-16	MARTIN MAC-16
FIXED POINT ADD (uS)	.8	2.0	1.6	1.7	1.25	2.0
FIXED POINT MUL (uS)	6.4	5.4	4.6	7.8	5.5	3.5
FLOATING POINT ADD (uS)	-	12.4	9.9	20.8	6.75	16.5
FLOATING POINT MUL (uS)	-	23.0	18.4	33.8	17.0	11.5
TECHNOLOGY	PMOS	TTL	TTL	TTL	TTL	CMOS/SOS
POWER (WATTS)	15.5	22	25.5	100	21	2
IC COMPONENT COUNT	50	107	5	84	?	89
REMARKS	24 BIT FIXED POINT		HYBRID PCKG		JPL MEMORY	

MAC-16 HARDWARE STATUS		REQMTS	DESIGN	BREADBOARD
SP-D32:	CENTRAL PROCESSOR MODULE	COMPLETE	COMPLETE	IN PROGRESS
PIC-16:	PRIORITY INTERRUPT CONTROLLER	COMPLETE	IN PROGRESS	1981
MMU-A:	MEMORY BUS DRIVER/RECEIVER	COMPLETE	COMPLETE	IN PROGRESS
MMU-B:	BASIC MEMORY MANAGEMENT UNIT	COMPLETE	IN PROGRESS	NOT SCHEDULED
MMU-C:	EXTENDED MEMORY MANAGEMENT UNIT	COMPLETE	NOT SCHEDULED	NOT SCHEDULED
RAM-8E:	HIGH SPEED 8K RANDOM ACCESS MEMORY	COMPLETE	COMPLETE	IN PROGRESS
RAM-16E:	16K RANDOM ACCESS MEMORY	COMPLETE	IN PROGRESS	1981
PROM-8:	8K PROGRAMMABLE READ ONLY MEMORY	COMPLETE	COMPLETE	IN PROGRESS
DMP-8:	DIRECT MEMORY PROCESSOR	COMPLETE	1981	NOT SCHEDULED

DEMONSTRATION UNIT PRIMARY ELEMENTS

MAC-16 COMPUTER ENGINEERING DEVELOPMENT UNIT

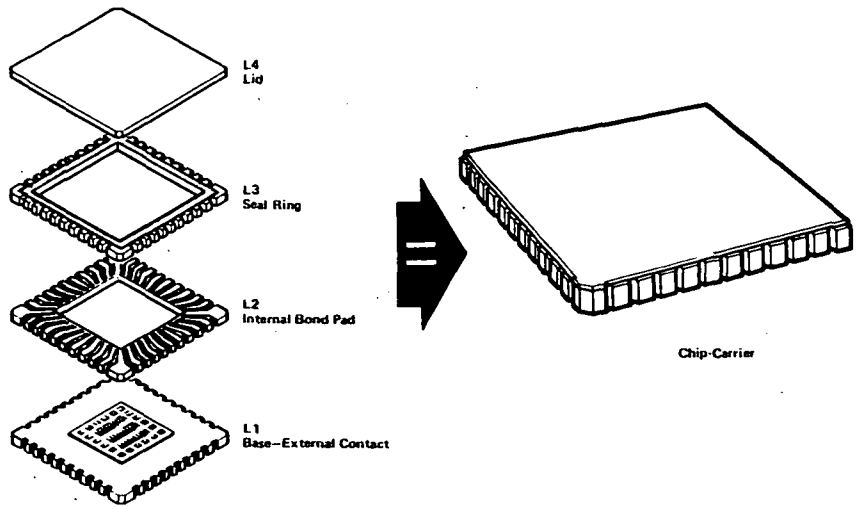
SP-D32	CENTRAL PROCESSOR MODULE
PIC-16	PRIORITY INTERRUPT CONTROLLER
MMU-A	MEMORY BUS DRIVER/RECEIVER
RAM-8E	RANDOM ACCESS MEMORY
PROM-8	PROGRAMMABLE READ ONLY MEMORY

SUPPORT EQUIPMENT

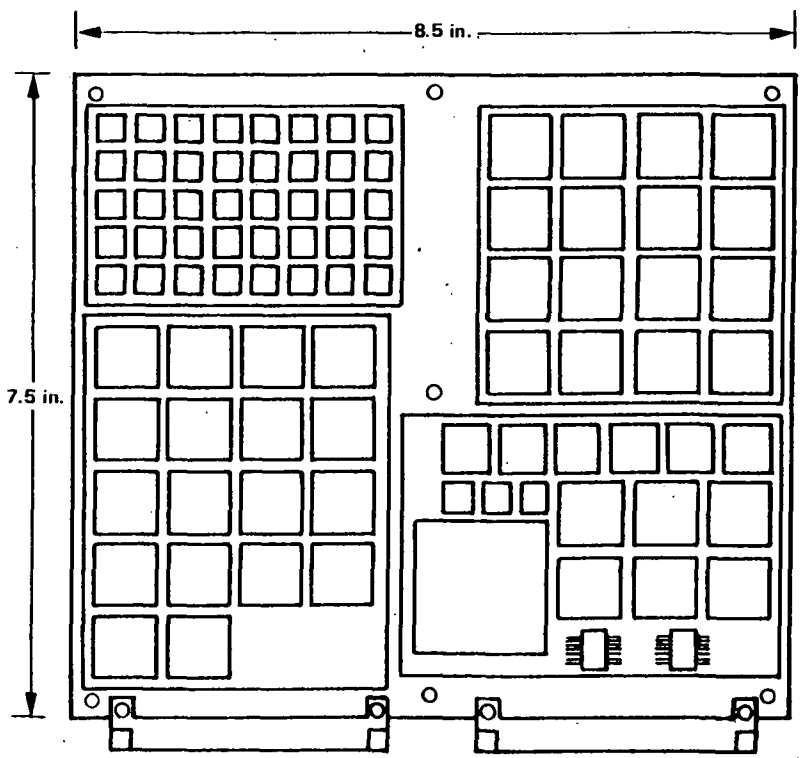
- SERIAL I/O MODULE
- OPERATOR CONTROL PANEL
- WRITABLE CONTROL STORE
- GUA TTL CIRCUIT EQUIVALENTS

MICROCOMPUTER - HARDWARE INTERFACE

VAX 11/780 - SHOFTWARE HOST



SP-D32 CENTRAL PROCESSOR MODULE FLIGHT UNIT



Quantity	Part	Package
43	TCS 075	24 HCC
1	TCS 158	48 HCC
5	TCS 129	48 HCC
16	TCS 196	64 HCC
4	TCS 092-843	64 HCC
1	TCS 092-844	64 HCC
19	TCS 093-845	64 HCC
2	Resistor Pack	16 FP
1	E34 TCXO	Hybrid
2	110 Lead Connectors	–
–	Capacitors	–

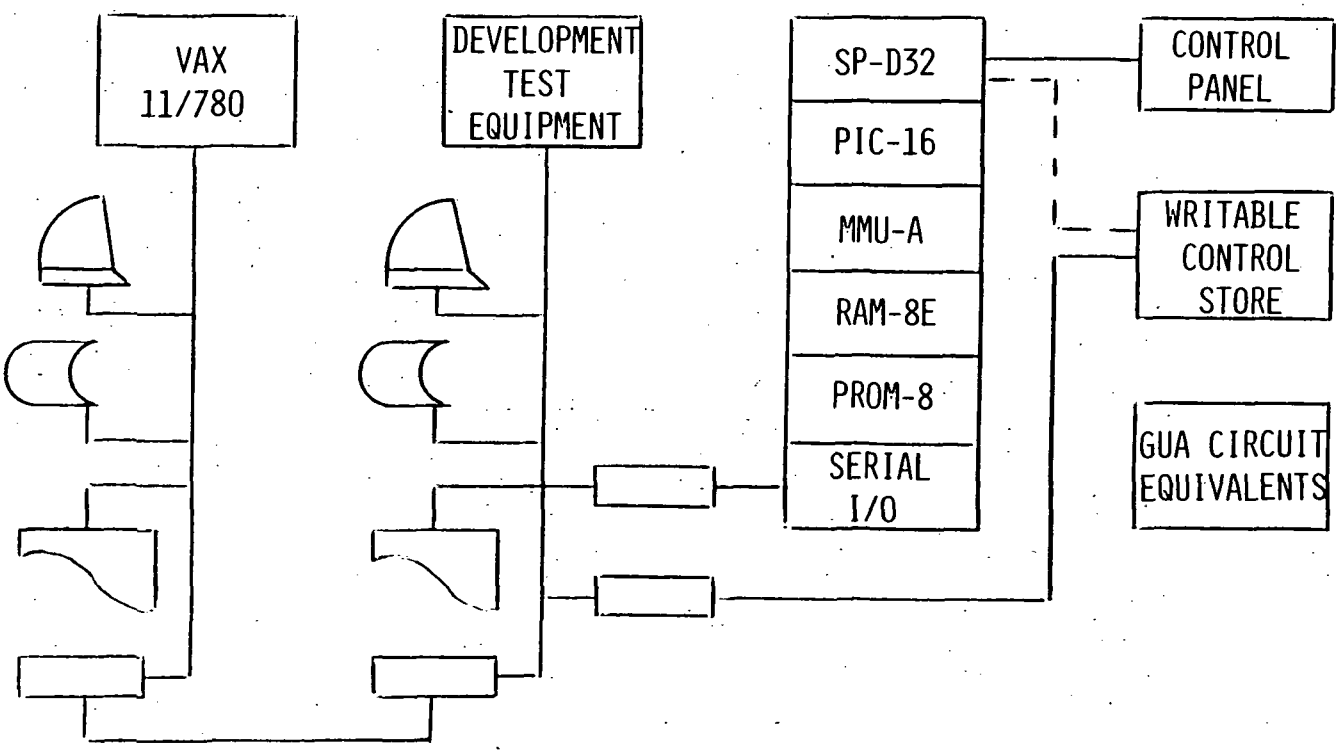
1981 HARDWARE OBJECTIVES

BUILD AND FUNCTIONAL TEST OF PRINTED CIRCUIT BOARDS FOR PROCESSOR MODULE, MEMORY MANAGEMENT UNIT, PRIORITY INTERRUPT CONTROLLER, AND 8K MEMORY MODULE

FUNCTIONAL TEST OF 4K RAMs (TCS 146) FOR AIR FORCE MATERIALS LAB

PERFORM PACKAGING MINI-QUALIFICATION TEST

MAC-16 COMPUTER TEST SET UP



MAC-16 PROJECTED FLIGHT UNIT DATA

SYSTEM CONFIGURATION

- 1 SP-D32
- 1 MMU-B
- 4 RAM-16E (64K WORDS)
- 1 DMP-8
- 1 PIC-16

WEIGHT ESTIMATE = 5.9 LBS

POWER ESTIMATE 10 WATTS