

**EVOLUTION OF A STANDARD
MICROPROCESSOR-BASED SPACE COMPUTER**

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Starting in 1976, an existing in-inventory computer hardware/software package (B-1 RFS/ECM) was repackaged and applied to multiple missile/space programs. Concurrent with the application efforts, low-risk modifications were made to the computer from program to program to take advantage of newer, advanced technology and to meet increasingly more demanding requirements (computational and memory capabilities, longer life, and fault tolerant autonomy).

In 1978, the 2901 microprocessor chip was incorporated; and since that time advances in this mature, multi-sourced, qualified chip (specifically the 2901B) have been used to improve computational capability.

This development establishes a base to explore the use of newer microprocessors and to discuss current trends from centralized to distributed processors. Key differences in computational and memory capabilities, orbital life, and autonomous fault-tolerant provisions are compared.

In summary, it is concluded that microprocessors hold promise in a number of critical areas for future space computer applications. However, the benefits of the DoD VHSIC Program are required and the old proliferation problem must be revised.

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OUTLINE

1. UNIQUE REQUIREMENTS OF SPACE COMPUTERS
2. STATE-OF-THE-ART SPACE COMPUTER (BASELINE)
3. STATISTICS OF BASELINE COMPUTER
4. DESIRED IMPROVEMENTS IN BASELINE COMPUTER
5. CURRENT TRENDS AND TRADEOFFS IN COMPUTERS
6. USE OF NEWER MICROPROCESSORS
7. SUMMARY

UNIQUE REQUIREMENTS OF SPACE COMPUTERS

LOW POWER

POWER IMPACTS

- THERMAL BALANCE OF SATELLITE
- RELIABILITY
- POWER SOURCE CAPABILITY

ENVIRONMENTAL DESIGN

- VIBRATION (20 g RMS)
- PYROTECHNIC SHOCK (3,000 g)
- SPACE RADIATION (INCLUDING COSMIC RAYS)
- EMI (MIL-STD-1541)
- OUTGASSING (SP-R-0022A AND JSC-08962)
- POWER SOURCE (21V TO 35V DC)
- THERMAL (-34C TO +71C "COLD PLATE")

(CONT)

UNIQUE REQUIREMENTS OF SPACE COMPUTERS (CONT)

HIGH RELIABILITY (LONG ORBIT LIFE WITH HIGH PROBABILITY)

- MATURE TECHNOLOGY
- SIMPLICITY
- WORST-CASE DESIGN
- EXTRA-RELIABILITY PARTS
- EXTRA-QUALITY WORKMANSHIP/INSPECTION
- EXTENSIVE UNIT TESTING
 - RANDOM VIBRATION
 - THERMAL CYCLING
 - THERMAL VACUUM OPERATION
 - BURN-IN
- ELIMINATION OF SINGLE-POINT FAILURE MODES
 - REDUNDANCY
 - FAULT-TOLERANT AUTONOMY

SATELLITE THERMAL BALANCE IN ORBIT *

<u>MAX INTERNAL POWER DISSIPATION</u>	<u>AVG. SURFACE TEMPERATURE</u>
8,200 WATTS	60°F
13,000 WATTS	115°F

ASSUMPTIONS

- SATELLITE - SPHERE, WHITE SURFACE, 10 FT DIAMETER
- SIMPLE THERMAL MODEL UTILIZED
- HEAT SOURCES - SUN, EARTH, INTERNAL POWER DISSIPATION
- HEAT SINK - SPACE

*THERMAL BALANCE EFFECTS

- MAX INTERNAL POWER DISSIPATION
- POWER SOURCE CAPABILITY
- RELIABILITY

UNIT ACCEPTANCE TESTING

1. INSPECTION
2. PERFORMANCE TEST
3. RANDOM VIBRATION TEST
 - DURATION 60 SEC/AXIS (ALL AXES)
 - OVERALL 9.2 gRMS
4. FUNCTIONAL TEST
5. THERMAL CYCLING (THIS TEST TAKES APPROXIMATELY 160 HRS, OR 6.67 DAYS)
 - EIGHT CYCLES TOTAL
 - 11C TO +61C
 - CONTINUOUS UNIT OPERATION
6. FUNCTIONAL TEST

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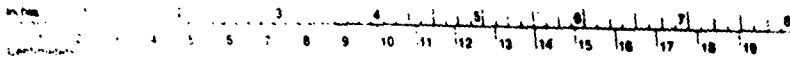
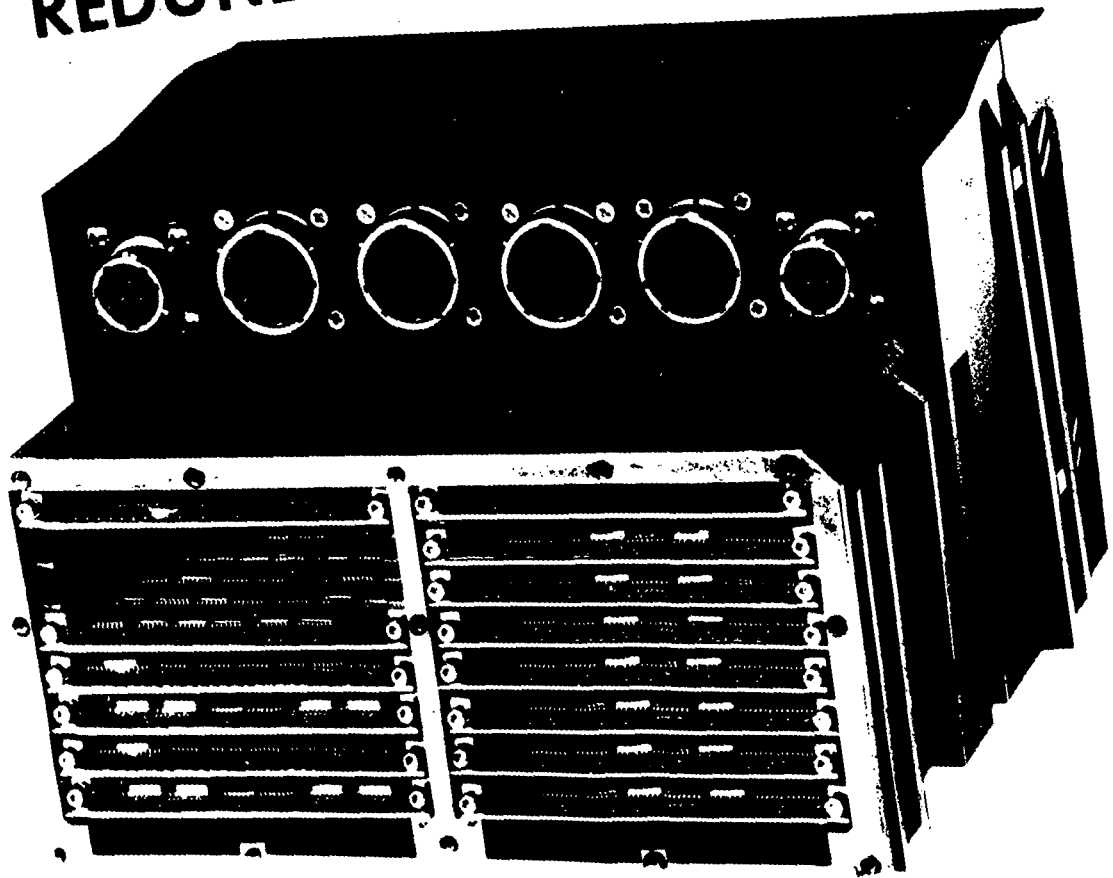
UNIT ACCEPTANCE TESTING (CONT)

7. OPERATING ORBIT THERMAL VACUUM TEST
 - 12-HOUR SOAKS AT -11C AND +61C, AFTER STABILIZATION, AND BEFORE
 - FUNCTIONAL TESTS AT -11C AND +61C
 - UNIT OPERATING CONTINUOUSLY
8. FUNCTIONAL TEST
9. PIN-RETENTION TEST (MIL-STD-1344A, METHOD 2014)
10. FUNCTIONAL TEST
11. BURN-IN TEST
 - +61C CONTINUOUS
 - UNIT OPERATING CONTINUOUSLY
 - 300 HR DURATION (12.5 DAYS)
 - DIAGNOSTICS TEST
 - GALWREC MEMORY TEST
12. PERFORMANCE TEST
13. POST TEST INSPECTION

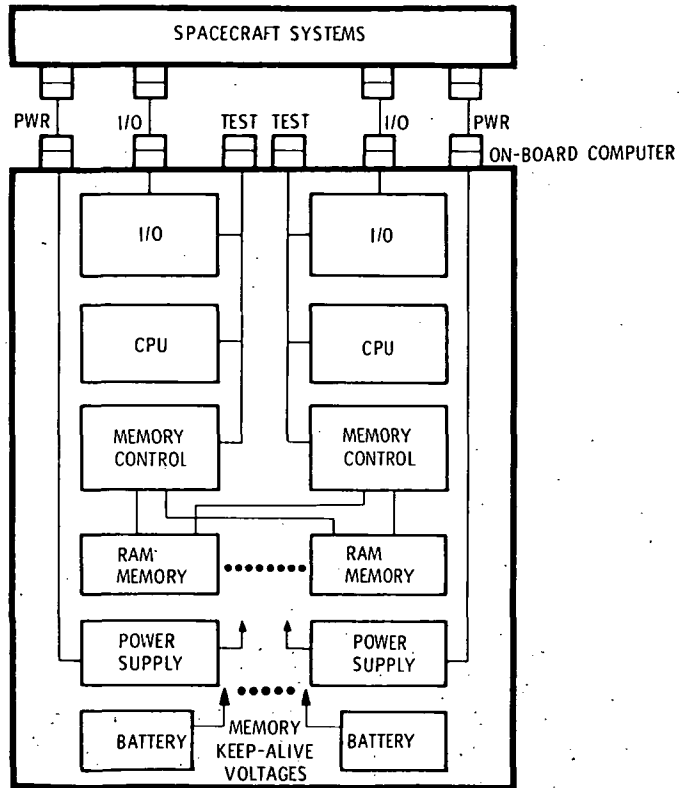
A STATE-OF-THE-ART SPACE COMPUTER (Baseline)

Based on 2901 (Now 2901B)
Microprocessor Chip

REDUNDANT COMPUTER



REDUNDANT COMPUTER



REDUNDANT COMPUTER

VOLUME	466 CU IN.
WEIGHT	26.4 LBS
POWER	77.3 WATTS (96K-WORDS ACTIVE)
THROUGHPUT	539 KOPS (GIBSON MIX)
MEMORY	128K-WORDS (ACTIVE/STANDBY) (ADDRESSING TO 256K-WORDS)
RELIABILITY	0.966 (5 YRS) (WITH 64K-WORDS ACTIVE, 16K-WORDS STANDBY)

STATISTICS OF BASELINE COMPUTER

POWER BREAKDOWN

CPU	26%
MEMORY	19
I/O	17
	—
S/T	62
POWER SUPPLY	38*
	—
TOTAL	100%

*62% EFFICIENCY, WORST CASE DUE
TO POWER SOURCE CHARACTERISTICS

FLIGHT UNIT COST BREAKDOWN

MATERIAL	64%
ASSEMBLY	16
TEST/INSPECTION	20
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TOTAL	100%

FLIGHT UNIT COST BREAKDOWN

CPU	11%
MEMORY	59*
I/O	6
POWER SUPPLY	6
OTHER	18
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	100%

*128K-WORDS TOTAL (ACTIVE/STANDBY)

FAILURE RATE BREAKDOWN

CPU	38%
MEMORY	23*
I/O	29
POWER SUPPLY	8
OTHER	2
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TOTAL	100%

*REFLECTS FAULT-TOLERANT MEMORY EFFECTS
(THIS IS RESIDUAL)

SPACE COMPUTER PROJECT COST BREAKDOWN

FLIGHT UNIT	18%
SUPPORT	40*
SOFTWARE	42
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TOTAL	100%

*INCLUDES SPARE FLIGHT UNIT

SUMMARY

MICROPROCESSORS COULD IMPACT BASELINE COMPUTER,
WHOSE STATISTICS YIELD:

- CPU 26% OF POWER
(EXCLUSIVE OF P.S. DISSIPATION PENALTY)
- CPU 11% OF FLIGHT UNIT COST
- CPU 38% OF FAILURE RATE
- SOFTWARE 42% OF PROJECT COST

DESIRED IMPROVEMENTS (IN BASELINE)

- FAULT-TOLERANT AUTONOMY
- HARDER RADIATION TOLERANCE
 - TOTAL IONIZING DOSE
 - SINGLE EVENT UPSETS
- LOWER POWER
- IMPROVED COMPUTATIONAL CAPABILITY
- LONGER ORBIT LIFE WITH HIGH PROBABILITY
- LOWER SOFTWARE COSTS

CURRENT TRENDS

- CENTRALIZED SIMPLEX COMPUTER ARCHITECTURES DEMANDING HIGHER WORKLOAD CAPABILITIES
- DISTRIBUTED SYSTEMS WITH FOLLOWING INTERPRETATIONS:
(FALL OUT OF POINT-OF-USE SYSTEMS, RESOURCE-SHARING NETWORKS, MULTIPLE PROCESSOR SYSTEMS ARCHITECTURES)
 - MULTIPROCESSORS (TO HANDLE LOAD), STILL CENTRALIZED
 - DEDICATED COMPUTERS (PER FUNCTION), LOOSELY FEDERATED
 - FEDERATED COMPUTER ARCHITECTURE WITH SYSTEM MGR AND DEDICATED SUBSYSTEM COMPUTERS
 - DISTRIBUTION OF TASKS/WORKLOADS AMONG NONDEDICATED COMPUTERS
 - COMBINATIONS OF ABOVE

TRADEOFFS

CENTRALIZED SYSTEM ADVANTAGES*

- MORE EFFICIENT LOAD SHARING AND LOWER RESPONSE TIME
- GREATER FLEXIBILITY
- MORE EFFICIENT COMMUNICATION
- LESS REDUNDANCY OF STORAGE
- GREATER TOTAL COMPUTATIONAL CAPABILITY
- HIGHER TOTAL SYSTEM RELIABILITY
- MORE EFFECTIVE USE OF REDUNDANCY

DEDICATED SYSTEM ADVANTAGES

- LESS COMPLEX SOFTWARE
- HIGHER RELIABILITY FOR INDIVIDUAL FUNCTIONS

*INCLUDES INTEGRATED, MULTIPROCESSOR, CENTRALIZED SYSTEMS

SUMMARY

MICROPROCESSORS COULD IMPACT BASELINE COMPUTER,
WHOSE CENTRALIZED COMPUTER ARCHITECTURE YIELDS:

- MORE COMPLEX SOFTWARE
- LESS RELIABILITY FOR INDIVIDUAL FUNCTIONS

UTILIZATION OF NEWER MICROPROCESSORS

MICROPROCESSOR POTENTIAL IMPACT (ON BASELINE)

ON BASELINE STATISTICS OF:

- CPU 26% OF POWER
- CPU 11% OF FLIGHT UNIT COST
- CPU 38% OF FAILURE RATE
- SOFTWARE 42% OF PROJ. COST
- PROMISING
- PROMISING
- PROMISING (BUT NOT YET MATURE)
- PROMISING (BUT NOT ASSURED)

ON DESIRED BASELINE IMPROVEMENTS OF:

- LONGER ORBIT LIFE
- FAULT-TOLERANT AUTONOMY
- IMPROVED COMPUTATIONAL CAPABILITY
- LOWER SOFTWARE COSTS
- HARDER RADIATION TOLERANCE
- PROMISING
- POTENTIAL NOT CLEAR
- PROMISING
- DEPENDENT ON REUSE OF SOFTWARE
- MICROPROCESSOR TECHNOLOGIES AND HIGHER LEVELS OF INTEGRATION OF FUNCTIONS ON A CHIP ARE NOT CONDUSIVE TO RADIATION HARDENING TOLERANCE (DoD VHSIC PROGRAM WILL HELP)

ON CENTRALIZED SYSTEM ARCHITECTURE

DISADVANTAGES

- MORE COMPLEX SOFTWARE
- LESS RELIABILITY PER FUNCTION
- PROMISING
- PROMISING

SUMMARY

- MICROPROCESSORS BEING DRIVEN BY LARGE COMMERCIAL MARKETPLACE
- MICROPROCESSORS LOOK PROMISING IN A NUMBER OF CRITICAL AREAS FOR FUTURE SPACE COMPUTER APPLICATIONS
- DoD VHSIC PROGRAM COULD HELP SOLVE CRITICAL RADIATION HARDENING PROBLEMS
- REUSE OF SOFTWARE A CRITICAL ITEM
- USE OF LARGE NUMBER OF MICROPROCESSOR TYPES FOR FUTURE SPACE APPLICATIONS NOT WISE, AND CHOICE WILL BE DIFFICULT
- FAULT-TOLERANT AUTONOMY NEEDS ATTENTION

KEY AREAS NEEDING STRESS

REDUNDANCY MANAGEMENT

FAULT TOLERANCE

SOFTWARE DEVELOPMENT