MODULAR MISSILE BORNE COMPUTERS

R. Ramseyer, R. Arnold, H. Applewhite and R. Berg
Honeywell Systems and Research Center
Minneapolis, Minnesota

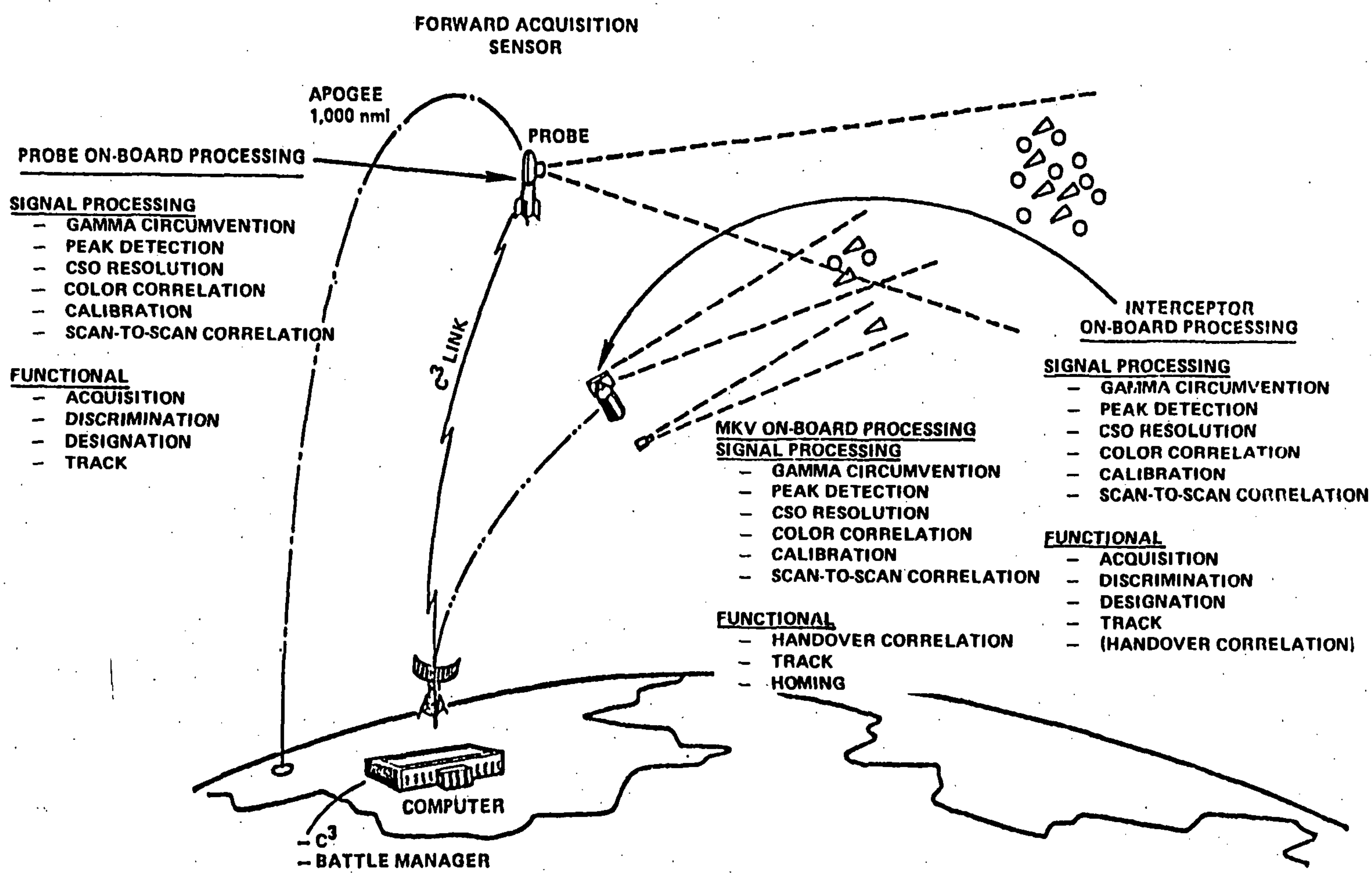
The increasing real time signal and data processing loads on-board BMD interceptors cannot be met with currently available and flyable processors. The Modular Missile Borne Computer is being developed to provide a solution to that problem through the use of a collection of microprocessors in a distributed processing system.

This paper discusses the Modular Missile Borne Computer's architecture with emphasis on how that architecture evolved from a careful analysis of both the physical constraints and the processing requirements. The development techniques used are generally applicable to real-time data processing systems and have resulted in the achievement of one of our most significant design goals. This goal is a modular, flexible, extensible system capable of adapting to evolving BMD problems as well as others where an ultra-high performance distributed processor is desirable.

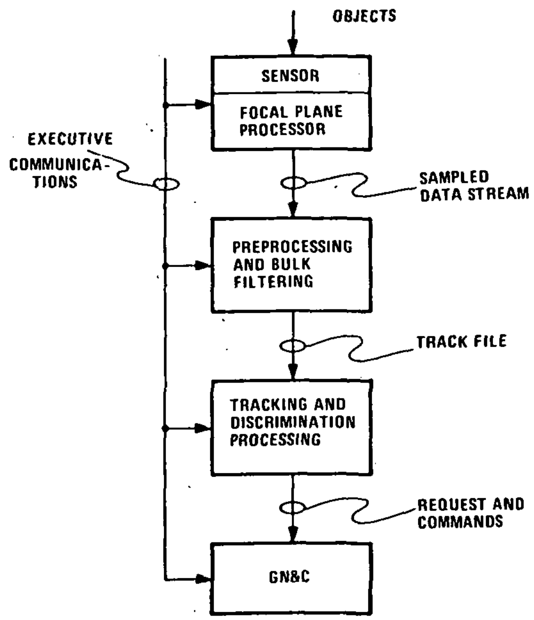
The general objective for the MMBC program is the development of a data processing system which lends itself readily to system growth, reconfiguration and changes in application or environment. Given the constraints and requirements imposed by the BMD threat, scenarios and environmental considerations, four driving architectural considerations result:

- The required processing is real time.
- There is a massive quantity of data and it is received at a rapid rate.
- A high degree of modularity, flexibility and potential for growth is desired in MMBC.
- MMBC must be capable of performing in an extremely hostile operating environment (e.g. shock, vibration, temperature, and nuclear).

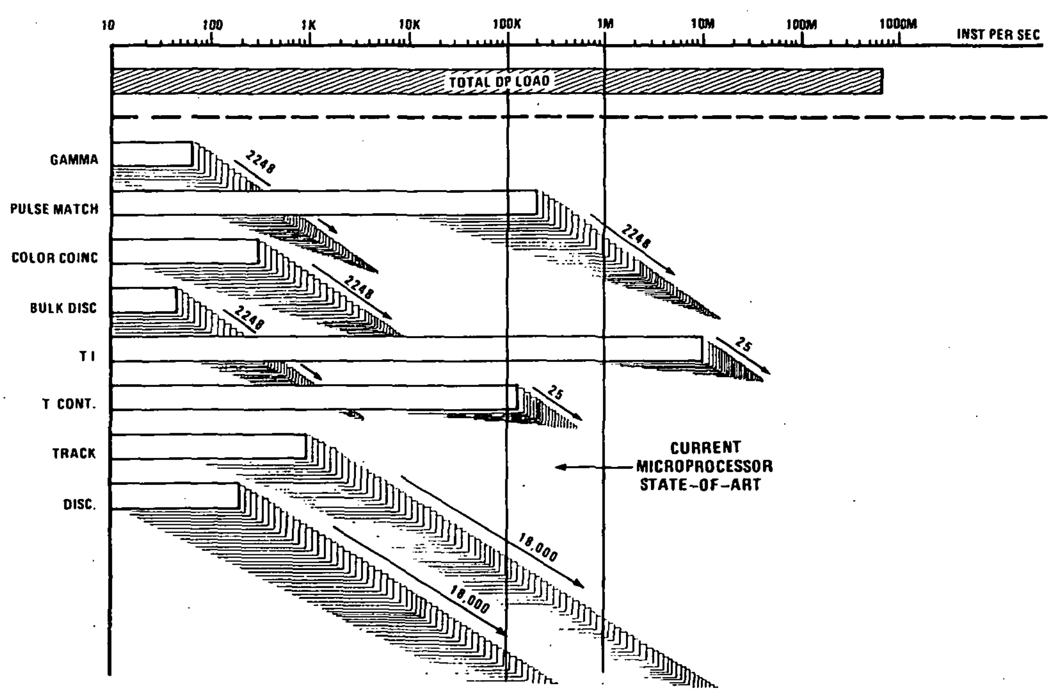
DATA PROCESSING IN A MIDCOURSE SYSTEM



HIGH LEVEL PROCESSOR STRUCTURE

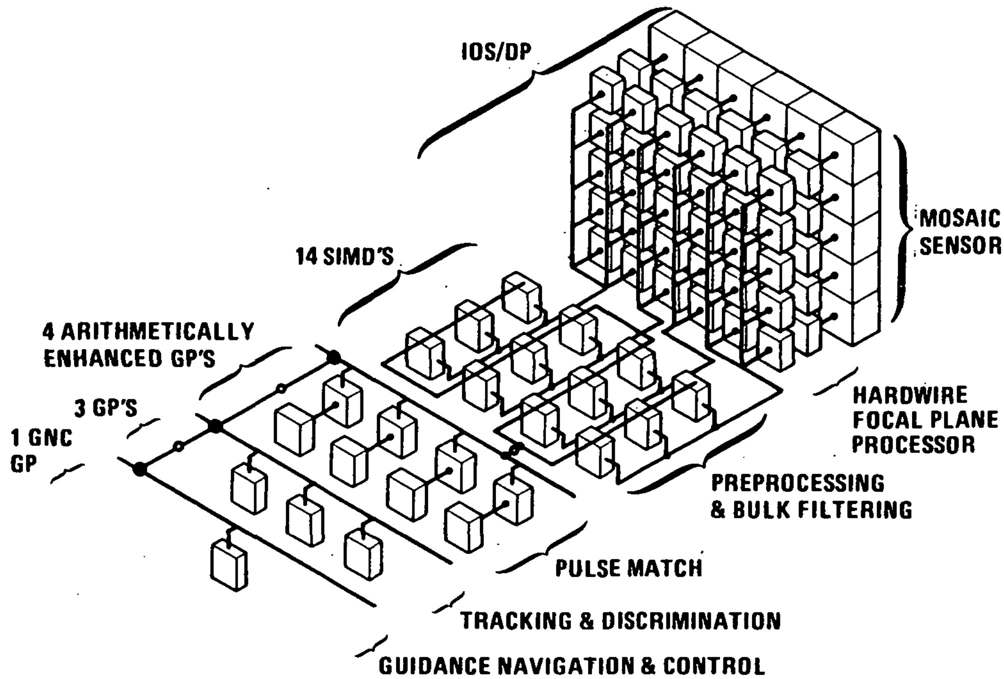


TOTAL DP LOAD IS COMPOSED OF MANY SMALL, INDEPENDENT LOADS



MODULAR MISSILE-BORNE COMPUTERS

OBJECTIVE: INVESTIGATE ADVANCED PREPROCESSING TECHNOLOGY & THE APPLICATION OF MODULAR, FLEXIBLE, EXTENDABLE MICROCOMPUTER ARRAYS TO PERFORM THE REAL TIME DATA PROCESSING NECESSARY ON BOARD A BMD INTERCEPTOR.



RATIONALE: ADVANCES IN INTERCEPTOR & TECHNOLOGY AS WELL AS INCREASING COMPUTATION OF BMD FUNCTIONS ON BOARD IMPOSE REQUIREMENTS ON THE DATA PROCESSOR THAT CANNOT BE MET BY CONVENTIONAL COMPUTER ARCHITECTURES. MODULAR, FLEXIBLE, AND EXTENDABLE COMPUTER STRUCTURES ARE REQUIRED TO MEET THE NEEDS OF THE FLUID AND RAPIDLY EVOLVING BMD SYSTEMS.

BENEFITS OF MICROPROCESSORS

- ALLOW MAXIMUM USE OF LSIC HARDWARE
  - MINIMIZES SIZE/WEIGHT/POWER/INTERCONNECTS
- SPECIAL PURPOSE OPERATION CAN BE ACHIEVED THROUGH MICROPROGRAMMING
- SIMULTANEOUS OPERATION OF MANY REAL TIME HARDWARE UNITS DRASTICALLY REDUCES NEED FOR MULTIPROGRAMMING
  - REDUCED SOFTWARE COST
  - REDUCED OVERHEAD TIME
- ALLOWS MAXIMUM MODULARITY TO BE ACHIEVED WHICH IMPROVES
  - FAULT TOLERANCE
  - FLEXIBILITY /ALTERABILITY

APPROXIMATE CAPABILITIES AND REQUIREMENTS

PROCESSING SECTION	PROCESSOR CONFIGURATION	REQUIREMENT	CAPABILITY
PREPROCESSING AND BULK FILTERING			
DMX TO PULSE MATCH	14 SIMD (1 TO 3 MIPS EA)	22 MIPS	~40 MIPS*
PULSE MATCH	4 GP W/SPECIAL ARITHMETIC (15 MIPS FOR PULSE MATCH; 1 MIPS OTHERWISE)	43 MIPS	45 MIPS
TRACKING AND DISCRIMINATION	3 GP (1 MIPS EACH)	151 KIPS	3 MIPS
GUIDANCE NAVIGATION AND CONTROL	1 GP (500 KIPS)	185 KIPS	500 KIPS
TOTAL CAPACITY			88.5 MIPS

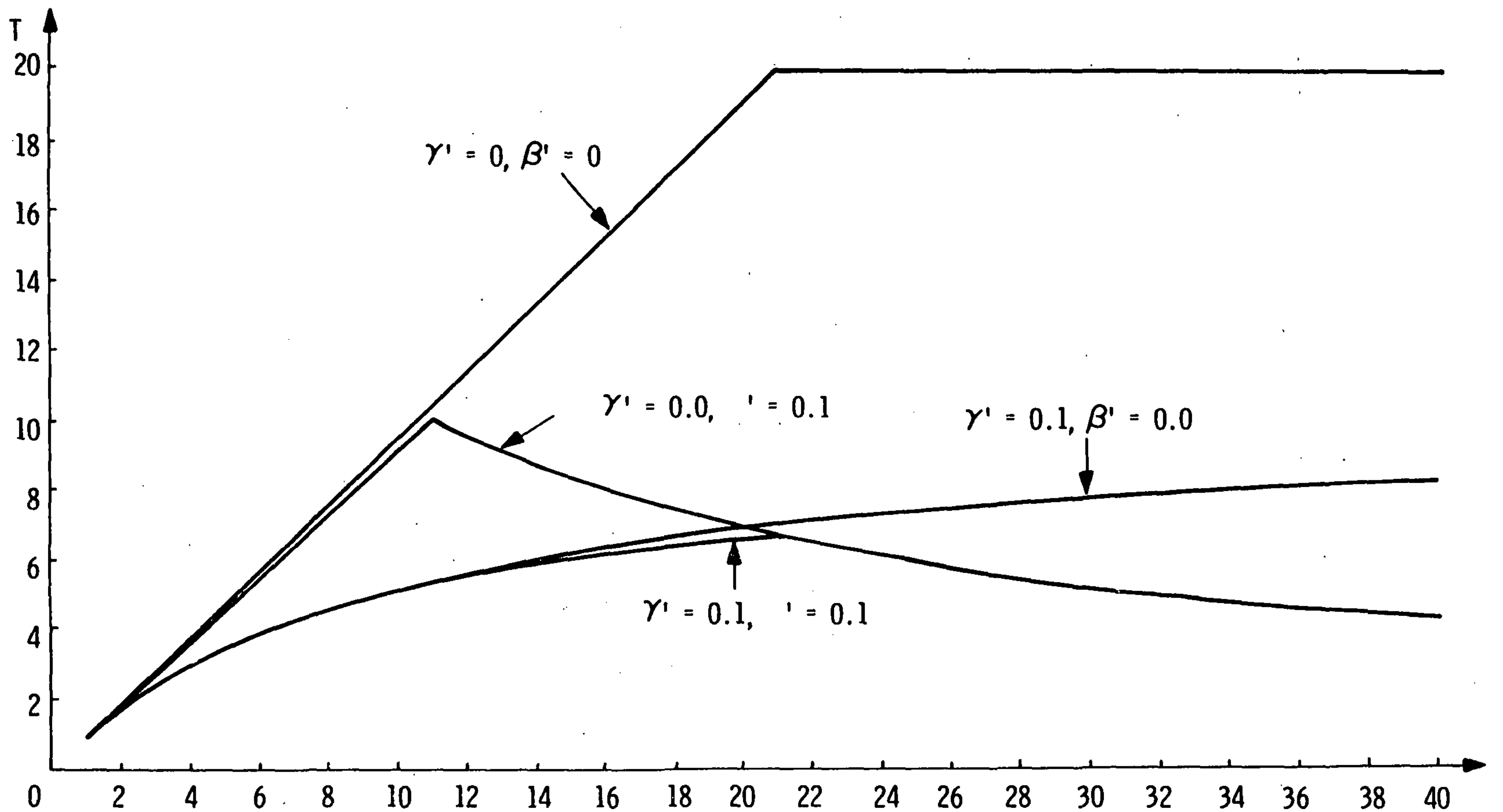
*HIGH THROUGHOUT REQUIRED TO ABSORB OVERHEAD AND SATISFY REAL-TIME RESPONSE REQUIREMENT.

EACH COMPUTER IN MMBC IS "TUNED" TO PERFORM WELL IN ITS AREA OF APPLICATION. E.G., MULTIPLE DATA STREAM PROCESSORS IN BULK FILTERING; PIPELINED, FAST ARITHMETIC UNIT IN PULSE MATCH.

CHARACTERISTICS OF HARDWARE MODULES

GENERAL PROCESSING ELEMENT (16 BITS)	1 MIPS
SIMD PE (3 ALU'S)	3 MIPS
VOA PROCESSOR	15 MIPS/5 MIPS
LOCAL MEMORY (3 PORT RAM)	
READ ACCESS TIME	270 ns
WRITE ACCESS TIME	75 ns
COMMON BULK MEMORY	
READ	375 ns
WRITE	140 ns
CYCLE	425 ns
GLOBAL BUS (3 BUSES)	
TRANSFER RATE	1 M WORDS/S 1 M WORDS/S
CAN HANDLE 40 K TRACKS/SEC/GLOBAL BUS	
UTILIZATION	60%

IDEALIZED SHARING-THROUGHPUT VERSUS NUMBER OF PROCESSORS



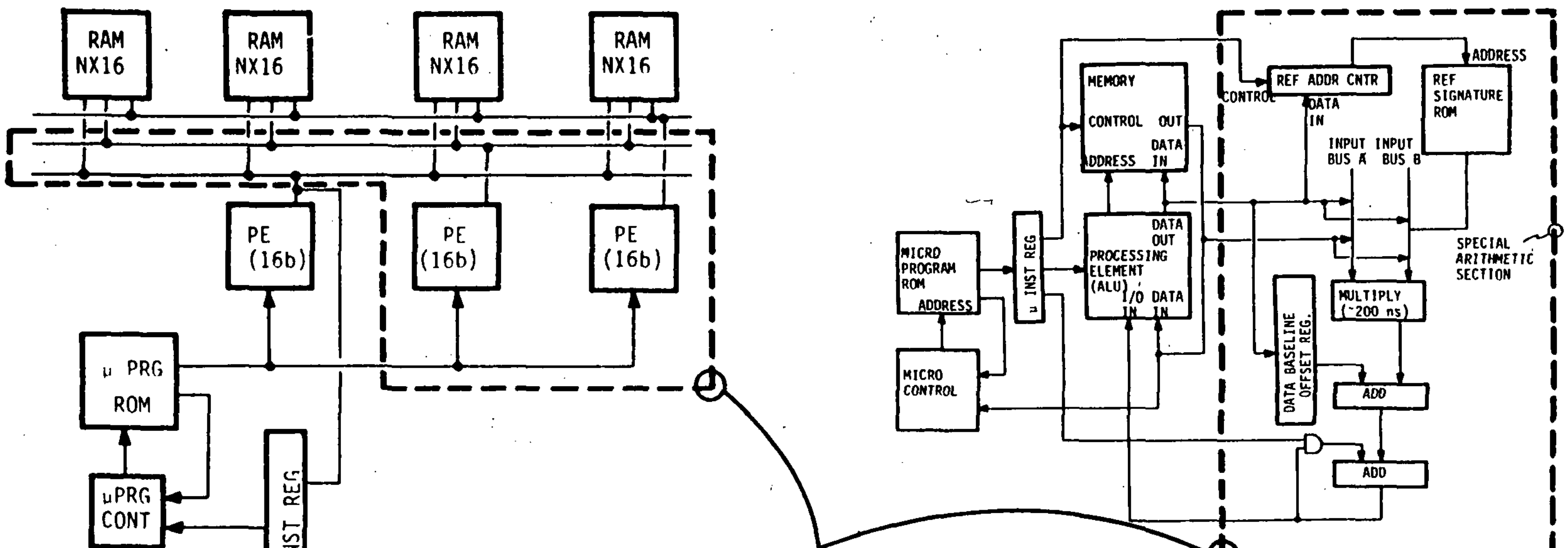
THROUGHPUT FOR E/I = 20

HARDWARE ARCHITECTURE

- REQUIRES MULTICOMPUTER
- MODULARITY, FLEXIBILITY, EXTENDABILITY REQUIRED
- OVERHEAD RESULTING FROM DISTRIBUTION MUST BE CONTROLLED
- REQUIRES SPECIAL PURPOSE HARDWARE
- SYSTEM MUST BE MANAGEABLE
- NO. OF COMPUTERS LIMITED BY SIZE, WT., POWER, PROBLEM STRUCTURE

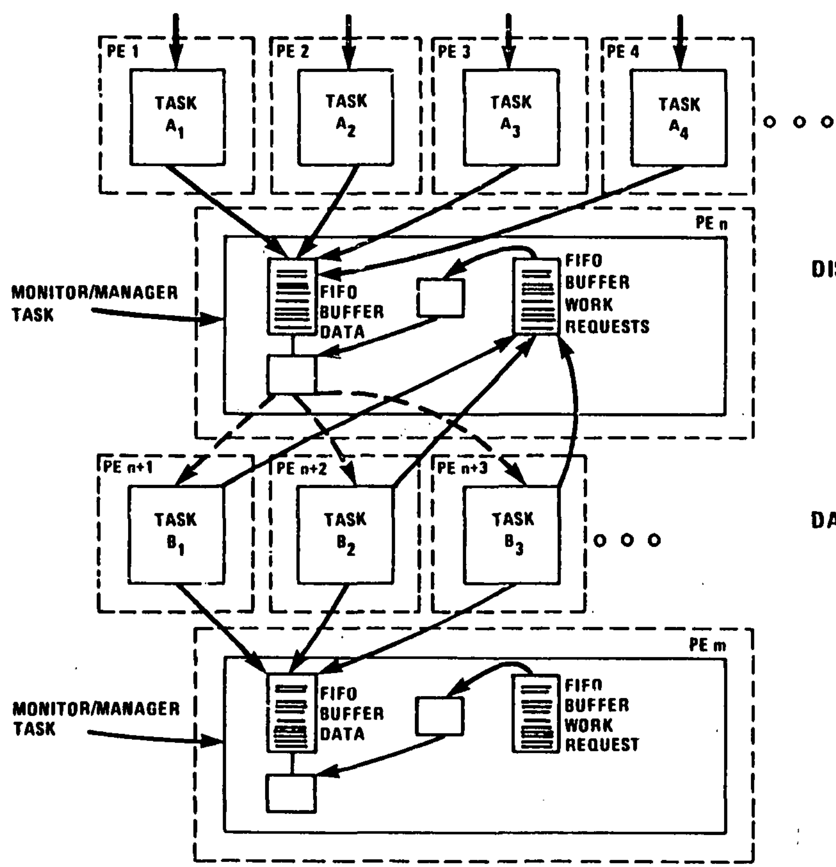
THEREFORE:

- EACH COMPUTER SHOULD BE AS POWERFUL AS POSSIBLE
- EACH COMPUTER CAN BE AUGMENTED TO PERFORM A CLASS OF ALGORITHMS WELL
- HARDWARE MUST ADAPT EASILY TO ALGORITHM STURCTURES



AUGMENTATION EXAMPLES

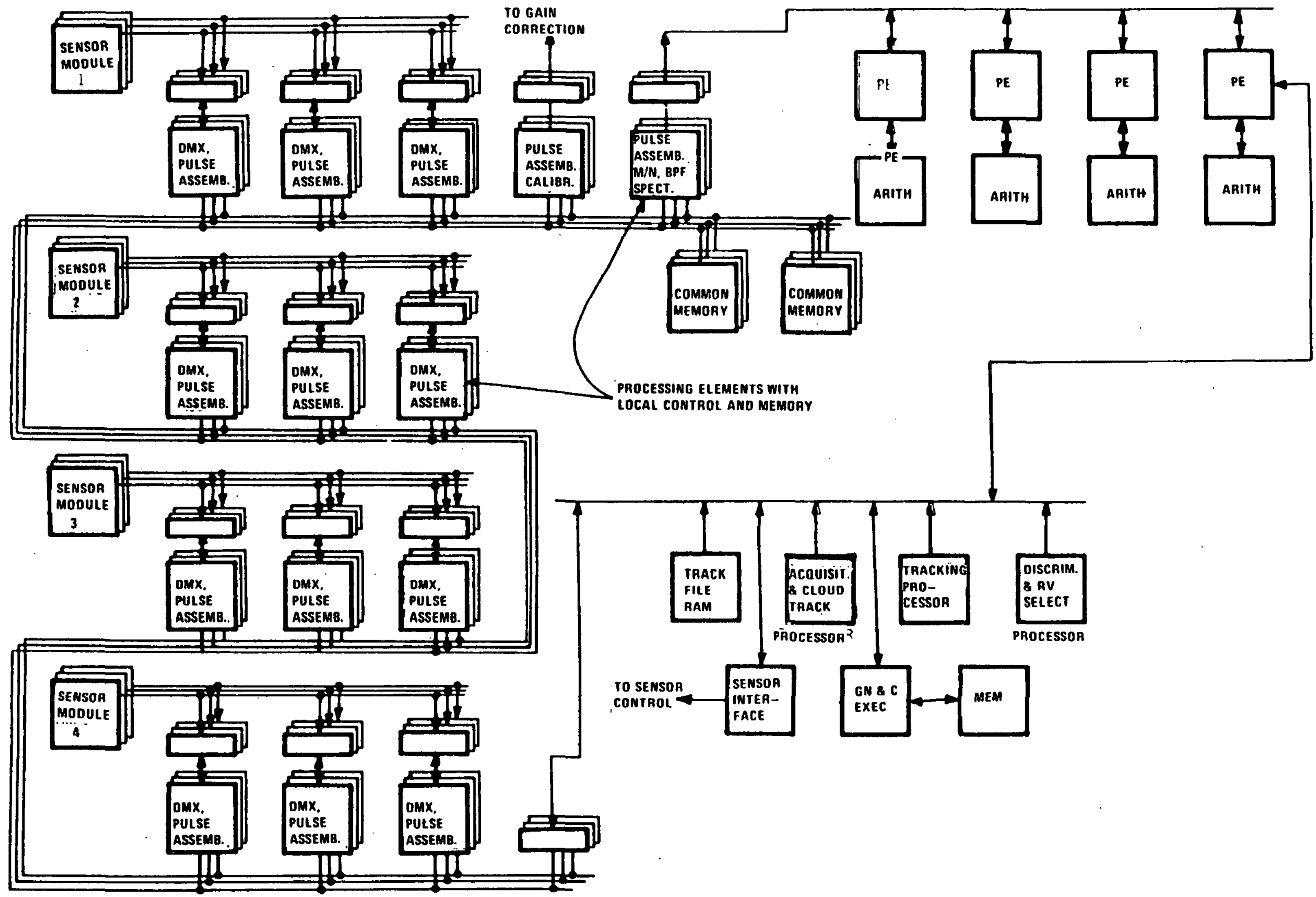
SOFTWARE ARCHITECTURE



DISTRIBUTED HARDWARE:
- NATURALLY DISCIPLINES SOFTWARE DESIGN AND IMPLEMENTATION
- MAKES STRUCTURED SOFTWARE DESIGN THE EASIEST APPROACH
- PROVIDES TIGHTLY DISCIPLINED INTERFACES
- LIMITS EFFECTS OF SOFTWARE FAULTS/BUGS/CHANGES

DATA DRIVEN SOFTWARE STRUCTURE:
- ALLOWS GRACEFUL EXPANSION/CONTRACTION (REQUIRES NO SOFTWARE CHANGES)
- PROVIDES INHERENT FAULT TOLERENCE

PRELIMINARY ARCHITECTURAL CONFIGURATION, ALTERNATIVE A



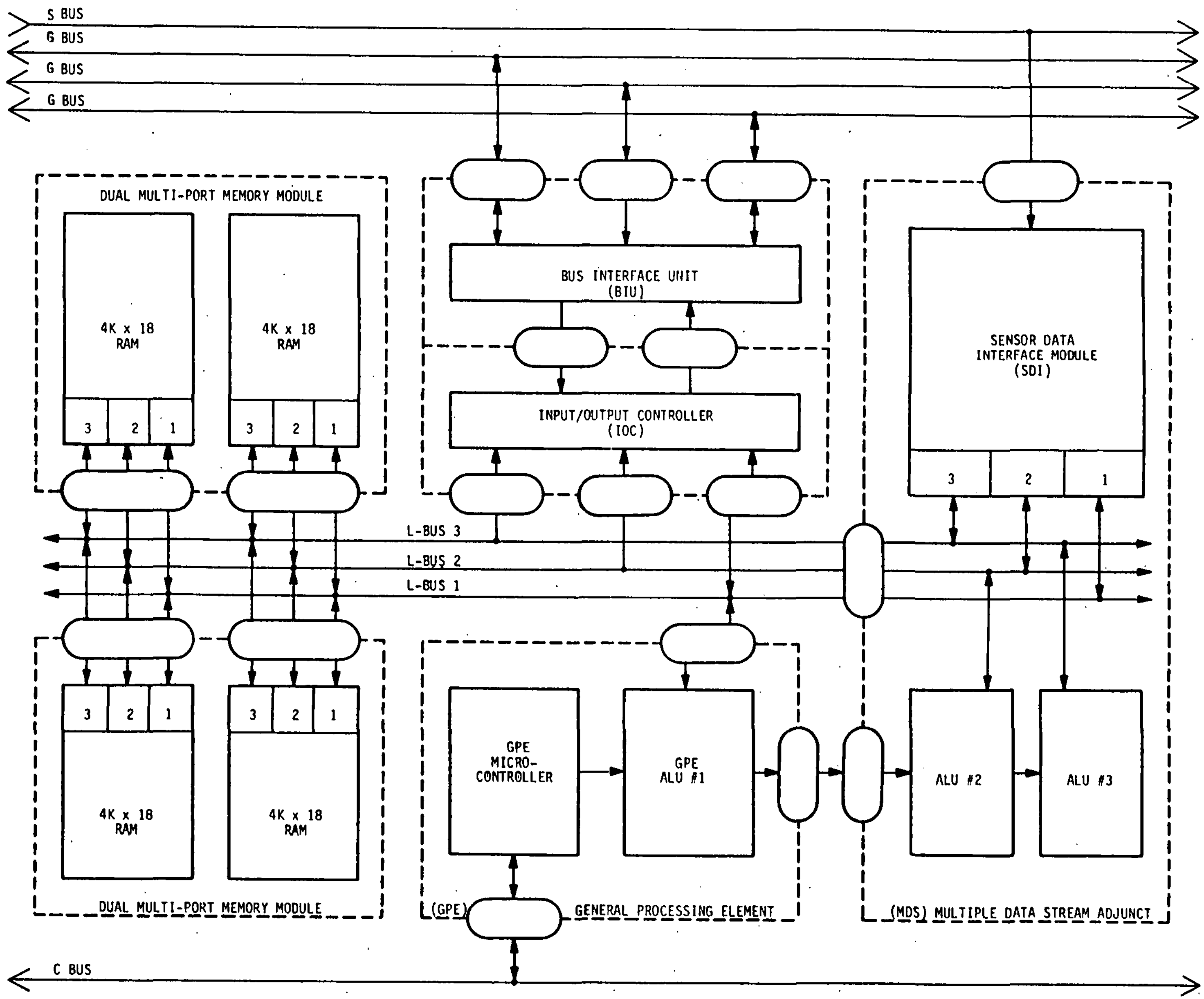
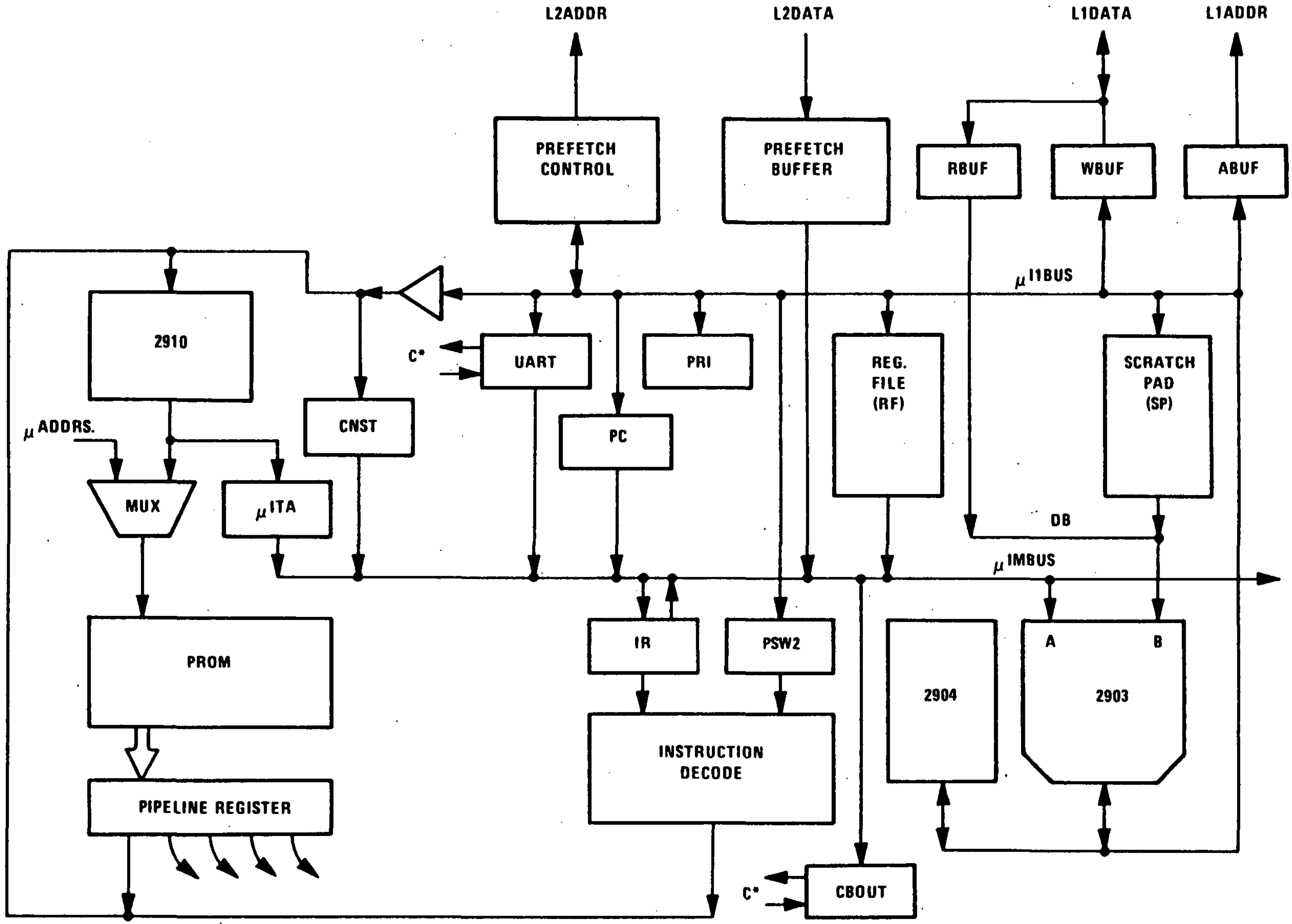


Figure 3.2. SIMD Functional Block Diagram

GPE BLOCK DIAGRAM

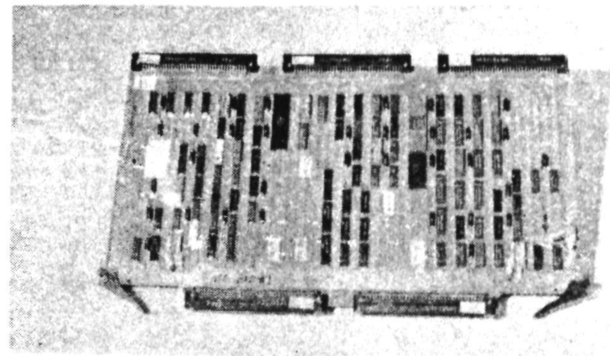


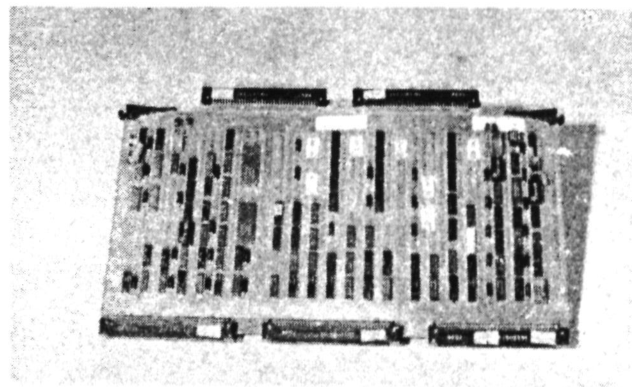
PROCESSING ELEMENT CPU

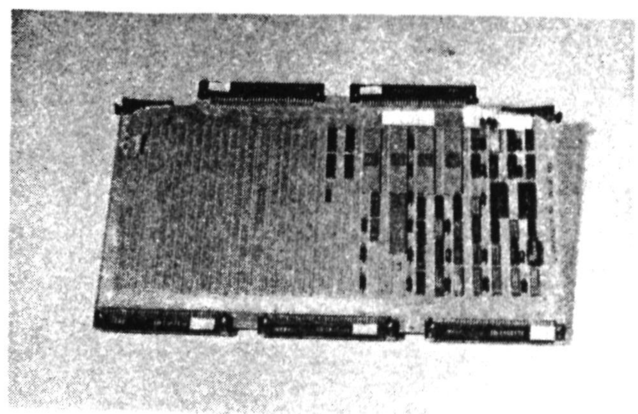
- SINGLE CPU MODULE USED THROUGHOUT SYSTEM

CHARACTERISTICS

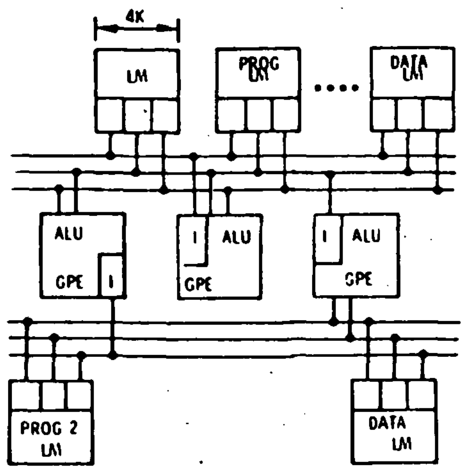
- 1 MIPS PERFORMANCE ($\sim$ 1 μs ADD)
- 16 BIT PARALLEL ORG.
- 65K WORD ADDRESS SPACE
- ASYNCHRONOUS INTERFACES
- MEMORY MAPPED I/O
- LARGE INSTRUCTION SET WITH OPERATING SYSTEMS PRIMATIVES AND FLOATING POINT
- CAPABLE OF AUGMENTATION (I.E., MORE CAPABILITY FOR PULSE MATCH, ETC.)
- 220 LOW POWER SCHOTTKY AND SCHOTTKY TTL IC's
- 96 BIT MICROINSTRUCTION WORD
- MAJOR SECTIONS: ALU, MICROCONTROLLER, CONTROL BUS INTERFACE, REAL-TIME CLOCK



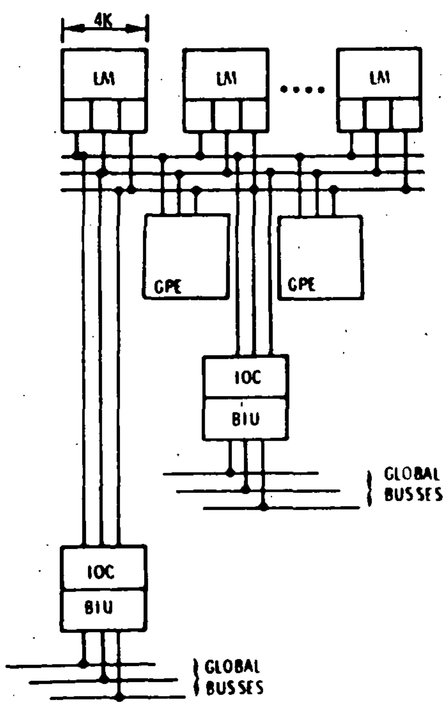




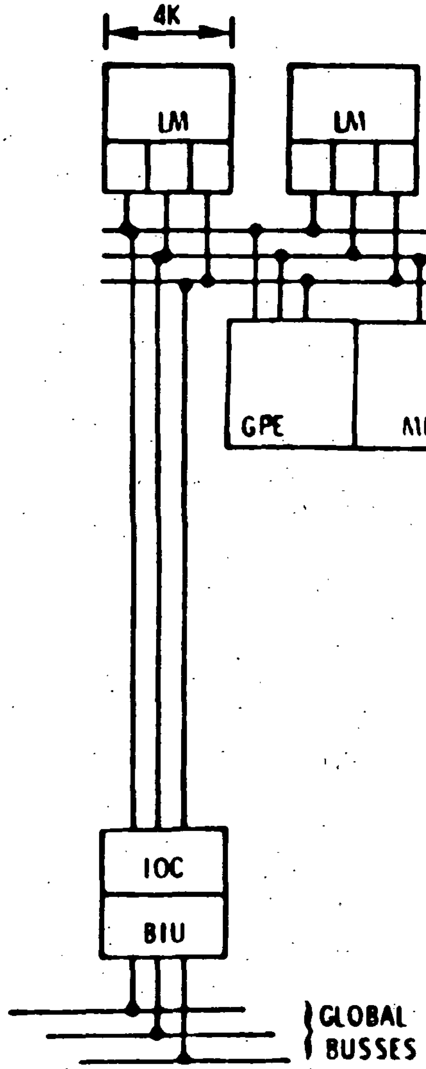
ALTERNATIVE CONFIGURATIONS OF MMBC MODULES



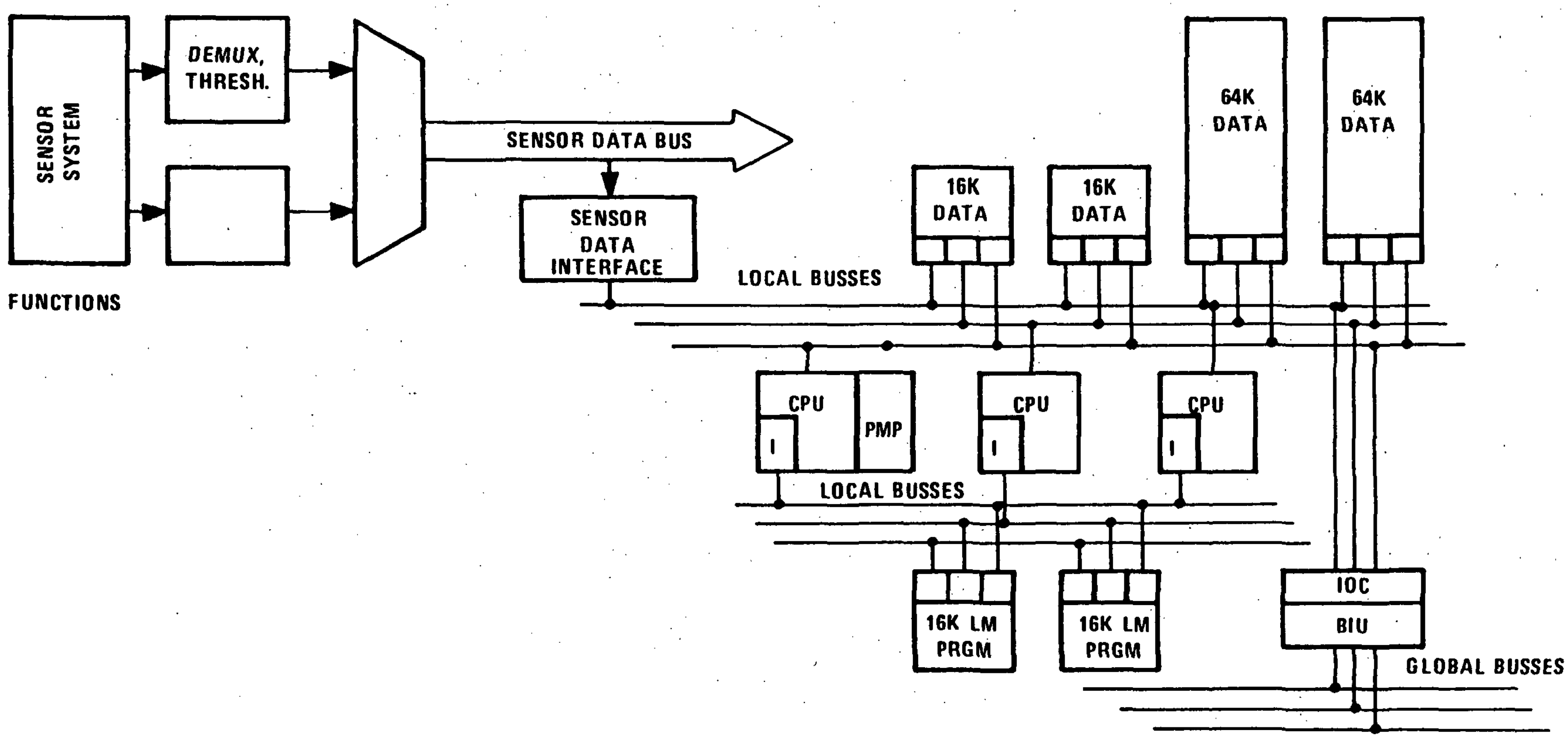
ALTERNATIVE CONFIGURATIONS OF MMBC MODULES



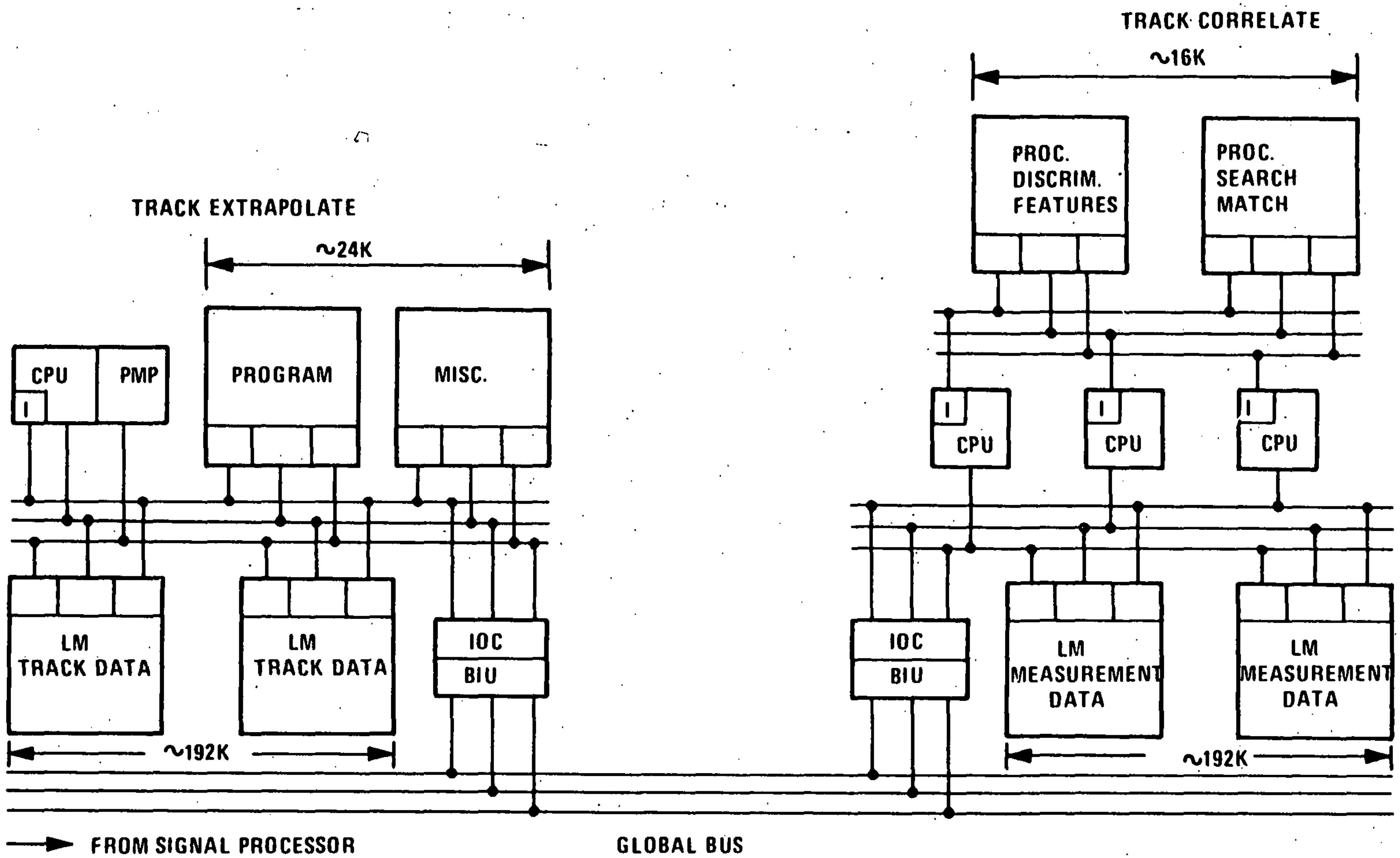
ALTERNATIVE CONFIGURATIONS OF MMBC MODULES



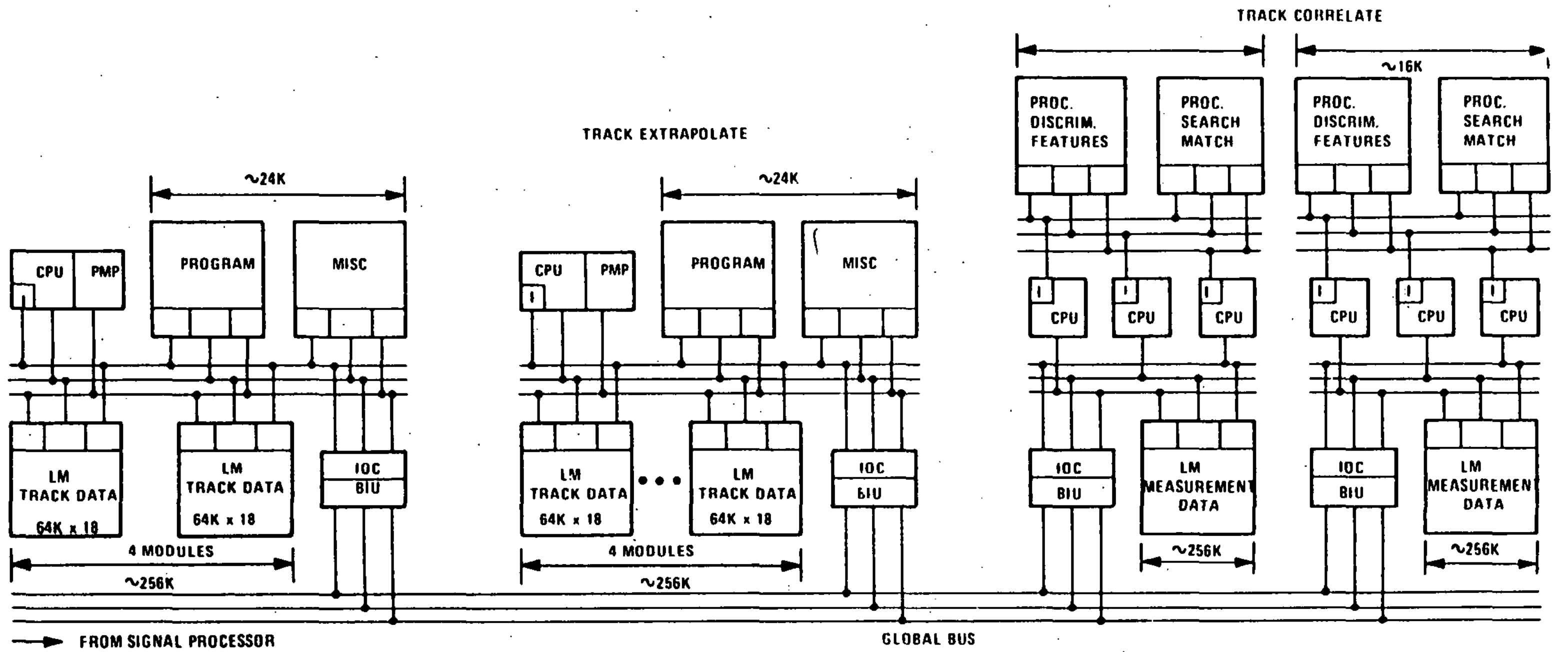
EWA PROGRAMMABLE SIGNAL PROCESSOR



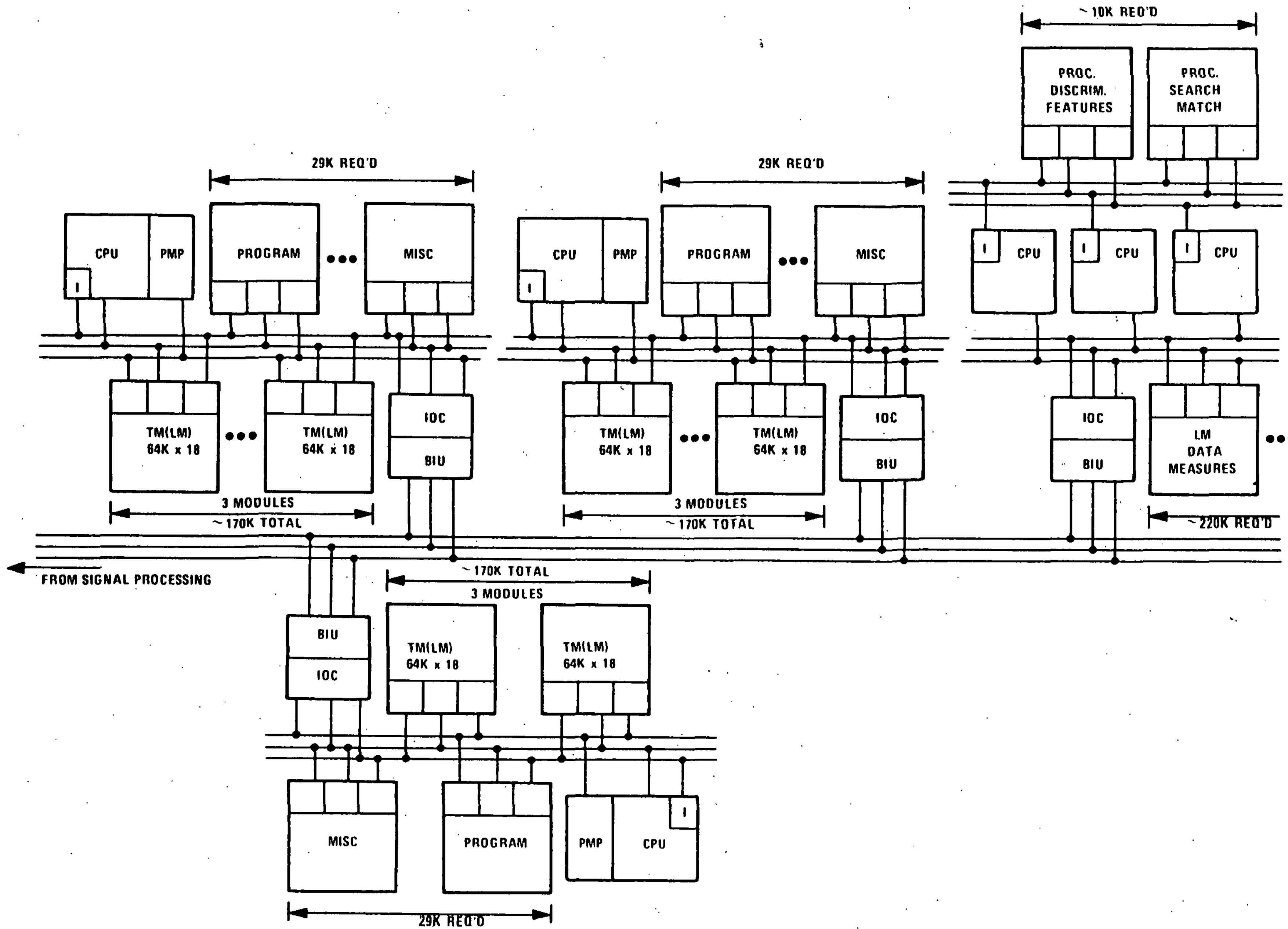
EWA DATA PROCESSING SYSTEM



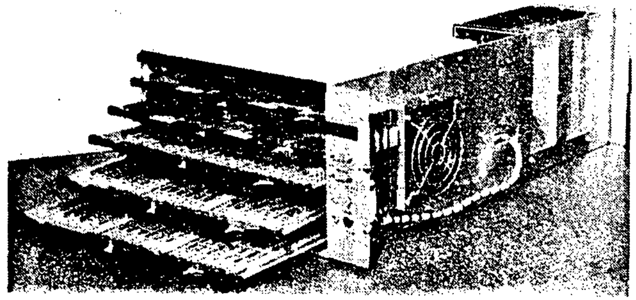
NEAR-TERM BMD DATA PROCESSING



ABMD DATA PROCESSING

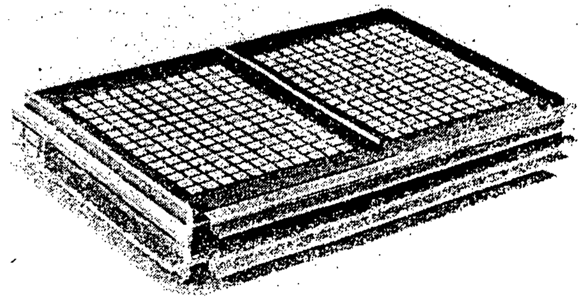


HARDWARE PACKAGING OPTIONS



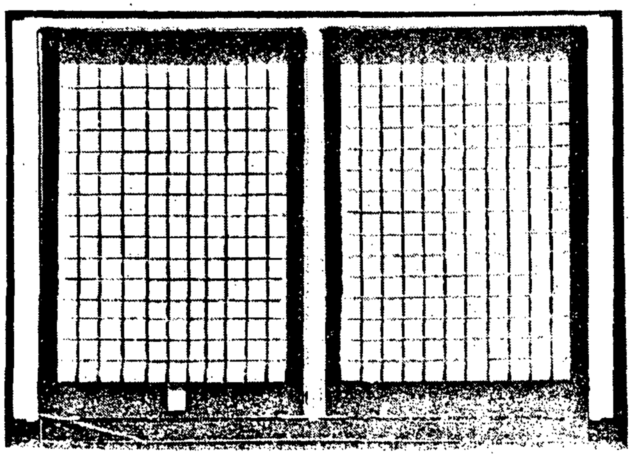
LAB PROTOTYPE IMPLEMENTATION -
CPU ON 2 15"x15" BOARDS

OPTION I



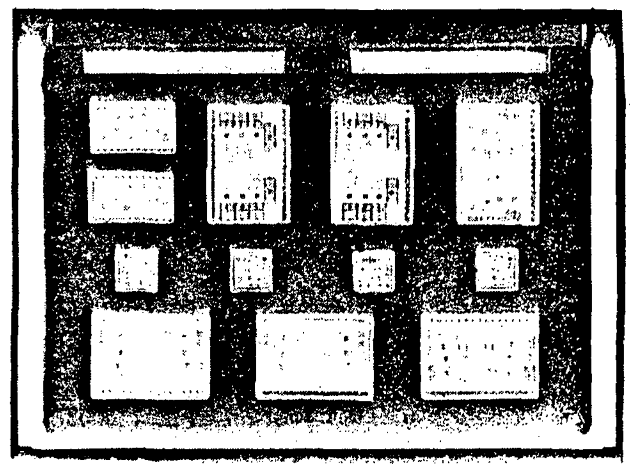
CPU ON DOUBLE MODULE -
FLAT PAKS AND CHIP CARRIERS

OPTION II



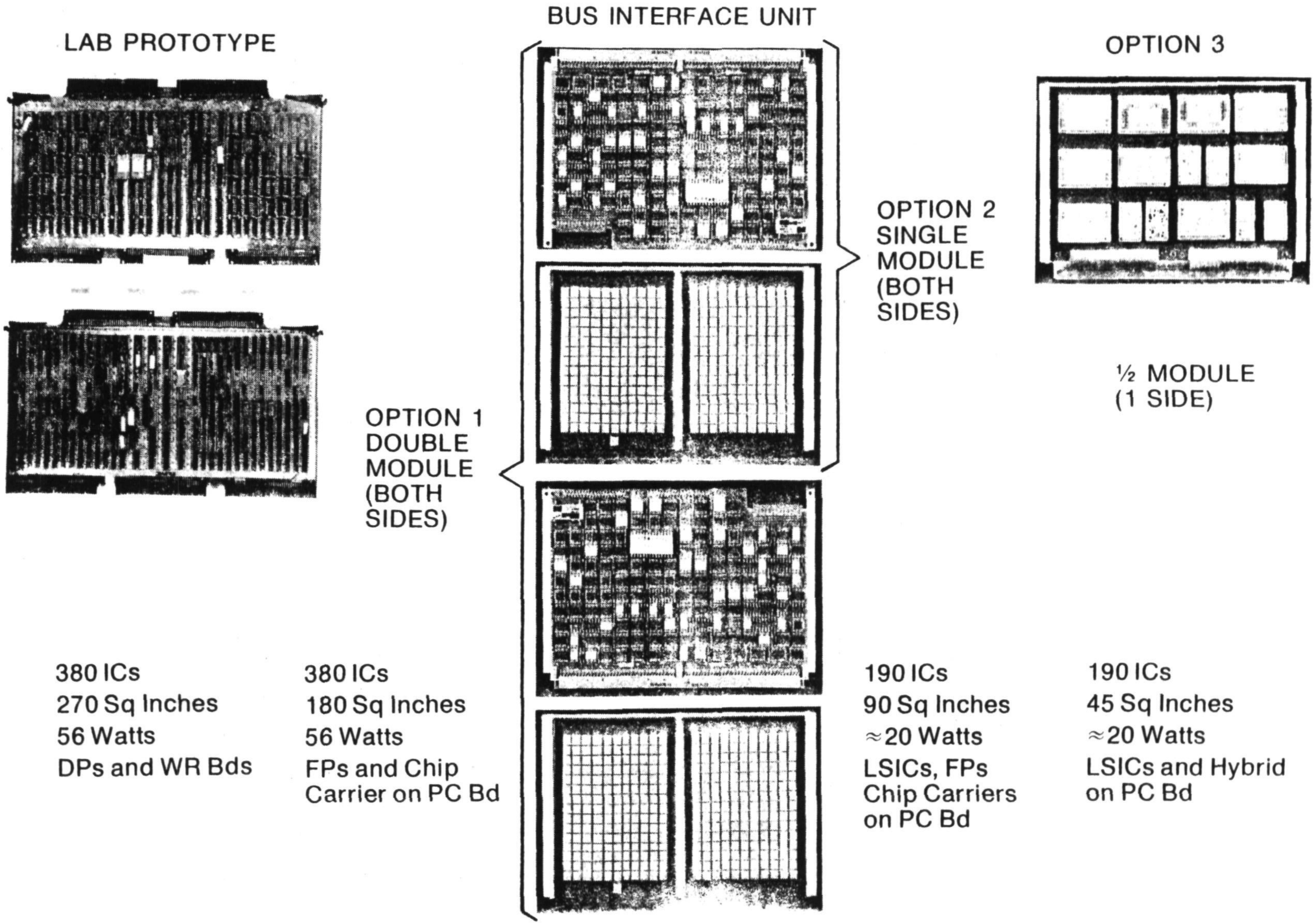
CPU ON SINGLE MODULE -
LSICs, FLAT PAKS AND
CHIP CARRIERS

OPTION III

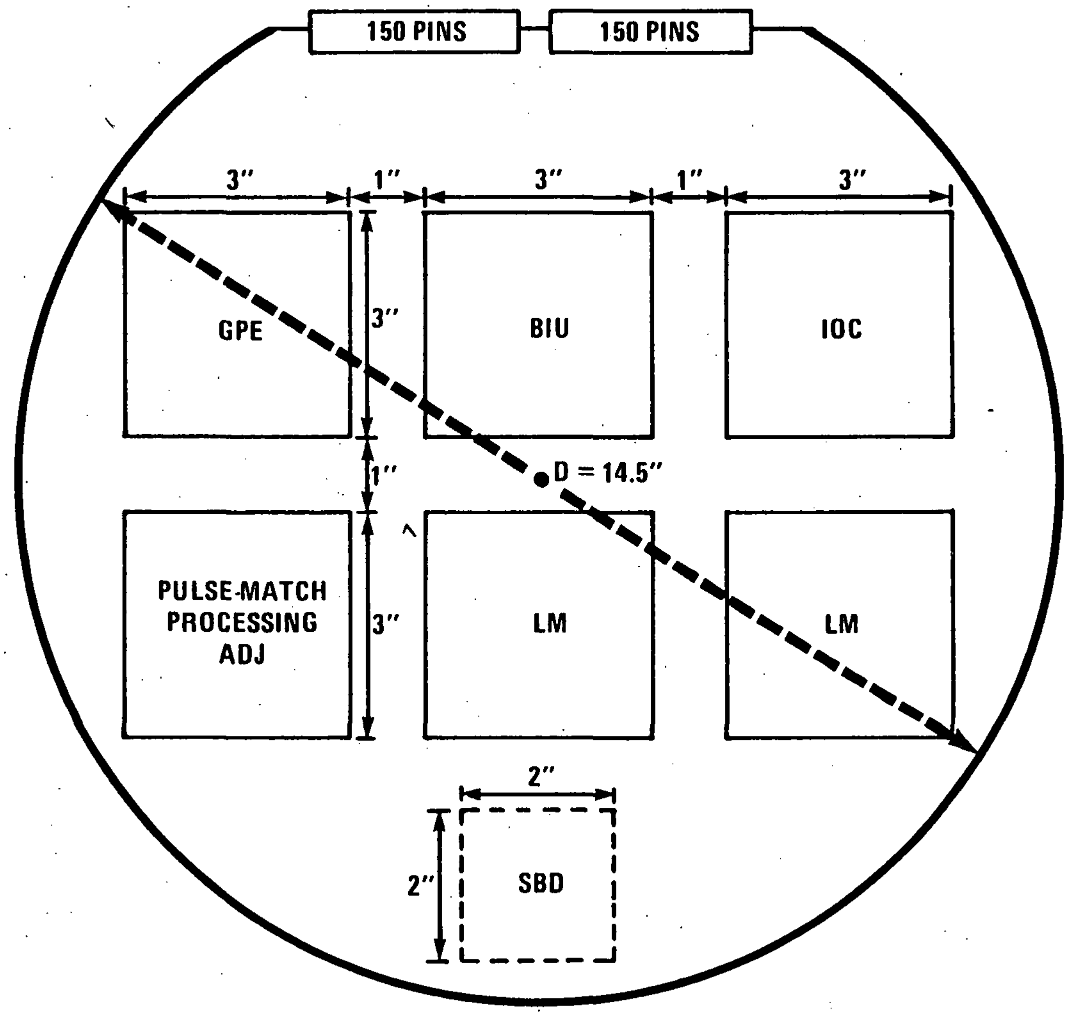


CPU ON HALF MODULE -
HYBRIDS AND LSICs

EXAMPLE OF SIZE REDUCTION FOR PACKAGING OPTIONS



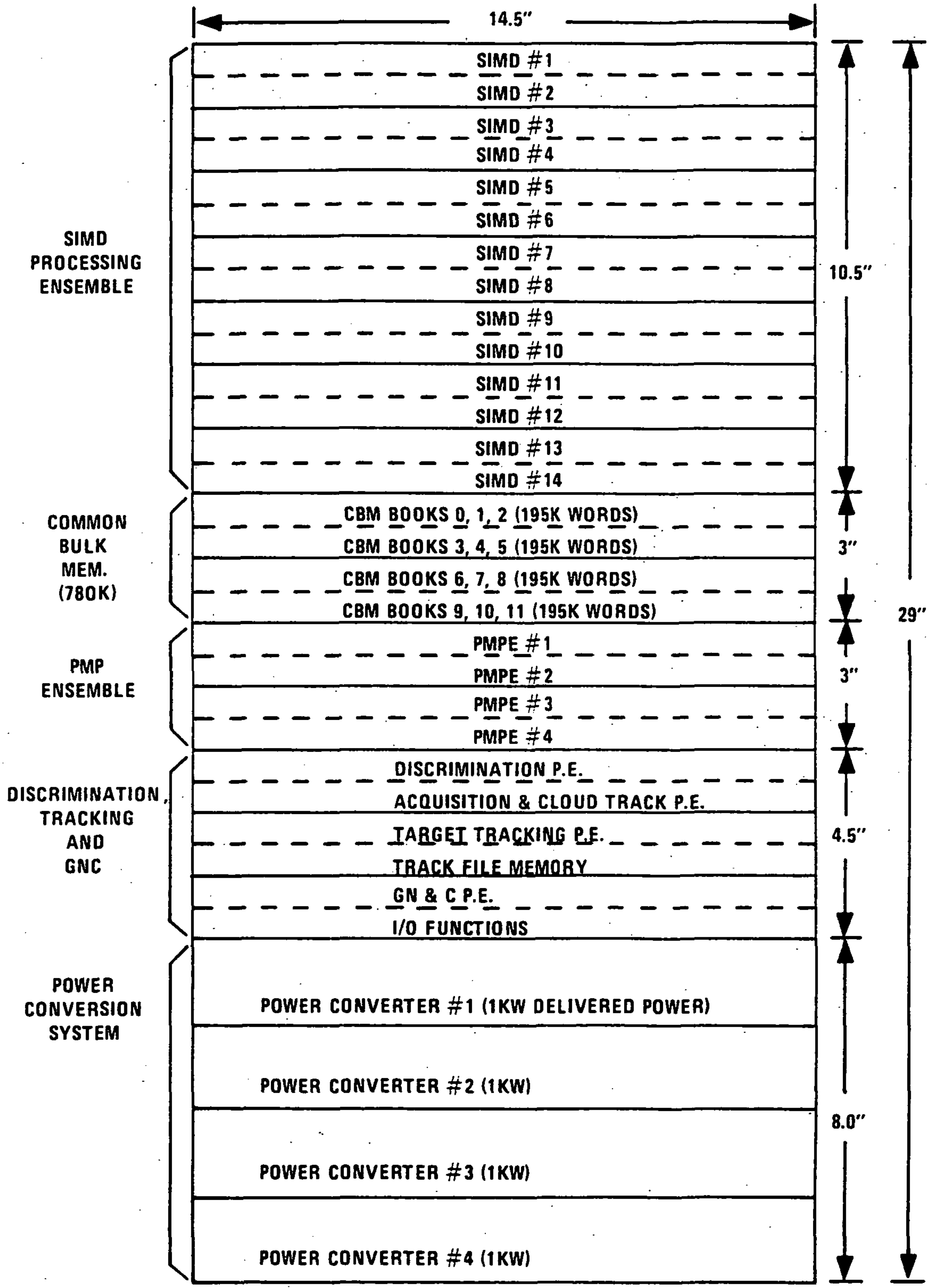
PACKAGING EXAMPLE
(PULSE-MATCH PROCESSOR MODULE)



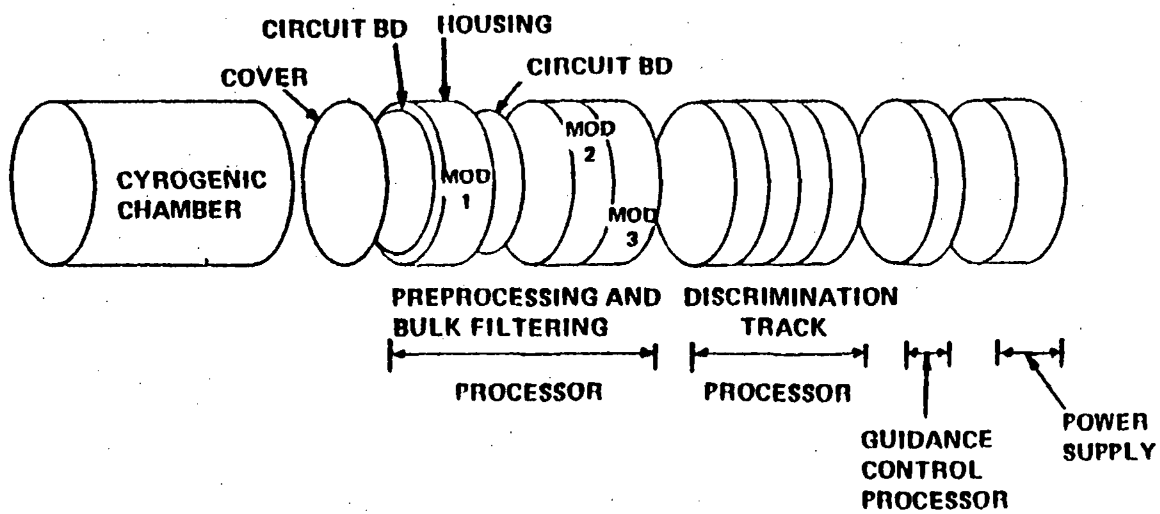
CHARACTERISTICS

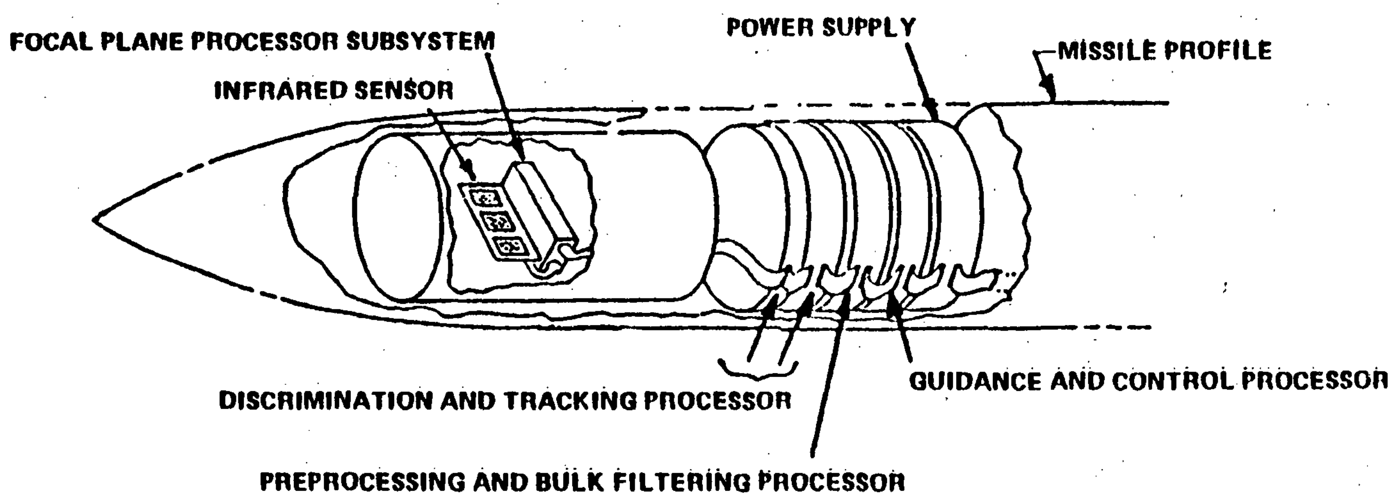
- 200 WATTS
- 14.5" DIAMETER
- TWO 150-PIN I/O CONN.
- OPTIONAL 2" X 2" (SBD) (SENSOR BUS DRIVER)
- 165 in^2
- 3/4" CENTERS BOARD SPACING

EXAMPLE OF HYBRID MMBC SYSTEM



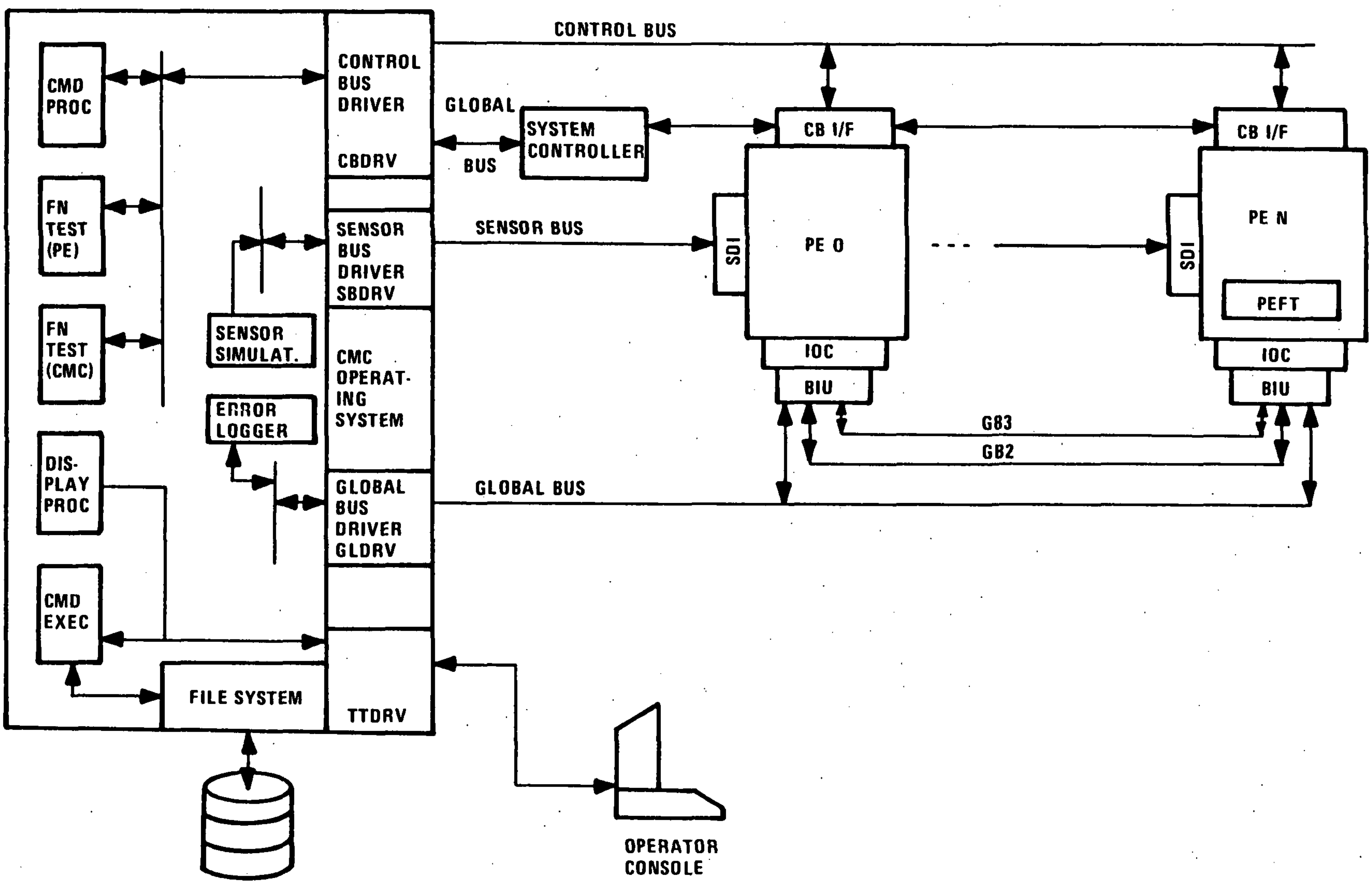
MODULAR MISSILE BORNE COMPUTERS





- ONBOARD BUDGETS FOR LDS PROBE APPEAR FEASIBLE

TEST BED

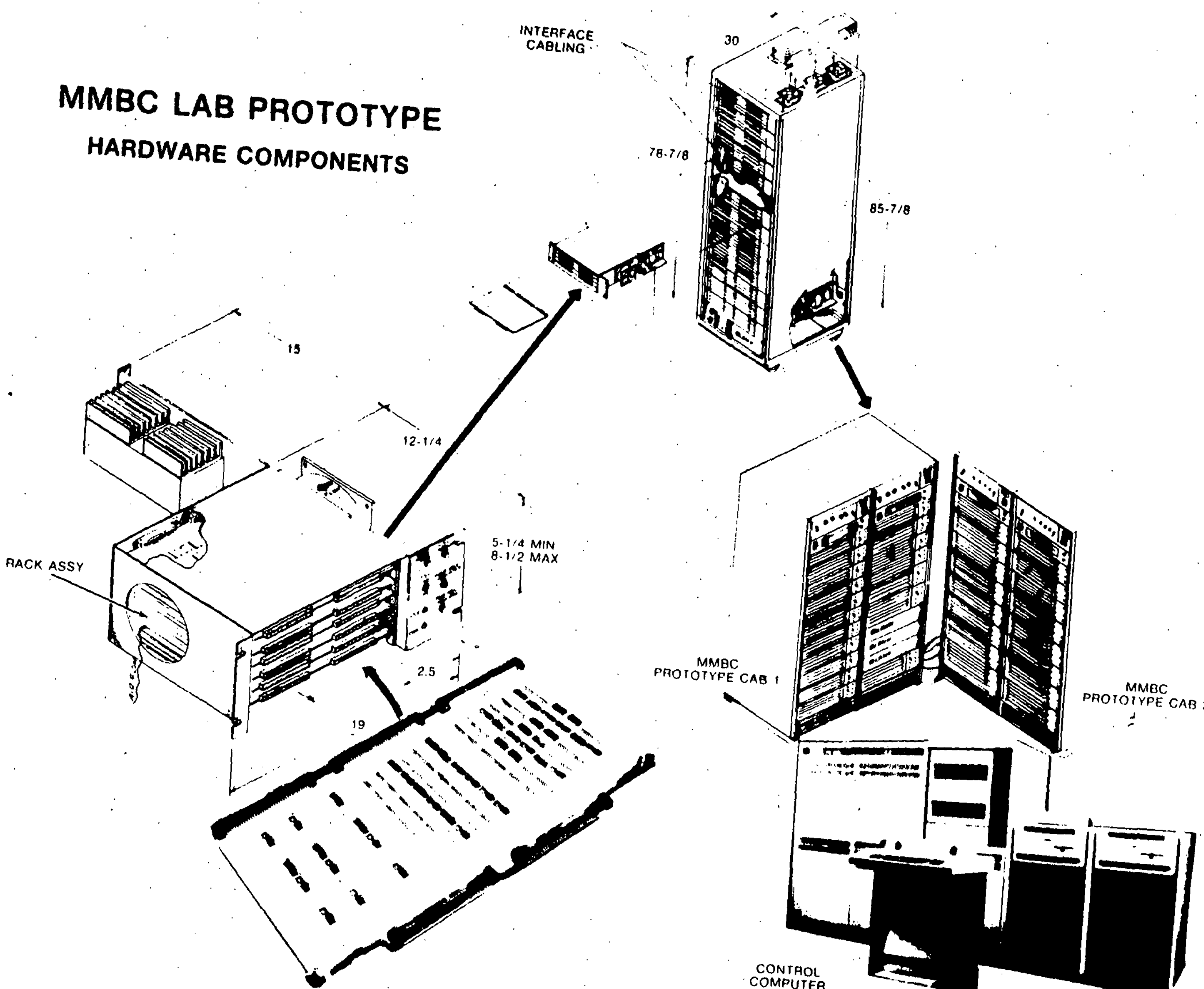


CONTROL BUS
CMD PROC
FN TEST (PE)
FN TEST (CMC)
DIS-PLAY PROC
CMD EXEC
SENSOR SIMULAT.
ERROR LOGGER
FILE SYSTEM
CONTROL BUS DRIVER CBDRV
SENSOR BUS DRIVER SBDRV
CMC OPERAT-ING SYSTEM
GLOBAL BUS DRIVER GLDRV
TTDRV
GLOBAL BUS
SYSTEM CONTROLLER
SENSOR BUS
GLOBAL BUS
CB I/F
PE 0
SDI
IOC
BIU
CB I/F
PE N
SDI
PEFT
IOC
BIU
GB3
GB2
OPERATOR CONSOLE

DIFFERENCES BETWEEN CURRENT SYSTEM & MMBC

CURRENT	MMBC
• SINGLE (OR SMALL NO.) OF PE'S	• MANY PE'S
• THRUPUT FIXED, ~10-20 MIPS MAX., 1-2 MIPS FLYABLE NOT EXPANDABLE	• EXPANDABLE, THRUPUT VARIABLE FROM ~1 TO 100 + MIPS; MAY BE TUNED TO APPLICATION REQUIREMENTS (FLYABLE)
• THRUPUT INVARIANT WITH APPLICATION	• THRUPUT DEPENDENT ON SW, SW STRUCTURE
• SOFTWARE STRUCTURE/ COMPLEXITY UNCONTROLLED	• STRUCTURED APPROACH EASIEST SW MODULARITY INHERENT, COMPLEXITY CONTROLLED; REQUIRES CAREFUL PARTITIONING
• GENERALLY SUBJECT TO SINGLE POINT FAILURES	• EASILY AVOIDS SINGLE POINT FAILURES; GRACEFULLY DEGRADES WITH FAULTS
• OVERHEAD FUNCTIONS GENERALLY IN SW	• HARDWARE IMPLEMENTS MOST OVERHEAD FUNCTIONS (ESPECIALLY THOSE DUE TO MULTI COMPUTER CONFIGURATION

MMBC LAB PROTOTYPE
HARDWARE COMPONENTS



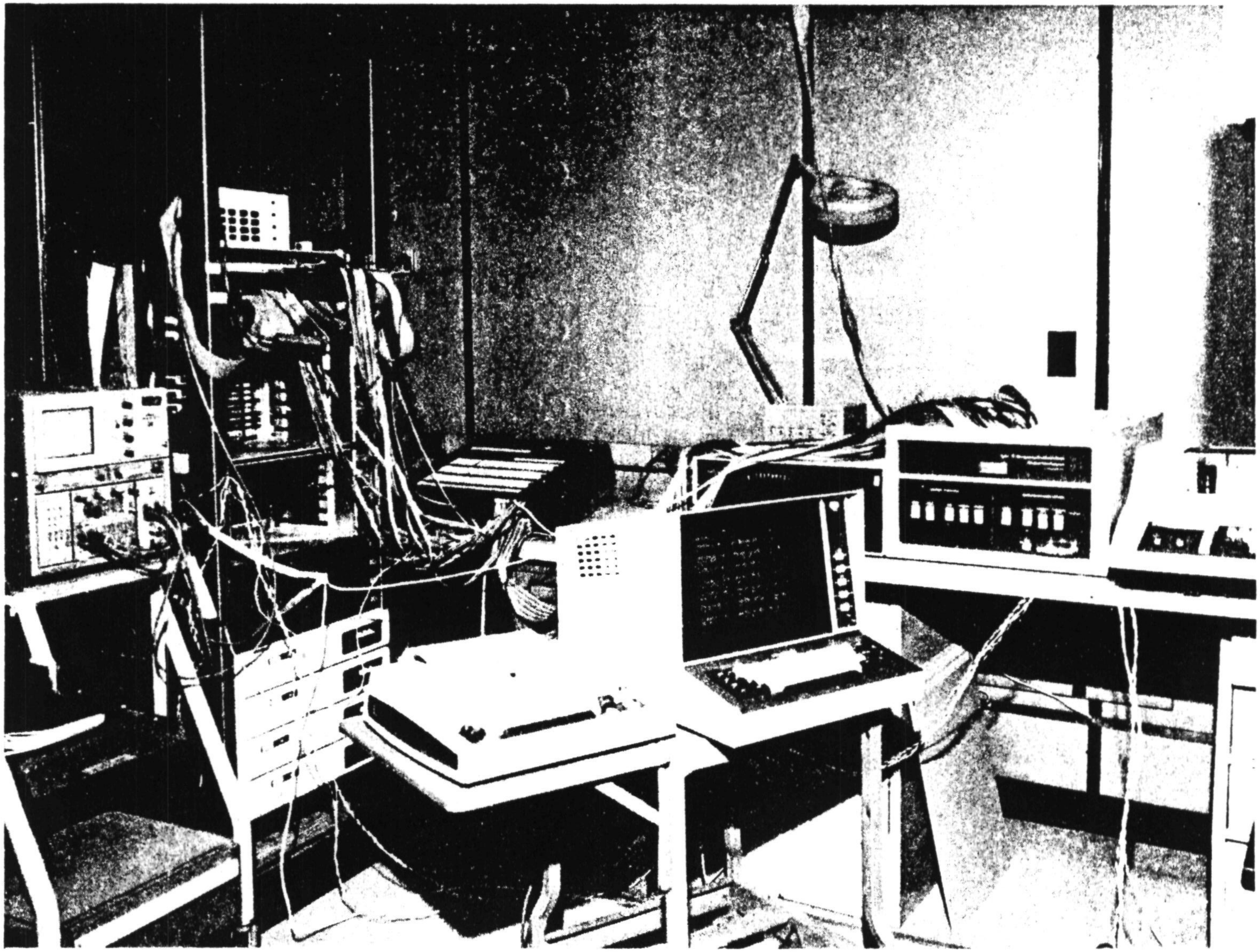


Figure 16. CPU Bus Display Box