MICROCOMPUTER ARRAY PROCESSOR SYSTEM

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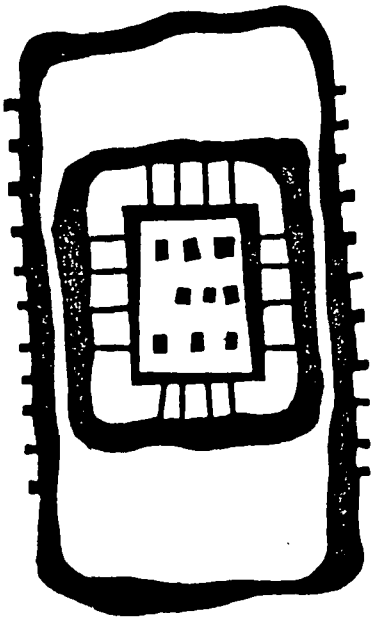
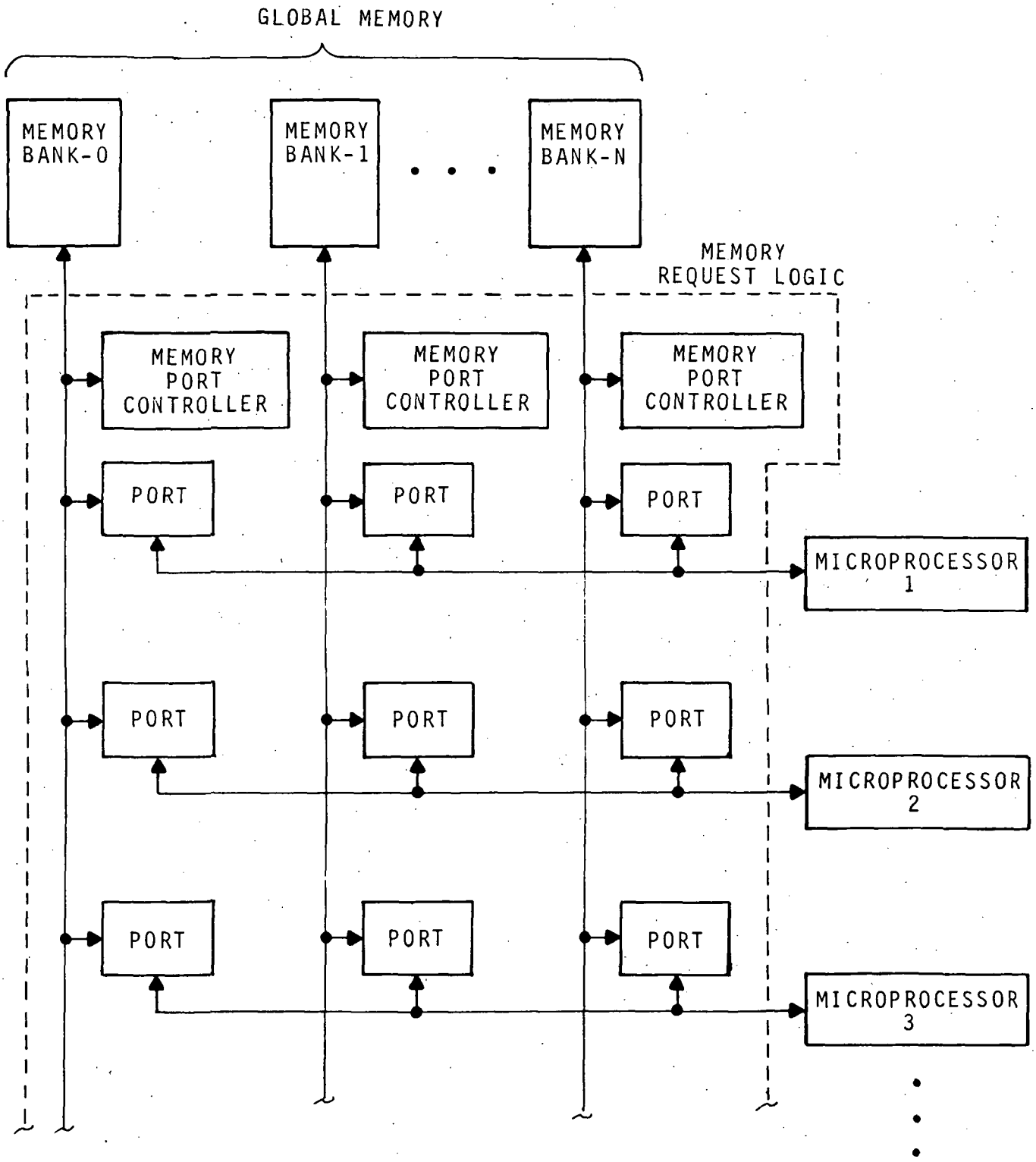
The Microcomputer Array Processor System (MAPS) is a programmable multiprocessor computer system designed for Electronic Warfare applications for the Air Force Avionics Laboratory (AFAL). The system architecture retains many of the classic multiprocessor design concepts including a master-slave relationship among its microprocessors under the control of a single operating system in a tightly coupled structure. Each processor is a 32-bit programmable computer with its own dedicated memory and a capability to execute approximately 4 million instructions a second. In addition to the dedicated memory, each processor can communicate with numerous banks of common memory (referred to as global memory). The various global memory modules and their communication structure serve to tie the individual processors together in a symmetrical multiprocessor computer architecture. The multiprocessor system is modular and can contain as few as 2 and as many as 8 processors coupled with from 1 to 16 banks of global memory and executes 32 million instructions per second. Expansions beyond these limits are possible if every processor does not have to have access to every global memory module. Currently, a 4 processor system (with 3 banks of global memory) is installed at Wright Patterson Air Force Base for use by AFAL. This system will be expanded to 6 processors during 1980. This multiprocessor subsystem is approximately 1.6 cubic feet and consumes under 400 watts of power.

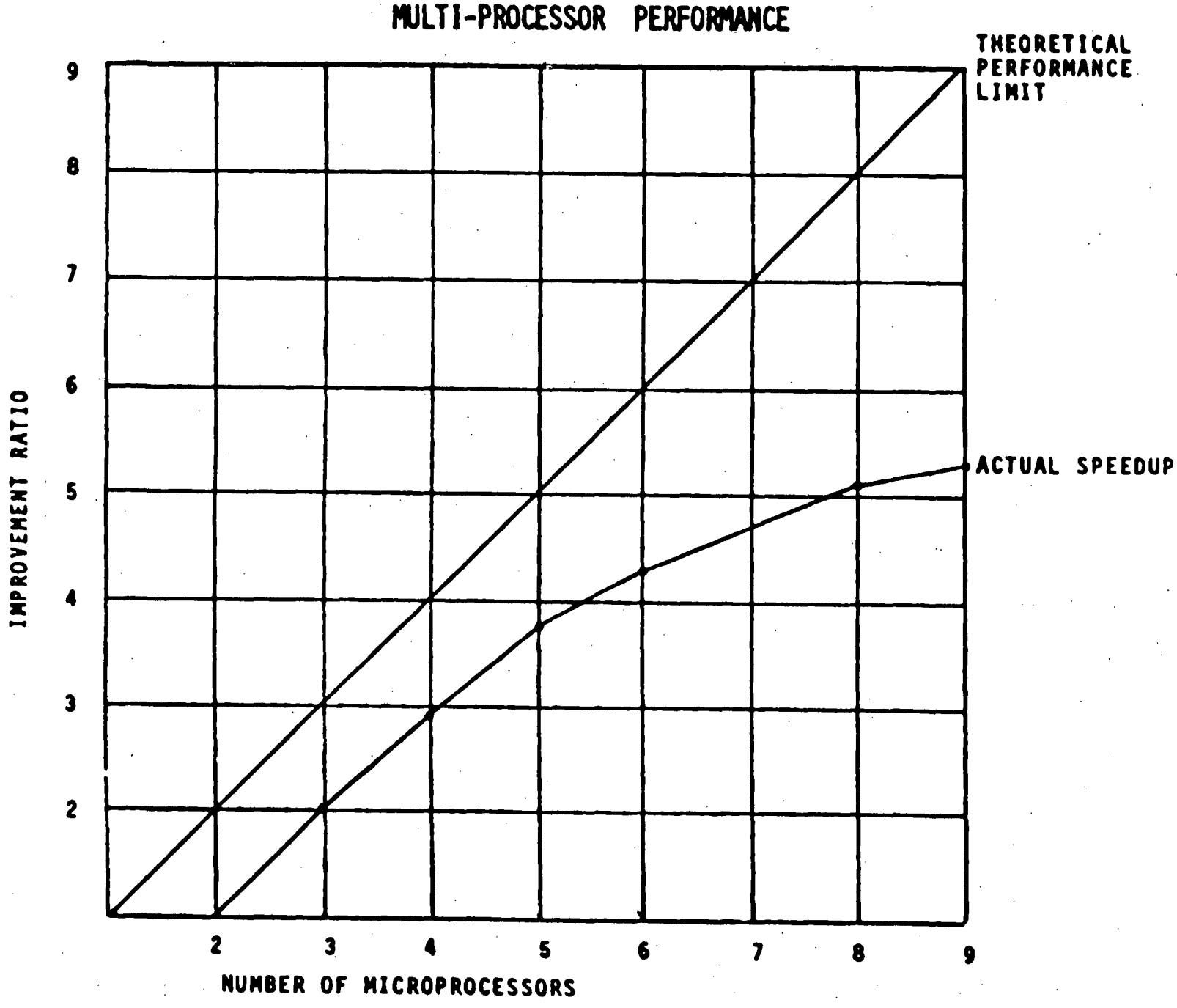


MICROCOMPUTER ARRAY PROCESSOR

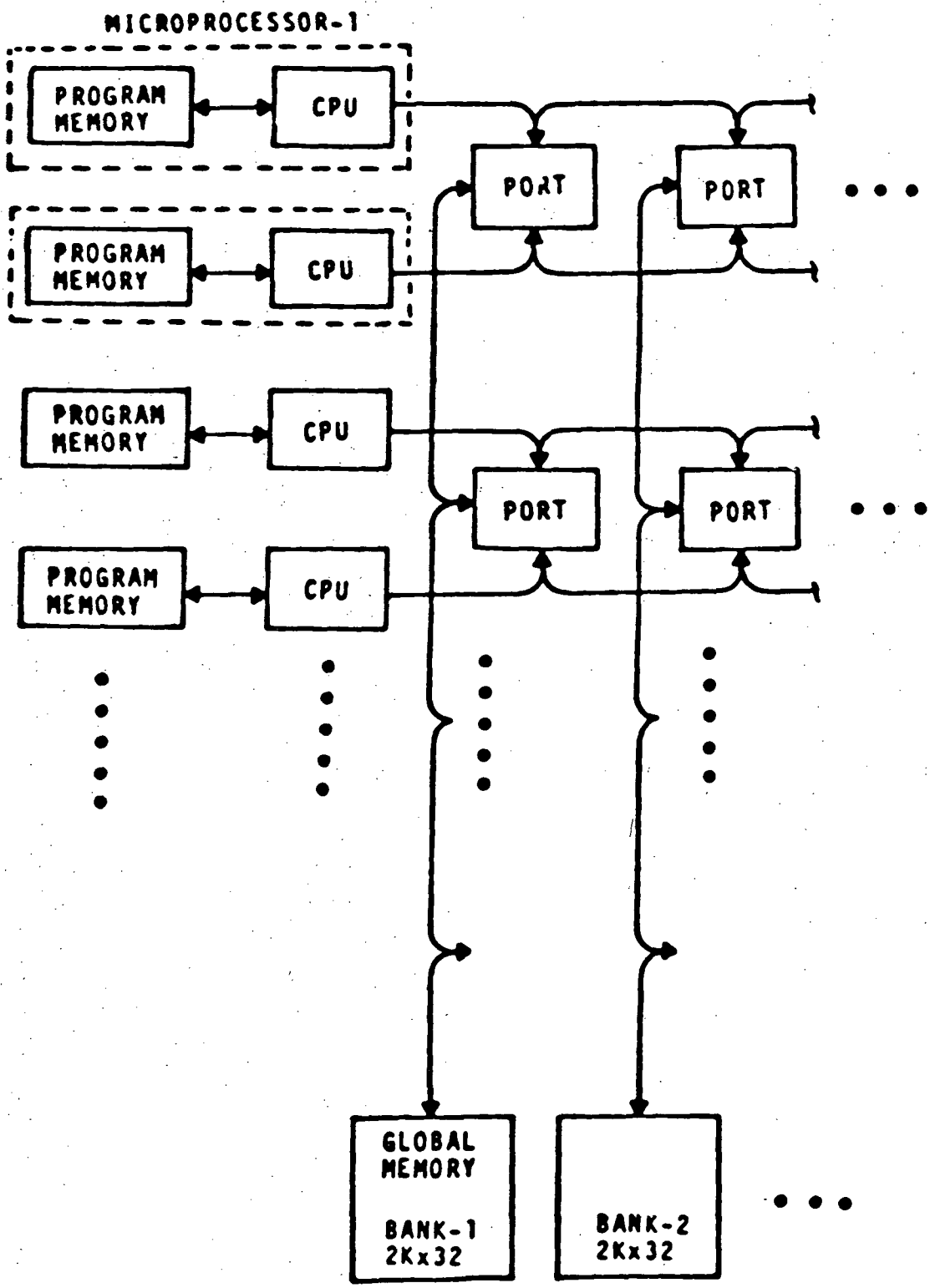
MULTIPROCESSOR SYSTEM ATTRIBUTES

- TASK
- SYMMETRY
- COMMUNICATION
- PROCESSOR INTELLIGENCE

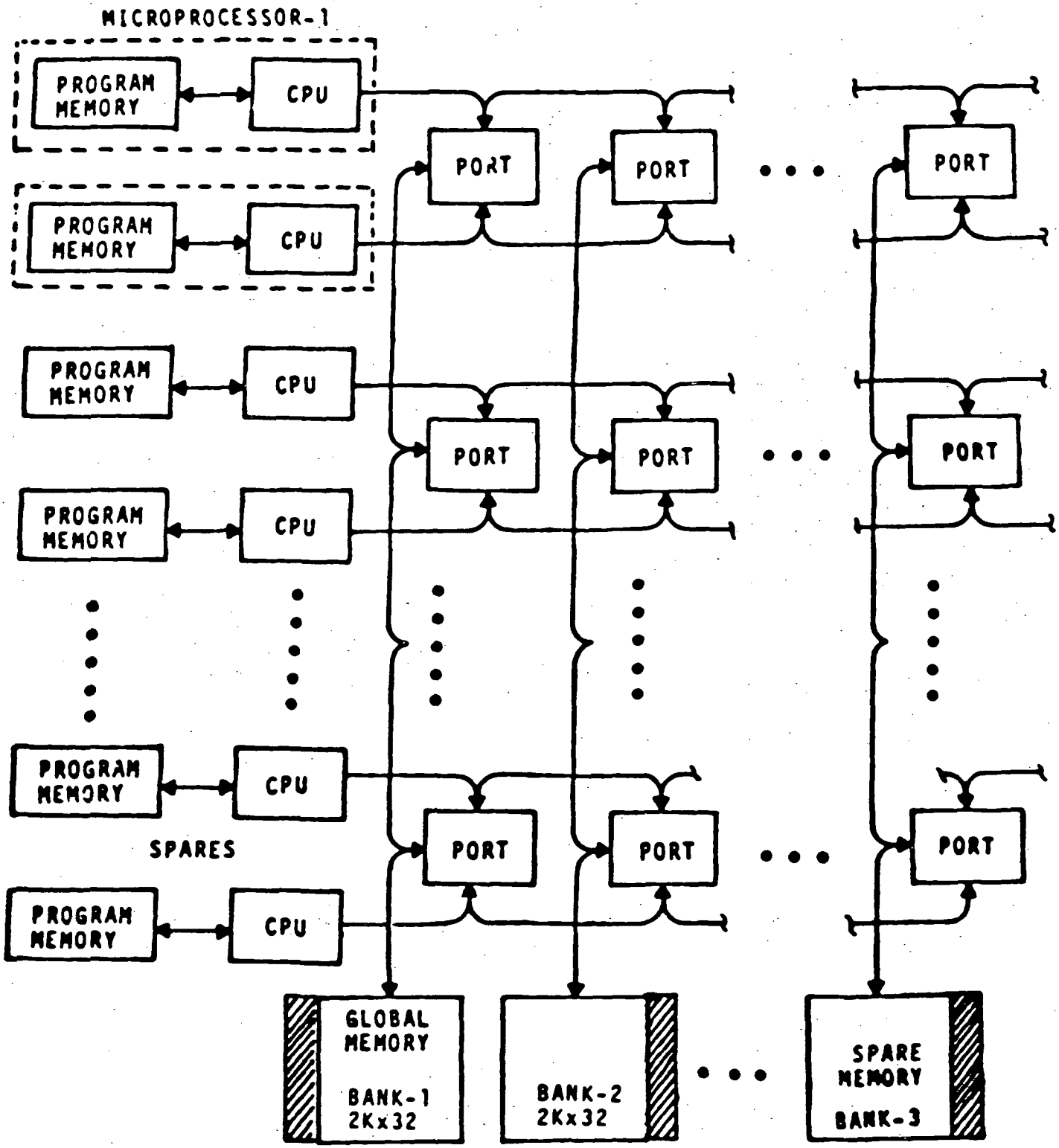

GLOBAL MEMORY
MEMORY BANK-0
MEMORY BANK-1
MEMORY BANK-N
MEMORY REQUEST LOGIC
MEMORY PORT CONTROLLER
MEMORY PORT CONTROLLER
MEMORY PORT CONTROLLER
PORT
PORT
PORT
PORT
PORT
PORT
PORT
PORT
PORT
MICROPROCESSOR 1
MICROPROCESSOR 2
MICROPROCESSOR 3


MULTI-PROCESSOR PERFORMANCE
THEORETICAL PERFORMANCE LIMIT
ACTUAL SPEEDUP
IMPROVEMENT RATIO
NUMBER OF MICROPROCESSORS
2
3
4
5
6
7
8
9

FAULT TOLERANT MAP ARCHITECTURE

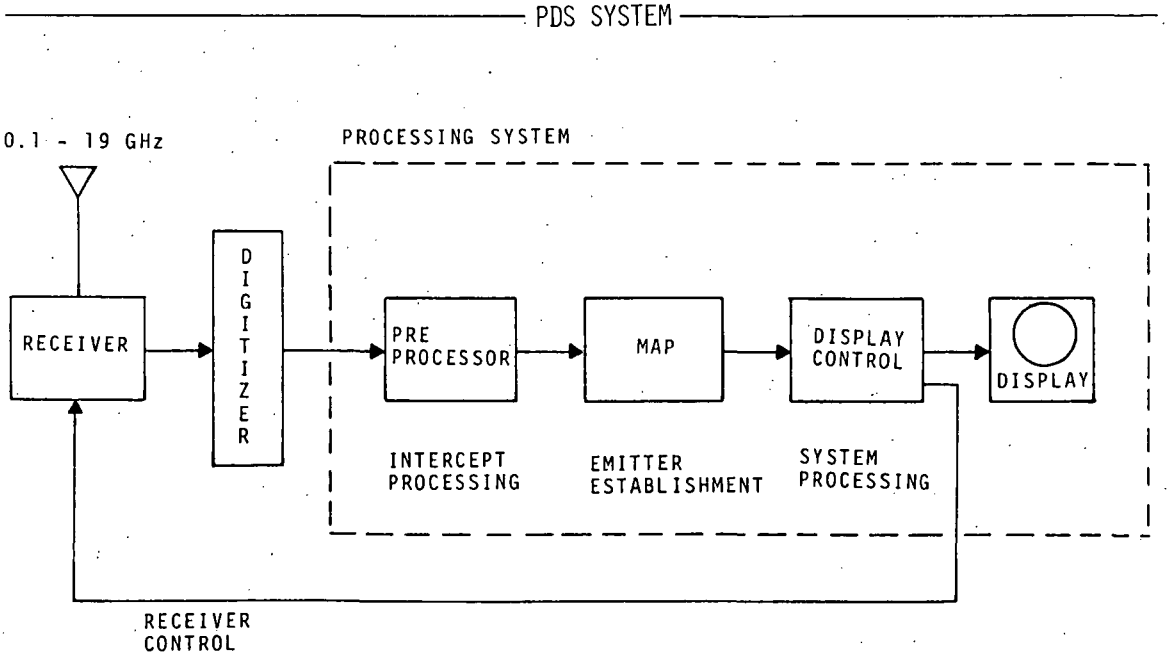


FAULT TOLERANT MAP ARCHITECTURE

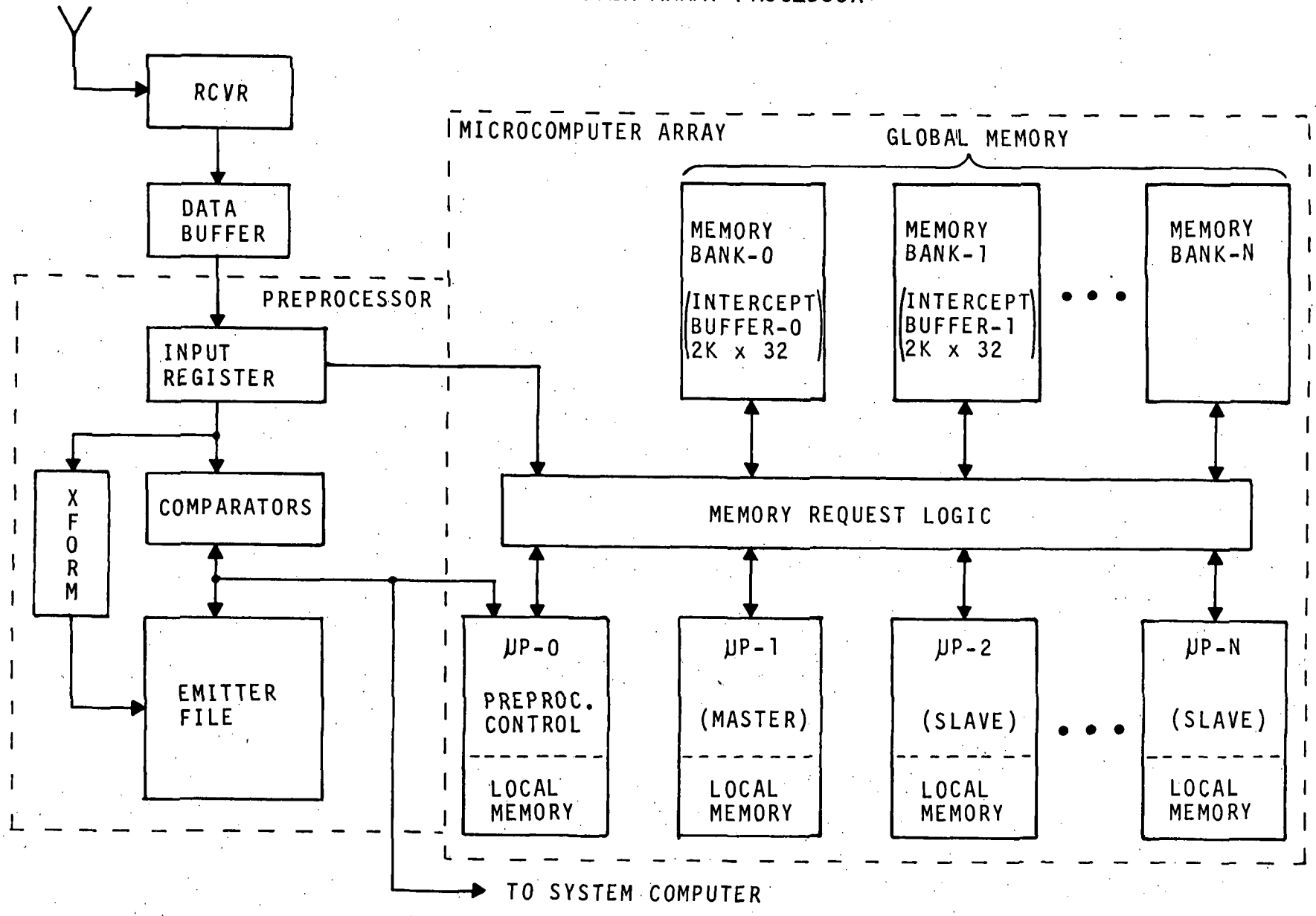


MAP PROCESSING FUNCTIONS

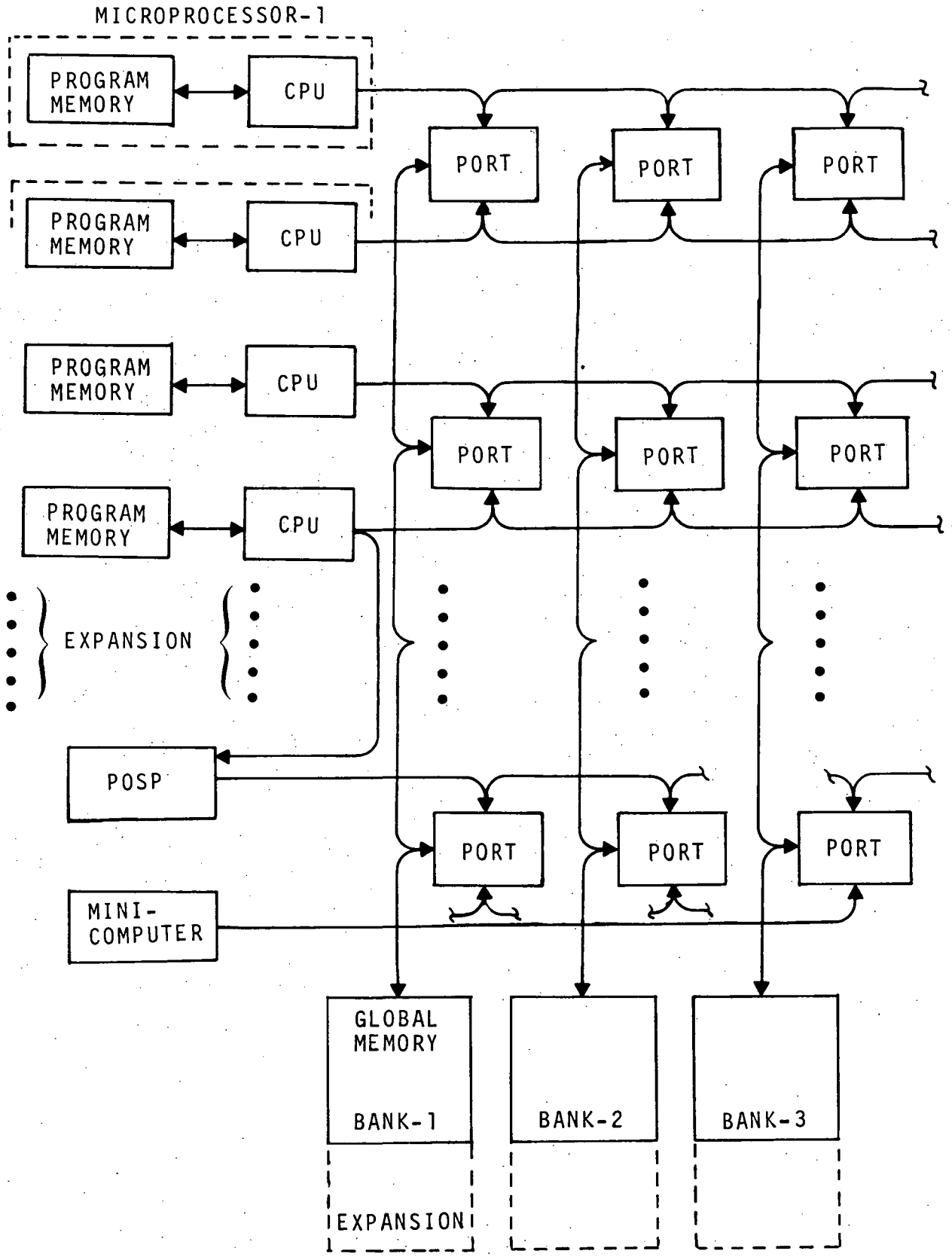
- ESTABLISHES FILE OF ACTIVE EMITTERS
  - . DETERMINES PRI
  - . REPORTS PRESENCE OF NEW EMITTERS.
- TRACKS ESTABLISHED EMITTERS
  - . TRACKS IN TIME AND ANGLE
- DELETES INACTIVE EMITTERS
- CAPABILITY FOR
  - . SCAN RATE DETERMINATION
  - . EMITTER TYPE IDENTIFICATION
  - . RECEIVER CONTROL
  - . POWER MANAGEMENT



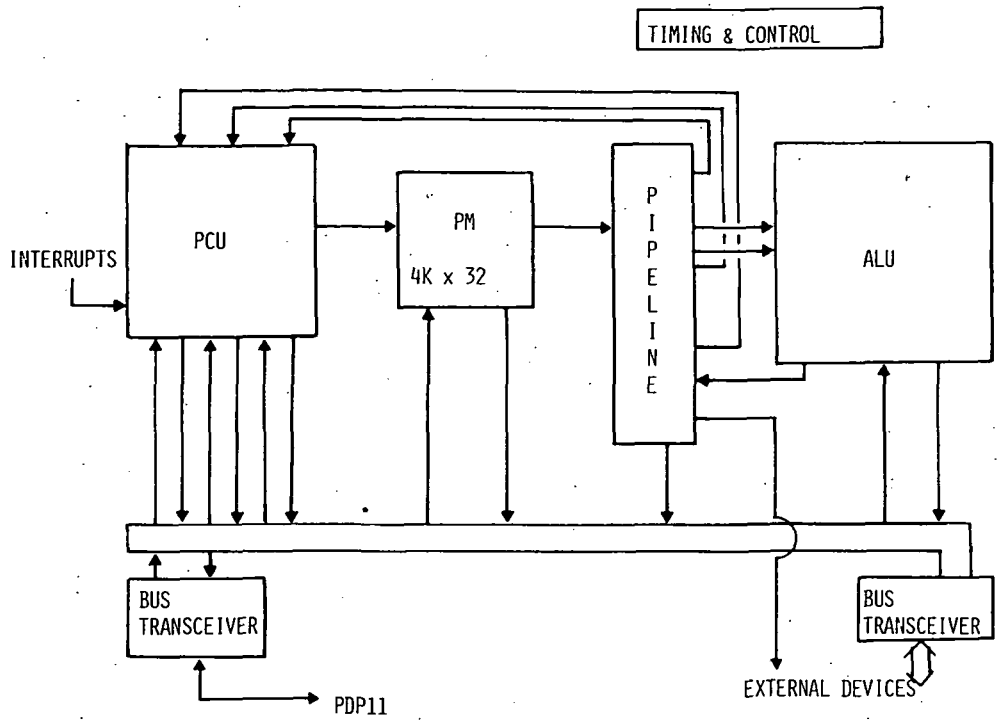
MICROCOMPUTER ARRAY PROCESSOR



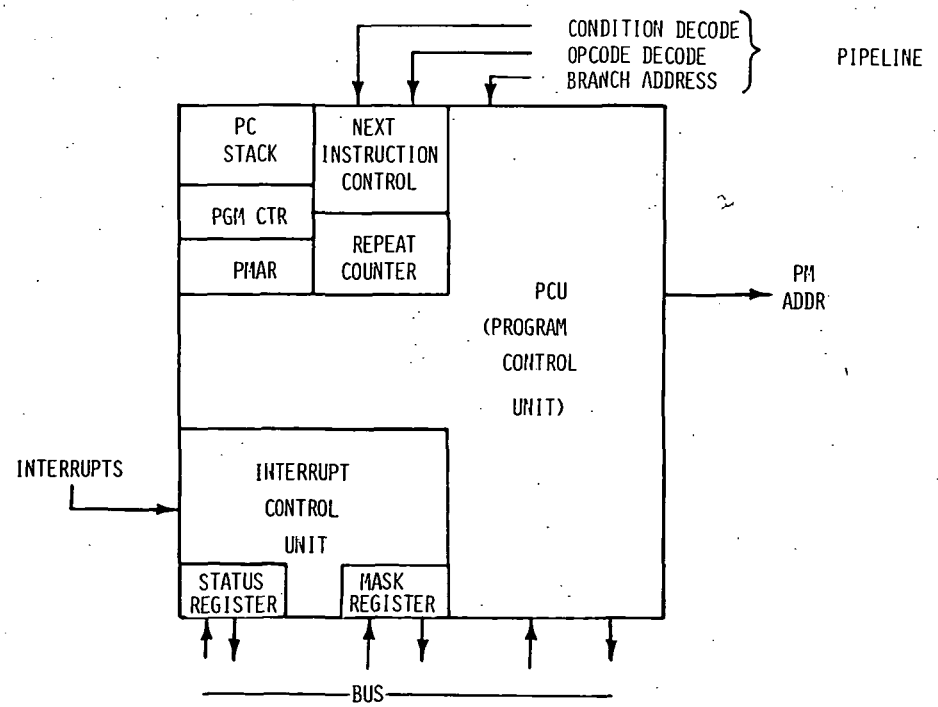
MAP ARCHITECTURE



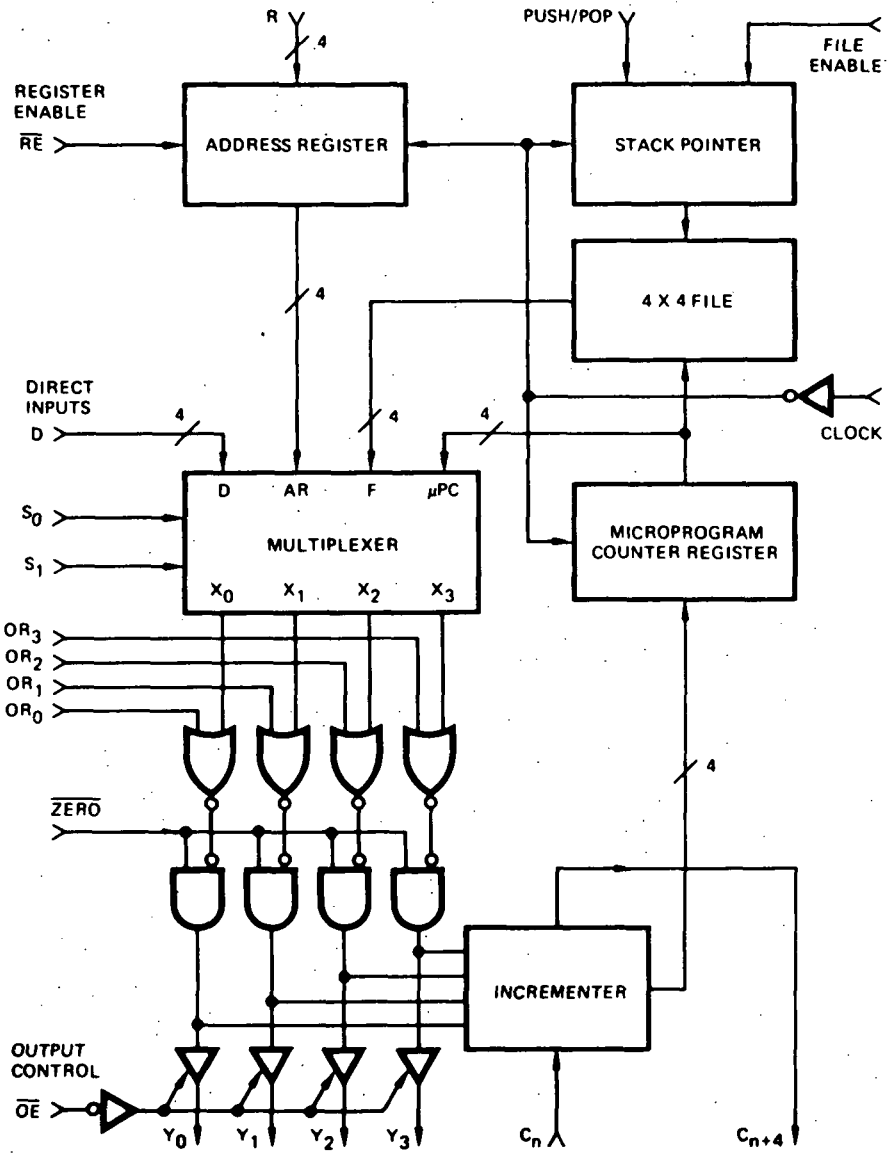
PROCESSOR



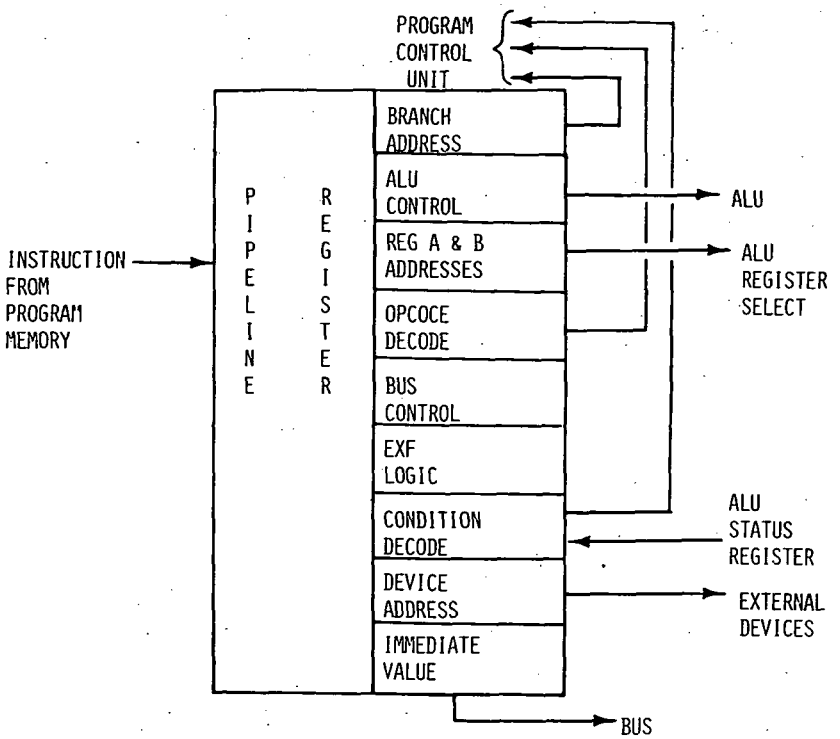
PCU



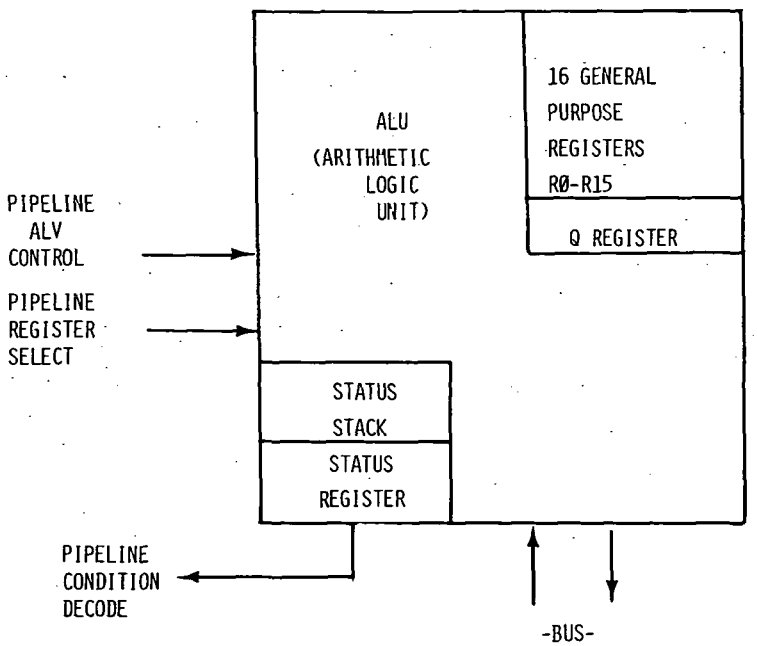
MICROPROGRAM SEQUENCER
BLOCK DIAGRAM



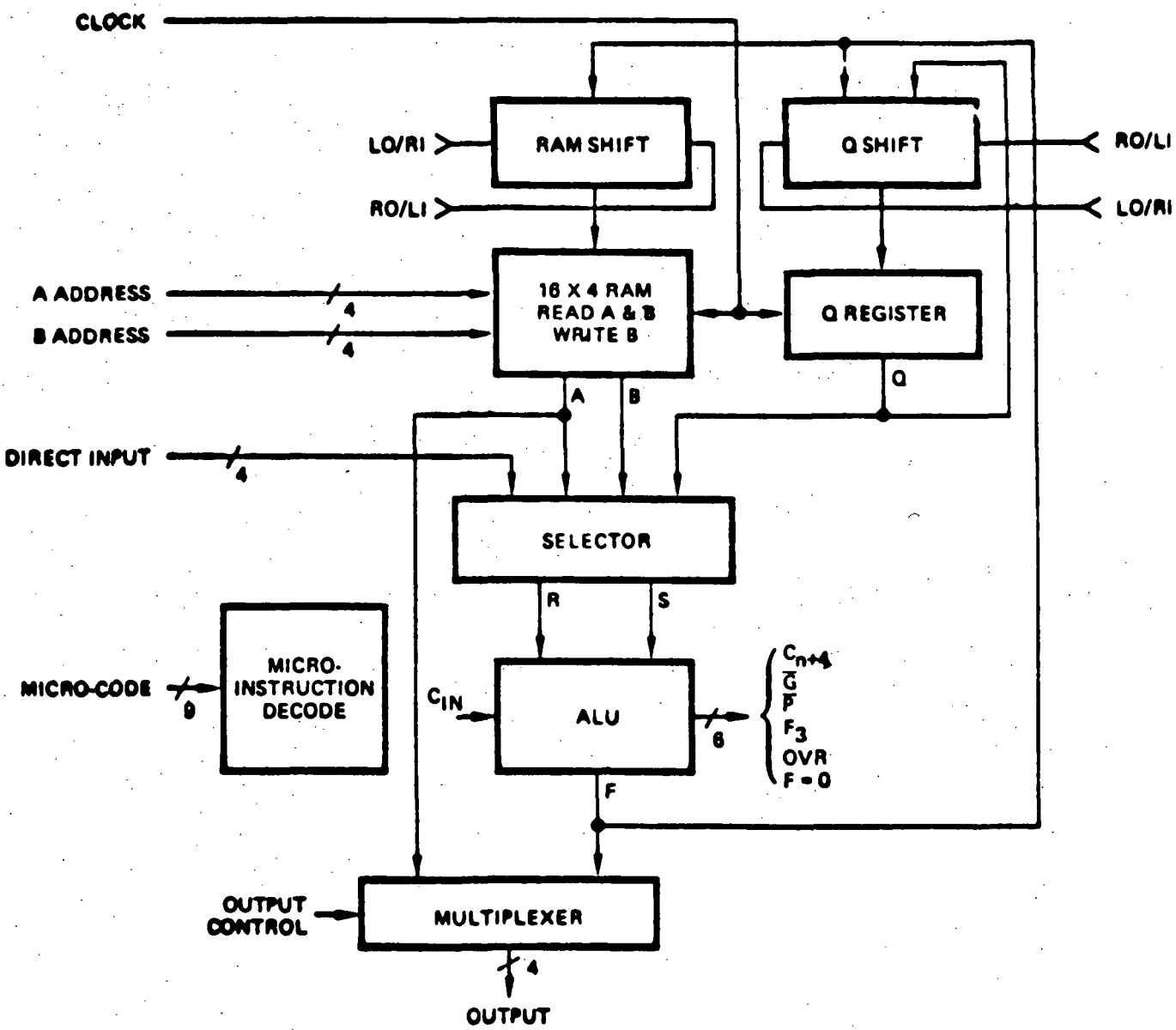
PIPELINE



ALU



MICROPROCESSOR SLICE BLOCK DIAGRAM



INSTRUCTION EXECUTION SPEED

TYPE	INSTRUCTION	EXECUTION (nSec)
0	REGISTER/REGISTER	250 or 325
1	INPUT/OUTPUT	350 OUTPUT 400 INPUT
2	REGISTER/IMMEDIATE	350
3	READ/WRITE PROGRAM MEMORY	525 READ 650 WRITE
4	EXTERNAL FUNCTION CONTROL	350
5	INTERRUPT CONTROL	400
6	PC STACK CONTROL	300
7	CONDITIONAL BRANCH	200 NO BRANCH 300 BRANCH

COMPARISON OF μPROCESSORS

	AMD AM2901	MMI MM6701	Intel 3002	TI SBP0400	Motorola M10800
Slice Width	4 bits	4-bits	2-bits	4-bits	4-bits
Cycle Time (Register to register; Read, Modify, Write)	100ns	200ns	150ns	1000ns	55ns
Power Dissipation (4 bits)	0.92W	1.12W	1.45W (2 x 0.73)	0.13W	1.3W
Addressable Registers	16	16	11	8	1 (External 4-256)
Register Addressing Mode	Two-Address	Two-Address	Single-Address	Single-Address	Single-Address
Number of Microcode Control Inputs	9	8	7	9	16
Primary Arithmetic Functions	R + S R - S S - R	R + S R - S S - R	R + S	R + S R - S S - R	R + S R - S S - R
Primary Logic Functions	5	3	3	8	6 - BCD 8 - Binary
Possible Source operand Combination to ALU	203	203*	24*	33*	6 - 262
Possible ALU Destination Registers	17	17	12	10	2 - 258
Flags	Carry Overflow Zero Negative	Carry Overflow Zero F=1111	Carry	Carry	Carry Overflow Zero

*Not all functions can be performed on all operand pairs.

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.