RCA

C-MOS ARRAY DESIGN TECHNIQUES

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Prepared for

NASA/Marshall Space Flight Center

Huntsville, Alabama

C-MOS ARRAY DESIGN TECHNIQUES

by A. Feller

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RCA
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for

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Huntsville, Alabama

ABSTRACT

The entire complement of standard cells and components, except for the Set-Reset Flip-Flop, have been completed. Two levels of checking were performed on each device. A description of each logic cell and a detailed topological layout are included.

All the related computer programs have been coded and one level of debugging has been completed.

The logic for the test chip was modified and updated. This test chip served as the first test vehicle to exercise the standard cell complementary MOS (C-MOS) automatic artwork generation capability.

PREFACE

Program Objectives

The objectives of this program are to develop and demonstrate the capability of automatically generating precision artwork for complementary MOS (C-MOS) integrated circuit arrays. The program encompasses the following design objectives:

1. Standard cell family - a basic family of standard circuit cells will be designed. Family members include:
   a. Inverter.
   b. Two-, three- and four-input NOR's.
   c. D-type and set-reset flip-flops.
   d. Two-, three- and four-input NAND's.
   e. Transmission and protective devices.
   f. Special process and mask components.
2. Circuit description:
   a. Static logic.
   b. Single supply.
   c. Logic swing - approximately equal to supply.
   d. Speed - a function of the process and the supply voltages. A realistic objective of nominal stage delays of 13 to 16ns with fan-outs of 2.5 loads appears to be obtainable with factory processes expected to be operational at the time chip fabrication is scheduled. This assumes a supply voltage of 10 volts.
3. Computer programs - Four major computer programs will be implemented for the C-MOS technology:
   a. Placement, routing and folding program - This program will provide for the automatic orientation or cell placement, the cell interconnections, and an acceptable form factor.
   b. Artwork program - This program will generate the instruction for an automatic artwork generator to plot the final mask artwork at some acceptable scale.

c. CalComp check plot - This program permits a composite check plot to be generated on a low-cost plotter for checking and optimization reasons.

d. Manual modification program - This program aids in implementing manual modifications when desired.

4. C-MOS standard cell basic system design including:

   a. Cell orientation.

   b. Power distribution.

   c. Low-leakage isolation.

   d. Variable standard cell heights.

   e. Production design rules.

   f. P-type tunnel.

   g. Standard guard band interface height.

   h. Maximum utilization of P-MOS programs.

5. Design of tests and generation of artwork for test chip encompassing:

   a. Static and dynamic evaluation of representative cells.

   b. Test of C-MOS system.

   c. Evaluation of programs.

   d. Determination of process and device parameters.

   e. Correlation.

6. Design criteria - The selection of the device geometries and therefore the standard cell height will reflect tradeoffs which consider the following:

   a. Design rules that are compatible with factory and production standards. This decision is based on insuring as reliable a device as possible since production standards are based on exhaustive preproduction evaluation and conservative quality control.

   b. Process parameters and characteristics either now in production or soon to be. Introduction of processes having significantly reduced threshold voltages and lower doping levels promise to deliver significant improvements in performance.

   c. Increased gate density.

   d. Chip dimension compatible with good yield.

   e. Compatibility with computer programs.

   f. Low power.

   g. Competitive speeds.

Scope of Work

The scope of this program encompasses the various phases of technology and families of computer programs required to automatically produce artwork for complex functional C-MOS integrated circuits arrays starting with the partitioned logic. Included in the program scope are the basic circuit designs and layouts for a defined standard cell family. Also included is the conceptual design and implementation of the C-MOS array or chip layout that considers systems, logic, and partition requirements, electrical and packaging considerations, mask generation and processing and fabrication constraints.

The required computer programs represent a family of programs. These programs are written in an atmosphere of close contact and continuing communication with circuit and device technologists forming part of the group responsible for this program.

Conclusions

why?

Generation of the seven levels of 80X artwork for the first logic design using this new technology has been accomplished with no fundamental problems experienced when combining the basic chip design concepts, the cell design and layouts, and the computer programming techniques.

Summary of Recommendations

It is recommended that the program continue since all objectives appear achievable within the program schedule and costs.

It is recommended that the fabrication of the test chip proceed without delay so that the program can be completed on schedule. With fabrication of the test chip, which NASA had stipulated it would arrange for, the successful implementation of the program will be easier to evaluate.

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Section 1

INTRODUCTION

Quarterly Report No. 2 covers the period from March 15, 1970 to June 15, 1970.

The information presented in this report includes:

(1) Status of the computer programs for the automatic generation of the mask artwork for the complementary MOS (C-MOS) integrated circuit arrays.

(2) Descriptions of the logic function, circuit configuration, and other engineering data for the C-MOS Standard Cell family.

(3) The seven-level topological composite drawing for each logic cell.

(4) Status of the Standard Cell family

(5) Characterization of each Standard Cell

(6) Description of C-MOS Standard Cell Array No. 1 - Test Chip.

Section 2

COMPUTER PROGRAM FOR C-MOS DESIGN AUTOMATION

A. C-MOS PLACEMENT ROUTING AND FOLDING (PRF) PROGRAMS.

Coding of the modifications for the Placement, Routing and Folding programs was completed. A CALCOMP plot of the first standard cell array, the test chip, was used to exercise and test the programs. This debugging process was used to check the Placement, Routing, and Folding Programs and the artwork generation, CALCOMP, Manual Modification, and other subroutines.

The debugging process also checked in various degrees all of the improvements in the Placement, Routing and Folding Programs that were coded during this reporting quarter. These improvements* include the following:

(1) Restart Capability
(2) Input Modification 1
(3) Input Modification 2
(4) Fixed Location Component
(5) Special Border Modification
(6) Chip Description Data
(7) Pad Relocation Capability.

The changes and modifications that arose out of the PRF program debugging phases were incorporated into the programs. The programs were then subjected to essentially their final test, the generation of the seven-level final mask artwork for the test chip. No errors were detected in the several program routines during the generation of this final mask artwork.

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*Descriptions of each of these capabilities can be found in Quarterly Report No. 1.

Section 3

STATUS OF THE DESIGN OF STANDARD CELLS

As indicated by the bar graph in Figure 1, all special-purpose and mask components have been configured, laid out, digitized, checked, and finalized. Electrical cell characterization does not apply to these cells. The functional logic cells (inverter, Buffer-Inverter, Two- Three- and Four-Input NOR, Two-, Three- and Four-Input NAND, and the Begin, Middle, End, and Free Shift) have been configured, laid out, digitized, checked, and finalized. Electrical characterization of these cells has begun as indicated in the bar graph. Errors were uncovered and corrected in several cells. The emphasis in this reporting period has been to assure that all cells associated with the test chip are correct and fully characterized before the test chip is fabricated.

Several layout arrangements for the Set-Reset Flip-Flop (Cell No. 1420) have been considered.

Cell No.	Cell Name	Configured	Laid Out	Digitized	Checked	Finalized	Verified	Characterized*
9010	Input Pad							N/A
9020	Output Pad							N/A
9100	Ground Pad							N/A
9110	V_D Pad							N/A
9210	Chip Alignment Key							N/A
9220	Chip Alignment Key							N/A
9230	Chip Alignment Key							N/A
9240	Chip Alignment Key							N/A
9250	Photo Alignment Key							N/A
9400	RCA Symbol							N/A
9410	NASA Symbol							N/A
9500	Tunnel End							N/A
9600	End Cap							N/A
9300	Test Transistor							N/A
1110	Inverter							
1120	Two-Input NOR							
1130	Three-Input NOR							
1140	Four-Input NOR							
1210	N & P Transistors							N/A
1220	Two-Input NAND							
1230	Three-Input NAND							
1240	Four-Input NAND							
1250	Test Resistors							N/A
1260	Begin Shift							
1270	Middle Shift							
1280	End Shift							
1290	Free Shift							
1310	Buffer Inverter							
1410	Miller Test							
1420	Set-Reset Flip-Flop							

*N/A is not applicable

Figure 1. C-MOS Standard Cell Design Status

Section 4

C-MOS STANDARD CELL ENGINEERING LIBRARY

The present family of C-MOS Standard Cell logical building blocks are described in Figures 2 through 13.

The library will provide the engineer with complete electrical, logical, and topological specifications for the family of cells. This data is presented in this section and in another independent section. The information in this section is in a form useful for systems design, logic design, and the preparation of inputs to the Standard Cell Design Automaton (DA) system for array design and analysis. The 7-level topological composites for each standard cell are presented in Section 5. Section 5 will be of particular importance when new cells are to be added.

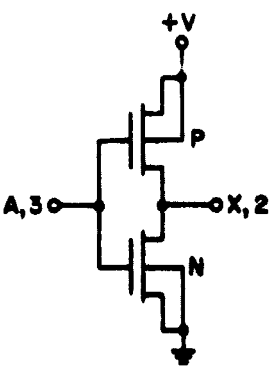
Each cell is listed by type and library number. To aid the logic designer, the logic symbol, Boolean expression, and truth table are given for each cell. The logic symbol and the truth table provide all necessary data to partition and generate the connection lists for any proposed logic system. More detailed cell information may be obtained by examining the circuit schematics or the composite topological layouts which are included in Section 5. The circuit designer will find the latter an invaluable aid in the analysis of interface problems between existing cells and proposed new cells.

When cell characterization is completed, input and output pin capacitance values and standard cell rise times, fall times, and propagation delays (as a function of output pin loading) will be included.

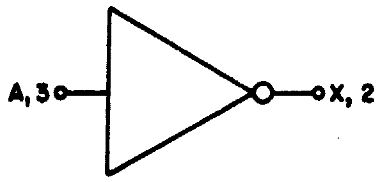
C-MOS STANDARD CELL

INVERTER — **CELL NO. 1110**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$X = \overline{A}$

TRUTH TABLE	
A	X
0	1
1	0

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
2	
3	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	19
RISE TIME	8
FALL TIME	7

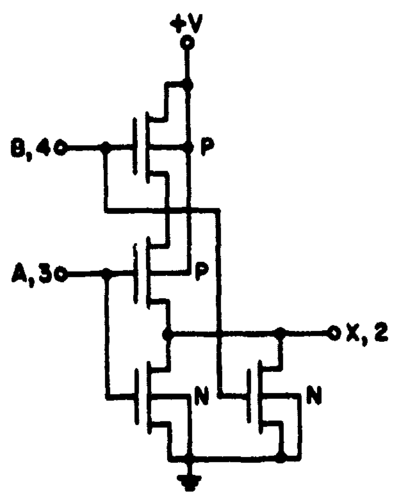
*C_L = 2.0 pF

Figure 2. Data for Inverter Cell No. 1110

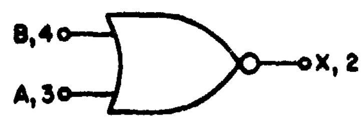
C-MOS STANDARD CELL

TWO-INPUT NOR **CELL NO. 1120**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$X = \overline{A + B}$

TRUTH TABLE		
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
2	
3	
4	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	22
RISE TIME	7
FALL TIME	8

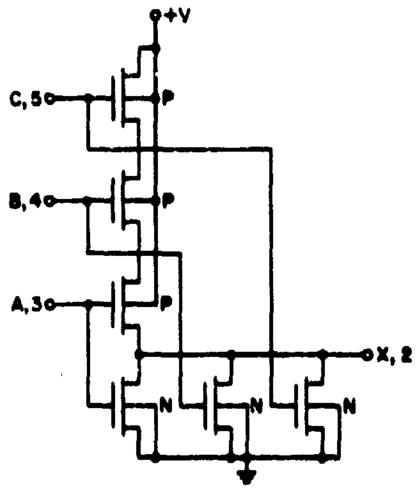
*C_L = 2.0 pF

Figure 3. Data for Two-Input NOR Cell No. 1120

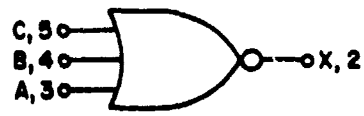
C-MOS STANDARD CELL

THREE-INPUT NOR — CELL NO. 1130

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = \overline{A + B + C}$$

TRUTH TABLE			
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
2	
3	
4	
5	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

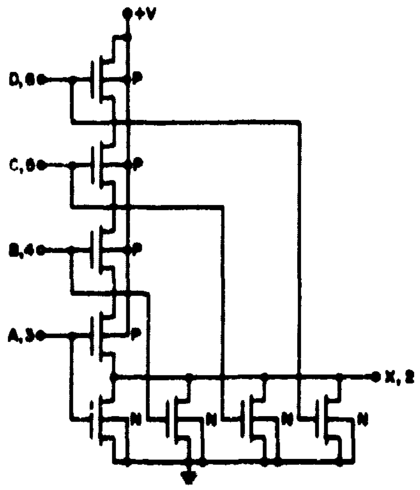
*C_L = 20 pF

Figure 4. Data for Three-Input NOR Cell No. 1130

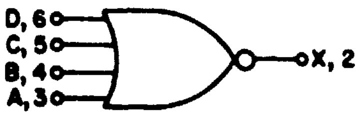
C-MOS STANDARD CELL

FOUR-INPUT NOR **CELL NO. 1140**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = \overline{A + B + C + D}$$

TRUTH TABLE

A	B	C	D	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	
3	
4	
5	
6	

DYNAMIC ELECTRICAL CHARACTERISTICS*

CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

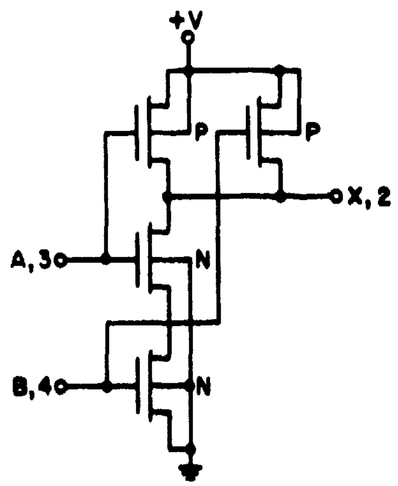
*C_L = 2.0 pF

Figure 5. Data for Four-Input NOR Cell No. 1140

C-MOS STANDARD CELL

TWO-INPUT NAND **CELL NO. 1220**

SCHEMATIC



LOGIC SYMBOL

LOGIC EQUATION

$$A = \overline{A \cdot B}$$

TRUTH TABLE		
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
2	
3	
4	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

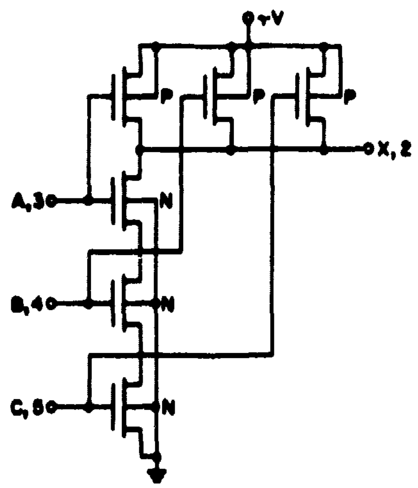
*C_L = 2.0 pF

Figure 6. Data for Two-Input NAND Cell No. 1220

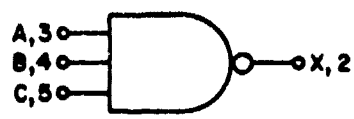
C-MOS STANDARD CELL

THREE-INPUT NAND **CELL NO. 1230**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = \overline{A \cdot B \cdot C}$$

TRUTH TABLE			
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
2	
3	
4	
5	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

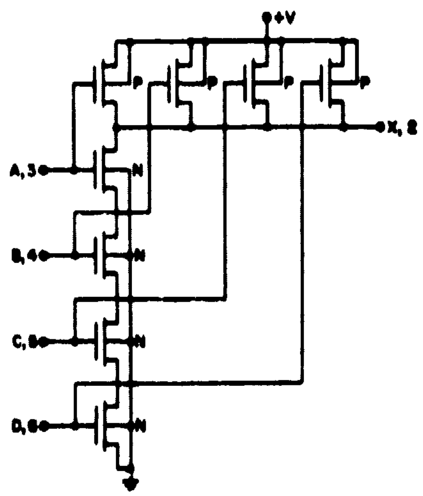
*C_L = 2.0 pF

Figure 7. Data for Three-Input NAND Cell No. 1230

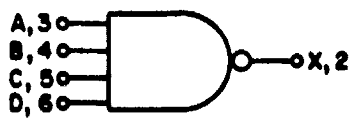
C-MOS STANDARD CELL

FOUR-INPUT NAND **CELL NO. 1240**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = \overline{A \cdot B \cdot C \cdot D}$$

TRUTH TABLE

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	
3	
4	
5	
6	

DYNAMIC ELECTRICAL CHARACTERISTICS*

CHARACTERISTIC	TIME (ns,
PAIR DELAY	
RISE TIME	
FALL TIME	

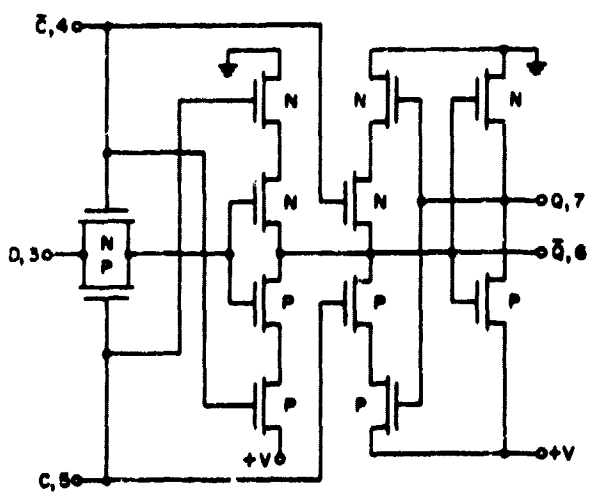
*C_L = 2.0 pF

Figure 8. Data for Four-Input NAND Cell No. 1240

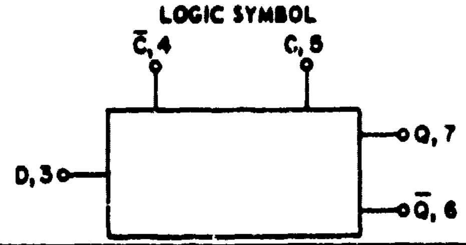
C-MOS STANDARD CELL

BEGIN SHIFT — **CELL NO. 1260**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

TRUTH TABLE			
C	D	Q	$\bar{Q}$
L→H	0	0	1
L→H	1	1	0
H→L	*	Q	$\bar{Q}$
L	*	Q	$\bar{Q}$
H	*	Q	$\bar{Q}$

*EITHER STATE

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
3	
4	
5	
6	
7	

DYNAMIC ELECTRICAL CHARACTERISTICS*

CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

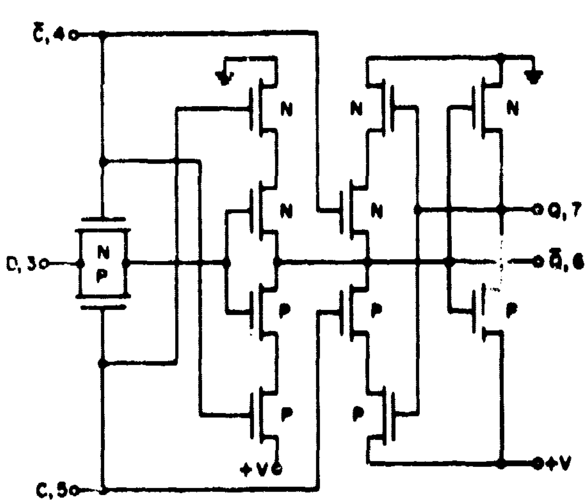
*C_L = 2.0 pF

Figure 9. Data for Begin Shift Cell No. 1260

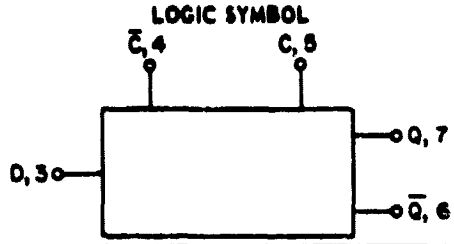
C-MOS STANDARD CELL

MIDDLE SHIFT **CELL NO. 1270**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

TRUTH TABLE

C	D	Q	Q̄
L→H	0	0	1
L→H	1	1	0
H→L	•	Q	Q̄
L	•	Q	Q̄
H	•	Q	Q̄

•EITHER STATE

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
3	
4	
5	
6	
7	

DYNAMIC ELECTRICAL CHARACTERISTICS•

CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

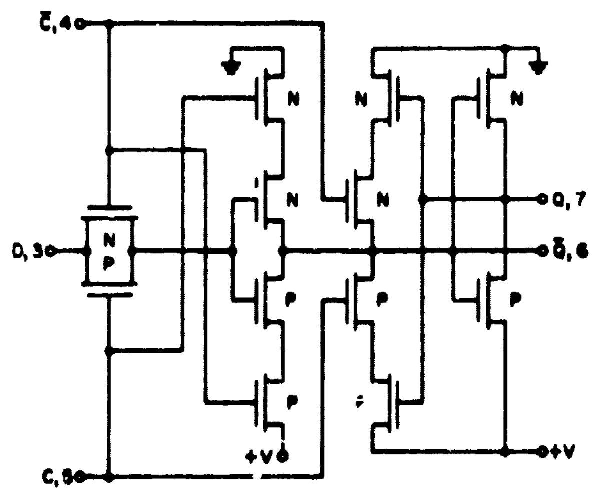
•C_L = 2.0 pF

Figure 10. Data for Middle Shift Cell No. 1270

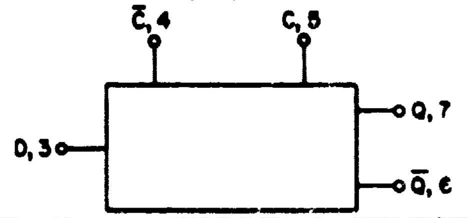
C-MOS STANDARD CELL

END SHIFT **CELL NO. 1280**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

TRUTH TABLE			
C	D	Q	$\bar{Q}$
L→H	0	0	1
L→H	1	1	0
H→L	*	Q	$\bar{Q}$
L	*	Q	$\bar{Q}$
H	*	Q	$\bar{Q}$

*EITHER STATE

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
3	
4	
5	
6	
7	

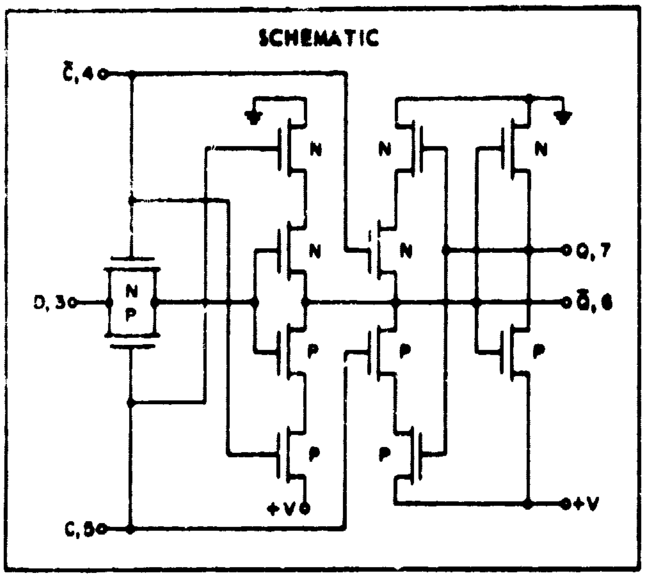
DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

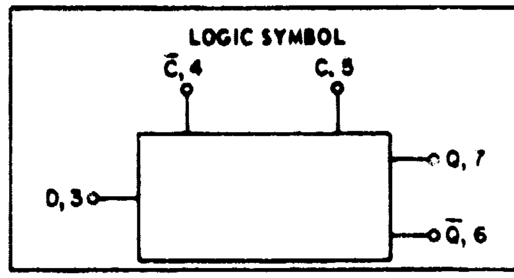
*C_L = 2.0 pF

Figure 11. Data for End Shift Cell No. 1280

C-MOS STANDARD CELL

FREE SHIFT **CELL NO. 1290**





LOGIC EQUATION

TRUTH TABLE			
C	D	Q	Q̄
L→H	0	0	1
L→H	1	1	0
H→L	*	Q	Q̄
L	*	Q	Q̄
H	*	Q	Q̄

*EITHER STATE

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
3	
4	
5	
6	
7	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

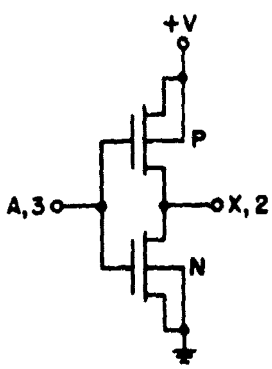
*C_L = 2.0 pF

Figure 12. Data for Free Shift Cell No. 1290

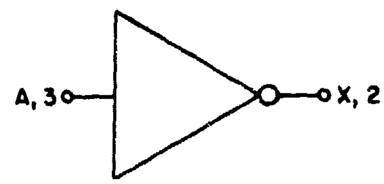
C-MOS STANDARD CELL

BUFFER INVERTER **CELL NO. 1310**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$X = \overline{A}$

TRUTH TABLE	
A	X
0	1
1	0

CELL I/O CAPACITANCE VALUES	
PIN	CAPACITANCE (pF)
2	
3	

DYNAMIC ELECTRICAL CHARACTERISTICS*	
CHARACTERISTIC	TIME (ns)
PAIR DELAY	
RISE TIME	
FALL TIME	

*C_L = 2.0 pF

Figure 13. Data for Buffer Inverter Cell No. 1310

Section 5

CMOS STANDARD CELL TOPOLOGIES

The detailed composite topological CALCOMP plots for each of the cells listed in Figure 1 are presented in Figures 14 through 35. The correct generation of the composite and each of the seven mask levels for each cell serves as one of the checking and monitoring steps in validating the various design steps which constitute the design cycle of each of the Standard Cells.

Because of the relative complexity of cell No. 1260, the Begin Shift cell, topologies of each of the first six levels are included in Figure 22 with the composite to facilitate the usefulness of the composite layout.

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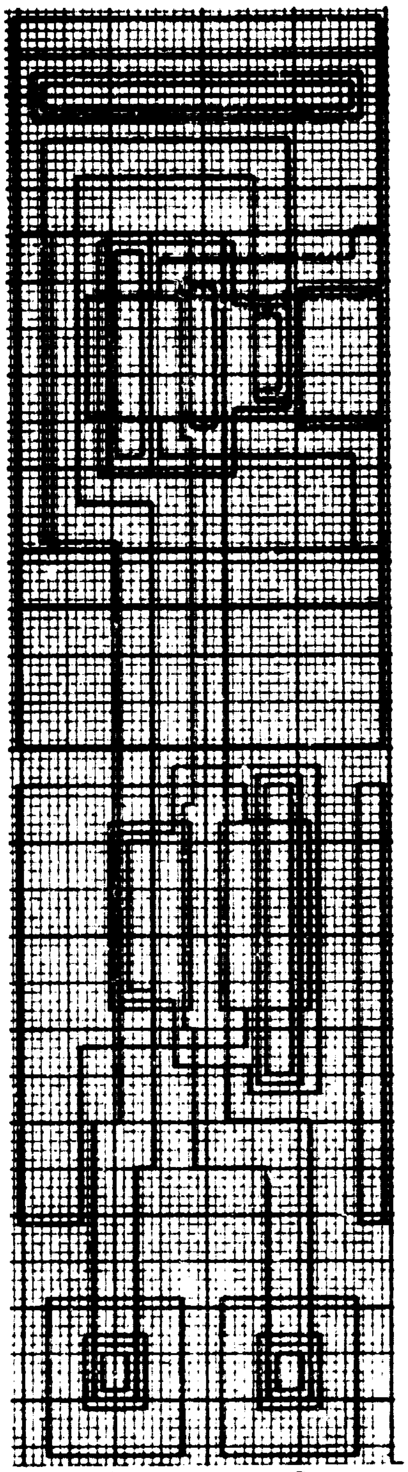

Figure 14. Composite Topology (Levels 1 through 6) for Inverter Cell No. 1110

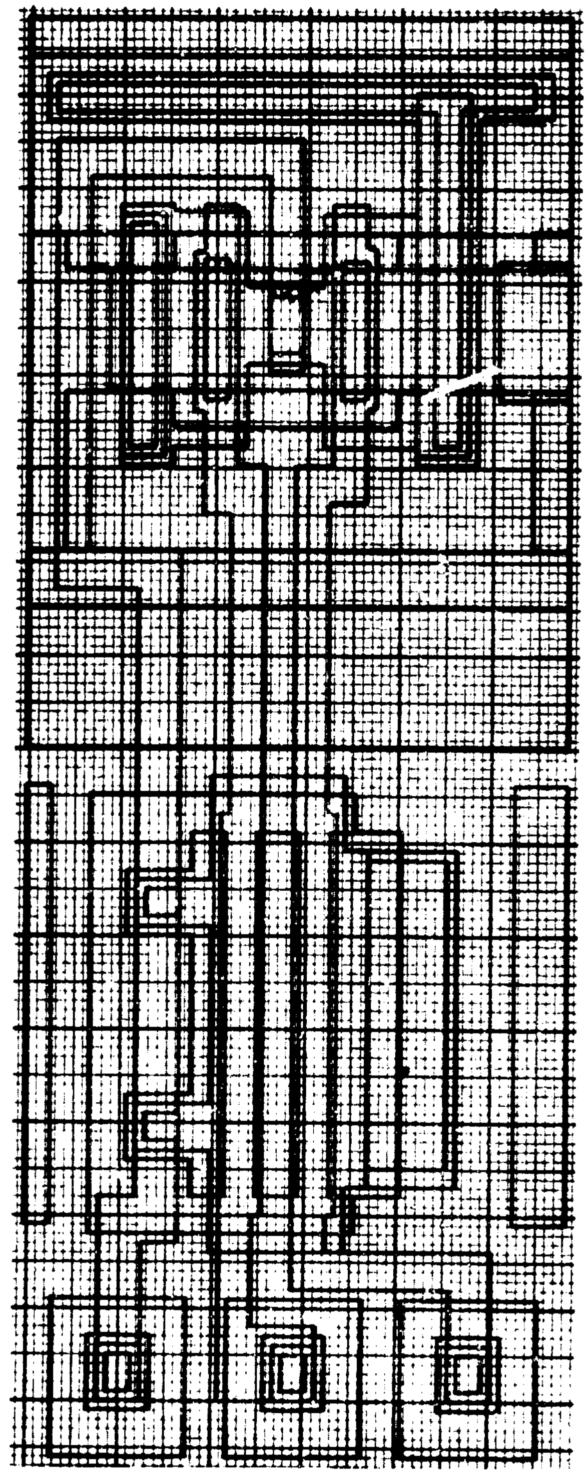

Figure 15. Composite Topology (Levels 1 through 6) for Two-Input NOR Cell No. 1120

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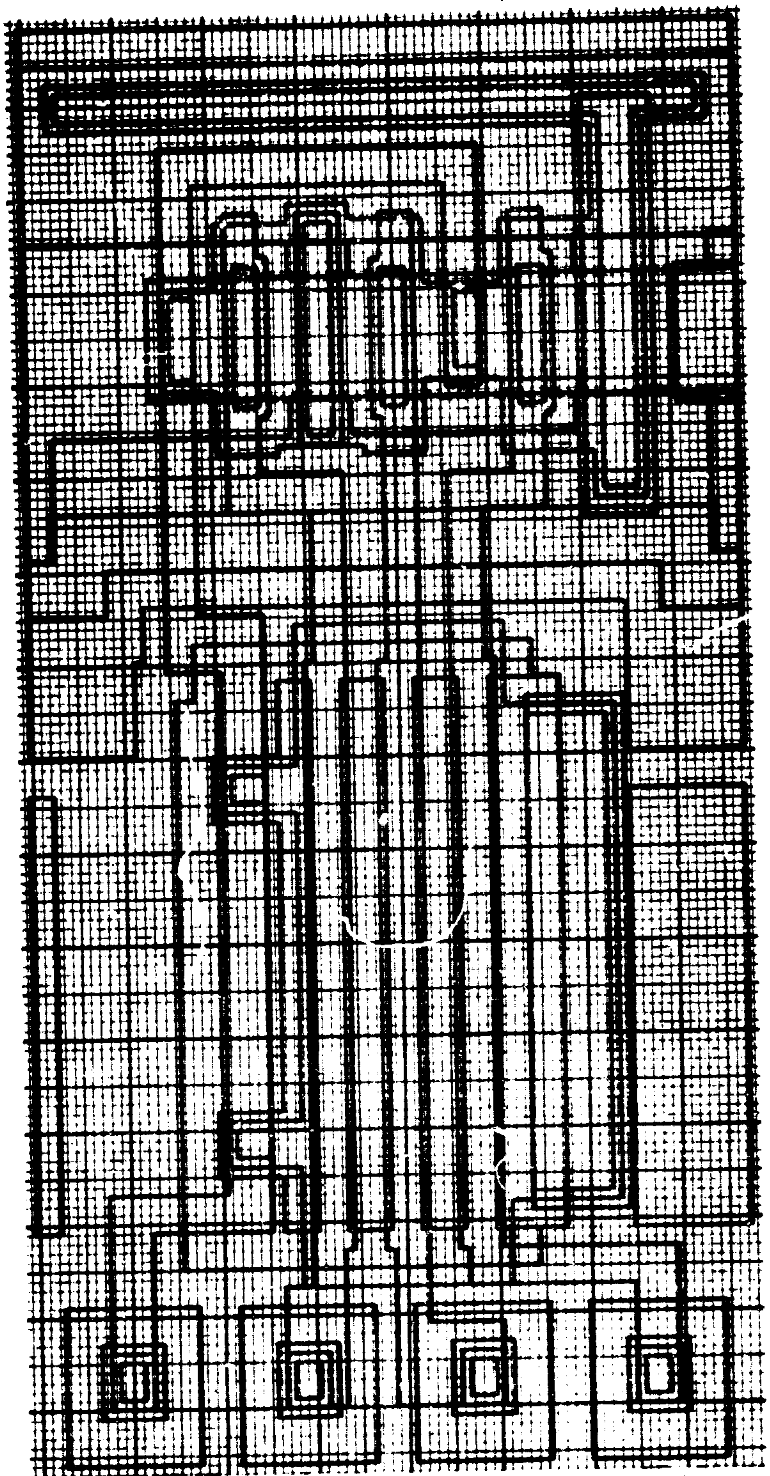

Figure 16. Composite Topology (Levels 1 through 6) for Three-Input NOR Cell No. 1130

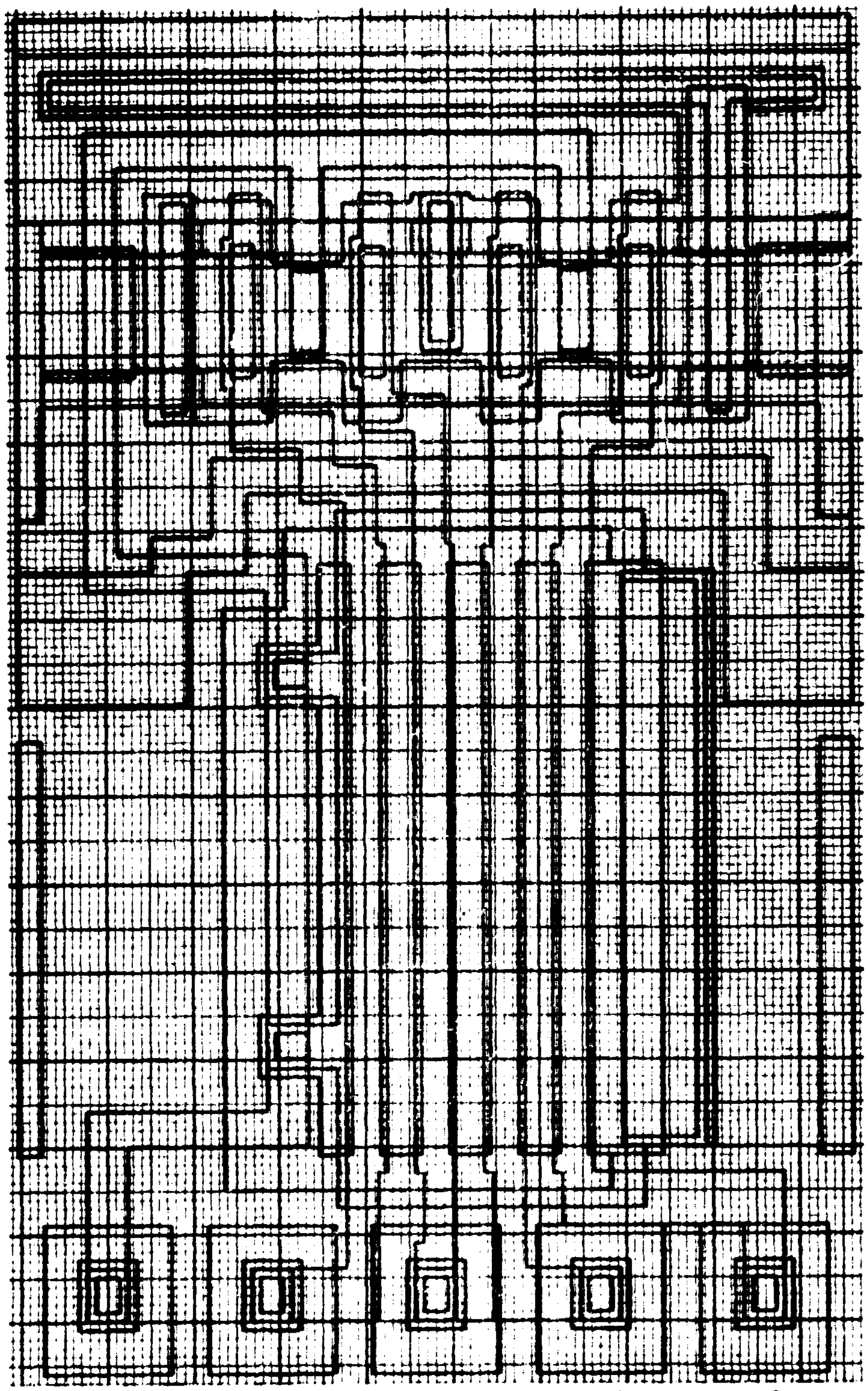

Figure 17. Composite Topology (Levels 1 through 6) for Four-Input NOR Cell No. 1140

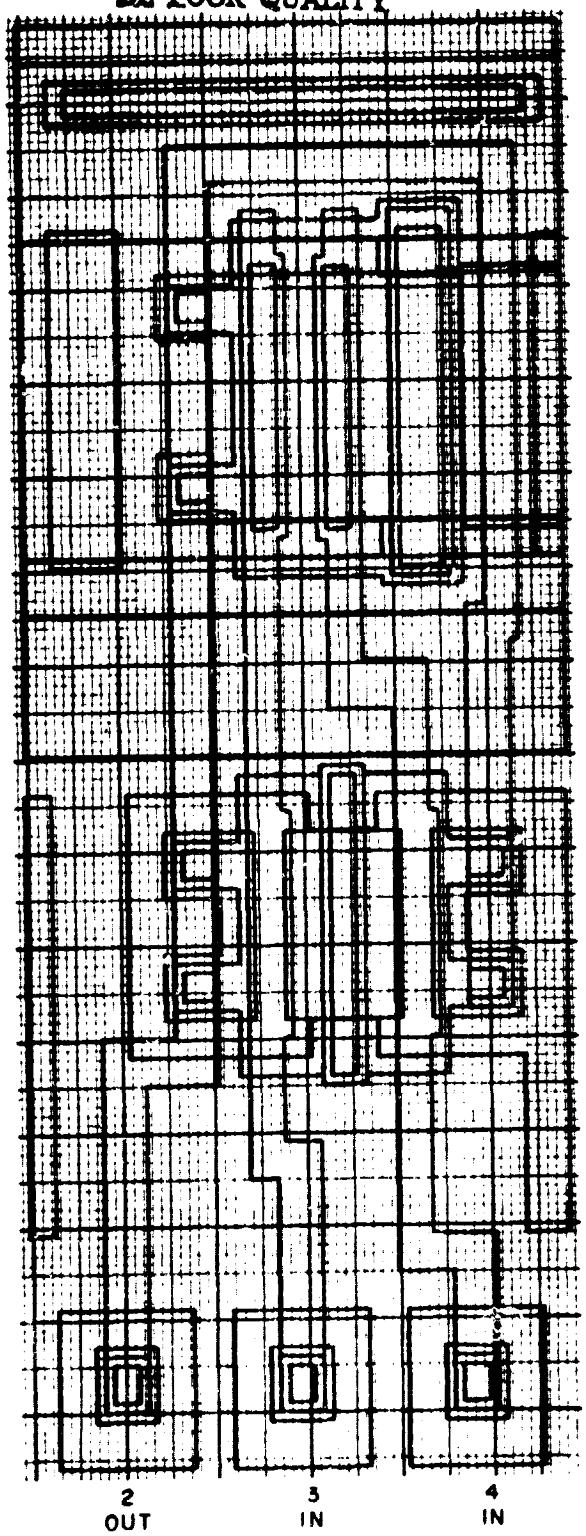

Figure 18. Composite Topology (Levels 1 through 6) for Two-Input NAND Cell No. 1220

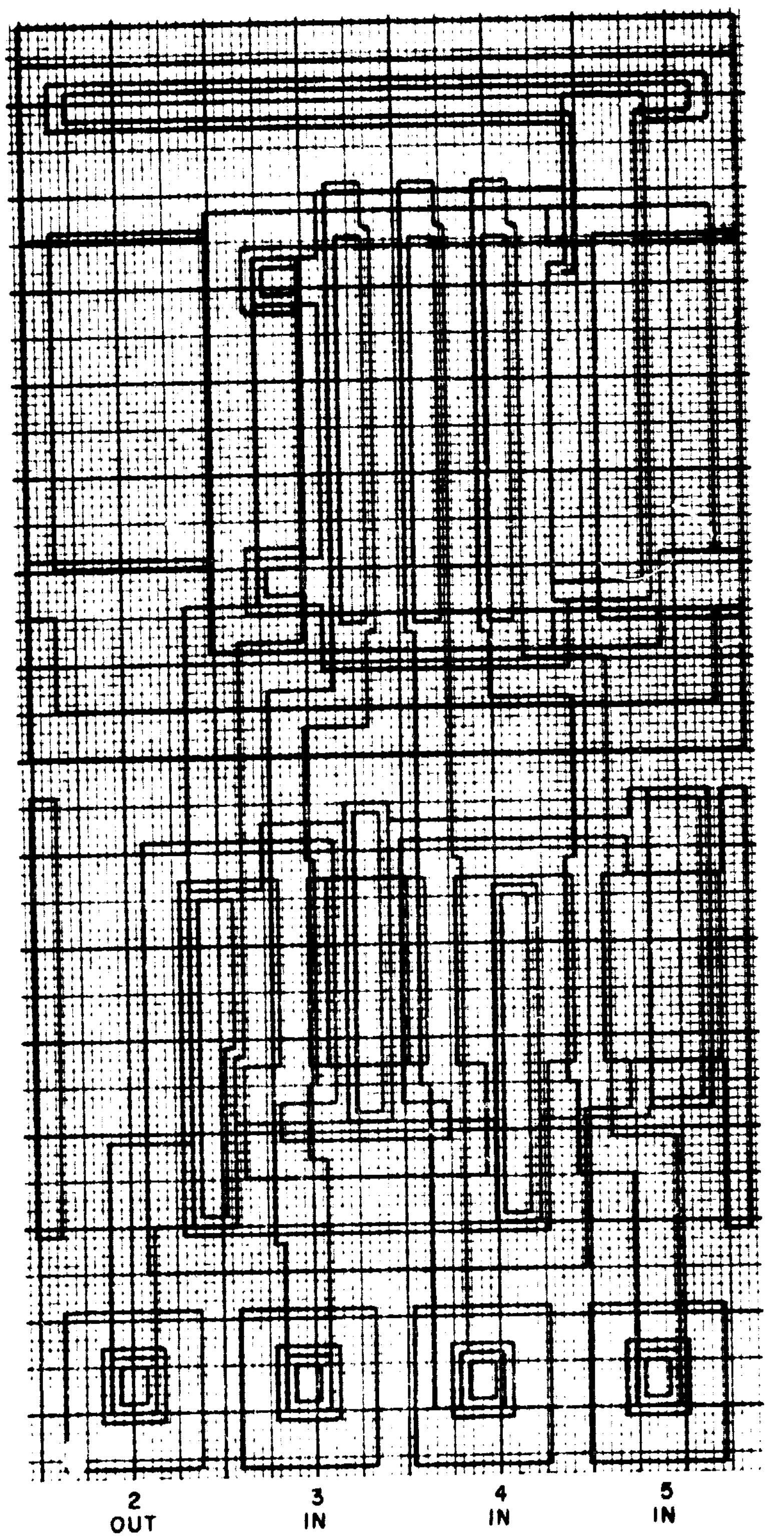

Figure 19. Composite Topology (Levels 1 through 6) for Three-Input NAND Cell No. 1230

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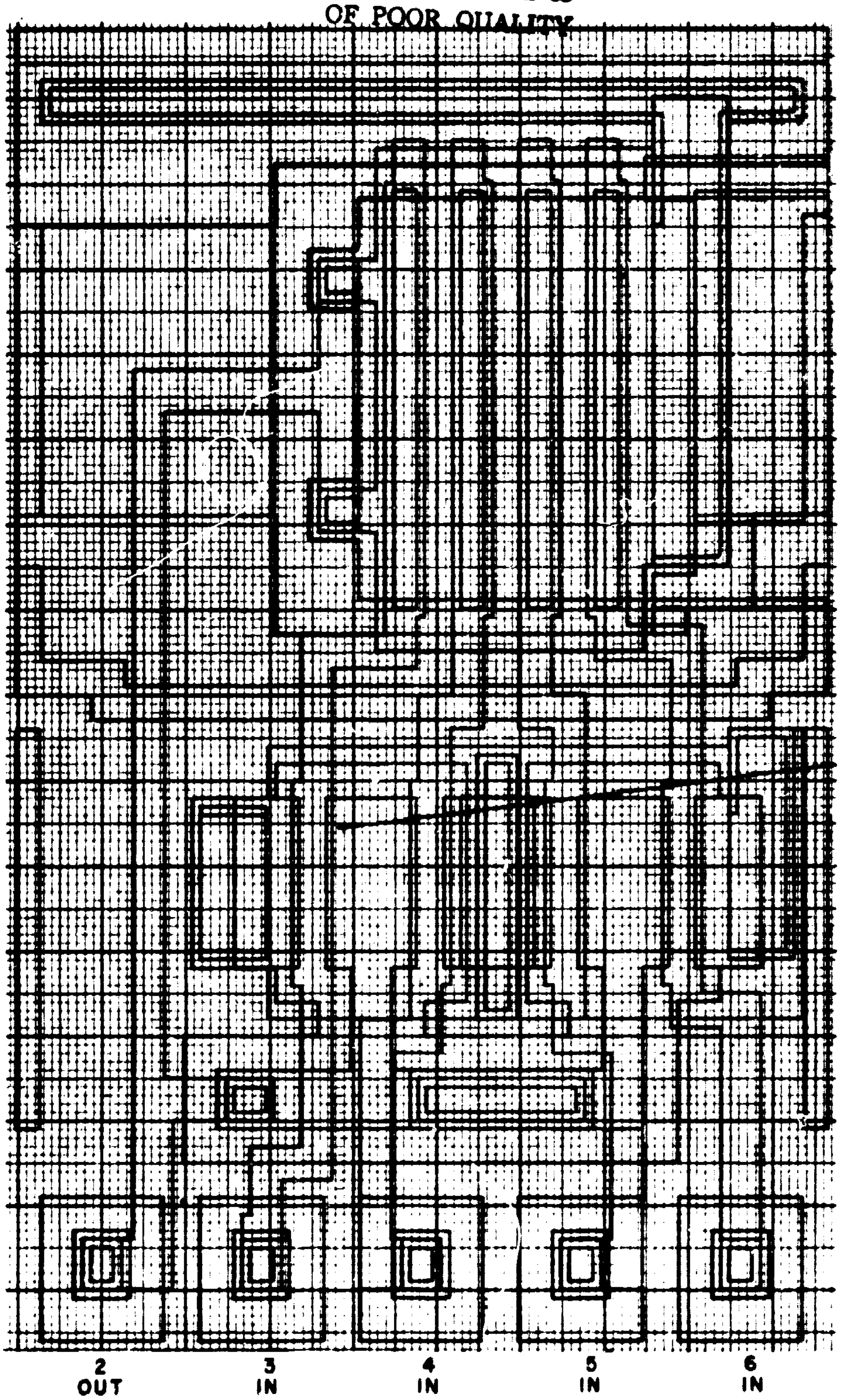


Figure 20. Composite Topology (Levels 1 through 6) for Four-Input NAND Cell No. 1240

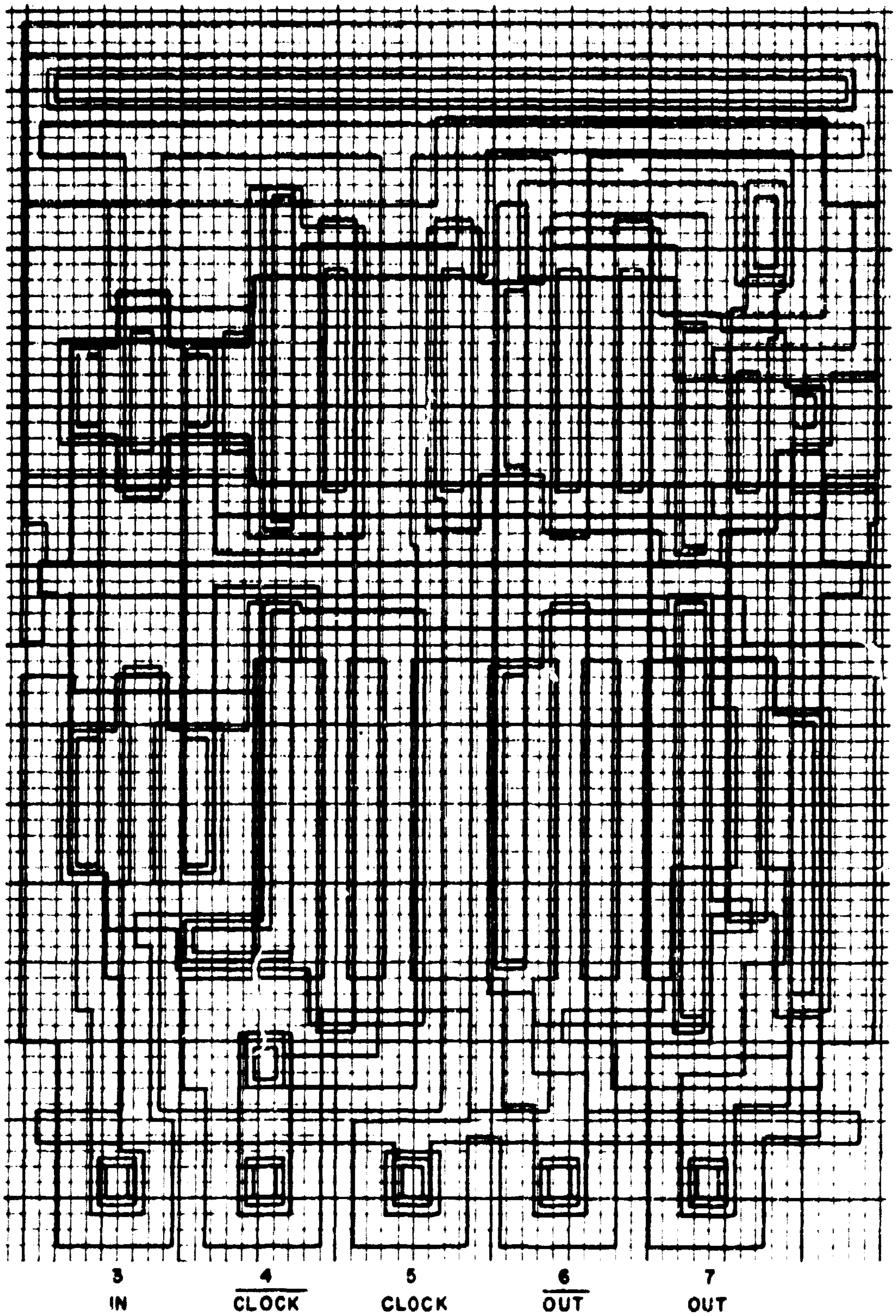
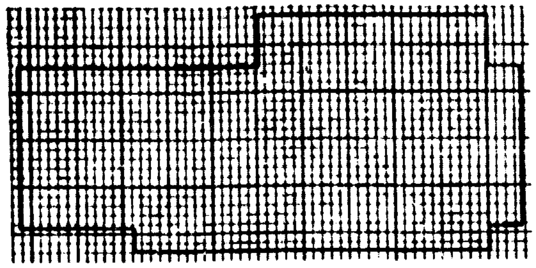
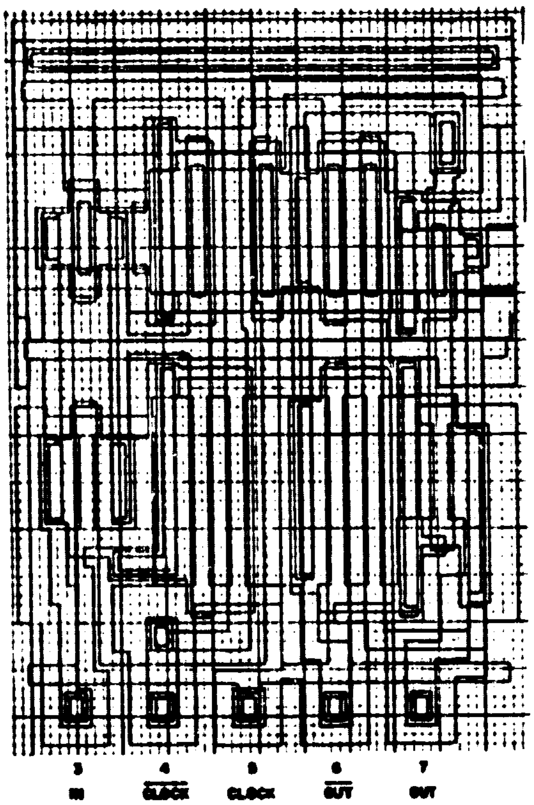


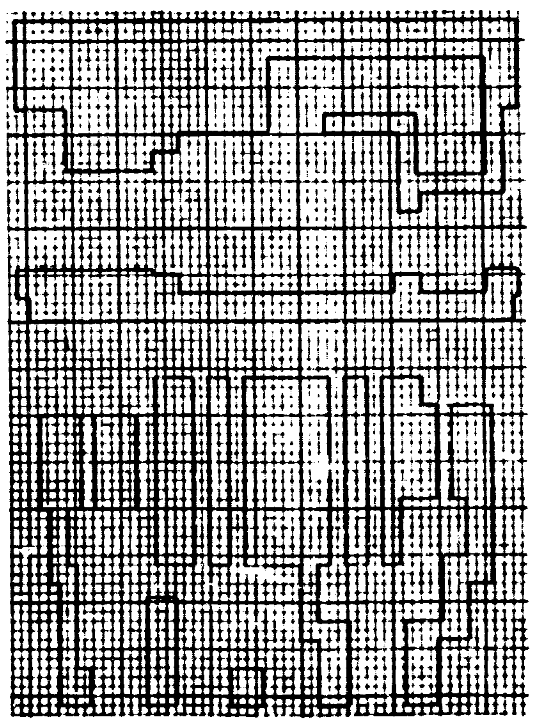
Figure 21. Composite Topology (Levels 1 through 6) for Begin Shift Cell No. 1260



LEVEL 1



COMPOSITE



LEVEL 2

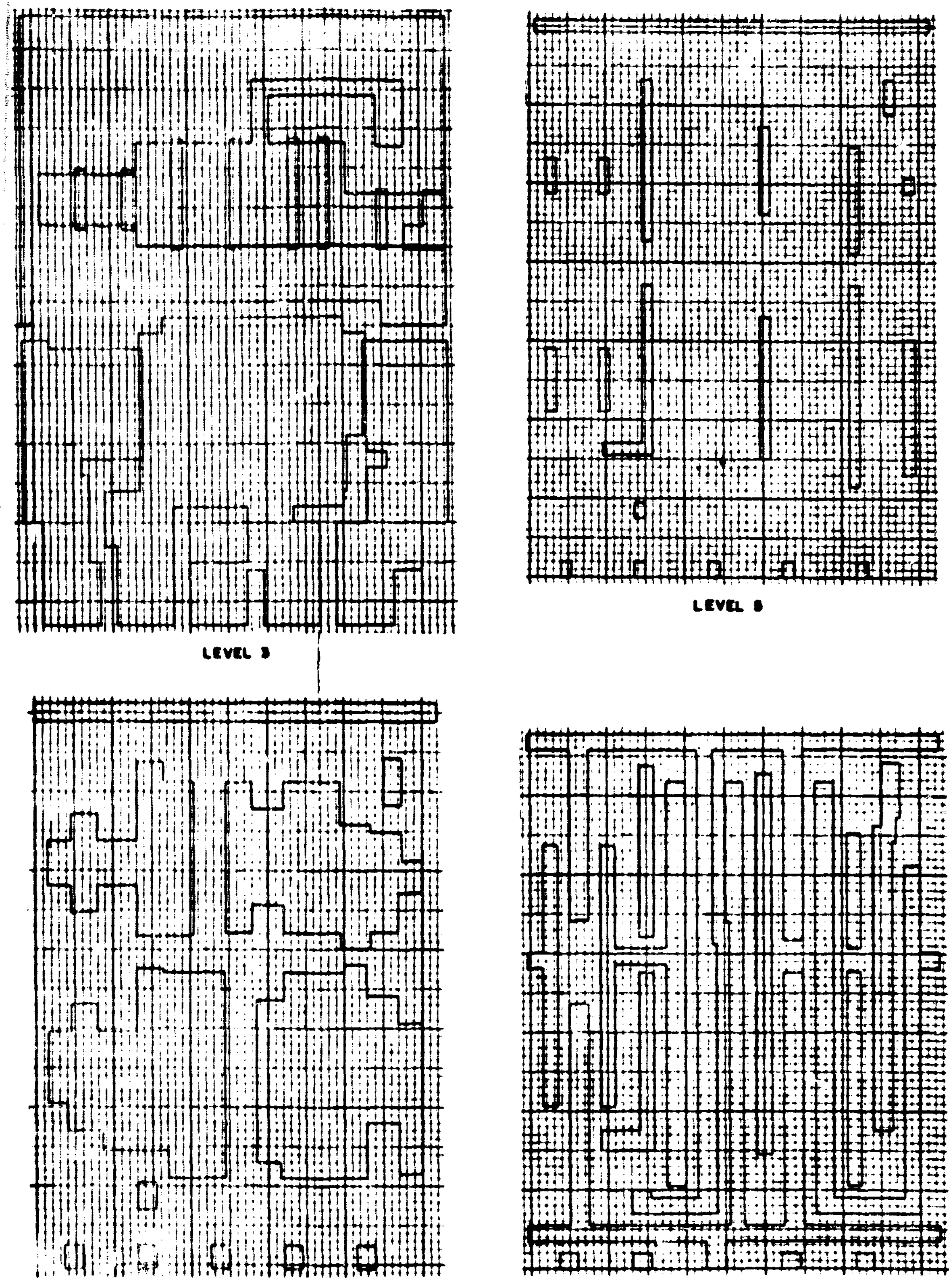


Figure 22. Composite and Individual Topologies (Levels 1 through 6) for Middle Shift Cell No. 1270

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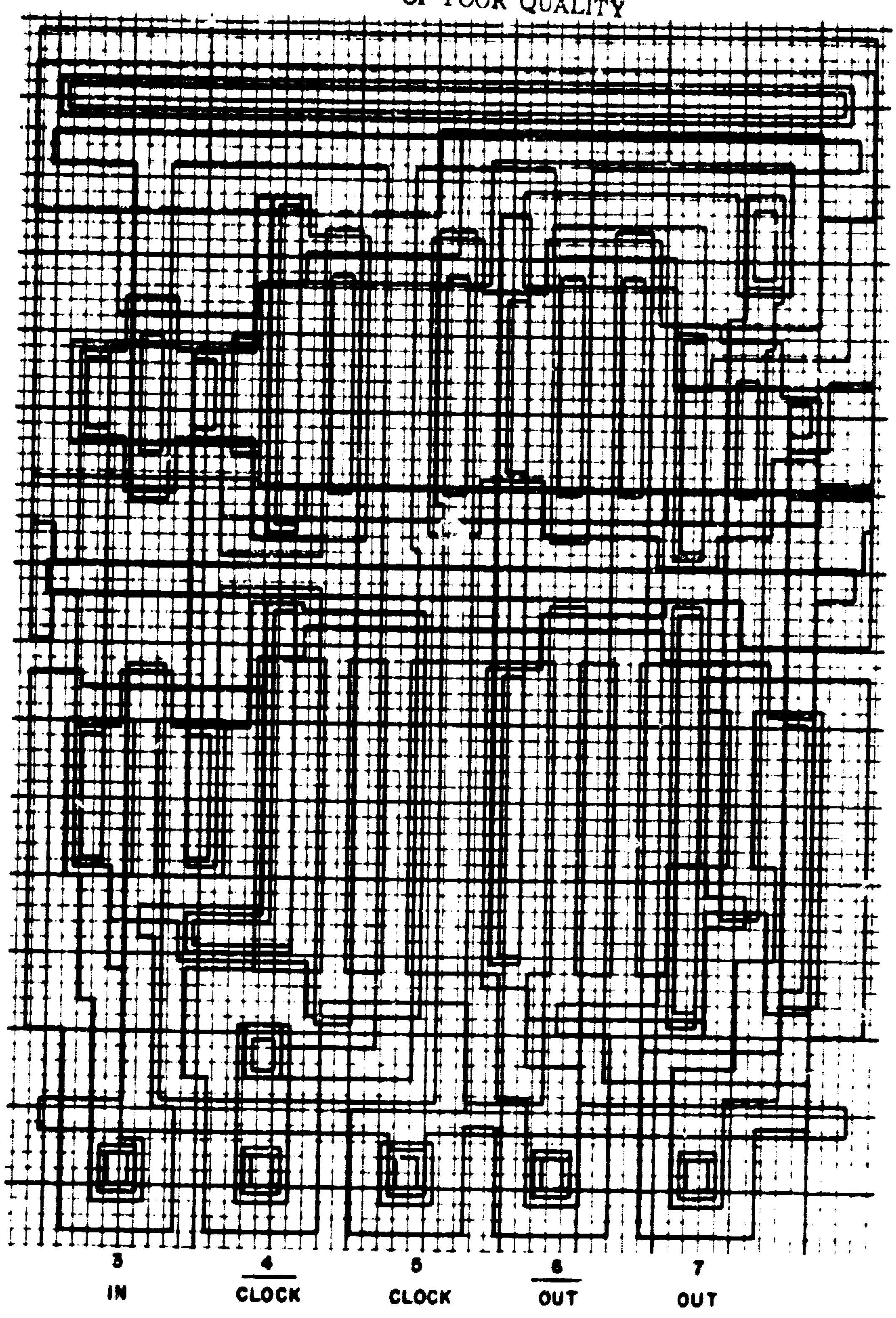

Figure 23. Composite Topology (Levels 1 through 6) for End Shift Cell No. 1280

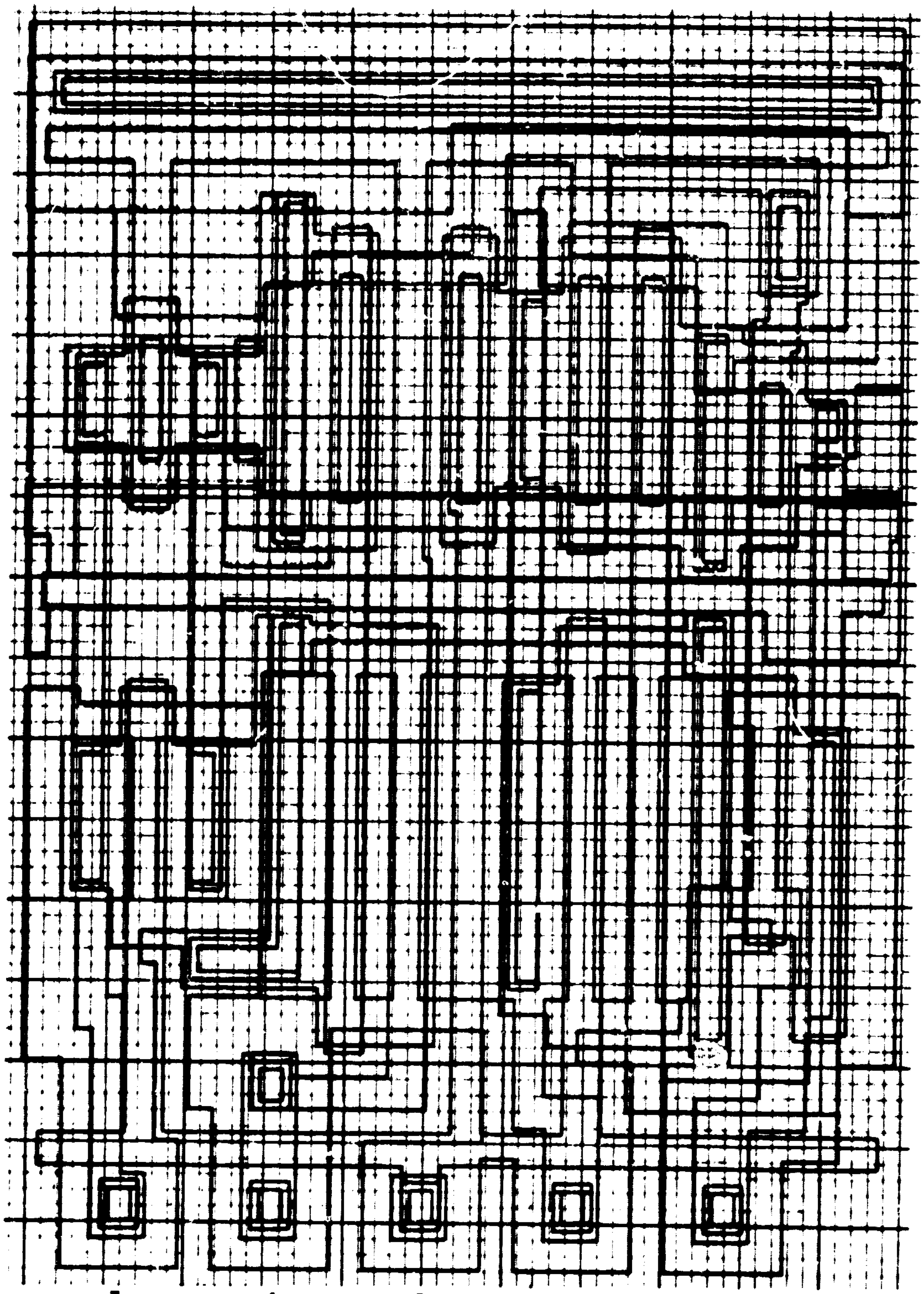

Figure 24. Composite Topology (Levels 1 through 6) for Free Shift Cell No. 1290

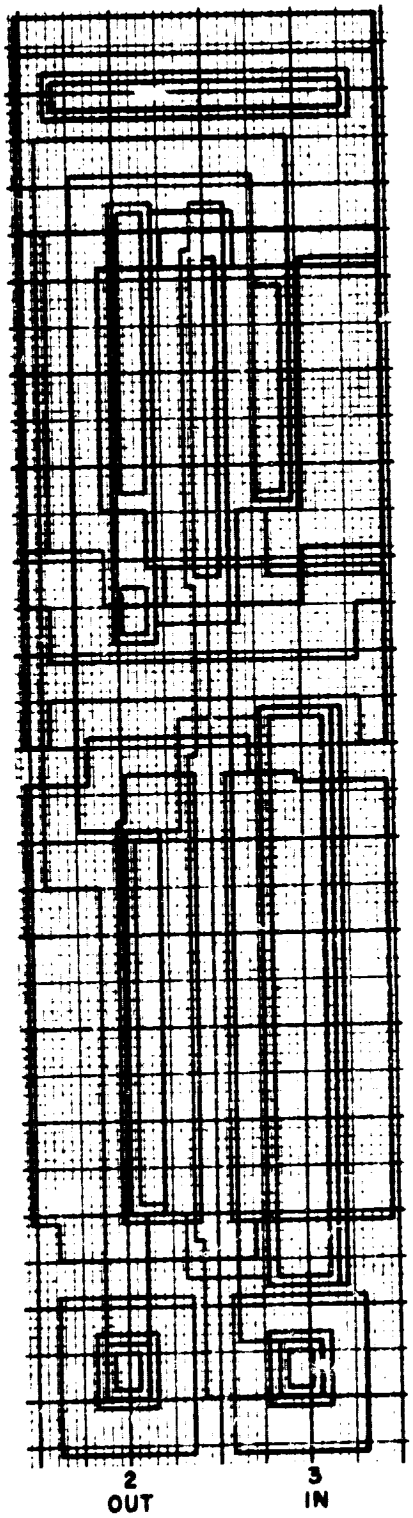

Figure 25. Composite Topology (Levels 1 through 6) for Buffer Inverter Cell No. 1310

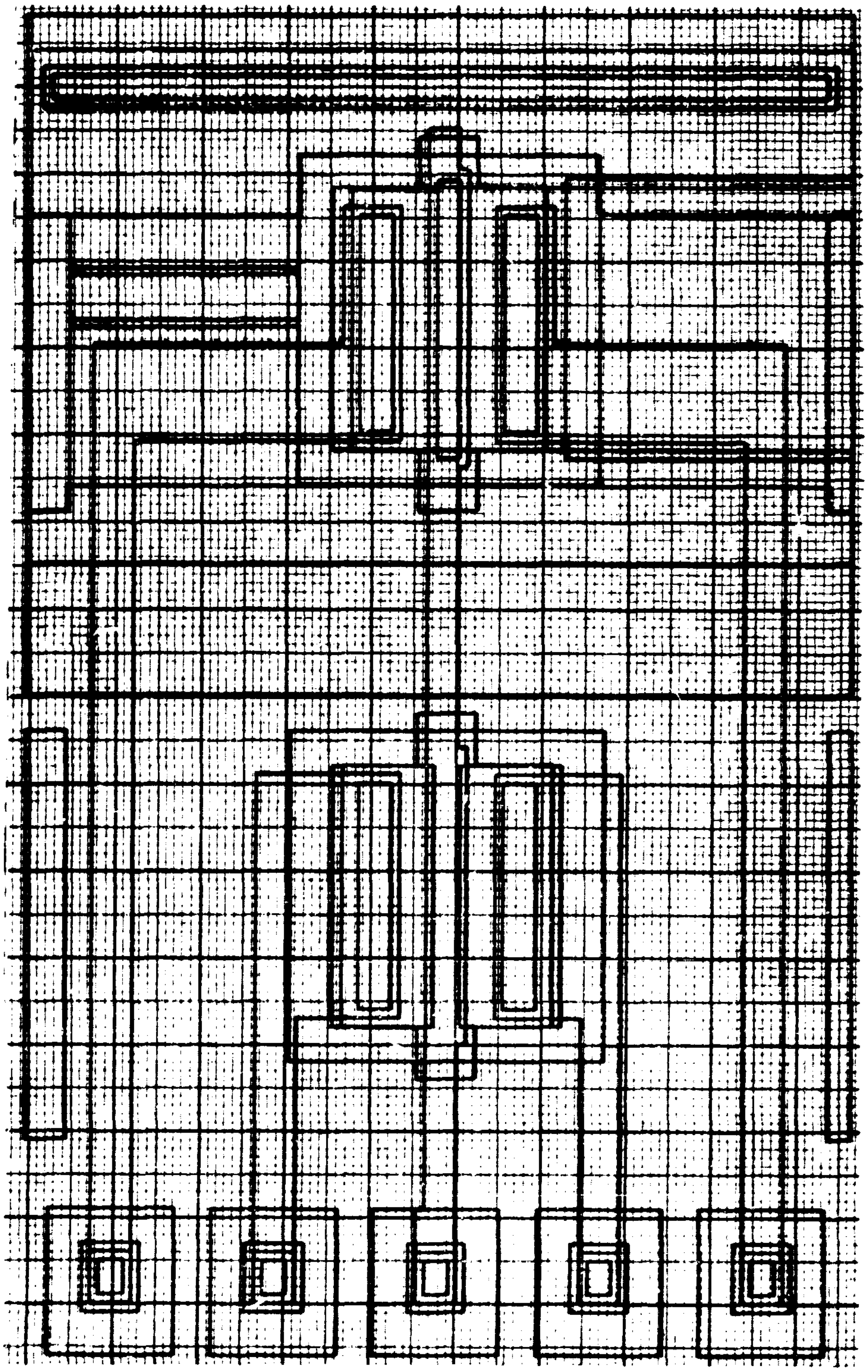

Figure 26. Composite Topology (Levels 1 through 6) for N&P Transistors Cell No. 1210

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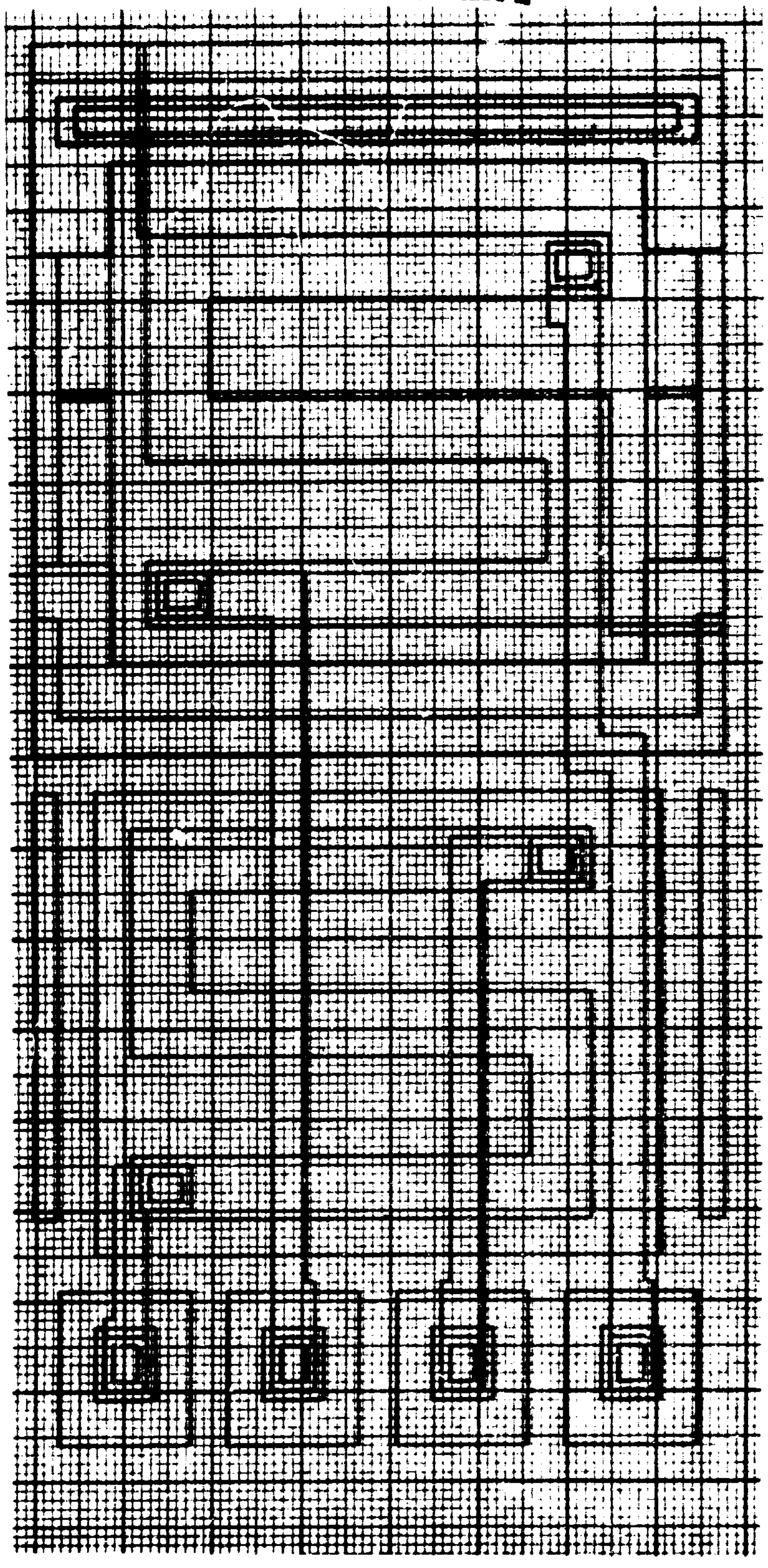

Figure 27. Composite Topology (Levels 1 through 6) for Test Resistors Cell No. 1250

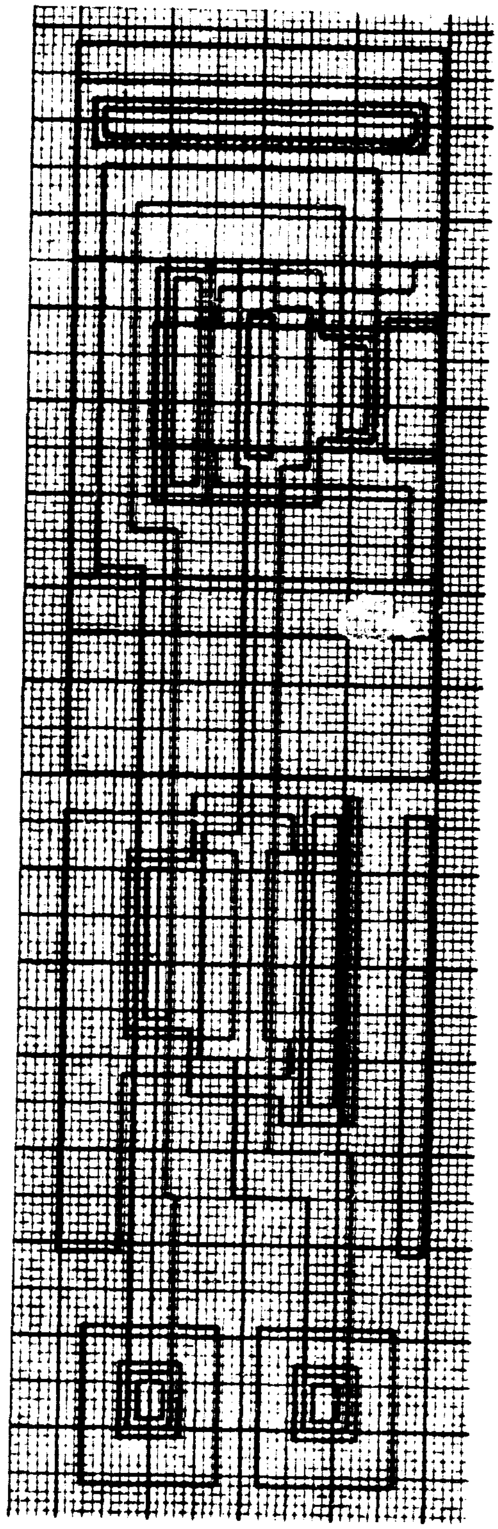

Figure 28. Composite Topology (Levels 1 through 6) for Miller Test Cell No. 1410

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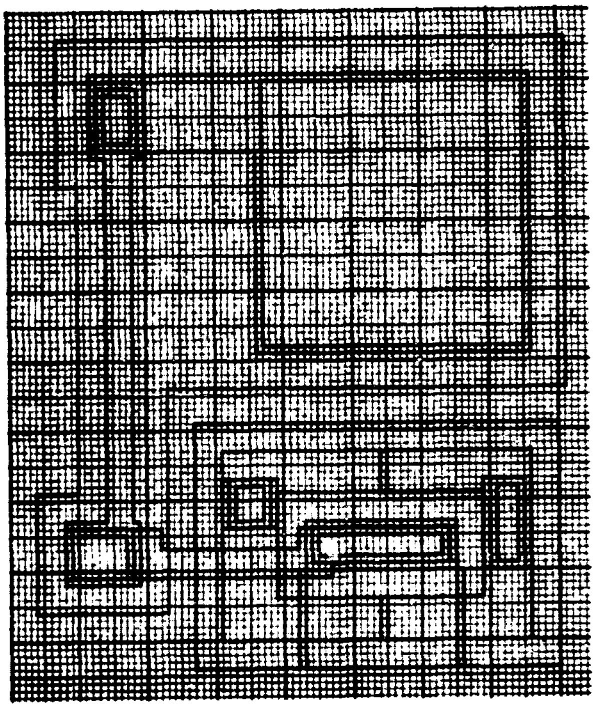

Figure 29. Composite Topology (Levels 1 through 7) for Input Pad Cell No. 9010

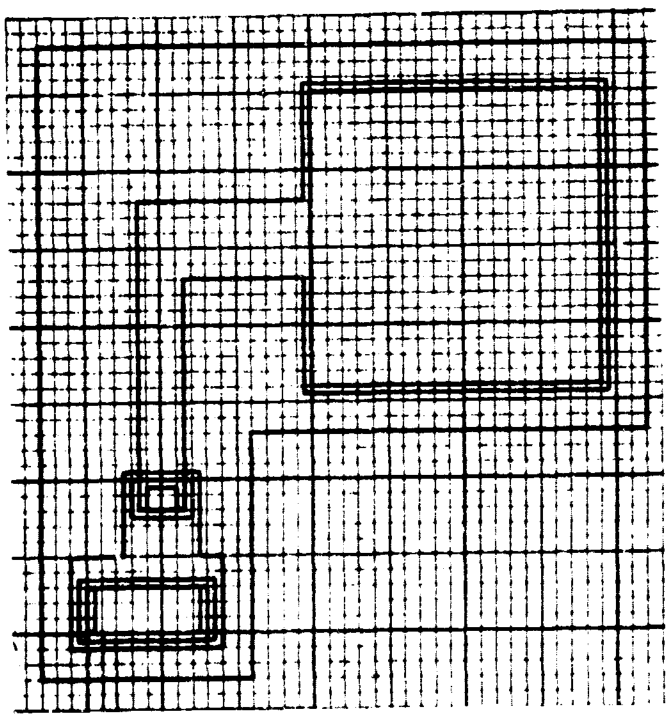

Figure 30. Composite Topology (Levels 2 through 7) for Output Pad Cell No. 9020

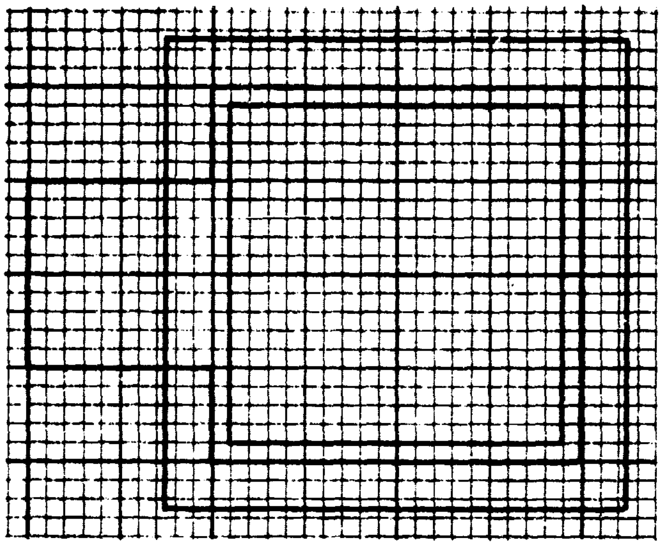

Figure 31. Composite Topology (Levels 3, 6, and 7) for Ground Pad Cell No. 9100

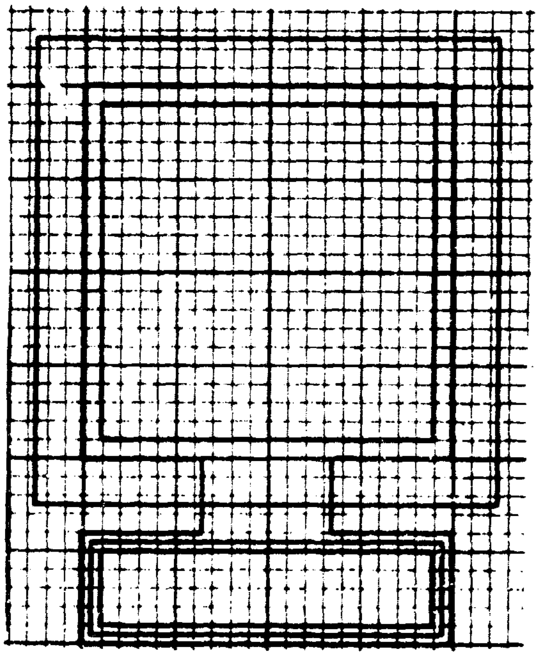

Figure 32. Composite Topology (Levels 3 through 7) for Power Pad Cell No. 9110

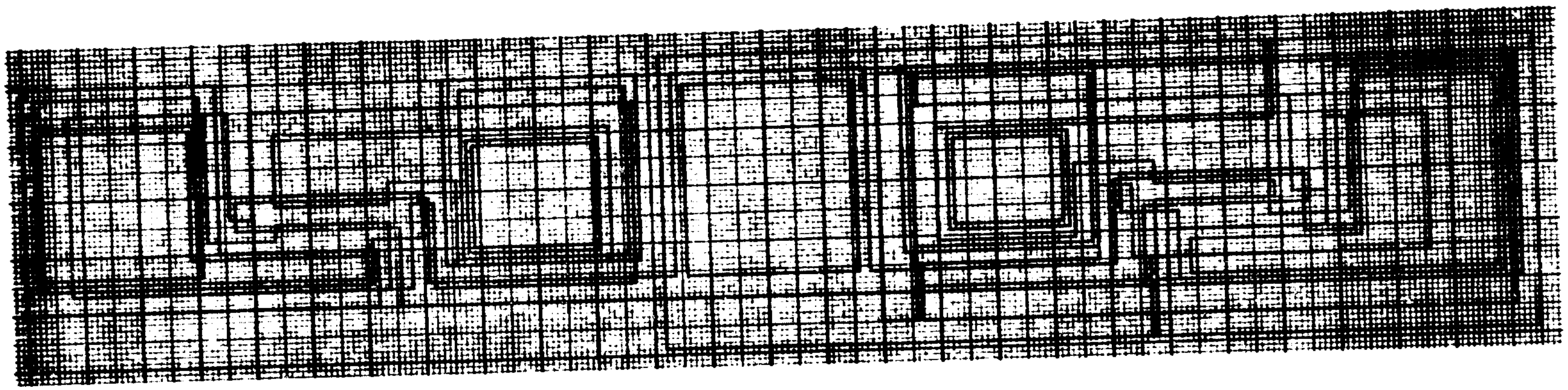

Figure 33. Composite Topology (Levels 1 through 7) for Test Transistor Cell No. 9300

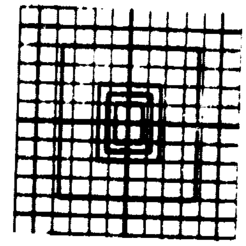

Figure 34. Composite Topology (Levels 2 through 6) for Tunnel End Cell No. 9500

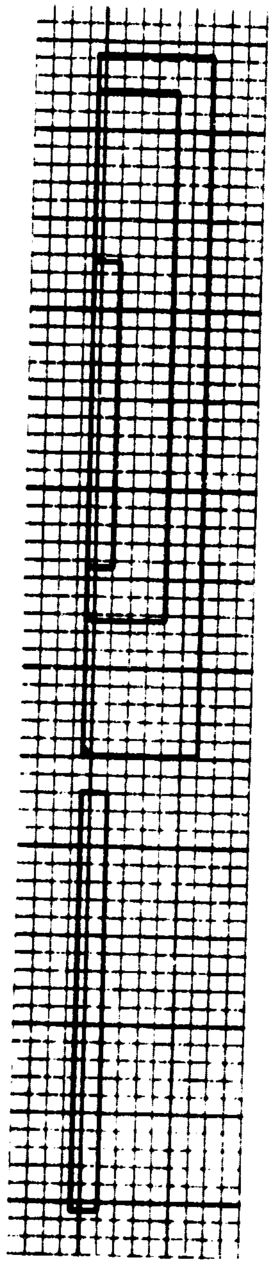

Figure 35. Composite Topology (Levels 1 through 3) for End Cap Cell No. 9600

Section 6

ELECTRICAL CHARACTERIZATION OF THE CMOS STANDARD CELL

This section describes those steps taken to date to verify and authenticate the circuit analysis techniques that are used to generate the delay characteristics for the standard cell family. The propogation delay for cell No. 1120, the two-input NOR, is generated using these correlated results. This first step correlation will be updated and refined after experimental measurements on the fabricated test chip have been made.

To obtain the parameters for the models used, both dc and transient measurements were taken on several commercially available RCA C-MOS Integrated Circuits that were processed using the new low-voltage process. From the dc measurements, the threshold voltage, substrate doping levels, channel mobilities, and channel lengths for the transistors in each circuit are obtained. A typical comparison of the measured transient response of several cascaded inverters with the computed transient reponse using experimentally measured device parameters is illustrated in Figure 36. A computed accuracy of greater than 10% (4ns/40ns) after three stages of logic was obtained as indicated in Figure 36. This correlation has been further improved by noting that the 0.8-pF Miller capacitance, shown in the schematic of Figure 36, was underestimated. Measurement at the pins of the IC package later indicated an actual Miller capacitance of 1.5 pF. When this measured values of capacitance is used, instead of the estimated value, correlations considerably better than 10% are obtained.

Having verified the accuracy of the RCA C-MOS Analysis Program, computed transient responses of C-MOS Standard Cell No. 1120 (Two-Input NOR) were generated.

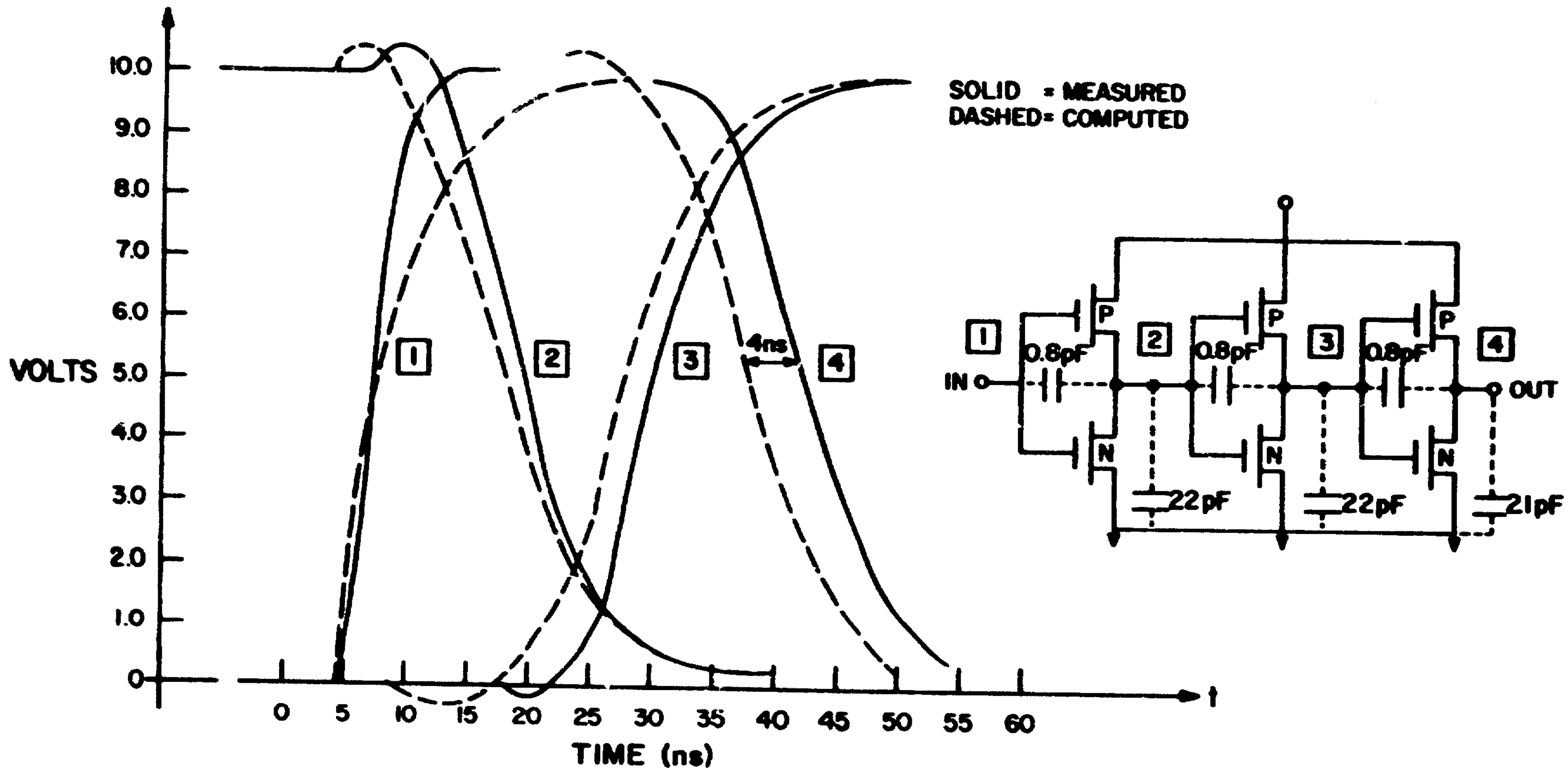

Figure 36. Schematic and Typical Computed and Measured Waveforms for RCA CD 4007 Cascaded Inverters

A schematic and the transient response for three cascaded Two-Input NOR cells are presented in Figure 37. The optimum process parameters assumed resulted in a computed 18-ns pair delay. The delay characteristics for the same cascaded Two-Input NOR cells calculated on the basis of nominal process parameters are presented in Figure 38. The somewhat slower speed (as indicated by the 23-ns pair delay) is attributable entirely to the higher substrate doping levels assumed for the nominal process parameters. For both cases nodes 5, 7, and 9 had 3.0-pF loads.

In addition to verifying the accuracy of the circuit analysis techniques that are to be used for the electrical characterization of the standard cells, it is also necessary to determine nominal values for the new low-voltage process transistor parameters. The parameter spread used for the delay calculations are presented in Table 1.

TABLE 1. PARAMETER RANGES FOR CHARACTERIZATION OF STANDARD CELLS

Parameter	Worst-Case Value	Best-Case Value
$N_A (cm^{-3})$	5.0×10^{16}	1.0×10^{16}
$N_D (cm^{-3})$	5.0×10^{15}	2.0×10^{15}
T_{ox} (cm)	$.105 \times 10^{-4}$	$.100 \times 10^{-4}$
V_{TN}, V_{TP} (V)	2.5, -2.7	1.3, -2.0
μ_N, μ_P (cm^2/V-s.)	400, 153	440, 170

Similarly, values for the P-N junction capacitance per unit area and the MOS gate capacitance per unit area have been determined. Presently the following values of capacitance are being used.

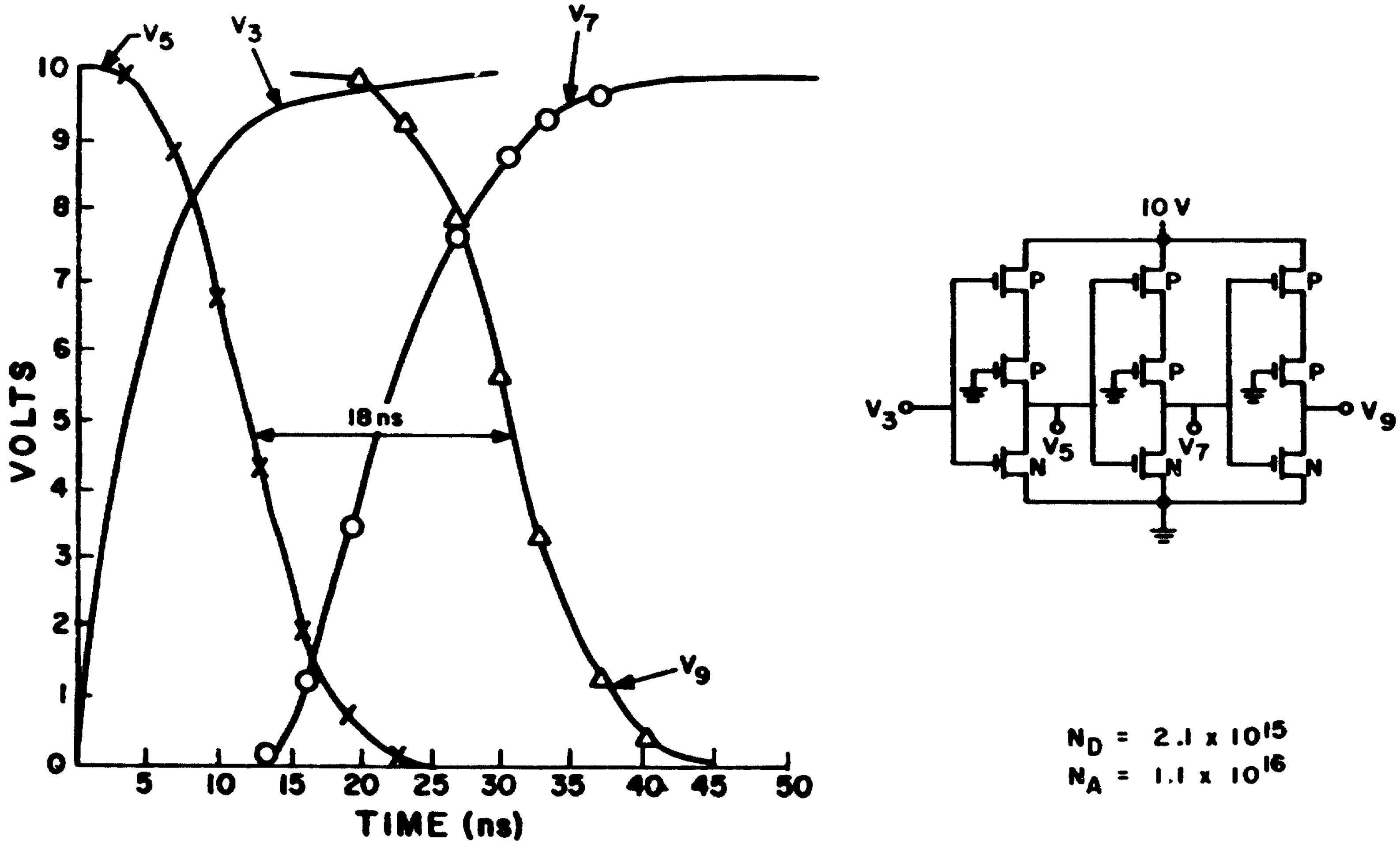

Figure 37. Schematic and Transient Response for Three Cascaded Two-Input NOR Cells (No. 1120) with Delay Characteristics Calculated on the Basis of Ophmum Process Parameters

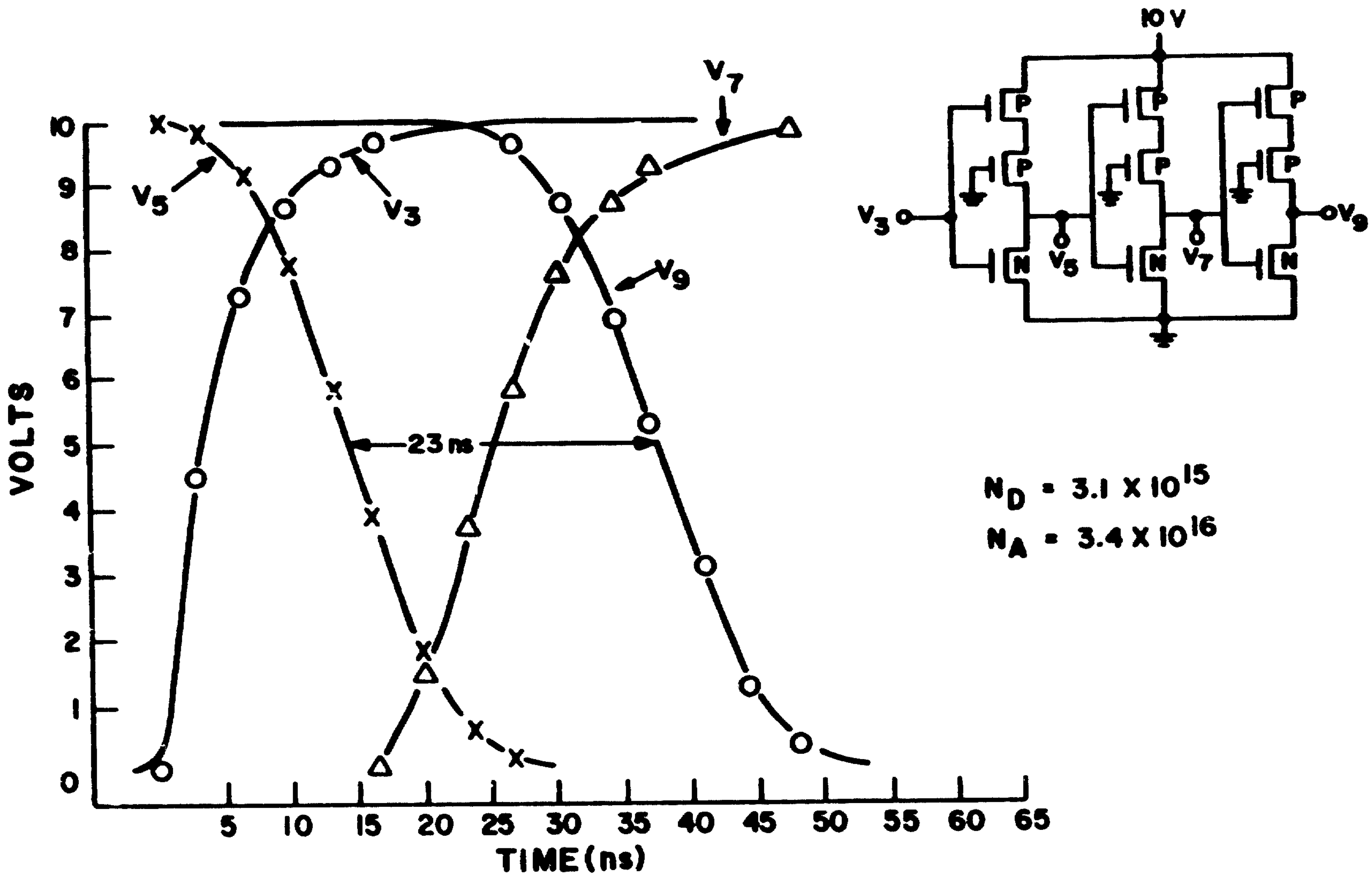

Figure 38. Schematic and Transient Response for Three Cascaded Two-Input NOR Cells (No. 1120) with Delay Characteristics Calculated on the Basis of Nominal Process Parameters

C_{NP} = Capacitance per unit area between N+ diffusion and P well = 0.21 pF/mil^2

C_{PN} - Capacitance per unit area between P+ diffusion and N- substrate=0.12pF/mil^2

C_{MOS} - Capacitance per unit area between gate metallization and N+ or P+ diffusions = 0.20 pF/mil^2

The first step in the characterization of the Three-Input NOR cell is presented in Figure 39. The solid lines represent the intended transistor logic, while the dashed lines represent the parasitic capacitance values. It is in the calculation of the parasitic capacitance values that the P-N junction and MOS gate capacitance per unit area values are needed.

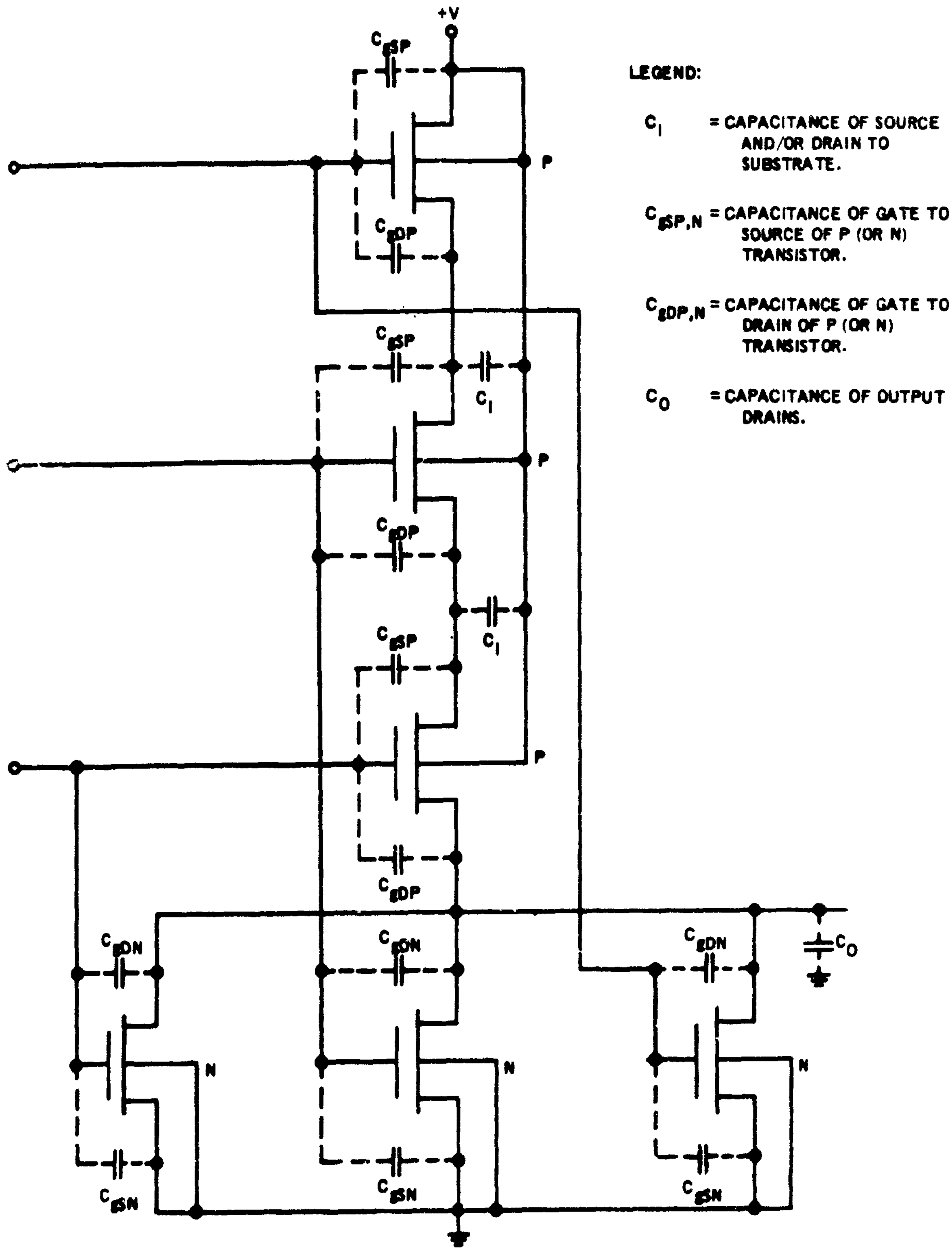

Figure 39. First Step in the Characterization of Three-Input NOR Cell

Section 7

DESIGN OF THE C-MOS STATIC SHIFT CELL

The C-MOS Static Shift cell has gone through a series of designs. In each design it is necessary to consider the topological and layout problems in addition to the circuit problems. A revision of the first circuit which allowed a compact layout (9.6 mils for the string cell) is shown in Figure 40. (See circuit description in Quarterly Report No. 1.) In this circuit the P-channel transmission devices could not transmit the logic node "zero" without attenuation at the storage node. This created the danger that the capacitive noise due to the attempted entry of data when the clock was high would partially turn on the wrong data gate. Further in this design the incoming data must overpower the previously "on" P-channel device in the holding circuit of the flip-flop, which put additional strain on design tolerances.

To avoid the problem of the imperfect transmission device, a new circuit, shown in Figure 41, was devised. A layout based on this circuit was the same size (9.6 mils for the string cell) as the previous cell. In this circuit two clock lines (clock and $\overline{\text{clock}}$) must be transmitted between the string cells, compared to only one before. However, only one data interconnection is needed between the cells where two were needed before (data and $\overline{\text{data}}$). The original philosophy of having a single cell layout with five pads along the bottom for use when needed is still preserved, and three connections along each side of the cell are available for adjacent cells when needed. The number of transistors (10) in this design is the same as that for the previous design. In this design it is still necessary to overpower the holding transistors in the flip-flop in order to enter data stored at a storage node which becomes isolated from its data source as the clock goes high. The difference is that data of either polarity is jam-transferred into the same side of the flip-flop from a single data storage node through a super-inverter

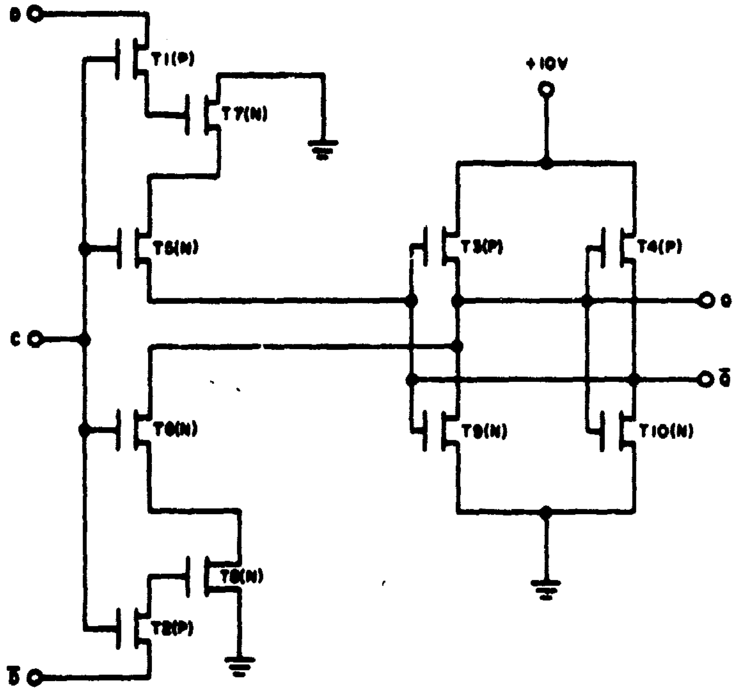

Figure 40. Circuit for Second Version of C-MOS Static Shift Register Cell

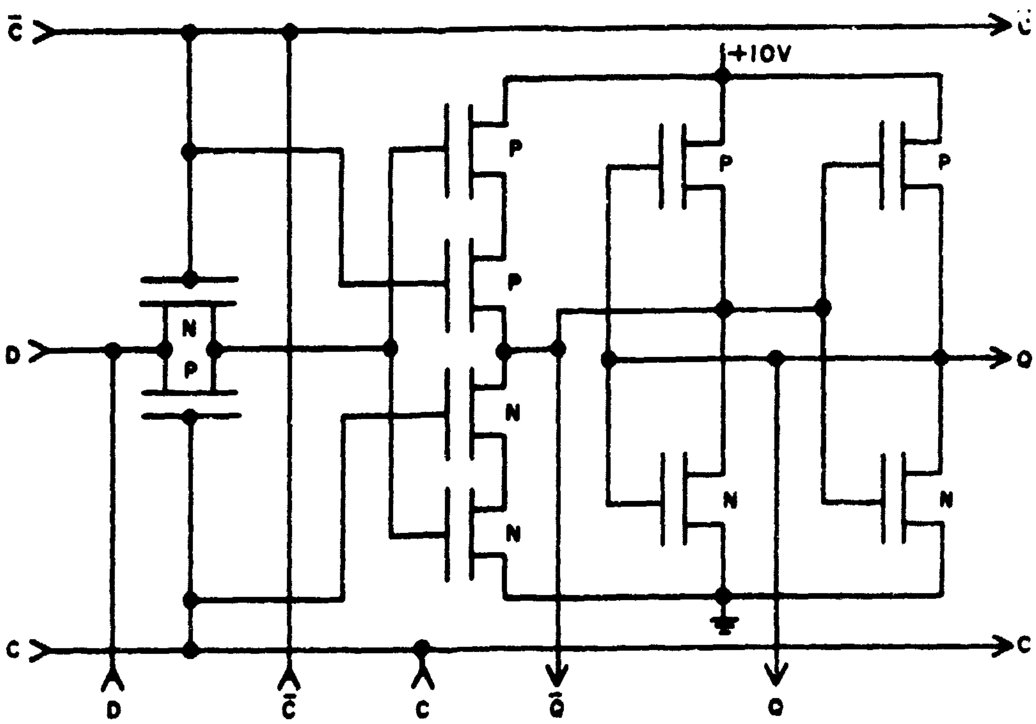

Figure 41. Circuit for Third Version of C-MOS Static Shift Register Cell

which can drive one and one-half times the output current. These two series transistors have to have three times the channel width as the output transistors. The really important difference, however, is that instead of two P-channel transmission devices on a single clock, a parallel N-channel and P-channel transmission device now works off of clock and $\overline{\text{clock}}$. This allows transmission of data of either polarity without attenuation, which yields significant improvement in the noise immunity at the storage node. The circuit, shown in Figure 42, was simulated with $\overline{Q}$ connected to D to make a triggerable flip-flop. Results of the simulation showed very good noise immunity at the storage node. However, the simulation indicated speeds not compatible with the speeds of the other C-MOS cells. This performance was associated with the fact that the inverter, which forced information into the flip-flop, can supply only one and one-half times the current of the output stage, which opposes this new data current. Therefore, the current available to charge the output capacitance is one and one-half minus one, or only one-half of the current which the output stage can supply, which is actually only three-quarters that of the basic inverter.

The design was improved significantly by adding two transistors to the configuration shown in Figure 41 to make the configuration shown in Figure 42. This opened the circuit path of the opposing output when new data was entered.

The two new series transistors in the Q output stage disconnect the regular output when the clock goes high, allowing the data entry stage, which is then activated, to enter the new data without opposition. The current driving ability and consequently the speed can now be fully compatible with the other C-MOS cells. All the other features of the old circuit are retained. The new cell layout is increased in width by only 0. 9 mil to 10. 5 mils for the string cell, a small price to pay for a three-fold speed improvement.

The simulated performance with zero clock skew of the circuit of Figure 42 connected as a binary counter is shown in Figure 43. The parameter values used in these computations are not the experimentally correlated values used in Section 6

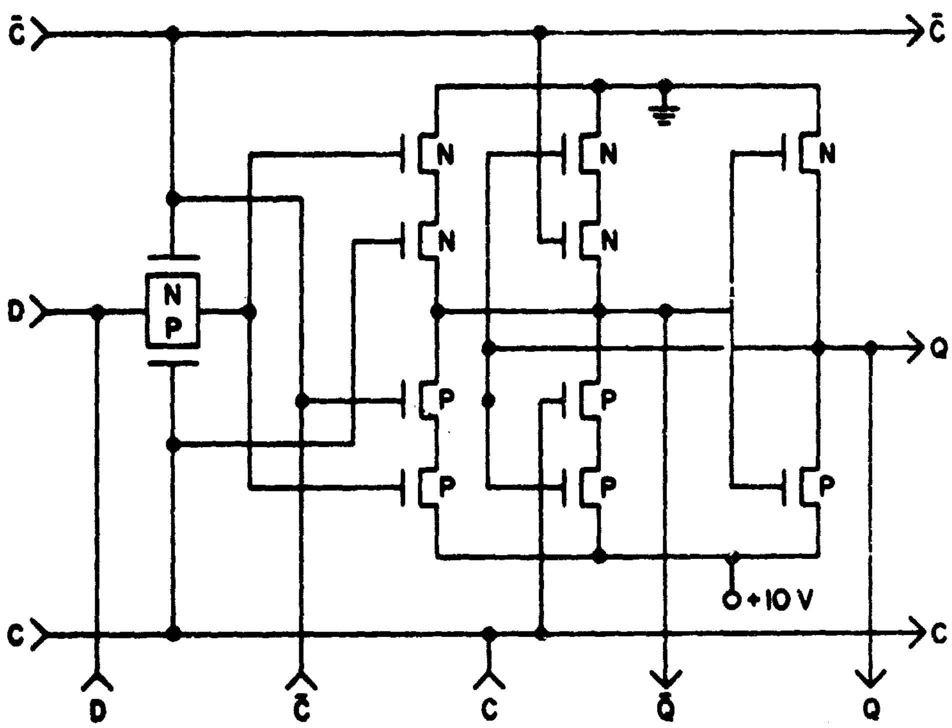

Figure 42. Circuit for Fourth Version of C-MOS Static Shift Register Cell

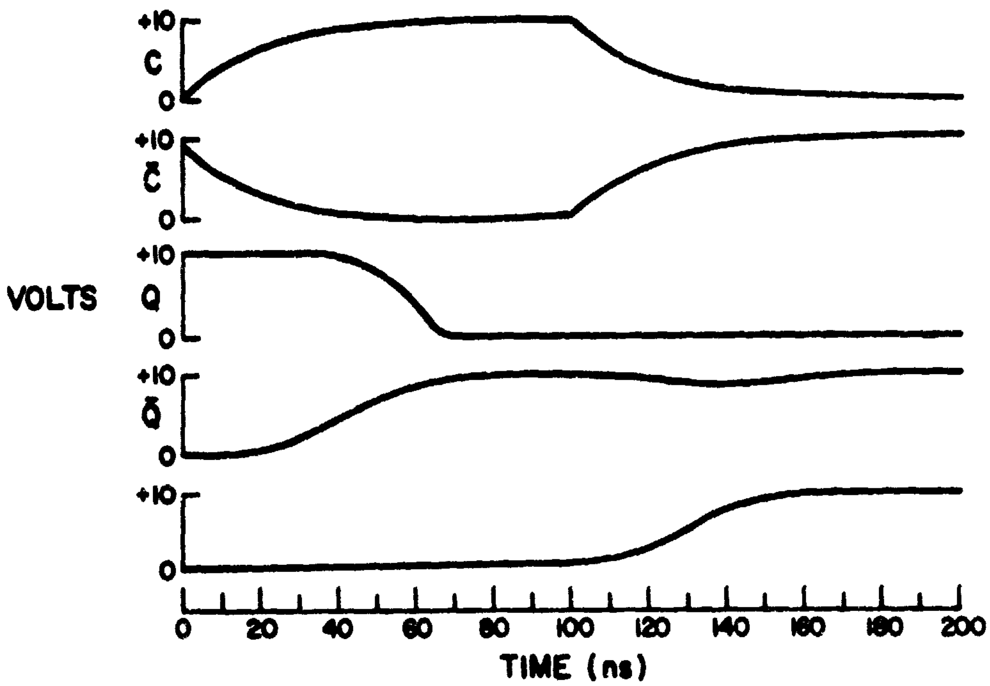

Figure 43. Simulated Performance with Zero Clock Skew of Fourth Version of Static Shift Register

since it was done at an earlier time. However, the values are not substantially different.

The performance of the register with a 40-ns clock skew is shown in Figure 44. This value was deemed the upper limit of clock skew based on results using clock skews 50 ns or higher.

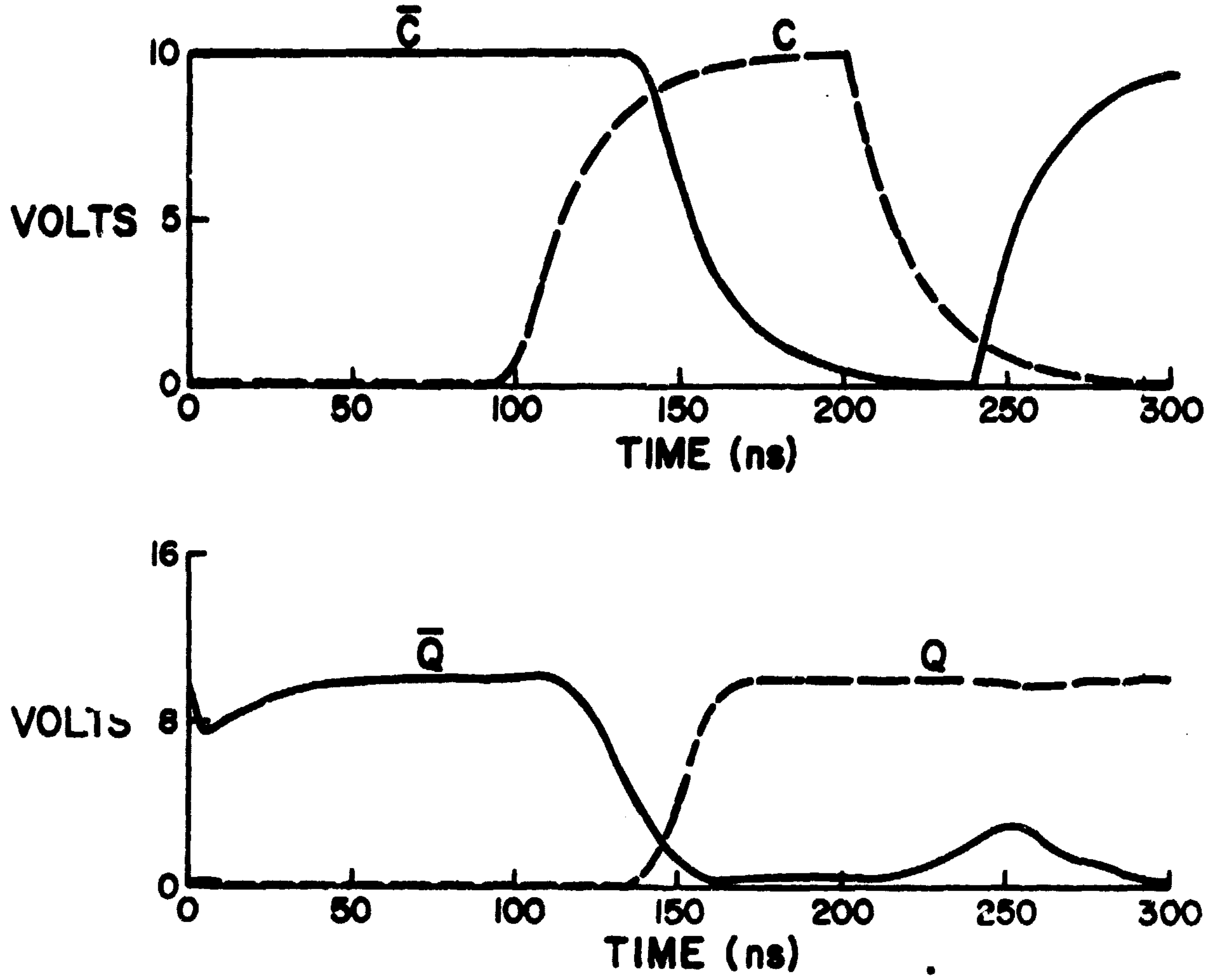

Figure 44. Performance with 40-ns Clock Skew of Fourth Version of Static Shift Register

Section 8

C-MOS STANDARD CELL ARRAY NO. 1 - NASA TEST CHIP

All of the cells and components required for the test chip have been completed. Two design reviews were performed. The logic of the test chip, the interconnections, pin allocations and definitions have been checked. The final logic contained on the test chip is shown in Figure 45.

A set of input data describing the test chip was prepared for the PRF, artwork, and CALCOMP plotting programs. A CALCOMP plot of the test chip containing the outline of all cells was generated. The original chip size was about 120 by 105 mils. With the use of the Manual Modifications program, various modifications and improvements were made. This included movement and placement of pads to provide a more uniform arrangement to facilitate bonding. In addition, tunnels were removed from certain outputs to increase the accuracy and reproducibility of parameter, performance and characterization measurements when they are made on the fabricated chip. Finally, the application of the Manual Modifications program facilitated the reduction of the chip size to approximately 100 by 95 mils.

Following evaluation of the CALCOMP plots the final 7-level mask artwork was plotted on the automatic plotter. Level 6, the metallization level, is shown in Figure 46.

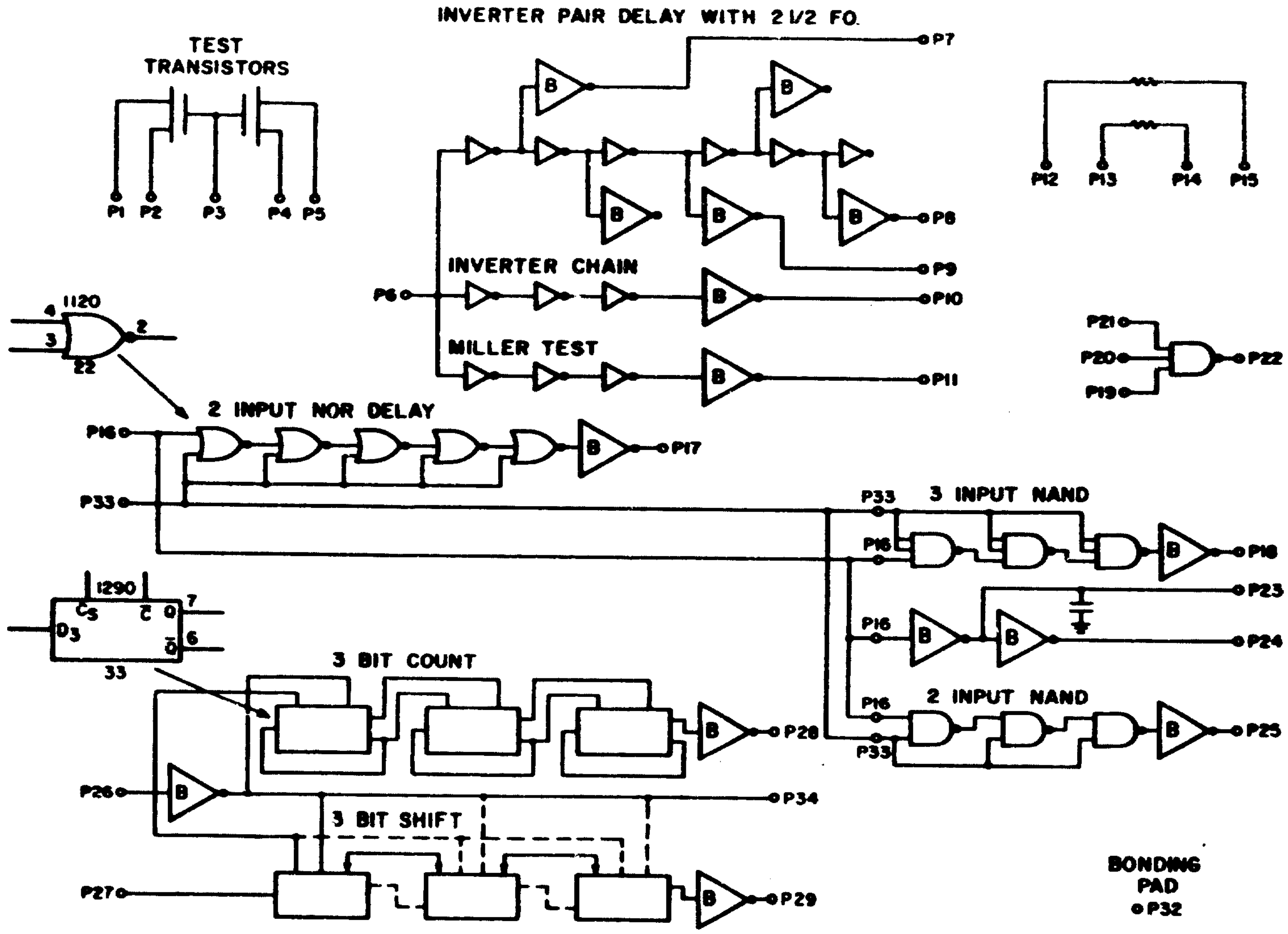

Figure 45. NASA C-MOS Test Chip, Logic Diagram

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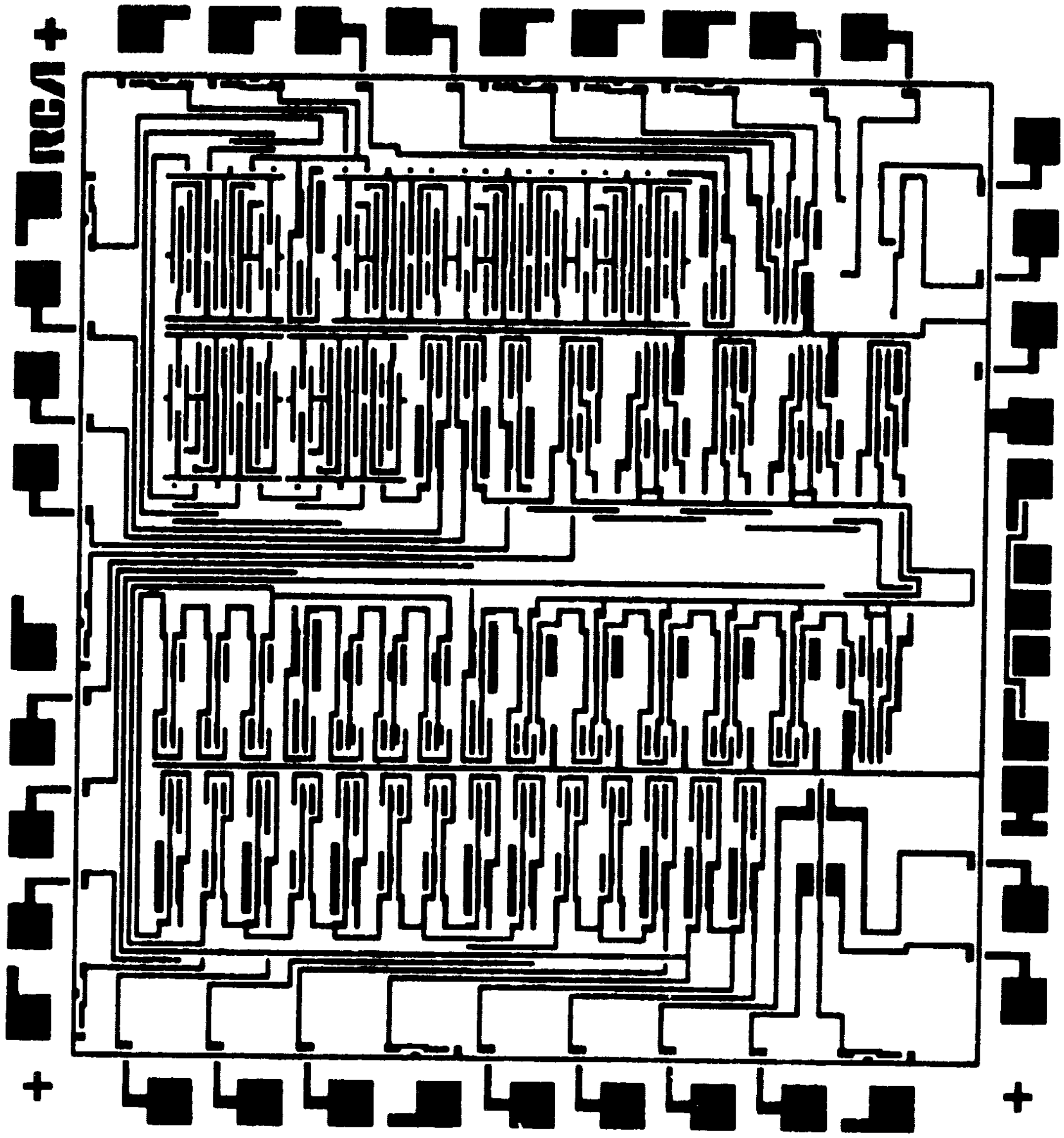

Figure 46. NASA C-MOS Standard Cell Test Chip Metallization Level Mask Artwork

Section 9

NEW TECHNOLOGY

A. C-MOS STATIC SHIFT REGISTER

A Patent Disclosure (RCA Docket No. 63,427) for the C-MOS Static Shift Register described in Section 7 of this report is now being processed by RCA.

Section 10

PROGRAM FOR NEXT REPORTING INTERVAL

The next report will be a monthly report covering the period from June 15, 1970 to July 15, 1970, the seventh month of this contract. The test chip will be run through the design automation cycle using the updated corrected tape. The working plates will be fabricated.

Cell characterization for the average propogation delay will continue.

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Section 11

CONCLUSION

All of the basic requirements to generate the mask artwork for C-MOS standard cell integrated circuit arrays have been completed.

Included among these requirements are:

1. Creation, design, and layout of the standard cell circuit complement including checking.
2. Completion and debugging of the various computer programs required in the design automation cycle.
3. Creation and definition of a C-MOS standard cell array concept.
4. Creation, definition, and design of the logic for the test chip.
5. Preliminary runs of the test chip through the Design Automation (DA) cycle using CALCOMP plots as check points.
6. Final mask artwork generation.

Examination of the final artwork suggested further improvements to increase accuracy. The test chip will, therefore, be re-run through the DA cycle.