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THE LARGE SCALE MICROELECTRONICS COMPUTER-AIDED DESIGN AND TEST (CADAT) SYSTEM

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16. ABSTRACT

This report describes a large scale microelectronic Computer Aided Design and Test system referred to as CADAT. CADAT consists of a number of computer programs written in FORTRAN that provide the capability to simulate, lay out, analyze, and create the artwork for large scale microelectronics. The function of each software component of the system is described with references to specific documentation for each software component.

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INTRODUCTION

The advent of large scale microelectronics has brought with it the virtues of reduced cost, volume, weight, and power consumption while improving reliability and performance. It has however required an adjustment in system design procedures. Formerly breadboard implementations of hardware could be utilized to work out the final changes in a design without appreciable penalty in time or cost. Large scale integrated circuits (LSIC's) permit no such luxury. A complex LSIC cannot properly be breadboarded with anything but the actual LSIC itself, and by the time the LSIC is available considerable time and money are commited to mask fabrication and wafer processing. In essence, the former breadboard phase must be replaced with a thorough computer evaluation of the LSIC design. The problem is further complicated because the system designer may be contracting for LSIC's from various manufacturers in addition to or instead of designing some of his own.

The point to be made here is that the computer aided design (CAD) requirements of the National Aeronautics and Space Administration (NASA) and its system contractors are quite different from those of an LSIC manufacturer. The manufacturer can afford to have a CAD system consisting of a layout subsystem followed by an evaluation subsystem which is locked in to the layout subsystem and to his own logic family, technology, and processing rules. Most CAD systems for LSIC's in existence today are truly design systems with little, if any, open-ended analysis capability. There is also a significant amount of LSIC design being done today with incomplete or coarse evaluation techniques being used before committing to mask fabrication and wafer processing. NASA and its system contractors, however, require an evaluation subsystem which can accommodate proposed mask designs generated by any layout method (regardless of whether it is any in-house or out-of-house method) before the commitment to mask fabrication and wafer processing is made. This realization set the tone for the development at MSFC of the Computer Aided Design and Test (CADAT) system. The purpose of MSFC's large scale microelectronics CAD effort is to provide the NASA centers and their contractors with comprehensive

software for the improvement of evaluation and design time, cost, and reliability. The embodiment of this software is the CADAT system. It has been developed such that an installation can gainfully adopt either the total system, parts of the system in a stand-alone mode, or parts of the system in a remote mode cooperating with a total system elsewhere. Figure 1 describes the capabilities that exist within the CADAT system.

OBJECTIVES

The following paragraphs present some objectives of the CADAT system and how they are met.

Pragmatic Implementation

The CADAT software must be compatible with many differing computing hardware configurations. System designers at NASA or contractor installations simply are not in control of their computational facilities; therefore, attempts at optimal technical solutions which involve common hardware or a common time sharing service are difficult to implement. (MSFC is attempting a common hardware approach wherein all programs, whether large batch or interactive graphics, would be run on common autonomous hardware systems costing less than $150K, while another government agency is trying the time-share approach.) The present CADAT software has therefore been segmented into large batch software to be run at an installation's computer center and interactive software to be run on a mini-computer or local time-share service. If necessary the total CADAT system functions can be accomplished without the benefit of the interactive software.

In addition, as previously mentioned, parts of the system can be used in the stand-alone mode to accomplish singular functions. Also excellent functional segmentation of the system exists such that part of the functions can be achieved at one installation and the remainder at another installation.

Evaluation of Designs Derived from any Layout Method

The CADAT evaluation subsystem is compatible with all manual, computer assisted, and computer automatic layout methods. This is achieved by the extreme functional separation of the layout and evaluation subsystems. The layout

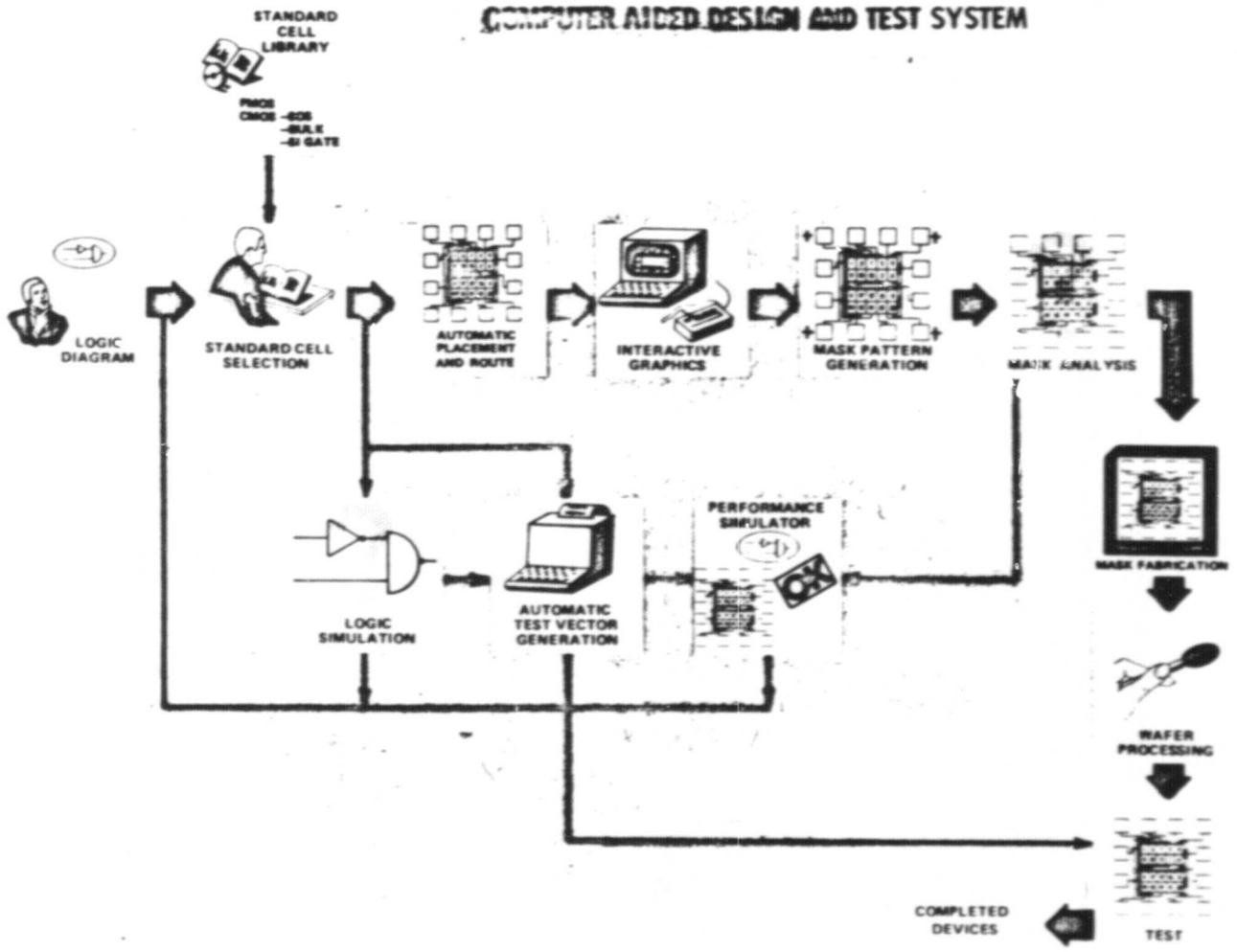

Figure 1. Computer Aided Design and Test (CADAT) system flowchart.

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subsystem simply provides mask geometry to the evaluation subsystem. This means that the CADAT system is flexible enough to permit the dropping of the complete layout subsystem and the substitution of another layout subsystem, e.g., draftsmen, computer assisted drafting, or different automatic layout programs.

Ease of Update for New Technologies

The functional segmentation of the software makes this objective reasonable. Strict logic programs require no update in response to technology changes. Layout programs require only minor changes. The artwork evaluation programs as such require no change. The geometric operations of these programs are modularized such that a separate control sequence can be used for each technology to achieve the desired results.

Ease of Update with More Powerful Programs

Once again the functional segmentation allows any particular area to be further developed or replaced with something better without upsetting program interactions within the CADAT system.

Compatibility with Multiple Technologies and Multiple Process Rules Within the Technologies

The CADAT system is compatible with N-metal oxide semiconductor (N-MOS), P-metal oxide semiconductor (P-MOS), and C-metal oxide semiconductor (C-MOS) technologies, bulk metal gate and silicon on sapphire (SOS) silicon gate. The process rules within a technology are simply input parameters to the system.

Ease of Use

One of the problems between design engineers and evaluation software has been the extensive data preparation required to operate the programs. The CADAT system allows the engineer to define a design once to the system in a reasonable format and then the system will reformat the data for other programs and handle program-output program-input interfaces.

Another problem has been in the area of simulators. Even if a design is entered into a simulator, the engineer is still required to decide and input the stimuli for the simulator to operate. The CADAT system however makes extensive use of test pattern generation (TPG) software to alleviate this problem. TPG can automatically create stimuli to exercise all the gates of a design. This stimulus applied to a simulator will provide most of the timing and operation data that the engineer requires.

Capabilities in the LSIC and Hybrid Areas

The CADAT system contains an automatic hybrid layout program and hybrid layout editing programs in addition to its LSIC programs. Also the capacity of the TPG and simulation programs is sufficient to handle the multiple LSIC's on a hybrid substrate. Additionally a fault isolation program is available within CADAT to assist in hybrid debug and repair.

DISCUSSION

The implementation of the CADAT system consisted first of the segmentation of the software into three subsystems: layout subsystem (LAYOUT), evaluation subsystem (EVAL), and design intent subsystem (LOGIC). As previously mentioned, LSIC evaluation is similar to breadboard testing and LSIC layout is similar to breadboard design. The input to breadboard test is breadboard hardware; the input to LSIC evaluation is mask geometries. In either case, stimuli and expected results must also be supplied to test or evaluate. This is the function of LOGIC. This function could be accomplished manually, but it is easier to simply define the intended logic to LOGIC and let it work out stimuli and expected performance data. LOGIC therefore provides the documentation and preparation of evaluation specifications. If all parties concerned cannot agree on these specifications, then this is the point to stop before the investment of time and effort in computer layout and evaluation when designing, or in computer evaluation alone when checking someone else's layout.

LOGIC is an excellent choice to be run at a location remote from a complete CADAT system especially for design purposes. It permits the remote designer to implement and check design intent in several configurations with good turnaround time for each iteration before proceeding on to LAYOUT and EVAL. Thus, remote designers can participate effectively in the use of the CADAT system by exercising LOGIC. LOGIC consists, in part, of a preprocessor

(NTRAN) [1], a postprocessor (TPGITF) [2], and a logic simulator (LOGSIM) [3,4,5]. NTRAN accepts data in a single, easy to use cell net format (identical to that used as input to the LSIC automatic layout programs) and provides circuit model data for TPG [5,6] and LOGSIM. When a problem involves multiple LSIC's, the MACROCELL preprocessor accepts data in chip net form (identical to that used by the printed circuit layout program) and outputs in the aforementioned cell net form.

The TPG postprocessor (TPGITF) will automatically supply stimuli to the LOGSIM simulator of LOGIC plus stimuli for EVAL. LOGSIM will output the expected performance of the intended design to the EVAL for perusal by the designer (Fig. 2).

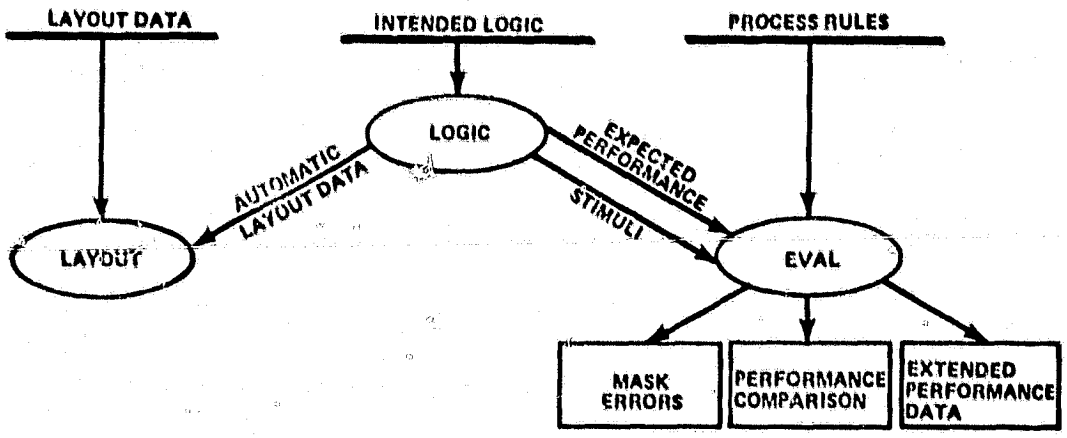

Figure 2. Performance evaluation flowchart.

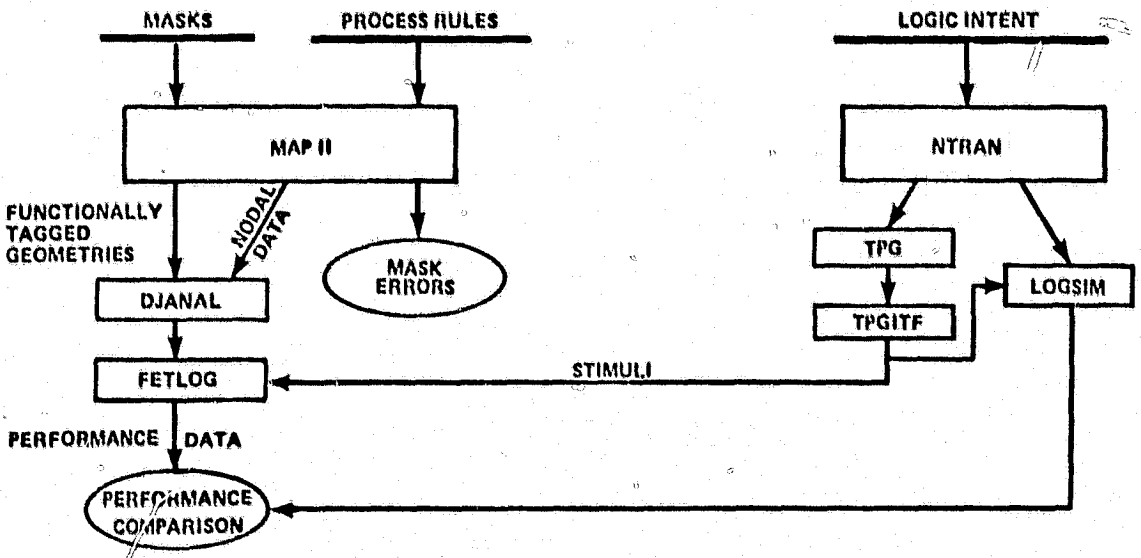

Figure 2. (Concluded)

EVAL requires, as input mask geometries (from either LAYOUT or any other source), process rules from the user, and stimuli and expected performance data from either LOGIC or the user. At this point masks, process rules, stimuli, and performance data are ready to be input to EVAL. The first program of EVAL is the Mask Analysis Program (MAP II) [5,7] which looks at the geometric blocks on all masks levels and determines where transistors, feedthroughs, conductors, guard bands, etc., exist. It may take complex geometries apart or gather simple geometries together to redescribe the same mask picture in terms of geometries tagged with their functions. These tagged geometries together with a definition of the process rules are checked for errors by MAP II. The location and nature of mask errors will be output by this program in graphic and line printer format. The MAP II program has the additional feature of describing the circuitry on the masks in nodal format. This nodal data together with the functionally tagged geometries are passed along to the Disjunct Analyzer (DJANAL) program [8]. Here the equations of operation are synthesized and the device performance data prepared for a simulator (FETLOG)[1] [3,4,5,9]. The FETLOG simulator combines the features of a transient analyzer (FETSIM) [9,10] with those of a logic simulator (LOGSIM) and is thus quite accurate. The previously prepared stimuli are now input to FETLOG simulator, and the simulated chip performance data are compared with the intended performance data.

EVAL can also supply extended performance data to provide further insights into chip performance. As the FETLOG simulator is generating data in response to the previously mentioned stimuli, it is also defining an accurate logic model for the chip. This logic model, which will be more complex than the intended logic model, is then available to provide performance data that can then be inspected for problems.

LAYOUT has been played down to emphasize the lack of dependence of the rest of the CADAT system upon it; however, LAYOUT is very powerful even as a stand-alone system. It contains automatic layout programs for hybrid and even printed circuit board layout (PWB) [11,12]; an automatic placement, route, and fold program for P-MOS and C-MOS (PRF) [13-17]; and an automatic two-dimensional placement and route program for C-MOS and C-MOS silicon gate SOS (PR2D) [15,18], plus a two dimensional program using multiport cells (MP2D) [19]. It also contains batch load programs for layout digitization and editing (MADP) [20], and a program to quickly check PRF automatic layouts for errors (CHECK) [21]. Lastly it contains a highly developed interactive graphics program (AIDS II) [5,22-25]. This program contains, but is not

1. A FETLOG users manual is in preparation and will be published at a later date.

limited to, an excellent computer assisted drafting tool similar to commercially available systems. However, it goes beyond these systems in that it will accept as input error masks from MAP II, will input and output Mann Pattern Generator tapes and, most importantly, high level art tapes. It can then graphically edit and produce updated tapes.

An example of a special operation is placing a metalization run to interconnect two widely spaced cells. If the viewing area is scaled to provide a display of both cells simultaneously, it is very difficult to position the interconnect with sufficient accuracy to realize a good connection. The new features alleviate this problem by allowing view window changes while the designer is in the process of placing the line that represents the connection. He can zoom in on the first cell and establish the begin point of the line, zoom in on the second cell, issue a command reset, and then establish the end point of the line.

By separating a portion of the design into another file, the AIDS software can locate, display, modify, delete, or otherwise manipulate elements at a faster rate than is possible for the entire file. The advantage of this feature is obvious if one considers a situation in which an isolated portion of a design requires extensive modification while the remainder is essentially correct. The LSI designer is able to extract the portion of the design requiring extensive modifications, operate on it at a rapid rate, and then recombine it with the remainder of the design, thereby greatly enhancing the effectiveness of interactive operations.

The tagged point feature is provided in conjunction with the file splitting operation to ensure that the relationship between the two files remains intact while they are separated. An example of the utility of tagged points is a situation in which a wiring channel must be opened up to permit additional interconnects to be made. The designer would fence the area to be moved, activate the fenced file, and bias the file by the amount required to enlarge the channel. If the move is unilateral (i.e., in the X-direction only or the Y-direction only), it is unlikely that manipulation of tagged point elements will be required. The elements that bridge the fenced area will effectively be stretched and maintain the topological integrity of the design. If, however, a bilateral bias is applied, the bridging elements will become distorted and will very likely require modification. The swap command is employed to accomplish the modifications in such a manner that the topological integrity in this case may be also retained.

SUMMARY

Source programs within CADAT were developed by RCA, Macrodata, GE, and the Navy. These programs were integrated, debugged, modified and documented by M&S Computing, Inc. In addition, in response to problem definition by MSFC, M&S has created preprocessors, post processors, new programs and has extensively designed and developed the interactive graphics system. MSFC has directed these efforts in addition to designing some of the auxiliary programs.

The future of CADAT entails the improvements of component program power, the adoption of a higher level logic language to permit easy specification of a total design followed by automatic partitioning to hybrid and LSIC level, plus automatic logic design on the LSIC. In the more distant future automatic package design to defined formats should be incorporated.

CADAT SYSTEM

The CADAT system is shown in Figure 3 and the function of each software component is described as follows:

1) LOGIC Subsystem:

a) NTRAN [1] — Network TRANslator — converts cell net data (as used by the LSIC automatic layout programs) to NAND gate models for TPG and gate models for LOGSIM.

b) TPG [6] — Test Pattern Generator — an adaptation of the LASAR program which generates stimuli to test for (stuck at faults) in combinatorial and sequential logic.

c) TPGITF [2] — Test Pattern Generator Interface — converts TPG output to format compatible with stimulus inputs to LOGSIM and FETLOG.

d) LOGSIM [3,4,5] — LOGic SIMulator — simulates the logic and timing performance of logic gates. A three valued simulator with separate timing specifications available on each gate input and a special feature to simulate the bus or node disconnect aspects of C-MOS logic.

e) MACROCELL — converts chip net data (as used by PWB) to NTRAN. Permits the definition of multifunction cells.

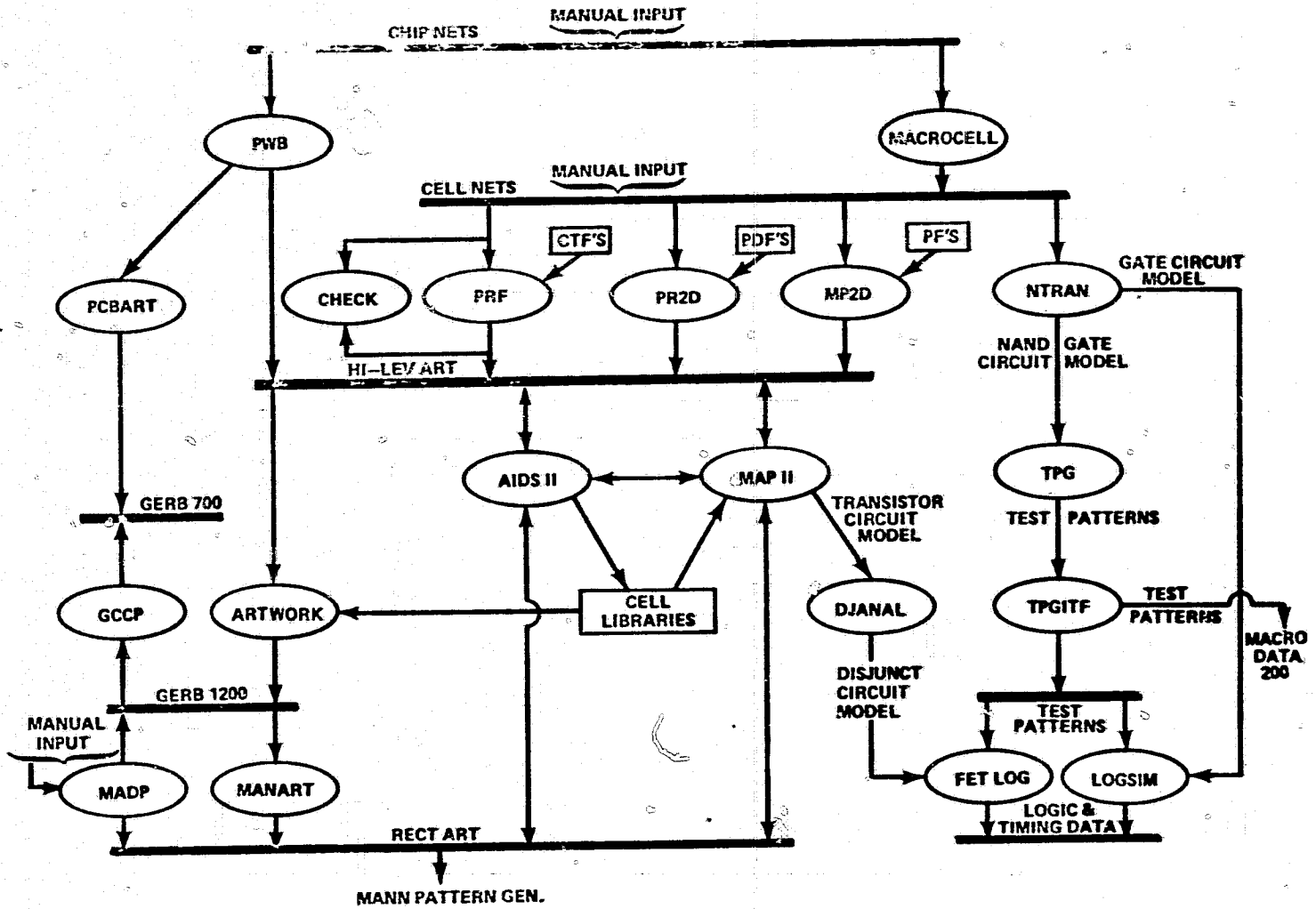

Figure 3. The Computer Aided Design and Test (CADAT) system software components.

2) EVAL Subsystem:

a) MAP II [5,7] — Mask Analysis Program II — an updated version of the original MAP which performs design rule checking and circuit synthesis. It can correspond (in and out) in high level art or rectangular art format as well as interface with AIDS II [5,22-24] for error mask display. It accepts data directly from an ARTWORK cell library in conjunction with the high level art capability. It provides transistor circuit model including capacitances to the DJANAL post processor.

b) DJANAL [8] — Disjunction ANALyzer — groups transistor circuits into disjunct circuits for use by FETLOG.

c) FETLOG [3,4,5,9] — Field Effect Transistor Simulator LOGic Simulator — a combination of the FETSIM transient analysis program with the LOGSIM logic simulator to provide a simulation which is slower, but more accurate, than LOGSIM and less accurate, but much faster and handles many more nodes, than FETSIM.

3) LAYOUT Subsystem:

a) PRF [13-17] — Placement Route and Fold — automatic layout used for P-MOS single ended cells.

b) MGCTF [13,14] — Metal Gate Circuit Type File — a data base for PRF providing pin placements of a family of C-MOS metal gate bulk silicon standard cells.

c) CHECK [21] — a program which provides a coarse but rapid check of the correlation between the networks input to PRF and the high level art defined by PRF.

d) PR2D [15,18,27] — Placement Route in Two Dimensions — automatic layout which is more efficient than PRF. Used for C-MOS metal gate bulk and C-MOS SOS silicon gate.

e) MGPDF — Metal Gate Pin Data File — A data base for PR2D providing pin placements of a family of C-MOS gate bulk silicon standard cells.

f) SOSPDF — Silicon on Sapphire Pin Data File — a data base for PR2D providing pin placements of a family of high speed, 7 mil high, C-MOS SOS silicon gate standard cells.

g) MP2D [19] — Multi Port in Two Dimensions — automatic layout which is more efficient than PR2D for C-MOS SOS double entry cells.

h) SOSPF — SOS Pin File — a data base for MP2D providing pin placements of a family of high density, 5 mil high, C-MOS SOS standard cells. SOSPF is not available at this time.

i) PWB [11, 12] — Printed Wiring Board — automatic layout for printed circuit boards or hybrid substrates. Output in high level art format.

j) PCBART — Printed Circuit Board ARTworks — a postprocessor for PWB which produces output in Gerber 700 plotter format.

k) ARTWORK [28, 29] — converts high level art to Gerber 1200 plotter format.

l) MANART [30, 31] — MANn pattern generator ARTwork — used in conjunction with artwork to produce rectangular art for the MANN pattern Generator.

m) GCCP [29] — converts Gerber 1200 format to Gerber 700 format.

n) MADP [20] — Mask and Pattern Display — a batch program for manually digitizing layouts when an interactive graphics system is not available. Produces check-plots in Gerber 1200 format and rectangular artwork in MANN Pattern Generator format.

o) MGBLIB [15, 16, 17] — Metal Gate Bulk LIBrary — a data base for the ARTWORK program of a family of C-MOS metal gate bulk silicon standard cells.

p) SOSLIB [18, 26, 32, 33] — SOS LIBrary — a data base for the ARTWORK program of a family of high speed C-MOS SOS silicon gate standard cells.

q) AIDSII [5, 22-25] — Artwork Interactive Design System II — includes an update of the original AIDS interactive graphics program plus the following supporting programs:

1. DSPLIB [22] — DISPlay LIBrarian — preformats application oriented displays.

2. DSPCTL [22] — DISP Controller — coordinates communications between user and AIDS application program.

3. PRFAID [24] — Converts high level art to AIDS data base.

4. AIDPRF [24] — Converts AIDS data base to high level art.

5. CTMN [25] — Converts AIDS data base to rectangular art.

6. MNTC [25] — Converts rectangular art to AIDS data base.

7. CPAT [25] — Converts AIDS cell library to ARTWORK cell library.

4) Associated Stand Alone Programs:

a) FETSIM [9,10] — Field Effect Transistor SIMulator — used for rigorous analysis of cell designs and critical paths through chips. Requires manual input.

b) SIMLOG [34,35] — SIMulate LOGic — a program to define input patterns which will cause certain output patterns to occur in combinatorial and sequential logic.

c) PARTLO — PARTition and Linear Order — a BASIC program to partition large groups of small cells into small groups of large cells by a clustering technique.

Output is displayed in an optimum linear placement of the original cells following the clustering order.

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APPROVAL

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By John M. Gould

The information in this report has been reviewed for technical content. Review of any information concerning Department of Defense or nuclear energy activities or programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

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Director, Electronics and Control Laboratory

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