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# DEVELOPMENT OF BOOLEAN CALCULUS AND ITS APPLICATIONS

FINAL REPORT
NASA GRANT NO. NSG 1436

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# AND

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# FINAL REPORT

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## 1. INTRODUCTION

The report describes the significant results obtained during the NASA GRANT NSG No 1436 period from August 1977 through December 31, 1980. The primary objective of the grant has been to develop Boolean Calculus so that it can be advantageously applied to developing new digital system design methodologies that would be desirable additions to existent methodologies in terms of reducing system complexity , size, cost, speed, power requirements, etc. New synthesis procedures were developed during the tenure of the grant with the above mentioned objectives in mind. These will be described in the following sections. Several publications that resulted from research efforts will be shown in a later section.

## 2. FORMALIZATION OF BOOLEAN CALCULUS:

Formalization of the existent and new concepts and relationships in the area of the Boolean Integral Calculus are given in Appendix I.

## 3. NEW SYNTHESIS TECHNIQUES:

Boolean Calculus has made it possible to synthesize fundamental-mode asynchronous sequential system using clock-triggered flipflops. It has been shown that synthesis techniques that utilize edge-sensitiveness property of flipflops require fewer flipflops and logic gates than conventional techniques do for many systems [11]. In order to describe the new synthesis technique, we need the following definitions:

Definition 2.1: Given a Fundamental Mode Asynchronous(FMA) system, FMAS = (I,S,O,f,g) where

$I$ = set of p distinct input conditions = $\{I_j\}$

$S$ = set of q states of the system = $\{S_j\}$

$O$ = set of outputs = $\{O_j\}$

$f$ = output function

= $f(S_k, I_j)$, $\forall_j$ and k

$g = g(S_k, I_j)$, $\forall j$ and k

= next state function,

we will need to tranform it to a <u>Differential Mode System</u>, DMS as defined below:

DMS = $(I', I^{*\prime}, S', O', f', g')$

where $I' = I$, $S' = S$

$I^{*\prime} = \{(I_j, I_k) \mid \forall_{j,k}\}$

$O' = O$

$f'$ = output function of DMS

$g'$ = next state function of DMS

$= g'(S_h, I_j, I_k)$

$$
= \begin{cases}
S_i, & \text{if } g(S_h, I_j) = S_h,\ g(S_h, I_k) = S_i \\
& \quad \text{and } g(S_i, I_k) = S_i \\
S_i, & \text{if } g(S_h, I_j) = S_h \text{ and there exist } S_{i1}, S_{i2}, ---, S_{in} \ \& \ S_i \\
& \quad \text{such that } g(S_h, I_k) = S_{i1}, \\
& \quad g(S_{i1}, I_k) = S_{i2}, ---, g(S_{in}, I_k) = S_i \\
& \quad \text{and } g(S_i, I_k) = S_i. \\
—, & \text{if } g(S_h, I_j) = S_h \ \& \ g(S_h, I_k) = — \\
—, & \text{if } g(S_h, I_j) = S_h \text{ and there exist} \\
& \quad S_{i1}, S_{i2}, ---, S_{in} \text{ such that} \\
& \quad g(S_h, I_k) = S_{i1},\ g(S_{i1}, I_k) = S_{i2}, \\
& \quad g(S_{i2}, I_k) = S_{i3}, ---,\ g(S_{in}, I_n) = — \\
—, & \text{if } g(S_h, I_j) \neq S_h
\end{cases}
$$

$f'(S_h, I_j, I_k)$

$$
= \begin{cases}
f(S_i, I_k), & \text{if } g'(S_h, I_j, I_k) = S_i \\
—, & \text{if } g'(S_h, I_j, I_k) \text{ is unspecified}
\end{cases}
$$

It will be assumed that only one input variable can change at a time.

In order to facilitate understanding of DMS construction, an example will be presented.

| | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| A | A,1 | C,— | A, 0 | C, — |
| B | B,0 | D,— | B, 1 | D, — |
| C | B,— | C,1 | B,— | C,0 |
| D | A,— | D,0 | A,— | D,1 |

Figure 1 (FMA System)

Figure 1 describes an FMA system.

| $x_1x_2$ | 00<br>10 | 00<br>01 | 01<br>11 | 01<br>00 | 10<br>00 | 10<br>11 | 11<br>01 | 11<br>10 |
|---|---|---|---|---|---|---|---|---|
| A | C,0 | C,1 | --- | --- | --- | --- | C,1 | C,0 |
| B | D,1 | D,0 | --- | --- | --- | --- | D,0 | D,1 |
| C | --- | --- | B,1 | B,0 | B,0 | B,1 | --- | --- |
| D | --- | --- | A,0 | A,1 | A,1 | A,0 | --- | --- |

Figure 2 (DM System)

Figure 2 describes a DMS system that has been transformed from the FMA system in Figure 1.

Observe that the FMA system table in Figure 1 is in its reduced form.

It can be shown that the method of state reduction normally used for reducing an FMA table can be applied to the next-state and output table for a DMS system. If such a reduction is carried out in case of Figure 2, one gets the reduced DM system in Figure 3.

| $x_1x_2$ | 00 10 | 00 01 | 01 11 | 01 00 | 10 00 | 10 11 | 11 01 | 11 10 |
|---|---|---|---|---|---|---|---|---|
| (A,C) A | A,0 | A,1 | B,1 | B,0 | B,0 | B,1 | A,1 | A,0 |
| (B,D) B | B,1 | E,0 | A,0 | A,1 | A,1 | A,0 | B,0 | B,1 |

Figure 3 (Reduced DM table)

The next step in the synthesis procedure is to assign state assignments to the states in the system. While doing so, we must ensure that the assignment is such that it allows only one state variable to change during state transition. If the state diagram corresponding to the DM table is not amenable to single-variable-change assignment, we will need to increase the number of states by adding equivalent states in order to accomplish single-variable-change assignment. This problem will be referred to again in the report later. Of course, even in the case of traditional techniques for synthesizing FMA systems, the same technique must be resorted to in order to achieve single-variable-change state assignment.

In order to get a feeling for the problems associated with synthesizing an asynchronous sequential system using clock-triggered flipflops, we will present a complete synthesis example given below:

| $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| A | A, 1 | B, — | D, — | B, — |
| B | A, 1 | B, 1 | C, — | B, 1 |
| C | C, 0 | B, — | C, 1 | D, — |
| D | C, — | A, — | D, 0 | D, 0 |

Figure 4

| $x_1x_2$ | 00<br>10 | 00<br>01 | 01<br>11 | 01<br>00 | 11<br>01 | 11<br>10 | 10<br>00 | 10<br>11 |
|---|---|---|---|---|---|---|---|---|
| A | B, 1 | B, 1 | --- | --- | --- | --- | --- | --- |
| B | --- | --- | C, 1 | A, 1 | --- | --- | A, 1 | C, 1 |
| C | D, 0 | B, 1 | --- | --- | --- | --- | --- | --- |
| D | --- | --- | --- | --- | A | D | C | D |

Figure 5

The system in Figure 4 is an FMA system which is to be synthesized using clock-triggered flipflops. The transformation of the system into DM system is given in Figure 5.

When the table in Figure 5 is reduced, we get the reduced DM system in Figure 6. Observe that the FMA system in Figure 5 is in its reduced form.

| | $x_1x_2$ 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|
| (A,B) A | A, 1 | A, 1 | C, 1 | A, 1 | --- | --- | A, 1 | C, 1 |
| (C,D) C | C,0 | A, 1 | --- | --- | A,— | C,— | C, — | C, — |

Figure 6

Let y = 0 represent A and y = 1 represent C. The excitation table for the DM system is given in Figure 7.

| y | $x_1x_2$ 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | - | - | 0 | 1 |
| 1 | 1 | 0 | - | - | 0 | 1 | 1 | 1 |

Figure 7

Observe that in the first row y changes when $x_1$ changes to 1 with $x_2 = 1$ and when $x_2$ changes to 1 with $x_1 = 1$. In the second row y changes when $x_2$ changes to 1 with $x_1 = 0$ and when $x_1$ changes to 0 with $x_2 = 1$. Hence the clock function should go through positive changes when any of these changes occur. Hence we can write down the differential expression for the clock function as follows:

$$dc = \bar{y}(x_2dx_1 + x_1dx_2) + y(\bar{x}_1dx_2 + x_2d\bar{x}_1)$$

Observe that

$$\int_1 dc = \bar{y}(x_1x_2) + y(\bar{x}_1x_2)$$

$$\int_0 dc = \bar{y}(\bar{x}_1x_2 + x_1\bar{x}_2) + y(\bar{x}_1\bar{x}_2 + x_1x_2)$$

Hence $\int_1 dc \cdot \int_0 dc = 0$ and dc is compatibly integrable.

$f_1 dc = \bar{y}(x_1x_2) + y(\bar{x}_1x_2)$ is a possible soulution. Let us, therefore try,

$$C = \bar{y}(x_1x_2) + y(\bar{x}_1x_2)$$

$$\frac{\partial C}{\partial x_1} = \bar{y}x_2 \quad , \quad \frac{\partial C}{\partial \bar{x}_1} = yx_2$$

$$\frac{\partial C}{\partial x_2} = \bar{y}(x_1) + y(\bar{x}_1), \quad \frac{\partial C}{\partial \bar{x}_2} = 0$$

$$\frac{\partial C}{\partial y} = (\bar{x}_1x_2) \quad , \quad \frac{\partial C}{\partial \bar{y}} = x_1x_2$$

Observe that as far as $x_1$ and $x_2$ are concerned, no undesired transitions are caused by them. Since $\frac{\partial C}{\partial y}$ and $\frac{\partial C}{\partial \bar{y}}$ are non-zero, we must make sure that when y changes, it does not cause undesired transitions. $\frac{\partial C}{\partial \bar{y}} = x_1x_2$. Hence when $x_1x_2 = 1$ and y changes from 1 to 0, it will cause a positive change in the value of C. Looking at the excitation table in Figure 7, we see that when input $x_1x_2$ changes to 11 (from 01 or 10), y changes from 0 to 1 rather than from 1 to 0. Hence this undesired transition cannot occur.

Consider next $\frac{\partial C}{\partial y} = \bar{x}_1x_2$. When $x_1x_2 = 1$ and y changes from 0 to 1, C will go through a positive transition. When $x_1x_2$ changes from 00 or 11 to 01, y changes from 1 to 0, rather than from 1 to 0. Hence, no undesired transition is caused by change in y when $x_1x_2$ changes from 00 or 11 to 01.

Hence we have no ripple and $C=\bar{y}(x_1x_2) + y(\bar{x}_1x_2)$ realizes the system. It can be shown that $z=\bar{y}+x_2$.

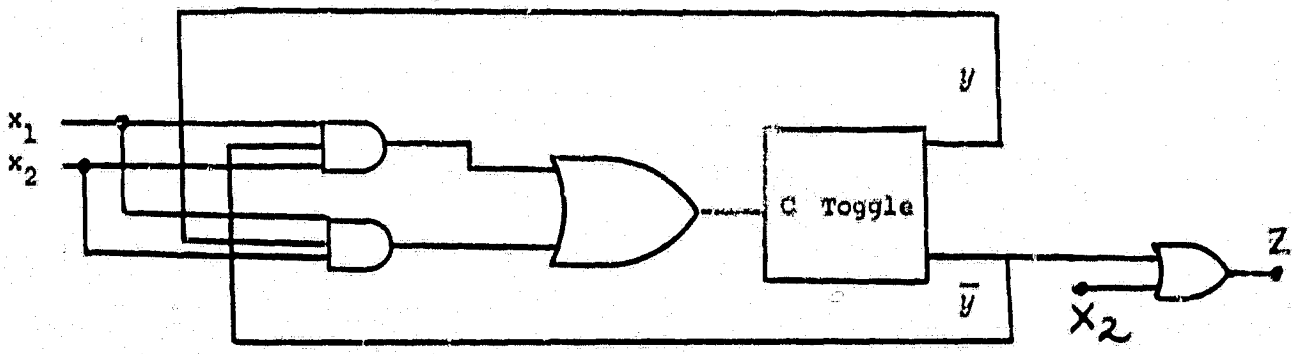



Figure 8

A toggle flipflop is used, since y changes whenever clock transition occurs.

Observe that $\bar{x}_1 x_2 \Delta y$ and $x_1 x_2 \nabla y$ are transitions that cannot occur.

## 4. DEFINITIONS

The following definitions will be needed to describe the results of the research:

Definition 4.1: $m_j(\underline{x} - x_i)$ denotes the product term obtained by deleting the variable $x_i$ from the jth minterm of variables $x_1, x_2, \ldots\ldots, x_n$.

Definition 4.2: $m_j(\underline{x} - x_i)\Delta x_i$ denotes the positive transition when $m_j(\underline{x} - x_i) = 1$ and $x_i$ changes from 0 to 1.

Definition 4.3: $m_j(\underline{x} - x_i)\nabla x_i$ denotes the negative transition when $m_j(\underline{x} - x_i) = 1$ and x changes from 1 to 0.

Definition 4.4: $TP(C_j)$ denotes set of all possible positive transitions of $C_j$ where $C_j$ is a function of $\underline{x}$ and $\underline{y}$.

The meanings of notations such as $m_j(\underline{x}, \underline{y} - y_i)$, $m_j(\underline{x}, \underline{y} - y_i)\ \nabla y_i$, etc., easily follow from the above definitions and will, therefore, not be defined.

<u>Definition 4.5</u>: A differential expression of the form

$$dF = m_0(\underline{y}) \sum_{i=1}^{n} (\alpha_{0i}dx_i + \beta_{0i}d\overline{x}_i)$$

$$+ \quad m_1(\underline{y}) \sum_{i=1}^{n} (\alpha_{1i}dx_i + \beta_{1i}d\overline{x}_i)$$

$$+\ldots+ \quad m_p(\underline{y}) \sum_{i=1}^{n} (\alpha_{pi}dx_i + \beta_{pi}d\overline{x}_i)$$

where $p = 2^m-1$

is said to be <u>exactly integrable with respect to variables</u> <u>$x_1,x_2,\ldots,x_n$</u> if there exists a function $G(\underline{x},\underline{y})$, such that

$$\frac{\partial G}{\partial x_i} = m_0(\underline{y})\alpha_{0i} + m_1(\underline{y})\alpha_{1i} +\ldots+m_p(\underline{y})\alpha_{pi}, \quad \&$$

$$\frac{\partial G}{\partial \overline{x}_i} = m_0(\underline{y})\beta_{0i} + m_1(\underline{y})\beta_{1i} +\ldots+m_p(\underline{y})\beta_{pi}, \quad \forall_i.$$

If a function G satisfying the above equations does exist, then G is called the <u>exact integral of dF with respect to</u> <u>$x_1x_2,\ldots,x_n$</u>.

<u>Defintion 4.6</u>: $I_k$ represents the binary vector $(b_1,b_2,\ldots,b_n)$ such that $b_i$'s are 0's or 1's and k is the numerical value of $(b_1b_2\ldots b_n)$, when the latter is interpreted as a binary number.

Observe that $m_k(\underline{x})\Big|_{\underline{x}=I_k} =1$

<u>Definition 4.7</u>: $S_k$ represents the binary vector $(b_1,b_2,\ldots,b_m)$ such that $b_i$'s are 0's or 1's and k is the numerical value of $(b_1,b_2\ldots b_m)$, when the latter is interpreted as a binary number.

Observe that $m_k(\underline{y})\Big|_{\underline{y}=S_k} = 1$

<u>Definition 4.8</u>: $S_{i1}$ and $S_{i2}$ are said to be $y_j$-adjacent to each other, if their representations as defined in Definition 4.7 agree in every bit except the $j^{th}$ one.

<u>Definition 4.9</u>: TP (dF) denotes the set of transitions specified by the differential expression dF which can cause F to change from 0 to 1, if dF is compatibly integrable. If dF is not integrable, TP(dF) is not defined.

<u>Definition 4.10</u>: If a change in the value of state variable $y_j$ resulting from a change in input causes another state variable $y_i$, for some $i \neq j$, to change its value, then a <u>secondary transition</u> or <u>ripple</u> is said to occur in flipflop that is associated with the state variable $y_i$. If in a DM system a ripple cannot occur, the system is called <u>ripple-free</u>.

<u>Definition 4.11</u>: $m_j(\underline{x} - x_i)\,\Delta x_i$ and $m_j(\underline{x} - x_i)\,\nabla x_i$ defined earlier will also, be denoted by $m_j(\underline{x} - x_i)dx_i$ and $m_j(\underline{x} - x_i)d\overline{x}_i$, respectively.

<u>Definition 4.12</u>: $\partial m_j(\underline{x} - x_i)$ denotes transitions defined in Definitions 4.2 and 4.3 as follows:

$$\partial(m_j(\underline{x} - x_i) = \begin{cases} m_j(\underline{x} - x_i)\Delta x_i, & \text{if } x_i \text{ is in true form in } m_j(\underline{x}) \\ m_j(\underline{x} - x_i)\nabla x_i, & \text{if } x_i \text{ is in complemented form in } m_j(x) \end{cases}$$

<u>Definition 4.13</u>: $m_j(\underline{x} - x_i) \mathbin{\Delta\kern-0.75em\nabla} x_i$ denotes a pair of transitions defined by $m_j(\underline{x} - x_i)\Delta x_i$ and $m_j(\underline{x} - x_i)\nabla x_i$.

<u>Definition 4.14</u>: A DMS system table is said to be <u>level-wise output-unambiguous</u>, if there exist no input conditions $I_i$, $I_j$, $I_k$ and states $S_a$ and $S_b$, $I_i$ and $I_k$ being adjacent, $I_j \neq I_k$ $S_a$ and $S_b$ not necessarily distinct, such that $g'(S_a, I_j, I_i)$, $g'(S_b\ I_k, I_i)$, $f'(S_a\ I_j, I_i)$ and $f'(S_b, I_k, I_i)$ are defined and

$g'(S_a, I_j, I_i) = g'(S_b, I_k, I_i) = S_c$ (say)

$f'(S_a, I_j, I_i) = O_{jc} \neq O_{kc} = f'(S_b, I_k, I_i)$.

| | $I_j$ $I_i$ | $I_k$ $I_i$ |
|---|---|---|
| $S_a$ (or $S_b$) | $S_c, O_{jc}$ | $S_c, O_{kc}$ |

| | $I_j$ | $I_k$ |
|---|---|---|
| $S_a$ | $S_c, O_{jc}$ | |
| $S_b$ | | $S_c, O_{kc}$ |

A DMS system table which is not level-wise output-unambiguous will be called <u>level-wise-ambiguous</u>.

## 4.2 BASIC ASSUMPTIONS

All the theorems that follow are pertaining to realization of a DM system table using clock-triggered flipflops. Unless otherwise stated, the following assumptions will be applicable to all our discussion:

1. only one input variable can change at a time
2. only one state variable is allowed to change during a state transition. This is equivalent to assuming that the specified

table (after state addition if necessary) lends itself to single-variable-change state assignment. This restriction will be removed later.

3. all flipflops respond to a positive transition in clock input
4. $C_i$ ($=C_i(\underline{x},\underline{y})$) denotes the function defining the input to the clock pin of the flipflop i, i.e., the flipflop associated with variable $y_i$, for $V_i$, $1 \leq i \leq m$.
5. an input (condition) $I_k$ corresponds to value of $\underline{x}$ such that

$$m_k(\underline{x}) \Big|_{\underline{x}=I_k} =1 .$$

6. a state (assignment) $S_k$ represents value of $\underline{y}$ such that

$$m_k(\underline{y}) \Big|_{y=S_k} =1 .$$

7. The number of states in the table is already reduced to minimum possible.

The following theorems establish conditions for realizing a DMS table using clock-triggered flipflops:

Theorem 4.1: Consider a DM system table whose realization exists. Then corresponding to every row (or state) $S_{i1}$ and input change from $I_{j1}$ to $I_{j2}$, $0 \leq i \leq q-1$, $0 \leq j1 \leq p-1$, $0 \leq j2 \leq p-1$, $I_{j1}$ and $I_{j2}$ being $x_i$-adjacent, if the next state function $g'(S_{i1}, I_{j1}, I_{j2})$ is defined and

(4.1.1) $g'(S_{i1}, I_{j1}, I_{j2}) = S_{i2}$ where

(4.1.2) $S_{i1}$ and $S_{i2}$ are $y_k$-adjacent, then

(4.1.3) $dC_k \supseteq m_{i1}(\underline{y}) \cdot \partial(m_{j2}(\underline{x}-x_i))$, $1 \leq k \leq m$

The proof is given in reference 14.

<u>Theorem 4.2</u>: Any finite-state asynchronous sequential system can be realized using clock-triggered flipflops and logic gates and employing Boolean calculus method.

The proof is given in Semi-Annual Status Report #2 [15].

<u>Theorem 4.3</u>: The complexity of network realization of a finite-state asynchronous sequential system, consisting of clock-triggered flipflops and logic gates obtained by employing Boolean calculus method is no higher than that of a network realization of the same system, consisting of S-R flipflops (without clock inputs) and logic gates obtained by conventional method for synthesis of an FMA system.

When the DMS table admits of a unit-distance state assignment, the realization of the system is possible using any commercially available flipflops. When the DMS table is such that unit-distance state assignment is not possible, then certain relationships among the tune response characteristics of the flipflops must be satisfied so that the different time responses of flipflops do not cause undesired transitions and hazards. These need to be obtained.

Synthesis procedures are illustrated in conference papers given in Appendices II & III.

## 5. SYNTHESIS USING SP COUNTER

Efforts to explore the possibility of using an SP (synchronous presettable) counter to realize an FMA system were successful. Such an approach significantly reduces the number of IC packages required for the system to be realized, thus reducing network complexity, size and cost.

### 5.1 SP COUNTER

An SP counter (such as 74LS160) has the following input and output pins of interest to us:

(1) count-enable inputs P & T, both of which must be high for the counter to count.

(2) Load input L which, on low level, causes the data on the data input pins to be transferred synchronously to the count output pins when a positive transition of clock pulse occurs.

(3) Clock input pin CK. Loading or counting occurs synchronously on the positive transition of clock pulse.

(4) Data input pins $D_1$, $D_2$, ..., $D_n$. The data on these pins are transferred to count output pins $Y_1$, $Y_2$, ... , $Y_n$ respectively on the positive transition of clock pulse when L = O.

(5) Output pins $Y_1$, $Y_2$, ... , $Y_n$ give the count output of the counter.

## 5.2 EXAMPLE

Before presenting a formal theory and procedure for synthesis, we will illustrate the procedure with the following example:

Consider the FMA system given in Figure 5.2.1.

| $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| a | a,0 | a,0 | b,- | a,0 |
| b | a,- | d,1 | b,1 | b,1 |
| c | a,- | a,- | c,0 | c,0 |
| d | a,- | d,1 | c,- | - |

Figure 5.2.1

Observe that the system is already minimized. Moreover it does not admit of a unit-distance state assignment using only two state variables. Hence three state variables are needed to realize the system, if conventional synthesis procedure is employed.

Using the transformation equations in Definition 2.1 we get the Differential Mode System (DMS) given in Figure 5.2.2 which is equivalent to the system under consideration.

| $Y_1Y_2$ | $X_1X_2$ | 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | a | a,0 | a,0 | b,1 | a,0 | - | - | a,0 | b,1 |
| 01 | b | - | - | - | - | d,1 | b,1 | a,0 | b,1 |
| 11 | c | - | - | - | - | a,1 | c,0 | a,0 | c,0 |
| 10 | d | - | - | c,0 | a,0 | - | - | - | - |

Figure 5.2.2

Let dC denote the differential expression for the clock function. dC is given by

(E5.2.1) $$dC = \bar{Y}_1\bar{Y}2(x_2dx_1+x_1dx_2) + \bar{Y}_1Y_2(x_2d\bar{x}_1+\bar{x}_2d\bar{x}_1) + \\ + Y_1Y_2(x_2d\bar{x}_1+\bar{x}_2d\bar{x}_1) + Y_1\bar{Y}_2(x_2dx_1+\bar{x}_1d\bar{x}_2)$$

Let $C_1$ be a compatible integral of dC. Then

(E5.2.2) $$C_1 = \bar{Y}_1\bar{Y}_2\ x_1x_2 + \bar{Y}_1Y_2\bar{x}_1 + Y_1\bar{Y}_2\cdot(x_1x_2+\bar{x}_1\bar{x}_2) \quad + Y_1Y_2(\bar{x}_1) \\ = \bar{Y}_2x_1x_2 + Y_2\bar{x}_1 + Y_1\bar{x}_1\bar{x}_2$$

Observe that

(E5.2.3) $$\frac{\partial C_1}{\partial x_1} = \bar{Y}_2x_2$$

(E5.2.4) $$\frac{\partial C_1}{\partial \bar{x}_1} = Y_2 + Y_1\bar{x}_2$$

(E5.2.5) $$\frac{\partial C_1}{\partial x_2} = \bar{Y}_2x_1$$ and

(E5.2.6) $$\frac{\partial C_1}{\partial \bar{x}_2} = Y_1\bar{x}_1$$

For the positive transitions that occur as shown in equations (E5.2.3) through (E5.2.6), we need to provide the appropriate values to data input pins $D_1$ and $D_2$ as shown in Figure 5.2.3.

| $Y_1Y_2$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | - | - | 01 | - |
| 01 | 00 | 10 | - | - |
| 11 | 00 | 00 | - | - |
| 10 | 00 | - | 11 | - |

$D_1D_2$

Figure 5.2.3

| $Y_1Y_2$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | - | 0 |
| 01 | - | 1 | 1 | 1 |
| 11 | - | - | 0 | 0 |
| 10 | - | 1 | - | - |

Z (Output)

Figure 5.2.4

From Figures 5.2.3 and 5.2.4 we get

(E5.2.7) $D_1 = \bar{x}_1 x_2 \bar{Y}_1 + x_1 Y_1$

(E5.2.8) $D_2 = x_1$ and

(E5.2.9) $Z = Y_1 \oplus Y_2$.

Equations (E5.2.2), (E5.2.7), (E5.2.8) and (E5.2.9) give the system realization with

(E5.2.10) $L = O = P = T$.

## 5.3 SYNTHESIS PROCEDURE

Given an FMA system that is already reduced, the first thing to do is to find an equivalent DMS table using the equations in Definition 2.1. If the table thus obtained is reduced, if it is reducible, then the system may or may not be realizable. The procedure that follows applies to DMS table as obtained after transforming the FMA system. Later we will present the procedure for synthesizing DMS table that is reducible.

1. Consider next state for every present state and every input change. If the next state is different than the present state for a given present state and input change, form a differential term that reflects the input change and the present state in which the change is occurring. Taking Boolean sum of all such differential terms, form the differential expression for the clock function.

2. Find a compatible integral, say $C_1$, of the differential expression obtained above.

3. Find the Boolean differential $dC_1$, of the function $C_1$ obtained so as to determine all possible positive transitions that can occur in the clock function.

4. Determine the value of next state and hence values of next state variables $D_1, D_2, \ldots D_n$ corresponding to every differential term in $dC_1$. On the Karnaugh map for $D_i$, $1 \leq i \leq n$ place the value of $D_i$ in the cell corresponding to the present state and the value of input that prevails after the input change described in the differential term occurs. The remaining cells are left unspecified. Realize functions $D_1, D_2, \ldots D_n$ from the Karnaugh maps.

5. Obtain the output function z in terms of input variables and state variables as is usually done.

6. The LOAD pin and count enable inputs P and T are grounded. The functions $C_1$, $D_1, D_2, \ldots, D_n$ and Z along with an SP counter give the desired network realization.

If the DMS table is reduced, then the conditions in Theorem 5.4.2 must be satisfied for it to be realized as a network with an SP counter in it. If the conditions are satisfied, the procedure mentioned above can be followed for synthesizing the table.

## 5.4 REALIZABILITY

Next we will consider some theorems pertaining to realizability of a given FMA system using an SP counter.

Theorem 5.4.1: Given a DMS table obtained from an FMA system that has the same number of states as the former, it is realizable using an SP counter. The proof is outlined in reference [18].

Theorem 5.4.2: If the DMS table derived from an FMA system is reduced, then it is realizable using an SP counter if the following conditions are satisfied:

(1) The differential expression for the clock function for the table is compatibily integrable.

(2) The table is level-wise next-state- and output-unambiguous.

# 6. NONCOMBINATIONAL BOOLEAN CALCULUS

In Boolean calculus studied so far it was assumed that a function being studied is the output of a combinational system whose inputs are the arguments of the function. Also, while integrability of a differential expression was studied, it was tacitly assumed that an integral, if it exists, would be realized with a combinational system.

An attempt was made to generalize the Boolean calculus that was developed with the limitations shown above. Such calculus, to be referred to, henceforth, as noncombinational Boolean calculus, will help us describe the output, after an input change, of a noncombinational system in terms of changes in the inputs to the system. Also, if the output, after an input change, is specified in terms of changes in inputs, realizability of such a specification using a noncombinational system will be studied. Some results obtained in this direction will be described in what follows. It will be assumed that only one variable can change at a time.

<u>Definition 6.1</u>: $\Delta x_i$, $1 \le i \le n$, denotes a change in $x_i$ from 0 to 1.

(D6.1.1) $$\Delta x_i = \begin{cases} 1 & \text{when } x_i \text{ changes from 0 to 1} \\ 0 & \text{otherwise} \end{cases}$$

$\nabla x_i$, $1 \le i \le n$, denotes a change in $x_i$ from 1 to 0.

(D6.1.2) $\nabla x_i = \begin{cases} 1, \text{ when } x_i \text{ changes from 1 to 0} \\ 0, \text{ otherwise} \end{cases}$

<u>Definition 6.2</u>: The terms $x_i\Delta x_i$, $\overline{x}_i\Delta x_i$, $x_i\nabla x_i$ and $\overline{x}_i\nabla x_i$ will be defined as follows:

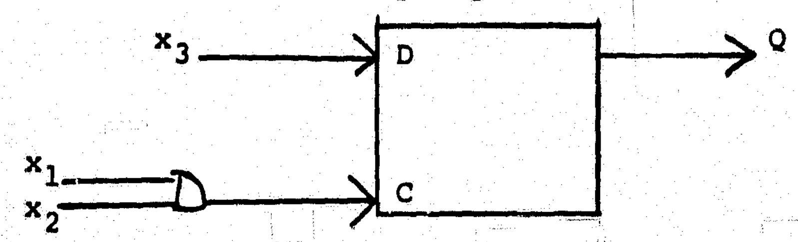
(D6.2.1) $x_i\Delta x_i = \Delta x_i$

(D6.2.2) $\overline{x}_i\Delta x_i = 0$

(D6.2.3) $x_i\nabla x_i = 0$

(D6.2.4) $\overline{x}_i\nabla x_i = \nabla x_i$

Consider a D-flipflop shown below:




Since the relationship between Q and $x_1$, $x_2$ and $x_3$ is not combinational, we cannot express Q in terms of a Boolean function of variables $x_1$, $x_2$ and $x_3$. However we could express the value of Q immediately following any transition of the clock.

Observe that

(D6.1.1) $$C = x_1 x_2$$

so that

(D6.1.2) $$dC = x_1 dx_2 + x_2 dx_1$$

Since only the positive transitions of clock are of interest, we may describe the positive transitions of clock in terms of changes in $x_1$ and $x_2$

(D6.1.3) $$\Delta c = x_1 \Delta x_2 + x_2 \Delta x_1$$

Let Q(T+) denote the value of Q immediately following any transition of clock. Then by definition

(D6.1.4) $$Q(T+) = D \, .\Delta c$$

or

(D6.1.5) $$Q(T+) = Dx_2 \Delta x_1 + Dx_1 \Delta x_2$$

If we let

(D6.1.6) $D = x_3$, then

(D6.1.7) $$Q(T+) = x_2 x_3 \Delta x_1 + x_1 x_3 \Delta x_2$$

Equation (D6.1.7) points out that Q is 1 after the following transitions:

(1) $x_2 = x_3 = 1$ and $x_1$ changes from 0 to 1.

(2) $x_1 = x_3 = 1$ and $x_2$ changes from 0 to 1.

Observe that if $x_3 = 0$ and $x_1 = 1$ while $x_2$ changes from 0 to 1, then a transition does occur making Q to remain at or go to 0. This is not to be seen from equation (D6.1.7) if the function D (i,e, $x_3$ in this case) is not kept separate from the transition terms. Hence a more desirable form for Q(T+) than that shown in equation (6.1.7) would be

(D6.1.8) $\quad Q(T+) = D\cdot[x_2\Delta x_1 + x_1\Delta x_2]$.

<u>Definition 6.3</u>: The function Q(T+) as shown in equation (D6.3.1) below will be called <u>next-value</u> function.

(D6.3.1) $\quad Q(T+) = D.\left[\sum_{i=1}^{n}(\alpha_i\Delta x_i + \beta_i\nabla x_i)\right]$ where D is a function of <u>x</u> and <u>y</u>.

Obviously the function D outside the square bracket refers to the value that Q would assume if and when one of the transition terms inside the square brackets assumes value of 1.

Addressing ourselves to the reverse problem of synthesizing a network that would realize a next-value function Q(T+) of the form

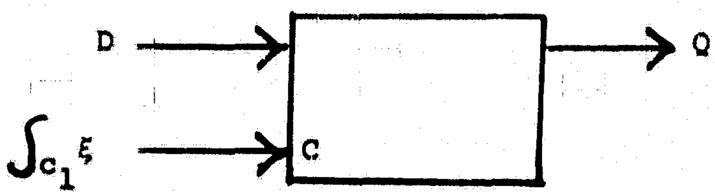
(D6.1.9) $\quad Q(T+) = D.\left[\sum_{i=1}^{n}(\alpha_i\Delta x_i + \beta_i\nabla x_i)\right]$,

where $\alpha_i$ and $\beta_i$ are assumed to be independent of $x_i$, for all i, without loss of generality (in view of Definition 6.2), all that we need to do is to find the exact integral, if it exists, of the differential expression

(D6.1.10) $\quad d\xi = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\overline{x}_i)$.

Of course, if the differential expression is not exactly integrable but compatibly integrable and if

$\int_{c1} d\xi$ is a compatible integral of the differential expression, then a realization of the form




will provide not only the transitions that are specified in equation (D6.1.9) but, also, some additional transitions.

<u>Theorem 6.1</u>: If the next-value function of a system is given by

(T6.1.1) $\quad Q(T+) = D.\left[\sum_{i=1}^{n} (\alpha_i \Delta x_i + \beta_i \nabla x_i)\right]$

where

(T6.1.2) $\quad D = D_1 \cdot x_{i1}\, x_{i2} \cdot\cdots\cdot x_{ik},\ 1 \leq k \leq n$

(T6.1.3) $\quad F(\underline{x}) = \int_{E}\left(\sum_{i=1}^{n} \alpha_i dx_i + \beta_i d\bar{x}_i\right)$ and

(T6.1.4) $\quad F(\underline{x}) = x_{i1} \cdot x_{i2} \cdot\cdots\cdot x_{ik} \cdot F(\underline{x})$,

then $Q_1(T+)$ described as

(T6.1.5) $\quad Q_1(T+) = D_1 \cdot \left[\sum_{i=1}^{n} (\alpha_i \Delta x_i + \beta_i \nabla x_i)\right]$

realizes the same next-value function as $Q(T+)$ in equation (T6.1.1) does.

<u>Proof</u>: Suppose due to a transition described by $\partial m_p(\underline{x} - x_q)$, $Q(T+) = 1$ if $\underline{y} = S_0$. This implies that

$D = 1$ when $\underline{x} = b_p$ & $\underline{y} = S_0$

Hence when $\underline{y} = S_0$ and $\underline{x} = b_p$

$1 = D = D_1 \cdot x_{i1} \cdots x_{ik}$

so that $D_1 = 1$ for $\underline{x} = b_p$ & $\underline{y} = S_0$

Definition 5.3: F is said to be a compatible integral of dH, denoted by $\int_c dH$, and dH is said to be compatibly integrable if

$$\frac{\partial F}{\partial x_i} = \alpha_i \quad \text{and} \quad \frac{\partial F}{\partial \bar{x}_i} = \beta_i \qquad \text{(D5.3.1)}$$

for all $i$, $1 \le i \le n$.

Observe that by the definitions given above if dH is exactly integrable, then $F = \int_E dH$ goes through exactly the changes which are described in dH.

In what follows we will obtain ways of finding all possible compatible integrals of dH, if dH is compatibly integrable. To accomplish this we need the following integral operators:

Definition 5.4: The zeroth order integral of dH, denoted by $\int_o dH$, is defined as

$$\int_o dH = \sum_{i=1}^{n} (\alpha_i \bar{x}_i + \beta_i x_i) \qquad \text{(D5.4.1)}$$

where

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i). \qquad \text{(D5.4.2)}$$

Also, the first order integral of dH, denoted by $\int_1 dH$, is defined as

$$\int_1 dH = \sum_{i=1}^{n} (\alpha_i x_i + \beta_i \bar{x}_i). \qquad \text{(D5.4.3)}$$

Definition 5.5: A binary point $\underline{b}_o \in B(n)$ is said to be "one" (or "zero") of a function $F(\underline{x})$ if

$$F(\underline{b}_o) = 1 \text{ (or } 0) \qquad \text{(D5.5.1)}$$

<u>Lemma 5.1</u>: If the differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \qquad \text{(L5.1.1)}$$

is compatibly integrable and $F_1$ is a compatible integral of dH, then every "one" of $\int_1 dH$ is also a "one" of $F_1$.

<u>Proof:</u> Since $F_1$ is a compatible integral, by Definition 5.3

$$\frac{\partial F_1}{\partial x_i} \supseteq \alpha_i \qquad \text{(L5.1.2)}$$

and

$$\frac{\partial F_1}{\partial \bar{x}_i} \supseteq \beta_i . \qquad \text{(L5.1.3)}$$

Also

$$dF_1 = \sum_{i=1}^{n} \left(\frac{\partial F_1}{\partial x_i} dx_i + \frac{\partial F_1}{\partial \bar{x}_i} d\bar{x}_i\right) \qquad \text{(L5.1.4)}$$

so that the "ones" of $\frac{\partial F_1}{\partial x_i} \cdot x_i$ (or $\frac{\partial F1}{\partial \bar{x}_i} \cdot \bar{x}_i$), $1 \leq i \leq n$, are also the "ones" of $F_1$

From equation (L5.1.2) (or (L5.1.3)) the "ones" of $\alpha_i x_i$ (or $\beta_i \bar{x}_i$), $1 \leq i \leq n$, are the "ones" of $\frac{\partial F_1}{\partial x_i} \cdot x_i$ (or $\frac{\partial F_1}{\partial \bar{x}_i} \cdot \bar{x}_i$) for all $1 \leq i \leq n$.

Hence the "ones" of $(\alpha_i x_i + \beta_i \bar{x}_i)$, $1 \leq i \leq n$, are also the "ones" of $F_1$. Hence the "ones" of $\int_1 dH$ are the "ones" of $F_1$.

Q.E.D.

Arguing on a similar basis, we can establish the following lemma.

<u>Lemma 5.2:</u> If the differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \qquad \text{(L5.2.1)}$$

is compatibly integrable and $F_1(\underline{x})$ is a compatible integral of dH, then the "ones" of $\int_0 dH$ are "zeroes" of $F_1$.

<u>Proof:</u> The proof is similar to that of Lemma 5.1.

<u>Theorem 5.1</u>: A necessary condition for compatible integrability of the differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \tag{T5.1.1}$$

is that

$$\left(\int_0 dH\right) \cdot \left(\int_1 dH\right) = 0 \tag{T5.1.2}$$

for all $\underline{x} \in B(n)$.

<u>Proof</u>: Suppose dH is compatibly integrable so that there exists $F_1(\underline{x})$ such that

$$F_1 = \int_c dH \tag{T5.1.3}$$

Also, suppose that there exists $\underline{b_o}$ such that

$$\left[\left(\int_0 dH\right) \cdot \left(\int_1 dH\right)\right]\Bigg|_{\underline{x}=\underline{b_o}} = 1 \tag{T5.1.4}$$

which implies that

$$\left(\int_0 dH\right)\Bigg|_{\underline{x} = \underline{b_o}} = 1 \tag{T5.1.5}$$

and

$$\left(\int_1 dH\right)\Bigg|_{\underline{x} = \underline{b_o}} = 1 . \tag{T5.1.6}$$

From Lemma 5.1 and equation (T5.1.6),

$\underline{b_o}$ is a "one" of $F_1$. (T5.1.7)

From Lemma 5.2 and equation (T5.1.5),

$\underline{b_o}$ is a "zero" of $F_1$ (T5.1.8)

Statements (T5.1.7) and (T5.1.8) contradict each other. Hence there exists no $\underline{b_o} \in B(n)$ that satisfies equation (T5.1.4). Hence equation (T5.1.2) is a necessary condition for dH to be compatibly integrable.

Q.E.D.

<u>Lemma 5.3</u>: If the differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \tag{L5.3.1}$$

satisfies the equation

$$(\textstyle\int_0 dH) \cdot (\int_1 dH) = 0 \text{ for all } \underline{x} \in B(n), \tag{L5.3.2}$$

then (a) $\alpha_i \int_1 dH = \alpha_i x_i,$ (L5.3.3)

(b) $\alpha_i \int_0 dH = \alpha_i \bar{x}_i$ (L5.3.4)

and (c) $\alpha_i \overline{(\int_0 dH)} = \alpha_i x_i.$ (L5.3.5)

<u>Proof</u>: From Definition 5.4 and equation (L5.3.2) we have

$$0 = (\sum_{j=1}^{n} (\alpha_j x_j + \beta_j \bar{x}_j)) \cdot (\sum_{i=1}^{n} (\alpha_i \bar{x}_i + \beta_i x_i))$$

$$= \sum_{i=1}^{n} \sum_{j=1}^{n} (\alpha_i \alpha_j \bar{x}_i x_j + \beta_i \alpha_j x_i x_j + \alpha_i \beta_j \bar{x}_i \bar{x}_j$$

$$+ \beta_i \beta_j x_i \bar{x}_j). \tag{L5.3.6}$$

Hence for all i, j, $1 \le i \le n$, $1 \le j \le n$

$$\alpha_i \alpha_j \bar{x}_i x_j + \beta_i \alpha_j x_i x_j + \alpha_i \beta_j \bar{x}_i \bar{x}_j + \beta_i \beta_j x_i \bar{x}_j = 0 \tag{L5.3.7}$$

so that $\alpha_i \alpha_j \bar{x}_i x_j = \beta_i \alpha_j x_i x_j = \alpha_i \beta_j \bar{x}_i \bar{x}_j = \beta_i \beta_j x_i \bar{x}_j = 0.$ (L5.3.8)

Now $\alpha_i \int_1 dH = \alpha_i \ (\sum_{j=1}^{n} \alpha_j x_j + \beta_j \bar{x}_j)$ (L5.3.9)

$$= \alpha_i x_i + \alpha_i \beta_i \bar{x}_i + \sum_{\substack{j=1 \\ j \neq i}}^{n} (\alpha_i \alpha_j x_j + \alpha_i \beta_j \bar{x}_j)$$

$$= \alpha_i x_i + \alpha_i \beta_i \bar{x}_i$$

$$+ \sum_{\substack{j=1 \\ j \neq i}}^{n} (\alpha_i \alpha_j x_i x_j + \alpha_i \alpha_j \bar{x}_i x_j + \alpha_i \beta_j x_i \bar{x}_j + \alpha_i \beta_j \bar{x}_i \bar{x}_j).$$

In equation (L5.3.8), setting i=j yields

$$\alpha_i \beta_i = 0 \tag{L5.3.10}$$

for all i, $1 \le i \le n$.

Hence using equations (L5.3.8)-(L5.3.10), we get

$$\alpha_i \int_1 dH = \alpha_i x_i + \alpha_i x_i \left( \sum_{\substack{j=1 \\ j \neq i}}^{n} (\alpha_j x_j + \beta_j \bar{x}_j) \right) = \alpha_i x_i . \qquad \text{(L5.3.3)}$$

By interchanging i and j in equation (L5.3.9), we get

$$\alpha_i \int_0 dH = \alpha_i \bar{x}_i . \qquad \text{(L5.3.4)}$$

Now $\alpha_i \overline{(\int_0 dH)}$

$= \alpha_i (1 \oplus \int_0 dH)$

$= \alpha_i \oplus \alpha_i \int_0 dH$

$= \alpha_i \oplus \alpha_i \bar{x}_i$ (from equation (L5.3.4))

$= \alpha_i x_i .$ (L5.3.5)

Q.E.D.

<u>Theorem 5.2</u>: If the differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \qquad \text{(T5.2.1)}$$

satisfies equation

$$(\int_0 dH) \cdot (\int_1 dH) = 0 \qquad \text{(T5.2.2)}$$

for all $\underline{x} \in B(n)$ then F given by

$$F = \int_1 dH + \Psi \overline{(\int_0 dH)} \qquad \text{(T5.2.3)}$$

is a compatible integral of dH, where $\Psi$ is an arbitrary function of $\underline{x}$.

<u>Proof</u>: ANDing both the sides of equation (T5.2.3) by $\alpha_i$, we have

$$\alpha_i F = \alpha_i \int_1 dH + \Psi\alpha_i . \overline{(\int_o dH)}$$

$$= \alpha_i x_i + \Psi \alpha_i x_i \quad \text{(from Lemma 5.3)}$$

$$= \alpha_i x_i \ (1 + \Psi)$$

$$= \alpha_i x_i \tag{T5.2.4}$$

Since $\alpha_i$ is independent of $x_i$, then

$$\alpha_i \frac{\partial F}{\partial x_i} = \frac{\partial(\alpha_i F)}{\partial x_i}$$

$$= \frac{\partial(\alpha_i x_i)}{\partial x_i} \quad \text{(from equation (T5.2.4)}$$

$$= \alpha_i \frac{\partial x_i}{\partial x_i} \tag{T5.2.5}$$

$$= \alpha_i$$

$$\therefore \quad \frac{\partial F}{\partial x_i} \geq \alpha_i . \tag{T5.2.6}$$

Similarly $$\frac{\partial F}{\partial \bar{x}_i} \geq \beta_i . \tag{T5.2.6}$$

Hence by Definition 5.2, F is a compatible integral of dH.

Q.E.D.

<u>Theorem 5.3</u>: A differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \tag{T5.3.1}$$

is compatibly integrable if and only if

$$(\int_o dH) . (\int_1 dH) = 0 \tag{T5.3.2}$$

for all $\underline{x} \in B(n)$.

<u>Proof</u>: The proof follows from Theorems 5.1 and 5.2.

A word regarding the arbitrary function $\Psi(\underline{x})$ in equation (T5.2.3) is in order. If sets $D_o$ and $D_1, \phi \subseteq D_i \subseteq B(n)$, $i=0$ and 1, are bases (Definition 2.2) of functions $\int_o dH$ and $\int_1 dH$, then every distinct-$\Psi$ would give rise to a distinct compatible integral provided $\Psi$ is based on a subset (not necessarily proper) of $D = \overline{D_o \cup D_1}$ In fact if $\Psi$ is based on a subset of D, then the factor $(\int_o dH)$ that is ANDed with $\Psi$ in equation (T5.2.3) may be dropped since $\overline{D_o} \supset \overline{D_o \cup D_1} = D$. Hence we can modify Theorem 5.2 as shown in the next theorem.

<u>Theorem 5.4</u>: Let $dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i)$ (T5.4.1)

be a differential expression.

If (a) $\int_o dH . \int_1 dH = 0$ for all $\underline{x} \in B(n)$, (T5.4.2)

(b) $D_o$ and $D_1$ are bases of $\int_o dH$ and $\int_1 dH$ respectively,

(c) the number of distinct points in the set $D = \overline{(D_o \cup D_1)}$ is m, (T5.4.3)

(d) $\theta_i(\underline{x})$, $1 \leq i \leq 2^m$, is a function based on a subset of D, $\theta_i(x) \neq \theta_j(\underline{x})$ for all i, j, $i \neq j$, $1 \leq j \leq 2^m$ and

(e) $F_i = \int_1 dH + \theta_i$, (T5.4.4)

then $F_i$ is a compatible integral of dH.

<u>Proof</u>: The essence of the proof is outlined in the discussion preceding the theorem. A formal proof can be given using the Tapia-Tucker method [36, 37] for obtaining the complete solution for Boolean equations.

We will, now, show an application of the results established in this section, to synthesis of a clock function illustrated in the next example.

<u>Example 5.1</u>

A clock function $C(x_1, x_2, x_3)$ is to be realized which goes through, at least, the transitions specified in the differential expression

$$dC = (x_2\bar{x}_3 + \bar{x}_2 x_3)\, dx_1 + (x_1\bar{x}_3)\, dx_2 + (x_1 x_3)\, d\bar{x}_2 + (x_1\bar{x}_2)\, dx_3 + (x_1 x_2)\, d\bar{x}_3 \quad \text{(E5.1.1)}$$

Find C, if it exists.

We have

$$\begin{aligned}\int_0 dC &= (\bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1\bar{x}_2 x_3) + x_1\bar{x}_2\bar{x}_3 \\ &\quad + x_1 x_2 x_3 + x_1\bar{x}_2\bar{x}_3 + x_1 x_2 x_3 \qquad \text{(E5.1.2)} \\ &= \bar{x}_1 x_2\bar{x}_3 + \bar{x}_1\bar{x}_2 x_3 + x_1\bar{x}_2\bar{x}_3 + x_1 x_2 x_3\end{aligned}$$

and

$$\begin{aligned}\int_1 dC &= x_1 x_2\bar{x}_3 + x_1\bar{x}_2 x_3 + x_1 x_2\bar{x}_3 + x_1\bar{x}_2 x_3 + x_1\bar{x}_2 x_3 \\ &\quad + x_1 x_2\bar{x}_3 \\ &= x_1 x_2\bar{x}_3 + x_1\bar{x}_2 x_3. \qquad \text{(E5.1.3)}\end{aligned}$$

Obviously

$$\left(\int_0 dC\right) \cdot \left(\int_1 dC\right) = 0\,. \qquad \text{(E5.1.4)}$$

Hence by Theorem 5.3, a compatible integral does exist.

Also, the term D referred to in equation (T5.4.3) is

$$\begin{aligned}D &= \overline{\{D_0 \cup D_1\}} \\ &= \overline{\{(0,0,1),\ (0,1,0),\ (1,0,0),\ (1,0,1),\ (1,1,0),\ (1,1,1)\}} \\ &= \{(0,0,0),\ (0,1,1)\} \qquad \text{(E5.1.5)}\end{aligned}$$

Thus $\theta_i(\underline{x})$, $1 \leq i \leq n$, can be constructed as follows

$$\theta_1(\underline{x}) = 0 \tag{E5.1.6}$$

$$\theta_2(\underline{x}) = \bar{x}_1\bar{x}_2\bar{x}_3 \tag{E5.1.7}$$

$$\theta_3(\underline{x}) = \bar{x}_1 x_2 x_3 \tag{E5.1.8}$$

$$\theta_4(\underline{x}) = \bar{x}_1\bar{x}_2\bar{x}_3 + \bar{x}_1 x_2 x_3 \tag{E5.1.9}$$

Also note that there are four solutions by Theorem 5.4:

$$C_1 = \int_1 dC + \theta_1 = x_1 x_2 \bar{x}_3 + x_1 \bar{x}_2 x_3 \tag{E5.1.10}$$

$$C_2 = x_1 x_2 \bar{x}_3 + x_1 \bar{x}_2 x_3 + \bar{x}_1\bar{x}_2\bar{x}_3 \tag{E5.1.11}$$

$$C_3 = x_1 x_2 \bar{x}_3 + x_1 \bar{x}_2 x_3 + \bar{x}_1 x_2 x_3 \tag{E5.1.12}$$

and

$$C_4 = x_1 x_2 \bar{x}_3 + x_1 \bar{x}_2 x_3 + \bar{x}_1\bar{x}_2\bar{x}_3 + \bar{x}_1 x_2 x_3. \tag{E5.1.13}$$

Observe that

$$dC_1 = (x_2 \oplus x_3)\, dx_1 + (x_1\bar{x}_3)\, dx_2 + (x_1 x_3)\, d\bar{x}_2 + (x_1\bar{x}_2)\, dx_3 + (x_1 x_2)\, d\bar{x}_3 \tag{E5.1.14}$$

$$= dC \tag{E5.1.15}$$

Hence $C_1$ realizes all the transitions specified in dC and no transitions which are not specified in dC. In fact by Definition 5.2, $C_1$ is also the exact integral of dC in equation (E5.1.1). Let us now examine $C_2$.

$$dC_2 = (x_2 \oplus x_3)\, dx_1 + \underline{(\bar{x}_2\bar{x}_3)\, d\bar{x}_1} + (x_1\bar{x}_3)\, dx_2 + (x_1 x_3 + \underline{\bar{x}_1\bar{x}_3})\, d\bar{x}_2 + (x_1\bar{x}_2)\, dx_3 + (x_1 x_2 + \underline{\bar{x}_1\bar{x}_2})\, d\bar{x}_3 \tag{E5.1.16}$$

Observe that $C_2$ realizes the transitions represented by differential terms $\bar{x}_2\bar{x}_3 d\bar{x}_1$, $\bar{x}_1\bar{x}_3 d\bar{x}_2$ & $\bar{x}_1\bar{x}_2 d\bar{x}_3$ which are not specified in dC in equation (E5.1.1). However it does realize all the transitions specified in dC.

As shown above, a differential expression that is exactly integrable is, also, compatibly integrable. Hence the necessary condition that

$$(\int_0 dH) \cdot (\int_1 dH) = 0$$

for all $\underline{x} \in B(n)$

$$\text{for} \quad dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i)$$

to be compatibly integrable is also necessary for dH to be exactly integrable. It can be shown that the condition is not sufficient for the differential expression to be exactly integrable.

Preliminary results pertaining to necessary and sufficient conditions for a differential expression to be exactly integrable are given in a recent publication [3]. Additional results on Boolean integrals have been developed and will be published in the near future.

Given a differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i),$$

if $(\int_0 dH0 \cdot (\int_1 dH) \neq 0$ for some $\underline{b} \in B(n)$, then the expression cannot be integrated exactly nor compatibly. However it could be decomposed as sum of several differential expressions, each one of which may be integrable separately as defined below.

<u>Definition 5.5</u> : Let $\left\{dH_j,\ 1\leq j\leq k\right\}$ be a set of Boolean differential expressions given by

$$dH_j = \sum_{i=1}^{n}[(\alpha_{ji})dx_i + (\beta_{ji})d\bar{x}_i]. \qquad \text{(D5.5.1)}$$

Then dH, the Boolean sum of all the differential expressions $dH_j$, $1\leq j\leq k$ is defined as

$$dH = \sum_{i=1}^{k} dH_j \qquad \text{(D5.5.2)}$$

$$= \sum_{i=1}^{n}\left[\left(\sum_{j=1}^{k}\alpha_{ji}\right)dx_i + \left(\sum_{j=1}^{k}\beta_{ji}\right)d\bar{x}_i\right]. \qquad \text{(D5.5.3)}$$

<u>Definition 5.6</u>: A differential expression dH is said to be integrable by parts if dH can be written as a sum of Boolean differential expressions $dH_j$, $1\leq j\leq k$ as defined in equations (D5.5.1) and (D5.5.3) such that $dH_j$ is compatibly integrable for all j, $1\leq j\leq k$. Any compatible integral of $dH_j$, $1\leq j\leq k$, will be called a <u>partial integral</u> of dH. A <u>complete set of partial integrals of Boolean differential expression</u> dH is a set of functions, $\left\{F_1, F_2, ---, F_k\right\}$ where for all j, $1\leq j\leq k$,

$$dF_j \supseteq dH_j. \qquad \text{(D5.6.1)}$$

Observe that k may assume one or more values between 1 and 2n. It will now be shown that any Boolean differential expression is integrable by parts.

<u>Theorem 5.5</u>: Any differential expression

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \qquad \text{(T5.5.1)}$$

is integrable by parts.

Proof: Observe that for any i, $1 \le i \le n$,

$$(\textstyle\int_1 \alpha_i dx_i) \cdot (\int_0 \alpha_i dx_i)$$

$$= (\alpha_i x_i) \cdot (\alpha_i \bar{x}_i)$$

$$= 0 \qquad (T5.5.2)$$

and

$$(\textstyle\int_1 \beta_i d\bar{x}_i) \cdot (\int_0 \beta_i d\bar{x}_i) \qquad (T5.5.2)$$

$$= 0 \qquad (T5.5.3)$$

so that $dH_{1,i}$ and $dH_{2,i}$ given by

$$dH_{1,i} = \alpha_i dx_i \text{ and } dH_{2,i} = \beta_i d\bar{x}_i \qquad (T5.5.4)$$

are compatibly integrable by Theorem 5.3 for all i, $1 \le i \le n$.

In view of the fact that we can write dH as

$$dH = \sum_{i=1}^{n} (dH_{1,i} + dH_{2,i}), \qquad (T5.5.5)$$

dH is compatibly integrable by Definition 5.6.

Q.E.D.

## 6. APPLICATION TO SYNTHESIS

As shown by Smith and Roth [34], techniques for synthesizing fundamental-mode asynchronous systems utilizing edge-sensitiveness property of clock-triggered flipflops often require fewer flipflops and gates than conventional techniques do.

The Smith and Roth technique [34, 35] requires a generalized edge-sensitive flipflop (as defined in [35]) in their design. We will present a procedure for synthesis of a fundamental-mode asynchronous system that uses a commercially available clock-triggered flipflop.

## EXAMPLE 6.1

A sequential system with two inputs, $X_1$ and $X_2$ and one output, Z is to be designed such that whenever $X_1$ changes from 0 to 1 the output changes to 1 if the output is 0. The output remains at 1 regardless of the values of $X_1$ till $X_2$ changes from 0 to 1. When $X_2$ changes from 0 to 1, Z goes to 0. After that $Z = 0$, regardless of the value of $X_1$, till, of course, a positive change in $X_1$ changes the value of Z to 1. Assume that $X_1=X_2=Z=0$ initially. Taking the conventional approach, we obtain the following reduced flow table for the system.

| $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| (A,B) 1 | 1,0 | 1,0 | 3,- | 2,- |
| (C,F) 2 | 2,1 | 1,- | 4,- | 2,1 |
| (D,G) 3 | 2,- | 3,1 | 3,1 | 2,- |
| (E,H) 4 | 1,- | 1,- | 4,0 | 4,0 |

Figure 6.1

Since the minimal system shown in Figure 6.1 has 4 states, 2 flipflops will be required to realize the system.

Now it will be shown that if edge-sensitive flipflops are used, one flipflop will be adequate to realize the system. The system under consideration can be described in terms of the state diagram given in Figure 6.2. The symbol $\Delta X_i$, i=1 or 2, implies a change in $X_i$ from 0 to 1. $\Delta X_i = 1$ if and only if $X_i$ changes from 0 to 1. $\Delta X_i = 0$ otherwise. The transition along a directed branch occurs if and only if the variable associated with it assumes the value of 1.

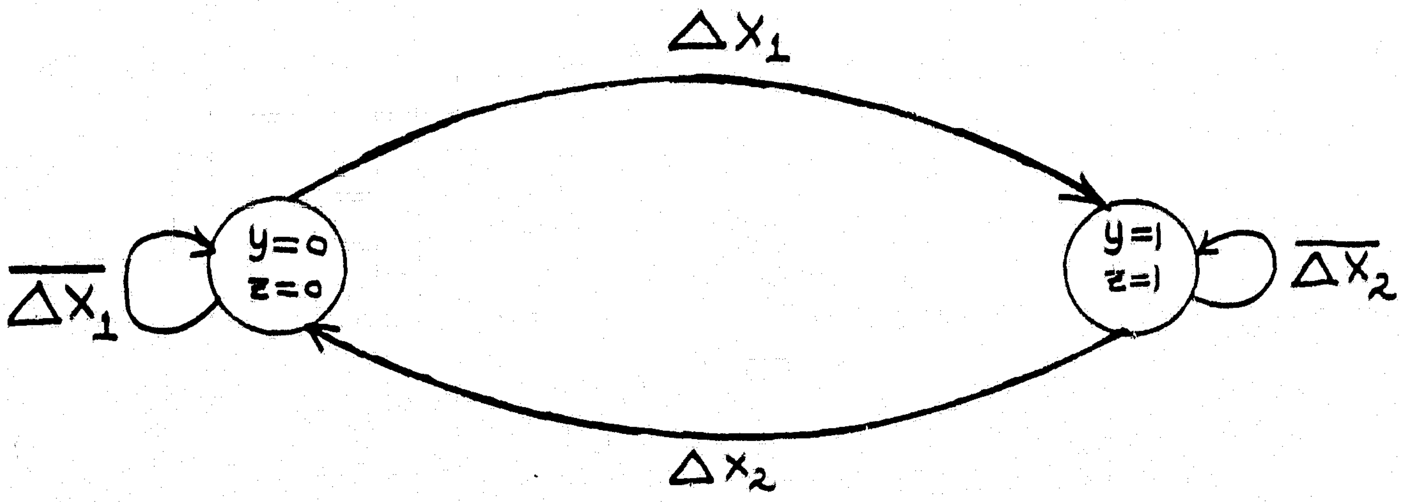



Figure 6.2

Observe that the system must change its state whenever

(a) $y=0$ and $X_1$ changes from 0 to 1

or (b) $y=1$ and $X_2$ changes from 0 to 1.

Hence the clock input function, C, must go through a positive transition when any of the changes stated above occurs. These transitions in terms of changes in $X_1$ and $X_2$ are described by the differential expression

$$dC = \bar{y}dx_1 + ydx_2. \tag{E6.1.1}$$

Note that $\int_0 dC \cdot \int_1 dC = (\bar{y}\bar{x}_1 + y\bar{x}_2)\cdot(\bar{y}x_1 + yx_2) = 0$ (E6.1.2)

so that by Theorem 5.3, dC is compatibly integrable and a compatible integral, say $C_1$, of dC is

$$C_1 = \bar{y}x_1 + yx_2 \tag{E6.1.3}$$

In fact since $\overline{D_o \cup D_1} = \emptyset$ (empty set) (E6.1.4)

($D_o$ & $D_1$ defined in Theorem 5.4),

by Theorem 5.4 no other compatible integral of dC exists.

Let $C = C_1 = \bar{y}x_1 + yx_2$ (E6.1.5) so that $Q_1(T+) = 1$. On the other hand if $Q_1(T+) = 1$ due to a transition $m_u(\underline{x} - x_v)$ when $\underline{y} = S_1$, then $D_1 = 1$ and $F(\underline{x}) = 1$ for $\underline{x} = b_u$ and equation (T6.1.6) implies that

$F(\underline{x}) = 1 = F(\underline{x}) \cdot x_{i1} \quad x_{ik}$ when $\underline{x} = b_u$,

which implies that $(x_{i1}.\text{----}.x_{ik}) = 1$ when $\underline{x} = b_u$.

Hence when $\underline{x} = b_u$ & $y = S_1$, $D = D_1.(x_{i1}.\text{----}.x_{ik})$

$$= 1 \cdot ( 1 )$$

$$= 1$$

Hence $Q(T+)$ and $Q_1(T+)$ have identical values immediately after any transition.

Q.E.D.

Theorem 6.2: Theorem 6.1 is valid if equations (T6.1.2) & (T6.1.4) are replaced by equations (T6.2.2) and (T6.2.4) respectively as given below:

(T6.2.2) $\quad D = D_1 \cdot \overline{x}_{i1} \cdot \overline{x}_{i2}.\text{----}.\overline{x}_{ik}$

(T6.2.4) $\quad F(\underline{x}) = \overline{x}_{i1}.\overline{x}_{i2}.\text{----}.\overline{x}_{ik}F(\underline{x})$.

The next-value functions for different types of flipflops (other than D-type) are currently under study. The results will be reported when the study is completed.

## 7. CONCLUSION

Boolean calculus was developed and formalized with the specific purpose of applying it to digital system synthesis. A procedure was developed to synthesize fundamental mode asynchronous systems using commercially available clock-triggered flipflops and Boolean calculus. It has been shown that synthesis techniques which utilize edge-sensitive property of flipflops judiciously lead to realizations which often require fewer flipflops and logic gates than those obtained by conventional techniques, thus reducing network complexity, size, the number of IC packages, power requirement, cost etc.

It has been established that any fundamental-mode asynchronous (FMA) system can be realized employing the new synthesis procedure proposed here. The procedure is applicable even when unit-distance state assignment is not used. However, in such a case certain relationships among the time response characteristics of the flipflops must be satisfied, which need to be obtained.

It has been shown that the procedure can be extended to synthesis of FMA system using a synchronous presettable counter. Again unit-distance state assignment is not required in this case.

The possibility of using the "dc" inputs of the flipflops in the synthesis procedure has been shown in the Semi-Annual Status Report #3 [14].

The concept of noncombinational Boolean calculus has been introduced. The next-value functions for flipflops are defined in terms of changes in the inputs. The reverse problem of synthesis is also considered. Considerable work remains to be done in this area.

Establishment of conditions for exact integrability, composition of differential functions, multi-variable-change calculus, methods of augmenting non-realizable DM tables so as to make them realizable, application to fault location and detection, etc. are among the many problems that remain to be solved.

The new results in Boolean calculus as well as the synthesis techniques developed here has opened an avenue for a large class of synthesis problems in which the components used are edge-sensitive and therefore present the potential of various economies if the edge-sensitiveness property is judiciously taken advantage of.

The publications that resulted from the research grant are listed next.

## 8. PUBLICATIONS GENERATED BY THE GRANT

(1) "Boolean Integral Calculus for Digital Systems", revised and submitted to IEEE Computer Transactions.

(2) "Development of Boolean Calculus and Its Applications", NASA Langley Basic Research Review Conference, Hampton, Va. April 1978.

(3) "Application of Boolean Calculus to Digital System Design", IEEE Southeastcon, Nashville, Tenn. April 14-16, 1980.

(4) Invited to present "Design of Asynchronous System Using a Synchronous presettable Counter", Southeastern Symposium on System Theory, Virginia Beach May 19-20, 1980.

(5) "Synthesis of Asynchronous Sequential Systems Using Edge-sensitive Flipflops", under preparation.

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## Appendix I

## BOOLEAN INTEGRAL CALCULUS FOR DIGITAL SYSTEMS


### ABSTRACT

The concept of Boolean integration is introduced and developed. When the changes in a desired function are specified in terms of changes in its arguments, then ways of "integrating" (i.e. realizing) such as a function, if it exists, are presented. Properties of newly defined integral operators are studied. Boolean Calculus has applications in design of logic circuits and in fault analysis. In the former case, it often leads to circuits which utilize fewer flipflops and logic gates than conventional methods.



INDEX TERMS: Boolean algebra, Boolean calculus, direct and inverse partial derivatives, Boolean differential, decompostion of function, Boolean differential expression, Boolean integration, compatible integral, exact integral, integration by parts, edge-sensitive flipflop, asynchronous sequential system synthesis.

## 1. INTRODUCTION

In recent years concepts of Boolean differentiation, difference, derivatives, differential and other logical operators have been introduced, developed and applied to digital network analysis and testing [6-27]. Also there has been a growing interest in Boolean integration and its application to synthesis of various types of logic circuits [1-5, 28-35]. The use of Boolean calculus in design of asynchronous sequential circuit with edge-sensitive flipflops often leads to simpler circuits utilizing fewer components than conventional techniques [5, 34, 35].

## 2. BOOLEAN FUNCTION AND ITS BASE

Throughout the paper, unless stated otherwise, a Boolean function $F(x_1, x_2, --- x_n)$ of $n$ Boolean variables $x_1, x_2, ---, x_n$ will be assumed. Also, it will be assumed that only one variable $x_i$, $1 \leq i \leq n$, can change at a time.

Definition 2.1: The set of $2^n$ binary vectors or points $(x_1, x_2, ---, x_n)$ where $x_i = 0$ or 1, $1 \leq i \leq n$, such that $x_i$ and $x_j$ may or may not be equal if $i \neq j$, will be called the Boolean set of variables $x_1, x_2, ---, x_n$, denoted by $B(n)$. The Boolean set of $(n-1)$ variables $x_1, x_2, ---, x_{i-1}, x_{i+1}, ---, x_n$, written $\underline{x}/x_i$, will be denoted by $B(n/i)$.

Definition 2.2: Given a set $S, \phi \subseteq S \subseteq B(n)$, a function $F(\underline{x})$ is said to be based on the set $S$ provided

$$F(\underline{x})\Big|_{\underline{x}=\underline{b}_o} = 1 \quad \text{if and only if } \underline{b}_o \in S.$$

On the other hand, if a function $F(\underline{x})$ is given, then the set

$$S = \left\{ \underline{b} \,\middle|\, \underline{b} \in B(n) \text{ and } F(\underline{b}) = 1 \right\}$$ is called

the base of the function $F(\underline{x})$ and denoted by $\text{BASE}\left\{F(\underline{x})\right\}$.

## 3. BOOLEAN DIFFERENTIATION

In order to study the effect of change in a variable $x_i$, on a function $F(x_1, x_2, ---, x_n)$ we introduce the concept of decomposition. $F(\underline{x})$ can be decomposed with respect to $x_i$, $1 \leq i \leq n$, as the sum of 3 functions as

$$F = P_i x_i + Q_i \bar{x}_i + R_i \qquad (3.0.1)$$

such that $P_i$, $Q_i$ and $R_i$ are independent of $x_i$ and

$$P_i Q_i = P_i R_i = Q_i R_i = 0 \qquad (3.0.2)$$

Definition 3.1: A function F that is decomposed as stated above, is said to be the decomposition of F with respect to $x_i$, $1 \leq i \leq n$.

It can be shown that the decomposition of F with respect to $x_i$, $1 \leq i \leq n$, is unique. For any point $\underline{x}$ with $\underline{x}/x_i \in \text{BASE}\left\{P_i\right\}$ $1 \leq i \leq n$,

$$F(x) = 1.x_i + 0.\bar{x}_i + 0 = x_i \qquad (D3.1.1)$$

so that $F(\underline{x})$ has the same value as $x_i$ and therefore changes the same way as $x_i$.

<u>Definition 3.2</u>: The <u>direct (or inverse) partial derivative of $F(\underline{x})$ with respect to $x_i$, $1 \le i \le n$,</u> denoted by $\frac{\partial F}{\partial x_i}\left(\text{or } \frac{\partial F}{\partial \bar{x}_i}\right)$ is defined as a function of (n-1) variables $x_1, x_2, ---, x_{i-1}, x_{i+1}, ---, x_n$ that is based on the union of all possible points $\underline{x}/x_i$ in the set $\Sigma(n/i)$ such that

$$F(\underline{x}) = x_i \text{ (or } \bar{x}_i) \qquad \text{(D3.2.1)}$$

The concept of partial derivatives has been reported earlier [33]. We will show some relationships involving the partial derivatives in the following theorem.

<u>Theorem 3.1</u>: The direct and inverse partial derivatives of a function $F(\underline{x})$ with respect to $x_i$, $1 \le i \le n$ satisfy the following relationships:

$$\frac{\partial F}{\partial x_i} = P_i = \left(F(\underline{x})\Big|_{x_i = 1}\right) \cdot \overline{\left(F(\underline{x})\Big|_{x_i=0}\right)} = \frac{\partial \bar{F}}{\partial \bar{x}_i} \qquad \text{(T3.1.1)}$$

$$\frac{\partial F}{\partial \bar{x}_i} = Q_i = \left(F(\underline{x})\Big|_{x_i = 0}\right) \cdot \overline{\left(F(\underline{x})\Big|_{x_i=1}\right)} = \frac{\partial \bar{F}}{\partial x_i} \qquad \text{(T3.1.2)}$$

$$\frac{\partial F}{\partial x_i} \cdot \frac{\partial F}{\partial \bar{x}_i} = 0 \qquad \text{(T3.1.3)}$$

$$F(\underline{x}) = x_i \Leftrightarrow \frac{\partial F}{\partial x_i} = 1 \qquad \text{(T3.1.4)}$$

$$F(\underline{x}) = \bar{x}_i \Leftrightarrow \frac{\partial F}{\partial \bar{x}_i} = 1 \qquad \text{(T3.1.5)}$$

## 4. BOOLEAN DIFFERENTIAL

Boolean differential introduced by Talantsev [28] and further developed by Brown and Young [33], is analogous to the differential of a function in the calculus of real variables and expresses the change in a Boolean function in terms of a change in one of its arguments.

<u>Definition 4.1</u>: dF will denote changes in the value of function F. These changes can be from "0" to "1" or "1" to "0". $dx_i$ or $d\bar{x}_i$ will denote a change in the variable $x_i$. The expression $dF=dx_i$ means that a "positive" (or "negative") change in $x_i$ causes a "positive" (or "negative") change in F. The expression $dF=d\bar{x}_i$ means that a "positive" (or "negative") change in $x_i$ causes a "negative" (or "positive") change in F. In order to relate dF, $dx_i$, $d\bar{x}_i$ and F, we will need to define dF, $dx_i$ and $d\bar{x}_i$, for all i, as entities in a Boolean algebraic system (i.e. as Boolean variables). When dF, $dx_i$ and $d\bar{x}_i$ are treated as such they have Boolean values as defined below:

$$dV = \begin{cases} 0, & \text{implies no change occurring in value of } V \\ 1, & \text{implies a change in value of } V \end{cases} \qquad \text{(D4.1.1)}$$

where V=F or $\bar{F}$ or $x_i$ or $\bar{x}_i$ for any i, $1 \leq i \leq n$.

Note that dV as defined here does not specify the direction of change. dV=1 implies merely a change in its value.

If $dF=f(\underline{x}/x_i).dx_i$ (or $f(\underline{x}/x_i) \,.\, d\bar{x}_i$), then by definition it implies that F changes the same (or opposite) way as $x_i$ changes when $f(\underline{x}/x_i) = 1$.

Consider dF, the change in F, in terms of $x_1$, $x_2$ and $dx_3$, the change in $x_3$ as given below:

$$dF = x_1 x_2 \, dx_3 \tag{D4.1.2}$$

When $$x_1 = x_2 = 1, \tag{D4.1.3}$$

then $$dF = (1 \cdot 1) \cdot dx_3 = dx_3. \tag{D4.1.4}$$

Equation (D4.1.4) by Definition 4.1 can be interpreted to mean that a change in F is the way same as the change in $x_3$ when $x_1 x_2 = 1$.

On the other hand, when

$$x_1 x_2 = 0, \tag{D4.1.5}$$

then $$dF = 0.dx_3 = 0, \tag{D4.1.6}$$

which means that there is no change in F when $x_1 x_2 = 0$ and $x_3$ changes.

<u>Definition 4.2</u>: <u>The Boolean differential of F with respect to $x_i$</u>, $1 \le i \le n$, denoted by $d_i F$, is defined as

$$d_i F = \frac{\partial F}{\partial x_i} \cdot dx_i + \frac{\partial F}{\partial \bar{x}_i} \cdot d\bar{x}_i \tag{D4.2.1}$$

<u>Definition 4.3</u>: The Boolean differential of F with respect to all <u>variables $x_1, x_2, \text{---} x_n$</u> or <u>simply Boolean differential of F</u>, denoted by dF, is defined as

$$dF = \sum_{i=1}^{n} d_i F = \sum_{i=1}^{n} \left( \frac{\partial F}{\partial x_i} dx_i + \frac{\partial F}{\partial \bar{x}_i} d\bar{x}_i \right) \tag{D4.3.1}$$

The Boolean differential of F is useful in analysis as it shows how F is affected by changes in $x_i$, $1 \le i \le n$. In synthesis, it is of interest to address ourselves to the question: "Is it possible to find a function that undergoes changes as a consequence of changes in its arguments in accordance with a given specification?" The answer to this question will be pursued in the next section.

## 5. BOOLEAN INTEGRATION

While designing systems, at times we come across situations when we want the output of a system to change the same way as some of its inputs under certain conditions and the output to change the opposite way as some inputs under other conditions, when the inputs change. In order to specify this desired relationship between the changes in the output in terms of the changes in the inputs, we introduce differential expression defined next.

__Definition 5.1__: A __differential expression__, denoted by dH, is a Boolean expression of the form

$$dH = \sum_{i=1}^{n} (\alpha_i \, dx_i + \beta_i \, d\bar{x}_i) \qquad \text{(D5.1.1)}$$

where in general $\alpha_i$ and $\beta_i$ are functions of the (n-1) variables $x_1, x_2, ---, x_{i-1}, x_{i+1}, ---, x_n$ and $\alpha_i$ and $\beta_i$ are independent of $x_i$ for all i, $1 \le i \le n$.

Observe that since by Theorem 3.1, $\frac{\partial F}{\partial x_i}$ and $\frac{\partial F}{\partial \bar{x}_i}$ are independent of $x_i$, $1 \leq i \leq n$, the Boolean differential of a function $F(\underline{x})$ as given in equation (D4.3.1) is a differential expression; however the converse is not true. For a differential expression to be a differential, there must exist a function such that its differential is the same as the given differential expression. For the expression dH in equation (D5.1.1) to be a differential, there must exist a function $H(\underline{x})$ such that

$$\alpha_i = \frac{\partial H}{\partial x_i} \qquad \text{(D5.1.2)}$$

and

$$\beta_i = \frac{\partial H}{\partial \bar{x}_i} \qquad \text{(D5.1.3)}$$

for all i, $1 \leq i \leq n$.

Given differential expression dH as described in (D5.1.1), in order to determine whether a function F exists that changes due to changes in its arguments as specified in the differential expression dH, we need the following definitions.

<u>Definition 5.2</u>: F is said to be the <u>exact integral of dH</u>, denoted by $\int_E dH$, and dH is said to be exactly integrable if

$$dH = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i) \qquad \text{(D5.2.1)}$$

and for all i, $1 \leq i \leq n$ $\frac{\partial F}{\partial x_i} = \alpha_i$ and $\frac{\partial F}{\partial \bar{x}_i} = \beta_i$. (D5.2.2)

Let us now determine the changes in C in terms of changes in $x_1$ and $x_2$.

$$\frac{\partial c}{\partial x_1} = \bar{y} \quad \text{and} \quad \frac{\partial c}{\partial \bar{x}_1} = 0. \qquad \text{(E6.1.6)}$$

$$\frac{\partial c}{\partial x_2} = y \quad \text{and} \quad \frac{\partial c}{\partial \bar{x}_2} = 0. \qquad \text{(E6.1.7)}$$

$$\frac{\partial c}{\partial y} = \bar{x}_1 . x_2 \quad \text{and} \quad \frac{\partial c}{\partial \bar{y}} = x_1 . \bar{x}_2 . \qquad \text{(E6.1.8)}$$

Observe that the clock transitions described by equations (E6.1.6) and (E6.1.7) are the desired transitions whereas those described by equation (E6.1.8) are the ones not specified in the differential expression (E.6.1.1). However these transitions cannot occur as can be seen from what follows. Consider the first of the equations in (E6.1.8). When $\bar{x}_1 x_2 = 1$ and y changes from 0 to 1, the clock will go through a positive transition. However y changes from 0 to 1 only if it is preceded by a change in $x_1$ from 0 to 1 so that when y changes from 0 to 1, $x_1$ cannot be 0. Hence the change in y cannot trigger the flipflop. Similarly the transition described by the second equation in (E6.1.8) cannot cause a clock transition.

Observe that every time a positive transition in the clock occurs, the state changes. Hence the input $D_i$ of the D-flipflop to be used is given by

$$D_i = \bar{y} \qquad \text{(E6.1.9)}$$

Equations (E6.1.5) and (E6.1.9) lead to the network realization in Figure 6.3

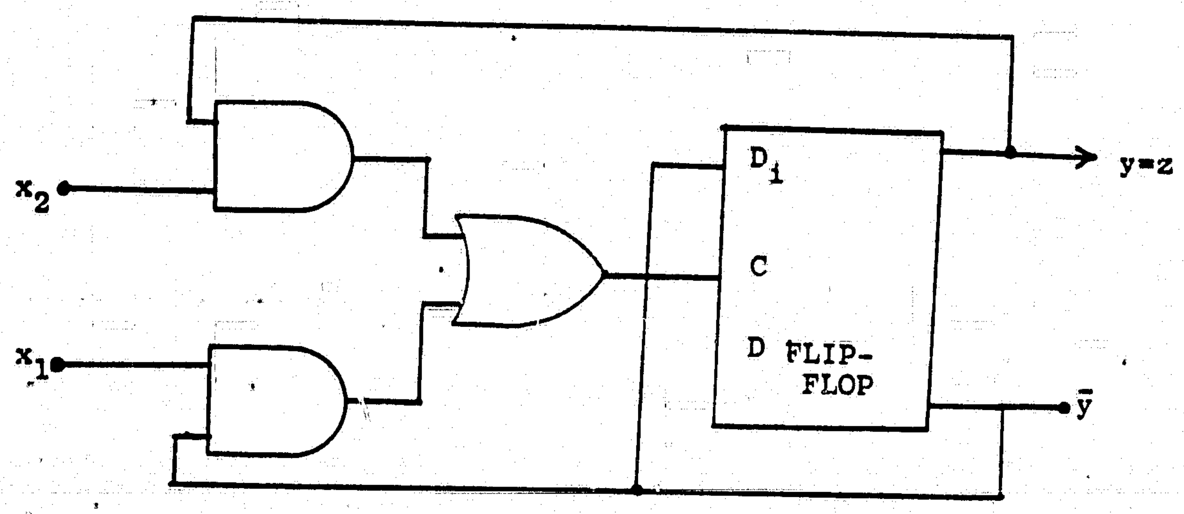


Figure 6.3

A possible hazard can be prevented by adding the term $(x_1x_2)$ to the OR-gate in Figure 6.3. It can be shown that this does not cause any undesired clock transitions.

It should be noted here that if a compatible integral of a clock differential expression has transitions which are not specified in the differential expression and which can occur, it poses no problem, since corresponding to those transitions we can provide the appropriate value(s) of the next state variable(s) to the input(s) $D_i$ of the D flipflop(s).

## 7. POTENTIAL FOR FURTHER APPLICATIONS

The traditional methods of the anlaysis and the synthesis of logic circuits are based on Boolean algebra and utilize the functional relationships between the output and input values(or levels). Analysis and design by Boolean calculus focuses on the changes in the output function in terms of changes in input arguments. The new concepts of integration, the ways of integrating a Boolean differential and the necessary and sufficient condition for its compatible integrability open an avenue to new areas of applications. Because of the nature of these applications, the specification in terms of the changes in the output of a system or a subsystem as a consequence of the changes in the inputs of the system or the subsystem, is more significant and desirable than that in terms of the functional relationship between output and input values. It should be noted here that clock-triggered flipflops, synchronous counters and many other MSI and LSI circuits are sensitive to input transitions. It is premature to predict long term utility of Boolean calculus, but the potential benefits dictate a need for further investigation [5, 38-40].

## 8. CONCLUSION

Boolean calculus is a powerful tool for analysis as well as synthesis of logic circuits. The use of Boolean integration in synthesis of asynchronous circuits using clock-triggered flipflops has led to circuits which require fewer flipflops and logic gates than circuits synthesized using conventional methods [5 , 38-40] ,thus reducing complexity, cost and size and improving reliability.

Earlier methods to realize a function from the specified changes in its value in terms of changes in its arguments do not possess the simplicity and ease that the integration method presented here does. The concept of a compatible integral was introduced in order to generalize the concept of the exact integral and recognizing the fact that we do have don't-care conditions and/or transitions in real-life situations. Moreover, if the exact integral does not exist for a specified differential but a compatible integral does, then the undesired transitions (changes) in the integral may be inhibited using a simple logic circuit. Integration by parts is a further generalization of compatible integration, which has possible applications in logic circuits.

## 9. ACKNOWLEDGEMENTS

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# Appendix II

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## APPLICATION OF BOOLEAN CALCULUS TO DIGITAL SYSTEM DESIGN



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### ABSTRACT

Conventional methods for synthesizing asynchronous sequential systems do not use clock-triggered flipflops. It has been shown that synthesis techniques for such systems, which utilize edge-sensitive flipflops lead to networks which require fewer flipflops and logic gates than those obtained by conventional techniques. A formal procedure for synthesis of asynchronous sequential systems using comercially available edge-sensitive flipflops, is given.

### 1. INTRODUCTION

In conventional asynchronous level-mode sequential system design direct emphasis is placed on relationship between outputs and inputs in terms of their levels only, and the possibility of using edge sensitiveness property of logic elements is not utilized. Smith and Roth have shown [6,5] that if edge-sensitive flipflops are used in the design of an asynchronous system and the edge-sensitiveness property is judiciously taken advantage of, then in many cases it leads to a realization that requires less flipflops and logic gates than conventional method does for a given system. Smith and Roth technique [6,5] utilizes a "general model of edge-sensitive flipflop" in their approach. The method proposed in this paper is applicable to any commercially available clock-triggered flipflop that responds to a clock transition (positive or negative).

### 2. DIFFERENTIAL MODE MODEL

Definition 2.1: A Fundamental Mode Asynchronous system

(D2.1.1) FMAS $\triangleq (I,S,O,f,g)$ where

(D2.1.2) $I \triangleq$ set of $p$ distinct input conditions = $(I_j)$

(D2.1.3) $S \triangleq$ set of states of the system = $(S_j)$

(D2.1.4) $O \triangleq$ set of outputs = $(O_j)$

(D2.1.5) $f \triangleq$ output function $\triangleq f(S_k,I_j)$, $\forall_j$ & $k$ and

(D2.1.6) $g \triangleq$ next state function $= g(S_k,I_j)$, $\forall_j$ & $k$ will be assumed.

It will further be assumed that only one state variable and only one input variable is allowed to change at a time.

In order to make it convenient to express the next state and output in terms of the change in the inp[illegible] and the present state, we will transform the FMA system to a Differential Mode model defined below. This is comparable to the DM Machine of Smith and Roth [5,6] but really different than that.

Definition 2.2: Given a fundamental mode asynchronous system FMAS, a Differential Mode System, DMS will be defined as a 6-tuple as given below:

(D2.2.1) DMS = $(I',I^{*\prime},S',O',f',g')$ where

(D2.2.2) $I'=I$,

(D2.2.3) $I^{*\prime} = ((I_j,I_k) \mid \forall_{j,k})$

(D2.2.4) $S' \triangleq S$

(D2.2.5) $f' \triangleq$ output function of DMS

(D2.2.6) $g' \triangleq$ next state function of DMS

The function $g'$ is related to the function of the FMA system as shown below:

(D2.2.9)

$$g'(S_h,I_j,I_k) = \begin{cases} S_i, \text{ if } g(S_h,I_j)=S_h, g(S_h,I_k)=S_i \text{ and } g(S_i,I_k)=S_i \\ S_i, \text{ if } (S_h,I_j)=S_h \text{ and there exist } S_{i1},S_{i2}, \text{---} S_{in} \text{ \& } S_i \\ \quad \text{such that } g(S_h,I_k)=S_{i1}, \\ \quad g(S_{i1},I_k)=S_{i2}, \text{---}, g(?_{in},I_k)=S_i \\ \quad \text{and } g(S_i,I_k)=S_i. \end{cases}$$

$$\begin{cases} —, & \text{if } g(S_h,I_j) = S_h \ \& \ g(S_h,I_k) = —— \\ —, & \text{if } g(S_h,I_j) = S_h \text{ and there exist} \\ & S_{i1},S_{i2},---,S_{in} \text{ such that} \\ & g(S_h,I_k) = S_{i1},\ g(S_{i1}, I_k) = S_{i2} \\ & g(S_{i2},I_k) = S_{i3},---,g(S_{in},I_k) = —— \\ —, & \text{if } g(S_h,I_j) \neq S_h \end{cases}$$

The function $f'(S_h,I_j,I_k)$ is related to the function $f(S_k,I_j)$ of the FMA system as shown below:

(D2.2.10) $f'(S_h,I_j, I_k)$

$$= \begin{cases} f(S_i, I_k), & \text{if } g'(S_h,I_j, I_k)=S_i \\ ——, & \text{if } g'(S_h,I_j,I_k) \text{ is unspecified} \end{cases}$$

Before we develop procedure for synthesizing the asynchronous sequential system described by the equations (D2.2.1) through (D2.2.10), we will assume that the FMA system (and hence DM system is amenable to single variable - change state assignment. Let us further assume that the system has $n$ input variables $X_1,X_2---,X_n$ $m$ state variables $Y_1$, $Y_2$---, $Y_m$ and hence $m$ clock-triggered flipflops that respond to positive transitions. We will, therefore, need to realize clock functions, say C 's such that whenever an input change occurs then one (and only one) of the clock functions goes through a positive transition providing a proper state transition.

## 3. A DIFFERENTIAL MODE SYSTEM

### EXAMPLE 3.1

Consider the FMA system described by the reduced flow table given in Figure 3.1, which is equivalent to the DM system given in Figure 3.2.

| | $X_1X_2$ 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| (A,B) 1 | 1,0 | 1,0 | 3,- | 2,- |
| (C,F) 2 | 2,1 | 1,- | 4,- | 2,1 |
| (D,G) 3 | 2,- | 3,1 | 3,1 | 2,- |
| (E,H) 4 | 1,- | 1,- | 4,0 | 4,0 |

Fig. 3.1

| $X_1X_2$ | 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|
| 1 | 2,1 | 1,0 | 3,1 | 1,0 | - | - | - | - |
| 2 | 2,1 | 1,0 | - | - | - | - | 2,1 | 4,0 |
| 3 | - | - | 3,1 | 2,1 | 3,1 | 2,1 | - | - |
| 4 | - | - | - | - | 1,0 | 4,0 | 1,0 | 4,0 |

Figure 3.2

Using the conventional methods to reduce flow tables for FMA systems, the DM table can reduced as shown in Figure 3.3.

| $X_1X_2$ | 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|
| (1,4)A | B,1 | A,0 | B,1 | A,0 | A,0 | A,0 | A,0 | A,0 |
| (2,3)B | B,1 | A,0 | B,1 | B,1 | B,1 | B,1 | B,1 | A,0 |

Figure 3.3

The reduced DM system has only two states. Let y=0 and y=1 be the assignments for states A and B respectively.

Observe that if y=0, the flipflop must change its state, when
(1) $X_2 = 0$ and $X_1$ changes from 0 to 1 or
(2) $X_2 = 1$ and $X_1$ changes from 0 to 1.
If y = 1, the flipflop must change when
(1) $X_1 = 0$ and $X_2$ changes from 0 to 1 or
(2) $X_1 = 1$ and $X_2$ changes from 0 to 1

This tells us when the clock should go through a positive transition. The desired changes in clock function in terms of changes in $X_1$ and $X_2$ can be described by the differential expression (E3.1.1) below:

(E3.1.1) $$dc = \left(\bar{y}\,\bar{X}_2dx_1+X_2dx_1\right)+y\left(\bar{X}_1dx_2+X_1dx_2\right)$$
$$= \bar{y}\ dx_1 + y\ dx_2$$

It can be shown that dc is compatibly integrable and a compatible integral of dc is

(E3.1.2) $$\int_c dc = \bar{y}x_1 + yx_2 \text{ (See Def. 4.4)}$$

Let us, then, try

(E3.1.3) $C_1 = \bar{y}x_1 + yx_2$ as the input to the clock pin of a flipflop to be used.
Then
(E3.1.4) $dc_1=\bar{y}dx_1+ydx_2+\bar{x}_1x_2dy+x_1\bar{x}_2d\bar{y}$

so that transitions $(\bar{x}_1 x_2 dy)$ and $(x_1 \bar{x}_2 d\bar{y})$ which are not specified by equation (E3.1.1) may be present. However a close examination at Figure 3.3 reveals the fact that when y=0 and input changes to $x_1 x_2 = 01$, then y does not change to 1 so that $(\bar{x}_1 x_2 dy)$ is a transition that cannot occur. Similarly $(x_1 \bar{x}_2 d\bar{y})$ cannot occur either. Hence the clock function $C_1$ will provide exactly those transitions which are specificed by equation (E3.1.1). Hence the circuit requires only one (toggle) flipflop, with the function given by $C_1$ as input to its clock pin and output of the flipflop (y) being identified as the output z of the system. See Figure 3.4 on page 4.

## 4. REVIEW OF BOOLEAN CALCULUS

The definitions and theorems given here are described in references 1, 2, 3 and 7.

**Definition 4.1:**

(4.1.1) $dx_i = 1$, when $X_i$, $1 \le i \le n$, changes from 0 to 1 or from 1 to 0

$dx_i = 0$, when $X_i$ does not change at all.

dF will be defined similarly

(4.1.2) $dF = dX_i$ by definition implies that when $X_i$ changes from 0 to 1 (or 1 to 0), so does F change from 0 to 1 (or 1 to 0).

Differential expression, denoted by $d\xi$, will be defined as

(D4.2.1) $$d\xi = \sum_{i=1}^{n} (\alpha_i dX_i + \beta_i d\bar{X}_i)$$

where $\alpha_i$ and $\beta_i$, $1 \le i \le n$ are functions of $X_1, X_2, \ldots, X_{i-1}, X_{i+1}, \ldots X_n$ (and independent of $X_i$) and only one of the variables $X_1, X_2, \ldots X_n$ is allowed to change at a time.

**Definition 4.3:** The integral of zeroth order, written as $\int_0 d\xi$, of the Boolean expression

(D4.3.1) $$d\xi = \sum_{i=1}^{n} (\alpha_i dx_i + \beta_i d\bar{x}_i)$$

is given by

(D4.3.2) $$\int_0 d\xi = \sum_{i=1}^{n} (\alpha_i \bar{X}_i + \beta_i X_i)$$

and the integral of first order, written as $\int_1 d\xi$, of the expression $d\xi$ in equation (D4-3-1) is given by

(D4.3.3) $$\int_1 d\xi = \sum_{i=1}^{n} (\alpha_i X_i + \beta_i \bar{X}_i).$$

**Definition 4.4:** A given differential expression d given in (D4.3.1) is said to be compatibly integrable if there exists a function F such that

(D4.4.1) $$\frac{\partial F}{\partial X_i} \ge \alpha_i \text{ and } \frac{\partial F}{\partial \bar{X}_i} \ge \beta_i \text{ for all } i,$$

$1 \le i \le n$. If F satisfying equation (D4.4.1) does exist then F is called a compatible integral of $d\xi$. (See Appendix).

**Theorem 4.1:** The necessary and sufficient condition for compatible integrability of given differential expression

$$d\xi = \sum_{i=1}^{n} (\alpha_i dX + \beta_i d\bar{X}_i) \text{ is that}$$

$$\left(\int_0 d\xi\right) \cdot \left(\int_1 d\xi\right) = 0$$

**Theorem 4.2:** If a given differential expression d is integrable, then a compatible of $d\xi$ is given by

$$\int_c d\xi = \int_1 d\xi + K \text{ where } d\xi K \le \overline{\int_0 d\xi + \int_1 d\xi}$$

## 5. SYNTHESIS PROCEDURE

Due to space limitation, it is not possible to outline here a general procedure, in details, for synthesizing an asynchronous sequential system using clock-triggered flipflops and Boolean calculus. Only a brief sketch of the procedure is given here in what follows.

Given an FMAS table which is already reduced, it is first transformed into DMS table. It has been shown that the latter can always be realized as a network consisting of edge-triggered (clock-triggered) flipflops and Boolean calculus. From the DMS table, differential expression [1,2,3, 7] for each clock function is determined taking into account what changes in clock functions are necessary in order to bring about changes in the state of the corresponding flipflop. These differential expressions are guaranteed to be integrable other inputs (such as S-R or J-K, if any) to the flipflops are determined by looking at the nature of next states in the entries in the table, thus a complete network realization is obtained.

Quite often the DMS table is further reducible as shown in the previous example. If the reduced DMS table is realizable using clock-triggered flipflop, a considerable saving in the number of flipflops and logic gates results. Synthesis procedure for a reduced DMS table is similar to the procedure just outlined, but a number of relationships have to be checked before the procedure can be successfully applied. Due to space limitations, the detailed procedure cannot be described here.

## 6. CONCLUSION

Design of asynchronous level-mode sequential systems using clocked flipflops has been known for a long time. However, such design using simpler circuits has been essentially limited to those cases where the logic designer possesses sufficient experience and inspiration to intuitively obtain such an implementation. Smith and Roth [5,6] presented a formal approach to realize asynchronous level-mode sequential system using "general model of edge-sensitive flipflop" [5,6]. The formal synthesis procedure proposed here is applicable to synthesis of such systems using any commercially available clock-triggered flipflops.

We have shown that any asynchronous level-mode sequential system could be realized using the proposed approach. In many cases this approach leads to designs which are less complex, less costly, more reliable and smaller in size than those obtained using conventional design techniques. In the worst case the complexity of the design obtained by the proposed approach are comparable to that obtained by conventional techniques.

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## APPENDIX

Definition A1: For a Boolean function $F(X_1, X_2, ---, X_n)$, of $n$ variables $X_1, X_2, ---X_n$ Boolean differential of F, denoted by dF is defined as

$$\text{(A1.1)} \quad dF = \sum_{i=1}^{n} \left( \frac{\partial F}{\partial X_i} dX_i + \frac{\partial F}{\partial \overline{X_i}} d\overline{X_i} \right)$$

The summation in Equation (A1.1) is with respect to the inclusive OR, and the partial derivatives are defined by

$$\text{(A1.2)} \quad \frac{\partial F}{\partial X_i} = F(\underline{x})|_{X_i=1} \cdot F(\underline{x})|_{X_i=0} \quad \text{and}$$

$$\text{(A1.2)} \quad \frac{\partial F}{\partial \overline{X_i}} = F(\underline{x})|_{X_i=0} \cdot F(\underline{x})|_{X_i=1}$$

With the interpretation given in Definition 4.1, equation A1.1 completely describes changes in F due to changes in $X_i$, $1 \leq i \leq n$.

Definition A2: If a function F exists such that dF=dξ, then the differential expression in D4.2.1 is exactly integrable.

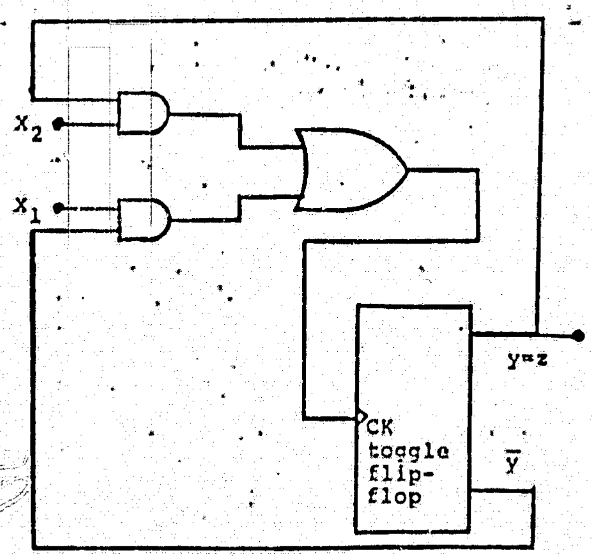


Figure 3.4

# Appendix III

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### SYNTHESIS OF ASYNCHRONOUS SEQUENTIAL SYSTEMS USING BOOLEAN CALCULUS


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#### Abstract

Recently there has been considerable interest in synthesis of asynchronous sequential systems using clock-triggered flipflops [2-7]. It has been shown [2,3] that synthesis techniques for such systems which utilize edge-sensitive (clock-triggered) flipflops lead to networks which, in many cases, require fewer flipflops and logic gates and which are less expensive and more reliable than those obtained by conventional techniques. The proposed paper aims at developing formal procedures for synthesis of asynchronous sequential systems using commercially available edge-sensitive flipflops.


#### 1. Introduction

In conventional asynchronous level-mode sequential system design direct emphasis is placed on relationship between outputs and inputs in terms of their levels only, and the possibility of using edge sensitiveness property of logic elements is not utilized. Smith and Roth have shown [3] that if edge-sensitive flipflops are used in the design of an asynchronous system and the edge-sensitiveness property is judiciously taken advantage of, then in many cases it leads to a realization that requires less flipflops and logic gates than conventional method does for a given system. The Smith and Roth technique [3] utilizes a "general model of edge-sensitive flipflop" in their approach. The method proposed in this paper is applicable to any commercially available clock-triggered flipflop that responds to a clock transition (positive or negative).

#### 2. Differential Mode Model

Definition 2.1: A Fundamental Mode Asynchronous system

(D2.1.1) FMAS = $(I, S, O, f, g)$ where

(D2.1.2) $I$ = set of p distinct input conditions = $\{I_j\}$

(D2.1.3) $S$ = set of q states of the system = $\{S_j\}$

(D2.1.4) $O$ = set of outputs = $\{O_j\}$

(D2.1.5) $f$ = output function = $f(S_k, I_j), \forall j \,\&\, k$ and

(D2.1.6) $g$ = next state function = $g(S_k, I_j), \forall_{j\&k}$

will be assumed.

It will, further, be assumed that only one input variable is allowed to change at a time and that the system has n input variables $X_1, X_2, \ldots X_n$ and m state variables $Y_1, Y_2, \ldots, Y_m$. In order to facilitate the expressing of the next state and output in terms of the change in the input and the present state, we will transform the FMA system to a Differential Mode System defined below:

Definition 2.2: Given a fundamental mode asynchronous system FMAS, a Differential Mode System (DMS) will be defined as a 6-tuple as given below:

(D2.2.1) DMS = $(I', I^{*\prime}, S', O', f', g')$ where

(D2.2.2) $I' = I$,

(D2.2.3) $I^{*\prime} = \{(I_j, I_k), \forall_{j,k}, j \neq k\}$

(D2.2.4) $S' = S$

(D2.2.5) $f'$ = output function of DMS

(D2.2.6) $g'$ = next state function of DMS

The function $g'$ is related to the function $g$ of the FMA system as shown below:

(D2.2.9) $g'(S_h, I_j, I_k)$

$$= \left[\begin{array}{l} S_i, \text{ if } g(S_h,I_j) = S_h,\ g(S_h,I_k) = S_i \\ \qquad \text{and } g(S_i,I_k) = S_i; \\ S_i, \text{ if } g(S_h,I_j) = S_h \text{ and there exists} \\ \qquad S_{i1}, ---, S_{in} \& S_i \text{ such that} \\ \qquad g(S_h,I_k) = S_{i1}, \\ \qquad g(S_{i1},I_k) = S_{i2}, ---, g(S_{in},I_k) = S_i \\ \qquad \text{and } g(S_i,I_k) = S_i; \\ -, \text{ if } g(S_h,I_j) = S_h \,\&\, g(S_h,I_k) = -; \\ -, \text{ if } g(S_h,I_j) = S_h \text{ and there exist} \\ \quad S_{i1}, S_{i2}, ---, S_{in} \text{ such that} \\ \quad g(S_h,I_k) = S_{i1},\ g(S_{i1},I_k) = S_{i2} \\ \quad g(S_{i2},I_k) = S_{i3}, ---, g(S_{in},I_k) = -; \\ -, \text{ if } g(S_h,I_j) \neq S_h. \end{array}\right.$$

The function $f'(S_h, I_j, I_k)$ is related to the function $f(S_k, I_j)$ of the FMA system as shown below:

(D2.2.10)
$$f'(S_h, I_j, I_k) = \begin{cases} \overline{f(S_i, I_k)}, \text{ if } g'(S_h, I_j, I_k) = S_i \\ -, \text{ if } g'(S_h, I_j, I_k) \text{ is unspecified} \end{cases}$$

Definition 2.3:

(D2.3.1)
$$dX_i = \begin{cases} 1, \text{ when } X_i,\ 1 \le i \le n, \text{ changes from 0 to 1 or from 1 to 0} \\ 0, \text{ when } X_i \text{ does not change at all} \end{cases}$$

$dF$ will be defined similarly.

(D2.3.2) $dF = dX_i$ by definition implies that when $X_i$ changes from 0 to 1 (or 1 to 0), so does $F$ change from 0 to 1 (or 1 to 0).

In order to relate changes in $F$ due to changes in $X_i$ under different conditions we will treat $dF$ and $dX_i$, $1 \le i \le n$ as entities in Boolean algebra having values of 0 or 1 as defined in equation (D2.3.1). Consider the equation

(D2.3.3) $$dF = (X_2 \cdot X_3)dX_1 + (X_1 \cdot X_2)d\overline{X}_3.$$

When $X_2 = X_3 = 1$ and $X_1$ is changing, then $d\overline{X}_3 = 0$ and $dF = dX_1$ so that $F$ changes the same way as $X_1$ changes. Similarly when $X_1 = X_2 = 1$ and $X_3$ changes, then $dF = d\overline{X}_3$ and $F$ changes the same way as $X_3$ changes

Differential expression, denoted by $dH$, will be defined as

(D2.3.4) $$dH = \sum_{i=1}^{n}\left(\alpha_i dX_i + \beta_i d\overline{X}_i\right)$$

where $\alpha_i$ and $\beta_i$, $1 \le i \le n$ are functions of $X_1, X_2, ---X_{i-1}, X_{i+1}, ---, X_n$ (and independent of $X_i$) and only one of the variables $X_1, X_2, ---, X_n$ is allowed to change at a time.

Differential expression as given in (D2.3.4) will be used to describe changes in clock functions in terms of changes in input and state variables.

The following definitions, relationships and theorems have been reported earlier [1,4,7] and will be presented here briefly for the sake of completeness and convenience of reference.

Definition 2.4: For a Boolean function $F(X_1, X_2, ---, X_n)$, of n variables $X_1, X_2, ---, X_n$ Boolean differential of F, denoted by $dF$, is defined as

(D2.4.1) $$dF = \sum_{i=1}^{n}\left(\frac{\partial F}{\partial X_i}dX_i + \frac{\partial F}{\partial \overline{X}_i}\ \overline{dX_i}\right).$$

The summation in Equation (D2.4.1) is with respect to the inclusive OR, and the partial derivatives are defined by

(D2.4.2) $$\frac{\partial F}{\partial X_i} = F(\underline{x})\big|_{X_i=1} \cdot \overline{F(\underline{x})\big|_{X_i=0}}\ .$$

and

(D2.4.3) $$\frac{\partial F}{\partial \overline{X}_i} = F(\underline{x})\big|_{X_i=0} \cdot \overline{F(\underline{x})\big|_{X_i=1}}\ .$$

With the interpretation given in Definition D2.3, equation (D2.4.1) completely describes changes in $F$ due to change in variable $X_i$, $1 \le i \le n$.

Definition 2.5: The integral of zeroth order, written as $\int_0 dH$, of the Boolean expression

(D2.5.1) $$dH = \sum_{i=1}^{n}\left(\alpha_i dX_i + \beta_i d\overline{X}_i\right)$$

is given by

(D2.5.2) $$\int_0 dH = \sum_{i=1}^{n}\left(\alpha_i \overline{X}_i + \beta_i X_i\right)$$

and the integral of first order, written as $\int_1 dH$, of the expression $dH$ in equation (D2.5.1) is given by

(D2.5.3) $$\int_1 dH = \sum_{i=1}^{n}\left(\alpha_i X_i + \beta_i \overline{X}_i\right).$$

Definition 2.6.: A given differential expression $dH$ given in (D2.5.1) is said to be compatibly integrable if there exists a function $F$ such that

(D2.6.1) $$\frac{\partial F}{\partial X_i} \supseteq \alpha_i \text{ and } \frac{\partial F}{\partial \overline{X}_i} \supseteq \beta_i$$

for all i, $1 \le i \le n$. If $F$ satisfying equation (D2.6.1) does exist, then $F$ is called a compatible integral of dH. The differential expression is said to be exactly integrable if there exists function $F$ such that

(D2.6.2) $$dF = dH$$

If $F$ satisfying the above equation does exist, then $F$ is called the exact integral of dH.

Theorem 2.1: The necessary and sufficient condition for compatible integrability of a given differential expression

(T2.1.1) $$dH = \sum_{i=1}^{n}\left(\alpha_i dX_i + \beta_i d\overline{X}_i\right)$$

is that

(T2.1.2) $$\int_0 dH \cdot \int_1 dH = 0$$

Theorem 2.2: If a given differential expression $dH$ is integrable, then a compatible integrable of $dH$ is given by

(T2.2.1) $$\int_0 dH = \int_1 dH + K \text{ where}$$

(T2.2.2) $$K \subseteq \overline{(\int_0 dH + \int_1 dH)}$$

## 3. Example

Before going into a formal synthesis procedure, we will outline the approach with an example. Consider the FMA system described by Figure 3.1.

| | $X_1X_2$ 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| A | A,1 | B,- | D,- | A,0 |
| B | B,0 | B,1 | C,- | A,- |
| C | B,- | C,0 | C,1 | D,- |
| D | A,- | C,- | D,0 | D,1 |

Fig. 3.1

On transforming the system, we get the DMS table in Figure 3.2.

| | $X_1X_2$ 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|
| A | A,0 | B,1 | - | - | - | - | A,1 | D,0 |
| B | A,0 | B,1 | C,1 | B,0 | - | - | - | - |
| C | - | - | C,1 | B,0 | C,0 | D,1 | - | - |
| D | - | - | - | - | C,0 | D,1 | A,1 | D,0 |

Fig. 3.2

| $Y_1Y_2$ | $X_1X_2$ 00 10 | 00 01 | 01 11 | 01 00 | 11 01 | 11 10 | 10 00 | 10 11 |
|---|---|---|---|---|---|---|---|---|
| (A)00 | 00,0 | 01,1 | - | - | - | - | 00,1 | 10,0 |
| (B)01 | 00,0 | 01,1 | 11,1 | 01,0 | - | - | - | - |
| (C)11 | - | - | 11,1 | 01,0 | 11,0 | 10,1 | - | -- |
| (D)10 | - | - | - | - | 11,0 | 10,1 | 00,1 | 10,0 |

Fig. 3.3

Let us assume that D-flipflops will be used and that the flipflops respond to the positive edge of the clock pulse.

Observe that in the first row, the state changes when $X_1X_2$ changes from 00 to 01 and from 10 to 11, that is to say that the state changes when transitions denoted by $\overline{X}_1dX_2$ and $X_1dX_2$ occur. Taking into account all the rows, we need the clock function to go through positive transitions whenever the transitions indicated on the right hand side of equation (E3.1) occur.

(E3.1) $$dC = \bar{y}_1\bar{y}_2(\bar{x}_1dx_2 + x_1dx_2) + \bar{y}_1y_2(\bar{x}_2dx_1 + x_2dx_1) + y_1y_2(\bar{x}_1d\bar{x}_2 + x_1d\bar{x}_2) + y_1\bar{y}_2(x_2d\bar{x}_1 + \bar{x}_2d\bar{x}_1)$$

By Theorem 2.1 dC is compatibly integrable and by Theorem 2.1, a compatible integral of dC, say $C_1$, is given by

(E3.2) $$C_1 = \bar{y}_1\bar{y}_2x_2 + \bar{y}_1y_2x_1 + y_1y_2\bar{x}_2 + y_1\bar{y}_2\bar{x}_1$$

In fact $C_1$ is an exact integral of dC with respect to variables $x_1$ and $x_2$ so that $dC_1$ = dC if the transitions in $dC_1$ due to changes in $y_1$ or $y_2$ are ignored. Whenever one of the transitions on the right hand side of equation dC does occur, then $y_1$ or $y_2$ will change. However, it can be shown that this change in $y_1$ or $y_2$ will not cause a positive transition in $C_1$.

| $y_1y_2$ | $X_1X_2$ 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| | - | 0 | 1 | - |
| | - | - | 1 | 0 |
| | 0 | - | - | 1 |
| | 0 | 1 | - | - |

Figure $D_{11}$ 3.4

| $y_1y_2$ | $X_1X_2$ 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| | - | 1 | 0 | - |
| | - | - | 1 | 0 |
| | 1 | - | - | 0 |
| | 0 | 1 | - | - |

Figure $D_{12}$ 3.5

$D_{11}$ and $D_{12}$ in Figures 3.4 and 3.5 respectively give the values of the inputs to the D-flipflops.

Observe that when $y_1y_2$=00, then positive transitions occur only when $X_2$ changes from 0 to 1 regardless of the value of $X_1$. Hence when $X_2$ changes from 1 to 0, regardless of the value of $X_1$, the value of the next state is left unspecified. Similarly it can be shown that every row has two unspecified entries in the K-maps for $D_{11}$ as well as $D_{12}$. From these maps we have

(E3.3) $$D_{11} = x_1x_2 + x_1y_1 + x_2y_1 \quad \text{and}$$

(E3.4) $$D_{12} = \bar{x}_1x_2 + \bar{x}_1y_2 + x_2y_2.$$

The output function, z, is obtained as

(E3.5) $$z = \overline{(X_1 \odot Y_2)} + (X_2 \odot Y_1)$$

Equation (E3.2) describes the expression corresponding to the combinational network whose output would be connected to the clock pins of both the D-flipflops. $D_{11}$ and $D_{12}$ defined in equations (E3.3) and (E3.4) are the expression for the combinational networks whose outputs would be connected to input pins $D_{11}$ and $D_{12}$ of the D-flipflops 1 and 2 respectively [See Appendix].

## 4. Realizability

In this section we will give results, without proof, pertaining to realizability of an asynchronous fundamental-mode (FMA) system using clock-triggered flipflops and employing Boolean calculus.

Theorem 4.1: If a differential mode system derived from an FMA system has the same number of states as the latter, then the differential mode system (DMS) is realizable using clock triggered flipflops and other logic gates.

**Theorem 4.2:** If the DMS table obtained from an already-reduced FMAS table is reduced further (if it is reducible), then the reduced table is realizable using clock-triggered flipflops, if the table is output- and next-state-unambiguous. [The terms "output-unambigous" and "next-state-unambiguous" are defined in reference 7 and will be defined in Appendix at the end of this paper, if space permits.]

## 5. Synthesis Procedure

Given an FMAS table, the procedure for synthesizing the system using D-flipflops would be as follows:

(1) Transform the given FMA system table to a DMS table using relationships given in Definition 2.2. Assign codes to the states.

(2) For every entry in the DMS table that is specified and that is different than the 'present' state corresponding to the row in which it lies, obtain a differential term corresponding to its column to form a Boolean differential expression, dC, for the CLOCK function.

(3) Find a compatible integral, say $C_1$, of the differential expression dC obtained in step (2).

(4) Find Boolean differential, $dC_1$, of $C_1$.

(5) Corresponding to every input change indicated by $dC_1$ that causes $C_1$ to change from 0 to 1, and every 'present' state, determine the 'next' state using the DMS table. For input changes not specified in the Boolean differential $dC_1$, leave the 'next' entry unspecified. Based on this mapping, determine the K-maps for the expressions corresponding to the input to D-flipflops denoted by $D_{in',j}$'s.

(6) Determine the output function Z in terms of $X_i$'s and $Y_j$'s as is usually done.

Observe that the CLOCK function $C_1$ obtained in step (3) is the common input expression for the clock pins of all the D-flipflops.

If the DMS table derived from an already-reduced FMAS table is further reduced (if it is reducible), then the reduced table is realizable using clock-triggered flipflops if the conditions specified in Theorem 4.2 are satisfied. Synthesis procedure for such a class of system will not be given here due to space limitations.

## 6. Conclusion

A method has been presented that uses clock-triggered flipflops in synthesis of fundamental-mode asynchronous systems. The method employs Boolean Calculus. The method leads to a network that requires fewer IC packages than those required by a network arrived at using conventional methods, thus leading to reduction in cost, complexity of network and power consumed by it.

## 8. Acknowledgements

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## Appendix

**Definition A.1:** A DM system table is said to be level-wise output-unambiguous, if there exists no input conditions $I_i$, $I_j$, $I_k$ and states $S_a$ and $S_b$, $I_i$ and $I_k$ being adjacent, $I_j$ and $I_i$ being adjacent, $I_j$ and $I_k$ not necessarily distinct and $S_a$ and $S_b$ not necessarily distinct, such that $g'(S_a, I_j, I_i)$, $g'(S_b, I_k, I_i)$, $f'(S_a, I_j, I_i)$ and $f'(S_b, I_k, I_i)$ are defined and

(A.1.1) $g'(S_a, I_j, I_i) = g'(S_b, I_k, I_i) = S_c$ (say)

(A.1.2) $f'(S_a, I_j, I_i) = O_{jc} \neq O_{kc} = f'(S_b, I_k, I_i)$.

| | $I_j$ / $I_i$ | $I_k$ / $I_i$ |
|---|---|---|
| $S_a$ (or $S_b$) | $S_c, O_{jc}$ | $S_c, O_{kc}$ |

| | $I_j$ / $I_i$ | $I_k$ / $I_i$ |
|---|---|---|
| $S_a$ | $S_c, O_{jc}$ | |
| $S_b$ | | $S_c, O_{kc}$ |

| | $I_j = I_k$ / $I_i$ |
|---|---|
| $S_a$ | $S_c, O_{jc}$ |
| $S_b$ | $S_c, O_{kc}$ |

Figure A.1

<u>Definition A.2</u>: A DM system table is said to be <u>level-wise next-state-ambiguous</u>, if there exist inputs $I_i$, $I_j$ and $I_k$ and states $S_a$, $S_b$ and $S_c$ such that

$I_j$ and $I_i$ are adjacent and $I_k$ and $I_i$ are adjacent

(A.2.1) $\quad S_b \neq S_c$,

(A.2.1) $\quad g'(S_a, I_j, I_i) = S_b$ and

(A.2.3) $\quad g'(S_a, I_k, I_i) = S_c$.

| | $I_j$ / $I_i$ | $I_k$ / $I_i$ |
|---|---|---|
| $S_a$ | $S_b$, $O_{ai}$ | $S_c$, $O_{ai}$ |

Figure A.2

<u>REALIZATION OF SYSTEM IN FIGURE 3.1</u>