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**DIGITAL DATA RECORDING SYSTEM (DDRS)  
OPERATING AND MAINTENANCE MANUAL**

Final Technical Manual under Contract NAS9-15217, Subtask 4

Carroll R. Griffin  
Jack I. Jones

**APPLIED RESEARCH LABORATORIES**  
THE UNIVERSITY OF TEXAS AT AUSTIN  
POST OFFICE BOX 8029, AUSTIN, TEXAS 78712

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## I. BACKGROUND

When the NASA/JSC B-57 synthetic aperture radar (SAR) development testbed program was planned, an existing side-looking radar, the APQ-102, was selected for remote sensing study programs. This radar is a purely analog system, employing photographic processing and azimuth correlation using analog film processing into a SAR map. When the investigation was expanded to include parametric variation for digital SAR, a system had to be acquired to digitize the video data produced by the APQ-102 and to record it on a wideband tape recorder aboard the aircraft.

The system designed and built by ARL:UT is called the digital data recording system, or DDRS. In addition to digitizing the raw (pulse compressed) video signals from the radar, the system provides for recording various parameters from the radar operating environment, such as the inertial platform signals and aircraft operating parameters. These parameters are necessary in the reconstitution of the radar video into a synthetic aperture high resolution radar map.

The purpose of the DDRS is to supplement the analog radar system with a digital SAR system which will permit the study and analysis of various radar parameters, leading to the effective design of an orbiting SAR for remote sensing applications.

## II. SYSTEM DESCRIPTION

The DDRS is mounted on a pallet carried in the pressurized and temperature controlled electronic equipment bay of a testbed aircraft, an RB-57.

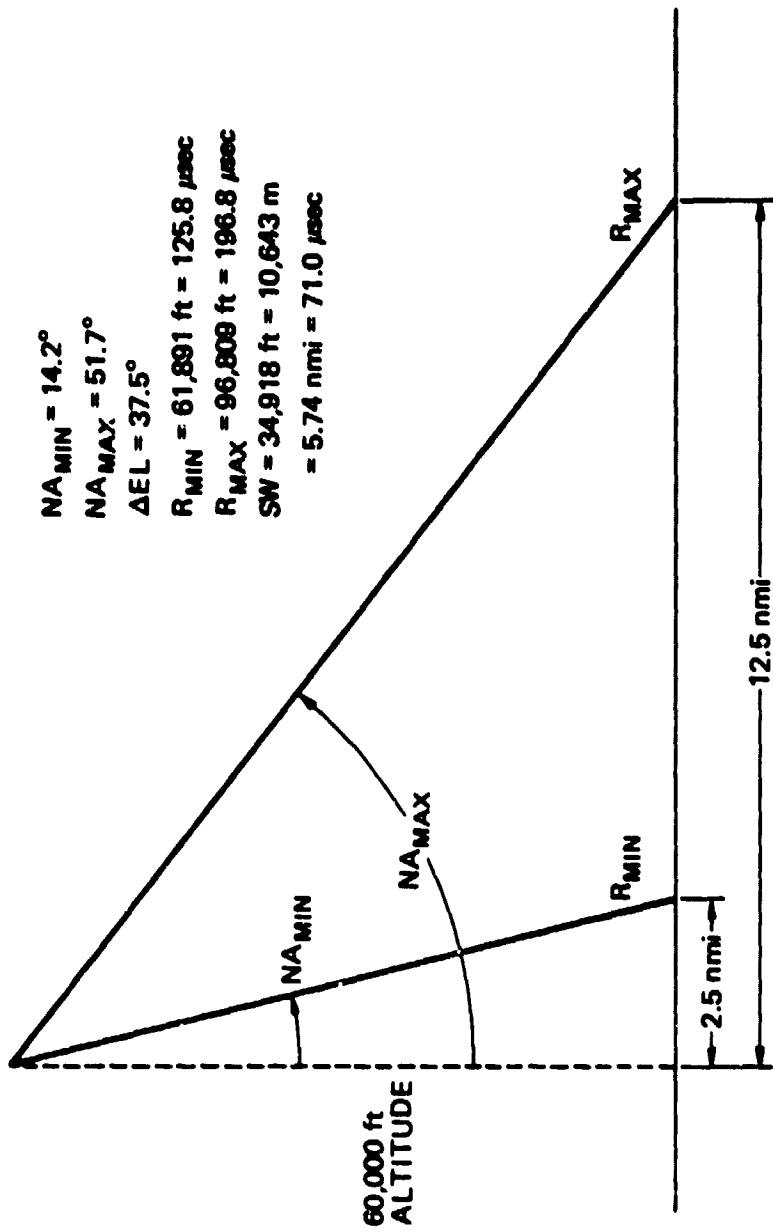
### A. Aircraft and Radar

#### 1. B-57 Flight Testbed

The aircraft testbed is a light twin-engine jet designed for high altitude operation, up to 65,000 ft. At this height the synthetic aperture radar (SAR) has the capability of simulating, in the geometry of ground mapping, the look-down angles (complement of nadir angle), associated with a SAR on an orbital platform. There are usually two flight modes at 60,000 ft: a start map nadir angle of 15°, or of 45°. The 15° nadir angle gives a swath coverage for the SAR map of 2.5-12.5 nmi (called Mode 1), and the 45° nadir angle gives coverage of 10-20 nmi-- a 10 nmi swath (Mode 2). See Figs. 1 and 2. Two antennas (and receivers) are used to obtain both horizontal and vertical polarized radar data.

The B-57 is equipped with the LTN-51 inertial platform, with clutter lock for velocity update. This platform provides antenna stabilizing signals to the radar antennas, and provides velocity information required for the synthetic aperture radar system.

The aircraft normally operates at a ground speed of about 400 kt, and this is important since the radar pulse repetition frequency (prf) is set at twice the ground speed in feet per second; in this case,  $2 \times 675$ , or 1350 pps.



$NA_{MIN} = 14.2^\circ$   
 $NA_{MAX} = 51.7^\circ$   
 $\Delta EL = 37.5^\circ$   
 $R_{MIN} = 61,891 \text{ ft} = 125.8 \mu\text{sec}$   
 $R_{MAX} = 96,809 \text{ ft} = 196.8 \mu\text{sec}$   
 $SW = 34,918 \text{ ft} = 10,643 \text{ m}$   
 $= 5.74 \text{ nmi} = 71.0 \mu\text{sec}$

**FIGURE 1**  
**MODE 1 GEOMETRY**

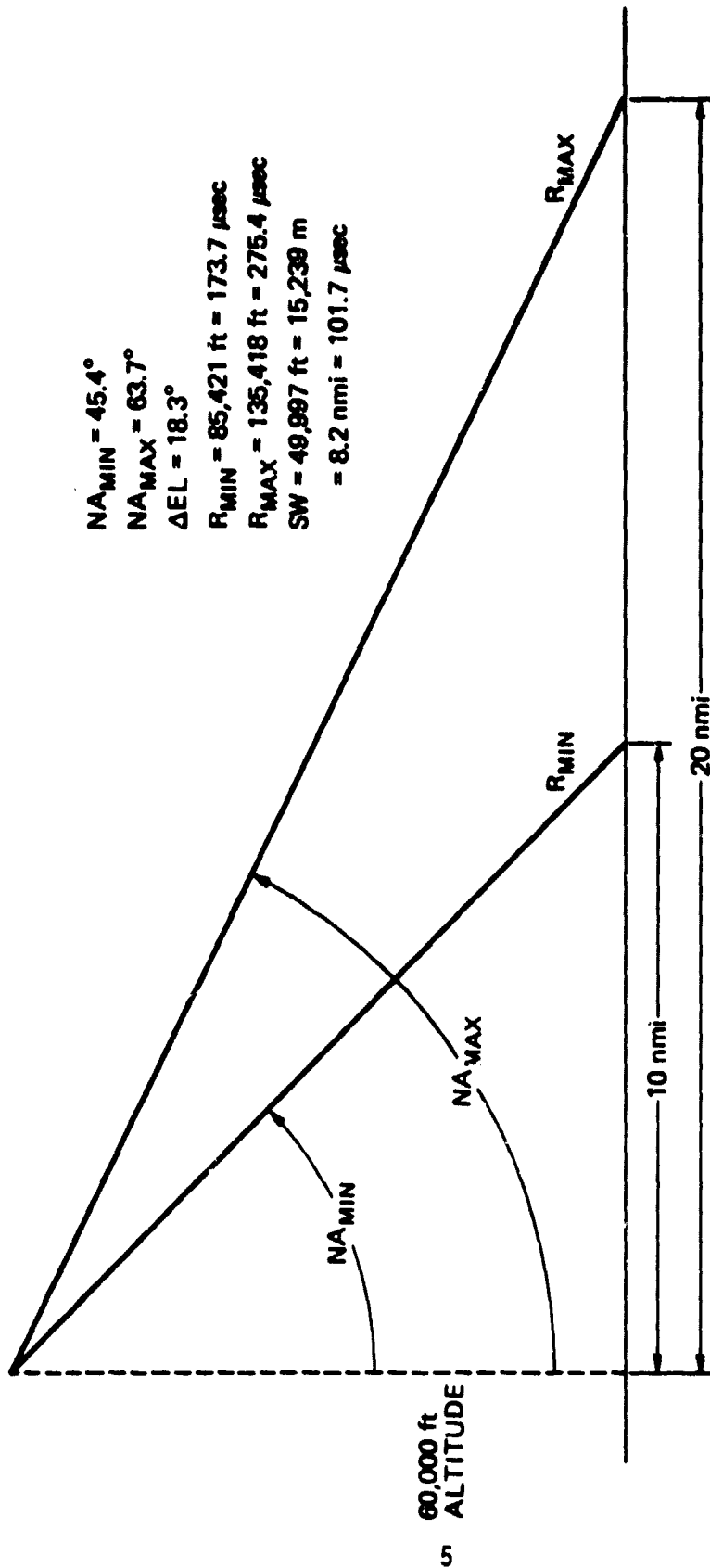


FIGURE 2  
MODE 2 GEOMETRY

The APQ-102 uses linear FM pulse compression and the pulse compressed, noncoherent video signals from the two receiver channels are provided to the DDRS for high speed conversion to digital format.

The radar uses sensitivity time control (STC) and it is the STC trigger which starts the DDRS data recording function.

Figure 3 indicates the various equipment locations in the testbed aircraft. A DDRS control panel in the cockpit permits the crew to digitize and record the SAR map data. The wideband (MINCOM) recorder is located in the pressurized section of the aircraft, and the right and left looking antennas are in the nose of the RB-57.

## 2. APQ-102 Radar

The radar is a standard Air Force procured item with some significant modifications. The original radar had a single polarized antenna; the modified system has both vertical and horizontal polarized receiver channels, both of which are recorded. The antenna has a cosecant squared pattern in elevation.

Another important modification is in the photographic film used for video recording. A 5 in. wide film is exposed with a 2 in. width utilized for each video channel, horizontal and vertical. This film is used in the azimuth correlation process, the usual analog processing which develops the SAR map.

The two channels of 15 MHz video are already motion compensated and pulse compressed when they are digitized by the DDRS. The antenna gimbals receive stabilizing signals from the LTN-51 inertial platform, and these motion compensating servo signals are recorded along with other dynamical parameters of the system.



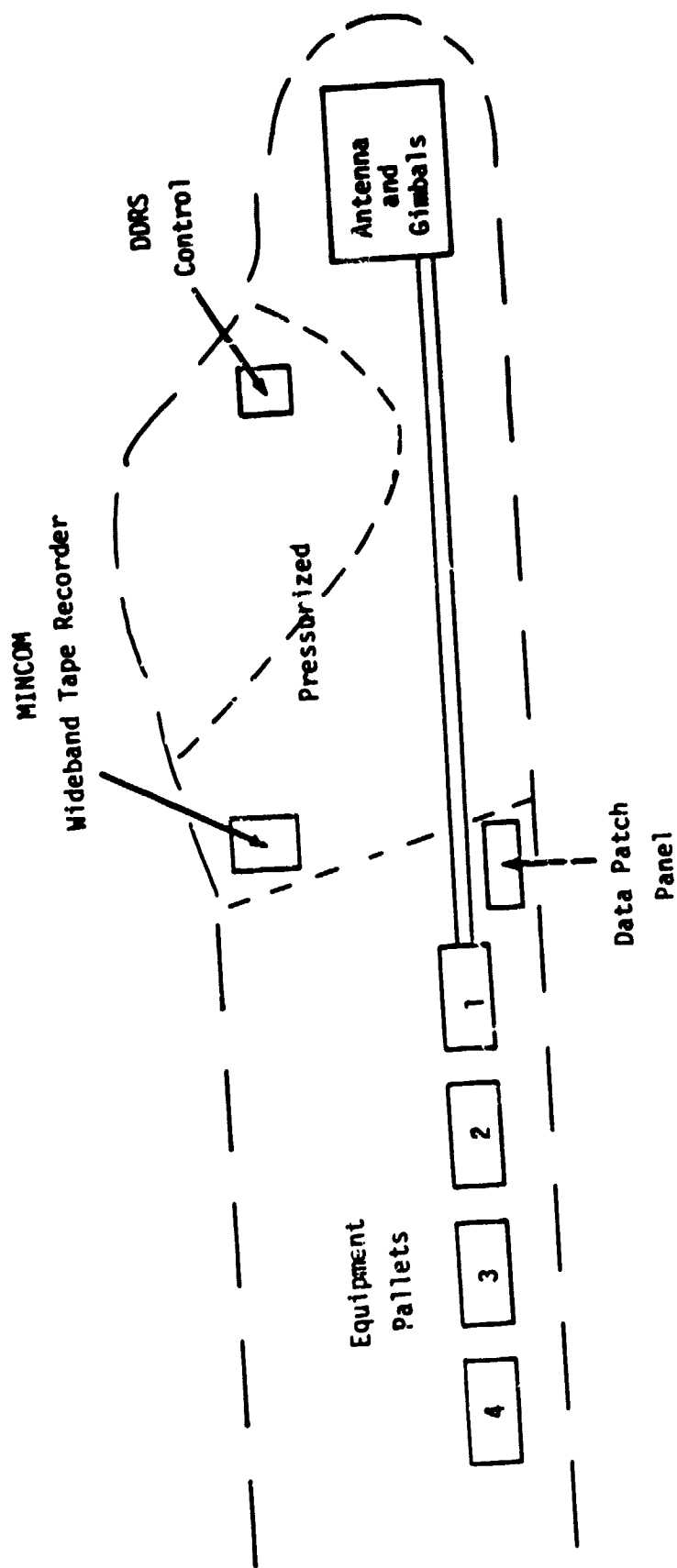


FIGURE 3  
AIRCRAFT EQUIPMENT LOCATIONS

The radar operates at an X-band frequency with variable prf, as indicated previously, such that two samples per foot of the synthetic aperture are obtained.

In addition to the two channels of video data, which the DORS records, various radar parameter environment (RPE) signals are recorded. Figure 4 shows the sources of these. Some are obtained from the universal programmable parameter stripper (UPPS), designed and built by Lockheed for NASA, and the data are from the NASA Earth Resources Data Acquisition System (NERDAS). The data are recorded on a wideband MINCOM tape recorder, carried in the pressurized section of the RB-57, after processing through the DORS.

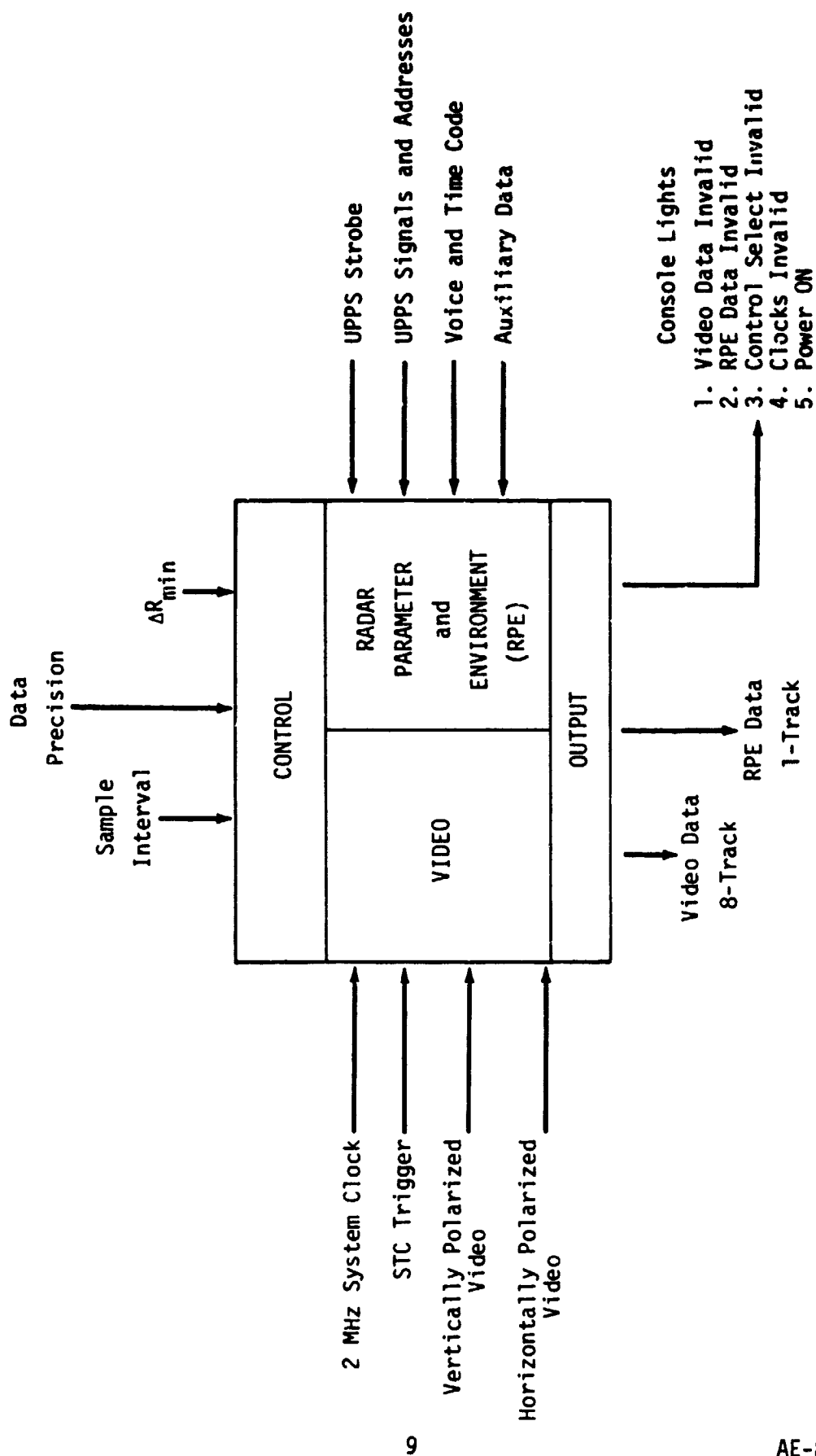


FIGURE 4  
DIGITAL DATA RECORDING SYSTEM  
OVERVIEW

### III. DDRS DESCRIPTION

The unit is designed to digitize the radar data and format it and the RPE data into a format compatible with the Hughes Aircraft digital recording interface equipment (DRIE). The DRIE is used at the ARL:UT SAR playback facility to both play back wideband tapes and reformat them onto computer-compatible tapes (CCT) on a 9-track standard tape recorder. Figure 5 is a block diagram of the system.

A MINCOM wideband tape recorder on board the aircraft produces 14 tracks of RPE and video data, which can be played back at the ARL:UT facility, since the data are properly formatted by the DDRS to be compatible with the DRIE playback equipment. The Doppler analysis software, called the ground signal processor (GSP), will produce digital SAR images on a high resolution display from the filter outputs.

#### A. Functions of the DDRS

The principal function of the DDRS is to digitize the two channels (called H and V) of raw video developed by the APQ-102 from the 70 MHz IF. In addition, it provides a single record track of RPE data corresponding to the video data. Figure 4 illustrates the sources of the data on which the DDRS operates, and the controls used by the operator to obtain the desired outputs to the wideband tape recorder.

The timing of the system is critical; it is controlled by the radar (APQ-102) timing. This comes from a 2.07065 MHz clock which controls a coherent oscillator in the DDRS. The start of a range sweep is controlled by the sensitivity time control trigger. The two video channels are picked off from the optical recorder of the radar system.

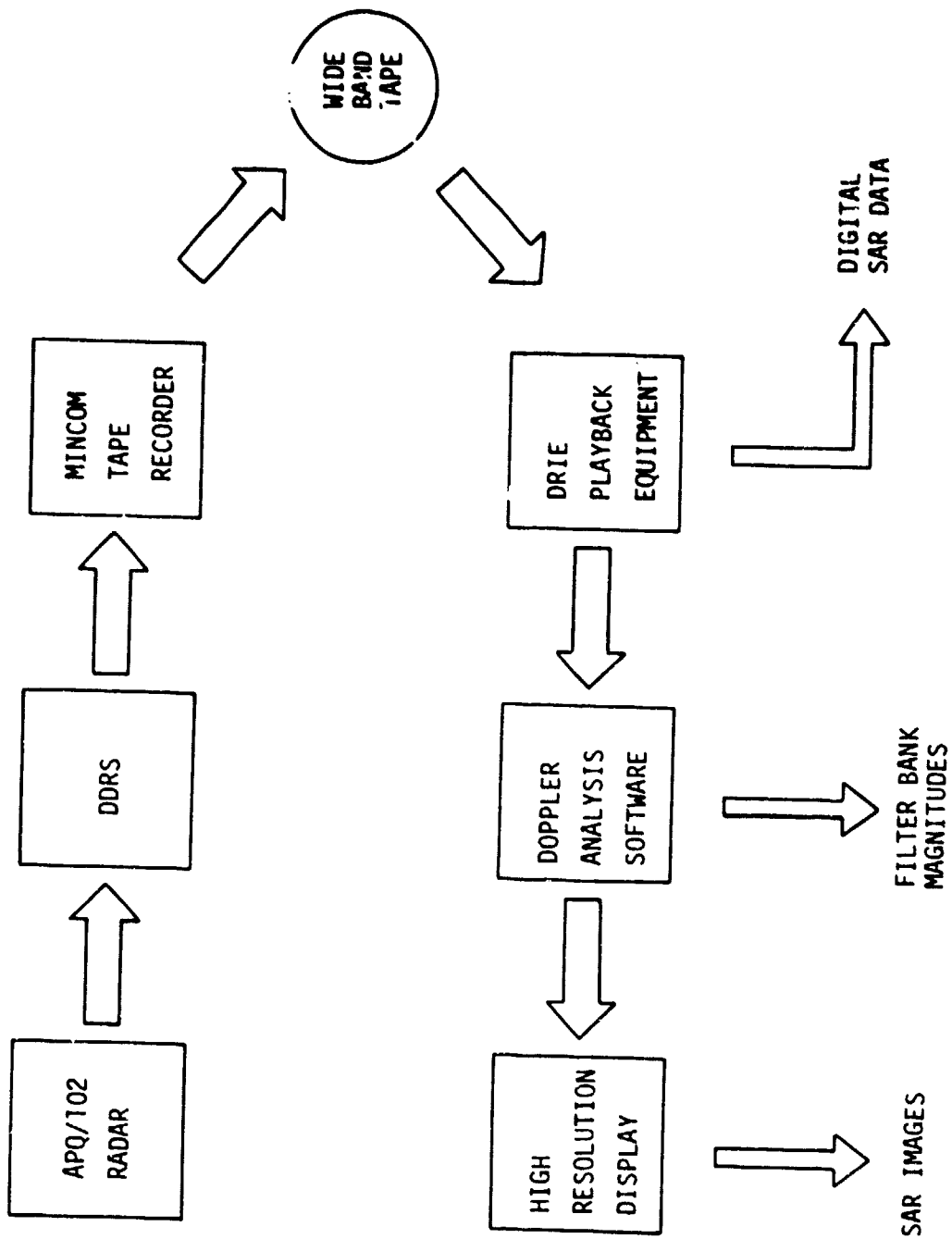


FIGURE 5  
SAR DATA FLOW

The universal programmable parameter stripper (UPPS) is a device which permits digitally coded radar system parameters to be input to the DDRS in a compatible format. Voice and time code data are also input for recording on the wideband tape.

The cockpit-mounted control panel permits an operator to enter a delay time from the start of the STC trigger to set the starting range for the radar map--a value called  $\Delta R_{\min}$ . The sampling rate may also be set by selecting the value of the sample interval. Finally, the operator may select from 7-, 4-, 2-, or 1-bit data precision.

### 1. Digitizing

The DDRS digitizes analog video in video A/D board 6. Two channels of video are digitized at a sample rate set by the operator (a crew member) setting switches which select the sample interval (SI) and the start of sampling (DRMIN), which is a selected delay from the STC trigger. The latter is routed through the AGC/STC processor, which is a Lockheed-built special device for the APQ-102 radar. See Fig. 6.

Besides the video, certain monitored environmental signals in the DDRS, temperature and pressure and operating voltages, are digitized externally in the auxiliary data board, located in the AGC/STC processor. Analog signals are shipped out to the auxiliary data board, converted to digital, and transferred back out to the DDRS, where they are formatted in the same manner as the UPPS data.

### 2. Recording

Figure 7, the DDRS block diagram, indicates those signals recorded on the wideband MINCOM tape recorder. One track of the recorder is used for the RPE data, made up from the UPPS output and the auxiliary data coming from the auxiliary data board. These digital data are transferred through the auxiliary data bus. Eight tracks of the recorder are used for the digitized video. All the digitized data are routed through

Lockheed-built AGC/STC Processor

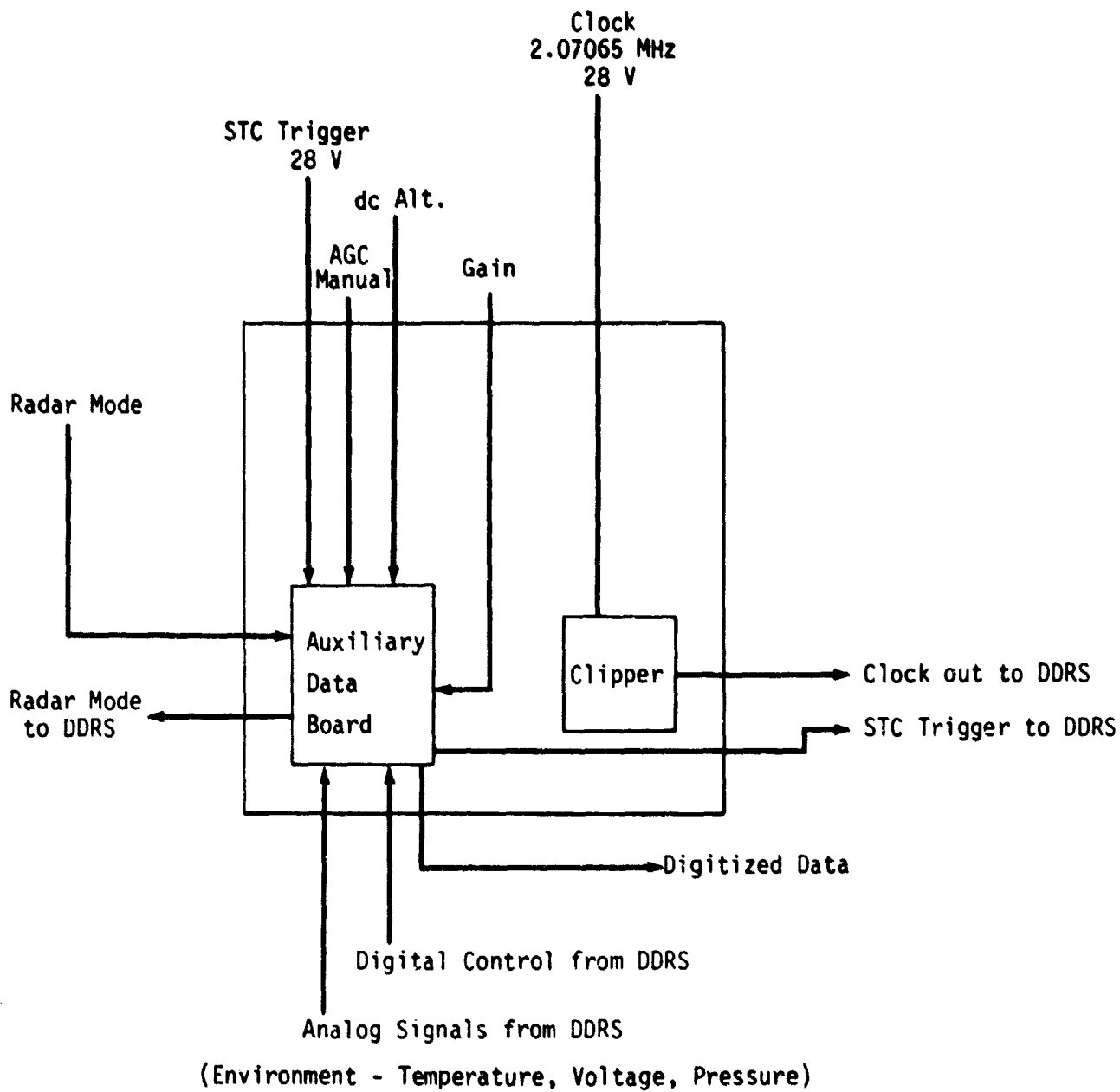


FIGURE 6  
AGC/STC PROCESSOR WITH AUXILIARY DATA BOARD

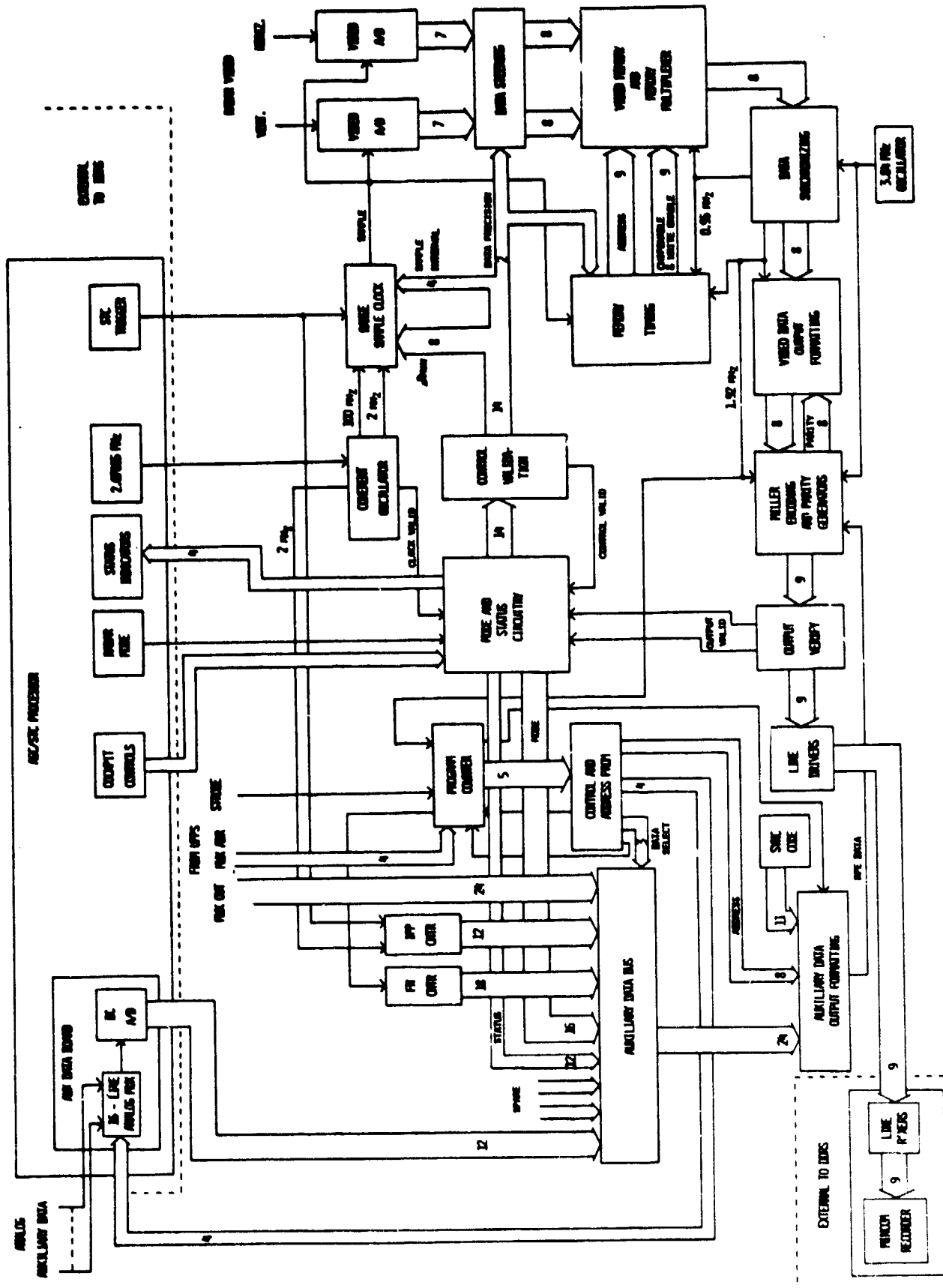


FIGURE 7  
DDRS BLOCK DIAGRAM



Miller encoders and a parity bit generator. The LSB of the video tape data is used for parity check (only in the 7-bit mode).

In addition to the outputs of the DDRS recorded in the MINCOM recorder, the voice from the crew and ground stations and time code signals from the IRIG time code generator are frequency modulation coded, and recorded on two more tracks of the MINCOM tape recorder. This is, of course, independent of the DDRS.

## B. Interfaces

The principal interfaces of the DDRS are with the radar system, to obtain the video data, with the NERDAS outputs via the Lockheed-built UPPS, with the auxiliary data board in the STC/AGC processor (built by Lockheed), the cockpit-mounted control box, and the DRIE by way of the wideband recorder. These will be described in turn.

### 1. Radar

Refer to Table I. The horizontal and vertical channel video signals, pulse compressed bipolar ( $\pm 0.5$  V) analog signals are supplied to the DDRS from the optical recorder subsystem of the APQ-102. A test signal is generated as a reference on the video A/D board, variable from zero to negative full scale for the analog input. This signal is furnished on a connector for use in testing and adjusting the video inputs.

### 2. UPPS/NERDAS

Four address lines and a strobe signal are supplied from the Lockheed-built universal programmable parameter stripper. In addition, on a separate connector (J-101), 24 data lines are available from the UPPS. These are differential, TTL signals.

TABLE I  
LIST OF FRONT PANEL CONNECTOR SIGNALS FOR THE DDRS

J101:	MUX <sub>0</sub> - MUX <sub>23</sub> ; differential signal inputs from the UPPS, TTL.
J102:	ADD <sub>0</sub> - ADD <sub>3</sub> , and STRB; differential signal inputs from the UPPS, TTL.
J103:	<p>REF; analog voltage reference output to patch into video inputs for test, 0 to -1 Vdc, adjustable on Board 6.</p> <p>TRIGRPE, TRIGVID: scope trigger output for the RPE and video channels, respectively; TTL.</p> <p>VIDNRZ<sub>0</sub> - VIDNRZ<sub>7</sub>; video data outputs, unencoded for scope viewing, TTL.</p> <p>RPENRZ; RPE data output, unencoded, TTL.</p> <p>PARCHK; parity error pulse output, for connection to an event counter, TTL.</p> <p><u>RPETEST</u>; input, when grounded puts the RPE subsystem into the test mode.</p> <p>AUX/UPPS; input, when <u>RPETEST</u> is grounded, determines either auxiliary or UPPS data to be displayed, UPPS when grounded.</p>
J104:	VIDMIL: differential outputs, Miller encoded video data, to recorder, TTL.
J105:	<p>SI<sub>0</sub> - SI<sub>3</sub>; ±5 V inputs, binary coded sample interval control.</p> <p>DRMIN<sub>0</sub> - DRMIN<sub>7</sub>; ±5 V inputs, 9's complement BCD delta RMIN control.</p> <p>DP<sub>0</sub> - DP<sub>1</sub>; ±5 V inputs, data precision control.</p> <p>RPEINVAL, VIDINVAL, CNTINVAL, ORALT, CLKINVAL: TTL outputs, TRUE (+2 V, 20 mA) indicates, respectively, poor RPE data, poor video data, invalid control setting, video overrange, clock out of sync.</p> <p>PWR ON; +2 V, 20 mA output whenever power is applied.</p>

TABLE I (Cont'd)  
LIST OF FRONT PANEL CONNECTOR SIGNALS FOR THE DDRS

	N5.7; - 5.7 V "false" voltage reference to control switches, limited by 100 $\Omega$ .
J106:	<p>AUX ADD<sub>0</sub> - AUXADD<sub>3</sub>, AUXCLK, AUXST: differential outputs to the auxiliary data board in the AGC/STC processor, TTL.</p> <p>RADMODE: AUXDATA, AUXSTRB, STCTRIG, differential inputs from the auxiliary data board, TTL.</p> <p>N2, P5, N5.7, TEMP1, TEMP2, PRES; analog dc voltage outputs to auxiliary data board, TTL.</p> <p>P15, +15 V at 20 mA, resistor limited, from the auxiliary data board.</p> <p>SYSCLK: 2.07065 MHz, TTL system clock signal input from the auxiliary data board.</p>
J107:	+28 V with return at 4 A max, fused; 200 V, 400 Hz, 3-phase, at 300 mA max
J108:	50 $\Omega$ vertical polarization video input from the optical recorder. Level is adjustable from $\pm 0.5$ V pp to $\pm 1.0$ V pp. The input is dc coupled.
J109:	50 $\Omega$ horizontal polarization input, at the same level as J108.

### 3. Auxiliary Data Board

Because of inadequate processing space in the DDRS, certain analog signals are shipped out to the AGC/STC processor for conversion to digital signals on the auxiliary data board. These are pressures, temperatures, and voltages, which are monitored in the DDRS and recorded on the wideband recorder. Clock strobe outputs and inputs control the operation of the auxiliary data board. Other outputs from the AGC/STC processor that involve the auxiliary data board are the STC trigger, which initiates a digitizing cycle in the DDRS, a dc altitude signal which is digitized and sent back to the DDRS for formatting, a signal conditioned 2.07065 MHz clock pulse, and a digitized radar mode signal.

### 4. Controls

The cockpit-mounted control panel permits an operator to send control signals in digital form to the DDRS. The operator can select the sample interval (SI), data precision or number of bits (DP), and the start sampling range (DRMIN). Power ON and logic voltages are also supplied. Signals sent to the control panel are invalid signals for the clock, video, and RPE data, to inform the operator of a problem in the DDSP. A control invalid (CNT INVALID) signal informs the operator that an invalid set of switch settings has been selected. An over-range alert (OR ALT) signal alerts the operator to video signals which are exceeding the range of the A/D converters.

### 5. Recorder

Eight tracks of formatted video (in FLAMR format) are sent to the wideband tape recorder in Miller code, and one track, similarly formatted and coded, of RPE data. A clock output signal is furnished to the same connector (J-104); however, it is not recorded.

## 6. Power

The DDRS uses +5 V for TTL operations, and -5.75/-2.0 V for MECL operations. These are supplied from two integral dc power supplies, which are driven from the aircraft 28 Vdc bus. A cooling fan is driven by 400 Hz ac power.

## 7. System Test

Video and RPE data encoded in NRZ format are supplied on connector J-103 for other uses, such as checking the performance of the DDRS in real time. A RPE test signal and a signal to select between UPPS and the auxiliary data board are input to the DDRS. A RPE trigger and parity check signal are supplied on the same connector, as is a video trigger.

## C. Performance Specifications

### 1. Controllable Parameters

Number of Range Samples Recorded:

- 7-bit data: 512 per polarization channel
- 4-bit data: 1024 per polarization channel
- 2-bit data: 2048 per polarization channel
- 1-bit data: 4096 per polarization channel

Allowable Slant-Range Sample Intervals: 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150 nsec

Recorded Slant Range and Ground Range Swath Widths:

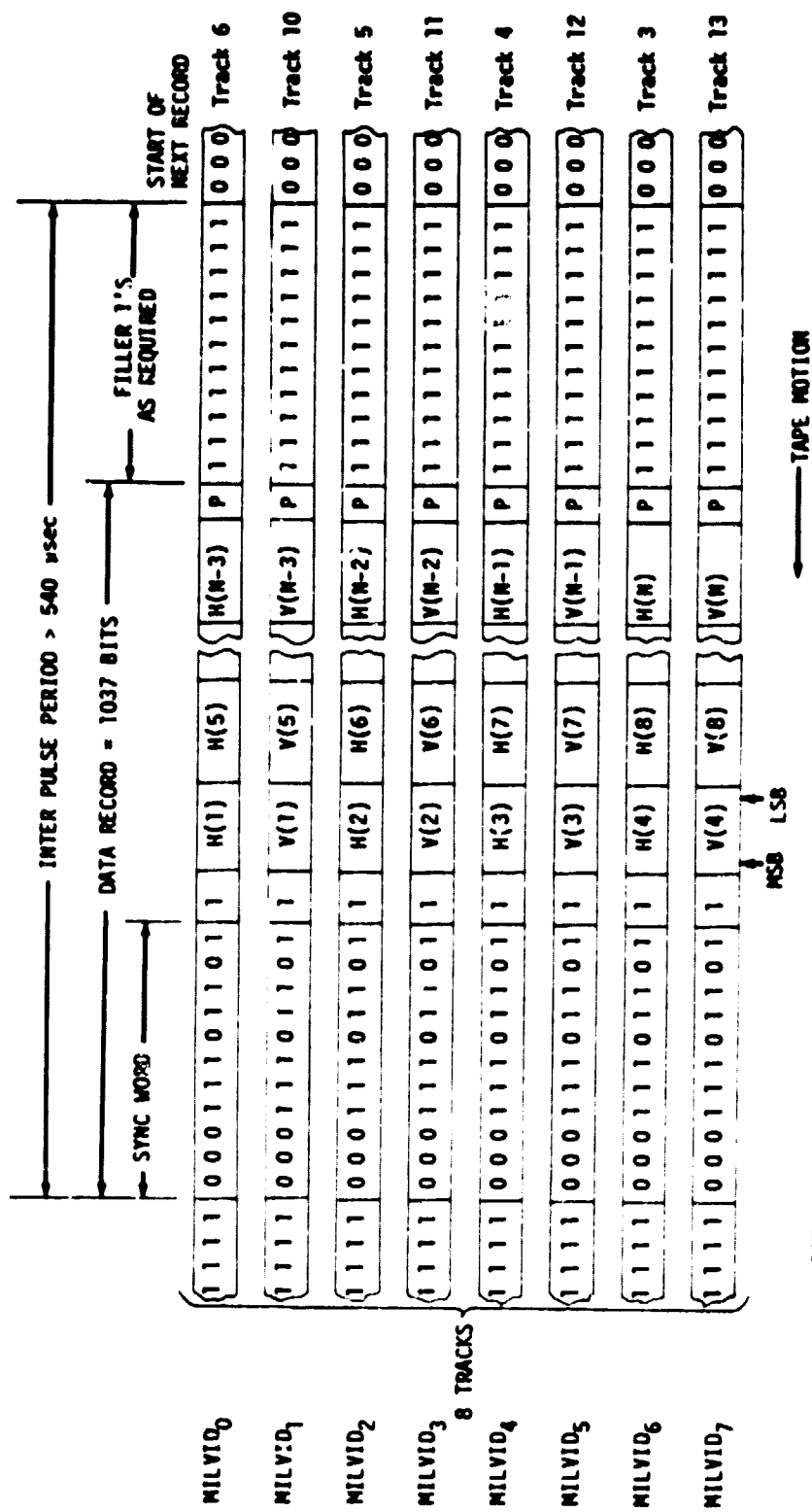
Slant Range Sample Interval (nsec)	Data Precision (bits)	Slant Range Swath Width (km)	Mode 1 G-R Swath (nmi)	Mode 2 G-R Swath (nmi)
40 (6.0 m)	7	3.1 (1.66 nmi)	2.5 - 6.5	10 - 12.2
"	4	6.1 (3.31 nmi)	2.5 - 9.2	10 - 14.3
"	2	12.3 (6.62 nmi)	2.5 - 13.6	10 - 18.2
"	1	24.6 (13.2 nmi)	2.5 - 21.2	10 - 25.4
50 (7.5 m)	7	3.8 (2.07 nmi)	2.5 - 7.3	10 - 12.7
"	4	7.6 (4.14 nmi)	2.5 - 10.4	10 - 15.3
"	2	15.2 (8.28 nmi)	2.5 - 15.6	10 - 20.0
"	1	30.4 (16.6 nmi)	2.5 - 24.9	10 - 29.0
60 (9.0 m)	7	4.6 (2.48 nmi)	2.5 - 7.9	10 - 13.3
"	4	9.2 (4.97 nmi)	2.5 - 11.5	10 - 16.3
"	2	18.4 (9.94 nmi)	2.5 - 17.5	10 - 21.9
"	1	36.8 (19.9 nmi)	2.5 - 28.4	10 - 32.5
100 (15.0 m)	7	7.6 (4.14 nmi)	2.5 - 10.4	10 - 15.3
"	4	15.2 (8.28 nmi)	2.5 - 15.6	10 - 20.0
"	2	30.4 (16.6 nmi)	2.5 - 24.9	10 - 29.0
"	1	60.8 (33.2 nmi)	2.5 - 42.2	10 - 46.2

Available Delays from STC Trigger to Start of Sampling:

2-99  $\mu$ sec in 1  $\mu$ sec intervals

2. Video Characteristics (each polarization channel)

Video Input Impedance	75 $\Omega$
Video 3 dB Bandwidth	>20 MHz
Maximum Video Level (adjustable)	$\pm 1.0$ V
Maximum Video Sampling Rate	25 MHz
Conversion Accuracy	<30 mV
rms Sampling Jitter	1 nsec
Digital Code after Conversion	2's complement
Minimum IPP (worst case)	700 $\mu$ sec
Data Record Format to Tape	Fig. 8
Tape Track Encoding	Miller Code
Tape Track Assignment	Table II



LEGEND

- H(2) = H DATA FOR RB NO. 2
- V(2) = V DATA FOR RB NO. 2
- P = PARITY BIT

FIGURE 8  
VIDEO DATA RECORD FORMAT

**TABLE II**  
**MINCOM RECORDER OPERATING PARAMETERS**

<b>Record Electronics Required: 11 Channels IRIG Wideband Direct Record</b>	
<b>Record Speed: 120 ips</b>	
<b>Tape Used: Scotch Type 888-1-9200-IRH, (1"x9200'), Stock No. 84-9800-3637-4, or equivalent</b>	
<b>Tape Reels Used: 14 in. metal precision</b>	
<b>Record Time: 920 sec (15.3 min)</b>	
<b>Recorder Track Assignments:</b>	
<b>Track</b>	<b>Signal</b>
1	IRIG Time Code
2	Open
3	Video Data Channel 6 (1.92 Mbs Miller Code)
4	Video Data Channel 4                   "
5	Video Data Channel 2                   "
6	Video Data Channel 0                   "
7	RPE Data (1.92 Mbs Miller Code)
8	Open (FLAMR PPD Track)
9	Open (FLAMR FB Track)
10	Video Data Channel 1 (1.92 Mbs Miller Code)
11	Video Data Channel 3                   "
12	Video Data Channel 5                   "
13	Video Data Channel 7                   "
14	Voice Direct



### 3. RPE Characteristics

Data Sampling Frequency (established by NERDAS)	100 Hz
Data Types and Formats	Table III
Data Record Format to Tape	Fig. 9

### 4. Power Requirements

+28 Vdc at 4 A max  
200 Vac, 400 Hz, 3 Phase at 0.4 A max

### 5. Physical Characteristics

Weight	25 lb
Dimensions	13 1/4 in. L x 8 1/2 in. W x 9 3/8 in. H

## D. Hardware Description

### 1. Mechanical Overview and Interconnection Scheme

The circuitry of the DDRS, other than the auxiliary data board, is contained in a custom fabricated enclosure designed for mounting in the RB-57 electronic pallet (Dwg. No. 1). On the back panel of this enclosure are mounted all input and output cylindrical connectors (J-101-J-109). Inside the enclosure are mounted two power supplies, a cooling fan, and a card cage with eleven numbered card slots, six of which (slots 2, 4, 6, 8, 9, and 11) contain circuit boards and one of which (slot 1) contains a cable connecting board.

Drawings No. 2 and 3 show the wiring scheme inside the enclosure. The six circuit boards plug into the backplane connectors (J2, J4, J6, J8, J9, J11) through the board-mounted plug connectors (P2, P4, P6, P8, P9, P11). The backplane connectors are wired to one another by wirewrap connections according to the backplane wiring diagram, Dwg. No. 2. Also, the circuit board plugged into J2 (in card cage slot 2) is connected to

**TABLE III  
RPE DATA FORMAT**



Data Bit Numbers							
	MSB					LSB	
	23	20	16	12		4	0
1. TIME	10xH	1xH	10xMIN	1xMIN	10xSEC	1xSEC	<u>BCD</u>
2. DATE	10xYR	1xYR	10xMO	1xMO	10xDAY	1xDAY	<u>BCD</u>
3. LATITUDE	SIGN	10xDEG	1xDEG	10xMIN	1xMIN	.1xMIN	<u>BCD</u>
4. LONGITUDE	SIGN	100xDEG	10xDEG	1xDEG	10xMIN	1xMIN	<u>BCD</u>
5. RADAR ALT	xxxx	10kxFT	1kxFT	100xFT	10xFT	1xFT	<u>BCD</u>
6. HEADING	xxxx	xxxx	100xDEG	10xDEG	1xDEG	.1xDEG	<u>BCD</u>
7. DRIFT	xxxx	xxxx	SIGN	10xDEG	1xDEG	.1xDEG	<u>BCD</u>
8. ROLL	SAME AS DRIFT						
9. PITCH	SAME AS DRIFT						
10. GND SPD	xxxx	xxxx	xxxx	100xkt	10xkt	1xkt	<u>BCD</u>
11. VERT ACC	xxxx	xxxx	SIGN	1xG	.1xG	.01xG	<u>BCD</u>
12. IPP	xxxxxxxxxxxxxxxxxxxxxxxx			$IPP_{11}$ <span style="float: right;"><math>IPP_0</math></span>  LSB = 482.94 nsec			<u>BIN</u>
13. FRAME NO.	xxxxxxxxxxxx		$FN_{18}$ <span style="float: right;"><math>FN_0</math></span>  incremented every 80 msec				<u>BIN</u>

TABLE III (Cont'd)  
RPE DATA FORMAT

14. STATUS WORD

- SW<sub>0</sub>: VIDVAL (1=video data valid)  
 SW<sub>1</sub>: RPEVAL (1=RPE data valid)  
 SW<sub>2</sub>: CLKVAL (1=clock in sync)  
 SW<sub>3</sub> SW<sub>7</sub>: OR<sub>0</sub>-OR<sub>4</sub> (count of video overranges in 100 msec)  
     LSB=8 for 7-bit precision data  
     LSB=16 for 4-bit precision data  
     LSB=32 for data precision=2-bit  
     LSB=64 for data precision=1-bit  
 SW<sub>8</sub> SW<sub>11</sub>: PARERR<sub>0</sub> - PARERR<sub>3</sub> (count of buffer memory parity errors  
     in 10 msec - active only in 7-bit data  
     precision mode)  
     LSB=1 error  
 SW<sub>12</sub> SW<sub>23</sub>: undetermined

15. MODE WORD

- MD<sub>0</sub> - MD<sub>7</sub>: undetermined  
 MD<sub>8</sub> - MD<sub>15</sub>: DRMIN<sub>0</sub> - DRMIN<sub>7</sub> - coded into 2 digits of 9's comple-  
     ment of BCD  
     (delta RMIN)  
     LSB=965.880 nsec  
 MD<sub>16</sub> - MD<sub>19</sub>: SI<sub>0</sub> - SI<sub>3</sub> (sample interval)  
     LSB=10.0613 nsec (inverted binary)  
 MD<sub>20</sub> - MD<sub>21</sub>: DP<sub>0</sub> - DP<sub>1</sub> (data precision)

DP <sub>0</sub>	DP <sub>1</sub>	Data Precision
0	0	1-bit
0	1	2-bit
1	0	4-bit
1	1	7-bit

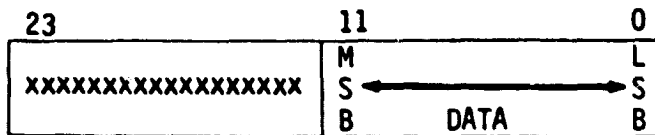
- MD<sub>22</sub>: RADMODE (Radar Mode: 0=Mode 1  
     1=Mode 2)  
 MD<sub>23</sub>: CNTLVAL (1=Mode Control Settings Valid)

NOTE: FOR NERDAS DATA, THE SIGN CODE IS: + : 1110  
 - : 1100

TABLE III (Cont'd)  
RPE DATA FORMAT

RPE ADDRESS 201 - 220 (AUXILIARY DATA)

DATA FORMAT



Binary bits 0-11 define a whole number integer (N) between 0 and 4095. To translate N into its corresponding voltage for each parameter, use the following equations:

AUXILIARY DATA

EQUATION

0. UNDEFINED	Voltage = $(2.443 \times 10^{-3})N$
1. TEMP1	TEMP, °C = $(0.0304) (N-1309)$
2. TEMP2	"
3. TEMP3 (not connected)	"
4. TEMP4	"
5. -5.7 V DDRS	Voltage = $-(2.397 \times 10^{-3})N$
6. +5 V DDRS	Voltage = $(2.443 \times 10^{-3})N$
7. -2 V DDRS	Voltage = $-(2.397 \times 10^{-3})N$
8. +5 V AUX	Voltage = $(2.443 \times 10^{-3})N$
9. -15 V AUX	Voltage = $-(4.986 \times 10^{-3})N$
10. REF (+10 V)	Voltage = $(4.888 \times 10^{-3})N$
11. dc ALT	Voltage = $(2.443 \times 10^{-3})N$
12. AGC/MAN	Voltage = $(7.473 \times 10^{-3})N$
13. GAIN	Voltage = $(2.443 \times 10^{-3})N$
14. +15 V AUX	Voltage = $(4.893 \times 10^{-3})N$
15. PRESSURE	PSIA = $[(4.618 \times 10^{-3})N] - 3.75$

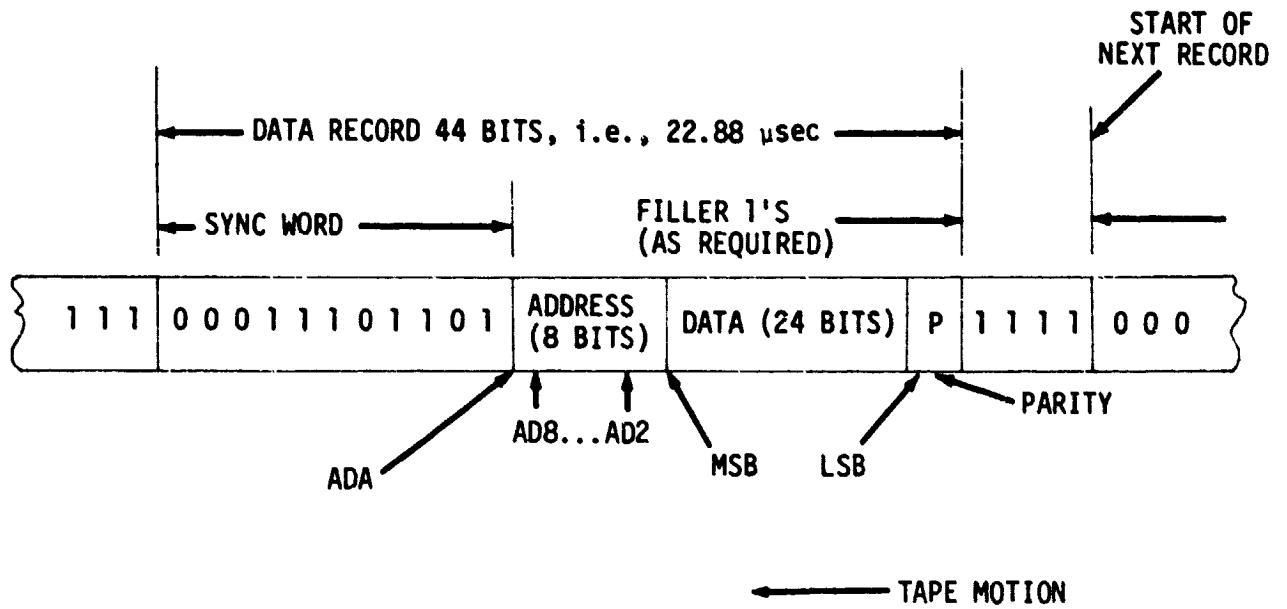
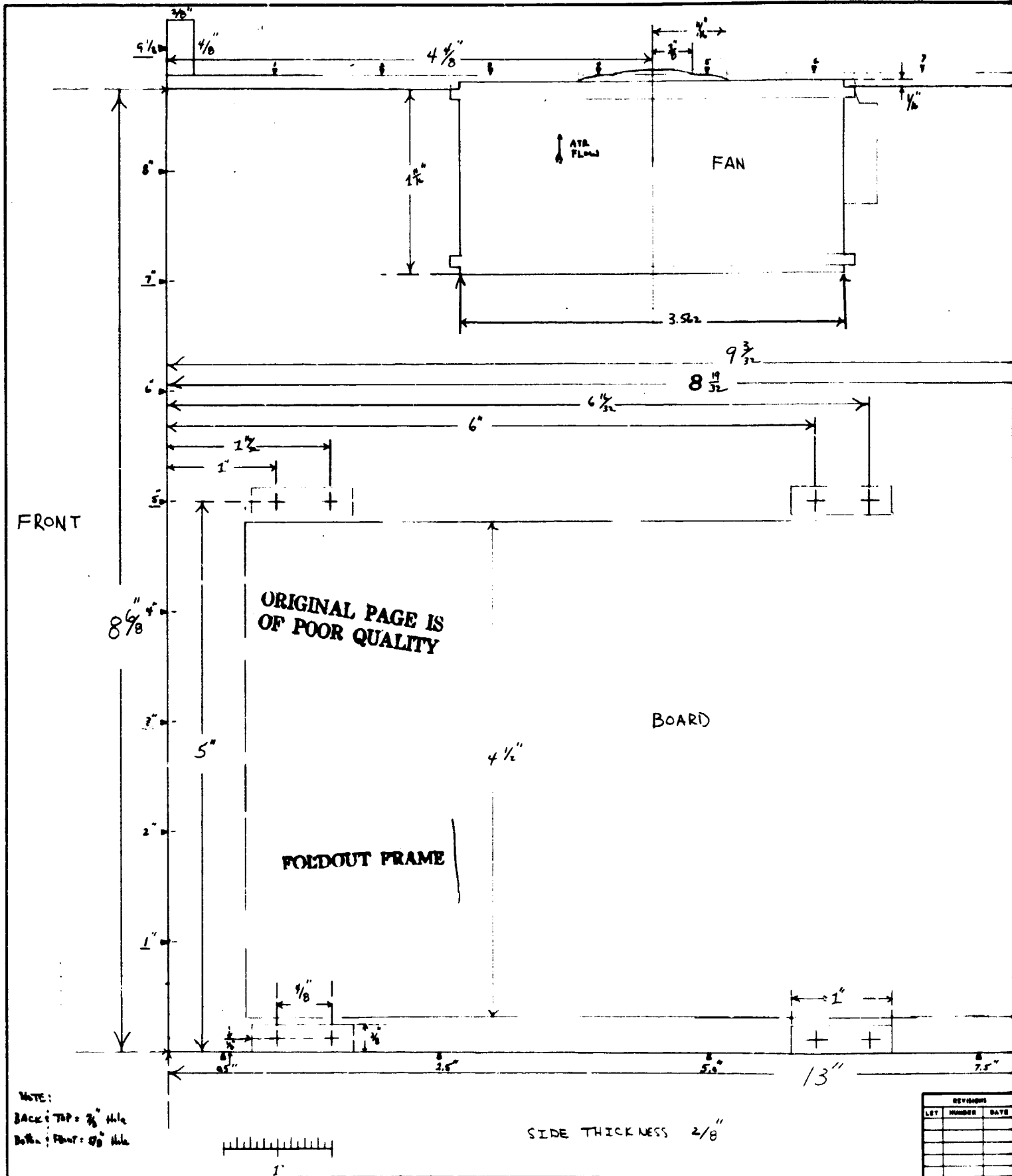
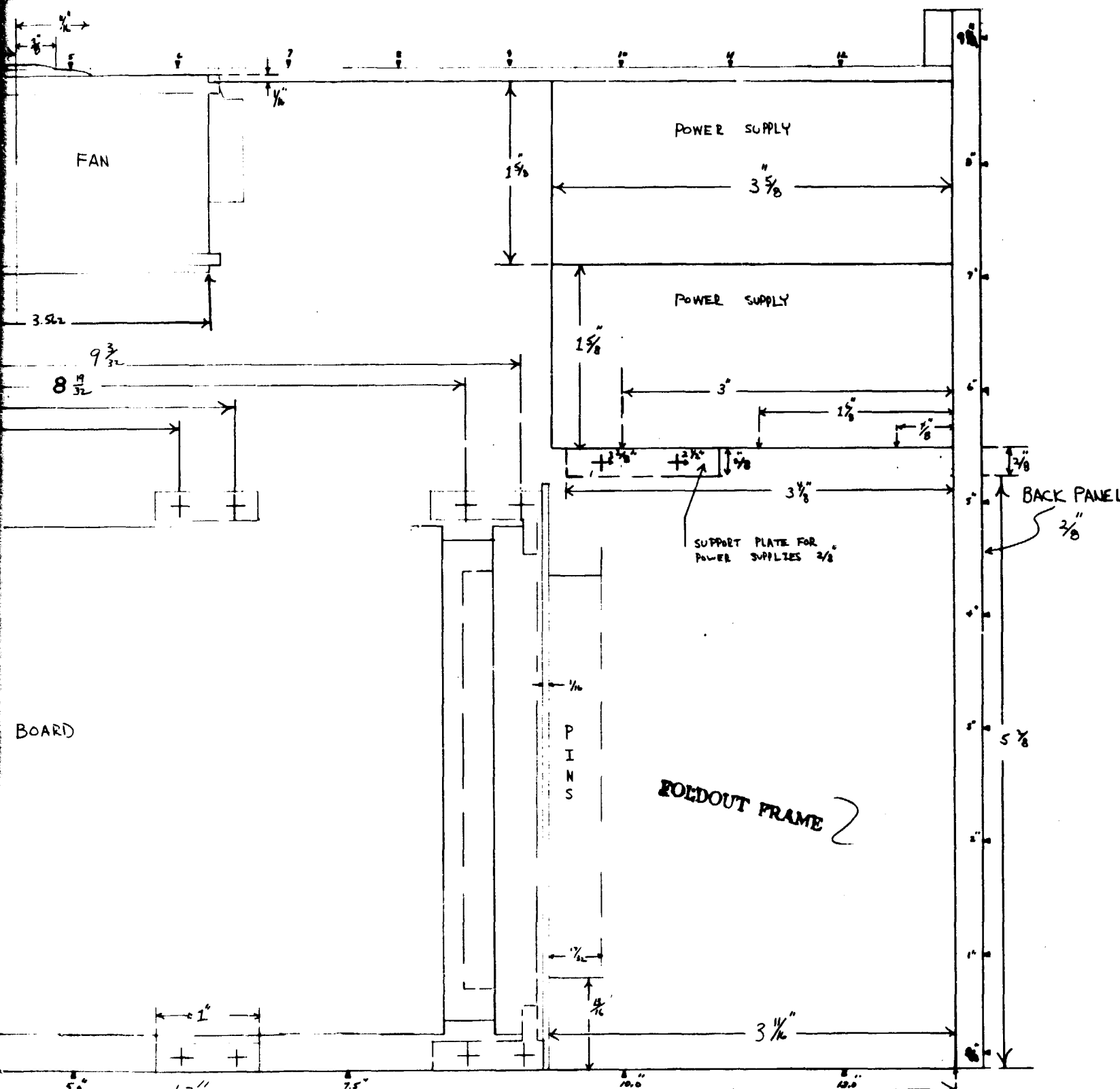


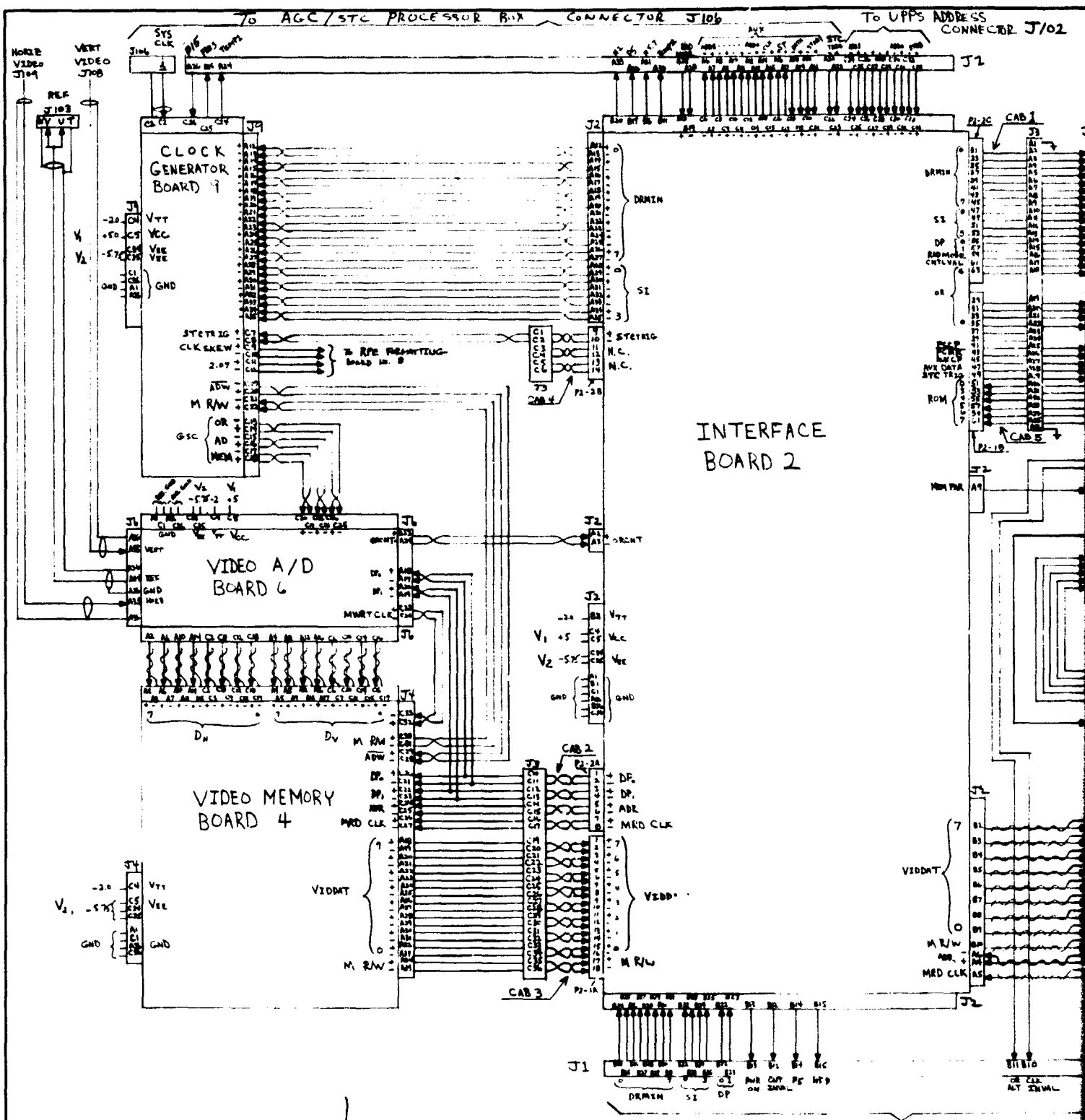
FIGURE 9  
MAGNETIC TAPE FORMAT - RPE DATA RECORD





NESS 2/8"

REVISIONS		APPROVED	DATE	SIGNED ENGINEER APPROVER	DO NOT SCALE DRAWING	FULL VIEW RIGHT SIDE DDRS	400 HD	APPLIED RESEARCH LABORATORIES THE UNIVERSITY OF TEXAS AT AUSTIN
LET	NUMBER	DATE	3/12/50		DATE			
				DECIMAL 2 FRACTIONAL 2 ANGULAR 2	HEAT TREATMENT	MATERIAL		
		CHECKED			NO. 0000	NASA-15217-4		
		DRAWN	7/11/50					



INTERFACE BOARD 2

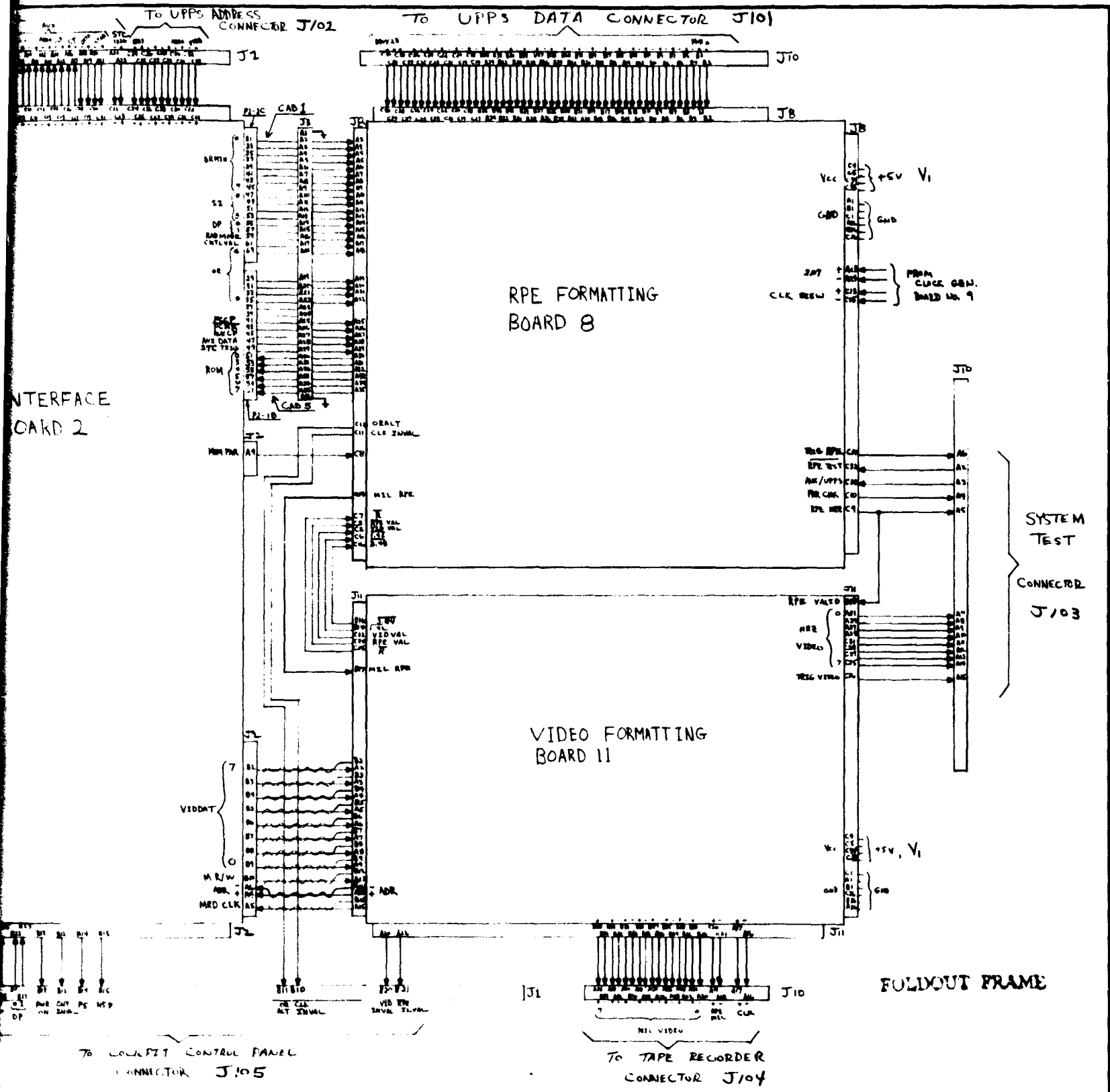
FOLDOUT FRAME

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TO COCKPIT CONTROL PANEL CONNECTOR J105

REV	NUMBER	DATE
A	11	SEPT 77
B	16	FEB 78





TO CONTROL PANEL CONNECTOR J105

TO TAPE RECORDER CONNECTOR J104

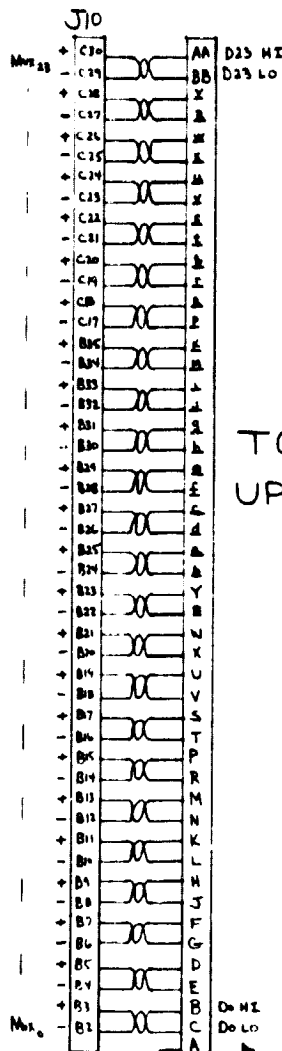
REVISION	APPROVED	DATE	DESIGN ENGINEER	DO NOT SCALE DRAWING	DDRS SYSTEM PACK ASSEMBLY SIGNAL WIRING DIAGRAM	JOB NO.
A 11 SEP 75		11/15/75				
B 11 FEB 77						
	CHECKED					
	DRAWN	11/15/75			MATERIAL NA: 9-15217-4	

APPLIED RESEARCH LABORATORIES  
THE UNIVERSITY OF TEXAS AT AUSTIN

SCALE

**D** Drawing No. 2

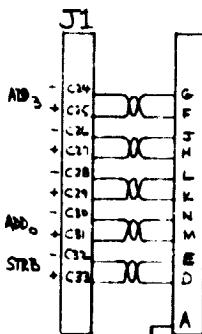
ORIGINAL PAGE IS OF POOR QUALITY



CONNECTOR J101

BURNDY (24-61)  
20 GA 61 PIN  
MALE  
PART # L12T0E61PNA  
(CANNON PART # PVAOR24861PNC)

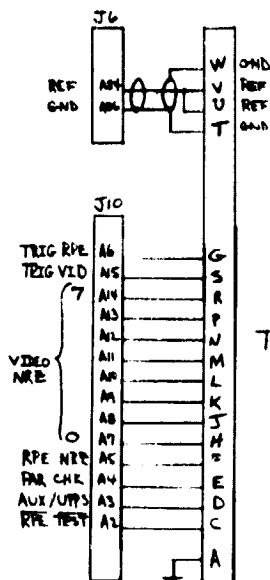
TO UPPS



CONNECTOR J102

BURNDY (23-55)  
20 GA 56 PIN  
MALE  
PART # L22T0E55PNA  
(CANNON PART # PVAOR23855PNC)

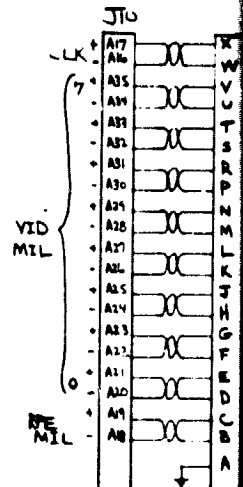
TO UPPS



CONNECTOR J103

BURNDY (16-26)  
20 GA, 26 PIN  
MALE  
PART # L16T0E26PNA  
(NORMAL POLARIZATION)  
(CANNON PART # PVAOR16265PNC)

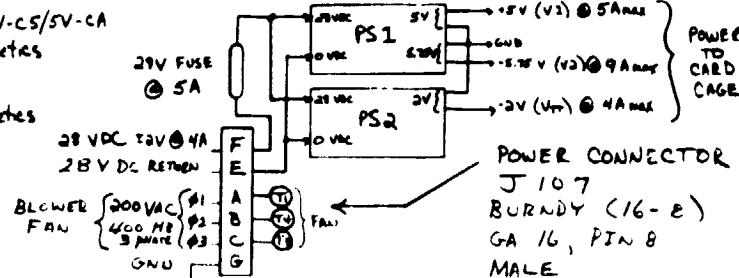
TEST



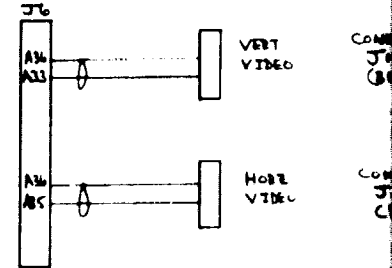
CONNECTOR J104

BURNDY (16-26)  
20 GA, 26 PIN  
FEMALE  
PART # L16T0E26PNA  
(NORMAL POLARIZATION)  
(CANNON PART # PVAOR16265PNC)

PS1: ASN-M5.5/4V-C5/5V-CA  
Arnold Magnetics  
PS2: SHU-2/4V  
Arnold Magnetics



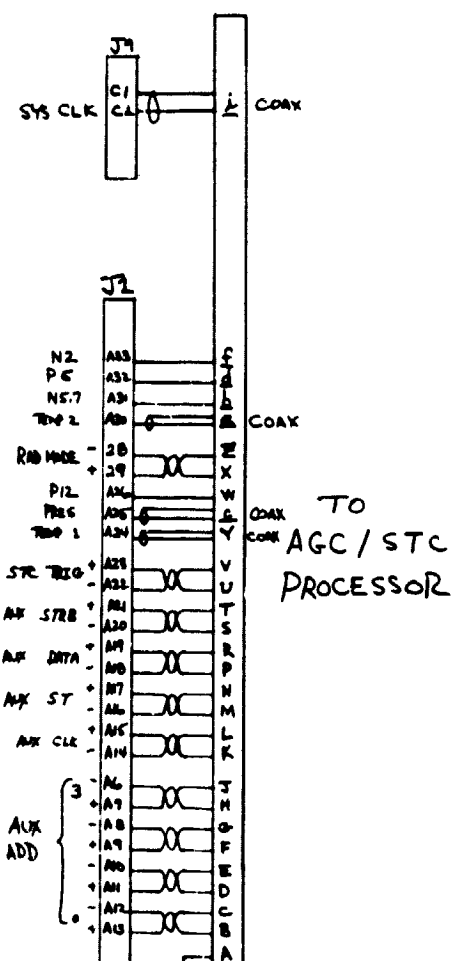
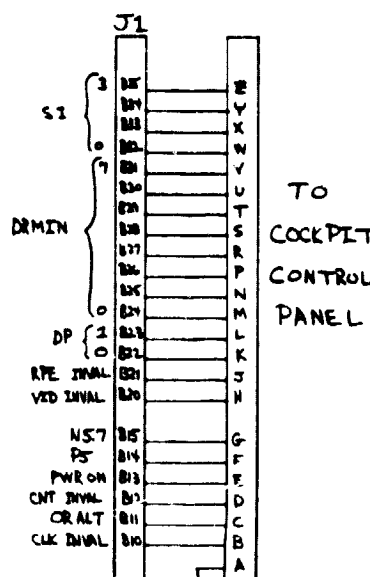
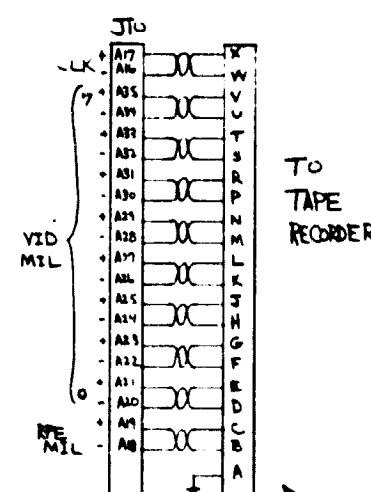
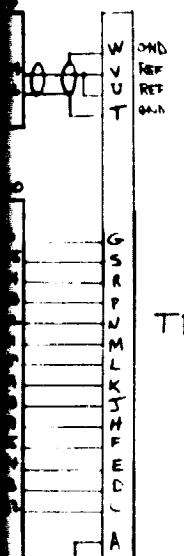
POWER CONNECTOR J107  
BURNDY (16-E)  
GA 16, PIN 8  
MALE  
PART # L16T0E8PNA  
(CANNON PART # PVAOR168PNC)



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FOLOUT FRAME

REVISED	DATE	BY
A	5/5/74	100074
B	5/5/74	100074
C	5/5/74	100074

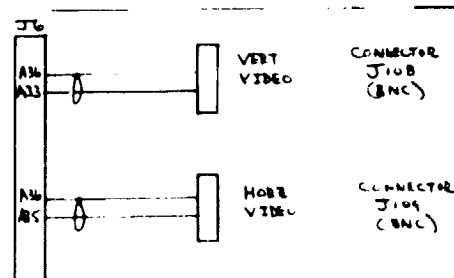


BURNDY (16-26)  
20 GA, 26 PIN  
FEMALE  
PART # L16T0E26 PNA  
(W POLARIZATION)  
(CANNON PART #  
PYAOR16 B26 SWC)

BURNDY (16-26)  
20 GA, 26 PIN  
FEMALE  
PART # L16T0E26 SVA  
(W POLARIZATION)  
(CANNON PART #  
PYAOR16 B26 SWC)

BURNDY (16-26)  
20 GA, 26 PIN  
FEMALE  
PART # L16T0E26 SNA  
(N POLARIZATION)  
(CANNON PART #  
PYAOR16 B26 SWC)

BURNDY (22-95)  
20 GA, 26 PIN, 6 COAX pins  
FEMALE  
PART # L22T0E95 SNA (COAX)  
(AMPHENOL PART #  
US-10233-223-102  
COAX)



NOTE: DDRS CONNECTORS  
TYPE - MINITURE CIRCULAR CONNECTORS  
SHELL STYLE - (ARROW) SQUARE FLANGE  
COUPLING - THREE LOCK BAYONET  
CLASS 1 TERMINATION - CONDUCTIVE FINISH WITH ENVIRONMENT  
RESISTANT (GROMMET WIRE SEAL  
PINS - CRIMP TYPE

REVISION	APPROVED	DATE	DESIGNED BY	DO NOT SCALE DRAWING	DDR SYSTEM 1 BACK PANEL CONNECTORS	APP NO	APPLIED RESEARCH LABORATORIES THE UNIVERSITY OF TEXAS AT AUSTIN
LET NUMBER DATE	DATE	DATE	DATE	DATE	NATIONAL NAS9-15217-4	SCALE	
A 5/18/72		5/15/72					D Drawing No 13
B 5/25/72							
C 5/25/72							
D 5/25/72							

20100000 FRAME 2

J3 in the backplane through the five ribbon cables (CAB 1 - CAB 5) and the plug connector (P3) which are mounted on the cable board (in slot 3).

Intercconnections between the card cage and the enclosure back panel are made by ribbon cables (for digital signals) and by coaxial cable (for analog signals) as specified in Dwg. No. 3. Digital signals leave the card cage backplane from connectors J1 and J10, which are mounted in slots 1 and 10. Unlike the other backplane connectors, J1 and J10 have no circuit boards plugged into them, but serve merely to connect the ribbon cables from the cylindrical I/O connectors on the enclosure to the backplane wiring on the card cage.

## 2. Circuitry Description and Theory of Operation

### a. Overview

The DDRS circuitry is partitioned into seven circuit boards, six of which are contained inside the main enclosure and one of which is in the AGC/STC processor unit. An effort was made to assign each circuit board a unique function, rather than randomly distribute the required system components among an arbitrary number of boards. Furthermore, the circuitry is composed of a very high speed section employing emitter coupled logic (ECL) and a medium speed section of transistor-transistor logic (TTL), each having very different requirements in terms of supply voltages and circuit layout. Finally, there simply was not enough room in the space allotted for the DDRS in the equipment pallet to fit in all the required circuitry and power supplies. So a seventh board (the auxiliary data board), containing all the components requiring  $\pm 15$  V supplies, was fabricated to go in the AGC/STC processor unit, where  $\pm 15$  V was already available.

The seven circuit boards perform the following functions:

Clock Generator Board (4-layer printed circuit - slot 9): Generates "clock" pulses which cause the radar video signals to be sampled

and digitized at a programmable frequency and with a programmable delay with respect to the STC trigger.

Phase locks the sample pulses to the 2.07065 MHz radar timing clock.

Provides detection of an out-of-lock condition in the phase lock loop.

Contains temperature and pressure sensors.

Video A/D board (4-layer printed circuit - slot 6): Converts the instantaneous horizontal and vertical video voltages into two digital data words, upon receipt of a sample pulse from the clock generator board.

Truncates the data words to a programmable number of bits (1, 2, 4, or 7) and steers the retained bits into the video memory to allow for packing of data words less than 8 bits long into 8-bit wide storage.

Adds an even parity bit to 7-bit data words.

Tests for overrange (clipping) of the video signals at the sampling times.

Provides a reference dc output to the test connector for testing purposes.

Video memory board (4-layer printed circuit - slot 4): Stores the video data words at the high sampling rates and reads them back out at the lower recording range.

Packs 4-, 2-, and 1-bit data into 8-bit words.

Multiplexes horizontal and vertical data words onto eight lines as they are read out of the memory.

Video formatting board (wirewrap - slot 11): Demultiplexes and formats the horizontal and vertical video data words from the video memory into eight channels of FLAMR-formatted serial data.

Miller-encodes the eight video channels and outputs them through differential line drivers to the wideband tape recorder.

Sets the 1.92 MHz recording clock rate.

Tests for activity on the video and RPE outputs to the tape recorder and alerts the operator in the case of an inoperative channel.

Radar parameters and environment (RPE) formatting board (wirewrap - slot 8):

Commutes and formats data words from the UPPS, the auxiliary data board, and the cockpit control panel switches, as well as data words generated on the RPE formatting board, into a single FLAMR-formatted serial data stream.

Measures the interpulse period (IPP).

Generates frame numbers.

Tests the phaselock of the clock generator board and alerts the operator of loss of lock.

Counts the video memory parity errors.

Miller-encodes the RPE output data stream.

Interface board (wirewrap - slot 2): Converts ECL-level logic signals to TTL-level, and vice versa.

Receives differential TTL signals and  $\pm 5$  V signals and converts them to single ended TTL.

Checks the cockpit control switch settings against a programmed set of valid settings and alerts the pilot if his settings are invalid.

Checks the parity of the video data as they are read out of the video memory.

Counts the number of A/D samples that were clipped.

Auxiliary data conversion board (wirewrap - inside the AGC/STC processor unit): Converts 16 channels of auxiliary analog information (temperatures, pressure, voltages, radar parameter signals) into 12-bit digital words.

Outputs the 12-bit words to the RPE formatting board to be formatted into the RPE data tape track.

Measures the temperature inside the AGC/STC processor unit.

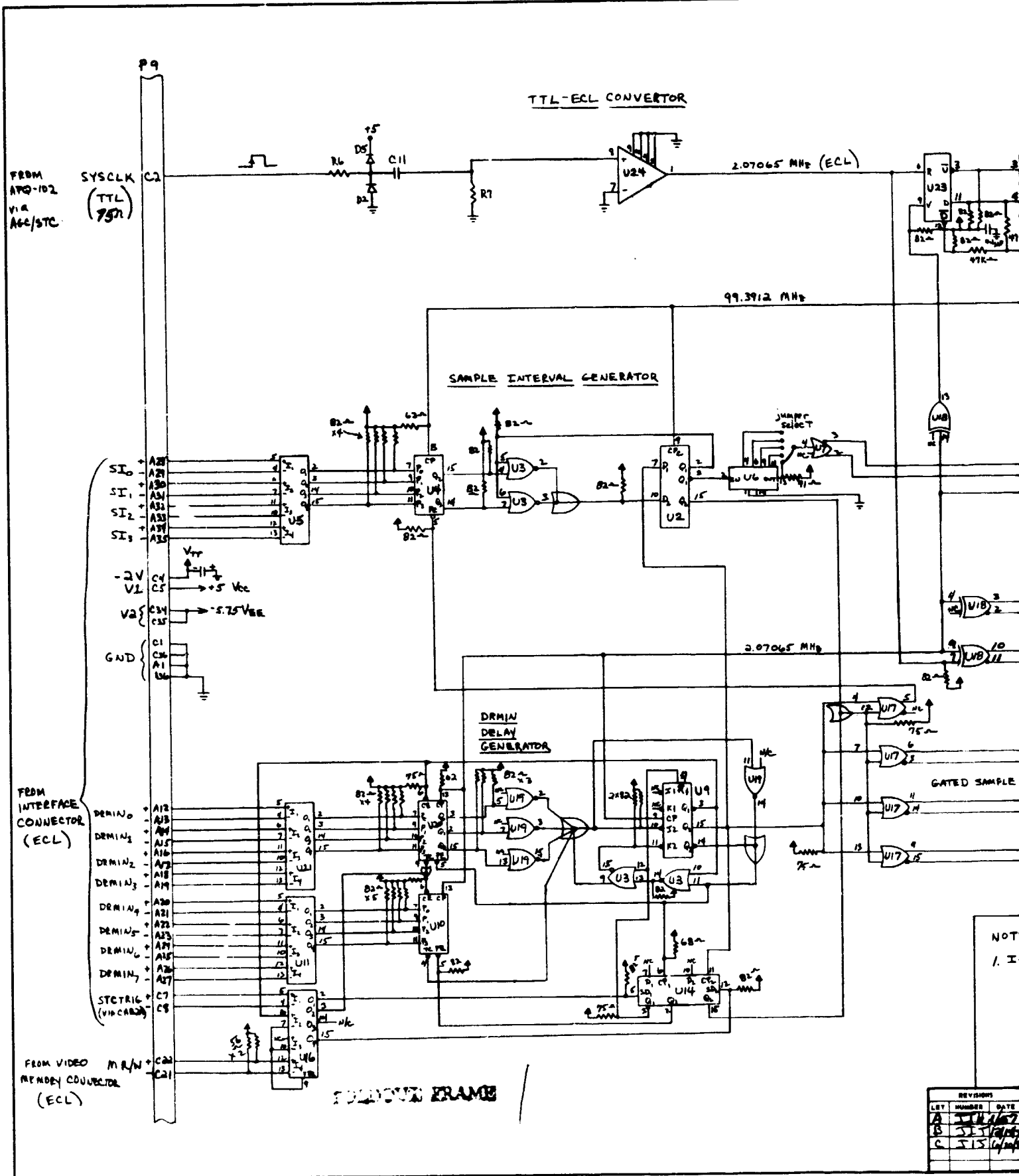
Buffers the STC trigger and radar mode output signals from the AGC/STC processor unit to the DURS.

b. Detailed Board-by-Board Description

(1) Clock Generator Board (Dwg. No. 4)

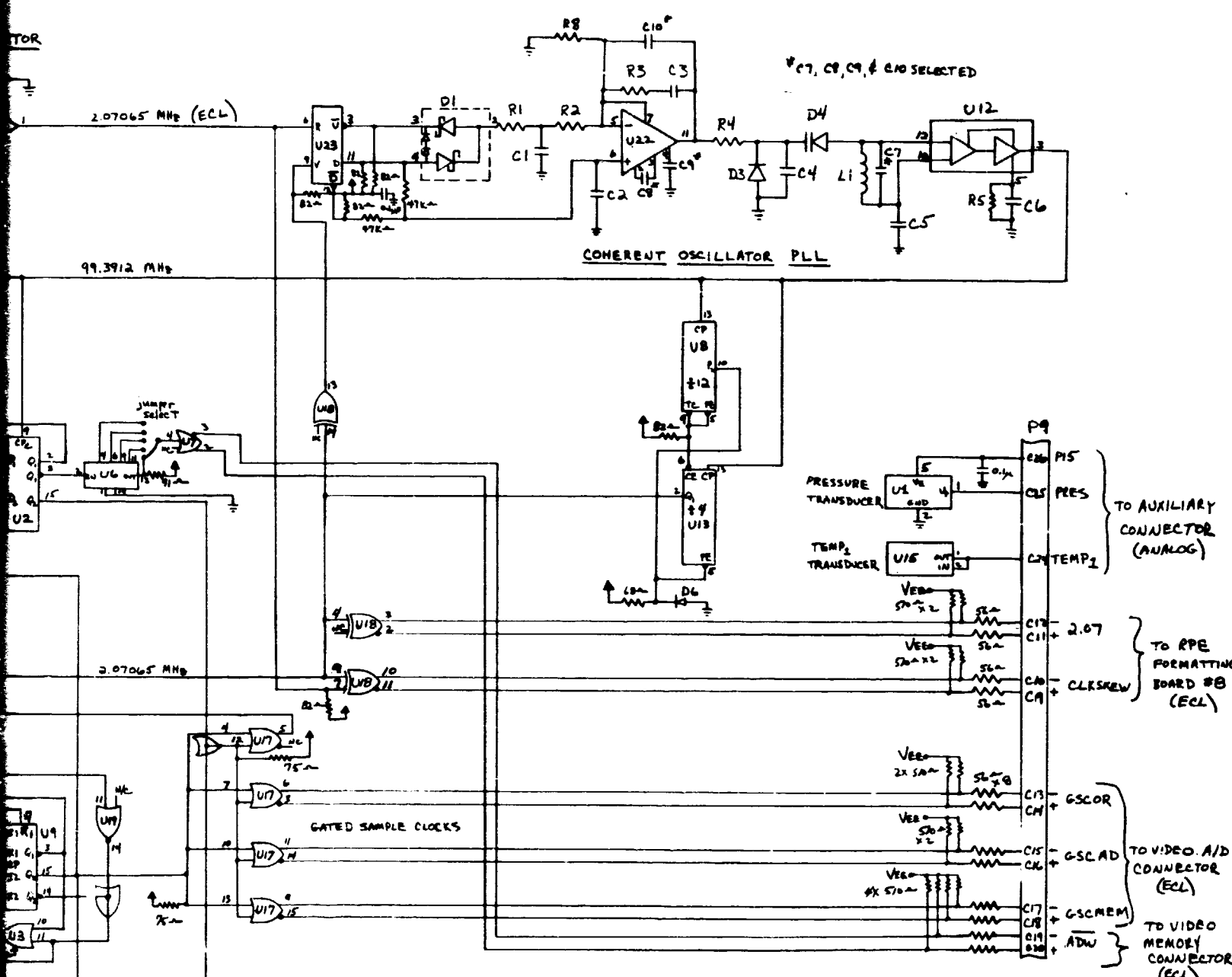
The primary input to the clock generator board is the SYCLK clock signal at 2.07065 MHz. This signal is clipped at +5 V and ground, and then converted to ECL levels by U24. ECL logic signals are described in Appendix D, Section 1.

The primary output of the circuit is the gated sample clock, the three identical copies of which are called GSCOR, GSCAD, and GSCMEM. Since this clock must be phase coherent with SYCLK but at a much higher frequency, a coherent oscillator at 99.3912 MHz is employed which is phase locked to the 2.07065 MHz SYCLK. U12 is an ECL oscillator; its



REVISIONS		
LET	NUMBER	DATE
A	1	JIS/1/79
B	2	JIS/2/79
C	3	JIS/3/79





NOTES:

1. IC POWER PIN ASSIGNMENTS:

DIP NO.	+5V PIN	GND PIN	-5V PIN
U16	—	3	7
U23	—	1,14	7
U12	—	1,14	7,8
U22	12	—	10
U24	11	3,14	6
U3	—	2	—
U6	—	1,16	—
ALL OTHERS	—	1,16	—

- POWER SUPPLY BYPASS CAPACITORS NOT SHOWN
- CIRCUIT IS CONTAINED ON 7.5" X 4.5" PC BOARD
- CONNECTOR P9 IS MURAC #3612056-01 72-PIN RIGHT ANGLE PLUG WITH SOLDER CONNECTORS.
- CIRCUIT BOARD PLUGGED INTO SL T 9 OF SYSTEM RACK AND CONNECTED TO J9 (#3612251-01 72-PIN RECEPTACLE) IN THE BACKPLANE.

REVISIONS	APPROVED	DATE	DESIGN ENGINEER	DO NOT SCALE DRAWING	JOB NO.
LET NUMBER DATE		2/15/79			
A					
B					
C					
CHECKED					
DRAWN					

FINISH	CLOCK GENERATOR BOARD 9	JOB NO.	APPLIED RESEARCH LABORATORIES THE UNIVERSITY OF TEXAS AT AUSTIN
HEAT TREATMENT	MATERIAL NAS9-15217-4	SCALE	D Drawing No 4
NO. 0000			

frequency is established by the resonance frequency of L1 in parallel with C7 and the reverse junction capacitance of varactor diode D4. The output of U12 is a phase coherent 99.3912 MHz timing signal used to synthesize the sampling frequency. It is divided by 48 in U8 and U13 to produce a 2.07065 MHz square wave coherent in phase and frequency to SYSCLK. Phase comparator U23 compares the phase of the SYSCLK signal to that of the synthesized 2.07065 MHz square wave; any phase difference results in correction pulses at pins 3 and 11 of U23. These pulses either sink or source current through Schottky diode bridge D1 to the integrating circuit built around the high speed operational amplifier U22. The integrated correction pulses at the output of U22 are connected to the cathode of the varactor D4 in order to correct the output frequency by changing the capacitance of D4. This closes the loop and ensures phase coherence.

The phase lock loop natural frequency and damping factor are set by R1, R2, R3, and C3. Loop stability is improved by C1 and C4. C8, C9, and C10 frequency compensate the operational amplifier. R6 injects a small dc current into the integrator, which results in a small constant phase offset in the VCO output. It was found when integrating the DDRS with the noisy radar equipment in the pallet that external noise rejection was improved by this phase offset.

The sampling frequency is synthesized by the circuit composed of U2, U3, and U4. The output of U2 at pin 15 is a series of 20 nsec pulses, which is gated (by a wire OR connection) with U14, pin 15. The repetition frequency of these pulses is determined by the programmable counter U4, which divides the 99.3912 MHz coherent clock frequency by any integer from 4-15. The actual divisor integer is set by the logic levels on the programming inputs of the counter; these levels are in turn set by the position of the cockpit "sample interval" switch. The resulting sampling intervals available range from approximately 40 nsec (divide by 4, actually 40.2 nsec) through 150 nsec (divide by 15, actually 150.9 nsec) in 10 n sec intervals.

The circuit composed of U3, U9, U10, U14, U19, and U20 gates the output of the sampling frequency synthesizer. This circuit

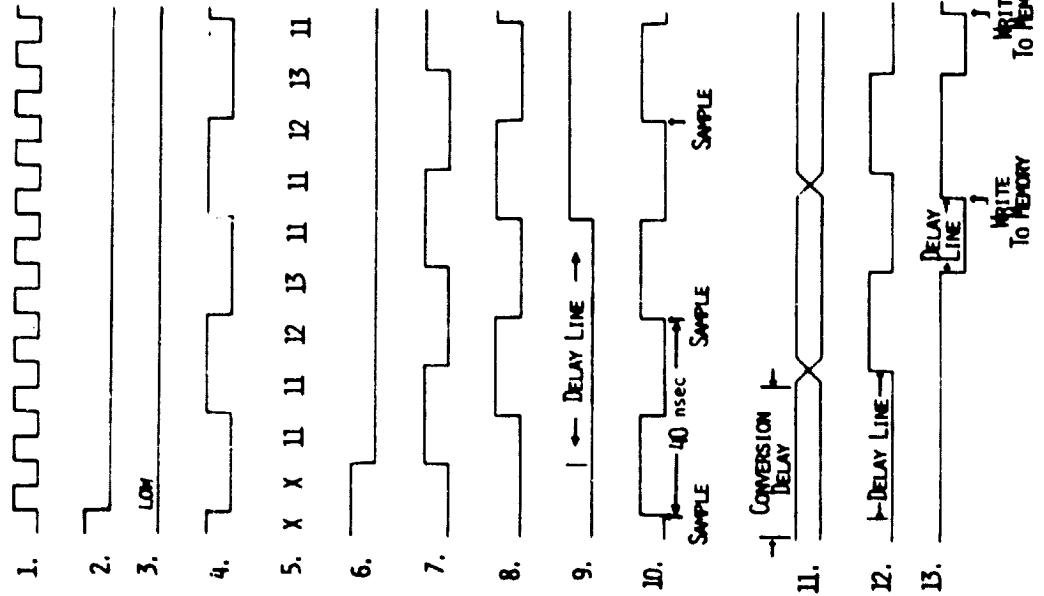
is triggered out of its quiescent state by the STC trigger pulse (STCTRIG), which sets the left side of dual flip-flop U14. This enables the decimal counters U10 and U20 to begin counting up from their pre-set values, which are set by the cockpit DRMIN control switches. The clock input to these counters is the phase locked 2.07065 MHz clock, and their enable input is a 1.035325 MHz signal from U9, pin 3; therefore, the counters increment once every microsecond (actually once every 0.966  $\mu$ sec). The pre-set values from the DRMIN cockpit control switches determine the number of counts (1  $\mu$ sec per count) that the counters must increment before gating "on" the sampling interval generator. After the programmed DRMIN delay has passed since the STC trigger, pin 15 of U9 and pin 15 of U14 have gone false and the sampling clock pulses from pin 15 of U2 are gated through U17 to the video A/D board.

Once the sampling pulses are gated on, they continue until the buffer memory has been filled with one IPP's worth of digitized data. At this time, the video memory board sets the memory read/write (MR/W) line high. This signal sets the right half of flip-flop U14 on the clock generator board, which in turn gates off the sampling clock. At this time, the DRMIN delay circuit has returned to its quiescent state, and awaits the return of MR/W to a low state and the occurrence of the next STC trigger. The net effect of the circuit is to deliver sample pulses to the A/D board in each IPP from the time the DRMIN delay times out after the STC trigger, until the buffer memory is full.

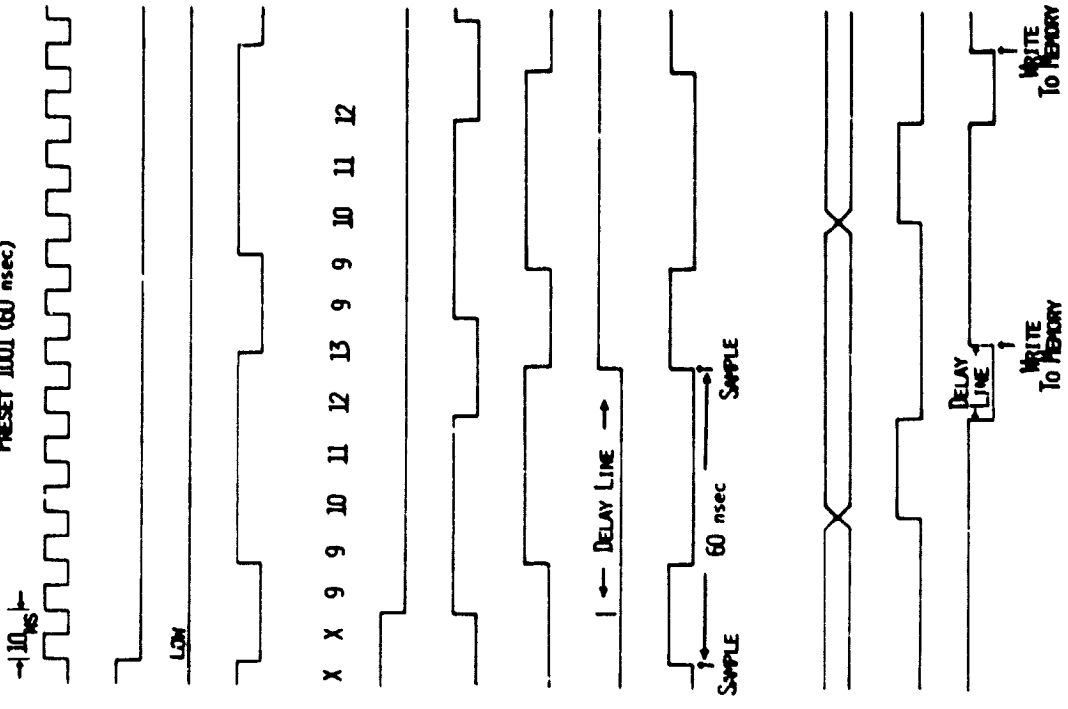
A detailed timing diagram of the sampling interval generator and DRMIN delay generator circuits is found in Figs. 10 and 11 which fully describe the operation of these circuits.

Included on the clock generator board are a pressure transducer and one of the three temperature transducers (TEMP 1) included in the DDRS. The transducer output is connected to the auxiliary data conversion board in the AGC/STC processor unit.

PRESET 1011 (40 nsec)

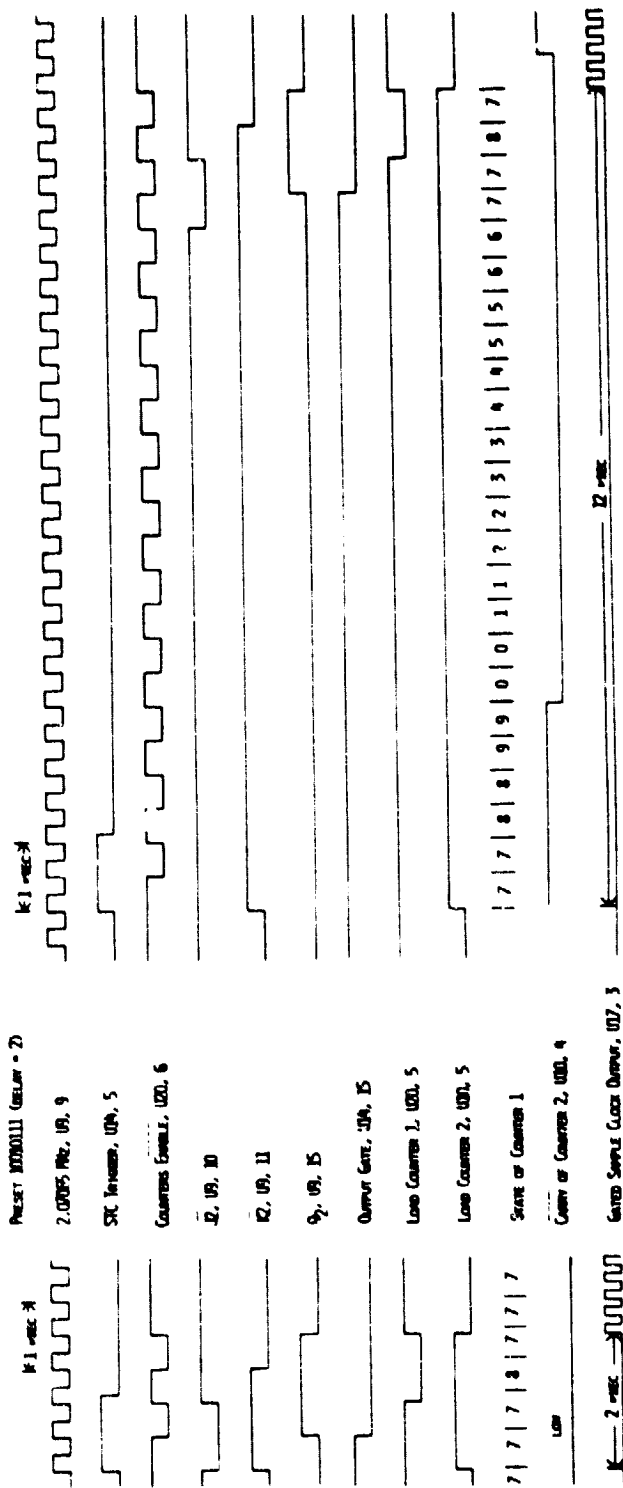


PRESET 1001 (60 nsec)



NOTE: WIRE-OR CONNECTIONS MAY ALTER THE APPEARANCE OF SOME OF THESE SIGNALS ON AN OSCILLOSCOPE. THIS IS A LOGICAL TIMING DIAGRAM, NOT AN ELECTRICAL ONE.

FIGURE 10  
SAMPLE CLOCK TIMING



NOTE: WIRE OR CONNECTIONS MAY ALTER THE APPEARANCE OF SOME OF THESE SIGNALS ON AN OSCILLOSCOPE. THIS IS A LOGICAL TIMING DIAGRAM, NOT AN ELECTRICAL ONE.

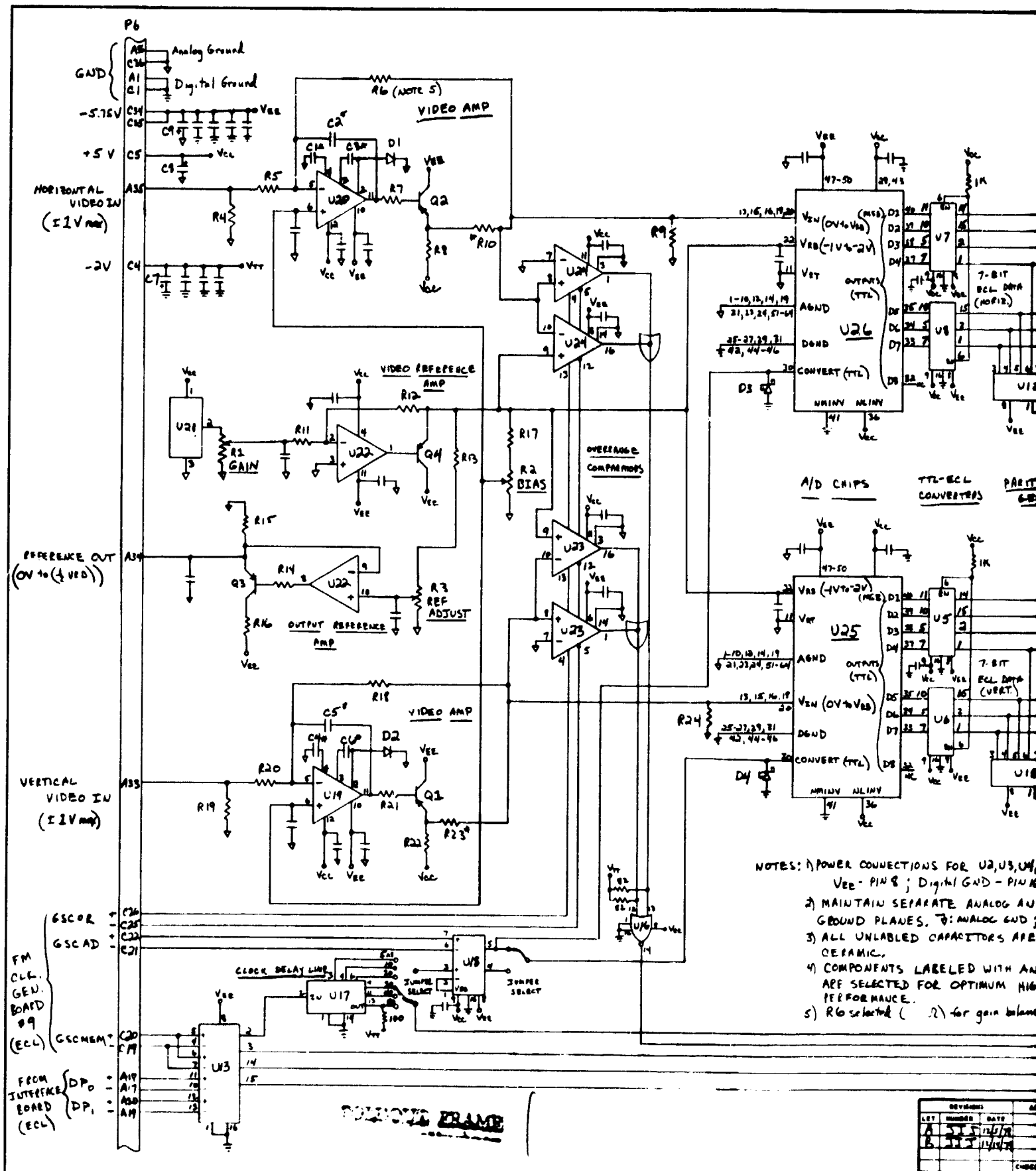
FIGURE 11  
DRMIN TIMING  
(CLOCK GENERATOR BOARD 9)

(2) Video A/D Board (Dwg. No. 5)

The primary inputs to the video A/D board are the two video channels and the three (identical) sampling clocks. The outputs are two channels of quantized video data, a memory write signal, and an overrange count signal.

The heart of the A/D board is the TRW 1007 8-bit, 33 MHz A/D converter integrated circuit (U25 and U26). The limits on the input voltage the chip can quantize are the potential at pin 11 (V RT) on the positive end and the potential at pin 22 (V RB) on the negative end. This voltage range is divided into 256 discrete subranges, to which the chip assigns consecutive 8-bit digital numbers. The most positive voltage (V RT) must be set to ground potential; the most negative voltage (V RB) may be set to between -1 V and -2 V. The A/D conversion is triggered by a TTL level pulse at pin 30 (CONVERT). The output words are TTL level, and one of four different digital encoding schemes may be selected by appropriate TTL levels on pins 36 (NL/NV) and 41 (NM/NV).

The horizontal and vertical video inputs to the video A/D board are bipolar signals of approximately 1 V pp, i.e.,  $\pm 0.5$  V. Video amplifiers U19 and U20 invert the video signals (voltage gain = -1) and offset them by an adjustable voltage (currently set at -0.5 V). The outputs of the video amplifiers have a voltage range of 0 to -1 V with a  $\pm 5$  V input and feed into the analog inputs of the two TRW 1007 chips (one chip for horizontal video and one for vertical). The negative full-scale voltage level at pins 22 of the chips is set by the gain adjustment potentiometer R1, which in conjunction with 2.5 V reference source U21 and voltage inverter U22A, effectively sets the A/D gain of the DDRS. If the video signals turn out to actually be, e.g., 2 V pp, R1 may be adjusted to set negative full scale at -2 V (as measured at the A/D chip, not at the video input; full scale at the input would in this case be  $\pm 1$  V). The bias (offset) of the video amplifier outputs is adjusted by R2, which varies the voltage at the noninverting inputs of the amplifiers from 0 to one-half the reference voltage. It is normally set at one-fourth the

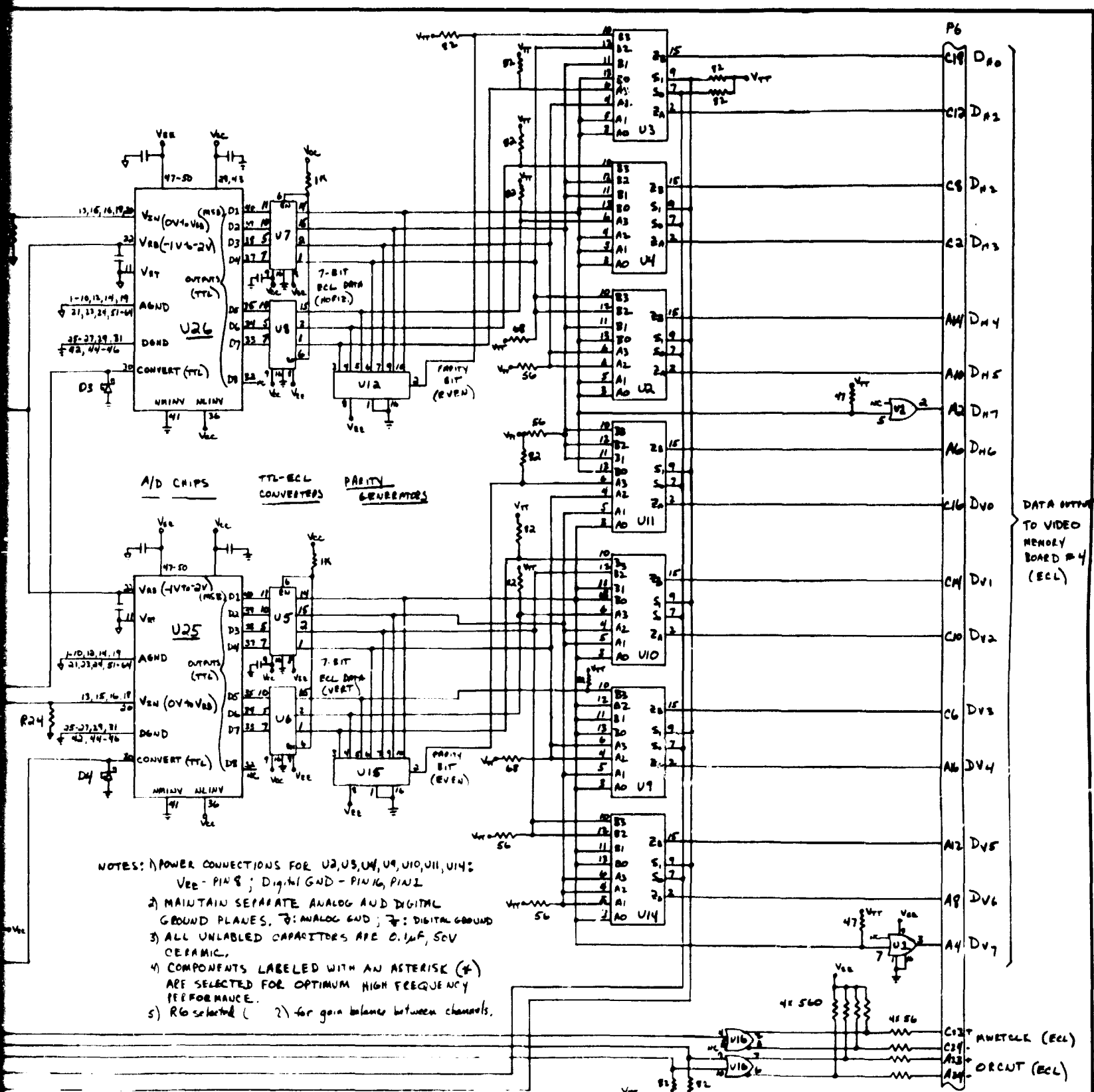


- NOTES:
- 1) POWER CONNECTIONS FOR U2, U3, U4  
VEE - PIN 8; Digital GND - PIN 1
  - 2) MAINTAIN SEPARATE ANALOG AND GROUND PLANES.  $\bar{T}$ : ANALOG GND
  - 3) ALL UNLABELED CAPACITORS ARE CERAMIC.
  - 4) COMPONENTS LABELED WITH AN  $\bar{A}$  ARE SELECTED FOR OPTIMUM HIGH PERFORMANCE.
  - 5) R6 selected (  $\bar{R}$  ) for gain balance

REV	NUMBER	DATE	BY
A	1	11/14/78	
B	2	11/14/78	

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A/D CHIPS      TTL-ECL CONVERTERS      PARITY GENERATORS

- NOTES: 1) POWER CONNECTIONS FOR U2, U3, U4, U9, U10, U11, U14:  
 VEE - PIN 8; Digital GND - PIN 16, PIN 2
- 2) MAINTAIN SEPARATE ANALOG AND DIGITAL GROUND PLANES. ⚡: ANALOG GND; ⚡: DIGITAL GROUND
- 3) ALL UNLABELED CAPACITORS ARE 0.1μF, 50V CERAMIC.
- 4) COMPONENTS LABELED WITH AN ASTERISK (\*) ARE SELECTED FOR OPTIMUM HIGH FREQUENCY PERFORMANCE.
- 5) R6 selected ( ) for gain balance between channels.

DATA OUTPUT TO VIDEO MEMORY BOARD #4 (ECL)

DESIGNED LET NUMBER DATE A 515 12/17/74	APPROVED DATE S 15/17/74	DESIGN ENGINEER CHECKED DATE S 15/17/74	DO NOT SCALE DRAWING P inch HEAT TREATMENT NO BOSS	VIDEO A/D BOARD #6 MATERIAL NAS9-15217-4	JOB NO SCALE D Drawing No 5	APPLIED RESEARCH LABORATORIES THE UNIVERSITY OF TEXAS AT AUSTIN
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FOLDOUT FRAME 2

44  
 47  
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reference voltage; as a result, a grounded video input translates into a one-half full scale voltage at the analog input of the TRW chip. This results in a digital "zero" on the TRW output. In case of an unwanted dc offset in the video signals, this potentiometer may be adjusted to compensate. Since the bias voltage tracks the reference voltage, adjustment of the gain control will not alter the effective bias setting.

Overrange voltage comparator IC's U23 and U24 produce a positive ECL level when the video inputs to the TRW chips exceed the positive or negative full scale levels. These levels are latched by the sampling clock (GSCOR) inside the comparators and are gated with the sampling clock (GSCMEM) to create a sample signal of one pulse per over-range (ORCNT).

A clock delay line, U17, is included to allow timing adjustments of the sampling clock. Provision is made for two jumper selectable delays: one allows the memory write clock (MWRTCLK) to be delayed in order to compensate for propagation delay from the rising edge of the sample clock to the presentation of data to the memory board; the other allows the sample clock to U25 to be delayed with respect to the sample clock to U26, to compensate for different propagation delays through the two TRW chips. The setting of these timing adjustments will be discussed in Sec. IV.

All logic signals to the TRW A/D chips are TTL level. U5, U6, U7, U8, and U18 perform ECL to TTL and TTL to ECL conversions. Separate ground planes are maintained on the board; the analog ground plane is ground for all analog components, while the digital ground plane is ground for all digital components. The two grounds are connected on the backplane where the video A/D board plugs in.

The output code selected by the NMINV and NLINV lines on the TRW chips is positive-true 2's complement:

DDRS VIDEO INPUT	A/D CHIP DIGITAL CODE
	MSB    LSB
+ full-scale:	01111111
+ one-step:	00000001
zero:	00000000
- one-step:	11111111
- full-scale:	10000000

The least significant bit (LSB) of this code is dropped by U12 and U15 and replaced by an even parity bit.

According to the data precision selected, each data word from the A/D's and parity generators is truncated and has its individual bits steered to the proper buffer memory chip by multiplexers U2, U3, U4, U11, and U9, U10, U11, U14. The following data patterns are output to the video memory board on lines  $D_{V0}-D_{V7}$  (and  $D_{H0}-D_{H7}$ ):

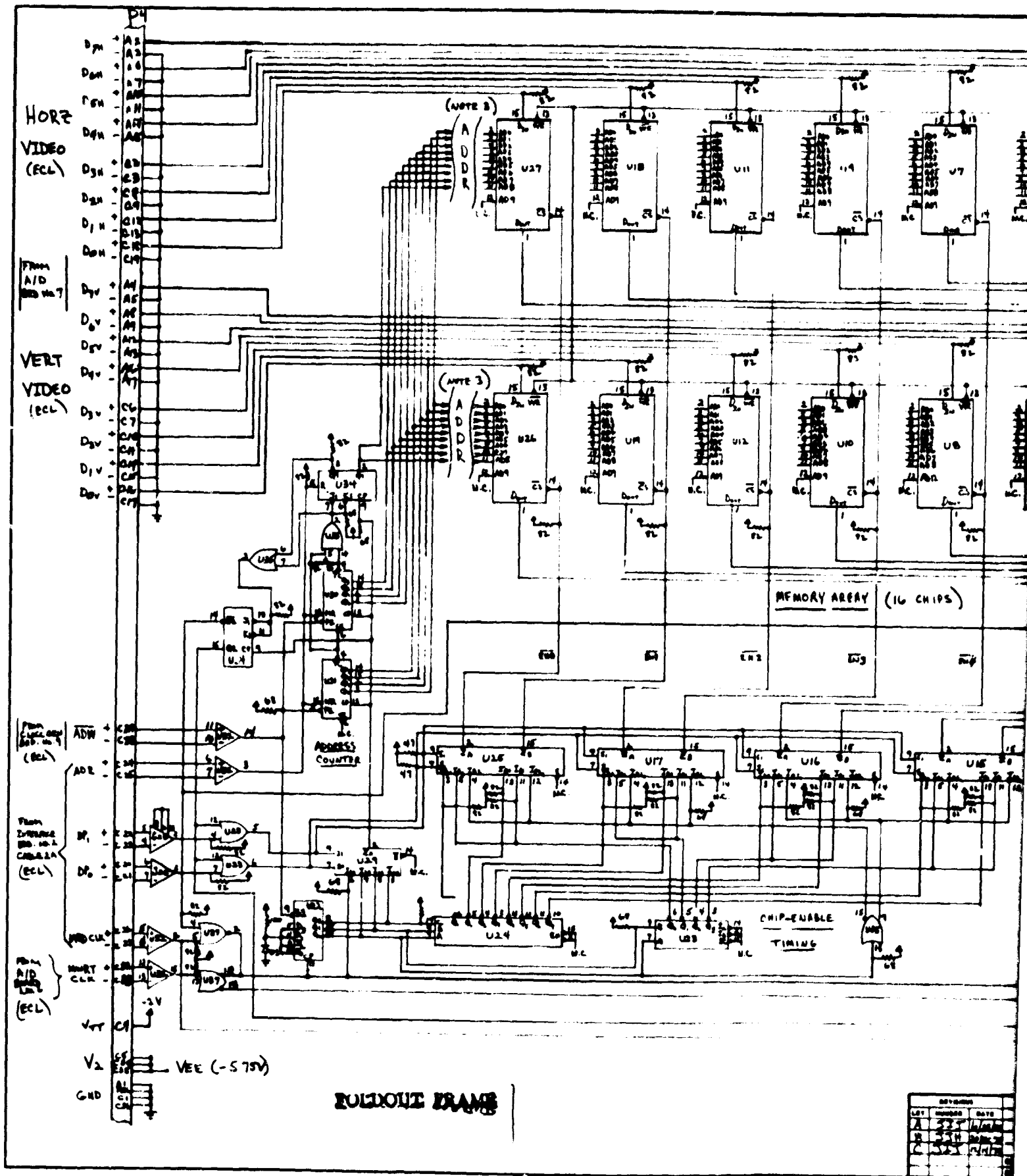
<u>Data Precision</u>	<u><math>D_{V7}</math></u>	<u><math>D_{V6}</math></u>	<u><math>D_{V5}</math></u>	<u><math>D_{V4}</math></u>	<u><math>D_{V3}</math></u>	<u><math>D_{V2}</math></u>	<u><math>D_{V1}</math></u>	<u><math>D_{V0}</math></u>
7 bit	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$	P
4 bit	$D_1$	$D_2$	$D_3$	$D_4$	$D_1$	$D_2$	$D_3$	$D_4$
2 bit	$D_1$	$D_2$	$D_1$	$D_2$	$D_1$	$D_2$	$D_1$	$D_2$
1 bit	$D_1$	$D_1$	$D_1$	$D_1$	$D_1$	$D_1$	$D_1$	$D_1$

Notes:  $D_1$ (MSB)- $D_7$  refer to outputs from the TRW A/D chip.  
P is the parity bit.

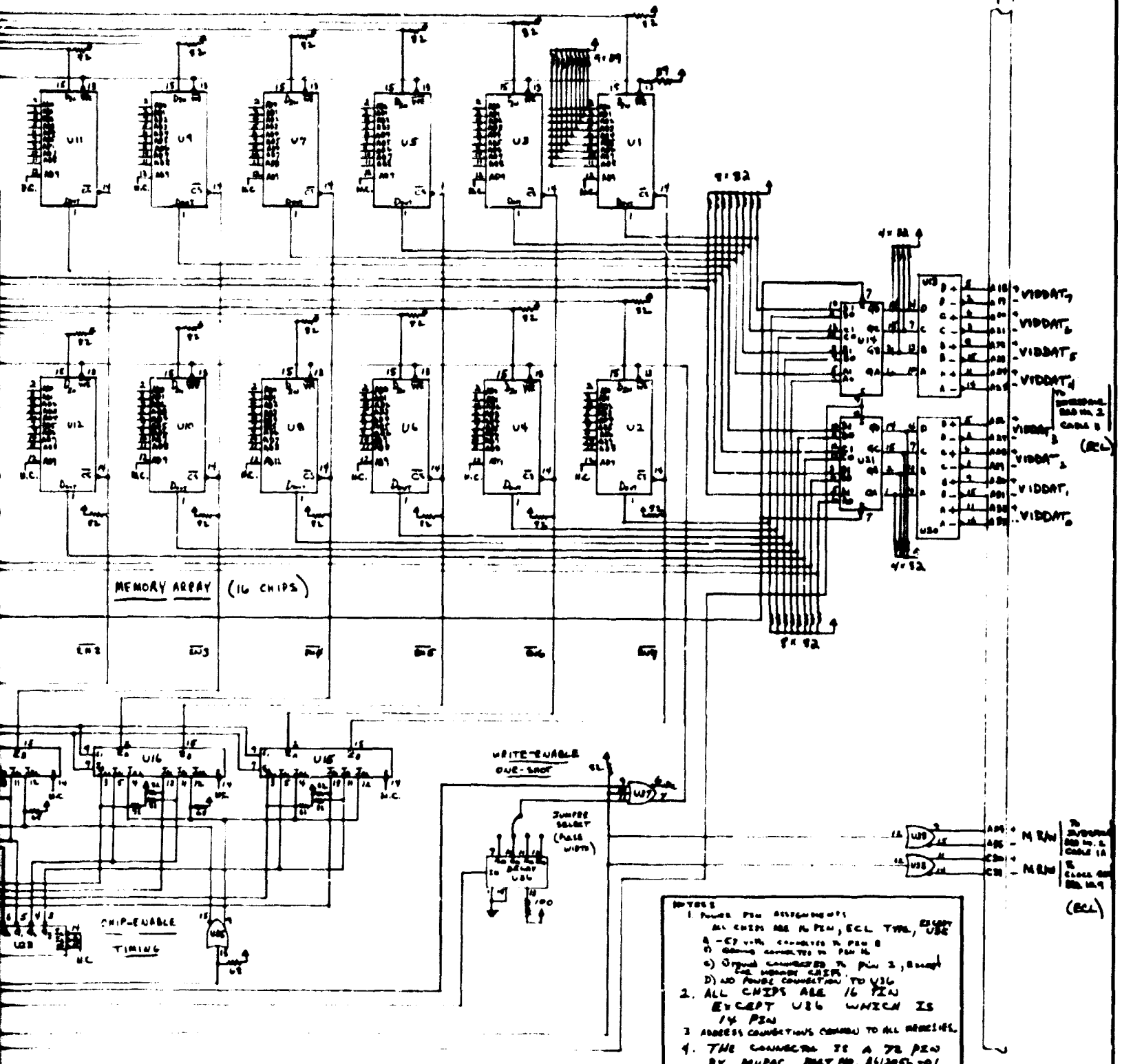
As shown above, only 7-bit data words contain a parity bit.

### (3) Video Memory Board (Dwg. No. 6)

The data patterns from the video A/D board are temporarily stored in 1024 by 1-bit random access memory (RAM) IC's on the video memory board. Separate write clock and read clock inputs are provided on the board so that the data in the memories may be read out at a slower rate than they are written in. The board produces a key



REV	DATE
A	5/25/78
B	6/21/78
C	6/21/78



**NOTES**

- POWER PIN ASSIGNMENTS  
 ALL CHIPS ARE 16 PIN, ECL TYPE, EXCEPT  
 A-C7 WHICH CONNECTED TO PIN 8  
 D) SIGNAL CONNECTED TO PIN 16  
 E) SIGNAL CONNECTED TO PIN 2, BUILT FOR MEMORY CHIPS  
 F) NO POWER CONNECTION TO V16
- ALL CHIPS ARE 16 PIN EXCEPT U86 WHICH IS 14 PIN
- ADDRESS CONNECTIONS COMMON TO ALL DEVICES.
- THE CONNECTOR IS A 78 PIN BY MUPAC PART NO. 813056-01
- POWER SUPPLY BYPASS CAPACITORS NOT SHOWN
- P4 IS MUPAC 813056-01, AND PLUGS ARE IN BACK PANEL.

<table border="1"> <tr> <th>REV</th> <th>CHANGED</th> <th>DATE</th> <th>BY</th> </tr> <tr> <td>A</td> <td></td> <td>12/17/76</td> <td></td> </tr> <tr> <td>B</td> <td></td> <td></td> <td></td> </tr> <tr> <td>C</td> <td></td> <td></td> <td></td> </tr> </table>	REV	CHANGED	DATE	BY	A		12/17/76		B				C				APPROVED: _____ DATE: _____ DESIGNER: _____ CHECKED: _____ DRAWN: _____	DO NOT SCALE DRAWING PART TOLERANCES AS SHOWN	VIDEO MEMORY BOARD No. 4 NATIONAL NAS9-15217-4	APPLIED RESEARCH LABORATORIES THE UNIVERSITY OF TEXAS AT AUSTIN SCALE: D Drawing No 6
REV	CHANGED	DATE	BY																	
A		12/17/76																		
B																				
C																				

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control signal, MR/W, which sets the DDRS in either the acquire-data state or the record-data state.

When DRMIN times out after the STC trigger, the clock generator board begins sending sampling pulses to the A/D board. These pulses are delayed on the A/D board (to allow the digitized video samples to propagate through the A/D board) and sent to the video memory board as a memory write clock (MWRTCLK). The pulses are 20 nsec wide and positive going. The rising edge of each pulse is used to clock the address counter composed of U30, U31, and U34; the falling edge triggers the write-enable one-shot composed of U36 and U37. The address counter increments from 0 to 511 and drives the address lines of the RAM; note that only the first 512 (out of 1024 total) locations in the RAM chips are used. The write-enable one-shot generates a negative going pulse to the write-enable input of each RAM chip when triggered. The width of this pulse is set by tapped delay line U36 and can be set to 12, 14, 16, or 18 nsec. The 20 nsec between the rising and falling edges of the write clock pulse allows the address lines to the RAM chips to settle at least 5 nsec before the write-enable pulse arrives, as specified by the RAM data sheet (Fairchild 10415A).

Each RAM chip has an enable input which must be brought low for data to be written or read. This input is used to control the number of parallel data bits that are written for each A/D sample, which depends on the data precision requested. For 7-bit data plus parity, eight parallel bits are required and all enable lines ( $\overline{EN}_7 - \overline{EN}_0$ ) to each 8-bit wide memory bank are brought low. For 4-bit data, first  $\overline{EN}_7 - \overline{EN}_4$  are brought low, then  $\overline{EN}_3 - \overline{EN}_0$  are brought low, and then the address lines are incremented for the next two 4-bit data words. Similarly, for 1-bit data, each enable line is sequentially pulsed low, beginning with  $\overline{EN}_7$  and ending with  $\overline{EN}_0$ , and after all eight enables have been pulsed, the address lines increment for the next round of eight samples. Changes on the enable lines are triggered by the rising edge of MWRTCLK, and all enable lines are stable by the time the write-enable pulse occurs. The chip-enable logic consists of U15, U16, U17, U22, U23, U24, and U25.

Since the address lines must change after every video sample in the 7-bit mode but only after every two, four, or eight samples in the 4-, 2-, and 1-bit modes, respectively, the clock frequency to the address counter must be changed with changes in the data precision. Multiplexer U29 selects the full frequency MWRTCLK or else divided-down frequencies, depending on the state of the data precision ( $DP_0$ ,  $DP_1$ ) lines, and outputs the clock signal to the address counter. The data precision lines are coded as follows:

<u><math>DP_0</math></u>	<u><math>DP_1</math></u>	<u>Data Precision</u>
0	0	1 bit
1	0	2 bit
0	1	4 bit
1	1	7 bit with parity

After the address counter has reached a count of 511, the next rising edge of the clock signal resets the counter to zero and toggles flip-flop U34 at pins 14 and 15. The state of this flip-flop determines whether the memory is in the read or the write mode. U34, pin 15, is the memory read write (MR/W) signal: true means read; false means write. A transition from read to write sets the clock generator board into a quiescent state, waiting for an STC trigger. A transition from write to read starts the video formatting board to immediately begin reading data from the memory.

When the memory is in the read mode, the data precision signals ( $DP_0$  and  $DP_1$ ) are gated true (at U33, pins 5 and 6) so that the memory reads out eight bits at a time. The memory read clock (MRDCLK) is gated on, and the write-enable one-shot (U37, pin 7) is gated off (true). The memory write clock (MWRTCLK) is gated off on the clock generator board. The net result is that the stored memory words are read out by MRDCLK. During this time, the 8-bit output of each memory bank is multiplexed by U14 and U21 onto eight lines ( $VIDDAT_0$ - $VIDDAT_7$ ) to the video formatting board. The multiplexers are controlled by MRDCLK: when MRDCLK is low, the horizontal video memory data appear on the VIDDAT lines;

when MRDCLK is high, the vertical video memory data appear. Figure 12 illustrates the memory read timing.

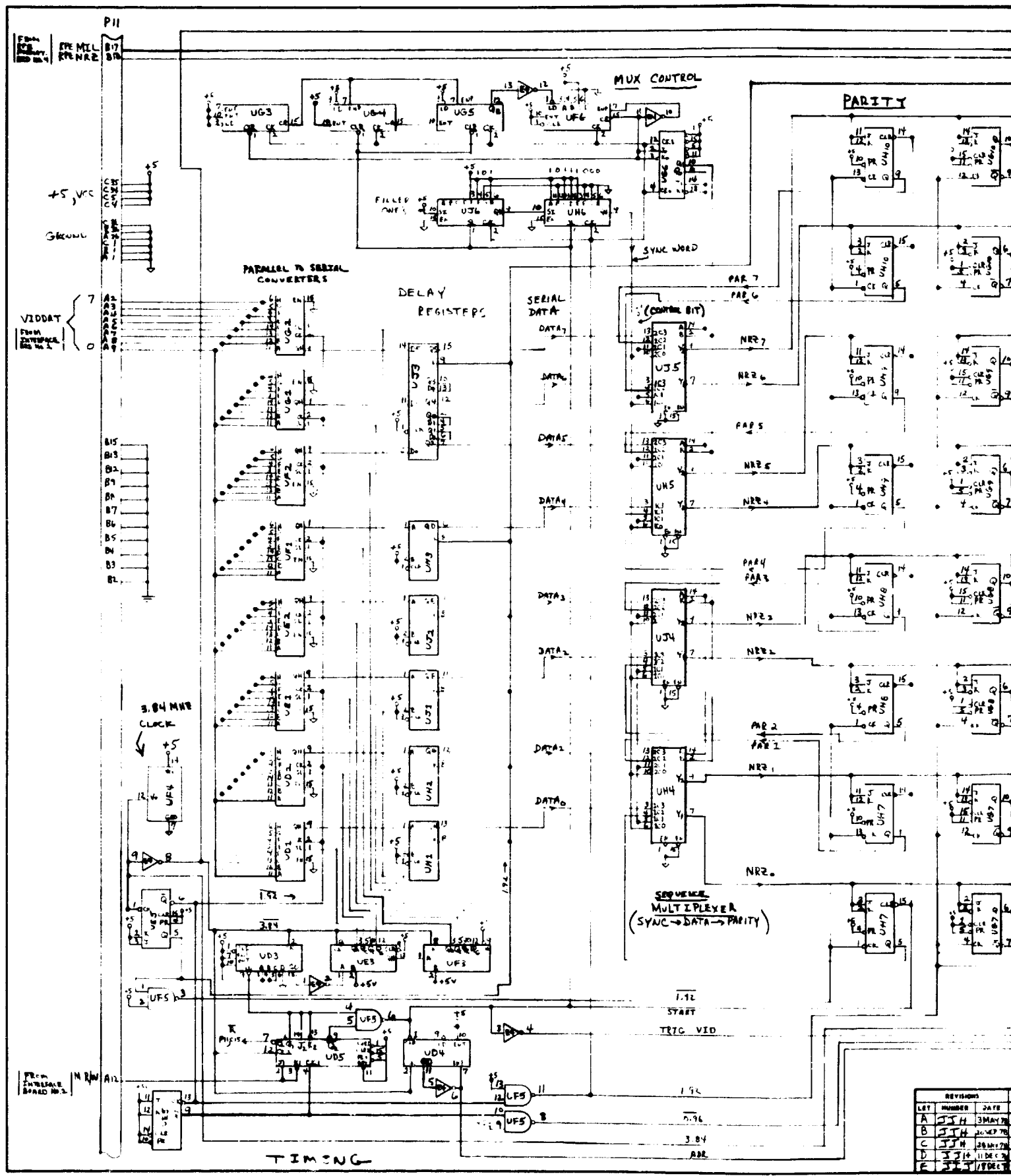
#### (4) Video Formatting Board (Dwg. No. 7)

The detailed timing and operation of the video formatting board is fully described in Fig. 12. A general summary of the board's functions will be given here.

The rising edge of MR/W, signifying that the buffer memory is full and ready to be read, triggers the video formatting circuitry from its quiescent state. This rising edge is synchronous with the sampling clock and, therefore, asynchronous with the 3.84 MHz timing clock in the video formatting board. Flip-flop VD5 synchronizes the rising edge of MR/W, loads the sync word into shift register UH5, and starts it clocking out the sequence multiplexers (UH4, UH5, UJ4, UJ5) to the Miller encoders at 1.92 MHz. Meanwhile, signal ADR clears the address counters in the video memory board for two MRDCLK cycles. Then the parallel-to-serial converting shift registers (VD1, VD2, UE1, UE2, UF1, UF2, UG1, UG2) begin loading data from the memory board. UD1 loads first; its first data word is the first sample of the horizontal video. UG2 loads last; its first data word is the fourth sample of the vertical video.

The outputs of the parallel-to-serial converters are differentially delayed by registers UH1, UH2, UH3, UJ1, UJ2, and UJ3. This ensures that the serial data lines (DATA<sub>0</sub>-DATA<sub>7</sub>) are bit parallel, i.e., the first bit of each data word emerges from the delay registers at the same time. Note that the parallel-to-serial converters are loaded such that the most significant bit (VIDDAT<sub>7</sub>) of a memory data word is shifted out first.

After the sync word has passed through the sequence multiplexers, the multiplexer control lines change state and gate the FLAMR format control bit through the multiplexers. This bit is wired true. One bit time later, the controls again change state and gate the

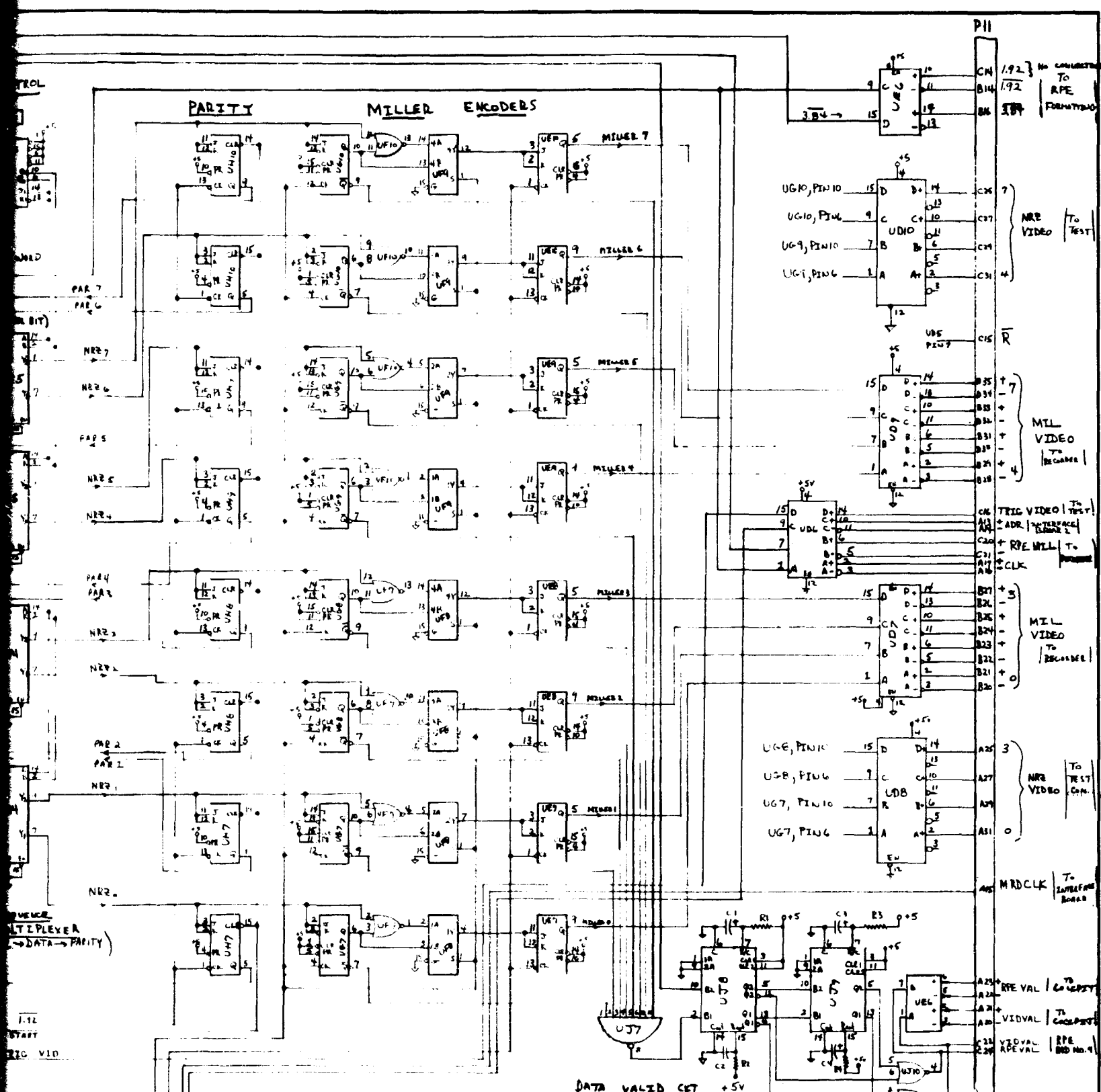


LET	REVISION	NUMBER	DATE
A	JTH	3MAY78	
B	JTH	20-SEP-78	
C	JTH	28-MAR-79	
D	JTH	11-DEC-79	
E	JTH	17-DEC-79	

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SOURCE  
 MULTIPLEXER  
 → DATA → PARITY  
  
 1-12  
 START  
 TRIG VID  
  
 1-5L  
 C-16  
 3-24  
 AM

DATA VALID SET +5V

REVISIONS	APPROVED	DATE	DESIGNED BY	DO NOT SCALE DRAWING	NO. 100
LET NUMBER DATE		5/10/77			
A JTH 3MAY78					
B JTH 26MAY78					
C JTH 28MAY78					
D JTH 11DEC78					
E JTH 17DEC78					
F JTH 17DEC78					

MILLER ENCODER DECIMAL 2 FRACTIONAL 5 ANNUAL 5	FINISH HEAT TREATMENT NO. 0000	<b>VIDEO</b> FORMATTING, BOARD 11 MATERIAL NASA-15217-4	APPLIED RESEARCH LABORATORIES THE UNIVERSITY OF TEXAS AT AUSTIN  <b>D Drawing No. 7</b>
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data lines from the delay registers through to the Miller encoders. At this time, the first bit of each of the first eight data words has appeared at the delay register outputs. 128 words (1024 bits) of data are clocked through the multiplexers at 1.92 Mbs and are counted by the MUX control circuitry (UG3, UG4, UG5), after which the control lines to the multiplexers again change state. Now the outputs of the parity accumulator flip-flops (UH7, UH8, UH9, UH10) are allowed through to the Miller encoders for 1-bit time. After this 1-bit time, the sync word shift register is again gated through the multiplexer; the output of this register (UH6, pin 9) remains true until the sync word is loaded on the next rising edge of MR/W. Thus, the interrecord gap on the wideband tape contains a series of filler ones.

Included on the video formatting board is a data validation circuit (UJ7, UJ8, UJ9, UJ10). This circuit tests for activity on the video and RPE output data lines before Miller encoding. Retriggerable one-shot UJ8 will normally remain constantly triggered. If, however, there is no activity on either the video data lines for approximately 6.6 msec or on the RPE data lines for 81 msec, then the one-shot outputs will go false, and the respective signals VIDINVAL or RPEINVAL to the cockpit will go true. One-shot UJ9 is included to catch short dropouts from UJ8 and stretch them into 1 sec pulses to the cockpit.

#### (5) RPE Formatting Board (Dwg. No. 8)

Operation of the RPE formatting board is controlled by the program counter (UF9, UF10) in conjunction with the control PROM (UE10). The program counter counts from 0 to 31; accordingly, there are 32 possible RPE data sources. Currently, only 30 of these possible sources are recorded; these are shown in line 9 in the timing diagram, Fig. 13. Timing for the entire board is described in this figure.

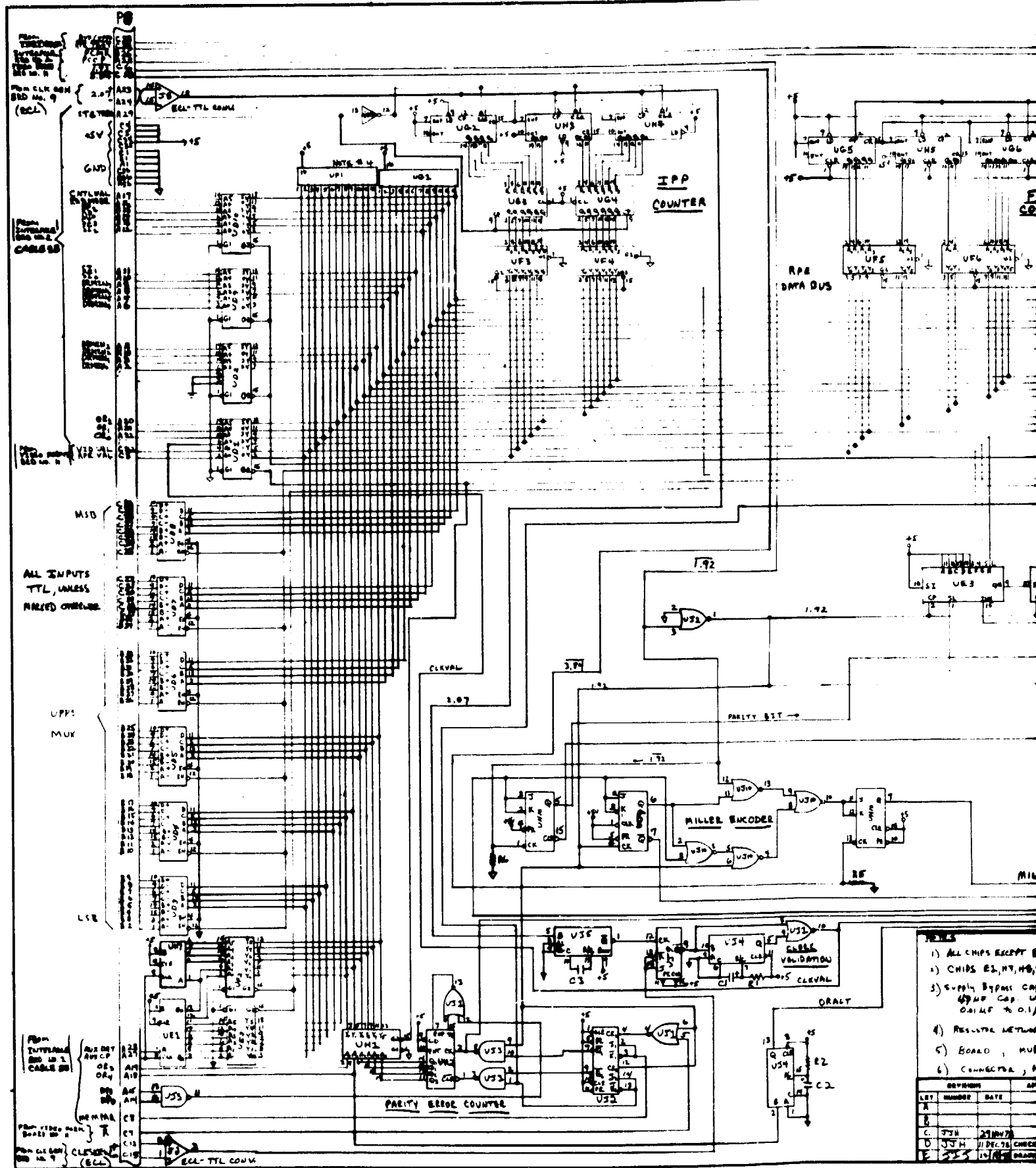
The primary control signals to the board are PCMR and PCCP (lines 2 and 3 of Fig. 13). PCMR, which is the (inverted) strobe signal from the UPPS corresponding to time-of-day, resets the counter to

zero, which initiates the RPE output cycle and accesses the first memory location in the control PROM. The control PROM is programmed as shown in Table IV. Bits 2, 3, and 4 of the PROM output determine the source of the data on the RPE data bus. For the first eleven locations, these bits are all zeroes which, when decoded by UG8, select the UPPS data bus driver (UD3, UD4, UD5, UD6, UD7, UD8). Thus, the first eleven RPE records after a PCMR pulse contain NERDAS data.

Bit 0 of the control PROM output selects either the UPPS strobe or a DDRS internal 15 kHz clock as source of the program counter clock, PCCP. The first eleven PCCP pulses are from the UPPS strobe. While the rising edge of PCCP increments the program counter, the falling edge initiates the output of an RPE data record by enabling the output shift register (UE3, UE4, UE5, UE6, UE7, UE8) to begin shifting the record out. The PCCP rising edge also resets both halves of flip-flop UG9, which commands the output multiplexer (UE9) to gate the data record through to the Miller encoder (UJ9, UJ10, UH11). After 43 bits (11 bits sync, 8 bits address, 24 bits data) have been shifted out of the output shift register, pin 12 of counter UH9 goes false, which causes the record parity bit (even parity) to be gated through the output multiplexer for 1-bit time. At this time, flip-flop UG9 is set, which gates a high level through the multiplexer (interrecord filler one's) until the next rising edge of PCCP.

The contents of each data record are latched into the parallel inputs of the output shift register on the rising edge of PCCP. The first eleven bits are hard-wired as the sync code 00011101101. The next eight bits are the output of the address PROM (UF8). This PROM is programmed as shown in Table IV. The addresses are chosen according to the following criteria:

(a) Parameters most useful during playback and CCT conversion are given the addresses of data which are displayed on the DRIE (at ARL:UT). These parameters are:



From CLK GEN  
SND NO. 9  
(ECL)

From CONTROL  
SND NO. 2  
(ECL)

From CLK GEN  
SND NO. 7  
(ECL)

ALL INPUTS  
TTL, UNLESS  
NOTED OTHERWISE

UPPS  
MUX

LSE

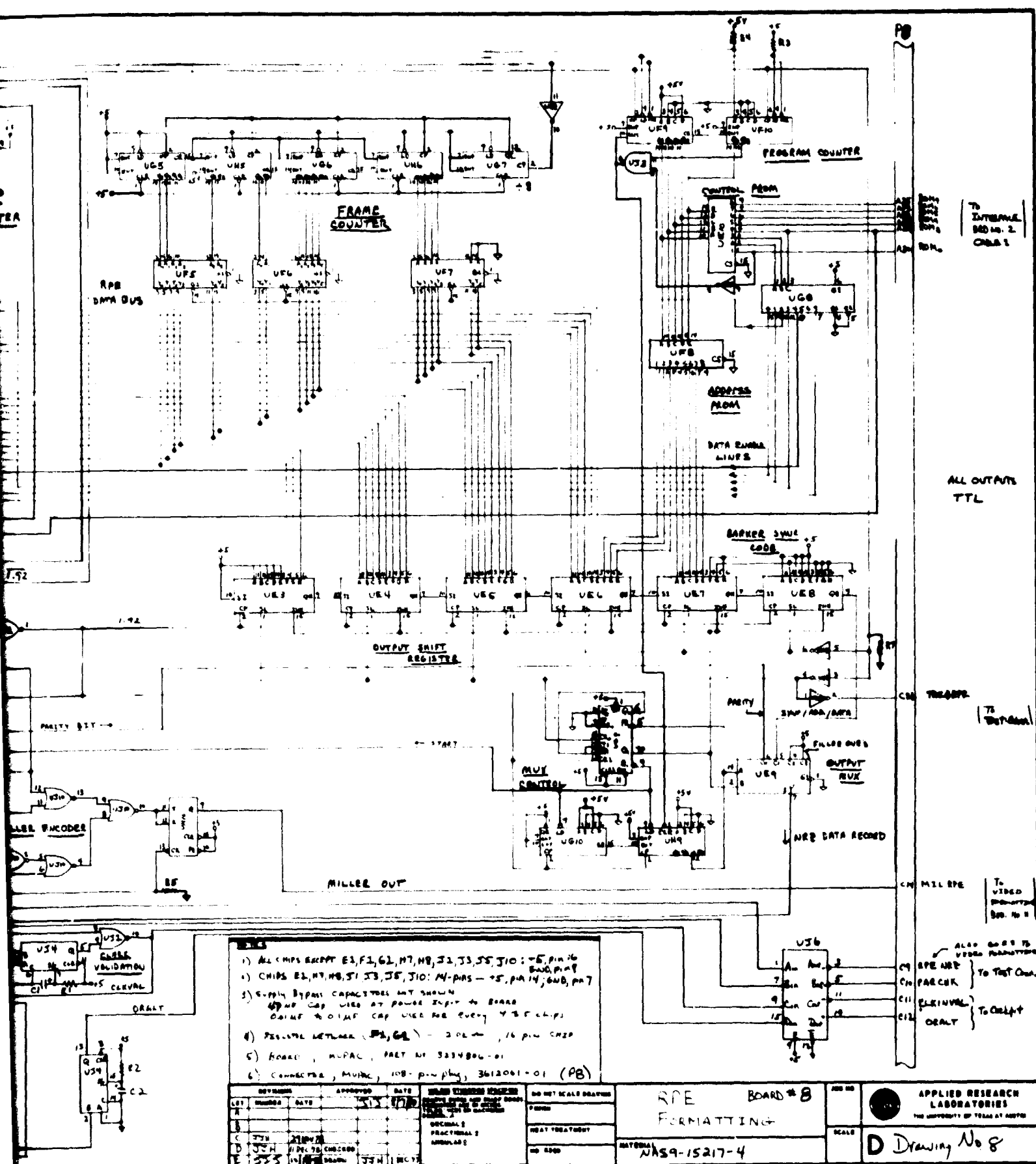
From INTRINSIC  
SND NO. 2  
CABLE 22

From CLK GEN  
SND NO. 9  
(ECL)

- NOTES
- 1) ALL CHIPS EXCEPT
  - 2) CHIPS E2, HT, HS,
  - 3) 5-Pin BYPASS CAP  
49PF CAP U  
OR 10K TO GND
  - 4) RESISTOR NETWORK
  - 5) BOARD, MUX
  - 6) CONNECTOR, M
- | REV | DESCRIPTION | DATE      | AP    |
|-----|-------------|-----------|-------|
| A   |             |           |       |
| B   |             |           |       |
| C   | 27H         | 27 NOV 72 |       |
| D   | 37H         | 11 DEC 72 | CHUCK |
| E   | 37H         | 11 DEC 72 | DRUM  |

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- NOTES**
- 1) ALL CHIPS EXCEPT E3, F1, G1, H7, H8, J1, J3, J5, J10: -E, pin 16
  - 2) CHIPS E3, H7, H8, J1, J3, J5, J10: -E, pin 14, 15, 16, 17
  - 3) Supply Bypass CAPACITORS NOT SHOWN  
470PF CAP USED AT POWER INPUT TO BOARD  
0.01UF CAP USED FOR EVERY 4 IC CHIPS
  - 4) RESISTOR NETWORK (R5, R6) - 20K - 16 pin CHIP
  - 5) BOARD: MUPAC, PART NO 3234806-01
  - 6) CONNECTOR, MILINC, 108-pin plug, 3612061-01 (PB)

REV	DATE	APPROVED	DATE	DESIGN ENGINEER	DO NOT SCALE DRAWING
A					9 DIMS
B					HEAT TREATMENT
C					NO ESD
D					
E					

RPE BOARD #8  
 FORMATTING  
 NATIONAL NAS9-15217-4

APPLIED RESEARCH LABORATORIES  
 THE UNIVERSITY OF TEXAS AT AUSTIN

SCALE: **D** Drawing No 8

TO INTERNAL  
 REQ NO. 2  
 ORG 1

ALL OUTPUTS  
 TTL

TO TEST POINT

TO VIDEO  
 PROPERTY  
 BOX NO 1

ALSO GOES TO  
 VIDEO PROPERTY  
 BOX NO 1

TO TEST CHAMBER  
 TO ORG 1

PROJECT NUMBER 2

1. UPPSTRB (STROBE SIGNAL FROM UPPS): No.2, U3B, 11

2. PCWR (RPE START SIGNAL AT 1st UPPS WORD): No.2, U27, 8

3. PCCP (RPE PROGRAM COUNTER CLOCK): No.8, U9, 2

4. PROGRAM COUNTER LSD (SHOWING PROGRAM COUNT) No.8, U9, 14

5. ROM<sub>0</sub> (CONTROL FROM LSD) No.8, UE10, 1

6. ROM<sub>3</sub> (CONTROL FROM BIT 3) No.8, UE, 4

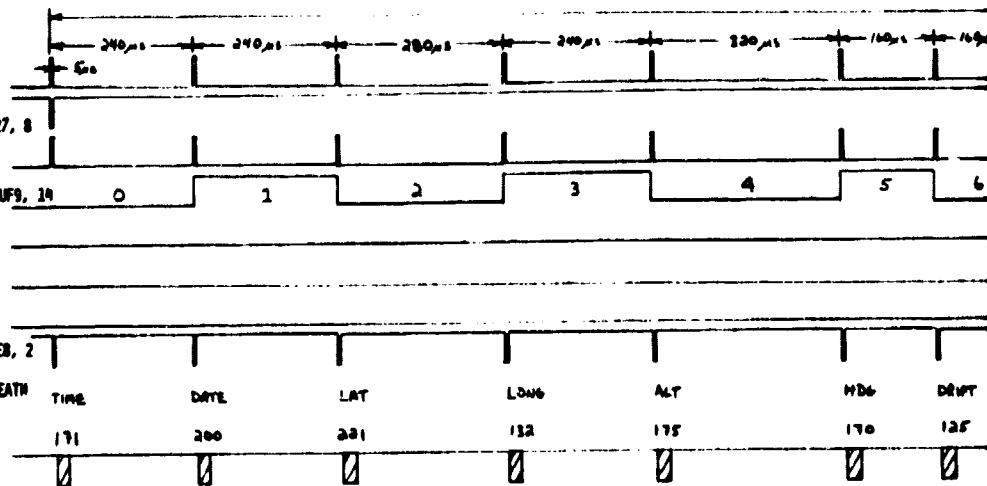
7. AUXADD<sub>0</sub> (LSB TO AUX ANALOG MUX): No.2, U10, 1

8. SHIFT/LOAD TO RPE OUTPUT SHIFT REGISTER: No.8, UE8, 2

9. TYPE OF DATA CONTAINED IN RECORD DIRECTLY UNDERNEATH

10. OCTAL ADDRESS OF RECORD DIRECTLY UNDERNEATH

11. NZZ OUTPUT RPE DATA (☑ - DATA RECORD)



12. 1.92 MHz CLOCK: No.8, U11, 1

13. MROCLK: No.2, U19, 2

14. AUXCLK: No.2, U19, 4

15. PCCP: No.2, U18, 2

16. AUXADD<sub>0</sub>: AUX BOARD, U5, 1  
(LSB OF ANALOG MUX)

17. AUXILIARY DATA ANALOG VOLTAGE (HYPOTHETICAL)  
TO A/D: AUX No. U9, 14

18. AUXST: No.2, U22, 6

19. CONVERT SIGNAL TO AUX A/D: AUX BOARD U9, 1

20. AUXSTRB FROM A/D: AUX BOARD U9, 22

21. No.2, U29, 10

22. AUXCF (CLOCK TO AUX S.R.): No.8, UE1, 8

23. AUXDAT (DATA TO AUX S.R.): No.8, UE1, 1

24. SHIFT/LOAD TO RPE OUTPUT S.R.:  
No.8, UE8, 2

25. No.8, U6, 6

26. RPE OUTPUT (No.8, UE9, 2)

27. MUX CONTROL (No.8, UE9, 14)

28. NZZ RPE OUTPUT RECORD: No.8, UE9, 7

INTER-RECORD FILLER (ONE'S)

*RECORDED*

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RECORD QUALITY

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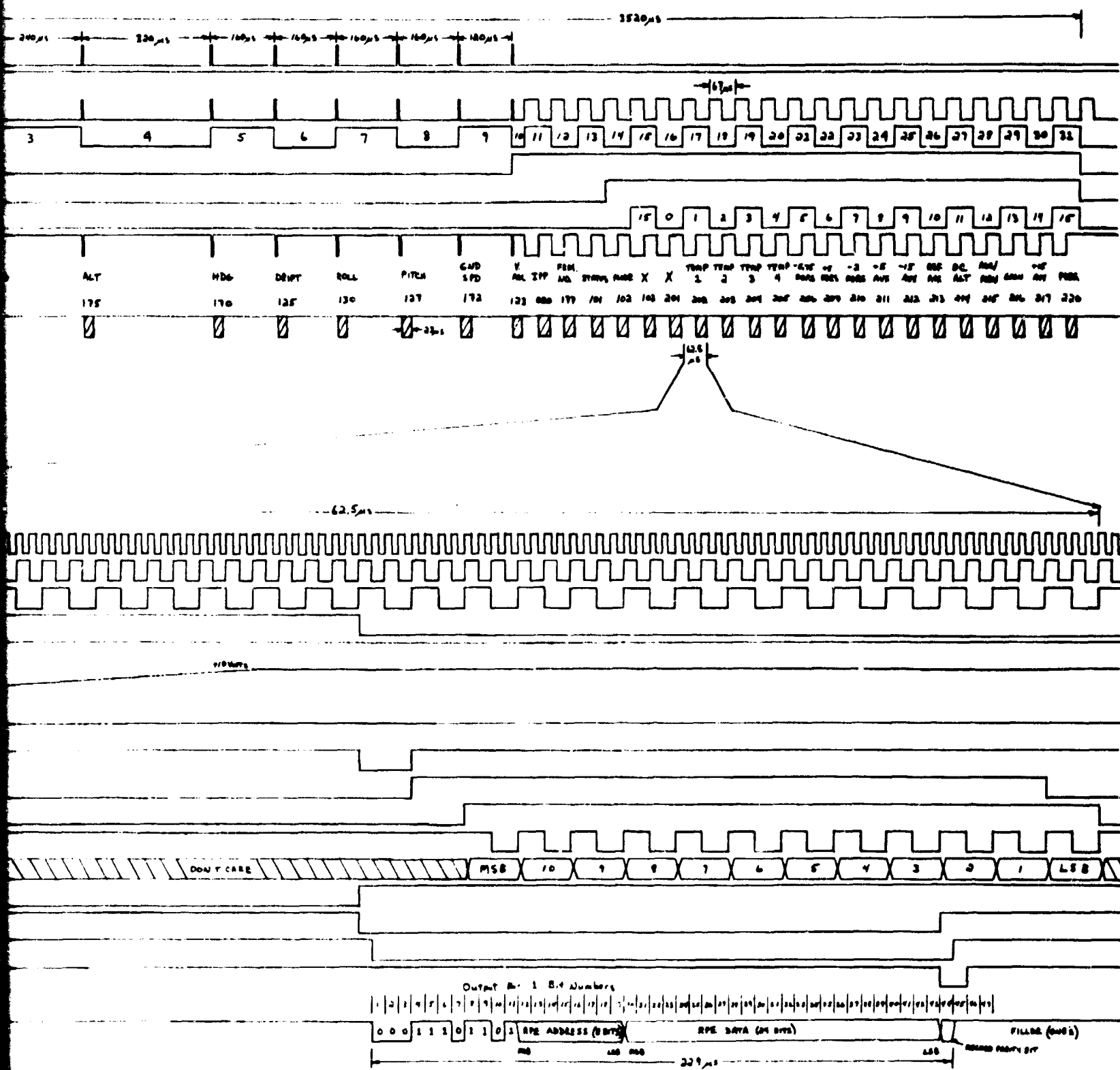


FIGURE 13  
RPE TIMING DIAGRAM

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TABLE IV  
RPE CONTROL PROM AND ADDRESS PROM BIT PATTERNS

PROGRAM COUNTER ADDRESS		CONTROL PROM OUTPUTS (UE10)					RPE ADDRESS PROM OUTPUTS (UF8)						
DECIMAL	HEX	BINARY			OCTAL	HEX	BINARY			OCTAL	HEX	DATA CORRESPONDING TO RPE ADDRESS	
		8765	432	1			87	654	321				
0	0	0000	000	0	000	00	01	111	001	171	79	TIME	NERDAS
1	1	0000	000	0	000	00	10	000	000	200	80	DATE	
2	2	0000	000	0	000	00	10	010	001	221	91	LATITUDE	
3	3	0000	000	0	000	00	01	011	010	132	5A	LONGITUDE	
4	4	0000	000	0	000	00	01	111	101	175	7D	ALTITUDE	
5	5	0000	000	0	000	00	01	111	000	170	78	HEADING	
6	6	0000	000	0	000	00	01	010	101	125	55	DRIFT	
7	7	0000	000	0	000	00	01	011	000	130	58	ROLL	
8	8	0000	000	0	000	00	01	010	111	127	57	PITCH	
9	9	0000	000	0	000	00	01	111	010	172	7A	GROUND SPEED	
10	A	0000	000	1	001	01	01	010	011	123	53	VERTICAL ACCELERATION	DDRS
11	B	0000	001	1	003	03	00	010	000	020	10	INTER-PULSE PERIOD	
12	C	0000	010	1	005	05	01	111	111	177	7F	FRAME NUMBER	
13	D	0000	011	1	007	07	01	000	001	101	41	STATUS	
14	E	0000	100	1	011	09	01	000	010	102	42	MODE	
15	F	1111	101	1	373	FB	01	000	011	103	43	UNDEFINED	
16	10	0000	111	1	017	0F	10	000	001	201	81	UNDEFINED	AUXILIARY DATA CONVERSION BOARD
17	11	0001	111	1	037	1F	10	000	010	202	82	TEMP 1 (DDRS BOARD 9)	
18	12	0010	111	1	057	2F	10	000	011	203	83	TEMP 2 (DDRS BOARD 2)	
19	13	0011	111	1	077	3F	10	000	100	204	84	TEMP 3 (NOT CONNECTED)	
20	14	0100	111	1	117	4F	10	000	101	205	85	TEMP 4 (AGC/STC)	
21	15	0101	111	1	137	5F	10	000	110	206	86	-5.75 V POWER (DDRS)	
22	16	0110	111	1	157	6F	10	000	111	207	87	+5 V POWER (DDRS)	
23	17	0111	111	1	177	7F	10	001	000	210	88	-2 V POWER (DDRS)	
24	18	1000	111	1	217	8F	10	001	001	211	89	+5 V POWER (AGC/STC)	
25	19	1001	111	1	237	9F	10	001	010	212	8A	-15 V POWER (AGC/STC)	
26	1A	1010	111	1	257	AF	10	001	011	213	8B	+10 V REFERENCE	
27	1B	1011	111	1	277	BF	10	001	100	214	8C	dc ALTITUDE	
28	1C	1100	111	1	317	CF	10	001	101	215	8D	AGC/MANUAL GAIN	
29	1D	1101	111	1	337	DF	10	001	110	216	8E	GAIN	
30	1E	1110	111	1	357	EF	10	001	111	217	8F	+15 V POWER (AGC/STC)	
31	1F	1111	111	1	377	FF	10	010	000	220	90	AMBIENT PRESSURE (DDRS)	

ANALOG MIX ADDRESS

RPE DATA BUS ENABLE SELECT

SELECTS UPP'S STROBE INTERNAL CLOCK

RECORDED ON TAPE AS RPE ADDRESS



<u>RPE Parameter</u>	<u>Address (Octal)</u>	<u>DRIE Display Label</u>
Time	171	LONGITUDE
Heading	170	LATITUDE
Ground Speed	172	HEADING
Frame Number	177	FRAME NUMBER
Altitude	175	RMIN

(b) The other parameters are assigned arbitrary addresses convenient for the ARL:UT software which reads and processes the RPE data.

The 24 bits following the eight address bits are latched from the RPE data bus. There are six sets of bus drivers, only one of which is enabled (by UG8, according to bits 2, 3, and 4 of the control PROM) at a time. The bus driver for UPPS data has been mentioned. The others are (1) the IPP counter driver (UF3, UF4), (2) the frame counter driver (UF5, UF6, UF7), (3) the mode driver (UD2, UD9, UD10), (4) the status driver (UD1, UH1), and (5) the auxiliary data driver (UE2, UF2).

The IPP counter (UG2, UG3, UG4, UH2, UH3, UH4) counts the number of cycles of the 2.07065 MHz radar clock that have occurred between STC triggers. This number is latched on the rising edge of each STC trigger pulse, about once every 750  $\mu$ sec. However, the IPP counter number, like all RPE data values, is only recorded on the wideband tape once every RPE output cycle, every 10 msec. Since the STC trigger is asynchronous with the RPE timing, occasionally the IPP number will change while being latched into the output shift register, resulting in faulty IPP reading. However, such an error should not occur more than once every 2.7 min, or about six times during an entire wideband tape.

A frame number is recorded on the RPE track which is used by the DRIE and the ARL:UT data reduction software to block off the

video data into manageable segments. The frame counter (UG5, UG6, UG7, UH5, UH6) on the PPE board increments with every eighth cycle of UPPS/NERDAS data. This amounts to once every 80 msec, or approximately once every 107 video data records (or once every 107 IPP's). The actual frame number is arbitrary. The playback operator will not use the frame number to identify the data; he will only use it to manage the data. Data identification and correlation with the optical recorder data may be accomplished using NERDAS time-of-day.

The mode data are the 15 bits of the operator control settings along with the control valid bit, which are recorded as one contiguous data word. The status data consist of a 5-bit count of video overranges (from the interface board), the video valid and RPE valid bits (from the video formatting board), the clock valid bit, and a 4-bit count of word-by-word parity errors, all composed into one 12-bit data word. The parity error counter is on the RPE board (UJ1, UJ2, UJ3, UH2). When the DDRS is in the 7-bit data precision mode, the circuit counts the number of parity errors (in the 7 bit plus even parity video data words) during each data record. The count accumulates for 10 msec up to a maximum of 15 errors, at which count it holds until output to the wideband tape. The clock validation circuit (UJ4, UJ5, UJ9, UJ1) tests for an out-of-lock condition on the clock generator board. The clock skew (CLKSKEW) signal from the clock generator board is an exclusive-NOR of the two inputs to the phase comparator. A false level on this line occurs during the time when the reference 2.07065 MHz signal and the synthesized phase locked 2.07065 MHz are out of phase. The rising edge of the clock to flip-flop UJ9, pin 12, occurs approximately 75 nsec after the rising edge 2.07065 MHz synthesized clock. If at this point, in each 2.07065 MHz clock cycle, CLKSKEW is false, then the CLKVAL line goes false and CLKINVAL to the cockpit goes true. One shot UJ4, pin 5, stretches momentary losses of lock into 1 sec pulses on CLKINVAL.

The auxiliary data comes from the auxiliary data conversion board as a serial data stream. The interface board generates a signal (AUXCP) to clock the serial data into the auxiliary data shift

register (UEi, UH7). The parallel outputs of this shift register constitute the 12-bit auxiliary data word. Fifteen different analog parameters are digitized, shifted into the auxiliary data shift register, and output through the output shift register during each 10 msec RPE cycle. The RPE timing diagram (Fig. 13) shows the order in which the auxiliary data are output. The order shown is determined by bits 5, 6, 7, and 8 of the control PROM (UE10). Data formats for all types of RPE data are shown in Table III.

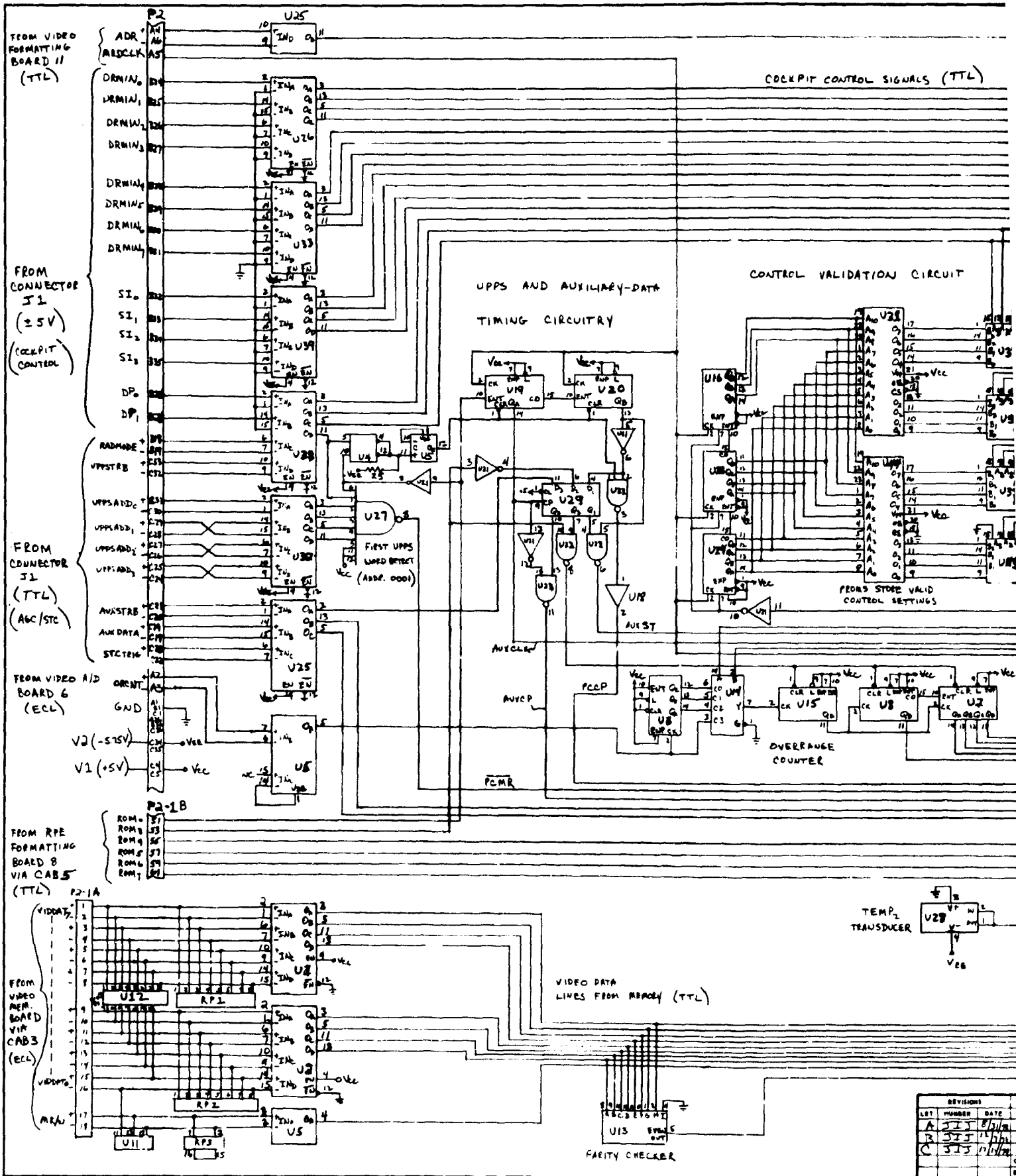
Included on the RPE formatting board is the overrange alert one-shot (UJ4), which outputs a 1 sec ORALT pulse to the cockpit when the MSB of the overrange counter (OR<sub>4</sub>) goes true. This condition will occur when about 30% of the video samples are in saturation.

#### (6) Interface Board (Dwg. No. 9)

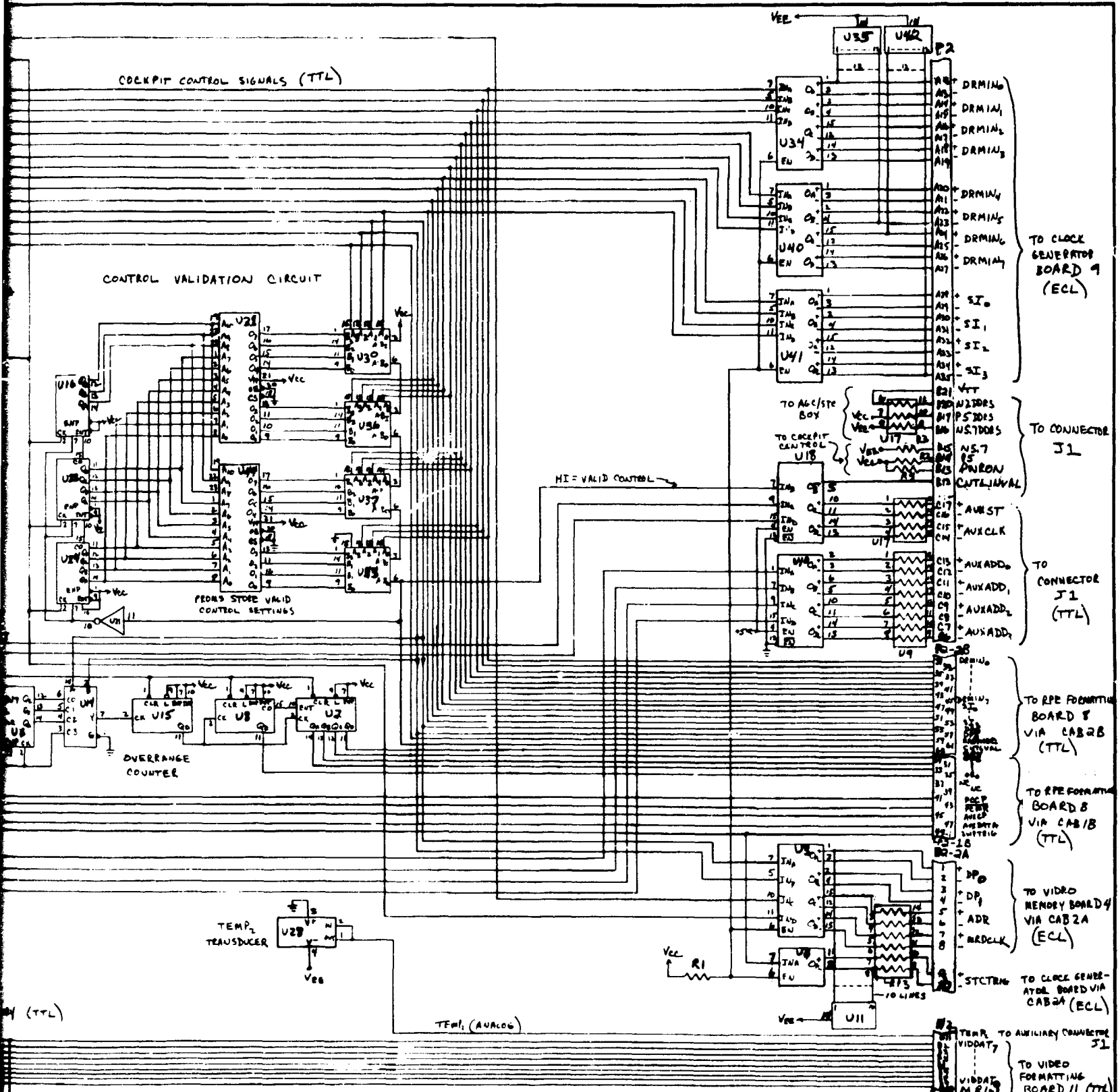
Most of the circuitry on the interface board is involved with logic level conversion, line receiving, and line driving. Most ECL-TTL and TTL-ECL signal conversions in the DDRS take place on the interface board. The  $\pm 5$  V logic signals from the cockpit control panel are converted to TTL and ECL levels here. Since Dwg. No. 9 clearly shows the signal conversion circuitry, no further discussion of it is necessary here.

However, there are a few control circuits included on the interface board. These are (1) UPPS and auxiliary data timing, (2) control validation, (3) overrange counting, and (4) parity checking.

The UPPS and auxiliary data timing circuit (U19, U20, U21, U22, U27, U29) synthesizes the PCMR and PCCP signals required by the RPE formatting board, as well as control and timing signals for the auxiliary data conversion board. U27 outputs the PCMR pulse when the first strobe (time-of-day) of a data cycle from the UPPS occurs. The UPPS address line receiver (U32) is currently wired to recognize an address of 0001 for the time-of-day strobe, but for future requirements, these may



REVISIONS		
LET	NUMBER	DATE
A	313	8/11/64
B	313	1/1/64
C	313	1/1/64



REV	NUMBER	DATE	APPROVED	DATE	DESIGN SPECIFICATIONS	DO NOT SCALE DRAWING	JOB NO.
A	313	8/14/68		8/14/68	GROUPS 1 AND 2 MUST BE MADE TO ORDER AND IN QUANTITIES OF 100 UNITS.	FINISH	
B	313	11/14/68			FRACTIONAL 2	HEAT TREATMENT	
C	313	1/14/69			ANGULAR 2	NOT REQD	
			CHECKED				
			DRAWN				

INTERFACE BOARD #2  
 MATERIAL NA39-15717-4

APPLIED RESEARCH LABORATORIES  
 THE UNIVERSITY OF TEXAS AT AUSTIN  
 SCALE D Drawing No. 9

69  
 2

be changed to recognize any time-of-day address by reversing the inverting and noninverting inputs as required.

The PCCP signal has for its source either the UPPS strobe or a 15 kHz square wave from U20, pin 13. Signal ROM<sub>0</sub> from the RPE formatting board (the LSB of the control PROM on that board) determines the source: a false level selects the strobe by disabling counters U19 and U20, while a true level selects the square wave by enabling the counters and gating off the strobe at U4, pin 10. (An ECL inverter with a wire OR connection followed by a ECL-TTL translator is used here because of lack of space for another TTL NAND gate on the board.)

The AUXST signal commands the A/D converter in the auxiliary data conversion board to start a conversion. It is a 2  $\mu$ sec negative going pulse generated on the rising edge of the 15 kHz square wave from U20, pin 13. The AUXCLK is the 0.96 MHz clock signal to the A/D converter chip on the auxiliary data board. The timing of these signals is shown in Fig. 13.

The control validation circuit (U16, U23, U24, U30, U31, U36, U37, U43, U44) compares the four cockpit settings (delta RMIN, sample interval, data precision, and radar mode) with preprogrammed valid control setting in the PROM's U31 and U34. Appendix C, Sec. 1, outlines the valid control settings as currently programmed, and Appendix C, Sec. 2, is a printout of the actual numbers (in base 16) stored in the PROM chips. Address counters U16, U23, and U24 count through the 2048 address location in the PROM's until one of the address locations is reached which contains data that match the control switch setting. At this time, the "equals" output of the 16-bit magnitude comparator (U30, U36, U37, U43) at pin 6, U43, goes true. This stops the address counters and turns off the CONTROL INVALID light in the cockpit.

The overrange counter circuit (U6, U7, U8, U14, U15) counts the number of video samples during a 10 msec period for which either the horizontal or the vertical video input circuitry was in saturation.

It was found during the FLAMR program that an optimum video level resulted in about 10% of the video samples being in saturation. The overrange counter circuit counts up to a maximum 60% saturation (at an IPP of 740  $\mu$ sec); the MSB goes high at 30% saturation and causes the overrange alert (ORALT) light to turn on in the cockpit. The lower the data precision is, the more video samples are produced in a 10 msec interval, and multiplexer U14 and counter U6 compensate to allow the overrange count to accumulate to a greater number for the lower data precisions.

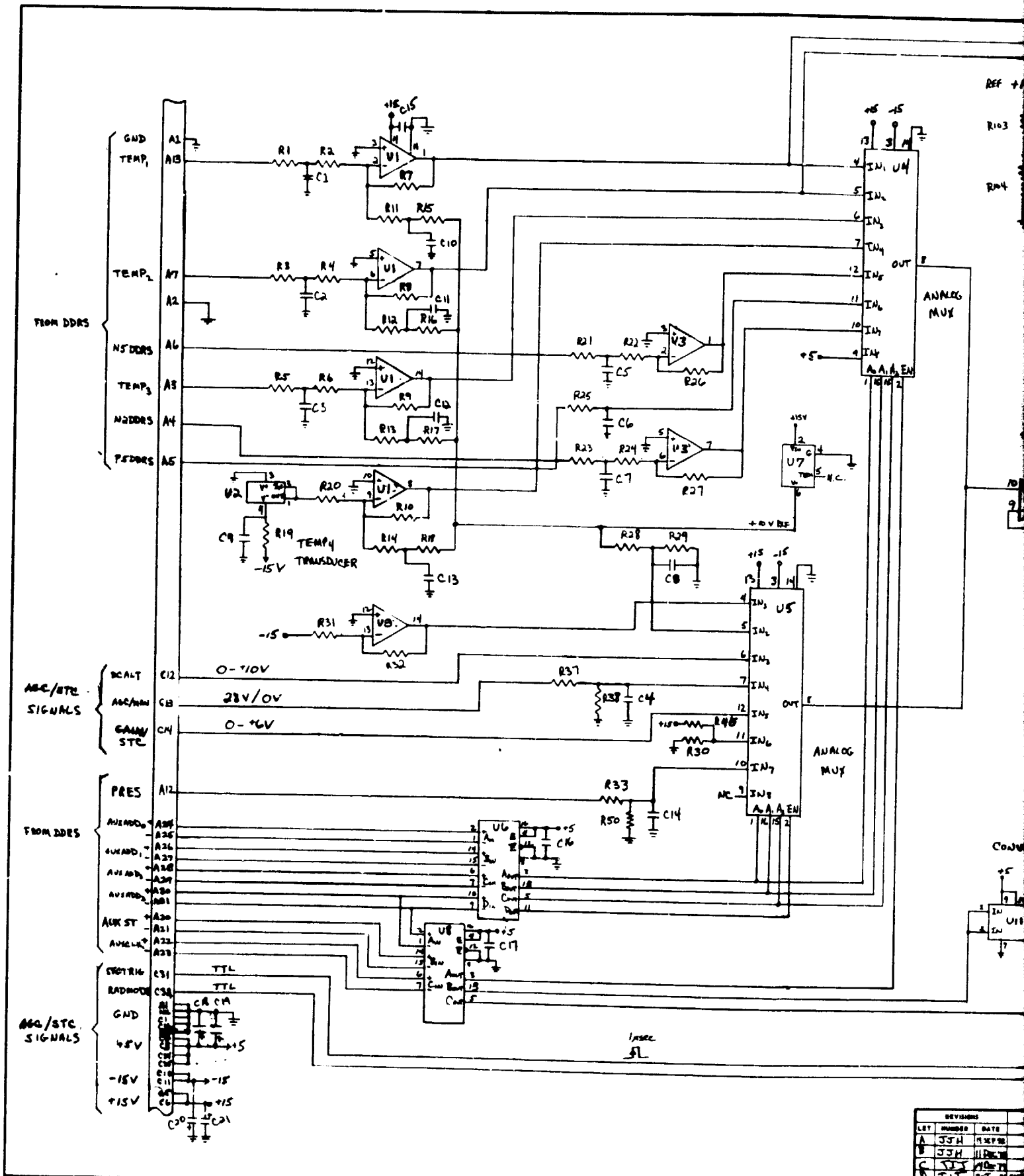
Finally, as the video data are read from the memory, U13 outputs a true level at pin 5 whenever the eight bits of the data words do not have even parity. This signal (MEMPAR) is sent to the RPE formatting board which, when the system is in the 7-bit mode, counts the number of memory words which do not have even parity when read, as indicated by MEMPAR.

#### (7) Auxiliary Data Conversion Board (Dwg. No. 10)

The main purpose of the auxiliary data conversion board is to digitize dc voltages corresponding to radar and environmental parameters. It also interfaces the STC trigger and the radar mode signals from the AGC/STC processor with the DDRS.

Temperature transducer outputs from the DDRS and the TEMP 4 transducer output on board the auxiliary data board are amplified by quad operational amplifier U1. Since the auxiliary A/D converter (U9) operates on an analog voltage range of 0 to +10 V, the negative polarity of the temperature transducer outputs and the negative supply voltages are inverted by U1 and U3.

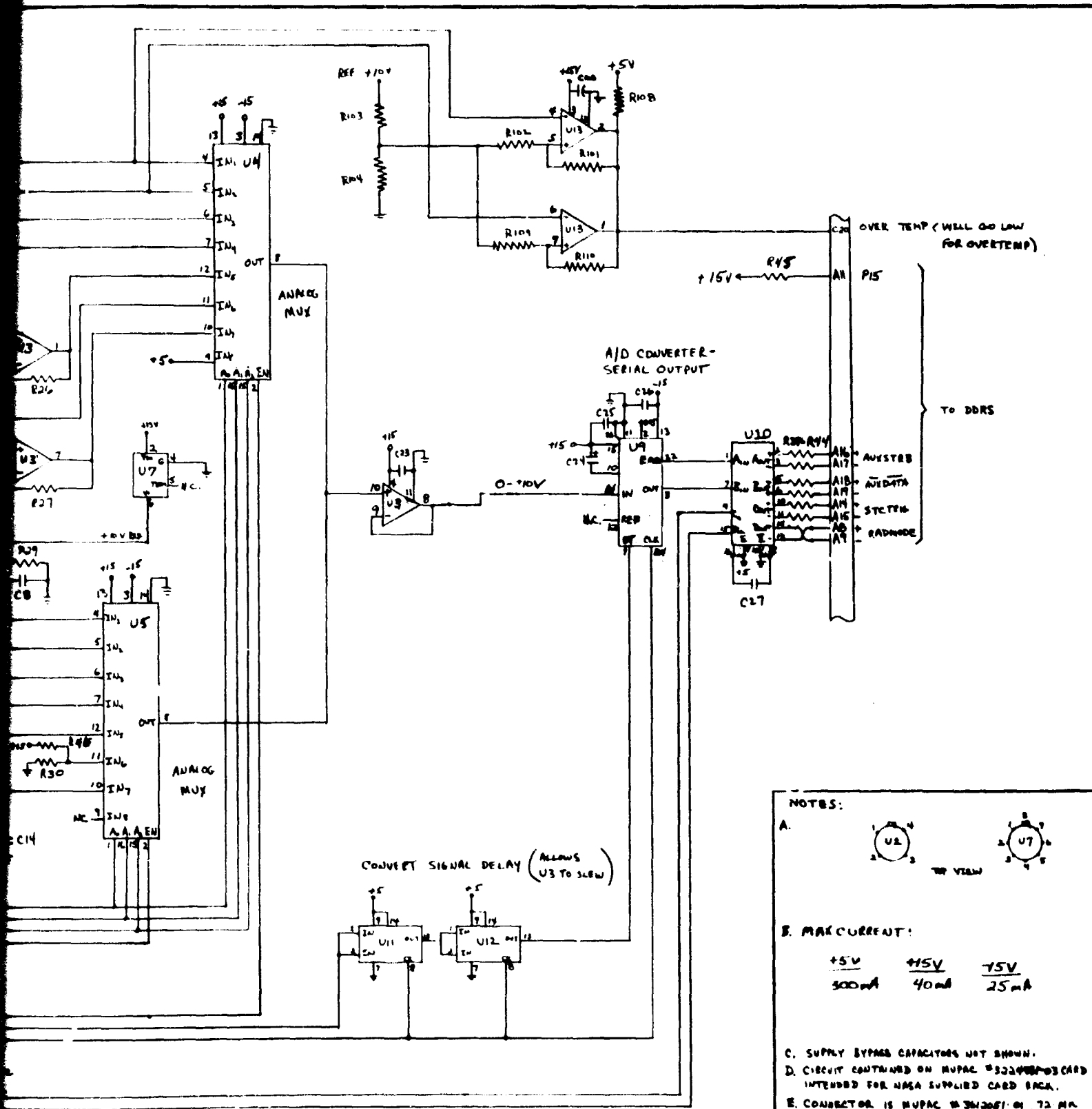
Sixteen analog voltages (one of which is not currently connected) are multiplexed through the analog multiplexers U4 and U5. Each of the 16 voltages are sequentially selected by the control PROM on the RPE formatting board through the auxiliary address lines (AUXADD<sub>0</sub>-




**EXPLODED FRAME**

REVISIONS		
REV	NUMBER	DATE
A	33H	11/27/78
B	33H	11/27/78
C	33H	11/27/78
D	33H	11/27/78





NOTES:

A. 

B. MAX CURRENT:

+5V	+15V	-15V
300mA	40mA	25mA

C. SUPPLY BYPASS CAPACITORS NOT SHOWN.  
 D. CIRCUIT CONTAINED ON MUPAC #3224803 CARD INTENDED FOR NMSA SUPPLIED CARD BACK.  
 E. CONNECTOR IS MUPAC #322081-01, 72 PIN RIGHT ANGLE PLUG.

REVISION	APPROVED	DATE	DESIGN ENGINEER	DO NOT SCALE DRAWING	AUXILIARY DATA CONVERSION BOARD	JOB NO.
A	SSM	8/1/77		FORM		
B	SSM			HEAT TREATMENT		
C	SSM					
D	SSM				MATERIAL NAS9-15217-4	SCALE D Drawing No 10

AUXADD<sub>3</sub>). The output of the multiplexers is buffered by part of U3 and connected to the analog input of the A/D.

The interface board of the DDRS synthesizes the start convert (AUXST) and the conversion clock (AUXCLK) signals to the auxiliary A/D, as required by the A/D data sheet (Micro Networks MN5216). The start conversion signal is delayed 33  $\mu$ sec by shift registers U11 and U12 to allow the multiplexer output buffer to slew between successive data voltages. Control timing for the auxiliary A/D is shown in the RPE timing diagram, Fig. 13.

Overtemperature comparator U13 senses the outputs of the DDRS temperature transducers (TEMP 1 and TEMP 2). The comparator output will go to a TTL low level when either of the transducers indicate 60°C or greater. This output (OVERTEMP) should be used to disconnect power to the DDRS. The relay to remove DDRS power should be latching; i.e., once triggered to remove power, it should have to be manually reset. This is necessary because as soon as the DDRS is turned off, the OVERTEMP signal will immediately go high again. If, at this time, the relay is not latched off, power will be reconnected to the DDRS and OVERTEMP will again go low, disconnecting power again, ad infinitum.

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## IV. OPERATION AND MAINTENANCE

### A. Preflight Checkout Procedure

#### 1. Test Equipment Required

oscilloscope, event counter

#### 2. Video System Checkout

##### a. Connections required to test connector J103:

- (1) VIDEO NRZ track 7 to the oscilloscope vertical input
- (2) TRIGVID to the oscilloscope
- (3) PARCHK to the event counter
- (4) REF to the video inputs J108 and J109

b. Connect all other DDRS I/O connectors to their respective pallet cables.

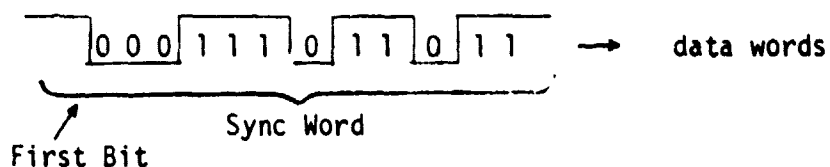
c. Double check connections and apply power.

d. From the control panel, switch the DDRS into the 4-bit data precision mode and adjust the event counter sensitivity to show a rapid count on the event counter.

e. From the control panel, switch the DDRS into the 7-bit mode. The count rate should decrease to zero. If the count rate is still high, decrease the counter sensitivity just until the counting stops and switch

back to the 4-bit mode. The count rate should always be very high in the 4-bit mode. Now switch back to the 7-bit mode for further tests and reset the event counter to zero.

f. Set the horizontal sweep rate on the oscilloscope to  $1 \mu\text{sec}/\text{div}$ , and adjust the trigger sensitivity to display a stable digital waveform on the CRT. This waveform is the first part of the video data record. The bit duration is  $0.51 \mu\text{sec}$ , or about 2 bits per horizontal division. The first bit begins where the waveform first falls from a high level to a low level. The first twelve bits in the record compose the sync word and should always be 000111011011:



The rest of the record is composed of 128, 8-bit, serial 2's complement data words, MSB (sign) first and parity bit last. The same word should be repeated all 128 times. The value of this word depends on the reference voltage level connected to the video inputs from the test connector, and is adjustable internally on board 6 of the DDRS. Note that the seventh bit of this word may toggle (on noise along with the eighth parity bit). Check all eight tracks of video NRZ data for the same characteristic waveform. This test may be more easily done in the 4-bit mode, if the toggling of the LSB and parity bits becomes too distracting.

g. Disconnect video inputs J108 and J109 and repeat step 6. The value of the data word should be within 1 or 2 LSB's of all zeroes.

h. Check the event counter for zero parity errors for as long as the system was in the 7-bit mode.

i. Check the eight Miller-encoded video data lines to the

wideband tape recorder with an oscilloscope for a phase encoded square wave on each.

### 3. RPE System Checkout

#### a. Connections required to test connector J103:

- (1) RPE NRZ to the oscilloscope vertical input
- (2) TRIGRPE to the oscilloscope trigger input
- (3) RPE TEST to ground
- (4) AUX/UPPS to ground

b. Input a constant 24-bit word (DOD-23) from the UPPS MUX output to the DDRS with a periodic strobe pulse from the UPPS STRB output. (Repetition rate of the STRB pulse not to exceed 25 kHz.)

c. Set the horizontal sweep rate of the oscilloscope to 1.0  $\mu$ sec/div and adjust the trigger sensitivity to obtain a stable waveform on the CRT. Observe the waveform. The first eleven bits are the sync words, 00011101101, and the next eight bits are the "test" address bits, 01111010:

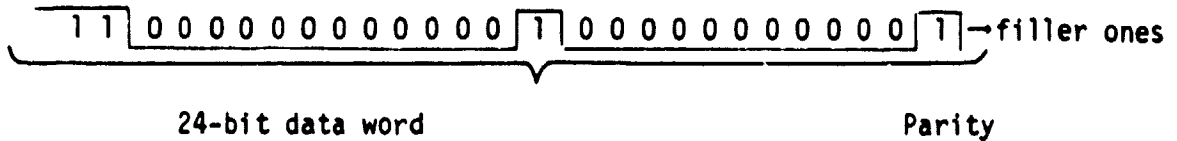


The following 24-bit data word (MSB first) should be identical to the 24-bit word input from the UPPS. After the 24th bit of the data word will be the record parity bit followed by filler ones.

d. Now disconnect the AUX/UPPS input on J103 from ground. Observe the scope waveform. The sync word should now be followed by a different 8-bit address, 10001010:



The 24-bit data word should be nominally  
000000000000 1 0000000:



The data word may vary several bits from its nominal value.

e. Check the Miller-encoded RPE data line to the wideband tape recorder for a phase encoded square wave.

4. Disconnect J103 and reconnect the video lines from the optical recorder. The DDRS is now ready for flight.

## B. System Operation

After a successful preflight checkout, the system is ready for in-flight operation. With the unit cabled up and installed in the pallet, the operator has only to set the required sample interval, data precision, and delta RMIN from the control panel. Once the pallet is powered up, and the DDRS receives UPPS data and clock and STC signals, all the control panel lights except "POWER ON" should go out. After this time, merely connect voice and time code to the wideband recorder and start the recorder when desired.

## C. Adjustments

There are few internal adjustments in the DDRS. Those most often requiring attention are the trimmer potentiometers on the A/D board. Other

adjustments rarely requiring attention are timing adjustments by jumper wires on the clock generator board, the video A/D board, and the video memory board.

The gain and bias potentiometer adjustments on the video A/D board are explained in Sec. III.D. The gain adjustment should be set so that the overrange alert (ORALT) light rarely, if ever, lights up. Otherwise, adjust the gain for optimum image quality, which past experience has shown to be about 10% overrange. The bias adjustment should be used to compensate for an unwanted dc offset in the video signals. There is also an output reference potentiometer which may be adjusted to set a desirable test voltage for preflight checkout of the video A/D subsystem (Sec. IV.A). The best reference voltage is that which, after being digitized, produces an easily recognized digital waveform on the video data recorder tracks.

The other internal adjustments are timing adjustments and involve changing jumper wires. These jumpers select one of several taps on tapped lumped-constant delay lines. There are four of these jumpers: one on the clock generator board 9 (Dwg. No. 4) to delay the reset memory address for write ( $\overline{ADW}$ ); one on the video A/D board 6 (Dwg. No. 5) to delay the sample pulse to the vertical channel A/D with respect to the sample pulse to the horizontal channel A/D; and finally, one on the video memory board 4 (Dwg. No. 6) to set the width of the write-enable pulse ( $\overline{WE}$ ) to the memory chips. The current positions of these jumpers are shown in the drawings. They should not have to be repositioned except when a TRW A/D chip is replaced, or perhaps as the TRW chips age and their propagation delay characteristics change.

The object in setting the jumpers is to meet the memory chip (Fairchild 10415A) requirements for write pulse width (14 nsec) and for stable A/D data at the memory chip inputs throughout the time the  $\overline{WE}$  signal is low. To check timing, use a high speed oscilloscope (Tek 7834 or 485 recommended) preferably with a fast FET input active probe (Tek P6201 or P6202). Observe the data input (pin 15) and the  $\overline{WE}$  input (pin 13) on a 10415A memory chip. With the system in the 7-bit mode and while digitizing

a video signal (a sine wave is good), A/D transitions at the  $D_{in}$  pin should be visible. Ensure that these transitions occur only when  $\overline{WE}$  is high. It is important to check every 10415A this way since propagation delays to each chip are slightly different. Check the timing at 40 nsec sampling intervals and also at 60 nsec sampling intervals. (Refer to Fig. 10.)

If data transitions occur during a  $\overline{WE}$  pulse, the timing of the  $\overline{WE}$  pulse must be changed. It can be advanced by decreasing the delay of the MWRTCLK on the video A/D board (currently set to 30 nsec) and it may be retarded by increasing the same delay. Line 12 of Fig. 10 illustrates this delay. If the data timing from one A/D channel is good, but the timing of the other A/D channel is off, the vertical A/D may be delayed with respect to the horizontal A/D by using the other jumper on the A/D board. This requires the faster A/D to be in socket U25 with the slower in U26, and the TRW chips may need to be reversed.

It is not recommended that the  $\overline{WE}$  pulse width be changed (by changing the jumper on the video memory board). This width is currently set to 14 nsec (as shown in line 13 of Fig. 10).

The other timing adjustment involves the delay of the  $\overline{ADW}$  signal on the clock generator board. This will not require adjustment unless the MWRTCLK delay is decreased. Refer to Fig. 10, line 9. The  $\overline{ADW}$  signal (available on the memory board at U31, pin 5) must rise after the first pulse of MWRTCLK (on memory board at U32, pin 15) in an IPP, but before the second one. The delay is currently set at 50 nsec.

#### D. Maintenance

##### Symptoms and Causes - Corrective Action

1. RPE-INVALID lights up  
Probable cause - no UPPS strobe or address



2. VIDEO-INVALID lights up  
Probable causes - no STC trigger  
- no 2.07065 MHz clock
3. CLOCK-INVALID lights up  
Probable causes - no 2.07065 MHz clock  
- noisy clock signal
4. CONTROL-INVALID lights up  
Probable cause - invalid control setting (will not disable DDRS)
5. OVERRANGE-ALERT lights up  
Probable cause - video A/D gain not properly adjusted
6. High parity error count (in 7-bit mode only)  
Probable causes - MWRTCLK timing needs adjustment (Sec. IV.C)  
- bad memory chip

The above symptoms will probably be most common and are fairly simple to correct. If more serious problems develop, a complete understanding of the DDRS circuitry and timing will be required, and the drawings and timing diagrams of this document will have to be studied thoroughly. It is recommended that before any major surgery is performed, all connector pins and sockets be checked (both on front panel I/O connectors and on internal card cage connectors) and all power supply outputs be checked. The DDRS circuitry is made up of reliable components; however, those most likely to be the first to fail will be the more complex components: the TRW A/D chips, the memory chips, and the power supplies.

It must be stressed that the key to reliability in the DDRS is in maintaining as low an operating temperature as possible. The cooling fan inside the unit will help in this regard, but even with the fan, the interior DDRS temperature runs 10°C hotter than outside ambient temperature at sea level. It is important that the power to the unit be disconnected when the OVERTEMP line on the auxiliary data board goes low, and it is

also recommended that close attention be given to the recorded values for TEMP 1, TEMP 2, and TEMP 4 on the first data tapes.

APPENDIX A

CRITICAL SPARES AND PARTS LIST  
WITH COMPONENT PLACEMENT DRAWINGS

CRITICAL SPARES LIST

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		14. Contract No.	2. Code Group	3. PL	4. Revision: Ltr. Date	
5. Line Title: SPARE PARTS FOR DDRS		6. Authentication:		7. Rev Auth No.		8. Sheet 1 OF 3 Sheets		
9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description			
1	1	pkg.		1301472-01	Mupac wire-wrap socket terminal			\$13.20
2	1	pkg.		1301402-01	Mupac wire-wrap slotted terminal			\$ 12.10
3	1	pkg.		1311517-01	Mupac mini terminal receptacle			\$ 15.40
4	1	unit		SHU-2V/AA	Arnold Magnetics 2 V power supply			\$353.00
5	1	unit		ASN-MS-5/9V -C5/5V-CA	Arnold Magnetics ±5 V power supply			\$791.00
6	1	unit		387JH	Rotron Propimax 38 fan			\$ 99.20
7	1	"		TDC 1007J	TRW Video A/D Converter Chip			\$745.00
8	3	"		54LS365	Integrated Circuit			\$ 0.92
9	3	"		54LS165	Integrated Circuit			\$ 2.09
10	2	"		54S28R	Integrated Circuit			\$ 4.37
11	1	"		54LS138	Integrated Circuit			\$ 1.44
12	2	"		54LS04	Integrated Circuit			\$ 0.61
13	2	"		54LS00	Integrated Circuit			\$ 0.61
14	2	"		54LS109A	Integrated Circuit			\$ 0.72
15	1	"		54LS123	Integrated Circuit			\$ 1.79
16	1	"		54121	Integrated Circuit			\$ 1.38
17	3	"		54LS112	Integrated Circuit			\$ 0.73
18	2	"		54LS02	Integrated Circuit			\$ 0.58
19	1	"		54LS30	Integrated Circuit			\$ 0.58
20	1	"		54LS37	Integrated Circuit			\$ 0.68
21	1	"		54LS85	Integrated Circuit			\$ 2.03
22	1	"		54LS280	Integrated Circuit			\$ 2.39
23	2	"		2N5583	Transistor			\$ 3.85
24	2	"		2N4403	Transistor			\$ 0.46

PARTS LIST		1. Agency (Contractor Identifications): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		2A. Contract No.	3. Code Vand.	3. PL	4. Revision Let. Date
3. List Title: SPARE PARTS FOR DDRS		6. Authentication:		7. Rev Auth No.		8. Sheet 2 of 3 Sheets	
9. Item or Find Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description		
25	2	unit		MC12049L	Motorola Integrated Circuit	•	7.09
26	2	"		MC1648L	Motorola Integrated Circuit	•	3.90
27	2	"		LH0932G	National Integrated Circuit	•	50.90
28	1	"		LX5600AH	National Integrated Circuit	•	6.50
29	1	"		LX1602A	National Integrated Circuit	•	85.00
30	1	"		LM139D	National Integrated Circuit	•	12.00
31	1	"		UA124DM	Fairchild Integrated Circuit	•	6.75
32	3	"		10115	Fairchild Integrated Circuit	•	0.80
33	2	"		10125	Fairchild Integrated Circuit	•	1.50
34	2	"		10105	Fairchild Integrated Circuit	•	0.50
35	3	"		10124	Fairchild Integrated Circuit	•	1.50
36	2	"		10160	Fairchild Integrated Circuit	•	3.20
37	4	"		10174	Fairchild Integrated Circuit	•	2.70
38	2	"		10103	Fairchild Integrated Circuit	•	0.47
39	3	"		10016	Fairchild Integrated Circuit	•	4.25
40	2	"		10010	Fairchild Integrated Circuit	•	4.25
41	2	"		10131	Fairchild Integrated Circuit	•	1.00
42	2	"		10135	Fairchild Integrated Circuit	•	1.60
43	2	"		10102	Fairchild Integrated Circuit	•	0.47
44	2	"		10107	Fairchild Integrated Circuit	•	0.50
45	2	"		10101	Fairchild Integrated Circuit	•	0.47
46	5	"		10415A	Fairchild Integrated Circuit	•	18.20
47	2	"		10173	Fairchild Integrated Circuit	•	2.70
48	2	"		10171	Fairchild Integrated Circuit	•	2.40

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS		1A. Contract No.	2. Code Veny.	3. PL	4. Revision Ltr. Date	
5. List Title: SPARE PARTS FOR DBRS		6. Authentication:		7. Rev Arch No.				
9. Item or Find Number	10. Qty Req	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description			8. Sheets of 3 Drawings
49	2	unit		10161	Fairchild Integrated Circuit		\$ 2.40	
50	2	"		10136	Fairchild Integrated Circuit		\$ 6.50	
51	2	"		AM 687	Advanced Micro Devices IC		\$ 42.00	
52	2	"		25LS 153	Advanced Micro Devices IC		\$ 1.60	
53	4	"		25LS 161	Advanced Micro Devices IC		\$ 2.01	
54	2	"		25 LS 174	Advanced Micro Devices IC		\$ 1.80	
55	3	"		25LS 164	Advanced Micro Devices IC		\$ 2.90	
56	5	"		25LS 32	Advanced Micro Devices IC		\$ 11.85	
57	6	"		25S 31	Advanced Micro Devices IC		\$ 13.65	
58	2	"		25LS 157	Advanced Micro Devices IC		\$ 1.60	
59	1	"		PE 9824	Pulse Engineering, Inc., Delay Line		\$ 21.25	
60	1	"		PE 21171	Pulse Engineering, Inc., Delay Line		\$ 21.40	
61	2	"		AD580SH	Analog Devices, Inc., Voltage Ref.		\$ 11.75	
62	2	"		HI-0508A-2	Harris Analog Multiplexer		\$ 39.00	
63	1	"		REF-01J	Precision Monolithics Voltage Ref.		\$ 15.75	
64	1	"		MNS216H	Micro Networks Corp. 12-bit ADL		\$ 330.00	
65	1	"		L 73E	Conner-Minfield Corp. 3.84 MHz Oscillator		\$ 63.00	
66	2	"		4116R-002-202	Bourns Resistor Network		\$ 1.25	
67	2	"		4308R-101-121	Bourns Resistor Network		\$ 0.50	
68	2	"		899-1-R560	Beckman Resistor Network		\$ 1.43	
69	2	"		316B560	Allen-Bradley Resistor Network		\$ 1.43	
70	2	"		316A561	Allen-Bradley Resistor Network		\$ 1.43	
Total Cost for Spare Parts							\$3301.78	

PARTS LIST WITH COMPONENT PLACEMENT DRAWINGS



PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS			1A. Contract No. NAS-15217	1. Code PL	4. Revision Lit. No. Date
5. List Title: AUXILIARY DATA CONVERSION BOARD		6. Authentication:			7. Rev Auth No.		
9. Item or Line Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description		
U1, U3	2	ea		UAI24DM	Quad Operational Amplifier, Fairchild		
U2	1	ea		LS5600A	Temperature Transducer, National Semiconductor		
U4, U5	2	ea		HI1-0508A-2	8-Channel Analog Multiplexer, Harris		
U6, U8	2	ea		AM26LS32DC	Quad Line Receiver, Advanced Micro Devices		
U7	1	ea		REF-01J	+10 V Precision Voltage Reference, Precision Monolithics		
U9	1	ea		MP5216M	12-Bit A/D Converter, Micro Networks Corp.		
U10	1	ea		AM26LS31DC	Quad Line Driver, Advanced Micro Devices		
U11, U12	2	ea		AM25LS164DC	8-Bit Serial-In, Parallel-Out Shift Register, Advanced Micro Devices		
U13	1	ea		LM339N	Quad Comparator, National		
C18, C19	4	ea		CSR13G226DM	Capacitor, 22 $\mu$ F, Tantalum		
C20, C21	1	ea		CSR13G225DM	Capacitor, 2.2 $\mu$ F, Tantalum		
C24	10	ea		1802- Z5U050A104M	Capacitor, 0.1 $\mu$ F, Green Goddess, Varadyne		
R1, R2, R3, R4, R5, R6, R21, R22, R23, R24	11	ea		RM60D4991	Resistors, 4.95 k $\Omega$ , 1%, 1/4 W		
R7, R8, R9, R10	4	ea		RM60D8062	Resistors, 80.6 k $\Omega$ , 1% 1/4 W		
R15, R16 R17, R18	4	ea		RM60D4222	Resistors, 42.2 k $\Omega$ , 1%, 1/4 W		

PARTS LIST		1. Agency (Contractor Identification):			1A. Contract No.		3.		4. Revision	
5. List Title		APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS			WAS9-15217		PL		Ltr. No.	
9. Item or Find Number		11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description					
AUXILIARY DATA CONVERSION BOARD										
R11, R12	4	ea		RM60D6340	Resistor, 634 Ω, 1%, 1/4 W					
R13, R14										
R20, R21	4	ea		RM60D1022	Resistor, 10.2 kΩ, 1%, 1/4 W					
R27, R28										
R29, R30, R46	4	ea		RM60D1001	Resistor, 1.00 kΩ, 1%, 1/4 W					
R37	1	ea		RM60D2001	Resistor, 2.0 kΩ, 1%, 1/4 W					
R33	1	ea		RM60D1051	Resistor, 1.05 kΩ, 1%, 1/4 W					
R50	1	ea		RM60D4021	Resistor, 4.02 kΩ, 1%, 1/4 W					
R38	1	ea		RM60D9790	Resistor, 979 Ω, 1%, 1/4 W					
R103	1	ea		RM60D2371	Resistor, 2.37 kΩ, 1%, 1/4 W					
R104	1	ea		RM60D1542	Resistor, 15.4 kΩ, 1%, 1/4 W					
R102	2	ea		RM60D4751	Resistor, 4.75 kΩ, 1%, 1/4 W					
R109	2	ea		RM60D4752	Resistor, 47.5 kΩ, 1%, 1/4 W					
R101										
R110	2	ea		RCR07-102	Resistor, 1 kΩ, 5%, 1/4 W					
R25	1	ea		RCR07-560	Resistor, 56 Ω, 5%, 1/4 W					
R39 - R44	6	ea		RCR07-270	Resistor, 27 Ω, 5%, 1/4 W					
R45	1	ea		RCR07-822	Resistor, 8.2 kΩ, 5%, 1/4 W					
R19	1	ea		RCR07-302	Resistor, 3.0 kΩ, 5%, 1/4 W					
Q108	1	ea								
Aux Board	1	ea		3223081-01	322-type universal panel w/o sockets, MUPAC Corp.					
Aux Connector	1	ea		3612061-01	108-contact right-angle connector, MUPAC Corp.					

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		1A. Contract No. NAS-15217	2. Code PL	3. PL	4. Revision Rev. None
5. List Title: AUXILIARY DATA CONVERSION BOARD		6. Identification:		7. Rev Auth No.		8. Sheet of 3 sheets	
9. Item or Prod Number	10. Qty Reqd	11. Unit Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description		
N/A	17 1/2	ea		1301402-01	Wire-wrap slotted terminals, MUPAC Corp.		
N/A	17 1/2	ea		1301422-01	Wire-wrap socket terminals, MUPAC Corp.		
--	--	--		-----	30 ga. wire-wrap as needed.		

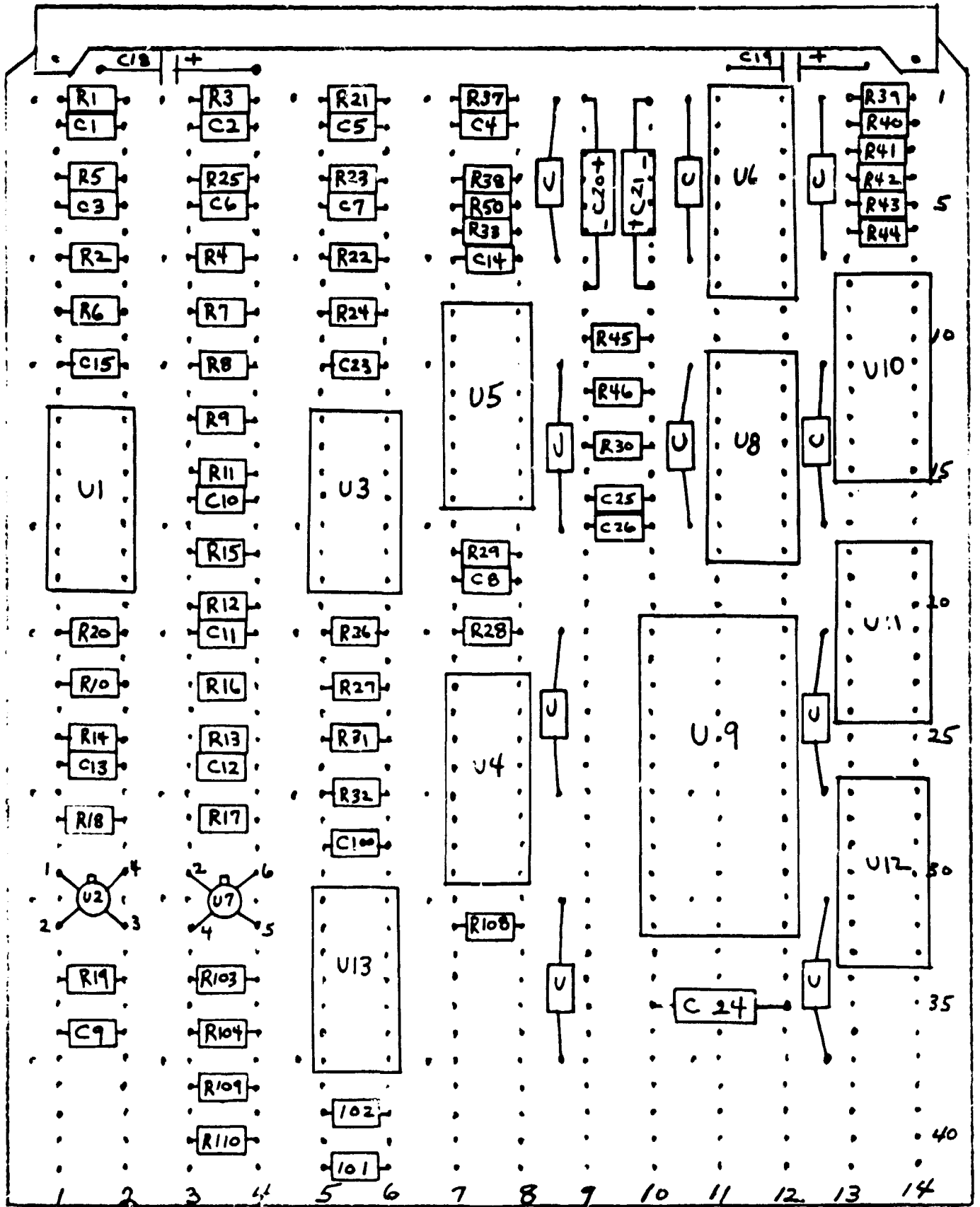


FIGURE A-1  
 AUXILIARY DATA CONVERSION BOARD

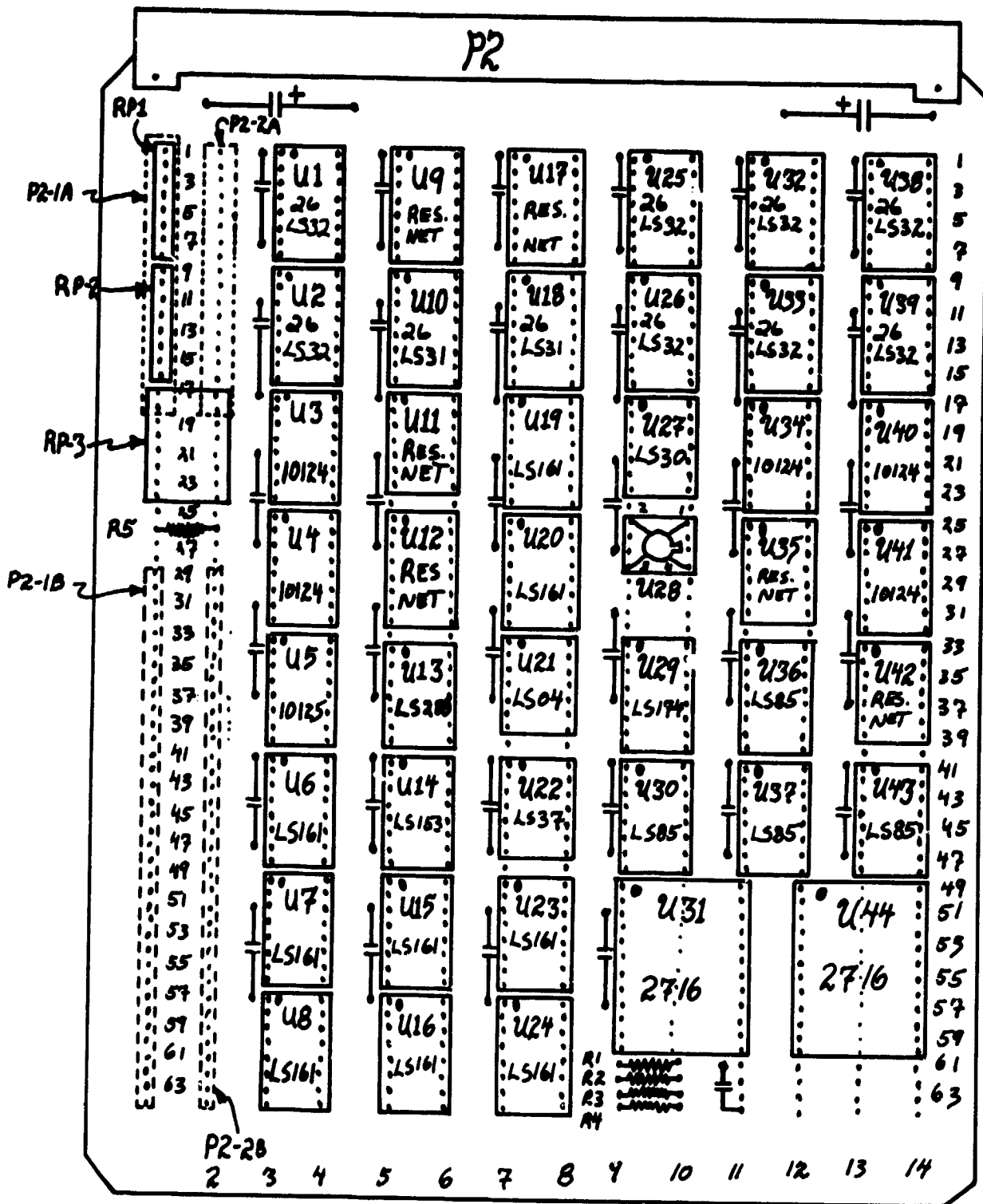
11 Oct 78 JJH  
 REV 11 Dec 78 JJH

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/ARMY OF TEXAS		1A. Contract No. NASS-15217-3		2. Code PL		3. Revision 1st	
5. LINE TITLE		6. Authorization:							
7. Description		8. Quantity		9. Unit		10. Part Number		11. Description	
<b>DDRS System Hardware</b>									
P2, P4, P11	3	ea.	3612061-01	108-pin Right Angle Plug					
J2, J4 J11, J3 J10	5	ea.	3612261-01	108-pin Receptacle					
P5, P7 P9	3	ea.	3612056-01	72-pin Right Angle Plug with Solder Connectors					
J5, J7, J9	3	ea.	3612251-01	72-pin Receptacle					
CAB1	1	ea.	3552015	36-conductor Flat Cable					
CAB2, CAB4	2	ea.	3552035	8-conductor Twisted-Pair Cable					
CAB3	1	ea.	3552045	18-conductor Twisted-Pair Cable Part of In --face Board					
P2-1, P2-2A P2-2B P2-2C	2	ea.	3234806-01	323 DIP Wirewrap Panel					
BOARD A BOARD B	1	ea.	3234890-01	323 Universal Wirewrap Panel Multilayer PC Board, ARL Custom					
BOARD C BOARD D BOARD E	3	ea.	3312045-01	6-position Half-Rack Assembly All hardware manufactured by NRPAC, Inc., with exception of PC boards.					

PARTS LIST		1. Agency (Contractor Identification)		1A. Contract No.		2. Code		3. PL		4. Revision	
5. List Title		APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		MS9-15217-4						B. Sheets 1 of 2	
6. Revision		7. New Assn. No.		8. Authentication:						C. Sheets 1 of 2	
INTERFACE BOARD (BOARD NO. 2)		11. Unit of Measure		12. Drawing (Spec.) or Document Number		13. Part or Ident. Number		14. Manufacturer or Description		15. Revision	
7. Item or Part Number	8. Qty Req	9. Unit of Measure	10. Drawing (Spec.) or Document Number	11. Part or Ident. Number	12. Manufacturer or Description	13. Revision	14. Revision	15. Revision	16. Revision	17. Revision	18. Revision
U5	1	ea		10125 DC	Quad ECL-to-TTL Translator, FAIRCHILD						
U3, U4, U34, U40 U41	5	ea		10124 DC	Quad TTL-to-ECL Translator, FAIRCHILD						
U6, U7, U8 U15, U16 U19, U20 U23, U24	3	ea		AM25LS161 DM	Hexadecimal Counter, ADVANCED MICRO DEVICES						
U10, U18	2	ea		AM26LS31 DM	Quad Differential Line Drivers, ADVANCED MICRO DEVICES						
U1, U2 U25, U26 U32, U33 U35, U39	8	ea		AM26LS32 DC	Quad Differential Line Receivers, ADVANCED MICRO DEVICES						
U14	1	ea		AM25LS153 DM	Dual Four-Input Multiplexer, ADVANCED MICRO DEVICES						
U29	1	ea		AM25LS174 DM	Hex D Flip-Flop, ADVANCED MICRO DEVICES						
U30, U36 U37, U43	4	ea		SN64LS85J	4-Bit Magnitude Comparators, TEXAS INSTRUMENTS						
U13	1	ea		SN64LS280J	9-Bit Parity Generator/Checker, TEXAS INSTRUMENTS						
U22	1	ea		SN64LS37J	Quad NAND Gate, TEXAS INSTRUMENTS						
U21	1	ea		SN64LS04J	Hex Inverter, TEXAS INSTRUMENTS						
U27	1	ea		SN64LS30J	Eight-Input NAND Gate, TEXAS INSTRUMENTS						
U28	1	ea		LA5600A	Temperature Transducer, National						
U1, U35 U42	3	ea		899-1-RES60	Resistor Network, 56 ohm, 13 Resistor, Pin 14 common, BECCOM						

PARTS LIST		1. Agency (Contractor Identification):		1A. Contract No.		2. Code		3.		4. Revision	
		APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS		MS9-15217-4		PL				Lit. Date	
5. List Title:		6. Authentication:		7. Rev Auth No.						8. Sheet 2 OF 2 Sheets	
INTERFACE BOARD (BOARD NO. 2)											
9. Item or Find Number	10. Qty Req	11. Unit Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Nomenclature or Description						
U9, U17 RP3	3	ea		316B 560	Resistor Network, 56 $\Omega$ , 8 resistors, ALLEN-BRADLEY						
U12	1	ea		316A561	Resistor Network, 560 $\Omega$ , Pin 16 common, ALLEN-BRADLEY						
RP1, RP2	2	ea		4308R-101-121	Resistor SIP, 120 $\Omega$ , 8 pin, BOURNS						
R1	1	ea		RCR07-102	Resistor, 1 k $\Omega$ , 5%, 1/4 W						
R2, R3, R4	3	ea		RCR07-101	Resistor, 100 $\Omega$ , 5%, 1/4 W						
R5	1	ea		RCR07-561	Resistor, 560 $\Omega$ , 5%, 1/4 W						
BYPASS CAP.	30	ea		1802- ZSUD50A104H	Capacitor, 0.1 $\mu$ F, GREEN GODDESS, VARADYNE						
BYPASS CAP.	2	ea		CSR1362264H	Capacitor, 22 $\mu$ F, Tantalum						
BOARD NO 2	1	ea		3234890-01	Universal 323-type wire-wrap panel, MUPAC						
CONNECTOR No. 2	1	ea		3612061-01	Connector, 108-pin, right angle, MUPAC						

COMPONENT SIDE



MUPAC # 3234890-01

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FIGURE A-2  
INTERFACE BOARD NO. 2



PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		1A. Contract No. 2. Code MASJ-15217-4		3. PL		4. Revision Ltr. Rev.	
3. List Title:		6. Authentication:		7. Rev Auth No.		8. Sheet 1 OF 2 Sheets			
VIDEO MEMORY (BOARD NO. 4)									
9. Item or Find Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description				
U1, U2				10415ADC	1024 x 1-bit RAM, Fairchild				
U3, U4									
U5, U6									
U7, U8									
U9, U10	16	ea.							
U11, U12									
U18, U19									
U26, U27									
U15, U16									
U17, U25	5	ea.		10174DC	Dual Multiplexer, Fairchild				
U29									
U13, U20	3	ea.		10101 DC	Quad OR/NOR Gate with Common Enable, Fairchild				
U33									
U32, U28	2	ea.		10115 DC	Quad Line Receiver, Fairchild				
U21, U14	2	ea.		10173 DC	Quad Multiplexer/Latch, Fairchild				
U30, U31	2	ea.		10016 DC	4-bit Binary Counter, Fairchild				
U34	1	ea.		10135 DC	Dual J-K Master-Slave Flip-Flop, FAIRCHILD				
U22	1	ea.		10136 DC	4-bit Up-Down Counter, Fairchild				
U23	1	ea.		10171 DC	Dual J-K Master-Slave Flip-Flop, Fairchild				
U37	1	ea.		10105 DC	Triple 2-3-2 Input OR/NOR Gate, Fairchild				
U36	1	ea.		PE 21171	20 nsec Delay Line, Pulse Engineering, Inc.				

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		2. Contract No. WAS-15217-4		3. Code PL		4. Revision Ltr. No.	
5. List Title: VIDEO MEMORY (BOARD NO. 4)		6. Authentication:		7. Bar Arch No.		8. Sheet 2 of 2 sheets			
9. Item or File Number	10. Qty Reqd	11. Unit Measure	12. Drawing (Spec.) or Document Number	13. Part Ident. Number	14. Manufacturer or Description				
—	75	ea.		RCR07-820	Resistor, 82 Ω, 1/4 W, 5%				
—	10	ea.		RCR07-390	Resistor, 39 Ω, 1/4 W, 5%				
—	7	ea.		RCR07-680	Resistor, 68 Ω, 1/4 W, 5%				
—	2	ea.		RCR07-470	Resistor, 47 Ω, 1/4 W, 5%				
D1	1	ea.		1N840	DIODE,				
—	14	ea.	2120	Z5V050R104M	Capacitor, Radial Lead, 0.1 μF, 50 V, Epoxy Dipped Ceramic Cap., VARADITE				
—	2	ea.			Tantalum/Capacitor, 33 μF, 25 V				
P4	1	ea.		3612056-01	72-pin Right-Angle Plug, MUPAC				
—	1	ea.			4.5 x 7.5, 4-layer Printed Circuit Board, ABL:UT				

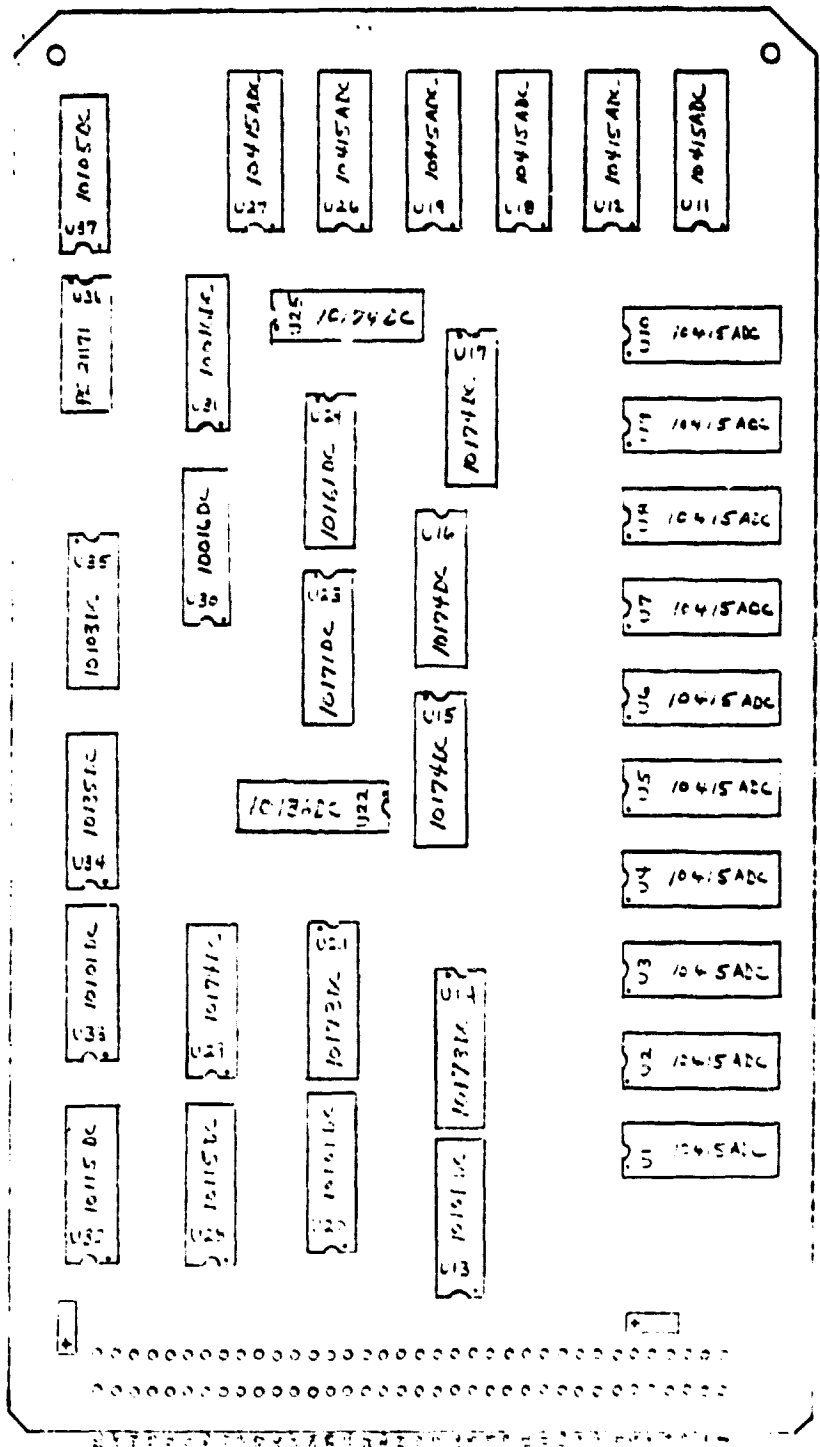
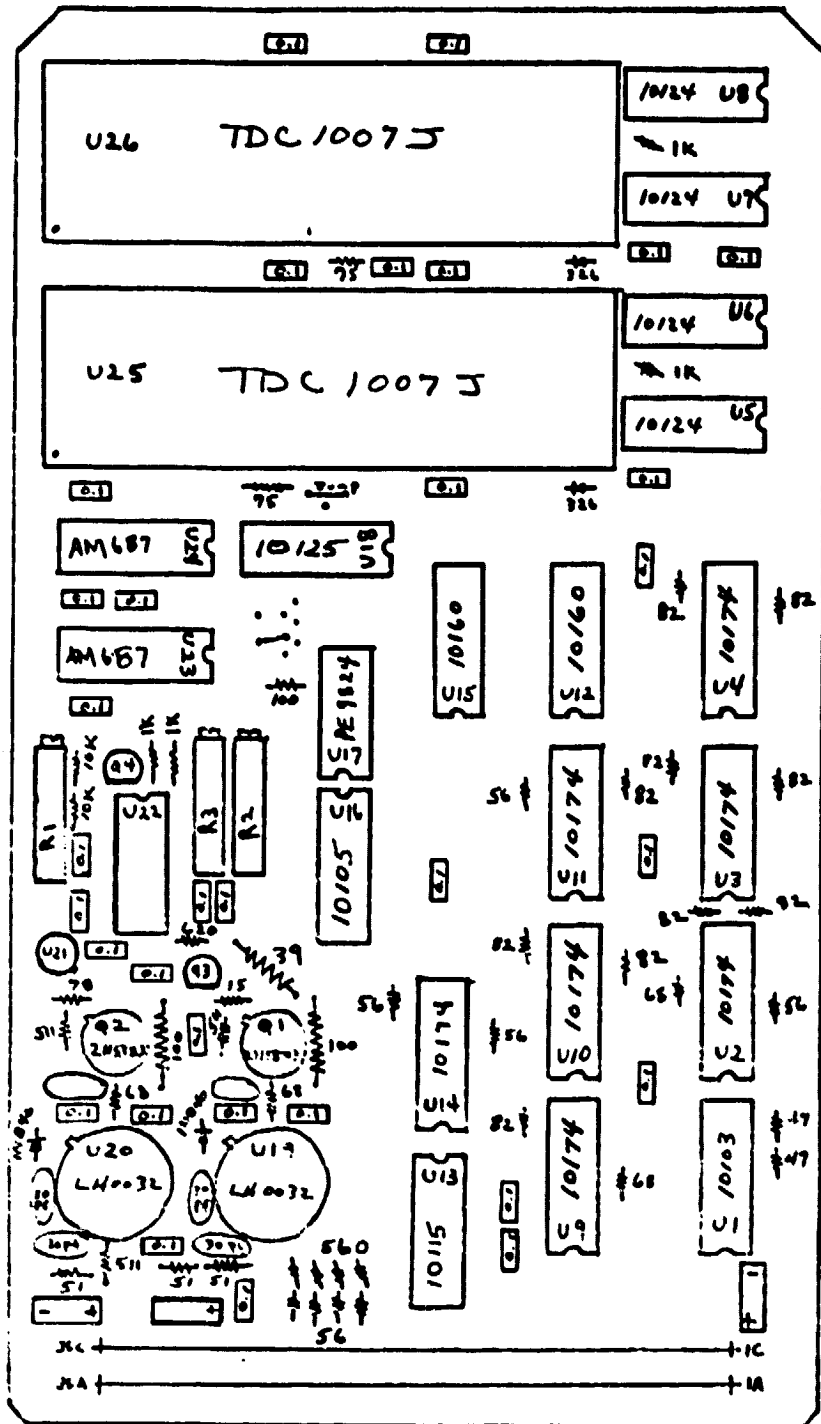


FIGURE A-3  
VIDEO MEMORY BOARD NO. 4

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS		1A. Contract No. HMS9-15217-4	2. Code PL	3. Rev. Auth. No.	4. Revision Ser. Date
5. List Title: Video A/D Board #6		6. Authentication:		7. Rev. Auth. No.		8. Sheet 1 of 2 Drawings	
9. Item or Part Number	10. Qty Reqd	11. Part Name (12. Drawing (Spec.) or Document Number)	13. Part or Ident. Number	14. Manufacturer or Description			
U26, U25	2	ea.	TDC1007J	8-bit Monolithic Video A/D Converter, TRM LSI Products			
U20, U19	2	ea.	LM0032G	Ultra-Fast FET Operational Amplifier, National			
U22	1	ea.	LM 1240	Quad Operational Amplifier, Fairchild			
U13	1	ea.	101150	Quad ECL Line Receiver, Fairchild			
U17	1	ea.	9824	50 nsec Delay Line, 5 nsec taps, Pulse Engineering, Inc.			
U18	1	ea.	101250	Quad ECL-to-TTL Translator, Fairchild			
U24, U23	2	ea.	94687D	Dual ECL Voltage Comparator, Advanced Micro Devices			
U16	1	ea.	101050	Triple OR/NOR Gate, Fairchild			
U5, U6,							
U7, U8	4	ea.	101240	Quad TTL-to-ECL Translator, Fairchild			
U12, U15	2	ea.	101600	12-bit ECL Parity Generator, Fairchild			
U2, U3, U4,							
U9, U10,							
U11, U14	7	ea.	101740	Dual 4-to-1 Multiplexer, Fairchild			
U1	1	ea.	101030	Quad ECL OR Gate, Fairchild			
U21	1	ea.	A05805H	Three-terminal 2.5 V Reference, Analog Devices			
Q1, Q2	2	ea.	2N5583	RF PNP Transistor, Motorola			
Q3, Q4	2	ea.	2N6403	PNP Transistor, Motorola			
C1, C2							
C3, C4							
C5, C6	6	ea.		Selected Silver Mica Capacitor			
C7, C8, C9	3	ea.		33 $\mu$ F, 25 V Tantalum Capacitor			
R1, R2, R3	3	ea.		1 k $\Omega$ Cermet Trimpot, Dale Series #784			
none				0.1 $\mu$ F, 50 V, Radial Leads, Ceramic Capacitor			

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PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		A. Contract No. MS9-15217-4		3. Code PL		4. Revision 1st	
5. List Title: Video A/D Board #6		6. Authentication:		7. Rev Auth No.		8. Sheet 2 of 2		9. Sheet 2 of 2	
9. Item or Find Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description				
R4, R19	2	ea.			51 Ω, 1/4 W, 5% resistor				
R5, R 6	4	ea.			511 Ω, 1/4 W, 1% resistor (see note 5)				
R20, R18	2	ea.			6.8 Ω, 1/4 W, 5% resistor				
R7, R21	2	ea.			100 Ω, 1/2 W, 5% resistor				
R8, R22	2	ea.			Selected 1/4 W, 5% resistor				
R10, R23	2	ea.			1 kΩ, 1/4 W, 5% resistor				
R13, R17	3	ea.			10 kΩ, 1/4 W, 5% resistor				
R15	2	ea.			75 Ω, 1/4 W, 5% resistor				
R11, R12	2	ea.			560 Ω, 1/4 W, 5% resistor				
R9, R24	1	ea.			39 Ω, 1/2 W, 5% resistor				
R14	1	ea.			5082-2800, Schottky Diode, Hewlett-Packard				
R16	4	ea.			assorted 47 Ω - 560 Ω, 1/4 W, 5%, as marked on schematic				
D1, D2	1	ea.		3612056-01	72-pin Right-Angle Plug, MUPAC, Inc.				
D3, D4	1	ea.			4.5 x 7.5, 4-layer Printed Circuit Board, ABL:UT				
none									
P6									



P6

FIGURE A-4  
VIDEO A/D BOARD NO. 6

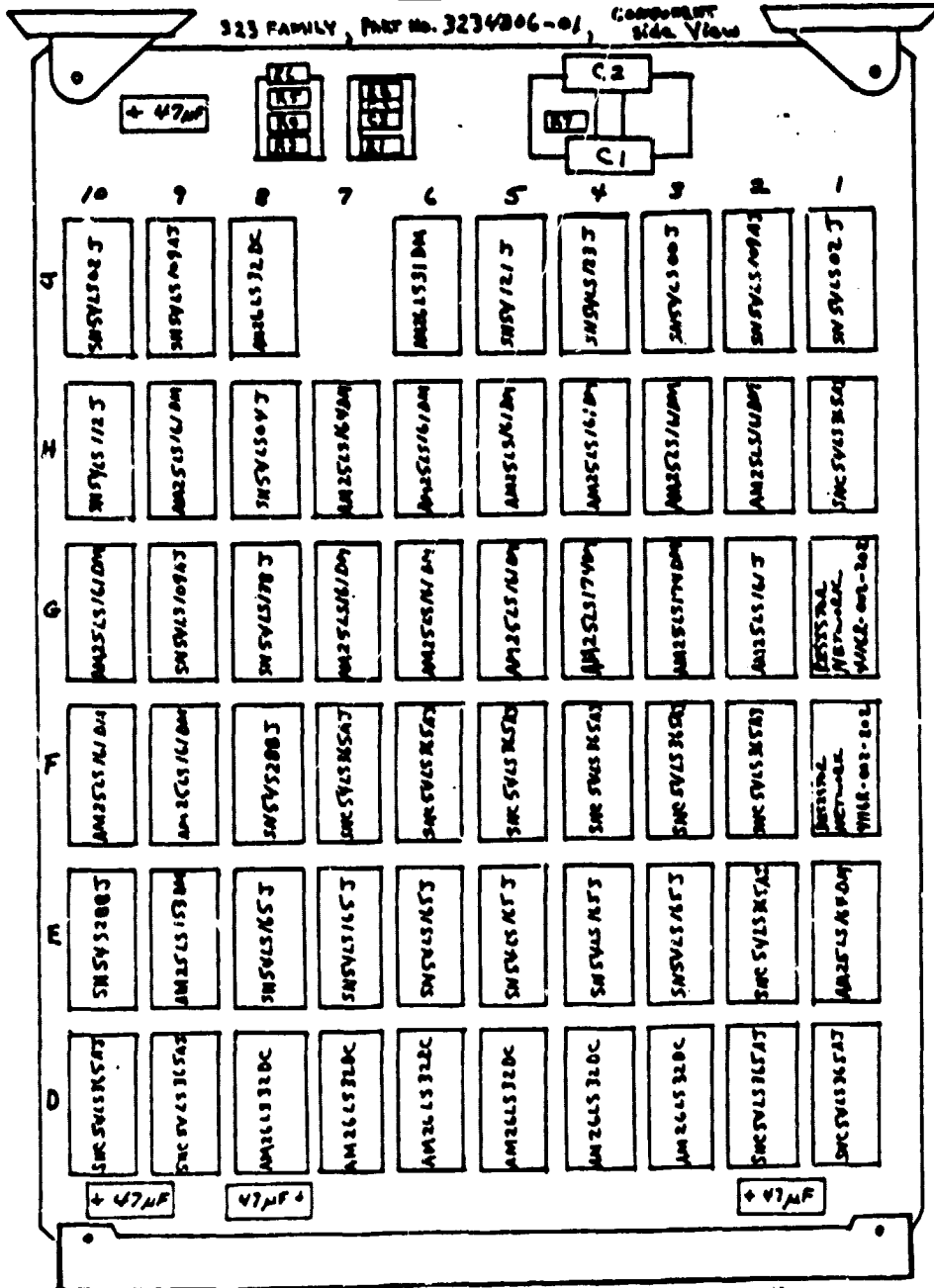
PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		1A. Contract No. MS9-15217-4		2. Code PL		3. Rev. Auth. No.		4. Revision Ltr. Date	
5. List Title: RPE FORMATTING BOARD		BOARD NO. 8		6. Architecture:		7. Rev. Auth. No.		8. Sheet 1 of 2		9. Sheet 1 of 2	
9. Item or Find Number	10. Qty Reqd	11. Unit Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description						
UD1, UD2 UD9, UD10 UE2, UF2 UF3, UF4 UF5, UF6 UF7, UH1	12	ea		SMC54LS365AJ	Hex Bus Buffer/Driver with 3-state outputs, Texas Instruments						
UE9	1	ea		AM25LS153 DM	Dual 4-to-1 Multiplexer, Advanced Micro Devices						
UF9, UF10 UG2, UG5 UG6, UG7 UG10, UH2 UH3, UH4 UH5, UH6 UH9	13	ea		AM25LS161 DM	4-Bit Synchronous Counter, Advanced Micro Devices						
UG3, UG4	2	ea		AM25LS174 DM	6-Bit D Flip-Flop, Advanced Micro Devices						
UF1, UG1	2	ea		4116A-002-202	Resistor Network, 2.0 k $\Omega$ , 15 resistors with one common pin, Bourns						
UE3, UE4 UE5, UE6 UE7, UE8	6	ea		SM54LS165J	Parallel Load 8-Bit Shift Register, Texas Instruments						
UE10, UF8	2	ea		SM54S288J	32 x 8 PROM with 3-state Output, TEXAS INSTRUMENTS						
UG8	1	ea		SM54LS138J	3-to-8 Decoder, Texas Instruments						
UH8	1	ea		SM54LS04J	Hex Inverter, Texas Instruments						
UJ3	1	ea		SM54LS00J	Quad NAND Gate, Texas Instruments						
UE9, UJ2 UJ9	3	ea		SM54LS109AJ	Dual J-K Positive Edge-Triggered Flip-Flop, Texas Instruments						

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		1A. Contract No. MSS-15217-9		2. Code PL		3. Rev. Auth. No.		4. Revision Exp. Date	
5. List Title: RPE FORMATTING BOARD (BOARD NO. 8)		6. Attachment:		7. Rev. Auth. No.		8. Sheet 2 of 2		9. Sheet 2 of 2		10. Sheet	
9. Item or Part Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description						
UJA	1	ea		SMS4LS123J	Dual Retriggerable One-Shot, TEXAS INSTRUMENTS						
UJS	1	ea		SMS4121J	One-shot with Schmitt Trigger Input, TEXAS INSTRUMENTS						
UHO	1	ea		SMS4LS112J	Dual J-K Negative Edge-Triggered Flip-Flop, TEXAS INSTRUMENTS						
UET, UH7	2	ea		AMS4LS164DN	8-bit Serial-in, Parallel-out Shift Register, ADVANCED MICRO DEVICES						
UD3, UD4 UD5, UD6 UD7, UDB ULB	7	ea		AMS4LS32DC	Quad Differential Line Receiver, ADVANCED MICRO DEVICES						
ULB	1	ea		AMS4LS10N	Quad Differential Line Driver, ADVANCED MICRO DEVICES						
UJ10, UJ1	2	ea		SMS4LS02J	Quad NOR Gate, TEXAS INSTRUMENTS						
R1, R2	2	ea		RCR07-184	Resistor, 180 oh, 5%, 1/4 W						
R3, R4	2	ec		RCR07-122	Resistor, 1.2 ka, 5%, 1/4 W						
R5, R6	2	ea		RCR07-121	Resistor, 120 oh, 5%, 1/4 W						
R7	1	ea		RCR07-221	Resistor, 220 oh, 5%, 1/4 W						
C1, C2	2	ea		CSR13C2261N	Capacitor, 22 uF, Tantalum						
C3	1	ea		CMFDM70J0	Capacitor, 47 pf, DIP MICA, 55						
BYPASS CAPS	25	ea		1802- Z5U050A104H	Capacitor, 0.1 uF, GREEN GOODNESS, VARIOUS						
BYPASS CAPS	4	ea		CSR13C4761N	Capacitor, 47 uF, Tantalum						
Board PB Connector	1	ea		3234806-01 3612061-01	Wire-wrap Board, RUPAC, Inc. Connector, 108 pin, RUPAC, Inc.						



# MUPAC

325 FAMILY, Part No. 3234806-01, COMPONENT Side View



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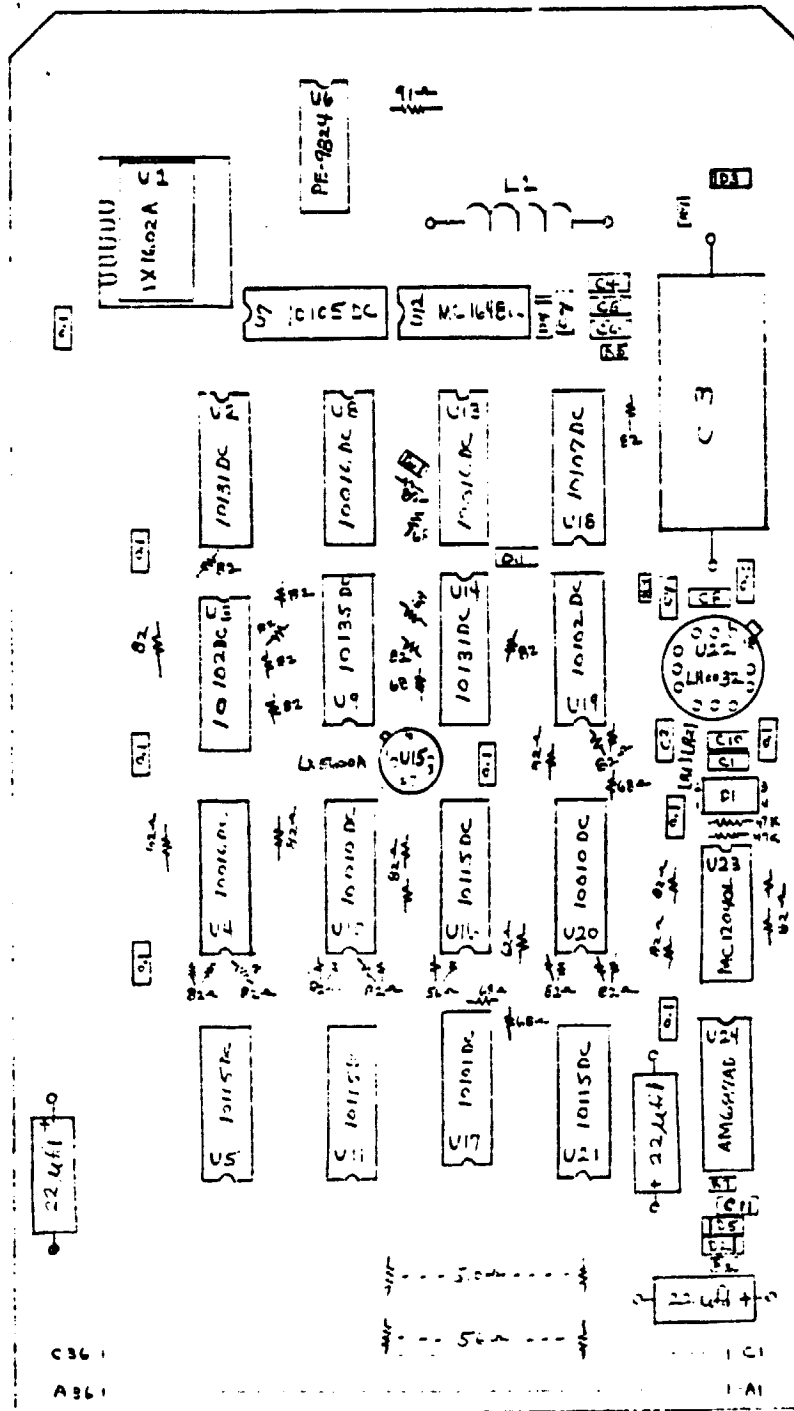
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DATE	DEC 78	BY	JUN
BOARD No.	00		
NAME	RPE FORMATTING		

FIGURE A-5  
RPE FORMATTING BOARD NO. 8

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS		14. Contract No. MAS9-15217-4		3. Code PL		4. Revision LIT. None	
5. Item Title: CLOCK GENERATOR BOARD #9		6. Authentication:		7. Rev Auth No.		8. Sheets 1 of 2 Sheet			
9. Item or Part Number	11. Unit or Quantity	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description					
U7	1 ea.		10105	Triple OR/NOR Gate, Fairchild					
U5, U11,									
U16, U21	4 ea.		10115	Quad Line Receiver, Fairchild					
U4, U8, U13	3 ea.		10016	Hexadecimal Counter, Fairchild					
U10, U20	2 ea.		10010	Decimal Counter, Fairchild					
U2, U14	2 ea.		10131	Dual D Flip-Flop, Fairchild					
U9	1 ea.		10135	Dual J-K Flip-Flop, Fairchild					
U3, U19	2 ea.		10102	Quad NOR Gate, Fairchild					
U18	1 ea.		10107	Triple Exclusive OR/NOR Gate, Fairchild					
U17	1 ea.		10101	Quad OR/NOR Gate, Fairchild					
U23	1 ea.		MC12040	Phase-Detector, Motorola					
U12	1 ea.		MC1648	Voltage Controlled Oscillator, Motorola					
U24	1 ea.		AM687A	Voltage Comparator, Advanced Micro Devices					
U22	1 ea.		LM0032	FET-Input Operational Amplifier, National					
U15	1 ea.		LX560CA	Temperature Transducer, National Semiconductor					
U1	1 ea.		LX1602A	Pressure Transducer, National Semiconductor					
U6	1 ea.		PC-3024	Delay Line, 50 nsec, 5 msec taps, Pulse Engineering, Inc.					
P9	1 ea.		N/A	4.5 x 7.5 4-layer Printed Circuit Board, ABL:UT					
R1, R2	2 ea.		3612056-01	72-pin Right Angle Plug with Solder Connectors, RUPAC, Inc.					
R3	1 ea.			Resistor, 8.2 k $\Omega$ , 1/8 W, 5%					
R4	1 ea.			Resistor, 27 k $\Omega$ , 1/8 W, 5%					
R5	1 ea.			Resistor, 100 $\Omega$ , 1/8 W, 5%					
R6, R7	2 ea.			Resistor, 1.0 k $\Omega$ , 1/8 W, 5%					
None	32 ea.			Resistor, 27 $\Omega$ , 1/4 W, 5%					
				Resistor, 82 $\Omega$ , 1/8 W, 5%					

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/LINKS OF TEXAS		2. Contract No. MS9-15277-4		3. Code PL		4. Revision Let. No. 2 of 2	
5. Main Title: CLOCK GENERATOR BOARD #9		6. Authorized Location:		7. Rev. Auth. No.					
9. Item or Part Number	10. Qty. of Part	11. Detail Drawing (Spec.) Description	12. Part or Material Number	13. Part or Material Number	14. Manufacturer or Description				
R7	1	08.			Resistor, 47 Ω, 1/4 W, 5% Resistor, 910 Ω, 1/4 W, 5%				
R8	1	08.			Resistor, 91 Ω, 1/8 W, 5% Resistor, 68 Ω, 1/8 W, 5% Resistor, 47 Ω, 1/8 W, 5%				
R9	1	08.			Resistor, 62 Ω, 1/4 W, 5%				
R10	12	08.			Resistor, 510 Ω, 1/4 W, 5%				
R11	12	08.			Resistor, 56 Ω, 1/4 W, 5%				
C1	1	08.			Capacitor, 1 μf, Dipped Mica				
C2	2	08.			Capacitor, 0.1 μf, Ceramic				
C3	1	08.			Capacitor, 5000 pf, Polystyrene				
C4, C5	3	08.			Capacitor, 0.01 f, Polycarbonate				
C6	1	08.			Capacitor, Selected, Dipped Mica				
C7	1	08.			Capacitor, Selected, Dipped Mica				
C8	1	08.			Capacitor, Selected, Dipped Mica				
C9	1	08.			Capacitor, Selected, Dipped Mica				
C10	1	08.			Capacitor, Selected, Dipped Mica				
R12	11	08.			Capacitor, 0.1 μf, Ceramic Bypass				
R13	3	08.			Capacitor, 22 μf, Tantalum				
D1	1	08.		CSR13C2260R WP-02-2814	Matched Quad Schottky Diode Bridge, Hewlett-Packard				
D2, D3	4	08.		1B840	DIODE				
D4, D5	1	08.		1B 5468A	Voltage-Variable Capacitance (Varactor) Diode, Motorola				
D6	1	08.			Inductor, 3 turns, 16 gauge wire				
L1	1	08.							



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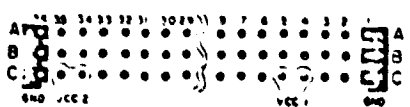
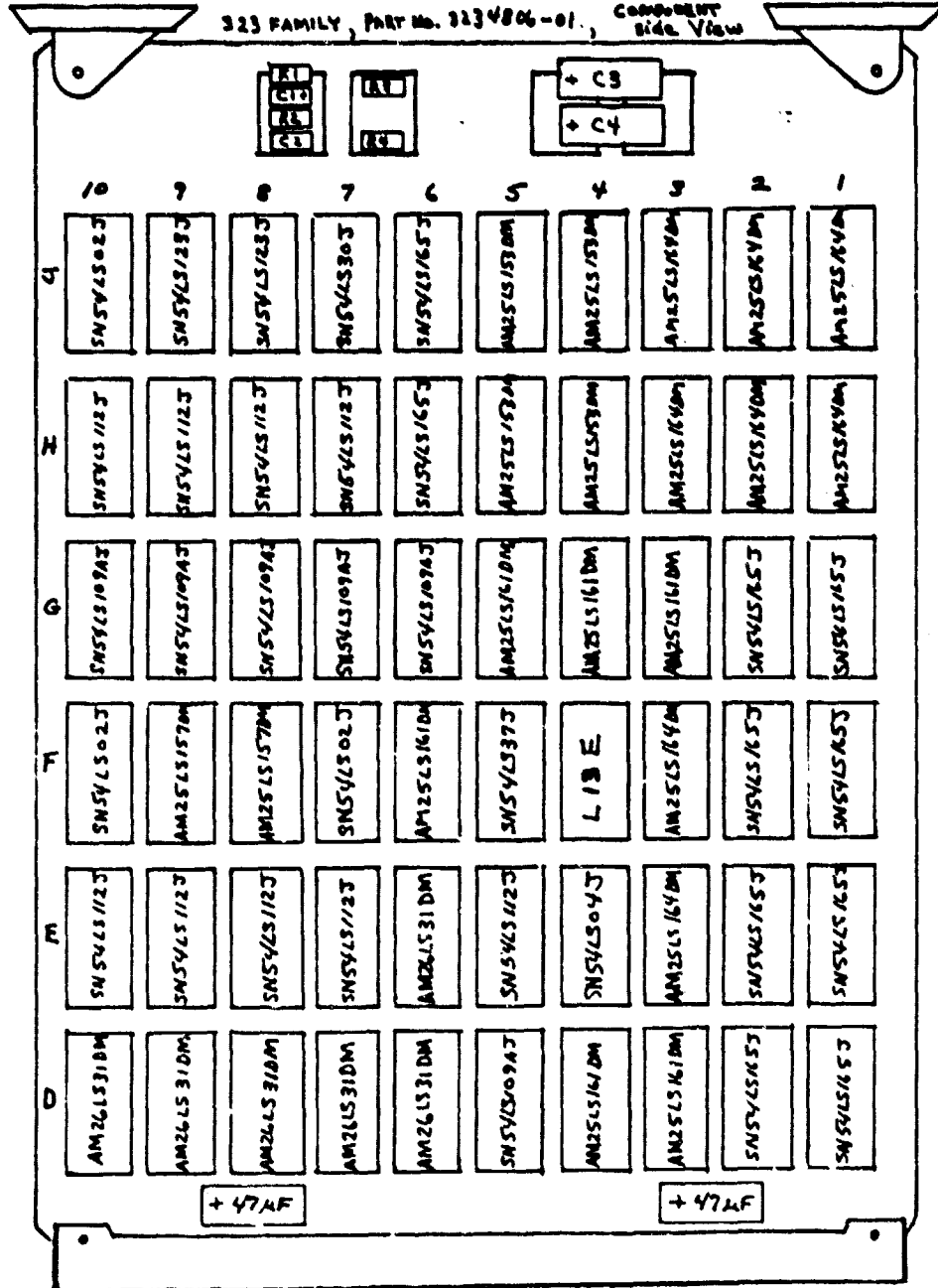
FIGURE A-6  
CLOCK GENERATOR BOARD NO. 9

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV OF TEXAS			1A. Contract No. MS9-15217-4	2. Code Agency	3. PL	4. Revision Ltr. Date
5. List Title: VIDEO FORMATTING BOARD (BOARD NO. 11)		6. Authentication:			7. Rev Auth No.		8. Sheet of 2 1 Sheets	
9. Item or Find Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part or Ident. Number	14. Manufacturer or Description			
UG5, UG6 UG7, UG8 UG9, UG10	6	ea.		SMS4LS109AJ	Dual J-K Positive-Edge Triggered, Flip-Flop, Texas Instruments			
UE5, UE7 UE8, UE9 UE10, UH7 UH8, UH9 UH10	9	ea.		SMS4LS112J	Dual J-K Negative-Edge Triggered, Flip-Flop, Texas Instruments			
UF8, UF9 UE6, UO6 UD7, UO8 UD9, UD10 UJ7 UJ8, UJ9	2 6 1 2	ea. ea. ea. ea.		AM25LS157DM AM26LS31DM SMS4LS30J SMS4LS123J	Quad 2-Input Multiplexer, ADVANCED MICRO DEVICES Quad Differential Line Driver, ADVANCED MICRO DEVICES 8-Input Positive NAND Gate, Texas Instruments Dual Retriggerable, Monostable Multivibrators with Clear, Texas Instruments			
UE4 UJ3 UD1, UD2 UE1, UE2 UF1, UF2 UG1, UG2 UH6, UH6 UE3, UF3 UH1, UH2 UH3, UJ1 UJ2	1 1 10 1 1 1 7	ea. ea. ea. ea.		SMS4LS04J AM25LS174DM SMS4LS165J AM25LS164DM	Hex Inverters, Texas Instruments 6-Bit Register with Common Clear, ADVANCED MICRO DEVICES Parallel-Load, 8-Bit, Serial Shift Register, Texas Instruments 8-Bit, Serial-In, Parallel-Out Shift Register, ADVANCED MICRO DEV			

PARTS LIST		1. Agency (Contractor Identification): APPLIED RESEARCH LABORATORIES/UNIV. OF TEXAS			1A. Contract No. MA59-15217-4	2. Code Army.	3. PL	4. Revision Let. Date
5. List Title: VIDEO FORMATTING BOARD (BOARD NO. 11)		6. Authentication:			7. Rev. Auth. No.			8. Sheet 2 of 2 (Sheet)
9. Item or Print Number	10. Qty Reqd	11. Unit of Measure	12. Drawing (Spec.) or Document Number	13. Part of Ident. Number	14. Manufacturer or Description			
U4A, U4B	4	ea.		AM25LS153DN	Dual 4-Input Multiplexer, ADVANCED MICRO DEVICES			
U4C, U4D	6	ea.		AM25LS161DN	Synchronous 4-Bit Binary Counter, Asynchronous Clear, ADVANCED MICRO DEVICES			
U4E, U4F	1	ea.		SN64LS37J	Quad 2-Input Positive NAND Buffers, Texas Inst.			
U4G, U4H	3	ea.		SN64LS02J	Quad 2-Input Positive NOR Gates, Texas Inst.			
U4I, U4J	1	ea.		L13E	DIP Crystal Oscillator, 3.84 MHz, Comer-Minfield Corp. Capacitor, 1 $\mu$ F			
U4K, U4L	1	ea.			Capacitor, 0.082, Tantalum			
U4M, U4N	2	ea.			Capacitor, 12 $\mu$ F, Tantalum			
U4O, U4P	4	ea.		RC07-184	Resistor, 180 $\Omega$ , 1/4 W, 5%			
U4Q, U4R	1	ea.		323A806-01	Panel (Wire Wrap Board) Mfg. MUPAC, Inc.			
U4S, U4T	1	ea.		3612061-01	108-Pin Plug, MUPAC, Inc.			
U4U, U4V	25	ea.			Capacitor, 0.1 $\mu$ F, Ceramic (Green Goddess) VARADYNE			
U4W, U4X	2	ea.			Capacitor, 47 $\mu$ F, Tantalum			

# MUPAC

323 FAMILY, Part No. 3234806-01, COMPONENT Side View



DATE	1 DEC 78	258
BOARD NO.	11	JJH
NAME	VIDEO FORMATTING	

FIGURE A-7  
VIDEO FORMATTING BOARD NO. 11

APPENDIX B

DIGITAL DATA RECORDING SYSTEM  
ACCEPTANCE PROCEDURE



**DIGITAL DATA RECORDING SYSTEM  
ACCEPTANCE PROCEDURE**

**STANDARD CONFIGURATION**

1. Data precision - 7 bit
2. Sample Interval - 70 nsec
3. Range Delay - 2  $\mu$ sec
4. Ramp Function - 1 V pp



JLW

## TEST 1. DATA PRECISION SELECTION (Cont'd)

## 5. Verify Proper RPE Words

Observed	
Data Precision	<u>7 BIT</u>
Sample Interval	<u>76.4 <math>\mu</math>SEC</u>
Range Delay	<u>1.93 <math>\mu</math>SEC</u>
Heading	<u>000</u>
Temp 1	<u>28.64 °C</u>
2	<u>27.15</u>
3	<u>X (NC)</u>
4	<u>19.24</u>
Negative Volt 5.7	<u>-5.75</u>
<i>POSITIVE</i>	
<i>DDRS</i> Negative Volt 5	<u>5.04</u>
Negative Volt 2	<u>-2.07</u>
<i>AUX</i> Positive Volt 5	<u>4.98</u>
Negative Volt 15	<u>-15.05</u>



1-30-79

*JLH*

TEST 1. DATA PRECISION SELECTION (Cont'd)

5. Verify Proper RPE Words

Observed

Data Precision 4 BIT

Sample Interval 70.4 MSEC

Range Delay 1.93 MSEC

Heading \_\_\_\_\_

Temp 1 29.03 °C

2 28.21

3 NC

4 19.58

Negative Volt 5.7 -5.75

DDRS <sup>POSITIVE</sup> Negative Volt 5 5.04

Negative Volt 2 -2.07

AUX Positive Volt 5 4.98

Negative Volt 15 -15.05

TEST 1. DATA PRECISION SELECTION

1. Set Standard Configuration

- a. Data Precision - 2 bit 2 BIT
- b. Sample Interval - 70 nsec ✓
- c. Range Delay 2  $\mu$ sec ✓
- d. Ramp Function (1 Vpp) - 225 KHZ

*MTD*

2. Set and Record Identifying word in RPE Data

Identifier word set 002  
Identifier word observed 002

3. Record and view data for 7-, 4-, and 2-bit precision 2 BIT

4. On print out verify proper operation of the recorded signals.

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	Range Bin	Range Bin
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
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1-30-79

TEST 1. DATA PRECISION SELECTION (Cont'd)

*MTP*

5. Verify proper RPE words

Observed

Data Precision 2 BIT

Sample Interval 70.4 mSEC

Range Delay 1.93  $\mu$ SEC

Heading \_\_\_\_\_

Temp 1 29.22 °C

2 28.61

3 NC

4 19.64

Negative Volt 5.7 -5.75

DDPS <sup>POSITIVE</sup> Negative Volt 5 +5.04

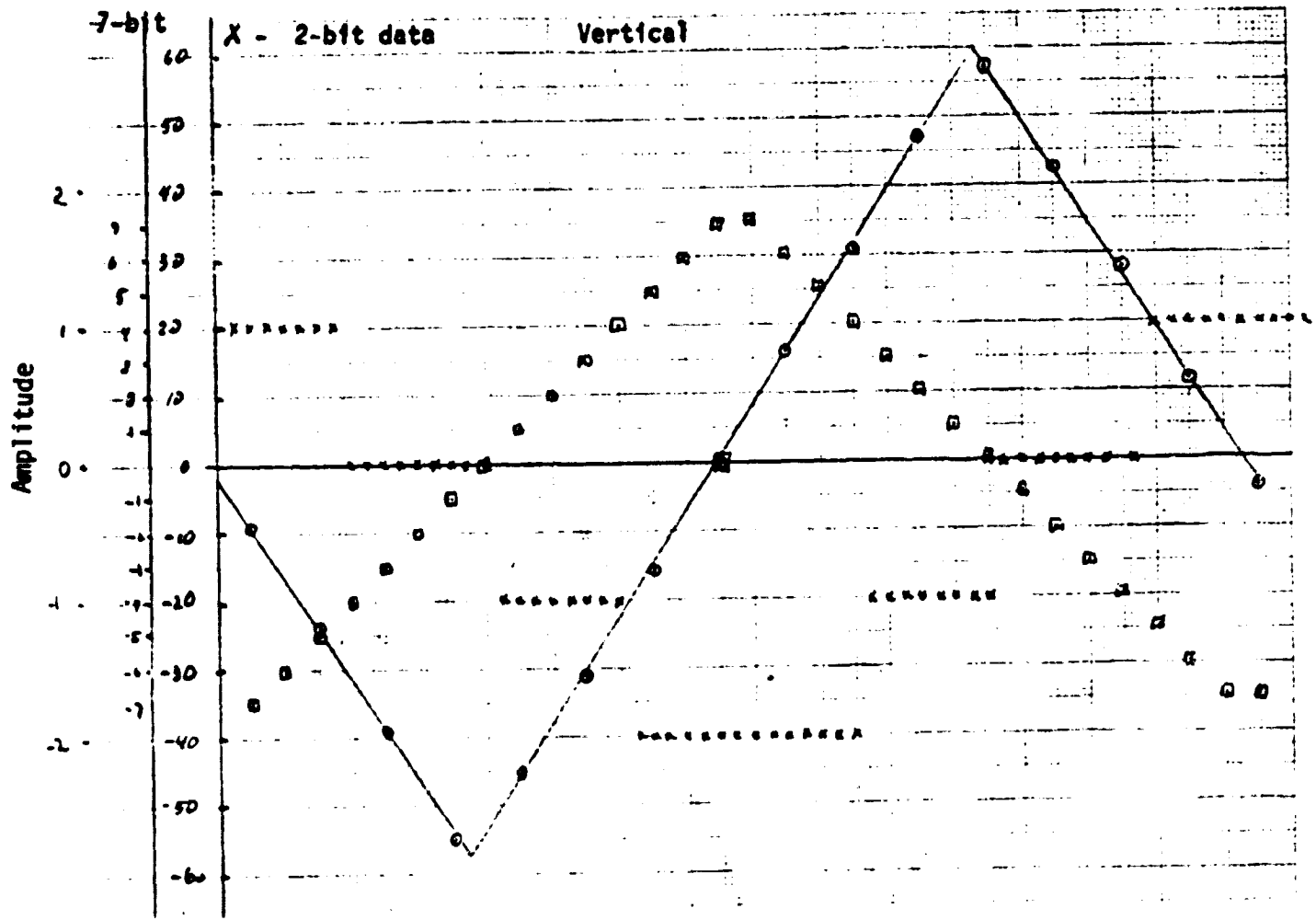
Negative Volt 2 -2.07

AUX Positive Volt 5 +4.98

Negative Volt 15 -15.05

1-30-79  
RTP

- PULSE NO. 1
- - Range Bins 16-31  
7-bit data            Horizontal
- - Range Bins 32-63  
4-bit data            Vertical



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FIGURE B-1  
DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVEFORM INPUT



1-30-79  
ETP

Test 000  
70 nsec Sample Interval  
7-bit Data Precision  
—○— Horizontal Channel  
--□-- Vertical Channel  
Pulse 1, Range Bins 16-31

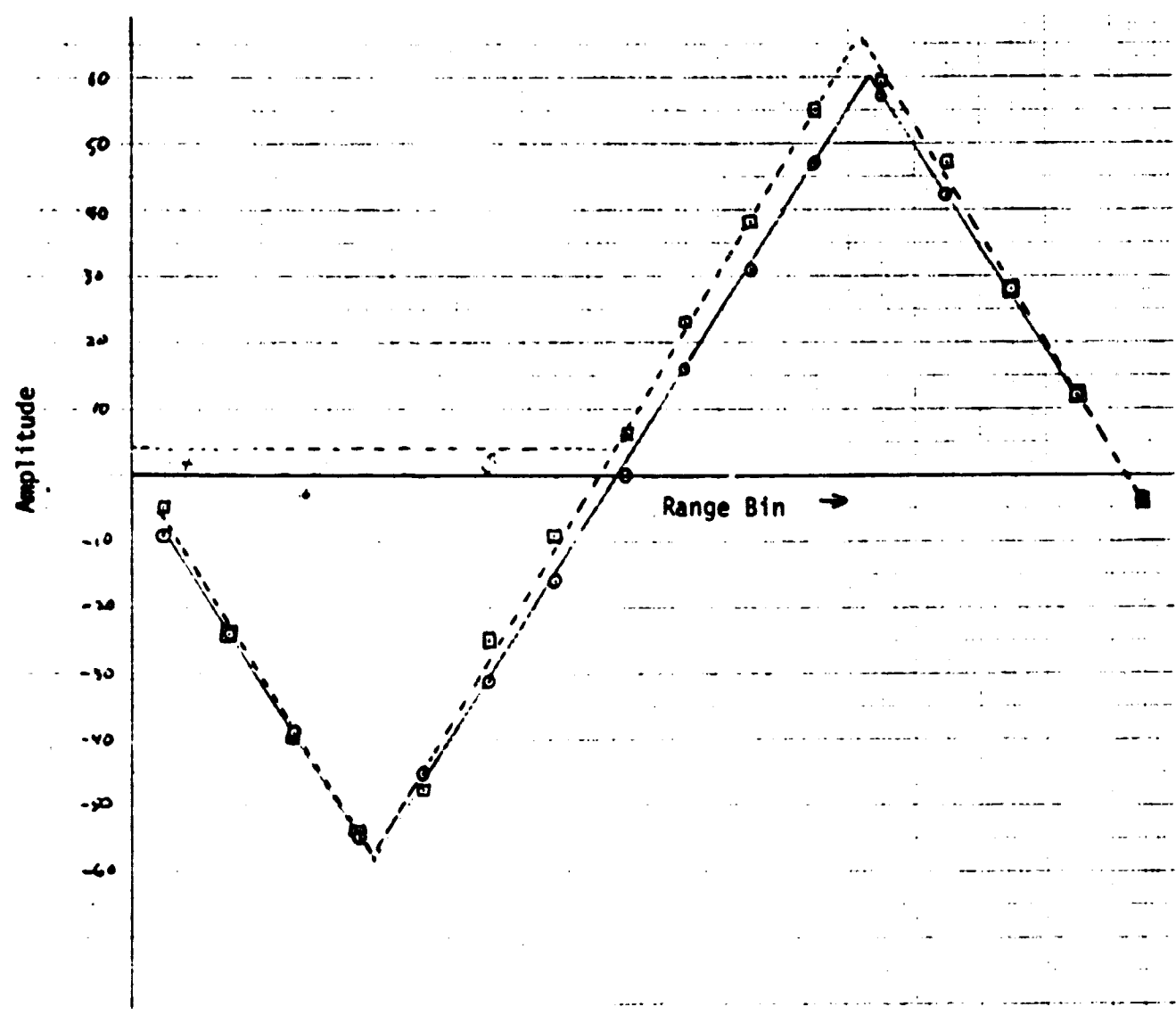


FIGURE B-2  
DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVEFORM INPUT

1-30-79  
JST

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Test 000  
70 nsec  
7-bit Data  
Pulse 21, Range Bins 16-31  
Arrows identify parity error indications

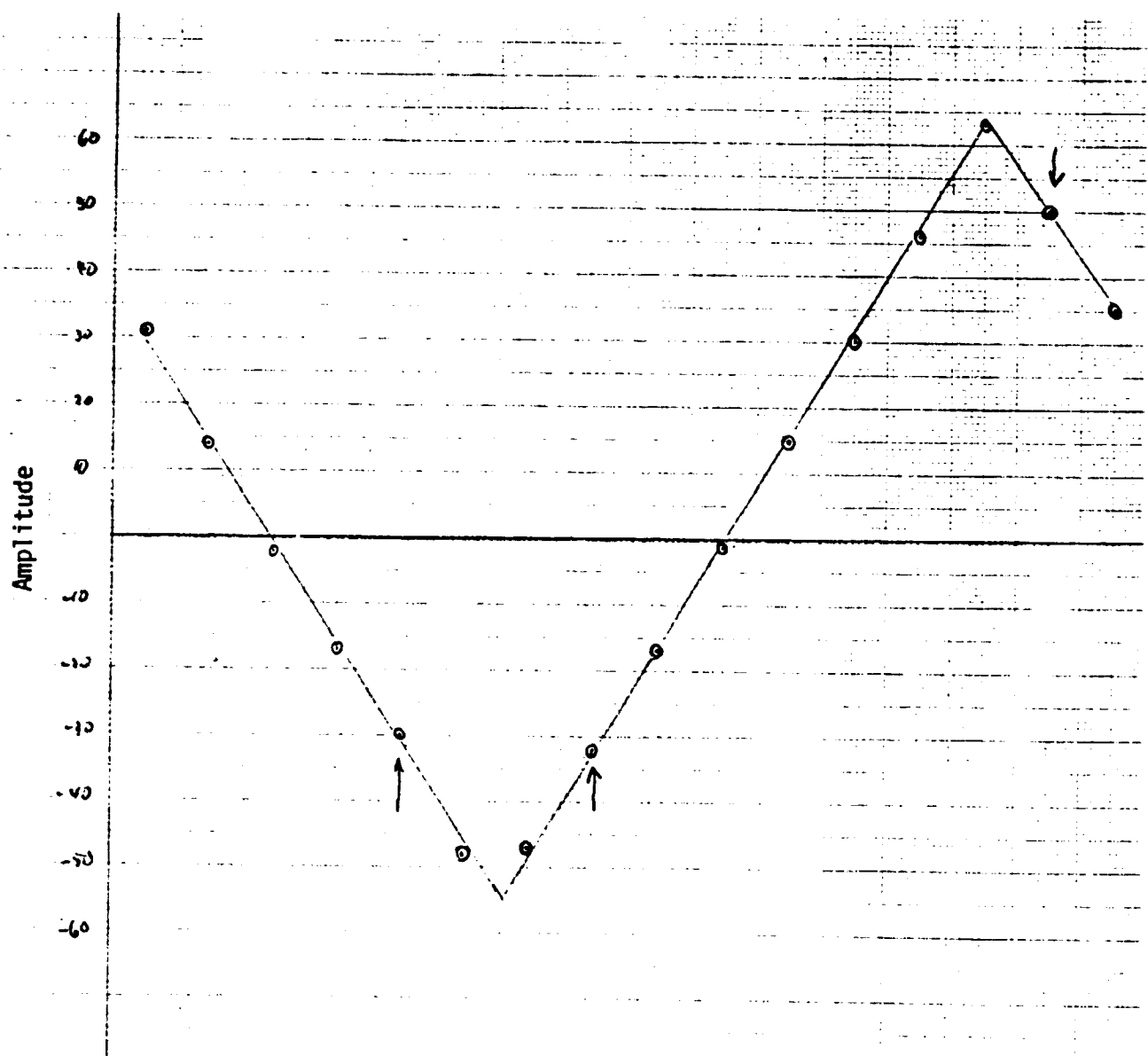


FIGURE B-3  
DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVEFORM INPUT  
125

TEST 2. SLANT RANGE SAMPLE INTERVAL

1-30-79

1. Set Standard Configuration a. 7-BIT b. \_\_\_\_\_ c. 2.456C d. RAMP-514 KHZ

2. Set and Record Identifying Word in RPE Data

Identifier word set 003

Identifier word observed 003

*ITP*

3. Verify proper sample interval using scope

Selected Sample Interval

40 <sup>M SEC</sup>  
~~42~~  
\_\_\_\_\_  
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Observed Sample Interval

42 <sup>M SEC</sup>  
~~42~~  
\_\_\_\_\_  
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4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin \_\_\_\_\_  
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TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd)

5. Verify proper RPE words

Observed

*MFP*

Data Precision 7 BIT

Sample Interval 40.2 mSEC

Range Delay 1.93 μSEC

Heading \_\_\_\_\_

Temp 1 27.03 °C

2 26.51

3 NC

4 19.27

Negative Voltage 5.7 - 5.75

*DDRS* <sup>POSITIVE</sup> Negative Voltage 5 + 5.04

Negative Voltage 2 -2.06

*AUX* Positive Voltage 5 +4.98

Negative Voltage 15 - 15.05

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7 BIT b. \_\_\_\_\_ c. 2 μSEC d. RAMP - 642 KHZ

2. Set and Record Identifying Word in RPE Data

Identifier word set 004

Identifier word observed 004

*JTP*

3. Verify proper sample interval using scope

Selected Sample Interval

Observed Sample Interval

50 μSEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

52.5 μSEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin \_\_\_\_\_  
\_\_\_\_\_  
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Range Bin \_\_\_\_\_  
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Range Bin \_\_\_\_\_  
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5. Verify proper RPE words

Observed

*JTP*

Data Precision 7 BIT

Sample Interval 50.31 mSEC

Range Delay 1.93 μSEC

Heading \_\_\_\_\_

Temp 1 27.61 °C

2 27.03

3 NC

4 19.58

Negative Voltage 5.7 -5.75

*DDPS* <sup>POSITIVE</sup> ~~Negative~~ Voltage 5 +5.04

Negative Voltage 2 -2.07

*AUX* Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7 BIT b. \_\_\_\_\_ c. 2  $\mu$  SEC d. RAMP-771 KHZ

2. Set and Record Identifying Word in RPE Data

Identifier word set 005

Identifier word observed 005

*LTP*

3. Verify proper sample interval using scope

Selected Sample Interval

Observed Sample Interval

60  $\mu$  SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

63  $\mu$  SEC  
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4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin \_\_\_\_\_  
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1-30-79

## 5. Verify proper RPE words

Observed

Data Precision 7 BITSample Interval 60.37  $\mu$ SECRange Delay 1.93  $\mu$ SEC

Heading \_\_\_\_\_

Temp 1 27.85 °C2 27.363 NC4 19.67Negative Voltage 5.7 -5.75DDPS ~~NEGATIVE~~ POSITIVE Voltage 5 +5.04Negative Voltage 2 -2.07AUX Positive Voltage 5 +4.98Negative Voltage 15 -15.06

JLTD





TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd)

1-30-79

5. Verify proper RPE words

*JFP*

Observed

Data Precision 7 BIT

Sample Interval 70.4  $\mu$ SEC

Range Delay 1.93  $\mu$ SEC

Heading \_\_\_\_\_

Temp 1 27.97 °C

2 27.57

3 NC

4 19.79

Negative Voltage 5.7 -5.75

*DDRS* <sup>POSITIVE</sup> ~~Negative~~ Voltage 5 +5.04

Negative Voltage 2 -2.07

*AUX* Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

TEST 2. SLANT RANGE SAMPLE INTERVAL

1-30-79

1. Set Standard Configuration a. 7 BIT b. \_\_\_\_\_ c. 2 μSEC d. RAMP - 1028 KHz

2. Set and Record Identifying Word in RPE Data

Identifier word set 007

Identifier word observed 007

*HTD*

3. Verify proper sample interval using scope

Selected Sample Interval

Observed Sample Interval

80 μSEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

84 μSEC  
\_\_\_\_\_  
\_\_\_\_\_  
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\_\_\_\_\_

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin \_\_\_\_\_  
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TEST 2. SLANT RANGE SAMPLE INTERVAL (Cont'd)

1-30-79

5. Verify proper RPE words

*JTD*

Observed

Data Precision 7 BIT

Sample Interval 80.49 m SEC

Range Delay 1.93 μ SEC

Heading \_\_\_\_\_

Temp 1 28.18°C

2 27.85

3 NC

4 19.88

Negative Voltage 5.7 -5.75

*DDRS* <sup>POSITIVE</sup> ~~Negative~~ Voltage 5 +5.04

Negative Voltage 2 -2.07

*AUX* Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

1-30-79

TEST 2. SLANT RANGE SAMPLE INTERVAL

1. Set Standard Configuration a. 7 BIT b. \_\_\_\_\_ c. 2 USEC d. RAMP-1157 KHZ

2. Set and Record Identifying Word in RPE Data

Identifier word set 008

Identifier word observed 008

*JFP*

3. Verify proper sample interval using scope

Selected Sample Interval

Observed Sample Interval

90 n SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

93 n SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin	_____
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## 5. Verify proper RPE words

Observed

Data Precision 7 BitSample Interval 90.55 MSECRange Delay 1.93  $\mu$  SEC

Heading \_\_\_\_\_

Temp 1 28.55°C2 28.493 NC4 20.03Negative Voltage 5.7 -5.75DDRS <sup>POSITIVE</sup> ~~Negative~~ Voltage 5 +5.04Negative Voltage 2 -2.08AUX Positive Voltage 5 +4.98Negative Voltage 15 -15.06

JTFP

TEST 2. SLANT RANGE SAMPLE INTERVAL

1-30-79

1. Set Standard Configuration a. 7 BIT b. \_\_\_\_\_ c. 24 SEC d. RAMP-1285KHz

2. Set and Record Identifying Word in RPE Data

Identifier word set 009

Identifier word observed 009

*HTP*

3. Verify proper sample interval using scope

Selected Sample Interval

Observed Sample Interval

100 MSEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

104 MSEC  
\_\_\_\_\_  
\_\_\_\_\_  
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\_\_\_\_\_

4. Record and view data for 40, 50, 60, 70, 80, 90, and 100 nanosecond sample interval

List and Plot Amplitudes for near, mid, and far range bin.

Range Bin \_\_\_\_\_  
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Range Bin \_\_\_\_\_  
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5. Verify proper RPE words

Observed

Data Precision 7 BIT

Sample Interval 100.6 MSEC

Range Delay 1.93 MSEC

Heading \_\_\_\_\_

Temp 1 28.67°C

2 28.82

3 NC

4 20.07

Negative Voltage 5.7 -5.75

*DDPS* <sup>POSITIVE</sup> ~~Negative~~ Voltage 5 +5.04

Negative Voltage 2 -2.08

*AJX* Positive Voltage 5 +4.98

Negative Voltage 15 -15.06

*JTP*





TEST 3. RANGE DELAY TEST

1-30-79

5. Verify proper RPE words.

Observed

Data Precision 7 BIT

Sample Interval 70.4 mSEC

Range Delay 1.93  $\mu$ SEC

Heading \_\_\_\_\_

Temp 1 20.88 °C

2 29.52

3 NC

4 20.28

Negative Volt 5.7 -5.75

*DDRS* <sup>POSITIVE</sup> ~~Negative~~ Volt 5 +5.04

Negative Volt 2 -2.09

*AUX* Positive Volt 5 +4.98

Negative 15 -15.06

*JFP*

1-30-79

TEST 3. RANGE DELAY TEST

1. Set Standard Configuration a. 7 BIT b. 70 mSEC c. \_\_\_\_\_ d. RAMP - 900KHZ

2. Set and Record Identifying word in RPE data

Identifier word set 011

Identifier word observed 011

*JTP*

3. Verify proper range delay using scope.

Selected Range Delay

Observed Range Delay

30  $\mu$  SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

30  $\mu$  SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

4. Record and view data for 2, 30, 60, and 90  $\mu$ sec range delay  
List and Plot Amplitudes for near, mid, and far Range bins.

Range Bin \_\_\_\_\_  
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Range Bin \_\_\_\_\_  
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Range Bin \_\_\_\_\_  
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5. Verify proper RPE words.

Observed

Data Precision 7 BIT

Sample Interval 70.4 mSEC

Range Delay 28.97 μSEC

Heading \_\_\_\_\_

Temp 1 28.70 °C

2 29.43

3 NC

4 20.28

Negative Volt 5.7 -5.75

*DDRS* <sup>POSITIVE</sup>  
~~Negative~~ Volt 5 +5.04

Negative Volt 2 -2.09

*AUX* Positive Volt 5 +4.98

Negative 15 -15.06

*RTP*



TEST 3. RANGE DELAY TEST

1-30-79

JFP

5. Verify proper RPE words.

Observed

Data Precision 7 BIT

Sample Interval 70.4 MSEC

Range Delay 57.95 MSEC

Heading \_\_\_\_\_

Temp 1 28.64°C

2 29.31

3 NC

4 20.28

Negative Volt 5.7 -5.75

DDRS <sup>Positive</sup> ~~Negative~~ Volt 5 +5.04

Negative Volt 2 -2.09

AUX Positive Volt 5 +4.98

Negative 15 -15.06

TEST 3. RANGE DELAY TEST

1-30-79

1. Set Standard Configuration a. 7 BIT b. 70 m SEC c. \_\_\_\_\_ d. RAMP - 900KHZ

2. Set and Record Identifying word in RPE data

Identifier word set \_\_\_\_\_ ~~012~~ 013 \_\_\_\_\_

*STP*

Identifier word observed \_\_\_\_\_ 013 \_\_\_\_\_

3. Verify proper range delay using scope.

Selected Range Delay

Observed Range Delay

90  $\mu$  SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

90  $\mu$  SEC  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

4. Record and view data for 2, 30, 60, and 90  $\mu$ sec range delay  
List and Plot Amplitudes for near, mid, and far Range bins.

Range Bin \_\_\_\_\_  
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Range Bin \_\_\_\_\_  
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TEST 3. RANGE DELAY TEST

1-30-79

5. Verify proper RPE words.

Observed

Data Precision 7BIT

Sample Interval 70.4 m SEC

Range Delay 86.93  $\mu$ SEC

Heading \_\_\_\_\_

Temp 1 28.91°C

2 29.61

3 NC

4 20.34

Negative Volt 5.7 -5.75

*DDRS* <sup>POSITIVE</sup>  
~~Negative~~ Volt 5 +5.04

Negative Volt 2 -2.07

*AUX* Positive Volt 5 +4.98

Negative 15 -15.06

*270*



TEST 4. BAND WIDTH

1-30-79

1. Standard Configuration a. 7 BIT b. 70 nSEC c. 2 MSFC d. SINE WAVE
  2. Using dc input observed and record DDRS output amplitude on scope 4.3 V P-P
  3. Using 7.5 MHz sine wave input observe and record DDRS output amplitude on scope 4.2 V P-P
  4. Using 15 MHz sine wave input observe and record DDRS output on scope 3.8 V P-P
- ! The dc and 15 MHz values should be within 3 dB of 7.5 MHz value.

*JTP*

17 MHz - 3.7 V P-P  
 12.5 MHz - 4.0 V P-P  
 10 MHz - 4.1 V P-P  
 5 MHz - 4.2 V P-P  
 2.5 MHz - 4.2 V P-P  
 1 MHz - 4.3 V P-P  
 50 KHz - 4.4 V P-P

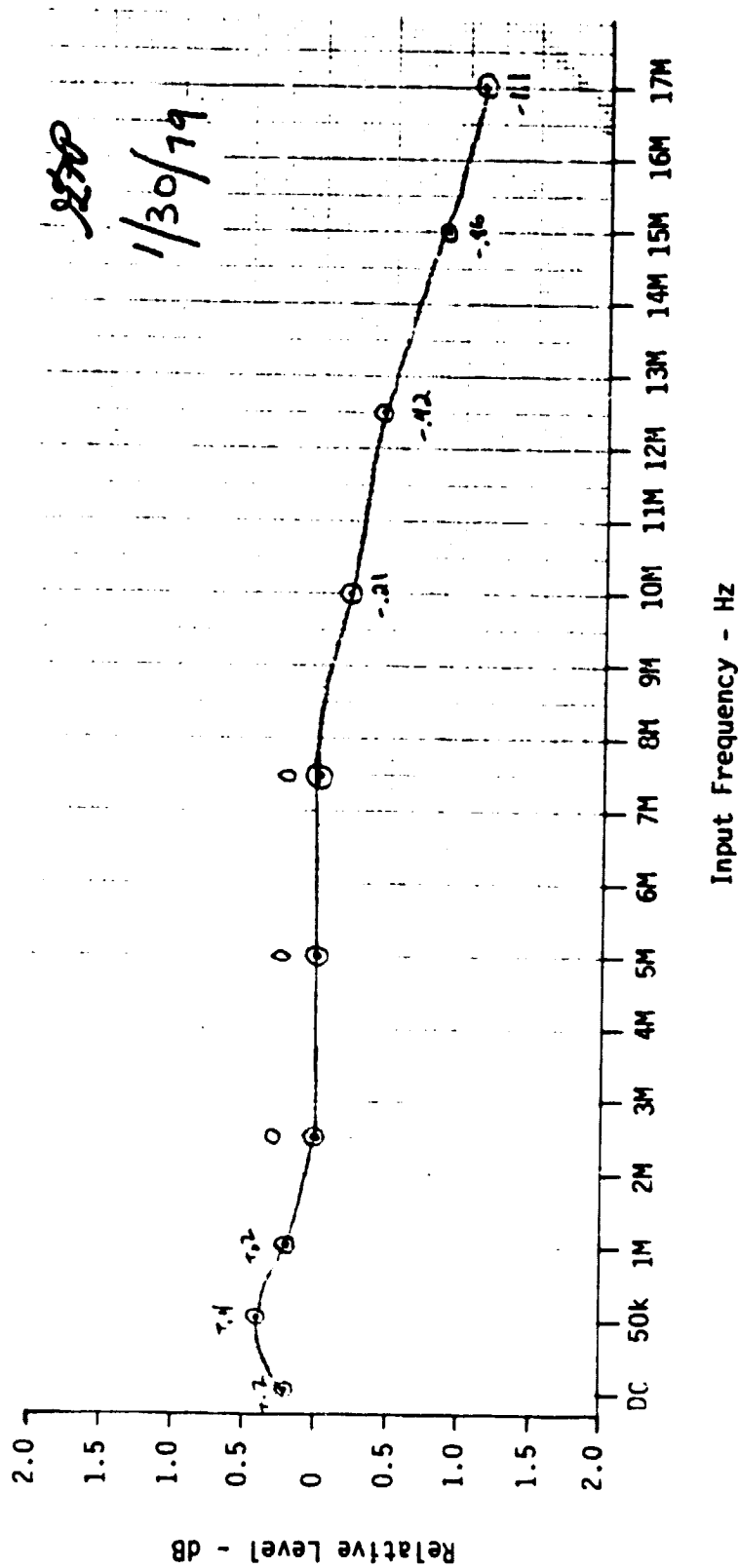


FIGURE B-4  
DDRS FREQUENCY RESPONSE

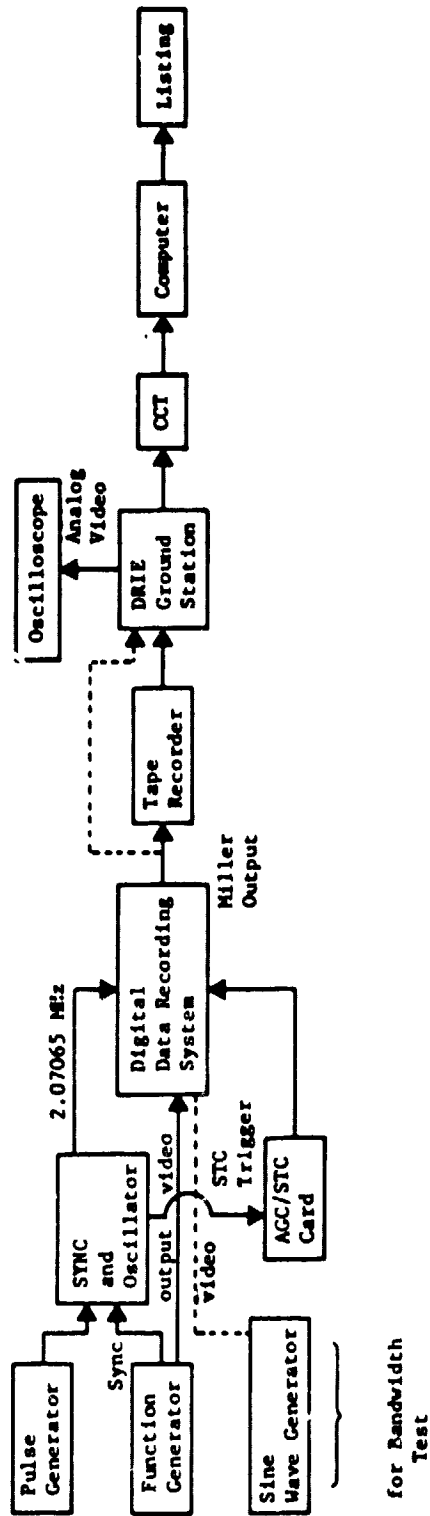


FIGURE B-5  
DORS ACCEPTANCE PROCEDURE BLOCK DIAGRAM

AE-80-114

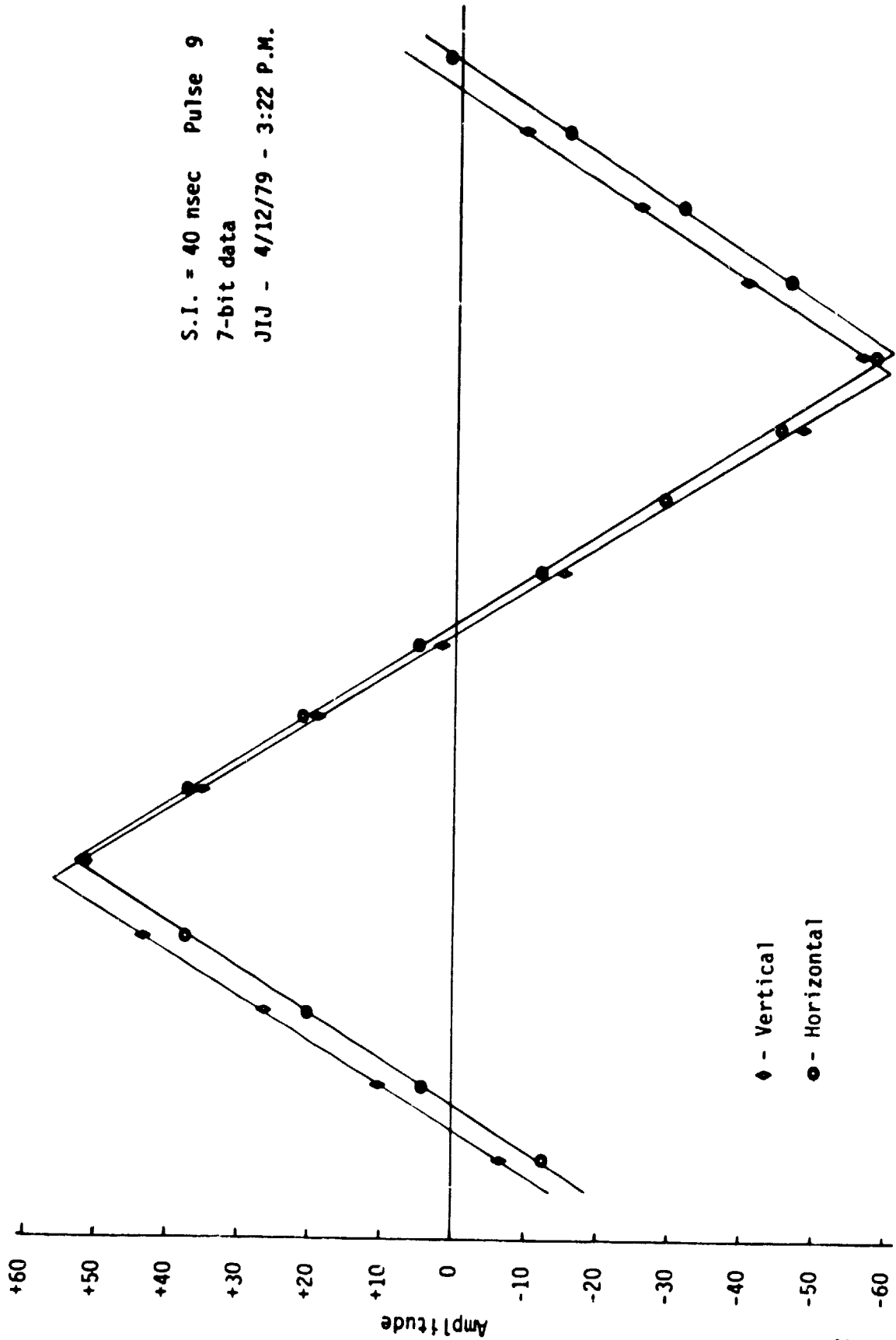


FIGURE B-6  
DIGITAL RESPONSE OF DDRS TO TRIANGULAR WAVE FORM INPUT  
(FINAL TEST OF DDRS)

APPENDIX C  
CONTROL VALIDATION PROMS

PRECEDING PAGE BLANK NOT FILMED

**TABLE C-1**  
**VALID CONTROL SETTINGS**

MODE	1	DELAYS	02	-	48	SI	040	DP	7
MODE	2	DELAYS	02	-	79	SI	040	DP	7
MODE	1	DELAYS	02	-	21	SI	040	DP	4
MODE	2	DELAYS	02	-	58	SI	040	DP	4
MODE	1	DELAYS	02	-	02	SI	040	DP	2
MODE	2	DELAYS	02	-	17	SI	040	DP	2
MODE	1	DELAYS	02	-	02	SI	040	DP	1
MODE	2	DELAYS	02	-	02	SI	040	DP	1
MODE	1	DELAYS	02	-	44	SI	050	DP	7
MODE	2	DELAYS	02	-	74	SI	050	DP	7
MODE	1	DELAYS	02	-	18	SI	050	DP	4
MODE	2	DELAYS	02	-	49	SI	050	DP	4
MODE	1	DELAYS	02	-	02	SI	050	DP	2
MODE	2	DELAYS	02	-	02	SI	050	DP	2
MODE	1	DELAYS	02	-	38	SI	060	DP	7
MODE	2	DELAYS	02	-	68	SI	060	DP	7
MODE	1	DELAYS	02	-	07	SI	060	DP	4
MODE	2	DELAYS	02	-	38	SI	060	DP	4
MODE	1	DELAYS	02	-	02	SI	060	DP	2
MODE	2	DELAYS	02	-	02	SI	060	DP	2
MODE	1	DELAYS	02	-	33	SI	070	DP	7
MODE	2	DELAYS	02	-	63	SI	070	DP	7
MODE	1	DELAYS	02	-	02	SI	070	DP	4
MODE	2	DELAYS	02	-	27	SI	070	DP	4
MODE	1	DELAYS	02	-	02	SI	070	DP	2
MODE	2	DELAYS	02	-	02	SI	070	DP	2
MODE	1	DELAYS	02	-	28	SI	080	DP	7
MODE	2	DELAYS	02	-	58	SI	080	DP	7
MODE	1	DELAYS	02	-	02	SI	080	DP	4
MODE	2	DELAYS	02	-	17	SI	080	DP	4
MODE	1	DELAYS	02	-	02	SI	080	DP	2
MODE	2	DELAYS	02	-	02	SI	080	DP	2
MODE	1	DELAYS	02	-	23	SI	090	DP	7
MODE	2	DELAYS	02	-	53	SI	090	DP	7
MODE	1	DELAYS	02	-	02	SI	090	DP	4
MODE	2	DELAYS	02	-	07	SI	090	DP	4
MODE	1	DELAYS	02	-	02	SI	090	DP	2
MODE	2	DELAYS	02	-	02	SI	090	DP	2
MODE	1	DELAYS	02	-	18	SI	100	DP	7
MODE	2	DELAYS	02	-	48	SI	100	DP	7
MODE	1	DELAYS	02	-	02	SI	100	DP	4
MODE	2	DELAYS	02	-	02	SI	100	DP	4
MODE	1	DELAYS	02	-	13	SI	110	DP	7
MODE	2	DELAYS	02	-	43	SI	110	DP	7
MODE	1	DELAYS	02	-	02	SI	110	DP	4
MODE	2	DELAYS	02	-	02	SI	110	DP	4
MODE	1	DELAYS	02	-	08	SI	120	DP	7
MODE	2	DELAYS	02	-	38	SI	120	DP	7
MODE	1	DELAYS	02	-	02	SI	120	DP	4
MODE	2	DELAYS	02	-	02	SI	120	DP	4
MODE	1	DELAYS	02	-	02	SI	130	DP	7
MODE	2	DELAYS	02	-	33	SI	130	DP	7
MODE	1	DELAYS	02	-	02	SI	130	DP	4
MODE	2	DELAYS	02	-	02	SI	130	DP	4
MODE	1	DELAYS	02	-	02	SI	140	DP	7
MODE	2	DELAYS	02	-	28	SI	140	DP	7
MODE	1	DELAYS	02	-	02	SI	140	DP	4
MODE	2	DELAYS	02	-	02	SI	140	DP	4
MODE	1	DELAYS	02	-	02	SI	150	DP	7
MODE	2	DELAYS	02	-	23	SI	150	DP	7
MODE	1	DELAYS	02	-	02	SI	150	DP	4
MODE	2	DELAYS	02	-	02	SI	150	DP	4
MODE									

**TABLE C-2  
BIT PATTERN PRINTOUT**

CONTROL VALIDATION FROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	77	77	77	77	77	77	77	77	77	77	77	77	77	77	77	77
0010	77	77	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0020	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	F7
0030	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7
0040	F7	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0050	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0060	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0070	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
0080	57	57	57	57	57	57	57	57	57	57	57	57	57	57	57	57
0090	56	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7
00A0	D7	D7	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6
00B0	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6
00C0	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6
00D0	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7	B7
00E0	75	75	75	75	75	75	75	75	75	75	75	75	75	75	75	75
00F0	74	74	74	74	74	74	74	74	74	74	74	74	74	74	74	74
0100	74	74	74	74	74	74	74	74	F5	F5	F5	F5	F5	F5	F5	F5
0110	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5	F5
0120	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4
0130	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4
0140	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4
0150	F4	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0160	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55	55
0170	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5
0180	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4
0190	D4	35	35	35	35	35	35	35	35	35	35	35	35	35	35	35
01A0	73	73	73	73	73	73	73	73	73	73	73	73	73	73	73	73
01B0	72	72	72	72	72	72	72	72	72	72	72	72	72	72	72	72
01C0	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3
01D0	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2
01E0	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2
01F0	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2
																53



TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0200	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3
0210	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3
0220	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2
0230	71	71	71	71	71	71	71	71	71	71	71	71	71	71	71	71
0240	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70	70
0250	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1
0260	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
0270	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
0280	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0	F0
0290	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1
02A0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0	D0
02B0	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F	6F
02C0	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E
02D0	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E
02E0	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E
02F0	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E	6E
0300	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D
0310	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D
0320	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D
0330	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D
0340	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D
0350	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D	6D
0360	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B
0370	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B	6B
0380	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A
0390	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A	6A
03A0	69	69	69	69	69	69	69	69	69	69	69	69	69	69	69	69
03B0	69	69	69	69	69	69	69	69	69	69	69	69	69	69	69	69
03C0	68	68	68	68	68	68	68	68	68	68	68	68	68	68	68	68
03D0	68	68	68	68	68	68	68	68	68	68	68	68	68	68	68	68
03E0	67	67	67	67	67	67	67	67	67	67	67	67	67	67	67	67
03F0	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66	66



TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0400	E6	E6	E6	47	C7	65	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5
0410	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5
0420	E4	E4	E4	E4	E4	E4	C5	C5	C5	E3	E3	E3	E3	E3	E3	E3
0430	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3
0440	E2	E2	E2	E2	43	C3	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1
0450	E1	E1	E1	E1	E1	E1	E1	E1	E1	E0	E0	E0	E0	41	C1	FF
0460	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0470	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0480	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0490	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0500	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0510	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0520	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0530	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0540	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0550	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0560	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0570	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0580	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0590	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U31

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0600	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0610	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0620	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0630	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0640	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0650	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0660	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0670	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0680	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0690	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0700	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0710	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0720	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0730	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0740	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0750	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0760	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0770	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0780	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0790	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0600	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0610	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0620	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0630	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0640	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0650	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0660	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0670	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0680	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0690	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
06F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0700	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0710	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0720	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0730	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0740	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0750	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0760	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0770	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0780	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0790	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
07F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF



TABLE C-2 CONT'D

CONTROL VALIDATION FROM 4U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0400	03	02	01	07	27	37	27	26	20	24	23	22	21	20	11	10	
0410	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	
0420	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0	F0	E7	E6	E5	
0430	20	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	
0440	E4	E3	E2	E1	E0	D7	D6	D5	D4	D3	D2	D1	D0	F0	E7	E6	E5
0450	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2
0460	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0470	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0480	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0490	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
04F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0500	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0510	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0520	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0530	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0540	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0550	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0560	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0570	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0580	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
0590	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05A0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05B0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05D0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
05F0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E
0200	22	27	26	25	24	23	22	21	20	11	10	07	06	05	04
0210	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0
0220	C6	C5	C4	C3	C2	C1	27	27	27	26	25	24	23	22	21
0230	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5
0240	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1	E6	E5
0250	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5
0260	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2	C1	E6	E5
0270	A7	A6	A5	A4	A3	A2	A1	A0	91	90	87	86	85	84	83
0280	81	80	71	70	67	66	27	27	26	25	24	23	22	21	20
0290	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
02A0	E2	27	27	27	26	25	24	23	22	21	20	11	10	07	06
02B0	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	27
02C0	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01
02D0	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5
02E0	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	91
02F0	87	86	85	84	83	82	81	27	27	26	25	24	23	22	21
0300	11	10	07	06	05	04	03	02	01	00	27	26	25	24	23
0310	21	20	11	10	07	06	05	04	03	02	01	00	F1	F0	E7
0320	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03
0330	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7
0340	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1
0350	91	90	87	86	85	84	83	27	27	26	25	24	23	22	21
0360	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00
0370	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01
0380	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5
0390	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	91
03A0	26	25	24	23	22	21	20	11	10	07	06	05	04	03	02
03B0	22	21	20	11	10	07	06	05	04	03	02	01	00	F1	F0
03C0	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3	C2
03D0	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	91	90	87	86
03E0	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01
03F0	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5



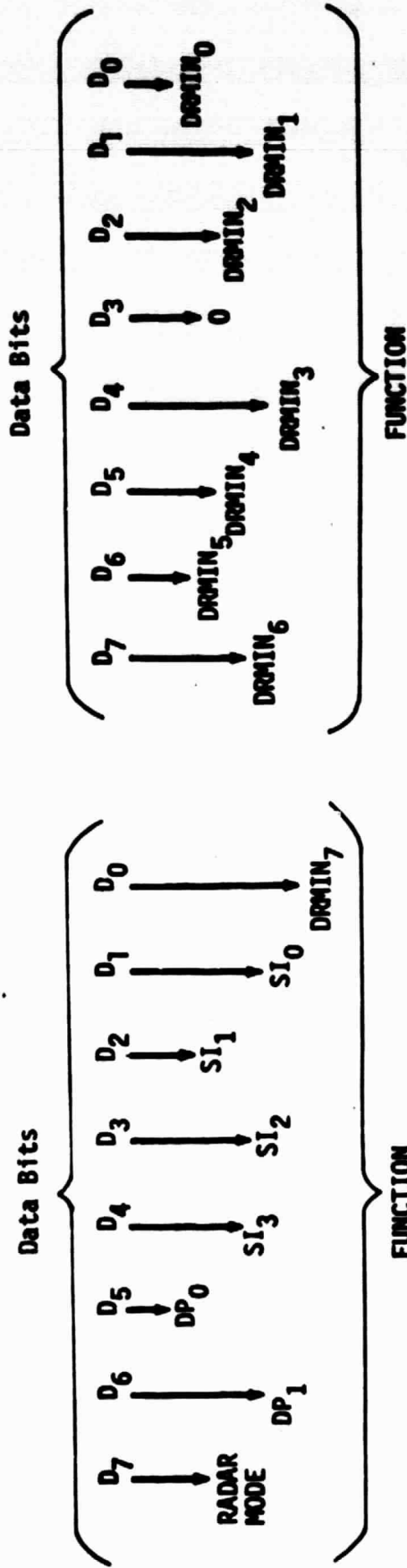
TABLE C-2 CONT'D

CONTROL VALIDATION FROM #U44

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12
0010	01	00	51	F0	E7	E6	E5	E4	E3	E2	E1	F0	D1	D0	C7	C6
0020	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	27
0030	26	25	24	23	22	21	20	11	10	07	06	05	04	03	02	01
0040	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5
0050	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	91
0060	90	87	86	85	84	83	82	81	80	71	70	67	66	65	64	63
0070	62	61	60	51	50	47	46	45	44	43	42	41	40	27	26	25
0080	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00	F1
0090	F0	F0	26	25	24	23	22	21	20	11	10	07	06	05	04	03
00A0	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7
00B0	C5	C5	C4	C3	C2	C1	C0	B1	B0	A7	A6	A5	A4	A3	A2	A1
00C0	AC	91	90	87	86	85	84	83	82	81	27	27	26	25	24	23
00D0	22	21	20	11	10	07	06	05	04	03	02	27	27	26	25	25
00E0	24	23	22	21	20	11	10	07	06	05	04	03	02	01	00	F1
00F0	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0	C7	C6	C5	C4	C3
0100	02	01	00	B1	B0	A7	A6	A5	27	26	25	24	23	22	21	20
0110	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
0120	05	04	03	F0	E1	D0	C7	C6	C5	C4	C3	C2	C1	C0	B1	B0
0130	A7	A6	A5	A4	A3	A2	A1	A0	91	90	87	86	85	84	83	82
0140	81	80	71	70	67	66	65	64	63	62	61	60	51	50	47	46
0150	45	27	26	25	24	23	22	21	20	11	10	07	06	05	04	03
0160	02	01	00	26	25	24	23	22	21	20	11	10	07	06	05	04
0170	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1	D0
0180	07	06	05	04	03	02	01	00	B1	B0	A7	A6	A5	A4	A3	A2
0190	01	00	27	26	25	24	23	22	21	20	11	10	07	06	05	04
01A0	04	03	02	01	00	F1	F0	E7	E6	E5	E4	E3	E2	E1	E0	D1
01B0	D0	D0	C6	C5	C4	C3	C2	C1	27	26	25	24	23	22	21	20
01C0	11	10	07	06	05	04	03	02	01	00	F1	F0	E7	E6	E5	E4
01D0	03	02	01	00	D1	D0	C7	C6	C5	C4	C3	C2	C1	C0	B1	B0
01E0	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
01F0	81	80	71	70	67	66	65	64	63	62	61	60	51	50	47	46

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TABLE C-3  
CONTROL VALIDATION PROMS BIT ASSIGNMENTS



DRMIN<sub>7</sub> - DRMIN<sub>0</sub> -- 8-bit value for ARMIN - coded in 9's complement of BCD (2 digits)  
 MSB                      LSB                      LSB = 1 μsec (e.g., 10010000 = 9 μsec)

SI<sub>3</sub> - SI<sub>0</sub> -- 4-bit value for sample interval - coded in complement binary  
 MSB                      LSB                      LSB = 10 nsec (e.g., 1011 = 40 nsec)

DP <sub>1</sub>	DP <sub>0</sub>	
0	0	1-bit data
0	1	2-bit data
1	0	4-bit data
1	1	7-bit data

RADAR MODE - 0 = Mode 1  
 1 = Mode 2

**APPENDIX D**

**MANUFACTURER'S DATA SHEETS**

- 1. ECL COMPONENT DATA**
- 2. TTL COMPONENT DATA**
- 3. ANALOG AND DATA CONVERSION COMPONENT DATA**

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**1. ECL COMPONENT DATA**

# F10K VOLTAGE COMPENSATED ECL SERIES

**GENERAL DESCRIPTION** — Fairchild F10K Series Emitter Coupled Logic (ECL) circuits are high speed, low power logic elements intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communication systems.

F10,000 ECL is designed to be fully compatible with conventional 10,000 ECL and has the same part numbers, functions, pinouts, temperature behavior, test methods, propagation delay limits and signal voltages.

F10K circuits employ Emitter Coupled Logic to achieve typical power levels of 25 mW/gate. The nominal power supply is specified as  $V_{EE}$  equal to -5.2 V. All devices, however, may be operated over  $V_{EE}$  ranges of -4.7 to -6.2 V with negligible loss of noise immunity. Some SSI gates may be operated over a  $V_{EE}$  range of -3.5 to -6.2 V, again with a negligible loss of noise immunity, due to the built-in voltage regulator.

In accordance with standard IC practice, F10K devices are specified over 0°C to +75°C temperature range. However, limits ensure that the F10K series is fully compatible with other 10,000 devices specified over a -30°C to +85°C ambient temperature range.

High input impedance (typically 50 k $\Omega$ ) and open outputs allow effective usage of series or parallel terminated line techniques and large numbers of OR-ties.

- Very high speed . . . typically 2 ns per gate.
- Low power dissipation . . . typically 25 mW per gate.
- Voltage compensated . . . noise margin insensitive to power supply variations and transients, relaxed power supply requirements.

- Internal 50 k $\Omega$  (nominal) input pull down resistors . . . unused inputs may be left open.
- Open emitter-follower outputs drive terminated lines.
- Separate  $V_{CC}$  leads eliminate noise coupling.
- Single  $V_{EE}$  power supply . . . -4.7 to -6.2 V.
- Wired-OR capability.
- Complementary, simultaneous outputs.
- Fully compatible with other 10,000 series ECL.

## RECOMMENDED OPERATING AND TEST CONDITIONS

— The Fairchild F10K series is designed to operate in a system whose ambient temperature is controlled by moving air or equivalent means. The ambient temperature may be any value between 0°C and +75°C, but the temperature gradient between the devices must be at a minimum to conserve noise immunity. The Fairchild F10K devices are designed to meet the specified dc characteristics when a thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50  $\Omega$  resistor to -2.0 V.

The Fairchild F10K series operates with a system power supply  $V_{EE}$  between -4.7 and -6.2 V. Detailed test specifications are for nominal  $V_{EE} = -5.2$  V.

## ABSOLUTE MAXIMUM RATINGS

(Non-operating, above which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Supply Voltage $V_{EE}$ (Continuous)	-8 V
Input Voltage	Gnd to $V_{EE}$
Output Current	-50 mA

**FUNCTIONAL DESCRIPTION**

F10K offers many high speed system design advantages. High speed is achieved by using small, low capacitance device geometries and operating the transistors between the active and off modes, thereby avoiding saturation. The basic ECL gate is shown in *Figure 1*.

If the input voltages are more negative than  $V_{gg}$ , Q1 and Q2 are cut off and Q3 conducts, holding the collector of Q3 LOW. If either input is more positive than  $V_{gg}$ , Q1 or Q2 will conduct and Q3 will be cut off, raising its collector voltage. Since one or more transistors are always conducting, there is a constant current drain, independent of frequency which eliminates sharp switching transients and frequency dependent power dissipation effects. The outputs of the circuit are emitter-followers, Q4 and Q5. They provide low impedance drive to terminated lines and voltage shifting to levels compatible with the inputs. The basic gate simultaneously performs the positive logic OR and NOR functions, providing both true and complement outputs within a single gate delay period. The outputs of several gates may be tied to provide a wired-OR function. An external load resistor must be provided in all cases.

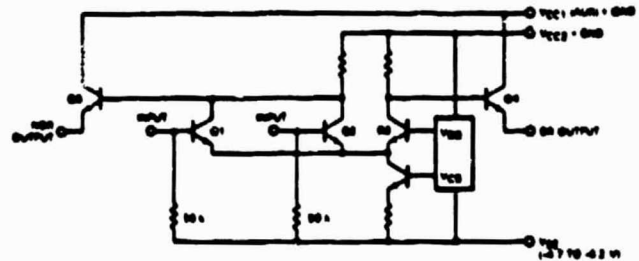


Fig. 1.

**TYPICAL ECL TRANSFER CHARACTERISTICS WITH SPECIFICATION POINTS**

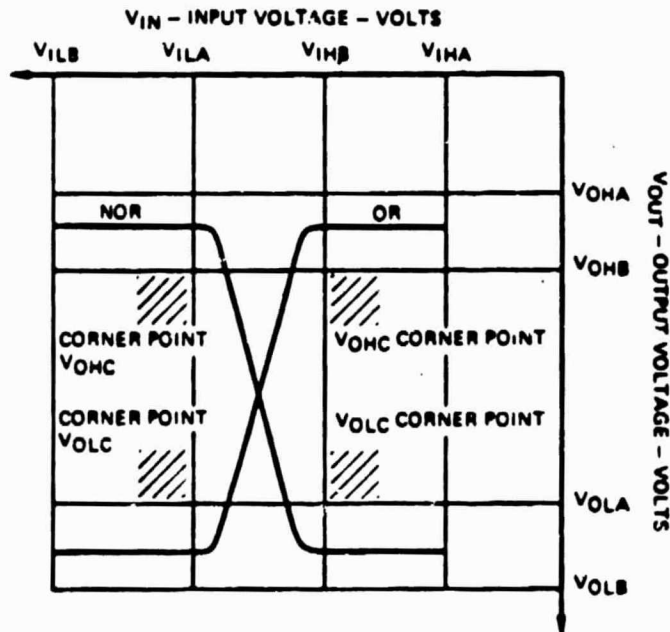
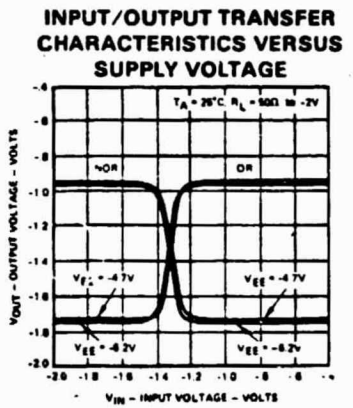
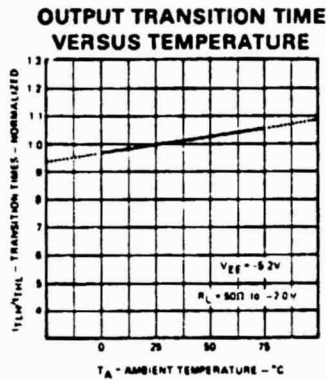
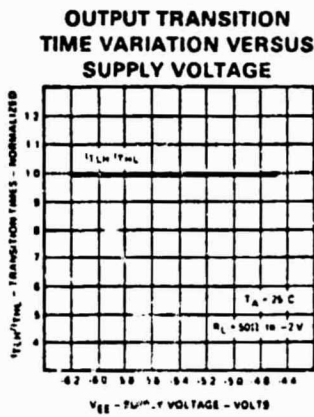
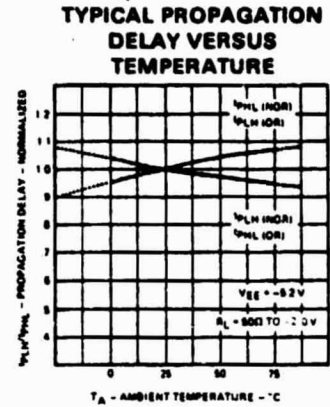
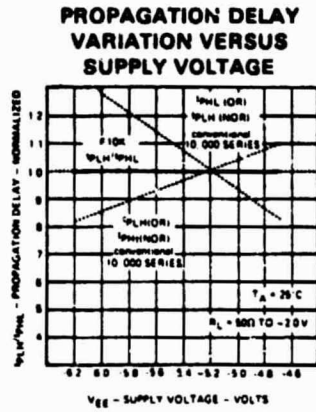
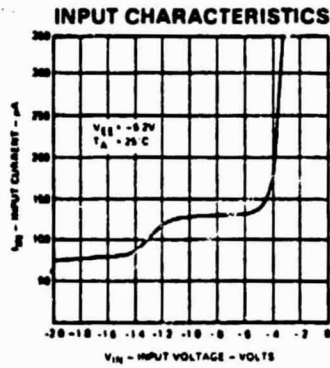
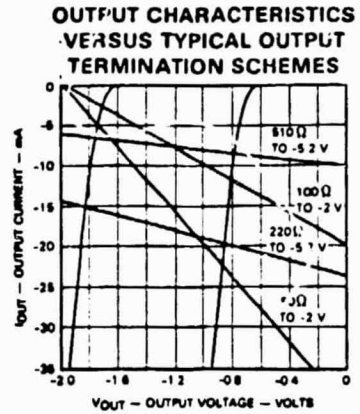
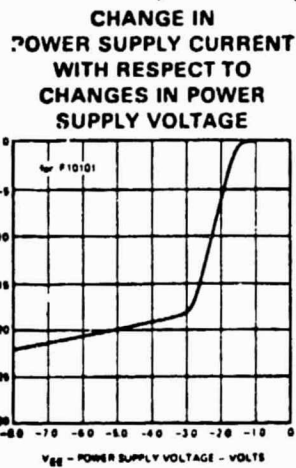
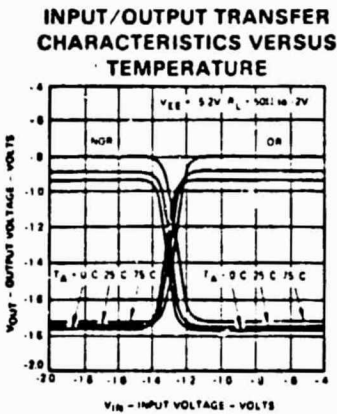


Fig. 2.

TYPICAL F10K SERIES CHARACTERISTICS

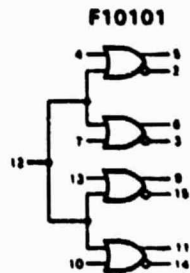


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# FAIRCHILD ECL DATA SHEET • F10K SERIES

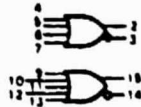
**LOGIC DIAGRAMS**  $V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8$



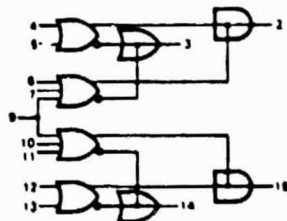
**F10105**



**F10109**



**F10117**

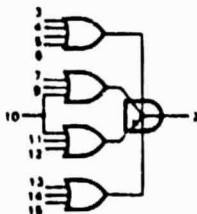


Logic Equation

$$2 = (4 \cdot 5) (6 \cdot 7 \cdot 9)$$

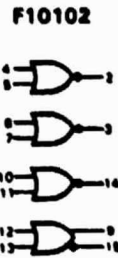
$$3 = \frac{(4 \cdot 5) (6 \cdot 7 \cdot 9)}{(4 \cdot 5) (6 \cdot 7 \cdot 9)}$$

**F10119**

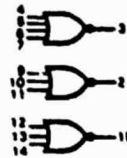


Logic Equation

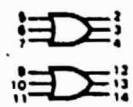
$$2 = (3 \cdot 4 \cdot 5 \cdot 6) (7 \cdot 9 \cdot 10) (10 \cdot 11 \cdot 12) (13 \cdot 14 \cdot 15);$$



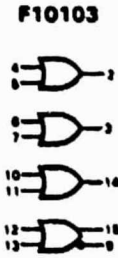
**F10106**



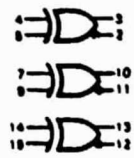
**F10110**



NOTE  $V_{CC1} = 1$   
 $V_{CC2} = 16$



**F10107**



Logic Equation

$$2 = 4 \cdot \bar{5} \cdot \bar{4} \cdot 5$$

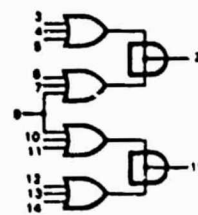
$$3 = 4 \cdot 5 \cdot \bar{4} \cdot \bar{5}$$

**F10111**



NOTE  $V_{CC1} = 1$   
 $V_{CC2} = 16$

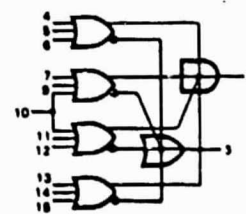
**F10118**



Logic Equation

$$2 = (3 \cdot 4 \cdot 5) (6 \cdot 7 \cdot 9)$$

**F10121**



Logic Equation

$$2 = (4 \cdot 5 \cdot 6) (7 \cdot 9 \cdot 10) (10 \cdot 11 \cdot 12) (13 \cdot 14 \cdot 15)$$

$$3 = \frac{(4 \cdot 5 \cdot 6) (7 \cdot 9 \cdot 10) (10 \cdot 11 \cdot 12) (13 \cdot 14 \cdot 15)}{(4 \cdot 5 \cdot 6) (7 \cdot 9 \cdot 10) (10 \cdot 11 \cdot 12) (13 \cdot 14 \cdot 15)}$$

DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$  F10101 • F10102 • F10103 • F10105 • F10106  
F10107 • F10109 • F10110 • F10111

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$V_{OH}$	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Logic Function  Loading is 50Ω to -2.0 V
$V_{OL}$	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C	
$V_{OHC}$	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	
$V_{OLC}$	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C	
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
$I_{IH}$	Input Current HIGH F10101 Lead 12 F10107 Leads 5,7,15 F10110 All Inputs F10111 All Inputs			265 550 220 435 435	μA	25°C	$V_{IN} = V_{IHA}$
$I_{IL}$	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$
$I_{EE}$	Power Supply Current	F10101 F10102 F10103 F10105 F10106 F10107 F10109 F10110 F10111	-26 -26 -26 -21 -21 -28 -14 -38 -38	-20 -20 -20 -15 -15 -22 -10 -28 -28		mA 25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$  F10101 • F10102 • F10103 • F10105 • F10106 • F10109

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.0	2.0	2.9	ns	
$t_{PHL}$	Propagation Delay, HIGH to LOW	1.0	2.0	2.9	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.3	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.3	ns	

FAIRCHILD ECL DATA SHEET • F10K SERIES

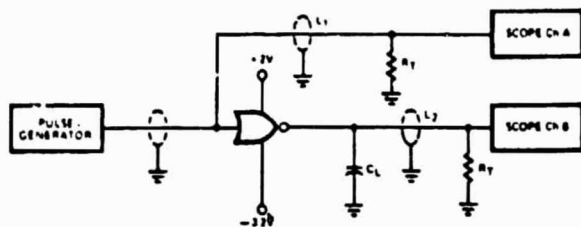
SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$  F10107

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.1	2.4	3.7	ns	See Figure 1
$t_{PHL}$	Propagation Delay, HIGH to LOW	1.1	2.4	3.7	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.5	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.5	ns	

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$  F10110 • F10111

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.4	2.4	3.5	ns	See Figure 1
$t_{PHL}$	Propagation Delay, HIGH to LOW	1.4	2.4	3.5	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	3.5	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	3.5	ns	

SWITCHING CIRCUIT AND WAVEFORMS



$L_1$  and  $L_2$  = equal length  $50 \Omega$  impedance lines  
 $R_T$  =  $50 \Omega$  termination of scope  
 $C_L$  = Jig and stray capacitance  $< 50 \text{ pF}$   
 Decoupling  $0.1 \mu\text{F}$  from gnd to  $V_{EE}$  and  $V_{CC}$



Jig set-up with no circuit under test  
 $V_{CC1} = V_{CC2} = +2.0 \text{ V}$   
 $V_{EE} = -3.2 \text{ V}$



# F10010 • F10016

## BCD DECADE COUNTER, 4-BIT BINARY COUNTER

**GENERAL DESCRIPTION** — The F10010 is a high speed synchronous, presettable, cascadable BCD Decade Counter and the F10016 is a high speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 10K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

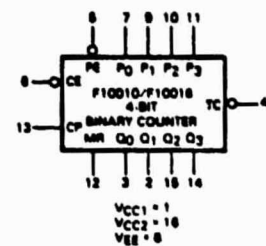
Both devices are packaged in hermetic ceramic 16-lead Dual In-Line packages and are specified for operation over the temperature range 0°C to 75°C.

- HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY
- INTERNAL COUNT ENABLE — FOR HIGHEST SPEED EXPANSION
- ASYNCHRONOUS MASTER RESET
- 50 Ω DRIVE CAPABILITY
- WIRED-OR CAPABILITY
- SEPARATE V<sub>CC</sub> LEADS — ELIMINATE NOISE COUPLING
- INTERNAL 50 k Ω INPUT PULL DOWNS
- SINGLE -5.2 V POWER SUPPLY

### LEAD NAMES

PE	Parallel Load Enable (Active LOW)
P <sub>n</sub>	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
CE	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
TC	Terminal Count (10010, LOW at HLLH; 10016 LOW at HHHH)
Q <sub>n</sub>	Counter Outputs

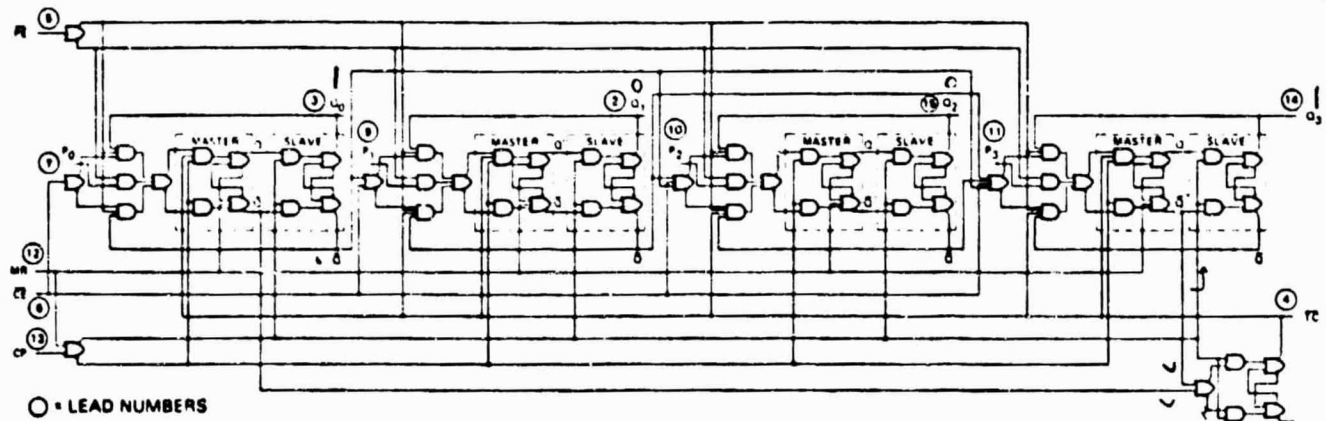
### LOGIC SYMBOL



### CONNECTION DIAGRAM DIP (TOP VIEW)



### LOGIC DIAGRAM F10010

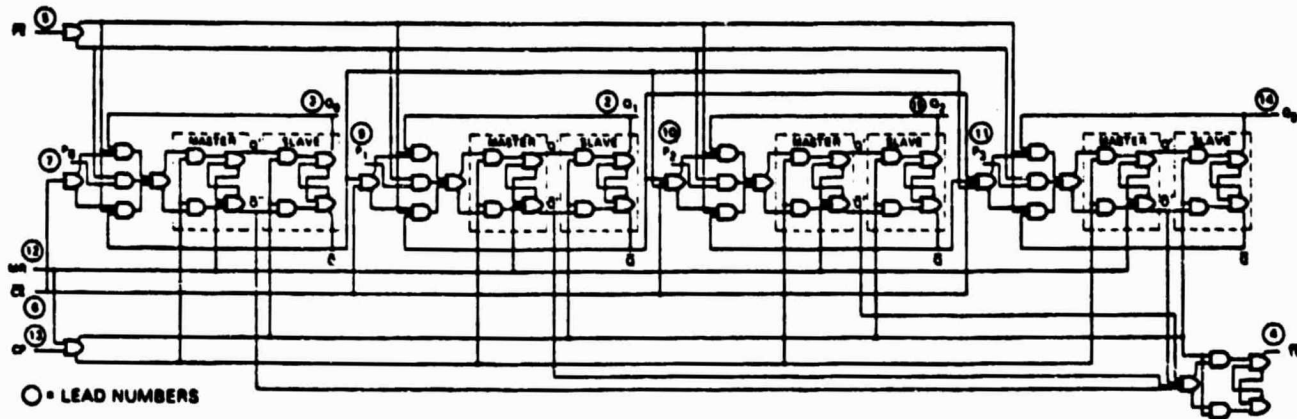


Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.



# FAIRCHILD ECL DATA SHEET • F10010 • F10016

## LOGIC DIAGRAM F10016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

**FUNCTIONAL DESCRIPTION** — The F10010 is a high speed BCD Decade Counter and the F10016 is a high speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ( $\overline{TC}$ ) is generated at count 9 (HLLH) on the 10010 and at count 15 (HMH) on the 10016.

The  $\overline{TC}$  output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ( $\overline{CE}$ ) and the Parallel Enable ( $\overline{PE}$ ) select the mode of operation as shown in the table below. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

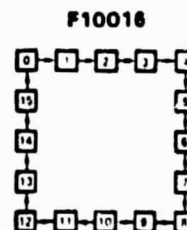
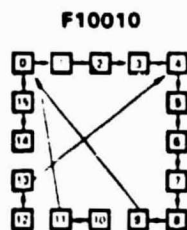
The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the  $\overline{TC}$  HIGH.

### TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	$\downarrow$	Load Parallel ( $P_n$ to $Q_n$ )
H	L	L	$\downarrow$	Load Parallel ( $P_n$ to $Q_n$ )
L	H	L	$\downarrow$	Count
H	H	L	$\downarrow$	Hold
X	X	L	$\downarrow$	Masters Respond; Slaves Hold
X	X	H	X	Reset ( $Q_n = \text{LOW}$ , $\overline{TC} = \text{HIGH}$ )

L = LOW  
 H = HIGH Voltage Level  
 X = Don't Care  
 $\downarrow$  = Clock Pulse (LOW to HIGH)  
 $\uparrow$  = Clock Pulse (HIGH to LOW)

### STATE DIAGRAMS



**NOTE** The 10010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

**FAIRCHILD ECL DATA SHEET • F10010 • F10016**

**DC CHARACTERISTICS:  $V_{EE} = -5.2$  V,  $V_{CC} = \text{GND}$**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS	
		B	TYP	A				
$V_{OH}$	Output Voltage HIGH	-1000 -990 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table	Loading is 50Ω to -2.0 V
$V_{OL}$	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C		
$V_{OHC}$	Output Voltage HIGH	-1020 -990 -920			mV	0°C 25°C 75°C		
$V_{OLC}$	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C		
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs	
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs	
$I_{IH}$	Input Current HIGH MR (Lead 12)			265 700	μA	25°C	$V_{IN} = V_{IHA}$	
$I_{IL}$	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
$I_{EE}$	Power Supply Current	-115	-80		mA	25°C	Outputs Open, Lead 12 Tied to $V_{IH}$	

**SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2$  V,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND}$**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$f_{\text{count}}$	Count Frequency	140	200		MHz	See Figure 1
$t_{PLH}$	Propagation Delay Clock to Output ( $Q_n$ or $\overline{TC}$ )	2.0	3.6	5.0	ns	See Figure 2
$t_{PHL}$	Propagation Delay Clock to Output ( $Q_n$ or $\overline{TC}$ )	2.0	3.6	5.0	ns	
$t_{PHL}$	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
$t_w$	Clock Pulse Width		2.3		ns	See Figure 2
$t_w$	MR Pulse Width		2.8		ns	See Figure 3
$t_s$	Set-Up Time Prior to Clock $P_n$ to CP	2.0			ns	
$t_h$	Hold Time After Clock $P_n$ to CP	1.0			ns	
$t_s$	Set-Up Time Prior to Clock PE or CE to CP	2.5			ns	
$t_h$	Hold Time After Clock	0.5			ns	

## SWITCHING CIRCUITS AND WAVEFORMS

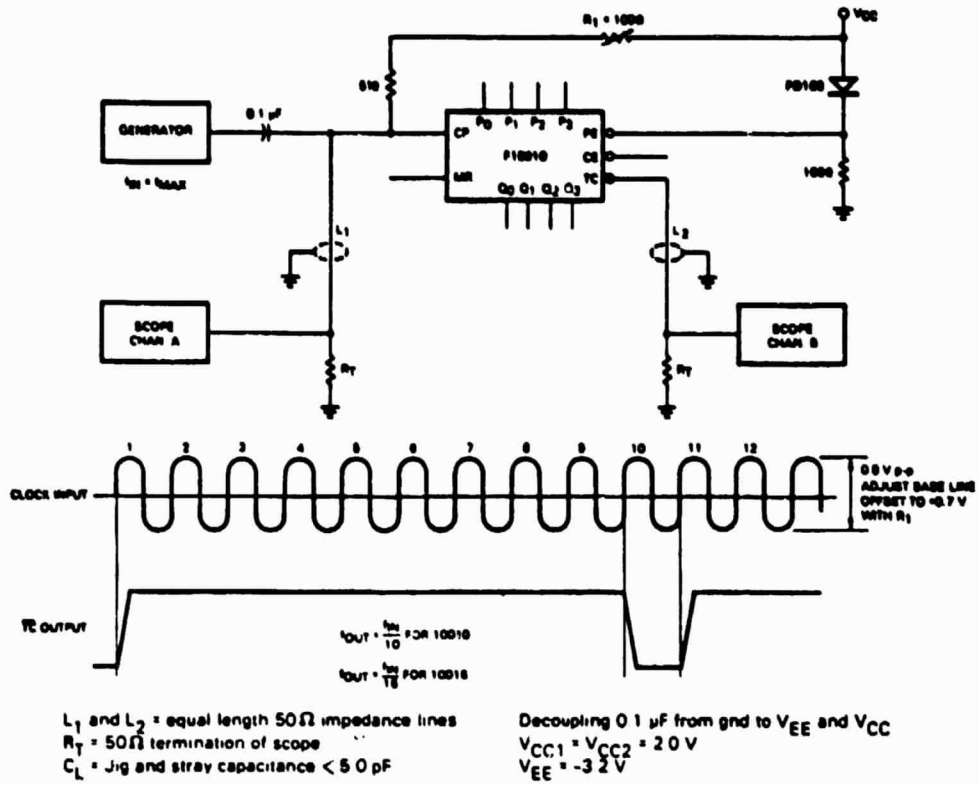
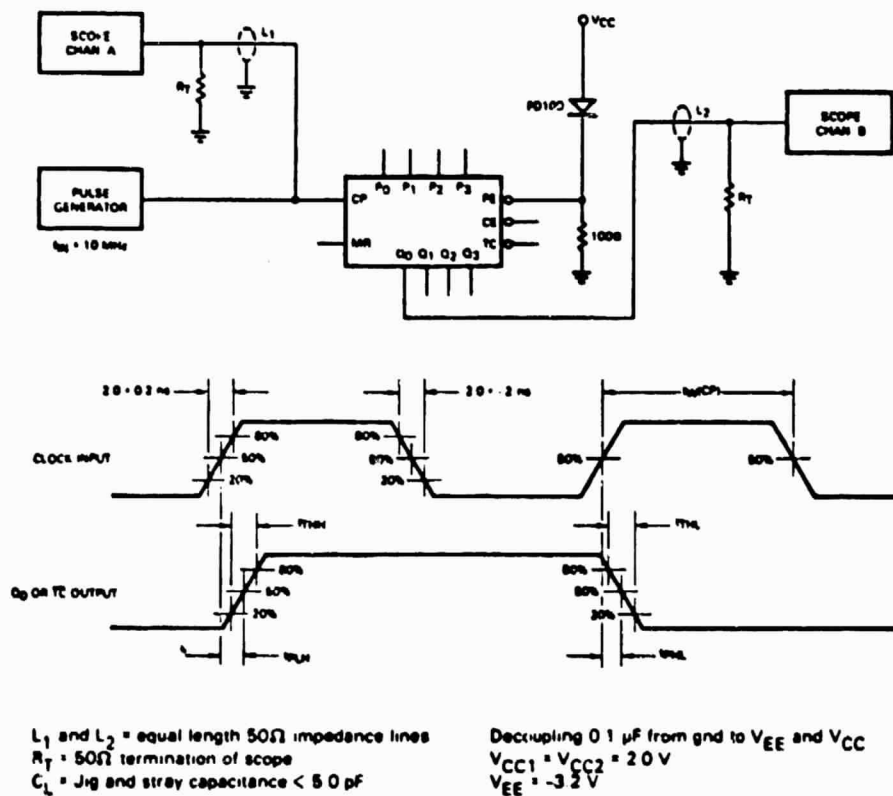


Fig. 1. Maximum Count Frequency



# F10115 • F10116

## LINE RECEIVERS

**DESCRIPTION** — The F10115 and F10116 are differential amplifiers with low impedance emitter-follower outputs. An internal reference supply ( $V_{BB}$ ) is available for added versatility. Active current sources provide improved common mode rejection. The F10115 is a quad line receiver with single ended outputs. The F10116 is a triple line receiver with complementary outputs. The devices are voltage compensated and are fully compatible with other 10,000 series devices. The line receivers are used primarily to receive data from balanced twisted pair lines, however, with appropriate connections and feedback, they may operate as Schmitt triggers, high speed comparators, oscillators, or broadband amplifiers.

### TRUTH TABLES

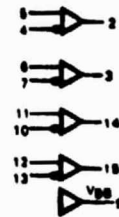
F10115 Quad Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	$V_{BB}$	L
H	$V_{BB}$	H
$V_{BB}$	H	L
$V_{BB}$	L	H

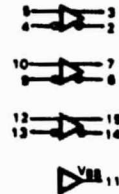
F10116 Triple Differential Line Receiver

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT	$\overline{\text{OUTPUT}}$
L	H	L	H
H	L	H	L
L	$V_{BB}$	L	H
H	$V_{BB}$	H	L
$V_{BB}$	H	L	H
$V_{BB}$	L	H	L

### LOGIC DIAGRAM

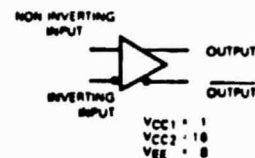
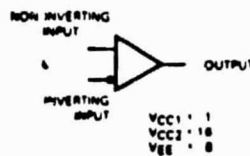


F10115



F10116

### FUNCTIONS



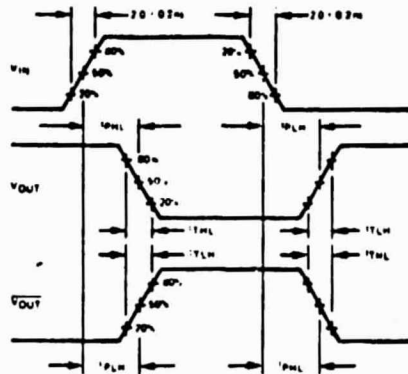
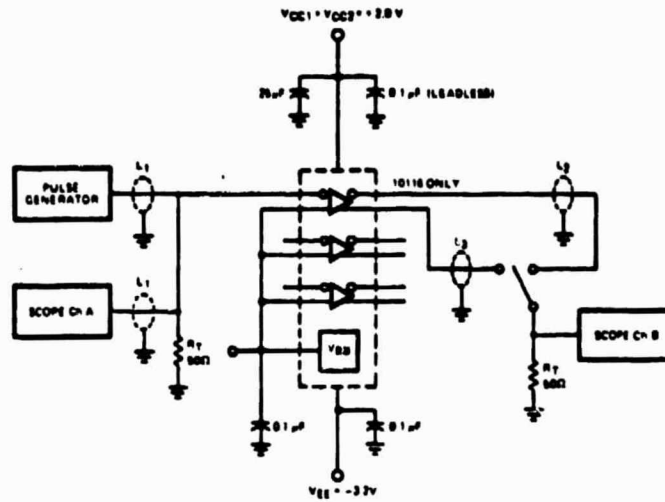
DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS		
		B	TYP	A					
$V_{OH}$	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table  Loading is 50 $\Omega$ to -2.0 V		
$V_{OL}$	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C			
$V_{OHC}$	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C			
$V_{OLC}$	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C			
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs		
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs		
$I_{IH}$	Input Current HIGH			95	$\mu\text{A}$	25°C	$V_{IN} = V_{IHA}$		
$I_{CBO}$	Input Collector - Base Leakage Current	-1.0			$\mu\text{A}$	25°C	$V_{IN} = -5.2 \text{ V}$		
$I_{EE}$	Power Supply Current	F10115	-26	-18		mA	25°C	Leads 4,7,10,13 = $V_{ILB}$ . Leads 5,6,11,12 = $V_{BB}$	
		F10116	-21	-14			mA	25°C	Leads 4,9,12 = $V_{ILB}$ . Leads 5,10,13 = $V_{BB}$
$V_{BB}$	Reference Voltage		-1380		-1255	mV	0°C	F10115, Connect Leads 5,6,11,12 to Lead 9	
			-1350		-1230		mV	25°C	
			-1305		-1165		mV	75°C	F10116, Connect Leads 5,10,13 to Lead 11

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1 0		2 9	ns	
$t_{PHL}$	Propagation Delay, HIGH to LOW	1 0		2 9	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1 5		3 3	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1 5		3 3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



Unused outputs connect to a  $50\Omega$  resistor to ground.

One input from each gate must be tied to  $V_{BB}$  during testing

$L_1$ ,  $L_2$ , and  $L_3$  = equal length  $50\Omega$  impedance lines

$R_T$  =  $50\Omega$  termination of scope

# FAIRCHILD ECL DATA SHEET • F10115 • F10116

A line receiver is shown in *Figure 2*. The line is normally terminated in its characteristic impedance (typically 100 Ω) and output pull down resistors (typically 510 Ω) are used. The voltage across the terminating resistor  $V_T$  may be calculated as follows:

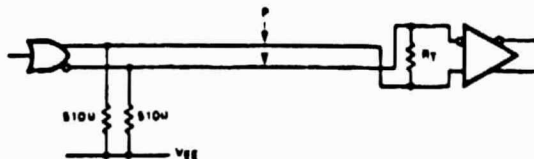
$$V_T = \frac{(V_{EE} - V_{OH}) R_T}{R_E + R_T + R_{LINE}}$$

Where  $V_{OH}$  is the output voltage HIGH of the driving gate,  $R_{LINE}$  is the resistance and  $R_T$  is the terminating resistor. With typical values,  $V_T$  is 620 mV. The line receivers have a minimum differential input voltage gain of 7 V/V allowing very long twisted pairs to be driven. The line receivers employ active current sources which allow them to reject common mode inputs between -0.55 and -3 V.

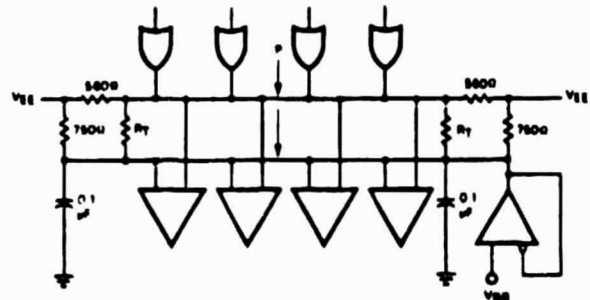
Information transfer is often organized with a data bus approach, where many sources may input and receive data on a common bus as illustrated in *Figure 3*. This configuration is a special case of wired-OR and the line receiver inputs are essentially single ended which reduces worst case voltage gain to 3.5 V/V. In practice it is possible to transmit data at rates in excess of 100 MHz over bus lengths of 10 feet, having 10 or more receivers and transmitters on the line.

Twisted pair differential lines are recommended for clock distribution since clock skew may be balanced by adjusting line lengths. Propagation time is approximately 1 ns per eight inches of line.

### TWISTED-PAIR CONNECTIONS



Differential Transmission and Reception



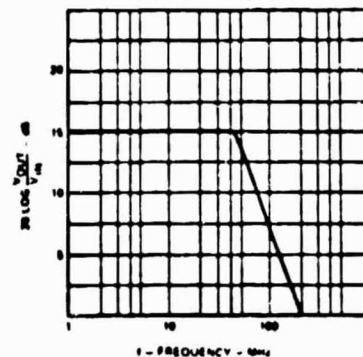
Backplane Data Bus

#### PARAMETERS FOR LINEAR APPLICATIONS

$V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	LIMITS			UNITS
	B	TYP	A	
Voltage Gain	3.5	5.0	6.0	V/V
Bandwidth		60		MHz
Input Resistance	4	6		kΩ
Input Capacitance		3		pF
Input Offset Current		2		μA
Input Bias Current		17	30	μA
Common Mode Input Voltage Range	-3.0		-0.55	V
Common Mode Rejection Ratio	50			dB
Supply Voltage Rejection Ratio		35		dB
Output Voltage Swing		0.40		V <sub>pp</sub>
Output Source Current			60	mA
Output Resistance		9		Ω

#### TYPICAL LINE RECEIVER DIFFERENTIAL GAIN VERSUS INPUT FREQUENCY



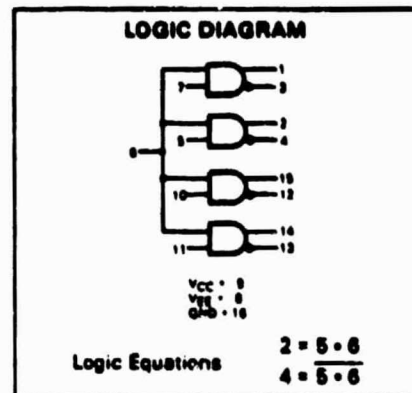


# F10124

## QUAD TTL TO ECL TRANSLATOR

**DESCRIPTION** — The F10124 is a Quad Translator, designed to convert TTL logic levels to 10K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input ( $E_C$ ), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the F10124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.



**DC CHARACTERISTICS:**  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = +5.0 \text{ V}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS	
		B	TYP	A				
$V_{OH}$	Output Voltage HIGH	-1000		-840	mV	0°C	$V_{IN} = +4.0 \text{ V}$ or $+0.4 \text{ V}$ per Logic Function  Loading is $50 \Omega$ to $-2.0 \text{ V}$	
		-960		-810		25°C		
		-900		-720		75°C		
$V_{OL}$	Output Voltage LOW	-1870		-1665	mV	0°C		
		-1850		-1650		25°C		
		-1830		-1625		75°C		
$V_{OHC}$	Output Voltage HIGH	-1020			mV	0°C		
		-980				25°C		
		-920				75°C		
$V_{OLC}$	Output Voltage LOW			-1645	mV	0°C		
				-1630		25°C		
				-1605		75°C		
$V_{IH}$	Input Voltage HIGH	+1.9		5.0	V	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		+1.8		5.0		25°C		
		+1.8		5.0		75°C		
$V_{IL}$	Input Voltage LOW	0		+1.1	V	0°C	Guaranteed Input Voltage LOW for All Inputs	
		0		+1.1		25°C		
		0		+0.95		75°C		
$V_{CD}$	Clamp Input Voltage	-1.5			V	25°C	$I_{IN} = -10 \text{ mA}$	
$V_{BD}$	Input Breakdown Voltage	+5.5			V	25°C	$I_{IN} = +1.0 \text{ mA}$ , Other Inputs $V_{IN} = GND$	
$I_{IH}$	Input Current HIGH			50	$\mu\text{A}$	25°C	$V_{IN} = +2.4 \text{ V}$ , $E_C V_{IN} = +0.4 \text{ V}$	
$I_{IHx}$	Input Current HIGH $E_C$			200	$\mu\text{A}$	25°C	$E_C V_{IN} = +2.4 \text{ V}$ , All Other Inputs $V_{IN} = +0.4 \text{ V}$	
$I_{ILx}$	Input Current LOW $E_C$	-12.8			mA	25°C	$E_C V_{IN} = +0.4 \text{ V}$ , All Other Inputs $V_{IN} = +4.0 \text{ V}$	
$I_{IL}$	Input Current LOW	-3.2			mA	25°C	$V_{IN} = +0.4 \text{ V}$ , $E_C V_{IN} = +0.4 \text{ V}$	
$I_{EE}$	Power Supply Current	-34	-26		mA	25°C	Inputs and Outputs Open	
$I_{CCH}$	Power Supply Current		+13	+16	mA	25°C	All Inputs $V_{IN} = +4.0 \text{ V}$	
$I_{CCL}$	Power Supply Current		+18	+25	mA	25°C	All Inputs $V_{IN} = GND$	

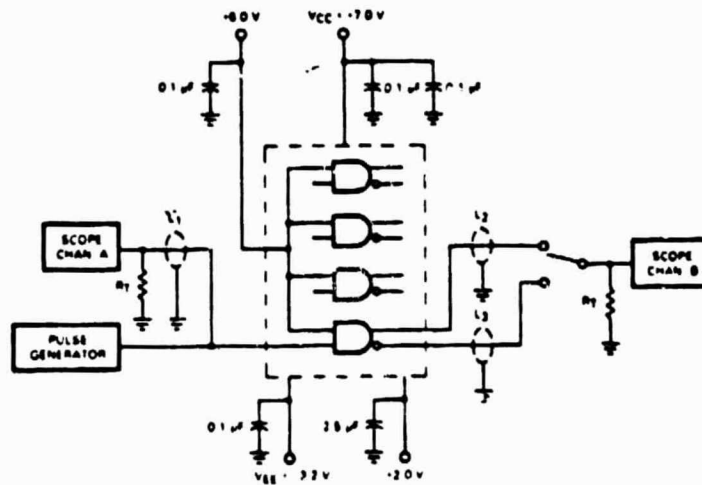


# FAIRCHILD ECL DATA SHEET • F10124

**SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2\text{ V}$ ,  $V_{CC} = +5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

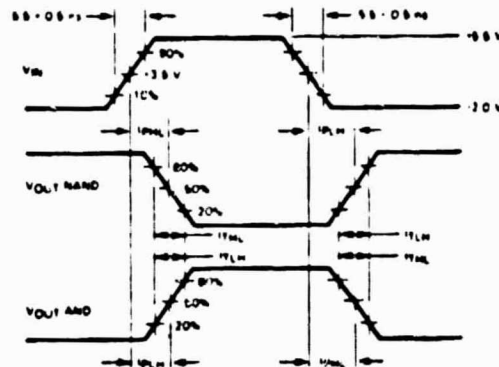
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.0	3.0	6.0	ns	
$t_{PHL}$	Propagation Delay, HIGH to LOW	1.0	3.0	6.0	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.5	3.9	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.5	3.9	ns	

## SWITCHING CIRCUIT AND WAVEFORMS



### NOTES

Connect unused outputs through  $50\Omega$  resistor to ground  
 $L_1$ ,  $L_2$  and  $L_3$  are equal lengths of  $50\Omega$  impedance lines  
 $R_T$  equals  $50\Omega$  termination of scope



# F10125

## QUAD ECL TO TTL TRANSLATOR

**DESCRIPTION** — The F10125 is a Quad Translator for converting F10K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or as a differential line receiver. An internal reference voltage generator provides  $V_{BB}$  on lead 1 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go LOW when the inputs are left unconnected, have a fan out of 10 Schottky TTL loads.

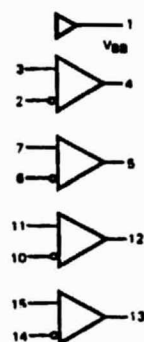
When used in the differential mode, the inputs have a common mode rejection of +1 V — making this device tolerant of ground offsets and transients between the signal source and the translator.

TRUTH TABLE

INPUTS		OUTPUT
Non-Inverting $I_n$	Inverting $\bar{I}_n$	$O_n$
L	H	L
H	L	H
L	L	•
H	H	•
OPEN	OPEN	L
$V_{EE}$	$V_{EE}$	L
L	$V_{BB}$	L
H	$V_{BB}$	H
$V_{BB}$	L	H
$V_{BB}$	H	L

•Undetermined

LOGIC DIAGRAM



$V_{CC} = 5$   
 $V_{EE} = 0$   
 $GND = 16$

FUNCTION



# FAIRCHILD ECL DATA SHEET • F10125

DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$V_{OH}$	Output Voltage HIGH	+2.5 +2.5 +2.5			V	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table  Loading is -2.0 mA $V_{OH}$ +20 mA $V_{OL}$
$V_{OL}$	Output Voltage LOW			+0.5 +0.5 +0.5	V	0°C 25°C	
$V_{OHC}$	Output Voltage HIGH	+2.5 +2.5 +2.5			V	0°C 25°C 75°C	
$V_{OLC}$	Output Voltage LOW			+0.5 +0.5 +0.5	V	0°C 25°C 75°C	
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
$V_{IHH}$	Common Mode Rejection Input Voltage HIGH +1.0 V			+0.160 +0.190 +0.280	V	0°C 25°C 75°C	
$V_{ILH}$	Common Mode Rejection Input Voltage LOW +1.0 V	-0.870 -0.850 -0.830			V	0°C 25°C 75°C	
$V_{IHL}$	Common Mode Rejection Input Voltage HIGH -1.0 V			-1.840 -1.810 -1.720	V	0°C 25°C 75°C	
$V_{ILL}$	Common Mode Rejection Input Voltage LOW -1.0 V	-2.870 -2.850 -2.830			V	0°C 25°C 75°C	
$V_{BB}$	Reference Voltage	-1380 -1350 -1305		-1250 -1230 -1165	mV	0°C 25°C 75°C	$V_{IN} = V_{ILB}$
$I_{CBO}$	Input Leakage Current	-1.0			$\mu\text{A}$	25°C	$V_{IN} = V_{EE}$ Note 1
$I_{IH}$	Input Current HIGH			115	$\mu\text{A}$	25°C	$V_{IN} = V_{IHA}$ Note 1
$I_{OS}$	Short Circuit Current	-100		-40	mA	25°C	$V_{IN} = \text{GND}$ Note 2
$I_{EE}$	Negative Power Supply	-40			mA	25°C	Inputs and Outputs Open
$I_{EH}$	High Power Supply			52	mA	25°C	$V_{IN} = V_{IHA}$ Note 3
$I_{CCL}$	Positive Power Supply			39	mA	25°C	$V_{IN} = V_{ILB}$ Note 3

**NOTES**

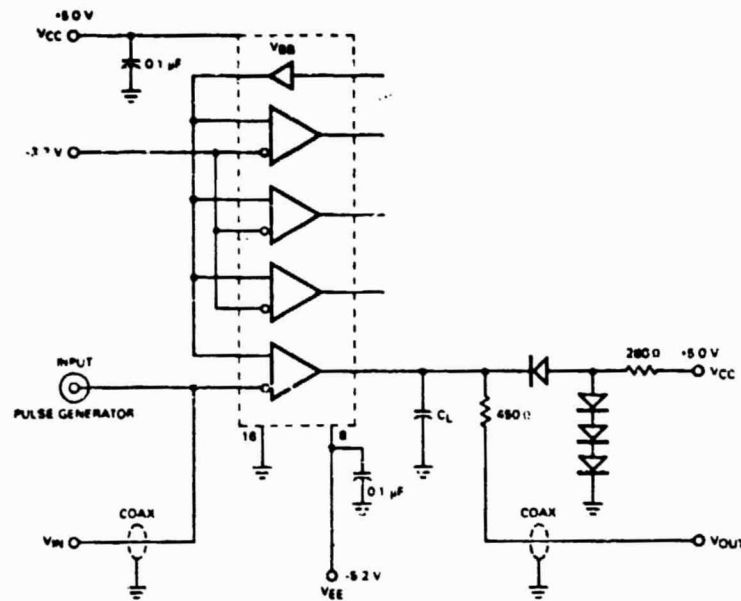
1. Complementary Input =  $V_{BB}$
2. One Output at a Time
3. Lead 2, 6, 10, 14 =  $V_{IN}$   
Lead 3, 7, 11, 15 = Lead 1 ( $V_{BB}$ )

# FAIRCHILD ECL DATA SHEET • F10125

**SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.0		6.0	ns	
$t_{PHL}$	Propagation Delay, HIGH to LOW	1.0		6.0	ns	
$t_{TLH}$	Output Transition Time 1.0 V to 2.0 V			3.3	ns	
$t_{THL}$	Output Transition Time 2.0 V to 1.0 V			3.3	ns	

## SWITCHING CIRCUIT AND WAVEFORMS

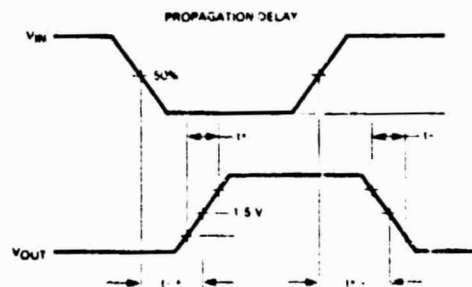


50  $\Omega$  termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50  $\Omega$  coaxial cable. Wire length should be <math>1/4</math> inch from  $TP_{IN}$  to input lead and  $TP_{OUT}$  to output lead.

$C_L = 25 \text{ pF}$ , including test fixture

One input from each gate must be tied to  $V_{BB}$  (Lead 1) during testing



# F10131

## HIGH SPEED DUAL D FLIP-FLOP

**DESCRIPTION** — The F10131 contains two master/slave D-type flip-flops. The internal clock is the OR of two clock inputs, one common to both flip-flops. The OR clock permits the use of one input as a clock pulse and the other as an active LOW enable. While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

Each flip-flop has separate set and clear inputs which asynchronously determine the state of the output independent of the clock levels. Note that the output voltage levels of a flip-flop are unpredictable if both set and clear signals are HIGH.

### LEAD NAMES

D <sub>1</sub>	Data Input to Master
CP <sub>1</sub>	Clock Input
CP <sub>C</sub>	Common Clock Input
Q <sub>1</sub>	Output
$\bar{Q}_1$	Complement Output
S <sub>D1</sub>	Set Direct Input
C <sub>D1</sub>	Clear Direct Input

### TRUTH TABLES

#### ASYNCHRONOUS OPERATION

#### S<sub>D</sub> C<sub>D</sub> TABLE

C <sub>D</sub>	S <sub>D</sub>	Q	$\bar{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	undetermined	

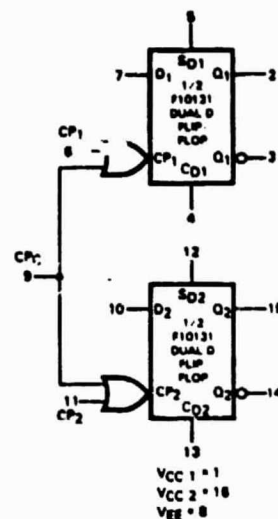
#### SYNCHRONOUS OPERATION

#### D TABLE

D	Q <sub>(t+1)</sub>
L	L
H	H
S <sub>D</sub> = C <sub>D</sub> = LOW	

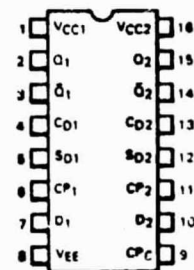
(t+1) = Time after positive going clock transition

### LOGIC SYMBOL

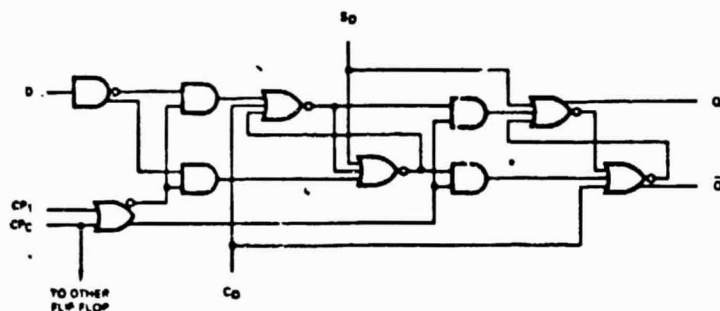


### CONNECTION DIAGRAM

#### DIP (TCP VIEW)



### LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

FAIRCHILD ECL DATA SHEET • F10131

DC CHARACTERISTICS:  $V_{EE} = -5.2\text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS			
		B	TYP	A					
$V_{OH}$	Output Voltage HIGH	-1000 -860 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table	Loading is 50Ω to -2.0 V	
$V_{OL}$	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C			
$V_{OHC}$	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C			$V_{IN} = V_{IHB}$ or $V_{ILA}$ per Truth Table
$V_{OLC}$	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C			
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs		
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs		
$I_{IH}$	Input Current HIGH CP C <sub>CP</sub> D S <sub>D</sub> & C <sub>D</sub>			220 265 245 330	μA	25°C	$V_{IN} = V_{IHA}$		
$I_{IL}$	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$		
$I_{EE}$	Power Supply Current	-56	-45		mA	25°C	Inputs and Outputs Open		

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2\text{ V}$ ,  $T_A = 25^\circ\text{C}$

$f_{\text{count}}$	Toggle Frequency	125	160		MHz	
$t_{PLH}$	Propagation Delay Clock to Output	1.5	3.0	4.5	ns	
$t_{PHL}$	Propagation Delay Clock to Output	1.5	3.0	4.5	ns	
$t_{PLH}$	Propagation Delay Set to Q, Clear to $\bar{Q}$	1.2	2.2	4.3	ns	
$t_{PHL}$	Propagation Delay Set to $\bar{Q}$ , Clear to Q	1.2	2.2	4.3	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.2	4.5	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.2	4.5	ns	
$t_s$	Set-Up Time Data to Clock	2.5	0.5		ns	
$t_h$	Hold Time Data to Clock	1.5	-0.5		ns	

# F10136 • F10536 • F10137 • F10537

## 4-STAGE UP/DOWN COUNTERS

### F10K VOLTAGE COMPENSATED ECL

**DESCRIPTION** - The F10136/F10536 and F10137/F10537 are 4-stage synchronous counters capable of operating at typical count rates of 250 MHz. The circuits are designed to operate in count up, count down, hold, and preset modes, as determined by signals applied to select inputs  $S_1$  and  $S_2$ . The F10136 is a modulo-16 binary counter and the F10137 is a BCD (8421) decade counter.

All operations are synchronous and state changes are initiated by the rising edge of the clock. Each circuit has an active LOW Count Enable ( $\overline{CE}$ ) input and an active LOW Terminal Count ( $\overline{TC}$ ) output which allow two or more counters to be cascaded without extra logic. The preset feature makes it possible to use the F10136 and F10137 as programmable counters in a broad variety of applications.

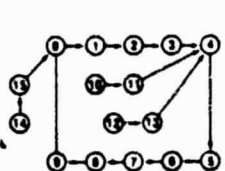
- HIGH SPEED . . . 250 MHz TYPICAL COUNT RATE
- FULLY SYNCHRONOUS
- RIPPLE CARRY SIMPLIFIES CASCADING
- PRESETTABLE, FOR VARIABLE MODULUS APPLICATIONS
- SELECT INPUTS CAN BE WIRED TO  $V_{CC}$
- 50  $\Omega$  LINE DRIVING CAPABILITY
- SEPARATE  $V_{CC}$  PINS ELIMINATE NOISE COUPLING
- INTERNAL 50 k $\Omega$  INPUT PULL-DOWN RESISTORS . . . UNUSED INPUTS CAN BE LEFT OPEN

#### PIN NAMES

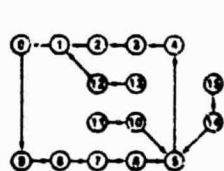
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Positive-Going Active Edge)
$P_n$	Preset Data Inputs
$Q_n$	Flip-flop Outputs
$S_n$	Operating Mode Select Inputs
$\overline{TC}$	Terminal Count Output (Active LOW)

#### STATE DIAGRAMS

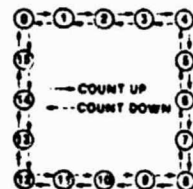
10537/10137 COUNT UP



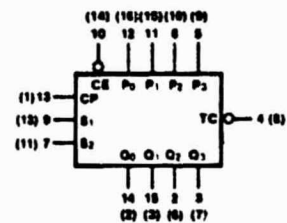
10537/10137 COUNT DOWN



10536/10136

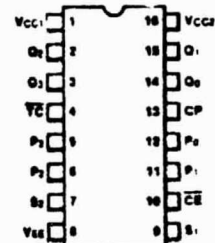


#### LOGIC SYMBOL



$V_{CC1}$  = Pin 1 (5)  
 $V_{CC2}$  = Pin 16 (4)  
 $V_{EE}$  = Pin 8 (12)  
 ( ) = Flatpak

#### CONNECTION DIAGRAM DIP (TOP VIEW)



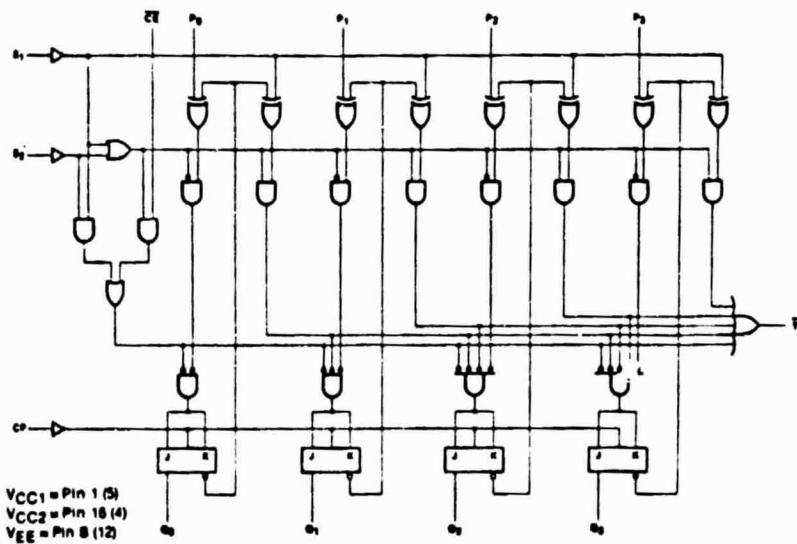
FAIRCHILD ECL • F10136 • F10536 • F10137 • F10537

Fig. 1. Sample Operating Sequences, F10136 • F10536 Binary

INPUTS								OUTPUTS					SELECT
S <sub>1</sub>	S <sub>2</sub>	$\overline{CE}$	CP	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	$\overline{TC}$	MODE
L	L	X	J	H	L	H	H	H	L	H	H	L	PRESET*
L	H	L	J	X	X	X	X	H	H	L	L	H	COUNT UP  (Max) ( $\overline{CE}$ Inhibit)
L	H	L	J	X	X	X	X	H	H	L	H	H	
L	H	L	J	X	X	X	X	H	H	H	H	L	
L	H	H	X	X	X	X	X	H	H	H	H	H	
L	H	L	J	X	X	X	X	L	L	L	L	H	
L	H	L	J	X	X	X	X	L	L	L	L	H	
L	H	L	J	X	X	X	X	L	L	L	L	H	
H	H	X	X	X	X	X	X	L	L	L	H	H	HOLD
L	L	X	J	L	H	L	L	L	H	L	L	L	PRESET*
H	L	L	J	X	X	X	X	L	L	H	H	H	COUNT DOWN  (Min)
H	L	L	J	X	X	X	X	L	L	L	L	H	
H	L	L	J	X	X	X	X	L	L	L	L	L	
H	L	L	J	X	X	X	X	H	H	H	H	H	
H	L	L	J	X	X	X	X	H	H	H	L	H	
H	L	L	J	X	X	X	X	H	H	H	L	H	

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 \* = Starting point, arbitrary previous data

F10136/F10536 LOGIC DIAGRAM



Note: that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.



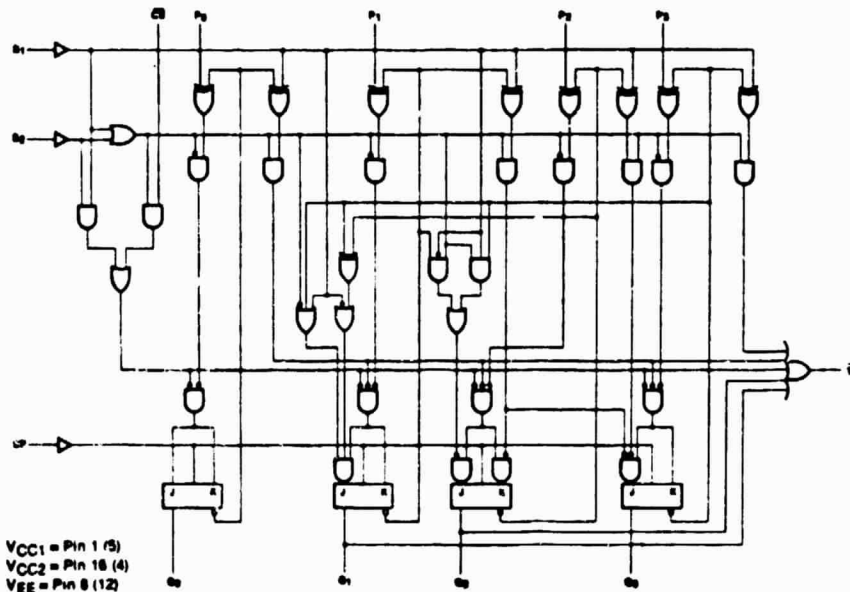
FAIRCHILD ECL • F10136 • F10536 • F10137 • F10537

Fig. 2. Sample Operating Sequences, F10137 • F10537 Binary

INPUTS								OUTPUTS					SELECT
S <sub>1</sub>	S <sub>2</sub>	$\overline{CE}$	CP	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	$\overline{TC}$	MODE
L	L	X	J	L	H	L	H	L	H	L	H	H	PRESET*
L	H	L	J	X	X	X	X	L	H	H	L	H	COUNT UP  (Max) ( $\overline{CE}$ Inhibit)
L	H	L	J	X	X	X	X	L	H	H	L	H	
L	H	L	J	X	X	X	X	L	H	H	L	H	
L	H	L	J	X	X	X	X	L	H	H	L	H	
L	H	L	J	X	X	X	X	L	L	L	L	H	
L	H	L	J	X	X	X	X	L	L	H	L	H	
H	H	X	X	X	X	X	X	L	L	H	L	H	HOLD
L	L	X	J	L	H	L	L	L	H	L	L	H	PRESET*
H	L	L	J	X	X	X	X	L	L	H	H	H	COUNT DOWN  (Min)
H	L	L	J	X	X	X	X	L	L	H	L	H	
H	L	L	J	X	X	X	X	L	L	L	L	L	
H	L	L	J	X	X	X	X	L	L	L	L	L	
H	L	L	J	X	X	X	X	H	L	L	H	H	
H	L	L	J	X	X	X	X	H	L	L	L	H	

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 \* = Starting point, arbitrary data

F10137/F10537 LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

FAIRCHILD ECL • F10136 • F10536 • F10137 • F10537

**FUNCTIONAL DESCRIPTION**—In the counting modes, the F10136 follows a straightforward binary sequence. The F10137 follows the 8421 BCD sequence, as indicated in the state diagrams on page 1. For either circuit type, the  $\overline{CE}$  input must be LOW for counting to occur, as indicated in the sample sequences of Figures 1 and 2.

The Select inputs determine the operating mode of a circuit, as shown in the table of Figure 3. All operations are synchronous and state changes are initiated by the rising edge of the clock. The  $\overline{CE}$  input has no effect on the preset and hold operations. Either of the Select inputs can be wired to  $V_{CC}$ ; this simplifies designs in which  $S_1$  or  $S_2$  is required to always be HIGH.

In the counting modes the  $\overline{TC}$  output is controlled by the  $\overline{CE}$  input and by the state of the flip-flops, as indicated in Figure 3.  $\overline{TC}$  is normally HIGH and goes LOW (assuming  $\overline{CE}$  is LOW) when the counter reaches zero in the count down mode or when it reaches maximum (15 for the F10136, 9 for the F10137) in the count up mode. The control that the  $\overline{CE}$  input has on the  $\overline{TC}$  output makes it possible to form multi-stage counters without external logic, as shown in Figure 4. In order for a given stage to count, the  $\overline{TC}$  outputs (and thus the  $\overline{CE}$  inputs) of all the preceding stages must be LOW. The frequency capability of this arrangement is limited by the time required for a negative-going  $\overline{TC}$  signal from the first stage to ripple through to the  $\overline{CE}$  input of the last stage. The time between successive positive-going clock edges must not be less than the sum of the CP to  $\overline{TC}$  delay of the first stage, the  $\overline{CE}$  to  $\overline{TC}$  delays of the intermediate stages, and the  $\overline{CE}$  to CP set-up time of the last stage. The counter can be enabled/disabled at the  $\overline{CE}$  input of the first stage (Figure 4), or by using the Select inputs.

In the preset mode, the  $\overline{TC}$  output of the F10136 is forced LOW, while that of the F10137 depends on the state of  $Q_1$  and  $Q_2$ , as indicated in Figure 3. For either circuit type, the  $\overline{TC}$  output is forced HIGH in the hold mode. This feature can be used to simplify designs for certain types of applications. In the simple counter of Figure 4, for example, the second and subsequent stages can be prevented from counting by putting the first stage into the hold mode, causing a HIGH signal to ripple through all  $\overline{TC}$  outputs. Wiring simplification is possible if the counter is to operate in only one of the counting modes, plus preset and hold. For example, if the  $S_1$  inputs of the second and subsequent stages are left open (LOW) and their  $S_2$  inputs wired in parallel with  $S_2$  of the first stage, then the  $S_2$  signal selects either the count up or preset mode for these latter stages. Putting the first stage into the hold mode effectively achieves a hold for the entire counter in the manner previously described. Designers should bear in mind that a  $\overline{TC}$  output is subject to decoding spikes and therefore should not be used as a clock.

The flip-flops are master/slave type with internal JK feedback. Information enters the master when the clock is LOW and transfers to the slave when the clock goes HIGH. Signals on the Preset, Select, and  $\overline{CE}$  inputs must be in the intended state at least a set-up time before the clock rising edge. Hold times for these inputs are negative, however, which offers simplifications in some applications. Figure 5 illustrates an arrangement for a programmable down counter using F10136 circuits. When the counter reaches the all-zeros state and the clock goes LOW, the  $\overline{TC}$  outputs will go LOW, starting at the first stage and rippling through to make the  $S_1$  inputs LOW. Thus with  $S_1$  and  $S_2$  LOW the circuits are in the preset mode and the preset data will be entered on the next rising clock edge.  $S_2$  also goes HIGH (with the clock) but this does not interfere with presetting because of the negative hold time characteristic. The  $\overline{CE}$  input of the first stage also goes HIGH with the presetting clock, causing the  $\overline{TC}$  output to go HIGH and ripple through the second and third stages to make the  $S$  inputs HIGH. After this is accomplished the circuits are in the hold mode when the clock is HIGH and in the count down mode when the clock is LOW.

The outputs of these circuits have no internal pull-down resistors and the 50 k $\Omega$  input pull-down resistors of F10K elements do not provide sufficient current to perform the pull-down function at electronic speeds. External pull-down current is an integral function of the termination scheme selected by the system designer, as discussed in Chapter 5 of the Fairchild ECL Handbook.

Fig. 3. Mode Select and Terminal Count Equation Table

Select		Operating Mode	Terminal Count Output Equation	
$S_1$	$S_2$		F10136 Binary	F10137 BCD
L	L	Preset	$\overline{TC} = \text{LOW}$	$\overline{TC} = Q_1 + Q_2$
L	H	Count Up	$\overline{TC} = \overline{CE} + \overline{Q_0} + \overline{Q_1} + \overline{Q_2} + \overline{Q_3}$	$\overline{TC} = \overline{CE} + \overline{Q_0} + Q_1 + Q_2 + \overline{Q_3}$
H	L	Count Down	$\overline{TC} = \overline{CE} + Q_0 + Q_1 + Q_2 + Q_3$	$\overline{TC} = \overline{CE} + Q_0 + Q_1 + Q_2 + Q_3$
H	H	Hold	$\overline{TC} = \text{HIGH}$	$\overline{TC} = \text{HIGH}$

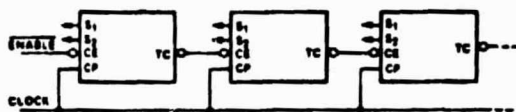
FAIRCHILD ECL • F10136 • F10536 • F10137 • F10537

DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

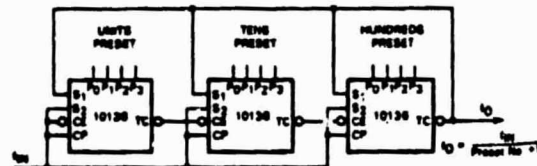
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$I_{IH}$	Input Current HIGH				$\mu\text{A}$	25°C	$V_{IN} = V_{IHA}$
	$P_n$			230			
	$S_2$			265			
	CP			290			
	$S_1, \overline{CE}$			245			
$I_{EE}$	Power Supply Current	-136	-106		mA	25°C	Outputs Open, Pin 12 tied to $V_{IH}$

AC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	TEST CONDITIONS
		B	TYP	A		
$f_{\text{count}}$	Count Frequency	125	250		MHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Clock to $Q_n$	1.0	2.2	4.5	ns	
$t_{PHL}$ $t_{PLH}$	Propagation Delay, Clock to $\overline{TC}$		4.5		ns	
$t_{PHL}$ $t_{PLH}$	Propagation Delay, $\overline{CE}$ to $\overline{TC}$	1.6	3.5	6.8	ns	
$t_{THL}$ $t_{TLH}$	Output Transition Time LOW-to-HIGH, HIGH-to-LOW (20% to 80%), (80% to 20%)	1.1	2.0	3.3	ns	
$t_s$	Set-Up Time Prior to Clock				ns	
	Data		2.0			
	Select		4.0			
	$\overline{CE}$ (to Enable Count)		2.7			
	$\overline{CE}$ (to Inhibit Count)		1.2			
$t_h$	Hold Time After Clock				ns	
	Data		-2.0			
	Select		-4.0			
	$\overline{CE}$ (to Enable Count)		-1.0			
	$\overline{CE}$ (to Inhibit Count)		-2.5			

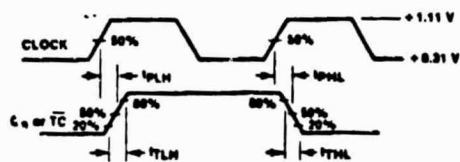
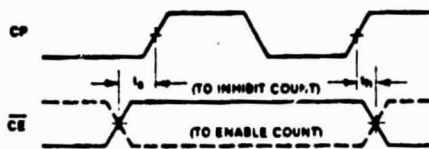
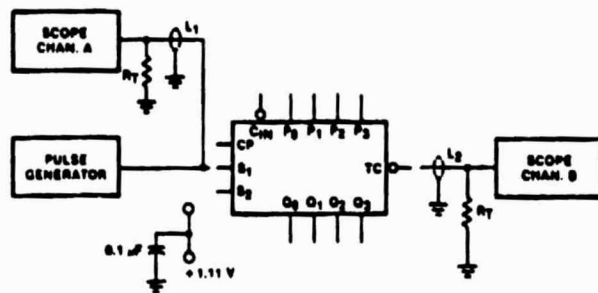


Multi-Stage Counter Using Ripple Carry



Programmable Down Counter

SWITCHING CIRCUIT AND WAVEFORMS



$L_1$  and  $L_2$  = equal length 50  $\Omega$  impedance lines  
 $R_T$  = 50  $\Omega$  termination of scope  
 $C_L$  =  $J_{14}$  and stray capacitance < 1.0 pF

Decoupling 0.1  $\mu$ F from gnd. to VEE and VCC  
 $V_{CC1} - V_{CC2} = 2.0$  V  
 $V_{EE} = -3.2$  V

# F10160

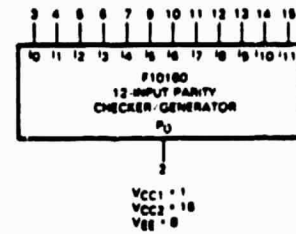
## 12-BIT PARITY CHECKER/GENERATOR

**DESCRIPTION** — The F10160 is a 12-Input Parity Generator. The output will be HIGH when an odd number of inputs are HIGH; typical delay is 4 ns. For applications requiring fewer than 12 inputs, unused inputs may be left open, since internal input resistors hold unconnected inputs LOW.

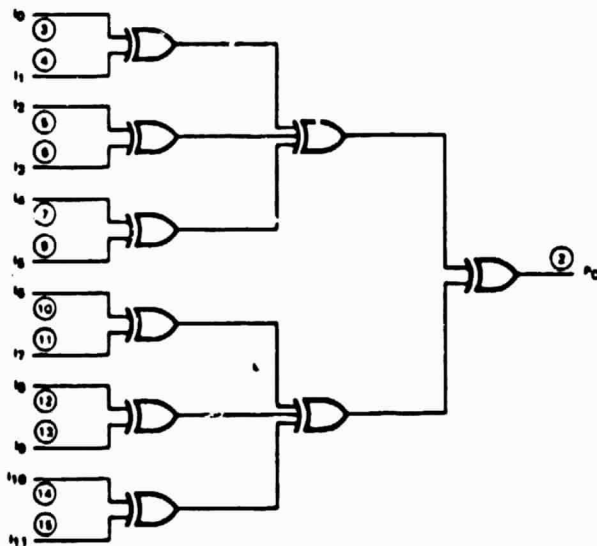
### LEAD NAMES

$I_n$             Inputs  
 $P_O$             Parity Odd

### LOGIC SYMBOL

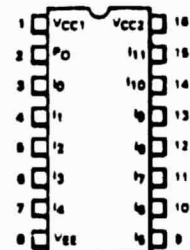


### LOGIC DIAGRAM



○ = LEAD NUMBERS

### CONNECTION DIAGRAM DIP (TOP VIEW)



DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$V_{OH}$	Output Voltage HIGH	-1000 -880 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Logic Function  Loading is 50Ω to -2.0 V
$V_{OL}$	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C	
$V_{OHC}$	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	
$V_{OLC}$	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C	
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
$I_{IH}$	Input Current HIGH (All Inputs)			220	μA	25°C	$V_{IN} = V_{IHA}$
$I_{IL}$	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$
$I_{EE}$	Power Supply Current	-59	-48		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH		4.0		ns	
$t_{PHL}$	Propagation Delay, HIGH to LOW		4.0		ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

# F10161

## 1-OF-8 DECODER

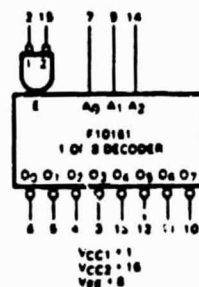
### ACTIVE LOW OUTPUTS

**DESCRIPTION** — The F10161 accepts a 3-bit binary input and provides eight mutually exclusive outputs. The selected output will be LOW while all other outputs are HIGH. Two enable inputs force all outputs HIGH when either or both are HIGH. Typical delay is 4 ns from any address or enable to any output.

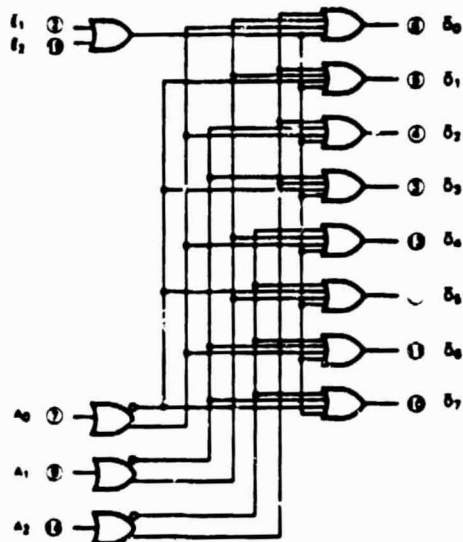
#### LEAD NAMES

$\bar{E}_n$  Enable (Active LOW)  
 $A_n$  Address Inputs  
 $\bar{O}_n$  Output (Active LOW)

#### LOGIC SYMBOL



#### LOGIC DIAGRAM



#### CONNECTION DIAGRAM DIP (TOP VIEW)



FAIRCHILD ECL DATA SHEET • F10161

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\bar{E}_2$	$\bar{E}_1$	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

L = LOW Voltage Level  
 H = HIGH Voltage Level  
 X = Don't Care

DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T <sub>A</sub>	CONDITIONS
		B	TYP	A			
V <sub>OH</sub>	Output Voltage HIGH	-1000		-840	mV	0°C	V <sub>IN</sub> = V <sub>IHA</sub> or V <sub>ILB</sub> per Truth Table
		-960		-810		25°C	
		-900		-720		75°C	
V <sub>OL</sub>	Output Voltage LOW	-1870		-1665	mV	0°C	
		-1850		-1650		25°C	
		-1830		-1625		75°C	
V <sub>OHc</sub>	Output Voltage HIGH	-1020			mV	0°C	V <sub>IN</sub> = V <sub>IHB</sub> or V <sub>ILA</sub> per Truth Table
		-980				25°C	
		-920				75°C	
V <sub>OLc</sub>	Output Voltage LOW			-1645	mV	0°C	
				-1630		25°C	
				-1605		75°C	
V <sub>IH</sub>	Input Voltage HIGH	-1145		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		-1105		-810		25°C	
		-1045		-720		75°C	
V <sub>IL</sub>	Input Voltage LOW	-1870		-1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		-1850		-1475		25°C	
		-1830		-1450		75°C	
I <sub>IH</sub>	Input Current HIGH			220	μA	25°C	V <sub>IN</sub> = V <sub>IHA</sub>
I <sub>IL</sub>	Input Current LOW	0.5			μA	25°C	V <sub>IN</sub> = V <sub>ILB</sub>
I <sub>EE</sub>	Power Supply Current	-76	-55		mA	25°C	Inputs and Outputs Open

Loading is 50Ω to -2.0 V

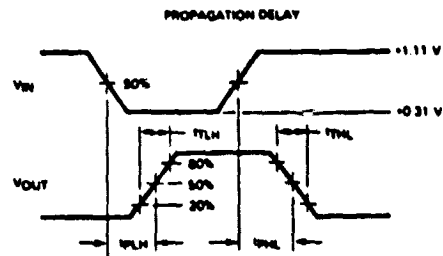
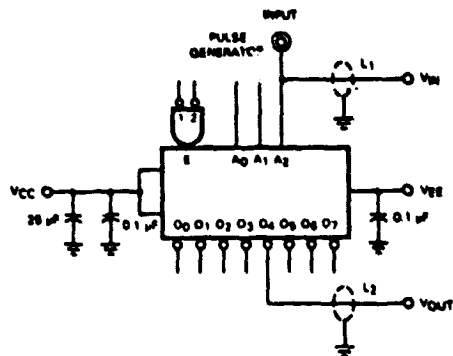


INTEGRAL ECL DATA SHEET • F10161

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	
$t_{PHL}$	Propagation Delay	1.5	4.0	6.0	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5		3.3	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5		3.3	ns	

SWITCHING CIRCUIT AND WAVEFORMS



$L_1$  and  $L_2$  = equal length  $50 \Omega$  impedance lines  
 $R_T$  =  $50 \Omega$  termination of scope  
 $C_L$  = jig and stray capacitance  $< 5.0 \text{ pF}$   
 Decoupling  $0.1 \mu\text{F}$  from gnd to  $V_{EE}$  and  $V_{CC}$   
 $V_{CC1} = V_{CC2} = 2.0 \text{ V}$   
 $V_{EE} = -3.2 \text{ V}$

# F10171

## DUAL 1-OF-4 DECODER/DEMULTIPLEXER

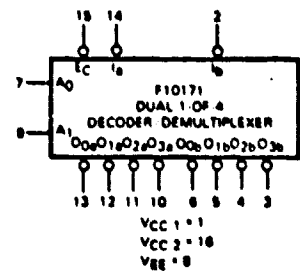
### SELECTED OUTPUTS LOW

**DESCRIPTION** — The F10171 contains a pair of 1-of-4 Decoder/Multiplexers with Common Enable ( $\bar{E}_C$ ) and Address ( $A_0$  and  $A_1$ ) inputs. In each decoder the unselected (or disabled) outputs are HIGH and the selected (or enabled) output repeats the information present on its data input ( $\bar{I}_a$  or  $\bar{I}_b$ ). If the  $\bar{E}_C$  input is HIGH all outputs of both decoders are HIGH, as indicated in the truth table. The F10171 can be used as a 1-of-8 decoder/demultiplexer by connecting the True and Complement of the third address bit to  $\bar{I}_a$  and  $\bar{I}_b$ , respectively, and using  $\bar{E}_C$  as either a data input or as an enable.

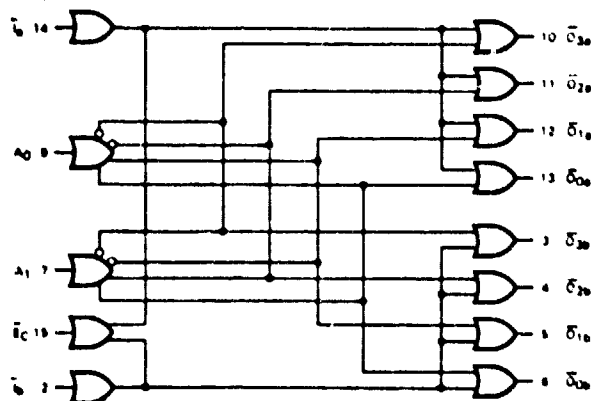
#### LEAD NAMES

$\bar{E}_C$	Common Enable (Active LOW)
$A_n$	Address Inputs
$\bar{I}_n$	Data Inputs
$\bar{O}_n$	Outputs

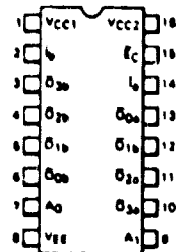
#### LOGIC SYMBOL



#### LOGIC DIAGRAM



#### CONNECTION DIAGRAM DIP (TOP VIEW)



# FAIRCHILD ECL DATA SHEET • F10171

### TRUTH TABLE

$E_C$	$I_b$	$A_1$	$A_0$	$O_{0a}$ $O_{0b}$	$O_{1a}$ $O_{1b}$	$O_{2a}$ $O_{2b}$	$O_{3a}$ $O_{3b}$
L	L	L	L	L	H	H	H
L	H	L	L	H	H	H	H
L	L	L	H	H	L	H	H
L	H	L	H	H	H	H	H
L	L	H	L	H	H	L	H
L	H	H	L	H	H	H	H
L	L	H	H	H	H	H	L
L	H	H	H	H	H	H	H
H	X	X	X	H	H	H	H

L = LOW Voltage Level  
 H = HIGH Voltage Level  
 X = Don't Care

### DC CHARACTERISTICS: $V_{EE} = -5.2\text{ V}$ , $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$V_{OH}$	Output Voltage HIGH	-1000		-840	mV	0°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table  Loading is 50Ω to -2.0V
		-960		-810		25°C	
		-900		-720		75°C	
$V_{OL}$	Output Voltage LOW	-1870		-1665	mV	0°C	
		-1850		-1650		25°C	
		-1830		-1625		75°C	
$V_{OHC}$	Output Voltage HIGH	-1020			mV	0°C	
		-980				25°C	
		-920				75°C	
$V_{OLC}$	Output Voltage LOW			-1645	mV	0°C	
				-1630		25°C	
				-1605		75°C	
$V_{IH}$	Input Voltage HIGH	-1145		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		-1105		-810		25°C	
		-1045		-720		75°C	
$V_{IL}$	Input Voltage LOW	-1870		-1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		-1850		-1475		25°C	
		-1830		-1450		75°C	
$I_{IH}$	Input Current HIGH			220	μA	25°C	$V_{IN} = V_{IHA}$
$I_{IL}$	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$
$I_{EE}$	Power Supply Current	-77	-62		mA	25°C	Inputs and Outputs Open

### SWITCHING CHARACTERISTICS: $V_{EE} = -5.2\text{ V}$ , $V_{CC} = \text{GND}$ , $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay, LOW to HIGH	1.5	4.0	6.0	ns	
$t_{PHL}$	Propagation Delay, HIGH to LOW	1.5	4.0	6.0	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.1	2.0	3.3	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.1	2.0	3.3	ns	

# F10173

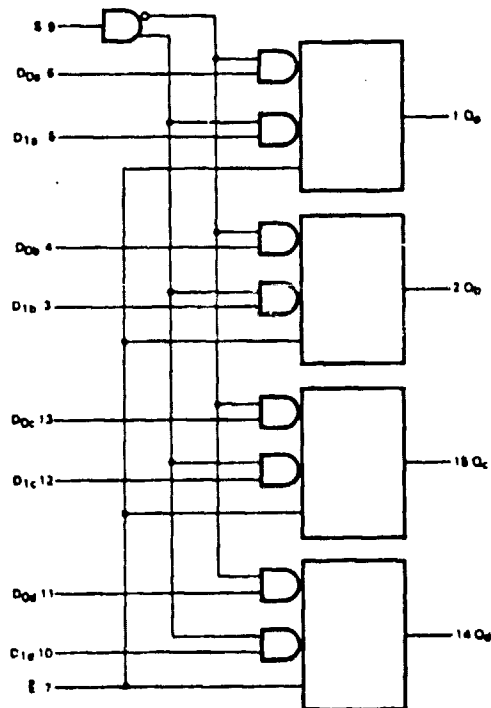
## QUAD MULTIPLEXER/LATCH

**DESCRIPTION** — The F10173 is a Quad 2-Channel Multiplexer with latches. It incorporates a common Enable and a common Data Select input. The Select input determines which Data input is enabled. A HIGH input enables Data inputs  $D_{0a}$ ,  $D_{0b}$ ,  $D_{0c}$ , and  $D_{0d}$  and a LOW enables Data inputs  $D_{1a}$ ,  $D_{1b}$ ,  $D_{1c}$ ,  $D_{1d}$ . Any change on the Data input appears at the outputs while the Enable is LOW. The outputs are latched on the positive transition of the enable. While the Enable input is in the HIGH state, a change in the information present at the Data inputs does not affect the output information.

### LEAD NAMES

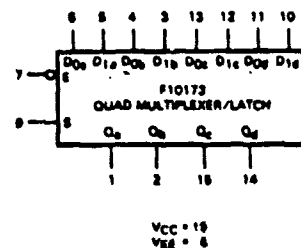
$S$	Data Select
$D_n$	Data Inputs
$\bar{E}$	Enable (Active LOW)
$Q_n$	Outputs

### LOGIC DIAGRAM

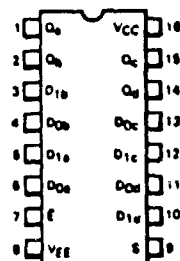


Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

### LOGIC SYMBOL



### CONNECTION DIAGRAM DIP (TOP VIEW)



### TRUTH TABLE

S	$\bar{E}$	$Q_{n+1}$
H	L	$D_{0a}$
L	L	$D_{1a}$
X	H	$Q_n$

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Don't Care

## FAIRCHILD ECL DATA SHEET • F10173

DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$V_{OH}$	Output Voltage HIGH	-1000		-840	mV	0°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table  Loading is 50 $\Omega$ to -2.0 V
		-960		-810		25°C	
		-900		-720		75°C	
$V_{OL}$	Output Voltage LOW	-1870		-1665	mV	0°C	
		-1850		-1650		25°C	
		-1830		-1625		75°C	
$V_{OHC}$	Output Voltage HIGH	-1020			mV	0°C	
		-980				25°C	
		-920				75°C	
$V_{OLC}$	Output Voltage LOW			-1645	mV	0°C	
				-1630		25°C	
				-1605		75°C	
$V_{IH}$	Input Voltage HIGH	-1145		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		-1105		-810		25°C	
		-1045		-720		75°C	
$V_{IL}$	Input Voltage LOW	-1870		-1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		-1850		-1475		25°C	
		-1830		-1450		75°C	
$I_{IH}$	Input Current HIGH Enable and Select Data			245 290	$\mu\text{A}$	25°C	$V_{IN} = V_{IHA}$
$I_{IL}$	Input Current LOW	0.5			$\mu\text{A}$	25°C	$V_{IN} = V_{ILB}$
$I_{EE}$	Power Supply Current	-66			mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PLH}$	Propagation Delay Enable to Output		4.5		ns	
$t_{PHL}$	Propagation Delay Data to Output		2.5		ns	
$t_{PLH}$	Propagation Delay Select to Output		3.5		ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)		2.0		ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)		2.0		ns	
$t_s$	Set-Up Time Data Select		1.5		ns	
			2.5			
$t_h$	Hold Time Data Select		0.0		ns	
			-0.5			

# F10174

## DUAL MULTIPLEXER

**DESCRIPTION** — The F10174 is a high speed Dual Channel Multiplexer with output enable capability. The Select inputs determine one of four active Data inputs for each multiplexer. When the Enable input is HIGH, both outputs are forced LOW. The Enable is also useful when OR-wiring several multiplexers to achieve additional channel capability.

### LEAD NAMES

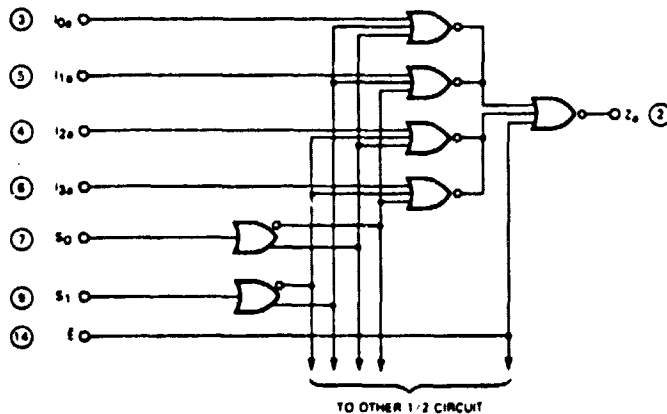
$I_n$	Address Inputs
$\bar{E}$	Enable (Active LOW)
$Z_a$	Outputs
$S_n$	Select Inputs

### TRUTH TABLE

$\bar{E}$	$S_1$	$S_0$	$Z_a$	$Z_b$
H	X	X	L	L
L	L	L	$I_{0a}$	$I_{0b}$
L	L	H	$I_{1a}$	$I_{1b}$
L	H	L	$I_{2a}$	$I_{2b}$
L	H	H	$I_{3a}$	$I_{3b}$

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Don't Care

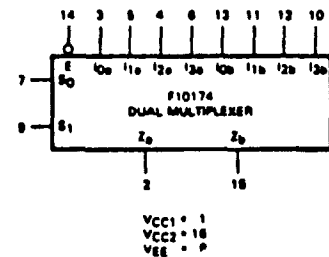
### LOGIC DIAGRAM



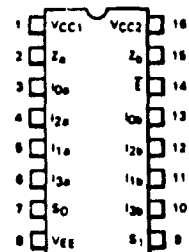
Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

○ = LEAD NUMBERS

### LOGIC SYMBOL



### CONNECTION DIAGRAM DIP (TOP VIEW)



## FAIRCHILD ECL DATA SHEET • F10174

DC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	$T_A$	CONDITIONS
		B	TYP	A			
$V_{OH}$	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C	$V_{IN} = V_{IHA}$ or $V_{ILB}$ per Truth Table  Loading is 50 $\Omega$ to -2.0 V
$V_{OL}$	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C	
$V_{OHC}$	Output Voltage HIGH	-1020 -980 -920			mV	0°C 25°C 75°C	
$V_{OLC}$	Output Voltage LOW			-1645 -1630 -1605	mV	0°C 25°C 75°C	
$V_{IH}$	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
$V_{IL}$	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
$I_{IH}$	Input Current HIGH Data Enable			220 330	$\mu\text{A}$	25°C	$V_{IN} = V_{IHA}$
$I_{IL}$	Input Current LOW	0.5			$\mu\text{A}$	25°C	$V_{IN} = V_{ILB}$
$I_{EE}$	Power Supply Current	-50	-40		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
$t_{PHL}$	Propagation Delay Data to Output	1.5	3.0	4.5	ns	
$t_{PLH}$	Propagation Delay Select to Output	2.0	4.0	6.0	ns	
$t_{PHL}$	Propagation Delay Enable to Output	1.0	2.0	2.9	ns	
$t_{TLH}$	Output Transition Time LOW to HIGH (20% to 80%)	1.5	2.0	3.3	ns	
$t_{THL}$	Output Transition Time HIGH to LOW (80% to 20%)	1.5	2.0	3.3	ns	

# ECL ISOPLANAR MEMORY F10415 / F10415A

## 1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

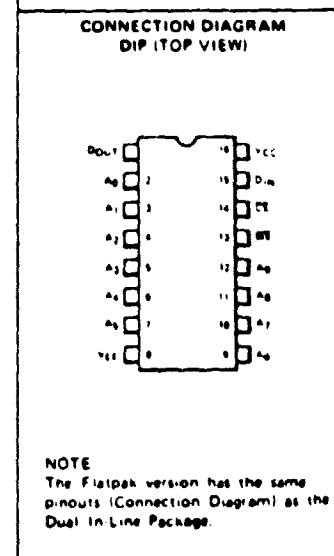
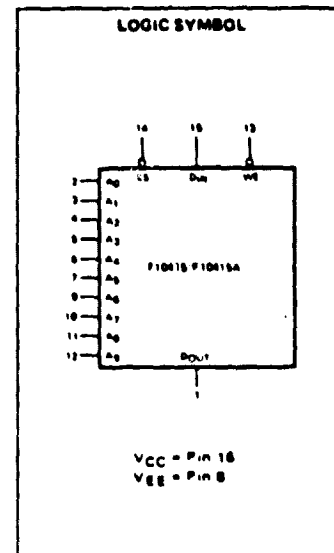
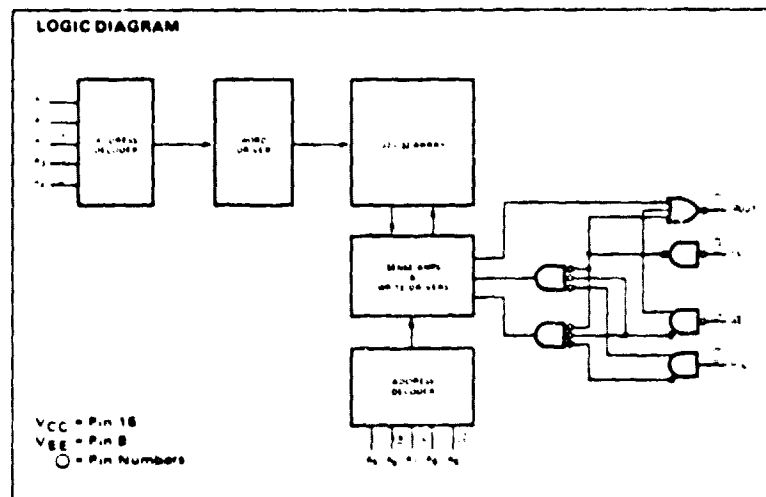
**GENERAL DESCRIPTION** - The F10415 and F10415A are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for high speed scratch pad, control and buffer storage applications. Both include full address decoding on the chip, have separate Data In and non-inverted Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

The F10415 and F10415A are packaged in a hermetic ceramic 16-pin dual in-line package and are specified for operation over the temperature range 0°C to 75°C.

- COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC
- TYPICAL READ ACCESS TIME
  - F10415 - 25 ns
  - F10415A - 12 ns
- TYPICAL CHIP SELECT ACCESS TIME
  - F10415 - 7 ns
  - F10415A - 5 ns
- ORGANIZED 1024 WORDS X 1 BIT
- OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION
- POWER DISSIPATION 0.5 mW/BIT
- POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE

### PIN NAMES

$\overline{CS}$	Chip Select Input
A <sub>0</sub> to A <sub>9</sub>	Address Inputs
D <sub>IN</sub>	Data Input
D <sub>OUT</sub>	Data Output
WE	Write Enable Input





## FAIRCHILD ECL ISOPLANAR MEMORY • F1041B/F1041BA

**FUNCTIONAL DESCRIPTION** - The F1041B and F1041BA are fully decoded 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A<sub>0</sub> to A<sub>9</sub>. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select (CS) from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable (WE). With WE and CS held LOW, the data at D<sub>IN</sub> is written into the addressed location. To read, WE is held HIGH and CS held LOW. Data in the specified location is presented at D<sub>OUT</sub> and is non-inverted.

An unterminated emitter-follower output is provided on the F1041B and F1041BA to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F1041Bs or F1041BAs can be tied together. In other applications the wired-OR is not used. In either case an external 90 Ω pull down resistor to -2 V or an equivalent network must be used to provide a LOW at the output when it is "0".

**ABSOLUTE MAXIMUM RATINGS** (above which the useful life may be impaired)

Storage Temperature	-55°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V <sub>EE</sub> Pin Potential to Ground Pin	-7.0 V to +0.5 V
Input Voltage (dc)	V <sub>EE</sub> to +0.5 V
Output Current (dc Output HIGH)	-30 mA to +0.1 mA

**TABLE 1 - TRUTH TABLE**

INPUTS			OUTPUT		MODE
CS	WE	D <sub>IN</sub>	OPEN EMITTER	D <sub>OUT</sub>	
H	X	X	L	L	NOT SELECTED
L	L	L	L	L	WRITE "0"
L	L	H	L	L	WRITE "1"
L	H	X	L	D <sub>OUT</sub>	READ

L = LOW Voltage Levels = -1.7 V  
 H = HIGH Voltage Levels = -0.9 V  
 (Nominal values)  
 X = Don't Care

**GUARANTEED OPERATING RANGES**

PART NUMBER	SUPPLY VOLTAGE (V <sub>EE</sub> )			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
F1041BDC, F1041BADC	-5.45 V	-5.2 V	-4.94 V	See Note 4 0°C to 75°C

**DC CHARACTERISTICS:** V<sub>EE</sub> = -5.2 V, Output Load = 90 Ω and 20 pF to -2.0 V, T<sub>A</sub> = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T <sub>A</sub>	CONDITIONS
V <sub>OH</sub>	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C +25°C +75°C	V <sub>IN</sub> = V <sub>IHA</sub> or V <sub>ILB</sub>  Loading is 90 Ω to -2.0 V
V <sub>OL</sub>	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C +25°C +75°C	
V <sub>OHc</sub>	Output Voltage HIGH	-1020 -980 -920			mV	0°C +25°C +75°C	
V <sub>OLc</sub>	Output Voltage LOW			-1645 -1630 -1605	mV	0°C +25°C +75°C	V <sub>IN</sub> = V <sub>INH</sub> or V <sub>ILA</sub>
V <sub>IH</sub>	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs
V <sub>IL</sub>	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs
I <sub>IH</sub>	Input Current HIGH			220	μA	0 to +75°C	V <sub>IN</sub> = V <sub>IHA</sub>
I <sub>IL</sub>	Input Current LOW, CS All others	0.5 -80		170	μA	+25°C	V <sub>IN</sub> = V <sub>ILB</sub>
I <sub>EE</sub>	Power Supply Current (Pin 8)	-150	-90		mA	+75°C 0°C	All Inputs and Outputs Open

**NOTES**

- 1 Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.
- 2 The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
- 3 Typical values are at V<sub>EE</sub> = -5.2 V, T<sub>A</sub> = 25°C and maximum loading.
- 4 Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2 minute warm up period. Typical resistance values of the package are:  
 θ<sub>JA</sub> (Junction to Ambient) = 80°C/Watt (still air)  
 θ<sub>JA</sub> (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)  
 θ<sub>JC</sub> (Junction to Case) = 25°C/Watt
- 5 The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
- 6 **DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET**  
 The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are "A" the value closest to positive infinity, "B" the value closest to negative infinity.

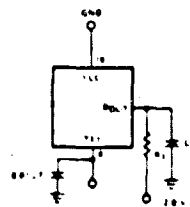
## FAIRCHILD ECL ISOPLANAR MEMORY • F10415/F10415A

AC CHARACTERISTICS:  $V_{EE} = -5.2 \text{ V} \pm 5\%$ , Output Load =  $50 \Omega$ ,  $30 \text{ pF}$  to  $-2.0 \text{ V}$ ,  $T_A = 0^\circ\text{C}$  to  $75^\circ\text{C}$

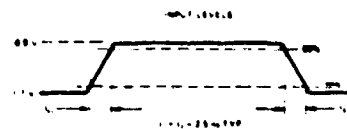
SYMBOL	PARAMETER	F10415ADC*			F10415DC			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
<b>READ MODE</b>									
t <sub>ACS</sub>	Chip Select Access Time		5			7	10	ns	Fig 1a & b measured at 50% of input and output (V <sub>IL</sub> for VOL or V <sub>IH</sub> for VOH)
t <sub>RCS</sub>	Chip Select Recovery Time		5			7	10	ns	
t <sub>AA</sub>	Address Access Time		12	20		25	35	ns	
<b>WRITE MODE</b>									
t <sub>W</sub>	Write Pulse Width (to Guarantee writing)	12	9		25	20		ns	F10415A t <sub>WSA</sub> = 8 ns F10415 t <sub>WSA</sub> = 20 ns
t <sub>WSD</sub>	Data Set-up Time Prior to Write		0		5	0		ns	
t <sub>WHD</sub>	Data Hold Time After Write		0		5	0		ns	
t <sub>WSA</sub>	Address Set-up Time Prior to Write		5		8	5		ns	F10415A t <sub>W</sub> = 12 ns F10415 t <sub>W</sub> = 25 ns
t <sub>WHA</sub>	Address Hold Time After Write		0		4	1		ns	
t <sub>WCS</sub>	Chip Select Set-up Time Prior to Write		0		5	0		ns	Fig 2 measured at 50% of input to valid output (V <sub>IL</sub> for VOL or V <sub>IH</sub> for VOH)
t <sub>WHCS</sub>	Chip Select Hold Time After Write		0		5	0		ns	
t <sub>WS</sub>	Write Disable Time		5			7	10	ns	
t <sub>WR</sub>	Write Recovery Time		7			7	10	ns	
<b>RISE TIME AND FALL TIME</b>									
t <sub>r</sub>	Output Rise Time		5			5		ns	Measured between 20% and 80% points (Fig 1a)
t <sub>f</sub>	Output Fall Time		5			5		ns	
<b>CAPACITANCE</b>									
C <sub>IN</sub>	Input Pin Capacitance		4	5		4	5	pF	Measure with a Pulse Technique
C <sub>OUT</sub>	Output Pin Capacitance		7	8		7	8	pF	

\*Note: The F10415A AC limits are preliminary.

### LOADING CONDITIONS



### INPUT LEVELS

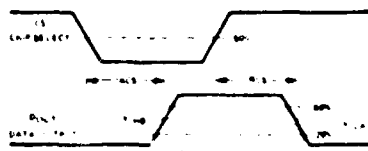


All Timing Measurements Referenced to 50% of Input Levels

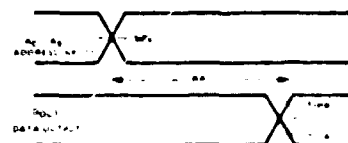
C<sub>L</sub> = 30 pF including Jig and Stray Capacitance

R<sub>T</sub> = 50 Ω Termination of Scope

### READ MODE PROPAGATION DELAY FROM CHIP SELECT

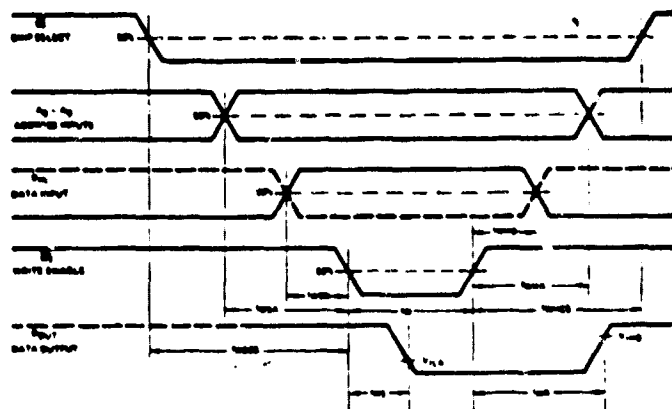


### READ MODE PROPAGATION DELAY FROM ADDRESS



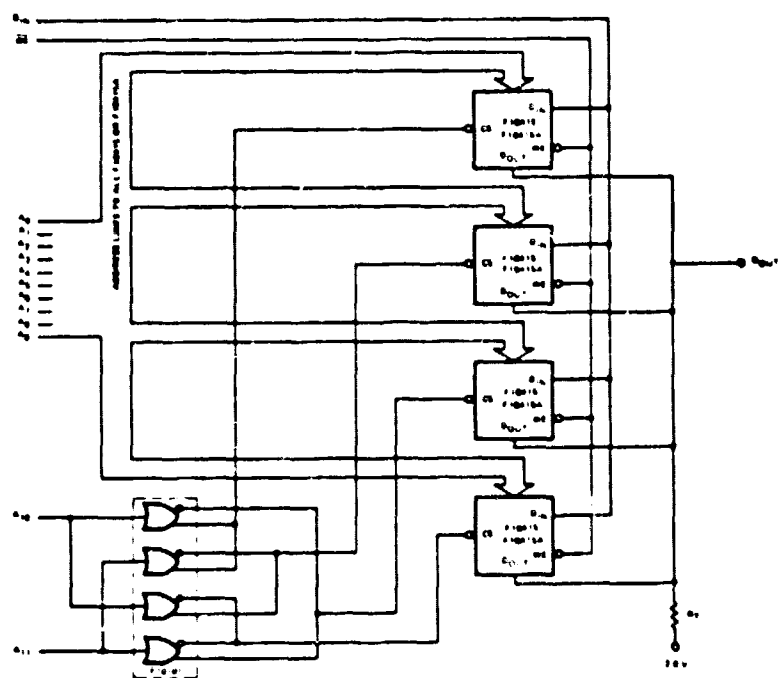
FAIRCHILD ECL ISOPLANAR MEMORY • F10415/F10415A

WRITE MODE



NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

APPLICATIONS

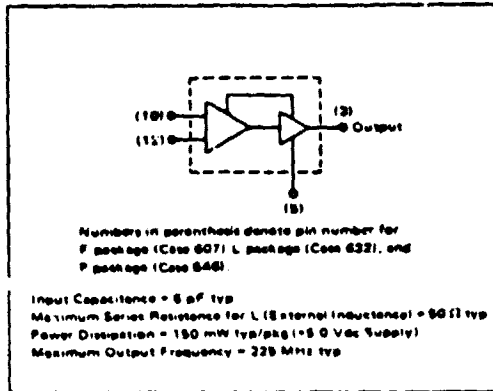


4096-WORD X 1-BIT SYSTEM

VOLTAGE-CONTROLLED  
OSCILLATOR

MECL III MC1600 series

MC1648



The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity (See Figure 2).

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply depending upon system requirements.

SUPPLY VOLTAGE	GND PIN	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 - CIRCUIT SCHEMATIC

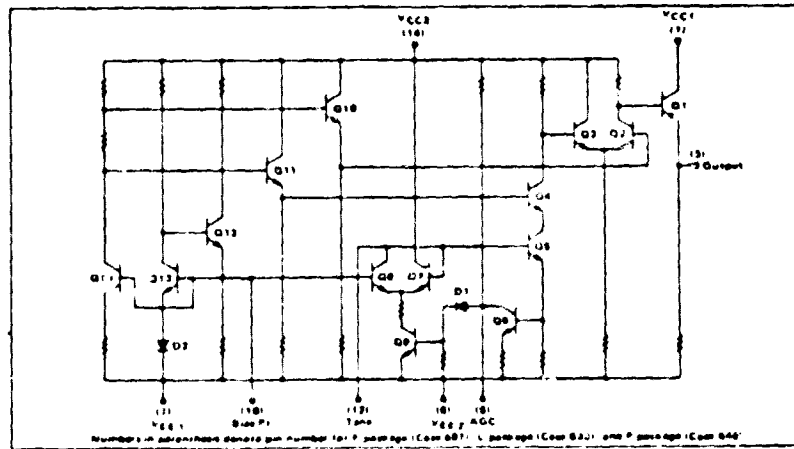
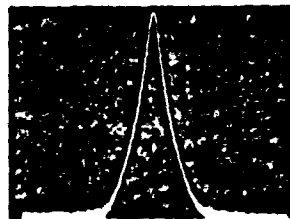
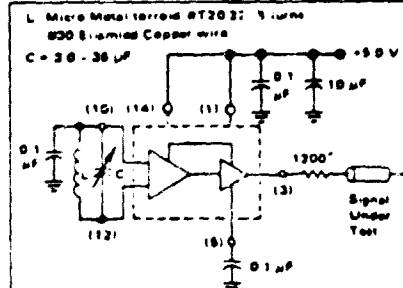


FIGURE 2 - SPECTRAL PURITY OF SIGNAL AT OUTPUT



BW = 10 kHz Scan Width = 50 kHz/div  
Center Frequency = 100 MHz Vertical Scale = 10 dB/div

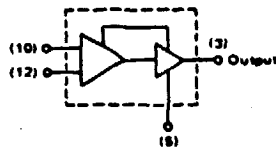


\*The 1200 ohm resistor and the scope terminating 100 ohm impedance contribute a 25:1 attenuator probe. Loss shall be CT 07382 or equivalent.

# MC1648 (continued)

## ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts

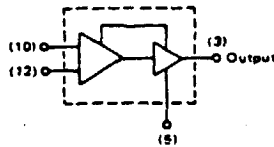


Characteristics	Symbol	Pin Number	MC1648 Test Limits										TEST VOLTAGE-CURRENT VALUES				V <sub>CC</sub> (V <sub>DD</sub> )
			-30°C		+25°C		+50°C		Unit	TEST VOLTAGE-CURRENT APPLIED TO PINS LISTED BELOW							
			Min	Max	Min	Max	Min	Max		V <sub>OH</sub> max	V <sub>OL</sub> min	V <sub>CC</sub>	I <sub>L</sub>				
Power Supply Drain Current	I <sub>S</sub>	8	—	—	—	—	—	—	—	—	—	—	—	1.14	—	7.0	
Logic 1 Output Voltage	V <sub>OH</sub>	3	2.94	4.10	4.84	4.25	4.11	4.20	—	—	—	—	—	12	1.14	3	7.0
Logic 0 Output Voltage	V <sub>OL</sub>	3	2.18	3.40	2.30	2.43	2.22	3.40	—	—	—	—	—	1.14	3	7.0	
Bus Voltage	V <sub>Bus</sub>	10	1.51	1.55	1.40	1.70	1.20	1.50	—	—	—	—	—	1.14	—	7.0	
Peak-to-Peak Jitter Voltage	V <sub>Jp-p</sub>	12	—	—	—	—	—	—	—	—	—	—	—	1.14	3	7.0	
Output Duty Cycle	V <sub>DC</sub>	2	—	—	—	—	—	—	—	—	—	—	—	1.14	3	7.0	
Distortion Frequency	f <sub>max</sub>	—	—	—	200	225	—	—	—	—	—	—	—	1.14	3	7.0	

\*The measurement is across the test point for purposes of measuring a resistor having leads at this point.

## ELECTRICAL CHARACTERISTICS

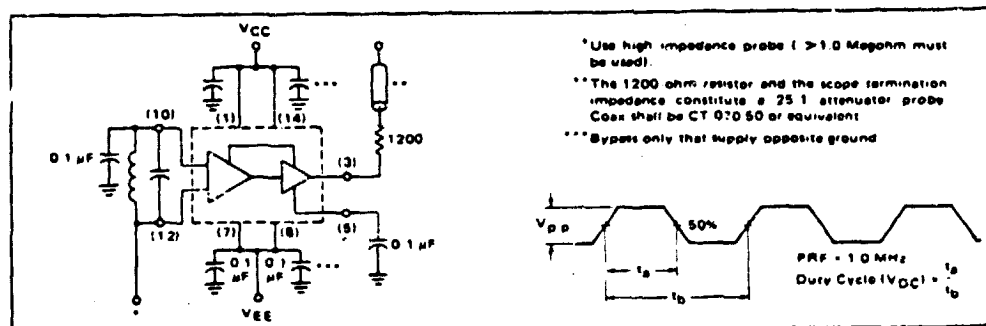
Supply Voltage = -5.2 volts



Characteristics	Symbol	Pin Number	MC1648 Test Limits										TEST VOLTAGE-CURRENT VALUES				V <sub>CC</sub> (V <sub>DD</sub> )
			-30°C		+25°C		+50°C		Unit	TEST VOLTAGE-CURRENT APPLIED TO PINS LISTED BELOW							
			Min	Max	Min	Max	Min	Max		V <sub>OH</sub> max	V <sub>OL</sub> min	V <sub>CC</sub>	I <sub>L</sub>				
Power Supply Drain Current	I <sub>S</sub>	8	—	—	—	—	—	—	—	—	—	—	—	7.0	—	1.14	
Logic 1 Output Voltage	V <sub>OH</sub>	3	-1.040	-0.815	-0.660	-0.730	-0.600	-0.600	—	—	—	—	—	12	7.0	3	1.14
Logic 0 Output Voltage	V <sub>OL</sub>	3	-1.000	-1.000	-1.000	-1.020	-1.020	-1.075	—	—	—	—	—	7.0	3	1.14	
Bus Voltage	V <sub>Bus</sub>	10	-3.000	-3.200	-3.000	-3.000	-3.020	-3.020	—	—	—	—	—	7.0	—	1.14	
Peak-to-Peak Jitter Voltage	V <sub>Jp-p</sub>	12	—	—	—	—	—	—	—	—	—	—	—	7.0	3	1.14	
Output Duty Cycle	V <sub>DC</sub>	2	—	—	—	—	—	—	—	—	—	—	—	7.0	3	1.14	
Distortion Frequency	f <sub>max</sub>	—	—	—	200	225	—	—	—	—	—	—	—	7.0	3	1.14	

\*The measurement is across the test point for purposes of measuring a resistor having leads at this point.

FIGURE 3 - TEST CIRCUIT AND WAVEFORMS



# MC1648 (continued)

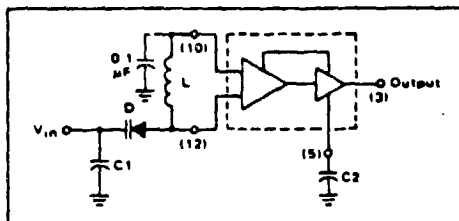
## OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

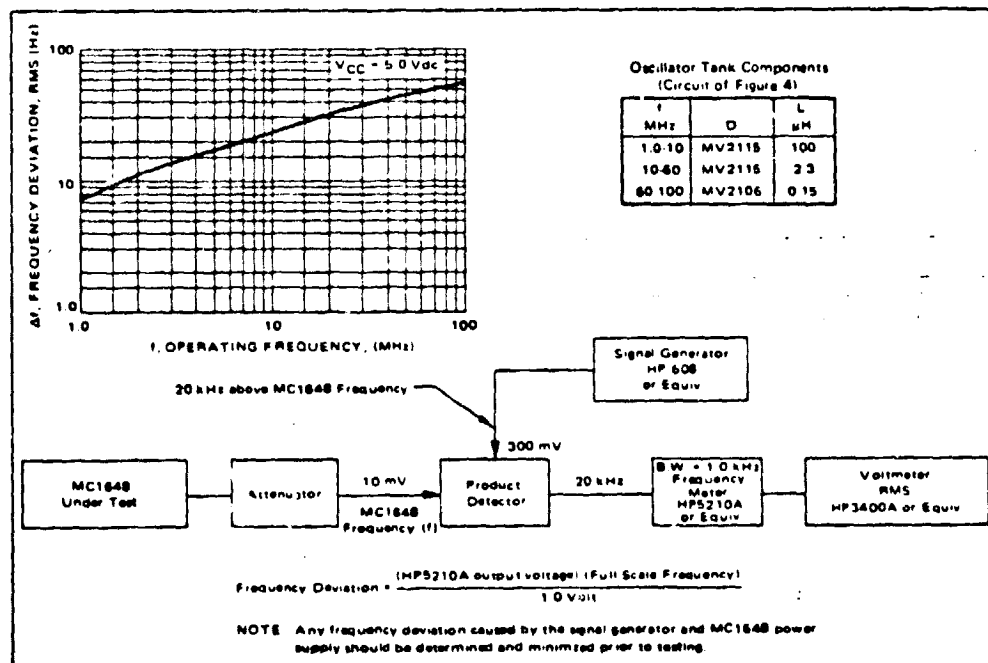
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 VBE above VEE ( $\approx 1.4$  V for positive supply operation).

**FIGURE 4 - THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE**



When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

**FIGURE 5 - NOISE DEVIATION TEST CIRCUIT AND WAVEFORM**



TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE  
USING EXTERNAL VARACTOR DIODE AND COIL.  $T_A = 25^\circ\text{C}$

FIGURE 6

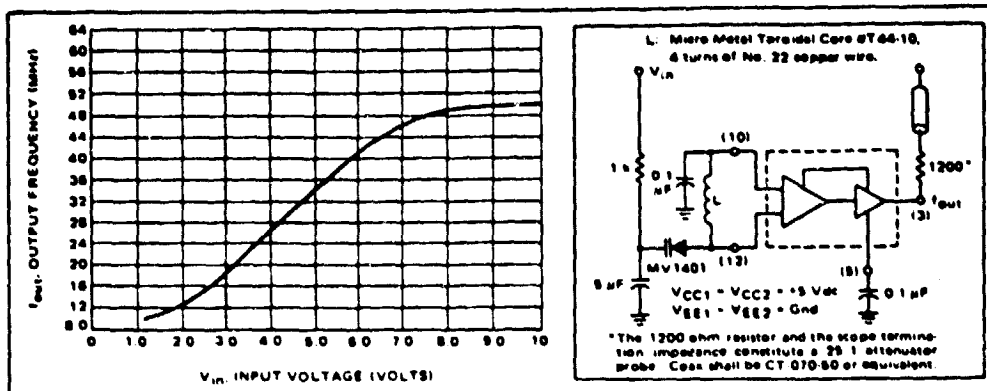


FIGURE 7

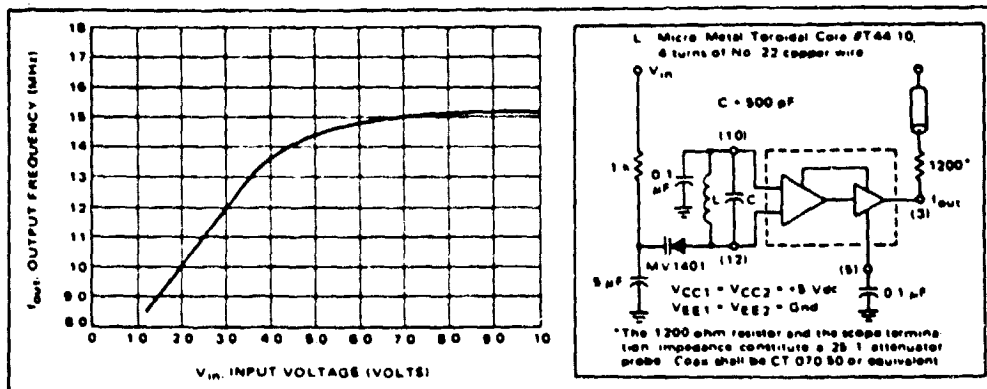
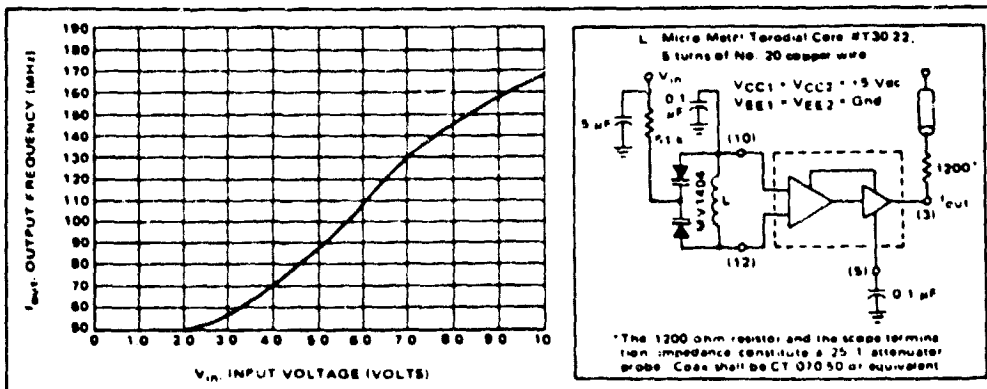


FIGURE 8



## MC1648 (continued)

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 k $\Omega$  resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 k $\Omega$ ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{\max}}{f_{\min}} = \frac{\sqrt{C_D(\max) + C_S}}{\sqrt{C_D(\min) + C_S}}$$

$$\text{where } f_{\min} = \frac{1}{2\pi \sqrt{L(C_D(\max) + C_S)}}$$

$C_S$  = shunt capacitance (input plus external capacitance).

$C_D$  = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1  $\mu$ F capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the MC1648. This is accomplished by tying a series resistor (1 k $\Omega$  minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

## APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (pref-

erable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter,  $f_{\text{out}} = Nf_{\text{ref}}$ . The channel spacing is equal to frequency ( $f_{\text{ref}}$ ).

For additional information on applications and designs for phase locked loops and digital frequency synthesizers, see Motorola Application Notes AN532A, AN 535, AN553, AN 564, AN 594, or Phase Locked Loop Systems Data Book.



PHASE-FREQUENCY  
DETECTOR

MECL Phase-Locked Loop Components

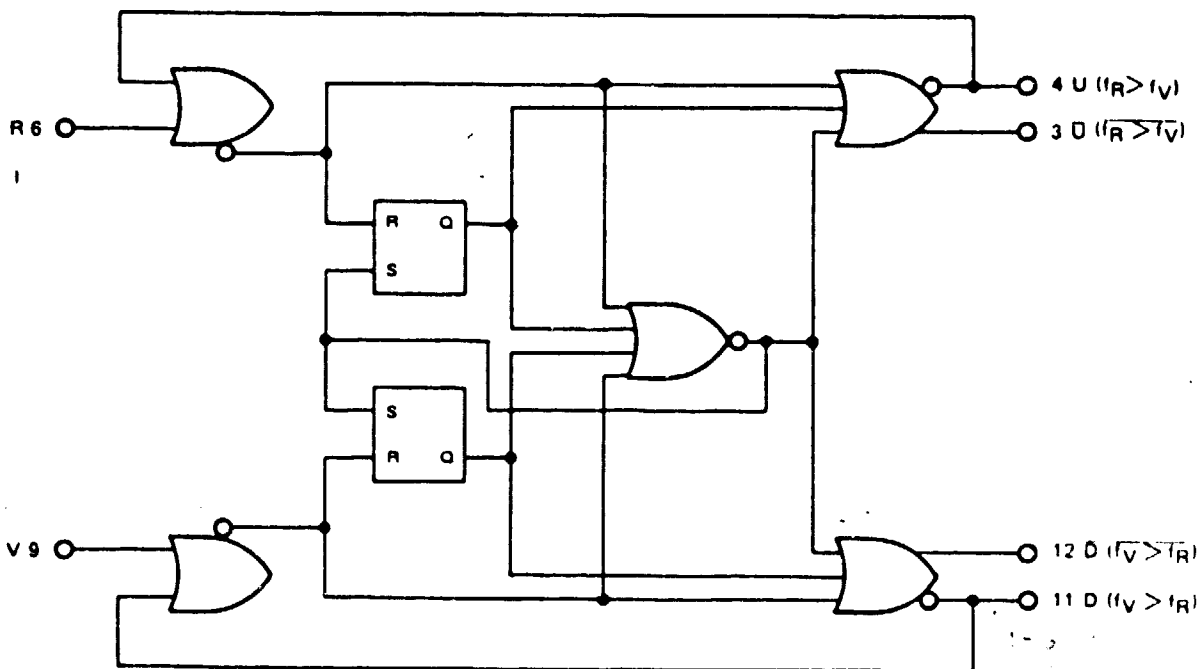
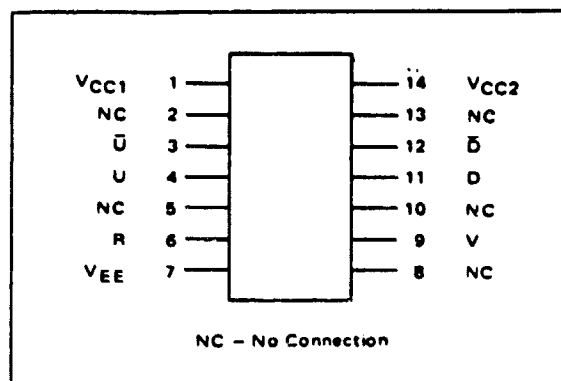
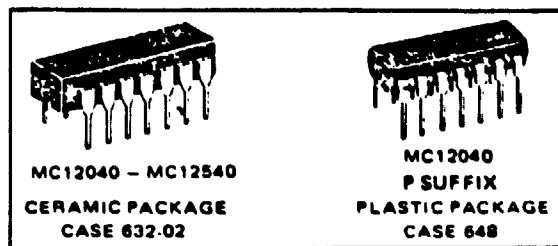
MOTOROLA (AA)

MC12040 • MC12540

ISSUE C

The MC12040/MC12540 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is very similar to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

- Operating Frequency = 70 MHz Min. -55° to +125°C

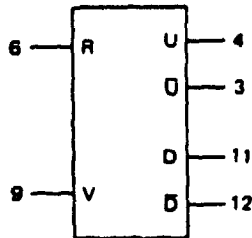


VCC1 = Pin 1  
VCC2 = Pin 14  
VCC3 = Pin 7

# MC12040 • MC12540

## ELECTRICAL CHARACTERISTICS - MC12040

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



INPUT		OUTPUT			
R	V	U	D	D	D
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	1	1	0
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = Don't Care

## TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

Supply Voltage = -5.2V

TEST VOLTAGE VALUES				
(Volts)				
V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>ILA</sub> max	V <sub>EE</sub>
-0.840	-1.870	-1.145	-1.490	-5.2
-0.810	-1.850	-1.105	-1.475	-5.2
-0.720	-1.830	-1.045	-1.450	-5.2

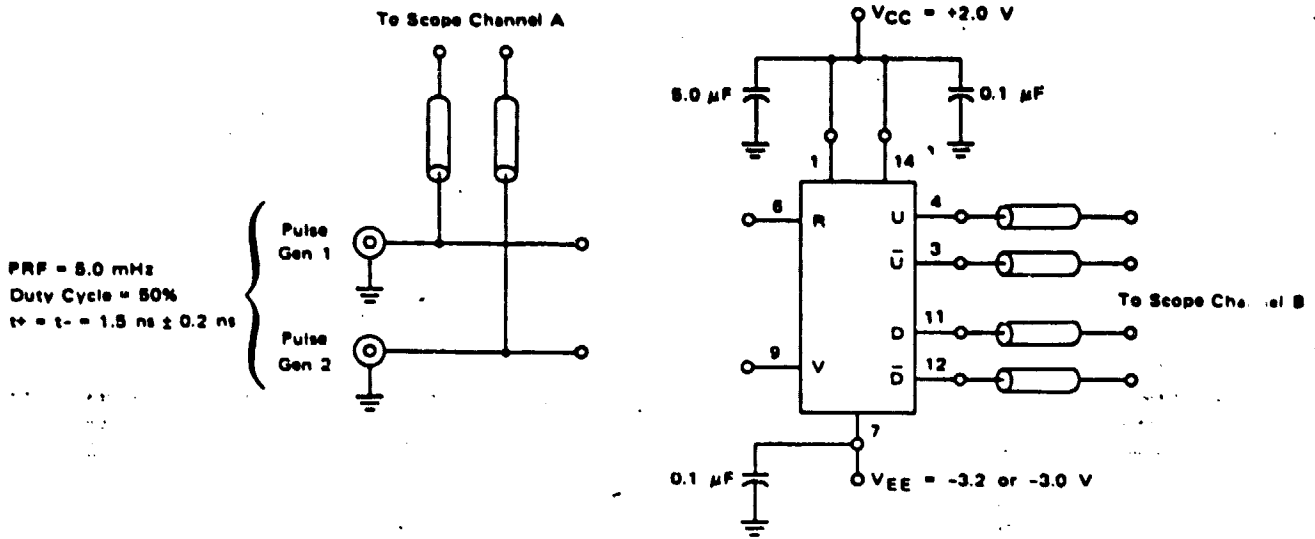
Characteristic	Symbol	Pin Under Test	MC12040						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					V <sub>CC</sub> (V <sub>EE</sub> ) Gnd
			0°C		25°C		-75°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>ILA</sub> max	V <sub>EE</sub>	
			Min	Max	Min	Max	Min	Max							
Power Supply Drain Current	I <sub>E</sub>	7	-	-	-120	-60	-	-	-	-	-	-	7	1.14	
Input Current	I <sub>INH</sub>	6	-	-	-	350	-	-	6	-	-	-	-	7	1.14
		9	-	-	-	350	-	-	9	-	-	-	-	7	1.14
Logic "1" Output Voltage	V <sub>OH</sub> ①	3	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	V <sub>dc</sub>	-	-	-	-	7	1.14
		4	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		11	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		12	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
Logic "0" Output Voltage	V <sub>OL</sub> ①	3	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	V <sub>dc</sub>	-	-	-	-	7	1.14
		4	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		11	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		12	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
Logic "1" Threshold Voltage	V <sub>OHA</sub> ②	3	-1.020	-	-0.980	-	-0.920	-	V <sub>dc</sub>	-	-	6.9	-	7	1.14
		4	↓	-	↓	-	↓	-	↓	-	-	↓	-	↓	↓
		11	↓	-	↓	-	↓	-	↓	-	-	↓	-	↓	↓
		12	↓	-	↓	-	↓	-	↓	-	-	↓	-	↓	↓
Logic "0" Threshold Voltage	V <sub>OLA</sub> ②	3	-	-1.615	-	-1.600	-	-1.575	V <sub>dc</sub>	-	-	9	6	7	1.14
		4	-	↓	-	↓	-	↓	↓	-	-	6	9	↓	↓
		11	-	↓	-	↓	-	↓	↓	-	-	9	6	↓	↓
		12	-	↓	-	↓	-	↓	↓	-	-	6	9	↓	↓

Supply Voltage = +5.0V

TEST VOLTAGE VALUES				
(Volts)				
V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>ILA</sub> max	V <sub>CC</sub>
+4.160	+3.130	+3.855	+3.510	+5.0
+4.190	+3.150	+3.895	+3.525	+5.0
+4.280	+3.170	+3.955	+3.550	+5.0

Characteristic	Symbol	Pin Under Test	MC12040						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					V <sub>CC</sub> (V <sub>EE</sub> ) Gnd
			0°C		25°C		-75°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>ILA</sub> max	V <sub>CC</sub>	
			Min	Max	Min	Max	Min	Max							
Power Supply Drain Current	I <sub>E</sub>	7	-	-	-115	-60	-	-	-	-	-	-	1.14	7	
Input Current	I <sub>INH</sub>	6	-	-	-	350	-	-	6	-	-	-	-	1.14	7
		9	-	-	-	350	-	-	9	-	-	-	-	1.14	7
Logic "1" Output Voltage	V <sub>OH</sub> ①	3	4.000	4.160	4.040	4.190	4.100	4.280	V <sub>dc</sub>	-	-	-	-	1.14	7
		4	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		11	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		12	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
Logic "0" Output Voltage	V <sub>OL</sub> ①	3	3.190	3.430	3.210	3.440	3.230	3.470	V <sub>dc</sub>	-	-	-	-	1.14	7
		4	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		11	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
		12	↓	↓	↓	↓	↓	↓	↓	-	-	-	-	↓	↓
Logic "1" Threshold Voltage	V <sub>OHA</sub> ②	3	3.980	-	4.020	-	4.080	-	V <sub>dc</sub>	-	-	6.9	-	1.14	7
		4	↓	-	↓	-	↓	-	↓	-	-	↓	-	↓	↓
		11	↓	-	↓	-	↓	-	↓	-	-	↓	-	↓	↓
		12	↓	-	↓	-	↓	-	↓	-	-	↓	-	↓	↓
Logic "0" Threshold Voltage	V <sub>OLA</sub> ②	3	-	3.450	-	3.460	-	3.490	V <sub>dc</sub>	-	-	9	6	1.14	7
		4	-	↓	-	↓	-	↓	↓	-	-	6	9	↓	↓
		11	-	↓	-	↓	-	↓	↓	-	-	9	6	↓	↓
		12	-	↓	-	↓	-	↓	↓	-	-	6	9	↓	↓

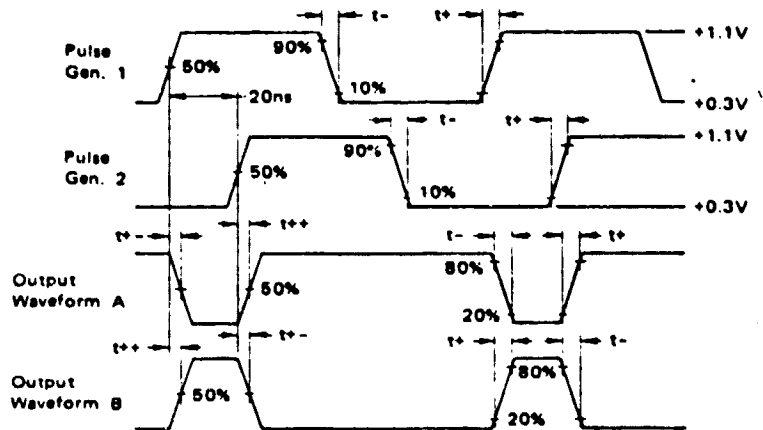
AC TESTS



PRF = 8.0 MHz  
Duty Cycle = 50%  
 $t_r = t_f = 1.5 \text{ ns} \pm 0.2 \text{ ns}$

NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω (MC12040) and 100 Ω (MC12540) resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 8 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040			MC12540			Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW			
				0°C	+25°C	+75°C	-55°C	+25°C	+125°C		Pulse Gen. 1	Pulse Gen. 2	VEE -3.0 or -3.2 V	VCC +2.0 V
				Max	Max	Max	Max	Max	Max					
Propagation Delay	16+4+	6 4	B	46	46	56	46	46	50	ns	6	9	7	1.14
	16+12+	6 12	A	60	60	72	60	60	66	↓	9	6	↓	↓
	16+3-	6 3	A	45	45	55	45	45	49	↓	6	9	↓	↓
	16+11-	6 11	B	64	64	77	64	64	70	↓	9	6	↓	↓
	19+11+	9 11	B	46	46	56	46	46	50	↓	9	6	↓	↓
	19+3+	9 3	A	60	60	72	60	60	66	↓	6	9	↓	↓
Output Rise Time	13-	3	A	34	34	38	34	34	38	ns	6	9	7	1.14
	14-	4	B	↓	↓	↓	↓	↓	↓	↓	6	9	↓	↓
	111+	11	B	↓	↓	↓	↓	↓	↓	↓	9	6	↓	↓
Output Fall Time	13-	3	A	34	34	38	34	34	38	ns	6	9	7	1.14
	14-	4	B	↓	↓	↓	↓	↓	↓	↓	6	9	↓	↓
	111-	11	B	↓	↓	↓	↓	↓	↓	↓	9	6	↓	↓

## APPLICATIONS INFORMATION

The MC12040/MC12540 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase

detector (U and D). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The U and D outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering embedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040/MC12540 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4344/MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of  $0.016/0.16 = 0.1$  radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 1 — TIMING DIAGRAM

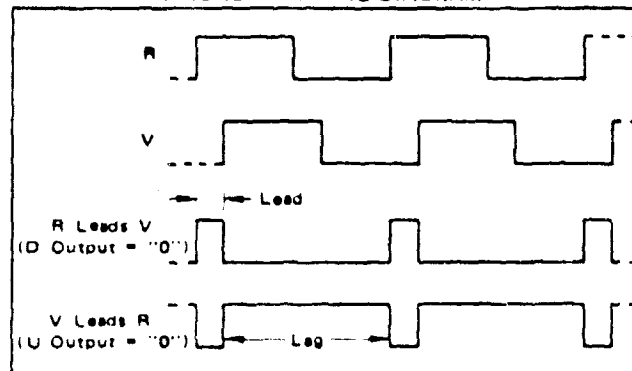
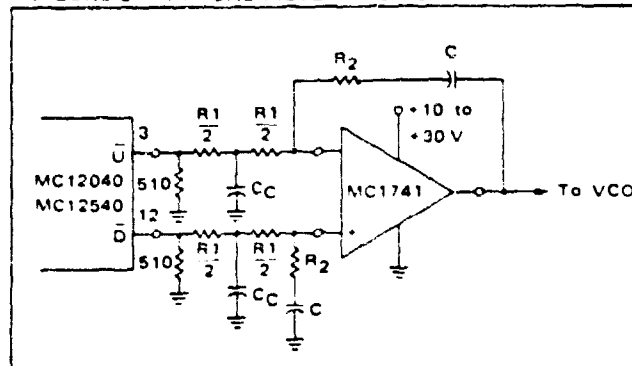


FIGURE 2 — TYPICAL FILTER AND SUMMING NETWORK



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

# Am687-Am687A

## Dual Voltage Comparators

### Distinctive Characteristics

- 8.0ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary ECL outputs
- 50Ω line driving capability

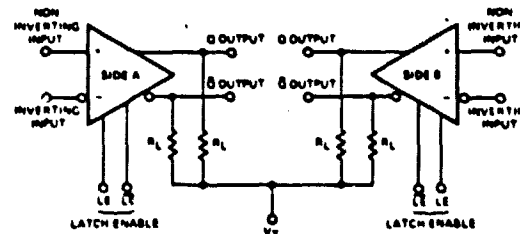
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assembly of hybrid products.
- Available in the hermetic dual-in-line package.

### FUNCTIONAL DESCRIPTION

The Am687 and Am687A are fast dual voltage comparators constructed on a single silicon chip with an advanced high-frequency process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

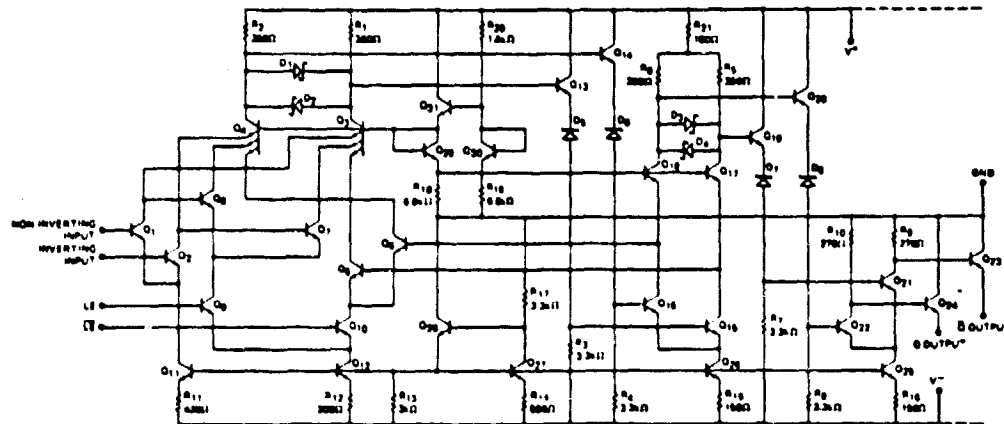
The comparators are similar to the Am685 high-speed comparator but have been designed to operate from a 5V positive supply (instead of 6V), dissipating less power than two Am685's. Separate latch functions are provided to allow each comparator to be independently used in a sample-and-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and  $\overline{LE}$  is LOW, the comparator functions normally. When LE is driven LOW and  $\overline{LE}$  is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

### FUNCTIONAL DIAGRAM



The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50-200Ω connected to -2.0V, or 200-2000Ω connected to -5.2V.

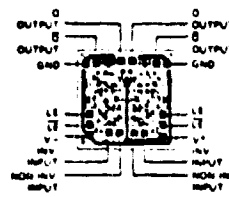
### CIRCUIT DIAGRAM (Each Comparator)



### ORDERING INFORMATION

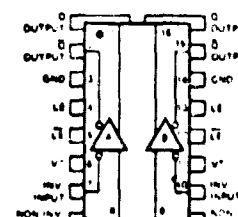
Part Number	Package Type	Temperature Range	Order Number
Am687A	DIP	-30°C to +85°C	AM687ADL
Am687A	DIP	-55°C to +125°C	AM687ADM
Am687	DIP	-30°C to +85°C	AM687DL
Am687	DIP	-55°C to +125°C	AM687DM
Am687	Dice	-30°C to +85°C	AM687XL
Am687	Dice	-55°C to +125°C	AM687XM

### METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.056"

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orient.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V	Operating Temperature Range	
Negative Supply Voltage	-7 V	Am687-L, Am687A-L	-30°C to +85°C
Input Voltage	±4 V	Am687-M, Am687A-M	-55°C to +125°C
Reference Input Voltage	±8 V	Storage Temperature Range	-65°C to +150°C
Input Current	30 mA	Lead Temperature (Soldering, 60 Sec.)	300°C
Power Dissipation (Note 2)	600 mW	Minimum Operating Voltage ( $V^+$ to $V^-$ )	0.7 V

## ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics Symbol	Parameter	Conditions (Note 3)	Am687A-L		Am687A-M		Units
			Min.	Max.	Min.	Max.	
$V_{OS}$	Input Offset Voltage	$R_S < 100 \Omega, T_A = 25^\circ\text{C}$	-3.0	+3.0	-2.0	+2.0	mV
		$R_S < 100 \Omega$	-3.5	+3.5	-3.0	+3.0	mV
$\Delta V_{OS}$	Average Temperature Coefficient of Input Offset Voltage	$R_S < 100 \Omega$	-10	+10	-10	+10	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current	$25^\circ\text{C} < T_A < T_{A(\text{max.})}$	-1.0	+1.0	-1.0	+1.0	$\mu\text{A}$
		$T_A = T_{A(\text{min.})}$	-1.3	+1.3	-1.6	+1.6	$\mu\text{A}$
$I_B$	Input Bias Current	$25^\circ\text{C} < T_A < T_{A(\text{max.})}$		10		10	$\mu\text{A}$
		$T_A = T_{A(\text{min.})}$		13		16	$\mu\text{A}$
$V_{CU}$	Input Voltage Range		-3.3	+2.7	-3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S < 100 \Omega, -3.3 < V_{CM} < +2.7\text{V}$	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S < 100 \Omega, \Delta V_S = \pm 5\%$	70		70		dB
$V_{OH}$	Output HIGH Voltage	$T_A = 25^\circ\text{C}$	-0.960	-0.810	-0.960	-0.810	V
		$T_A = T_{A(\text{min.})}$	-1.060	-0.890	-1.100	-0.920	V
		$T_A = T_{A(\text{max.})}$	-0.890	-0.700	-0.850	-0.620	V
$V_{OL}$	Output LOW Voltage	$T_A = 25^\circ\text{C}$	-1.850	-1.650	-1.850	-1.650	V
		$T_A = T_{A(\text{min.})}$	-1.890	-1.675	-1.910	-1.690	V
		$T_A = T_{A(\text{max.})}$	-1.625	-1.625	-1.810	-1.575	V
$I^+$	Positive Supply Current		35		32	mA	
$I^-$	Negative Supply Current		48		44	mA	
$P_{D(55)}$	Power Dissipation		485		450	mW	

Switching Characteristics ( $V_{IN} = 100\text{mV}, V_{OD} = 5\text{mV}$ )

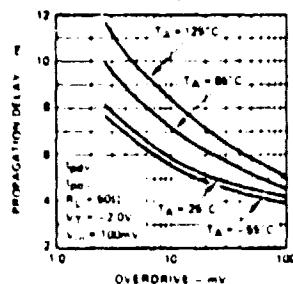
$t_{pd-100}$	Propagation Delay, Am687A	$T_{A(\text{min.})} < T_A < 25^\circ\text{C}$		8.0		8.0	ns
		$T_A = T_{A(\text{max.})}$		10		12.5	ns
$t_{pd-10}$	Propagation Delay, Am687	$T_{A(\text{min.})} < T_A < 25^\circ\text{C}$		10		10	ns
		$T_A = T_{A(\text{max.})}$		14		20	ns
$t_{L(1)}$	Minimum Latch Set-up Time	$T_A = 25^\circ\text{C}$		4.0		4.0	ns

Note 2: Operate at 80mW for operation at ambient temperatures above +115°C

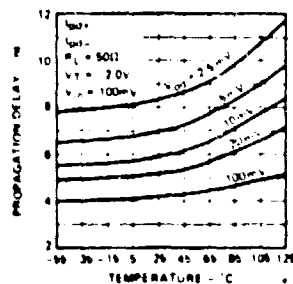
Note 3: Unless otherwise specified  $V^+ = +5.0\text{V}$ ,  $V^- = -5.2\text{V}$ ,  $V_T = -2.0\text{V}$  and  $R_L = 80\Omega$  all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for  $V_{OS}$ ,  $I_{OS}$ ,  $I_B$ , CMRR, SVRR,  $I_{pd}$ , and  $I_{pd-}$  apply over the full  $V_{CM}$  range and for 15% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFM or greater.

## PERFORMANCE CURVES

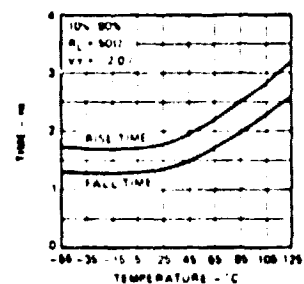
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature



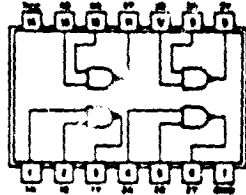
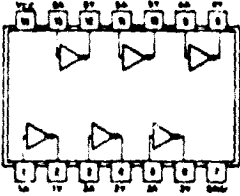
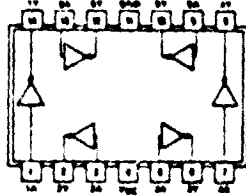
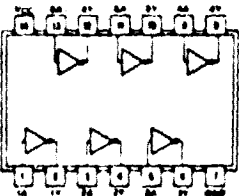
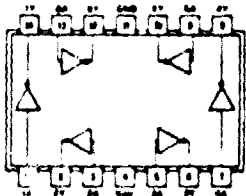
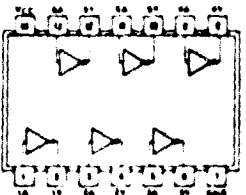
Output Rise and Fall Times as a Function of Temperature



2. TTL COMPONENT DATA

## 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

### PIN ASSIGNMENTS (TOP VIEWS)

<p><b>QUADRUPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS</b></p> <p><b>03</b></p> <p>positive logic: <math>Y = \overline{ABC}</math></p> <p>See page 6-4</p>	 <p>SN5403 (J)      SN7403 (J, N)  SN54L03 (J)    SN74L03 (J, N)  SN54LS03 (J, W) SN74LS03 (J, N)  SN5403 (J, W)   SN7403 (J, N)</p>
<p><b>HEX INVERTERS</b></p> <p><b>04</b></p> <p>positive logic: <math>Y = \overline{A}</math></p> <p>See page 6-2</p>	 <p>SN5404 (J)      SN7404 (J, N)  SN54M04 (J)    SN74M04 (J, N)  SN54L04 (J)    SN74L04 (J, N)  SN54LS04 (J, W) SN74LS04 (J, N)  SN54S04 (J, W) SN74S04 (J, N)</p>  <p>SN5404 (W)      SN54M04 (W)  SN54L04 (T)</p>
<p><b>HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS</b></p> <p><b>05</b></p> <p>positive logic: <math>Y = \overline{A}</math></p> <p>See page 6-4</p>	 <p>SN5405 (J)      SN7405 (J, N)  SN54M05 (J)    SN74M05 (J, N)  SN54LS05 (J, W) SN74LS05 (J, N)  SN54S05 (J, W) SN74S05 (J, N)</p>  <p>SN5405 (W)      SN54M05 (W)</p>
<p><b>HEX INVERTER BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS</b></p> <p><b>06</b></p> <p>positive logic: <math>Y = \overline{A}</math></p> <p>See page 6-24</p>	 <p>SN5406 (J, W)    SN7406 (J, N)</p>



## 64/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

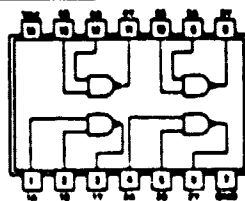
### PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT  
POSITIVE-NAND GATES

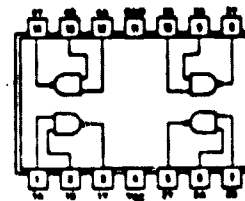
00

positive logic:  
 $Y = \overline{AB}$

See page 6-2



SN5400 (J) SN7400 (J, N)  
SN5400D (J) SN7400D (J, N)  
SN54L00 (J) SN74L00 (J, N)  
SN54L00D (J, W) SN74L00D (J, N)  
SN54000 (J, W) SN74000 (J, N)



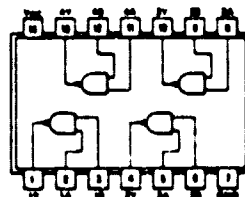
SN5400 (W)  
SN54L00 (T)

QUADRUPLE 2-INPUT  
POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS

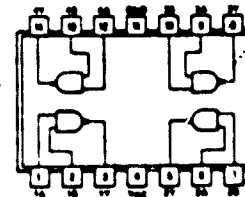
01

positive logic:  
 $Y = \overline{AB}$

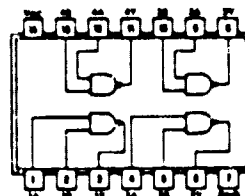
See page 6-4



SN5401 (J) SN7401 (J, N)  
SN54L01 (J, W) SN74L01 (J, N)



SN5401 (W)  
SN54L01 (T)



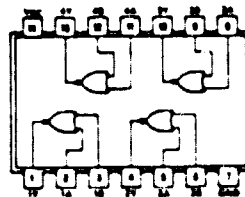
SN5401 (J) SN7401 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-NOR GATES

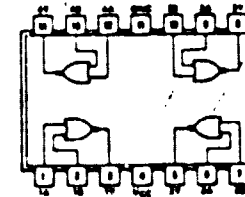
02

positive logic:  
 $Y = \overline{A+B}$

See page 6-6



SN5402 (J) SN7402 (J, N)  
SN54L02 (J) SN74L02 (J, N)  
SN54L02D (J, W) SN74L02D (J, N)  
SN54S02 (J, W) SN74S02 (J, N)



SN5402 (W)  
SN54L02 (T)

## 64/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

### PIN ASSIGNMENTS (TOP VIEWS)

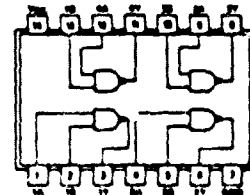
QUADRUPLE 2-INPUT  
HIGH-VOLTAGE INTERFACE  
POSITIVE-NAND GATES

26

positive logic:

$$Y = A \cdot B$$

See page 6-24 and 6-26



SN6426 (J) SN7426 (J, N)  
SN64LS26 (J, W) SN74LS26 (J, N)

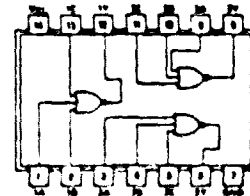
TRIPLE 3-INPUT  
POSITIVE-NOR GATES

27

positive logic:

$$Y = \overline{A+B+C}$$

See page 6-8



SN6427 (J, W) SN7427 (J, N)  
SN64LS27 (J, W) SN74LS27 (J, N)

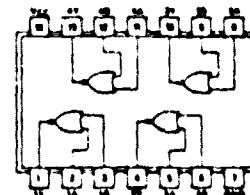
QUADRUPLE 2-INPUT  
POSITIVE-NOR BUFFERS

28

positive logic:

$$Y = \overline{A+B}$$

See page 6-20



SN6428 (J, W) SN7428 (J, N)  
SN64LS28 (J, W) SN74LS28 (J, N)

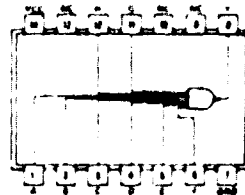
8-INPUT  
POSITIVE-NAND GATES

30

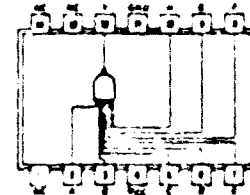
positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

See page 6-2



SN6430 (J) SN7430 (J, N)  
SN64H30 (J) SN74H30 (J, N)  
SN64L30 (J) SN74L30 (J, N)  
SN64LS30 (J, W) SN74LS30 (J, N)  
SN64S30 (J, W) SN74S30 (J, N)

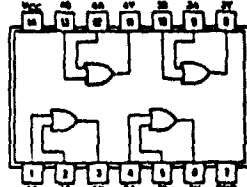
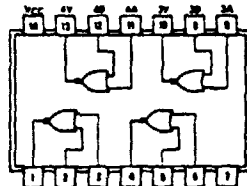
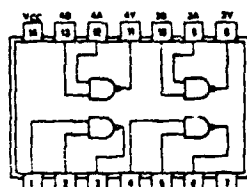
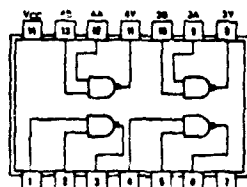


SN6430 (W)  
SN64H30 (W)  
SN64L30 (T)

NC - No internal connection

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

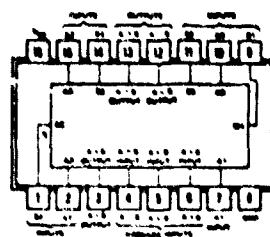
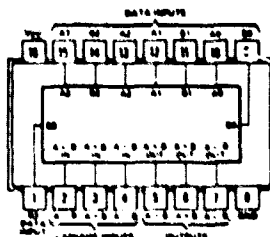
<p><b>QUADRUPLE 2-INPUT POSITIVE-OR GATES</b></p> <p><b>32</b></p> <p>positive logic: <math>Y = A+B</math></p> <p>See page 6-26</p>	 <p>SN5432 (J, W)    SN7432 (J, N) SN54LS32 (J, W)    SN74LS32 (J, N) SN54S32 (J, W)    SN74S32 (J, N)</p>
<p><b>QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS</b></p> <p><b>33</b></p> <p>positive logic: <math>Y = \overline{A+B}</math></p> <p>See pages 6-24 and 6-26</p>	 <p>SN5433 (J, W)    SN7433 (J, N) SN54LS33 (J, W)    SN74LS33 (J, N)</p>
<p><b>QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS</b></p> <p><b>37</b></p> <p>positive logic: <math>Y = \overline{AB}</math></p> <p>See page 6-26</p>	 <p>SN5437 (J, W)    SN7437 (J, N) SN54LS37 (J, W)    SN74LS37 (J, N) SN54S37 (J, W)    SN74S37 (J, N)</p>
<p><b>QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS</b></p> <p><b>38</b></p> <p>positive logic: <math>Y = \overline{AB}</math></p> <p>See pages 6-24 and 6-26</p>	 <p>SN5438 (J, W)    SN7438 (J, N) SN54LS38 (J, W)    SN74LS38 (J, N) SN54S38 (J, W)    SN74S38 (J, N)</p>

## 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

### PIN ASSIGNMENTS (TOP VIEWS)

#### 4 BIT MAGNITUDE COMPARATORS

85



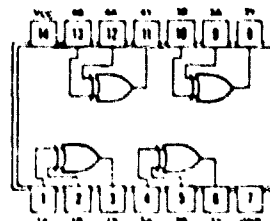
SN5485 (J, W) SN7485 (J, N)  
 SN54LS85 (J, W) SN74LS85 (J, N)  
 SN54ES85 (J, W) SN74ES85 (J, N)

SN54L85 (J) SN74L85 (J, N)

See page 7-57

#### QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86  $Y = A \oplus B = AB + \bar{A}\bar{B}$

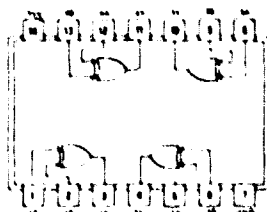


SN5486 (J, W) SN7486 (J, N)  
 SN54LS86 (J, W) SN74LS86 (J, N)  
 SN54ES86 (J, W) SN74ES86 (J, N)

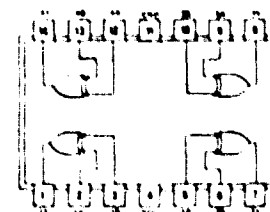
#### FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



SN54L86 (J) SN74L86 (J, N)



SN54L86 (T)

See page 7-65

#### 4 BIT TRUE-COMPLEMENT, ZERO-ONE ELEMENTS

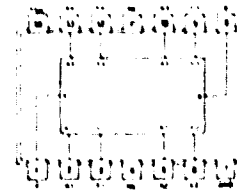
87

#### FUNCTION TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	A1	A2	A3	A4
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level, L = low level

A1, A2, A3, A4 = the level of the respective A input



SN5487 (J, W) SN7487 (J, N)

NC - No internal connection

See page 7-70

## 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

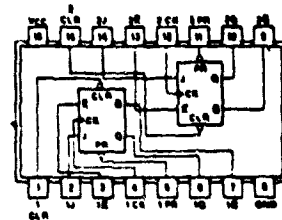
### PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

**109**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54109 (J, W)      SN74109 (J, N)  
SN54LS109A (J, W)      SN74LS109A (J, N)

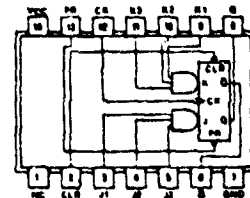
See pages 6-46 and 6-56

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

**110**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⌋	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	⌋	H	L	H	L
H	H	⌋	L	H	L	H
H	H	⌋	H	H	TOGGLE	



SN54110 (J, W)      SN74110 (J, N)

positive logic: J = J1·J2·J3  
K = K1·K2·K3

See page 6-46

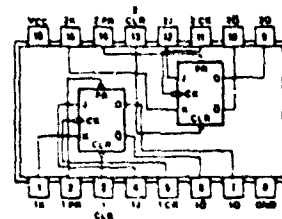
NC—No internal connection

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

**111**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⌋	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	⌋	H	L	H	L
H	H	⌋	L	H	L	H
H	H	⌋	H	H	TOGGLE	



SN54111 (J, W)      SN74111 (J, N)

See page 6-46

See explanation of function tables on page 3-8.

\* This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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## 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

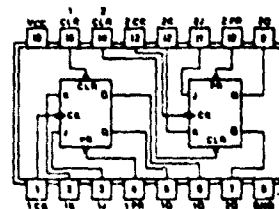
### PIN ASSIGNMENTS (TOP VIEWS)

#### DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS			OUTPUTS			
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	$Q_0$	$\bar{Q}_0$



SN54LS112 (J, W) SN74LS112 (J, N)  
SN54S112 (J, W) SN74S112 (J, N)

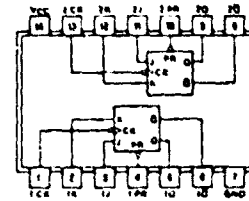
See pages 6-56 and 6-58

#### DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

113

FUNCTION TABLE

INPUTS		OUTPUTS			
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	$Q_0$	$\bar{Q}_0$



SN54LS113 (J, W) SN74LS113 (J, N)  
SN54S113 (J, W) SN74S113 (J, N)

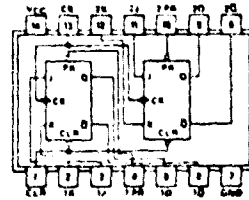
See pages 6-56 and 6-58

#### DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

114

FUNCTION TABLE

INPUTS			OUTPUTS			
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	$Q_0$	$\bar{Q}_0$



SN54LS114 (J, W) SN74LS114 (J, N)  
SN54S114 (J, W) SN74S114 (J, N)

See pages 6-56 and 6-58

See explanation of function tables on page J-8.

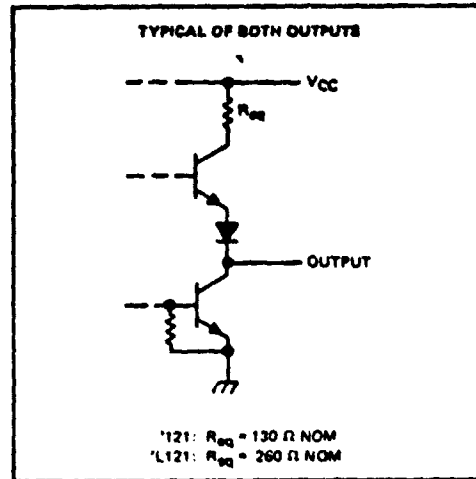
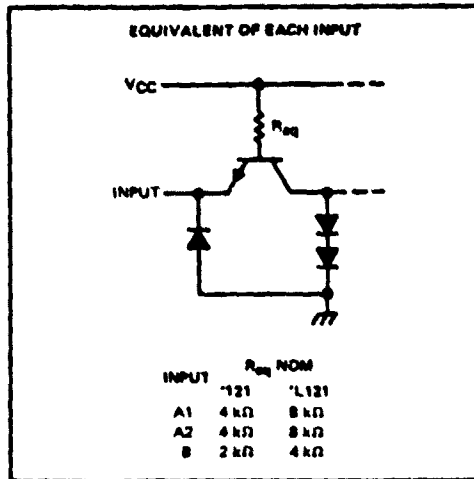
\*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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## TYPES SN54121, SN54L121, SN74121, SN74L121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

### schematics of inputs and outputs



### recommended operating conditions

	54 FAMILY	SN54121			SN54L121			UNIT	
	74 FAMILY	SN74121			SN74L121				
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, $V_{CC}$	54 Family	4.5	5	5.5	4.5	5	5.5	V	
	74 Family	4.75	5	5.25	4.75	5	5.25		
High-level output current, $I_{OH}$				-400			-200	$\mu$ A	
Low-level output current, $I_{OL}$				16			8	mA	
Rate of rise or fall of input pulses, $dv/dt$	Schmitt input, B	1			1			V/s	
	Logic inputs, A1, A2	1			1			V/ $\mu$ s	
Input pulse width, $t_w(\text{in})$		50			100			ns	
External timing resistance, $R_{ext}$	54 Family	1.4		30	1.4		30	k $\Omega$	
	74 Family	1.4		40	1.4		40		
External timing capacitance, $C_{ext}$		0			1000			$\mu$ F	
Duty cycle	$R_T = 2 \text{ k}\Omega$					67		67	%
	$R_T = \text{MAX } R_{ext}$					70		90	
Operating free-air temperature, $T_A$	54 Family	-55		125	-55		125	$^{\circ}$ C	
	74 Family	0		70	0		70		

## TYPES SN54121, SN54L121, SN74121, SN74L121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Programmable Output Pulse Width  
With  $R_{int}$  ... 35 ns Typ  
With  $R_{ext}/C_{ext}$  ... 40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

**FUNCTION TABLE**

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	I	H		
I	H	H		
I	I	H		
L	X	I		
X	L	I		

For explanation of function table symbols, see page J-8.

### description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

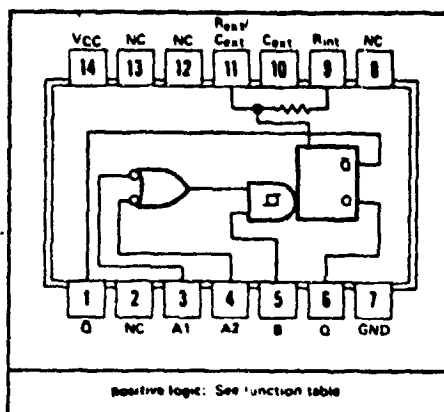
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to VCC noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e.,  $R_{int}$  connected to VCC,  $C_{ext}$  and  $R_{ext}/C_{ext}$  open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of VCC and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and VCC ranges for more than six decades of timing capacitance (10 pF to 10  $\mu$ F) and more than one decade of timing resistance (2 k $\Omega$  to 30 k $\Omega$  for the SN54121/SN54L121 and 2 k $\Omega$  to 40 k $\Omega$  for the SN74121/SN74L121). Throughout these ranges, pulse width is defined by the relationship  $t_{w(out)} = C_{ext}RT \ln 2 \approx 0.7 C_{ext}RT$ . In circuits where pulse cutoff is not critical, timing capacitance up to 1000  $\mu$ F and timing resistance as low as 1.4 k $\Omega$  may be used. Also, the range of jitter-free output pulse widths is extended if VCC is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended RT. Higher duty cycles are available if a certain amount of pulse width jitter is allowed.

SN54121 ... J OR W PACKAGE  
SN54L121 ... J OR T PACKAGE  
SN74121, SN74L121 ... J OR N PACKAGE



positive logic: See function table

NC—No internal connection

- NOTES
1. An external capacitor may be connected between  $C_{ext}$  (positive) and  $R_{ext}/C_{ext}$ .
  2. To use the internal timing resistor, connect  $R_{int}$  to VCC. For improved pulse width accuracy and repeatability, connect an external resistor between  $R_{ext}/C_{ext}$  and VCC with  $R_{int}$  open-circuited.



## TYPES SN54LS122, SN54LS123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

### recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Pulse width, $t_w$	40			40			ns
External timing resistance, $R_{Ext}$	5		180	5		280	k $\Omega$
External capacitance, $C_{Ext}$	No restriction			No restriction			
Wiring capacitance at $R_{Ext}/C_{Ext}$ terminal	50			50			pF
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
		MIN	TYP‡	MAX	MIN	
$V_{IH}$ High-level input voltage		2		2		V
$V_{IL}$ Low-level input voltage			0.7		0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN.}$ $I_I = -18 \text{ mA}$		-1.5		-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL \text{ max}}$ $I_{OH} = -400 \mu\text{A}$	2.5	3.5	2.7	3.5	V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL \text{ max}}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25	0.4	0.35	0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX.}$ $V_I = 7 \text{ V}$		0.1		0.1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX.}$ $V_I = 2.7 \text{ V}$		20		20	$\mu$ A
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX.}$ $V_I = 0.4 \text{ V}$		-0.4		-0.4	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX.}$	-20	-100	-20	-100	mA
$I_{CC}$ Supply current (quiescent or triggered)	$V_{CC} = \text{MAX.}$ See Note 13	'LS122 5 11		6 11		11 mA
		'LS123 12 20		12 20		20 mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 12. To measure  $V_{OH}$  at Q,  $V_{OL}$  at  $\bar{Q}$ , or  $I_{OS}$  at Q, ground  $R_{Ext}/C_{Ext}$ , apply 2 V to B and pulse A from 2 V to 0 V.

13. With all outputs open and 4.5 V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to clock.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ , see note 14

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Q	$C_{Ext} = 0$ , $R_{Ext} = 5 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$	23	33		ns
	B	Q		23	44		
$t_{PHL}$	A	$\bar{Q}$		32	45		ns
	B	$\bar{Q}$		34	56		
$t_{PHL}$	Clear	Q		20	27		ns
$t_{PLH}$	A or B	$\bar{Q}$		28	45		ns
$t_{WQ}$ (min)	A or B	Q		116	200		ns
$t_{WQ}$	A or B	Q		4	4.5	5	$\mu$ s

†  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

$t_{WQ}$  = width of pulse at output Q

NOTE 14. Load circuit and voltage waveforms are shown on page 3-11.

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## TYPES SN54LS122, SN74LS122, SN54LS123, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

### TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when  $C_{ext} \leq 1000$  pF, see Figure 7.

When  $C_{ext} > 1000$  pF, the output pulse width is defined as:

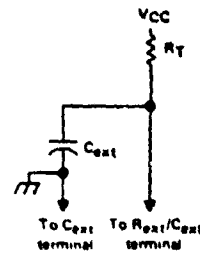
$$t_w = 0.45 \cdot R_T \cdot C_{ext}$$

where

$R_T$  is in  $k\Omega$  (internal or external timing resistance.)

$C_{ext}$  is in pF

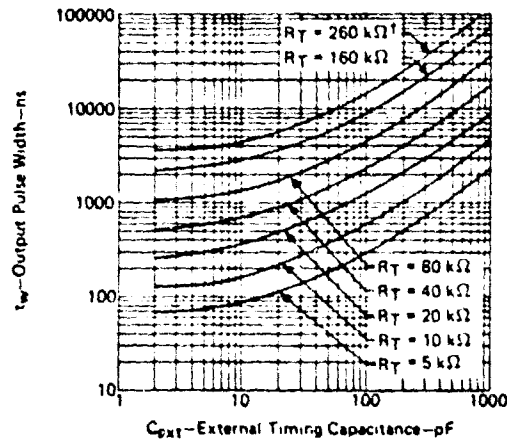
$t_w$  is in nanoseconds



TIMING COMPONENT CONNECTIONS

For best results, system ground should be applied to the  $C_{ext}$  terminal. The switching diode is not needed for electrolytic capacitance applications.

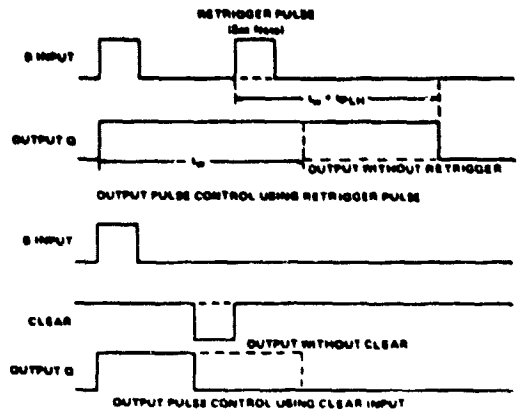
'LS122, 'LS123  
TYPICAL OUTPUT PULSE WIDTH  
vs  
EXTERNAL TIMING CAPACITANCE



† The value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

**TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123,  
SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123  
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

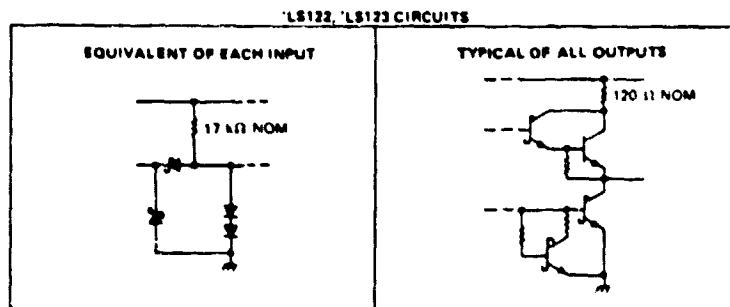
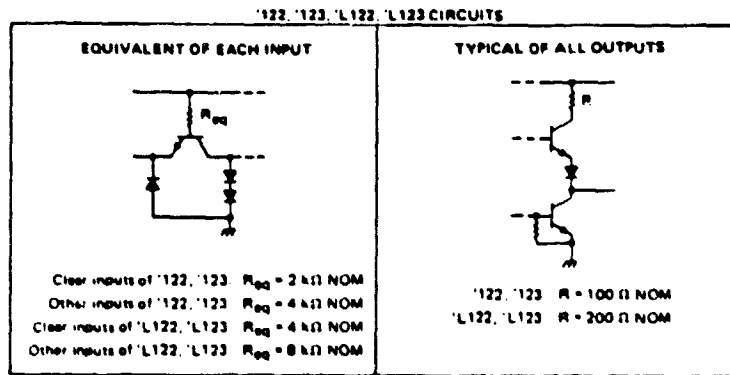
description (continued)



NOTE Retrigger pulse must not start before 0.22  $C_{out}$  (in picoseconds) nanoseconds after previous trigger pulse.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs



## TYPES SN54122, SN54123, SN54L122, SN54L123, SN54LS122, SN54LS123, SN74122, SN74123, SN74L122, SN74L123, SN74LS122, SN74LS123 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for VCC and Temperature Variations
- '122, 'L122, 'LS122 Have Internal Timing Resistors

'122, 'L122, 'LS122  
FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	H	H	U	U
H	L	X	H	H	U	U
H	X	L	H	H	U	U
H	X	L	H	H	U	U
H	H	L	H	H	U	U
H	H	L	H	H	U	U
H	L	H	H	H	U	U
H	L	H	H	H	U	U
H	X	L	H	H	U	U
H	X	L	H	H	U	U

'123, 'L123, 'LS123  
FUNCTION TABLE

CLEAR	INPUTS			OUTPUTS	
	A	B	Q	Q̄	Q̄
L	X	X	L	H	H
X	H	X	L	H	H
X	X	L	L	H	H
H	L	H	H	U	U
H	L	H	H	U	U
H	X	L	H	U	U
H	X	L	H	U	U

See explanation of function tables on page 3-8.

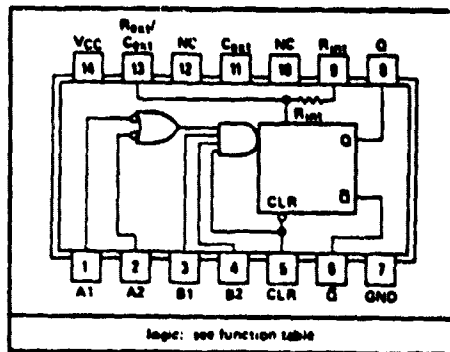
### description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, 'L122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

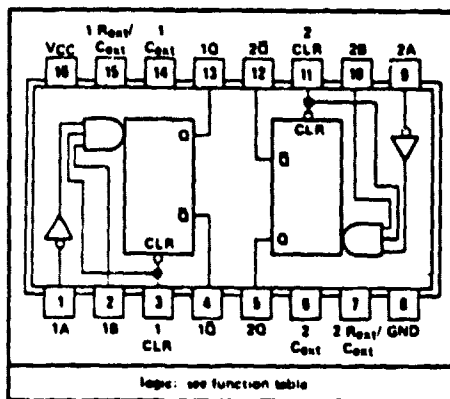
- NOTES:
1. An external timing capacitor may be connected between C<sub>EXT</sub> and R<sub>INT</sub>/C<sub>INT</sub> (positive).
  2. To use the internal timing resistor of '122, 'L122 or 'LS122, connect R<sub>INT</sub> to VCC.
  3. For improved pulse width accuracy and repeatability, connect an external resistor between R<sub>INT</sub>/C<sub>EXT</sub> and VCC with R<sub>INT</sub> open-circuited.
  4. To obtain variable pulse widths, connect an external variable resistance between R<sub>INT</sub> or R<sub>EXT</sub>/C<sub>EXT</sub> and VCC.

SN54122, SN54LS122 ... J OR W  
SN54L122 ... J OR Y  
SN74122, SN74L122, SN74LS122 ... J OR N  
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table  
NC—No internal connection.

SN54123, SN54LS123 ... J OR W  
SN54L123 ... J  
SN74123, SN74L123, SN74LS123 ... J OR N  
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see function table

# Am25LS138 • Am54LS/74LS138

## 3-Line To 8-Line Decoder/Demultiplexer

### DISTINCTIVE CHARACTERISTICS

- Inverting and non-inverting enable inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower VOL
  - Twice the fan-out over military range
  - 440µA source current
- 100% product assurance screening to MIL-STD-883 requirements

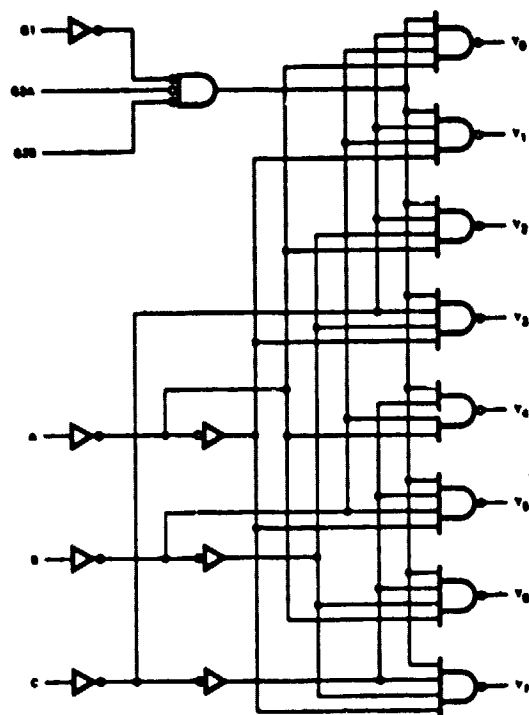
### FUNCTIONAL DESCRIPTION

The Am25LS138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

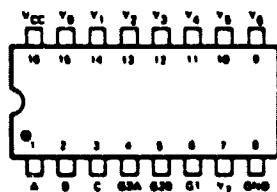
One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

The Am54LS/74LS138 is a standard performance version of the Am25LS138. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

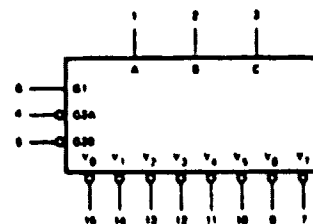


### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



VCC = Pin 16  
GND = Pin 8

### Am25LS/54LS/74LS138

#### ELECTRICAL CHARACTERISTICS Am25LS138

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  (MIN. = 4.75V MAX. = 5.25V)

MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  (MIN. = 4.50V MAX. = 5.50V)

#### DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -400 $\mu$ A	MIL	2.5	3.4	Volts
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	COM'L	2.7	3.4	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., I <sub>OL</sub> = 4mA			0.4	Volts
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 8mA			0.45	
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL		0.7	Volts
			COM'L		0.8	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN., I <sub>IN</sub> = -18mA			-1.5	Volts
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.4V			-0.36	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.7V			20	$\mu$ A
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 7.0V			0.1	mA
I <sub>SC</sub>	Output Short Circuit Current (Note 3)	V <sub>CC</sub> = MAX.	-15		-85	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX (Note 4)		63	10	mA

### ELECTRICAL CHARACTERISTICS Am54LS/74LS138

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  (MIN. = 4.75V MAX. = 5.25V)

MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  (MIN. = 4.50V MAX. = 5.50V)

#### DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -400 $\mu$ A	MIL	2.5	3.4	Volts
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	COM'L	2.7	3.4	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., All I <sub>OL</sub> = 4mA			0.4	Volts
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , 74LS only, I <sub>OL</sub> = 8mA			0.5	
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL		0.7	Volts
			COM'L		0.8	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN., I <sub>IN</sub> = -18mA			-1.5	Volts
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.4V			-0.36	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.7V			20	$\mu$ A
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 7.0V			0.1	mA
I <sub>SC</sub>	Output Short Circuit Current (Note 3)	V <sub>CC</sub> = MAX.	-15		-85	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX (Note 4)		63	10	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. Outputs enabled and open.

#### MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	-0.5V to +V <sub>CC</sub> max
DC Input Voltage	-0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	-20mA to +5.0mA

# Am25LS153 • Am54LS/74LS153

# Am25LS253 • Am54LS/74LS253

Dual 4-Line To 1-Line Data Selectors/Multiplexers

## DISTINCTIVE CHARACTERISTICS

- Performs serial to parallel conversion
- Standard, 'LS153, and three-state, 'LS253, output versions
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower VOL
  - Twice the fan-out over military range
  - 440µA source current
- 100% product assurance screening to MIL-STD-883 requirements

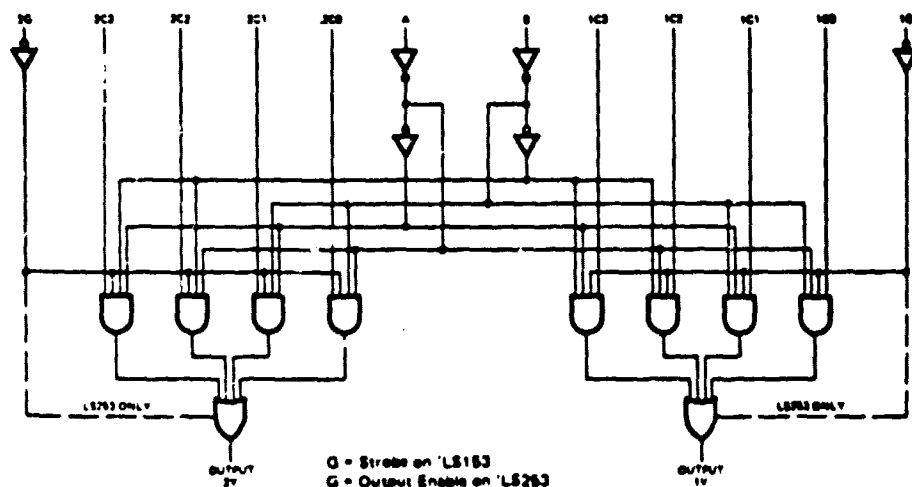
## FUNCTIONAL DESCRIPTION

These dual four-input multiplexers provide the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am25LS153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

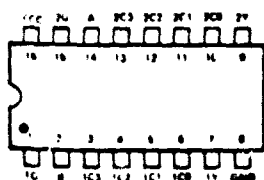
The Am25LS253 features a three-state output to interface with bus-organized systems. Each section of the Am25LS253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

The Am54LS/74LS153 and 253 are standard performance versions of the Am25LS153 and 253. See appropriate electrical characteristic tables for detailed Am25LS improvements.

## LOGIC DIAGRAM

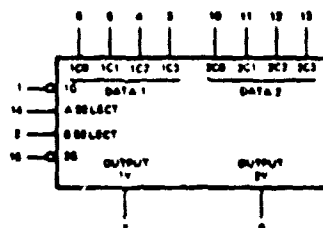


## CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation

## LOGIC SYMBOL



VCC = Pin 16  
 GND = Pin 8

## Am54LS/74LS153 • Am54LS/74LS253

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified.

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  (MIN. = 4.75V MAX. = 5.25V)  
 MIL  $T_A = -65^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
$V_{OH}$	Output HIGH Voltage	54LS153	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -400\mu\text{A}$	2.5	3.4	Volts
		74LS153			2.7	3.4	
		54LS253		$I_{OH} = -1\text{mA}$	2.4	3.4	
		74LS253			2.4	3.2	
$V_{OL}$	Output LOW Voltage					0.4	Volts
						0.5	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7	Volts
						0.8	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MAX.}$ , $V_{IN} = -18\text{mA}$				-1.5	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}$ , $V_{IN} = 0.6\text{V}$				-0.36	mA
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}$ , $V_{IN} = 2.7\text{V}$				20	$\mu\text{A}$
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}$ , $V_{IN} = 7.0\text{V}$				0.1	mA
$I_{OZ}$	Off-State (HIGH Impedance) Output Current Am54LS/74LS253 Only	$V_{CC} = \text{MAX.}$		$V_O = 2.4\text{V}$		20	$\mu\text{A}$
				$V_O = 0.4\text{V}$		-20	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$		-1E		-100	mA
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX.}$ (Note 4)		LS153		6.2	mA
				LS253		7	

- Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4.  $I_{CC}$  is measured with all outputs open and all inputs grounded.

3

Am25LS153/54LS153  
 SWITCHING CHARACTERISTICS  
 ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )

Parameters	Description	Am25LS			Am54LS/74LS			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
$t_{PLH}$	Data to Output		10	15		10	15	ns	$C_L = 15\text{pF}$ $R_L = 20\text{k}\Omega$
$t_{PHL}$			10	16		17	26		
$t_{PLH}$	Select to Output		19	29		19	29		
$t_{PHL}$			15	23		25	38		
$t_{PLH}$	Strobe to Output		16	24		18	24		
$t_{PHL}$			12	18		21	32		

Am25LS153 ONLY  
 SWITCHING CHARACTERISTICS  
 OVER OPERATING RANGE\*

Parameters	Description	Am25LS COM'L		Am25LS MIL		Units	Test Conditions
		Min.	Max.	Min.	Max.		
$t_{PLH}$	Data to Output	$T_A = 0^\circ\text{C to } -70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		$T_A = -65^\circ\text{C to } -125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		ns	$C_L = 50\text{pF}$ $R_L = 20\text{k}\Omega$
			24		27		
$t_{PHL}$	Select to Output		26		29	ns	
$t_{PLH}$			42		48		
$t_{PHL}$	Strobe to Output		34		39	ns	
$t_{PLH}$			26		41		
$t_{PHL}$			28		32		

\*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 5



# Am25LS157 • Am54LS/74LS157

# Am25LS158 • Am54LS/74LS158

Quadruple 2-Line To 1-Line Data Selectors/Multiplexers

### DISTINCTIVE CHARACTERISTICS

- Selects four of eight data inputs with single select line and overriding strobe
- Inverting 'LS158 and Non-inverting 'LS157 configurations
- Standard TTL outputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower  $V_{OL}$
  - Twice the fan-out over military range
  - 440 $\mu$ A source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

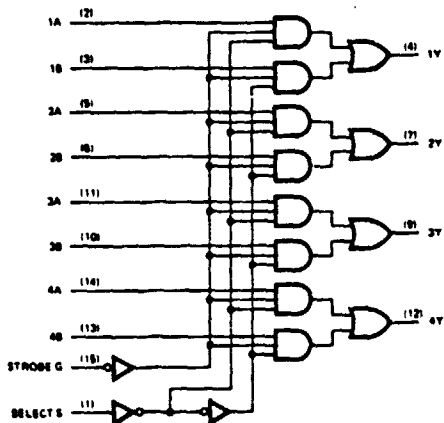
These data selectors/multiplexers are used to select a 4-bit word from one of two sources. The four outputs at the Am25LS157 present true data with respect to the input data. The four outputs of the Am25LS158 present inverted data with respect to the inputs and also minimize propagation delay. A common active-HIGH strobe (active-LOW enable) is provided on all devices.

A single select line, S, is used to select one of the two multiplexer input words. When the select is LOW, the A input word is present at the output. When the select is HIGH, the B input word is present at the output.

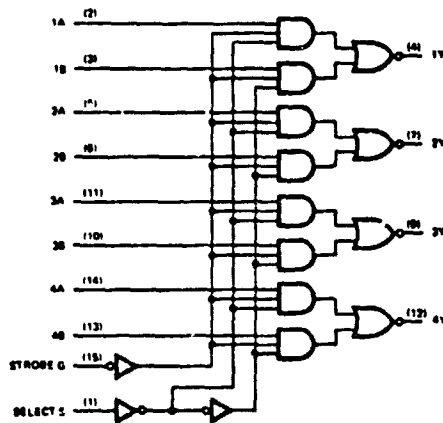
The Am54LS/74LS157 and 158 are standard performance versions of the Am25LS157 and 158. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

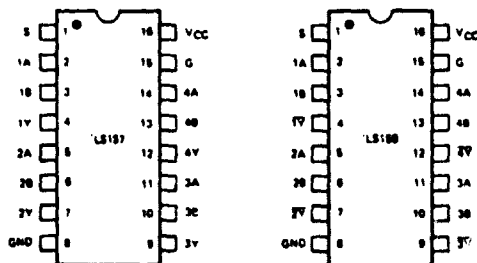
Am25LS157  
Am54LS/74LS157



Am25LS158  
Am54LS/74LS158

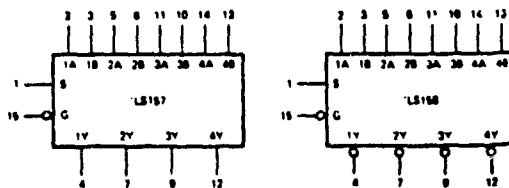


### CONNECTION DIAGRAMS Top Views



Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



$V_{CC}$  = Pin 16  
GND = Pin 8

## Am25LS157 • Am25LS158

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  (MIN. = 4.75V MAX. = 5.25V)MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -440\mu\text{A}$	MIL	2.5	3.4	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	COM'L	2.7	3.4	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.}$			0.4	Volts
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 4\text{mA}$		0.45	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2			Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL		0.7	Volts
			COM'L		0.8	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$			-1.5	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$	S or G		-0.36	mA
			A or B		-0.4	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$	S or G		20	$\mu\text{A}$
			A or B		20	
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$	S or G		0.1	mA
			A or B		0.1	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$	-15		-85	mA
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX.}$		9.7	16	mA
		(Note 4)	LS157			
			LS158	4.8	8	

- Notes: 1 For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2 Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3 Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4  $I_{CC}$  is measured with all outputs open and 4.5V applied to all inputs.

3

## Am54LS/74LS157 • Am54LS/74LS158

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  (MIN. = 4.75V MAX. = 5.25V)MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -400\mu\text{A}$	Am54LS	2.5	3.4	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	Am74LS	2.7	3.4	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.}$			0.4	Volts
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	All, $I_{OL} = 4\text{mA}$ 74LS only, $I_{OH} = 8\text{mA}$		0.5	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2			Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	Am54LS		0.7	Volts
			Am74LS		0.8	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$			-1.5	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$	S or G		-0.8	mA
			A or B		-0.4	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$	S or G		40	$\mu\text{A}$
			A or B		20	
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$	S or G		0.2	mA
			A or B		0.1	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$	-15		-100	mA
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX.}$		9.7	16	mA
		(Note 4)	LS157			
			LS158	4.8	8	

- Notes: 1 For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2 Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3 Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4  $I_{CC}$  is measured with all outputs open and 4.5V applied to all inputs.

# Am25LS160A/161A/162A/163A Am54LS/74LS160A/161A/162A/163A

## Synchronous Four-Bit Counters

### DISTINCTIVE CHARACTERISTICS

- Synchronous presettable counters
- Decade ('LS160A and 'LS162A) and binary ('LS161A and 'LS163A) counters
- Asynchronous ('LS160A and 'LS161A) and synchronous ('LS162A and 'LS163A) clear inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower VOL
  - Twice the fan-out over military range
  - 440µA source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

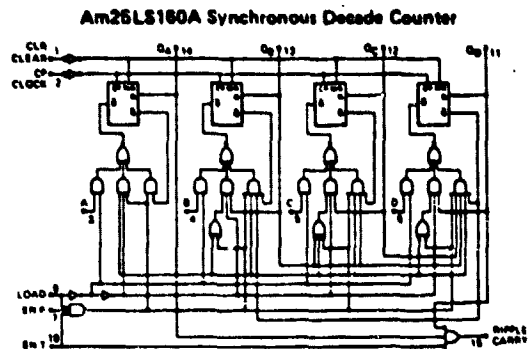
The Am25LS160A, Am25LS161A, Am25LS162A and Am25LS163A synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am25LS160A and Am25LS162A are decade counters and the Am25LS161A and Am25LS163A are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. The load need meet only the set-up and hold time requirements with respect to the clock.

The Am25LS160A and the Am25LS161A feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am25LS162A and Am25LS163A have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

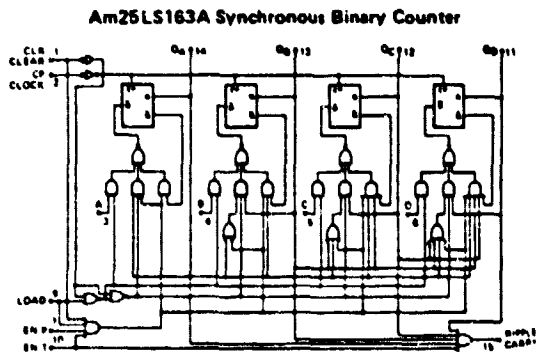
Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. The enable P or T inputs need meet only the set-up and hold time requirements with respect to the clock.

The Am54LS/74LS160A series are standard performance versions of the Am25LS160A series counters. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

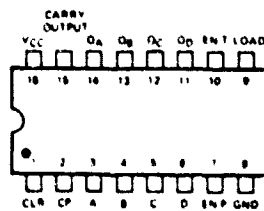


Am25LS162A synchronous decade counters are similar; however, the clear is synchronous as shown for the Am25LS163A binary counters.



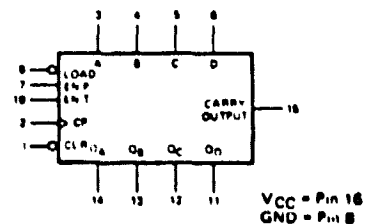
Am25LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the Am25LS160A decade counters.

### CONNECTION DIAGRAM Top View



Note Pin 1 is marked for orient.

### LOGIC SYMBOL



## Am25LS160A, 161A, 162A and 163A

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  (MIN. = 4.75V MAX. = 5.25V)MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units	
VOH	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -440\mu\text{A}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
VOL	Output LOW Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 4.0\text{mA}$		0.25	0.4	Volts
			$I_{OL} = 8.0\text{mA}$		0.35	0.45	
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts	
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L				
V <sub>I</sub>	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$			-1.5	Volts	
I <sub>IL</sub>	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$	A, B, C, D, EN, P, CP			-0.4	mA
			Load, EN, T			-0.8	
			Clear '160A, '161A			-0.4	
			Clear '162A, '163A			-0.4	
I <sub>IH</sub>	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$	A, B, C, D, EN, P, CP			20	$\mu\text{A}$
			Load, EN, T			40	
			Clear '160A, '161A			20	
			Clear '162A, '163A			20	
I <sub>I</sub>	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$	A, B, C, D, EN, P, CP			0.1	mA
			Load, EN, T			0.2	
			Clear '160A, '161A			0.1	
			Clear '162A, '163A			0.1	
I <sub>SC</sub>	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$	-15		-85	mA	
I <sub>CCH</sub>	Power Supply Current All Outputs HIGH	$V_{CC} = \text{MAX.}$ (Note 4)		18	31	mA	
I <sub>CCL</sub>	Power Supply Current All Outputs LOW	$V_{CC} = \text{MAX.}$ (Note 5)		19	32	mA	

- Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4. I<sub>CCH</sub> is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.  
 5. I<sub>CCL</sub> is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V <sub>CC</sub> max.
DC Input Voltage	-0.5V to +7.0V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

# Am25LS164 • Am54LS/74LS164

## 8-Bit Serial-In, Parallel-Out Shift Register

### DISTINCTIVE CHARACTERISTICS

- Gated serial inputs
- Asynchronous clear
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower  $V_{OL}$  at  $I_{OL} = 8\text{mA}$
  - Twice the fan-out over military range
  - 440 $\mu\text{A}$  source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

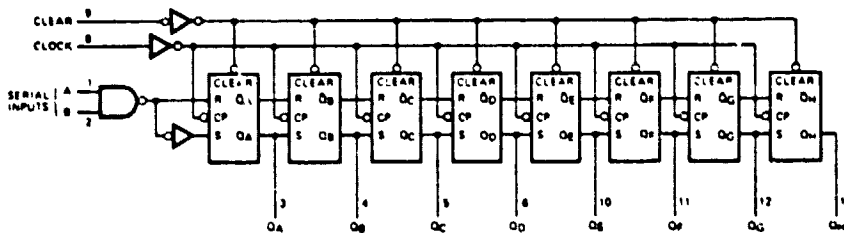
### FUNCTIONAL DESCRIPTION

The Am25LS164 and Am54LS/74LS164 are eight-bit, serial in/parallel out shift registers built using advanced Low-Power Schottky processing. A gated input provides enable/disable control over incoming data such that the data can be entered or logic zeros can be entered into the register.

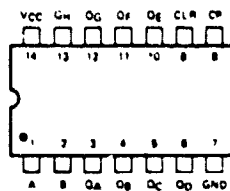
An asynchronous clear input can be used to simultaneously clear the eight flip-flops in the device. When the clear input is LOW, all internal flip-flops are forced LOW independent of the clock input. An incoming data bit is entered into the  $Q_A$  flip-flop and the data in all internal flip-flops is shifted right on the LOW-to-HIGH transition of the clock input.

The Am54LS/74LS164 is a standard performance version of the Am25LS164. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

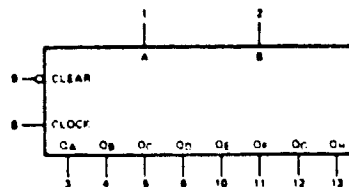


### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



VCC = Pin 14  
GND = Pin 7

**Am25LS/54LS/74LS164**

**Am25LS164**

**ELECTRICAL CHARACTERISTICS**

The Following Conditions Apply Unless Otherwise Specified:

COM'L  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 5\%$  MIN. = 4.75V MAX. = 5.25V  
 MIL  $T_A = -55^\circ\text{C to } +125^\circ\text{C}$   $V_{CC} = 5.0\text{V} \pm 10\%$  MIN. = 4.50V MAX. = 5.50V

**DC CHARACTERISTICS OVER OPERATING RANGE**

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -440\mu\text{A}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.},$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 4.0\text{mA}$		0.25	0.4	Volts
			$I_{OL} = 8.0\text{mA}$		0.35	0.45	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts	
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$			-1.5	Volts	
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$	Clock, Clear A, B			-0.36	mA
						-0.4	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$			20	$\mu\text{A}$	
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$			0.1	mA	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$	-15		-85	mA	
$I_{CC}$	Power Supply Current (Note 4)	$V_{CC} = \text{MAX.}$		16	27	mA	

- Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4. Measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V applied to the clear input.

**Am25LS • Am54LS/74LS**

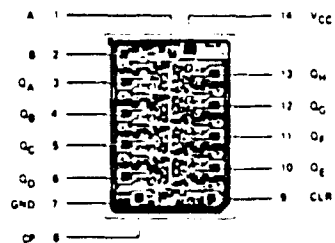
**MAXIMUM RATINGS (Above which the useful life may be impaired)**

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to + $V_{CC \text{ max}}$
DC Input Voltage	-0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

**DEFINITION OF FUNCTIONAL TERMS**

- A, B** The serial inputs to the device. If either the A input is LOW or the B input is LOW, the  $Q_A$  flip flop will be set LOW on the LOW-to-HIGH transition of the clock.
- Clear** An asynchronous master reset for the eight flip flops in the device. When the clear input is LOW, all internal flip flops are set LOW independent of the clock.
- $Q_A$ - $Q_H$**  The eight true outputs of the eight-bit register.
- Clock** The clock input to the register. Data is entered into the register on the LOW-to-HIGH transition of the clock input.

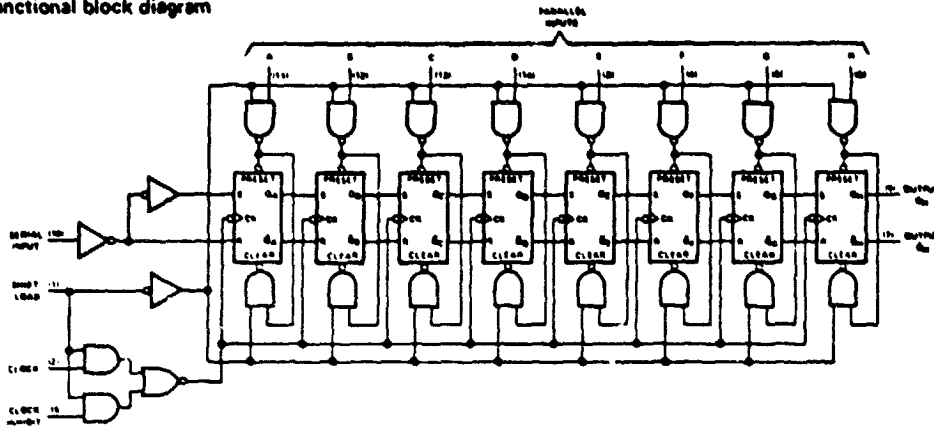
**Metallization and Pad Layout**



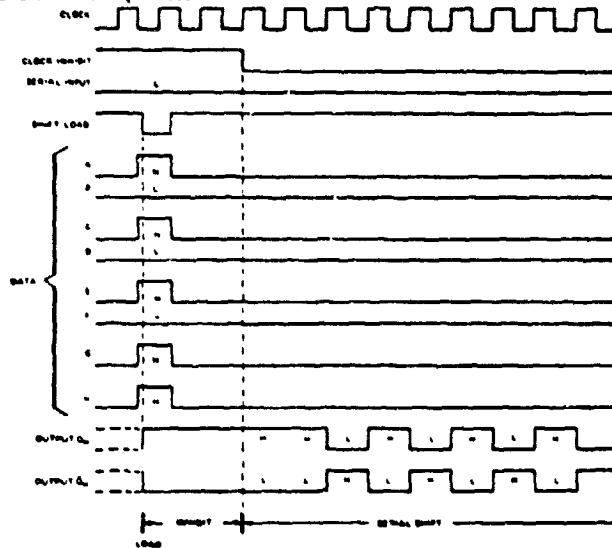
DIE SIZE 0.066" X 0.090"

## TYPES SN54165, SN54LS165, SN74165, SN74LS165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

functional block diagram



typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: SN54165, SN74165	5.5 V
SN54LS165, SN74LS165	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54165, SN54LS165	-55°C to 125°C
SN74165, SN74LS165	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the shift/load input in conjunction with the clock-inhibit inputs.

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## TYPES SN54165, SN54LS165, SN74165, SN74LS165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

BULLETIN NO. DL-3 7611375, OCTOBER 1976

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

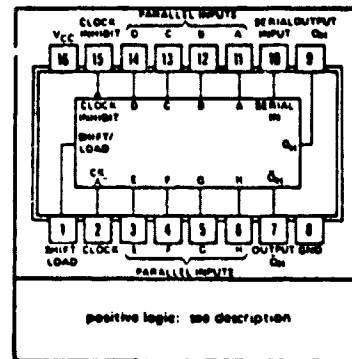
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165	35 MHz	105 mW

### description

The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of  $Q_A$  toward  $Q_H$  when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

SN54165, SN54LS165 ... J OR W PACKAGE  
SN74165, SN74LS165 ... J OR N PACKAGE  
(TOP VIEW)

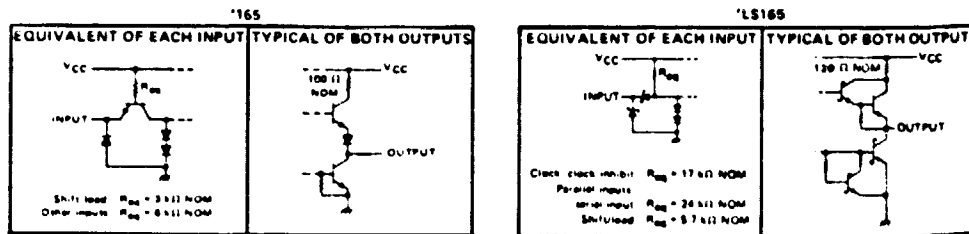


FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	$Q_A$	$Q_B$	$Q_H$
L	X	X	X	a...h	a	b	h
H	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	↑	H	X	H	$Q_{An}$	$Q_{Gn}$
H	L	↑	L	X	L	$Q_{An}$	$Q_{Gn}$
H	H	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

See explanation of function tables on page 38.

### schematic of inputs and output



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## TYPES SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-8 7611829, DECEMBER 1972—REVISED OCTOBER 1976

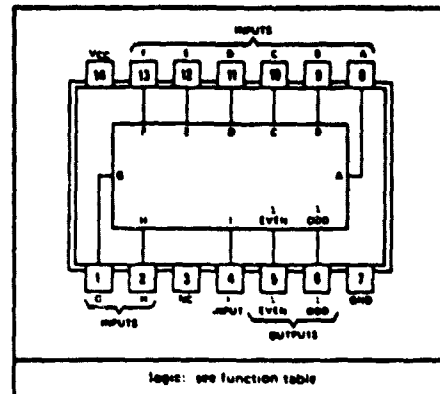
- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:  
'LS280 . . . 80 mW  
'S280 . . . 335 mW

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

SN54LS280, SN54S280 . . . J OR W PACKAGE  
SN74LS280, SN74S280 . . . J OR N PACKAGE  
(TOP VIEW)



Logic: see function table

NC—No internal connection

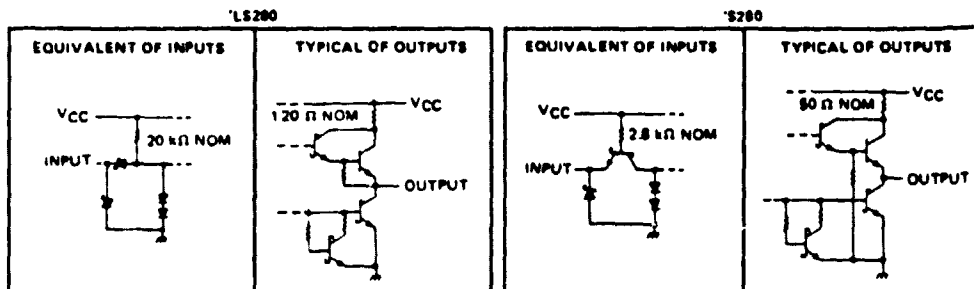
### description

These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade-off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

These devices are fully compatible with most other TTL and DTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

### schematics of inputs and outputs



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## TYPES SN54LS280, SN74LS280 8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS280	-55°C to 125°C
SN74LS280	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS280			SN74LS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I <sub>OH</sub>			-0.4			4	mA
Low-level output current, I <sub>OL</sub>			4			8	mA
Operating free-air temperature, T <sub>A</sub>	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>1</sup>	SN54LS280			SN74LS280			UNIT		
		MIN	TYP <sup>2</sup>	MAX	MIN	TYP <sup>2</sup>	MAX			
V <sub>IH</sub>	High-level input voltage	2			2			V		
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5			-1.5	V		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA		2.5	3.4	2.7		3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX		0.25		0.4		0.25	0.4	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1		0.1		0.1	mA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		20		20		20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4		-0.4		-0.4	mA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-20	-100	-20	-100	mA		
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 2		16	27	16	27	mA		

<sup>1</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>2</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>3</sup>Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I<sub>CC</sub> is measured with all inputs grounded and all outputs open.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER <sup>1</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Data	Σ Even	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 3			33	50
t <sub>PHL</sub>						29	45
t <sub>PLH</sub>	Data	Σ Odd				23	35
t <sub>PHL</sub>						31	50

<sup>1</sup>t<sub>PLH</sub> = propagation delay time low to high level output; t<sub>PHL</sub> = propagation delay time high to low level output.

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

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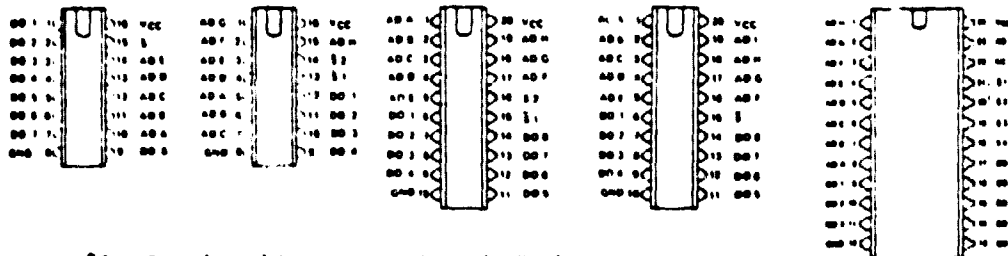
# SCHOTTKY<sup>†</sup> PROM'S

## SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
-55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	51 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

256 BITS (32 WORDS BY 8 BITS) '188, '288  
 1024 BITS (256 WORDS BY 4 BITS) '287, '387  
 2048 BITS (256 WORDS BY 8 BITS) '470, '471  
 4096 BITS (512 WORDS BY 8 BITS) '472, '473  
 4096 BITS (512 WORDS BY 8 BITS) '474, '475



### description

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip select times.

The high-complexity 2048- and 4096-bit 20 pin PROM's can be used to significantly improve system density for fixed memories as all are offered in a dual-in-line package having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET  
Supplementary data may be  
published at a later date.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U. S. Patent Number 3,463,875.

## SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

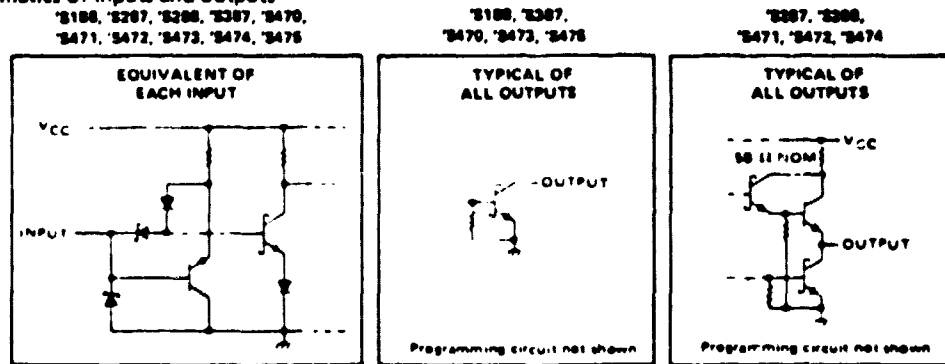
### description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S267 and 'S367, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti:W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Off state output voltage		5.5 V
Operating free-air temperature range	SN54S' Circuits	-55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		-65°C to 150°C

### recommended conditions for programming

		SN54S', SN74S'			UNIT	
		MIN	NOM	MAX		
Supply voltage, V <sub>CC</sub> (see Note 1)	Steady state	4.75	5	5.75	V	
	Program pulse	10	10.5	11 <sup>†</sup>		
Input voltage	High level, V <sub>IH</sub>	2.4	5		V	
	Low level, V <sub>IL</sub>	0	0.5			
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)				
Voltage applied to output to be programmed, V <sub>O(p)</sub> (see Note 2)		0	0.25	0.3	V	
Duration of V <sub>CC</sub> programming pulse Y (see Figure 2 and Note 3)		0.9	1	10	ms	
Programming duty cycle		25			35	%
Free-air temperature		0	55		°C	

<sup>†</sup> Absolute maximum ratings.

- NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.  
 2. The 'S188, 'S268, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S267 and 'S367 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.  
 3. Programming is guaranteed if the pulse applied is 0.9 ms long.

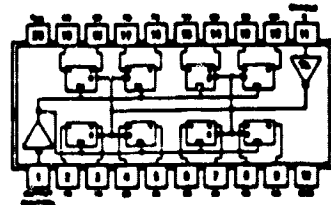


## 64/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

### PIN ASSIGNMENTS (TOP VIEWS)

#### OCTAL D-TYPE LATCHES

**363** TRANSPARENT LATCH  
3-STATE OUTPUT  
COMMON OUTPUT CONTROL  
COMMON ENABLE

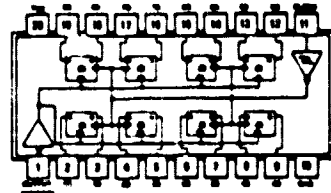


See page 7-467

SN64LS363 (J) SN74LS363 (J, N)

#### OCTAL D-TYPE FLIP-FLOPS

**364** COMMON CLOCK  
COMMON OUTPUT CONTROL  
3-STATE OUTPUTS

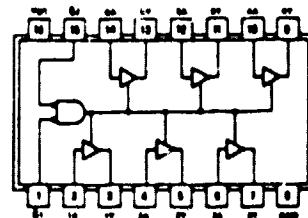


See page 7-467

SN64LS364 (J) SN74LS364 (J, N)

#### HEX BUS DRIVERS

**365** 3-STATE OUTPUTS  
NONINVERTED DATA OUTPUTS  
GATED ENABLE INPUTS

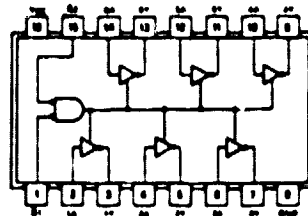


See page 6-26

SN64365A (J, W) SN74365A (J, N)  
SN64LS365 (J, W) SN74LS365 (J, N)

#### HEX BUS DRIVERS

**366** INVERTED DATA OUTPUT  
GATED ENABLE INPUTS  
3-STATE OUTPUTS



See page 6-26

SN64366A (J, W) SN74366A (J, N)  
SN64LS366 (J, W) SN74LS366 (J, N)

# Am26LS32 • Am26LS33

## Quad Differential Line Receivers

### DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- 10.2V sensitivity over the input voltage range on Am26LS32; 20.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

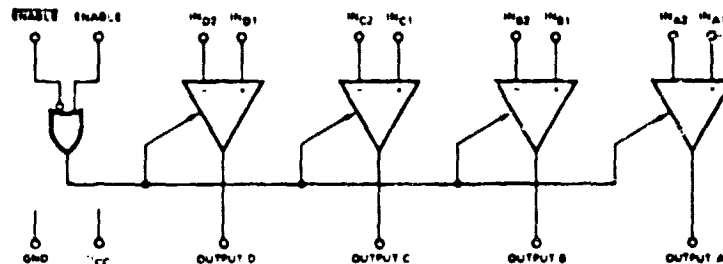
The Am26LS32 features an input sensitivity of 200mV on the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV on the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

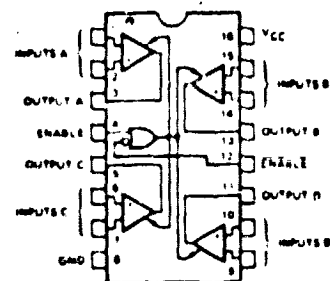
### LOGIC DIAGRAM



### ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32	Am26LS33
		Order Number	Order Number
Hermetic DIP	-65°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pack	-65°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	-65°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

**Absolute Maximum Ratings** (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Output Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	-65°C to +185°C

**Electrical Characteristics** Over the operating temperature range

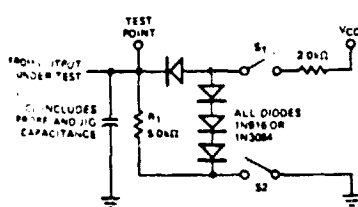
The following conditions apply unless otherwise specified:

Am26LS32	Am26LS33XM (MIL)	T <sub>A</sub> = -85°C to +125°C	V <sub>CC</sub> = 5.0V ± 10%
Am26LS33	Am26LS33XC (COM'L)	T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = 5.0V ± 5%

Parameter	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units	
V <sub>IH</sub>	Differential Input Voltage	V <sub>OUT</sub> = V <sub>OL</sub> or V <sub>OH</sub>	Am26LS32, -7V < V <sub>CM</sub> < +7V	0.2	0.06	0.2	Volts
			Am26LS33, -15V < V <sub>CM</sub> < +15V	0.5	0.12	0.5	
R <sub>IN</sub>	Input Resistance	-15V < V <sub>CM</sub> < +15V (One input AC ground)	6.0k	8.5k		Ω	
I <sub>IN</sub>	Input Current (Under Test)	V <sub>IN</sub> = +15V, Other Input -15V < V <sub>IN</sub> < +15V			2.3	mA	
I <sub>IN</sub>	Input Current (Under Test)	V <sub>IN</sub> = -15V, Other Input -15V < V <sub>IN</sub> < +15V			-2.8	mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., ΔV <sub>IN</sub> = +1.0V V <sub>ENABLE</sub> = 0.8V, I <sub>OH</sub> = -440μA	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., ΔV <sub>IN</sub> = -1.0V V <sub>ENABLE</sub> = 0.8V	I <sub>OL</sub> = 4.0mA		0.4		Volts
			I <sub>OL</sub> = 8.0mA		0.45		
V <sub>IL</sub>	Enable LOW Voltage				0.8	Volts	
V <sub>IH</sub>	Enable HIGH Voltage		2.0			Volts	
V <sub>I</sub>	Enable Clamp Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA			-1.5	Volts	
I <sub>O</sub>	Off-State (High Impedance) Output Current	V <sub>CC</sub> = Max.	V <sub>O</sub> = 2.4V		20	mA	
			V <sub>O</sub> = 0.4V		-20		
I <sub>HL</sub>	Enable LOW Current	V <sub>IN</sub> = 0.4V			-0.36	mA	
I <sub>IH</sub>	Enable HIGH Current	V <sub>IN</sub> = 2.7V			20	μA	
I <sub>SC</sub>	Output Short Circuit Current	V <sub>O</sub> = 0V, V <sub>CC</sub> = Max., ΔV <sub>IN</sub> = +1.0V	-15		-85	mA	
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max., All V <sub>IN</sub> = GND, Outputs Disabled		52	70	mA	
I <sub>H</sub>	Input High Current	V <sub>IN</sub> = 5.5V			100	μA	
V <sub>HY</sub>	Input Hysteresis	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, V <sub>CM</sub> = 0V		30		mV	
t <sub>PLH</sub>	Input to Output	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 15pF, see test cond. below		17	25	ns	
t <sub>PHL</sub>	Input to Output	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 15pF, see test cond. below		17	25	ns	
t <sub>LZ</sub>	Enable to Output	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 5pF, see test cond. below		20	30	ns	
t <sub>HZ</sub>	Enable to Output	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 5pF, see test cond. below		15	22	ns	
t <sub>ZL</sub>	Enable to Output	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 15pF, see test cond. below		15	22	ns	
t <sub>ZH</sub>	Enable to Output	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 15pF, see test cond. below		15	22	ns	

Note 1: Typical values are V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C.

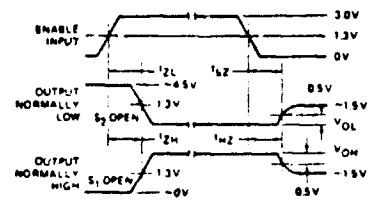
**LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS**



**PROPAGATION DELAY** (Notes 1 and 3)



**ENABLE AND DISABLE TIMES** (Notes 2 and 3)



- Notes:
- Diagram shown for Enable LOW.
  - S<sub>1</sub> and S<sub>2</sub> of Load Circuit are closed except where shown.
  - Pulse Generator for All Pulses. Rate < 1.0MHz. Z<sub>0</sub> = 50Ω, t<sub>r</sub> < 15ns; t<sub>f</sub> < 6.0ns

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# Am26LS31

Quad High Speed Differential Line Driver

## DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0ns typical
- Input to output delay – 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when  $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 50Ω transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

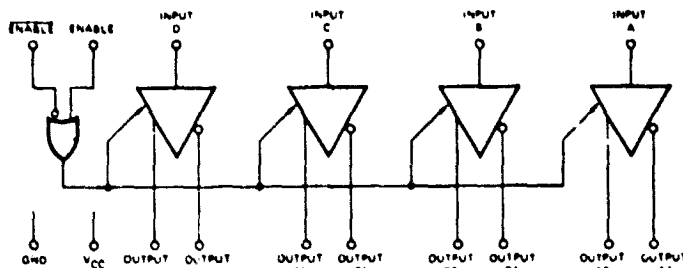
## FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logically AND-ed complementary outputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

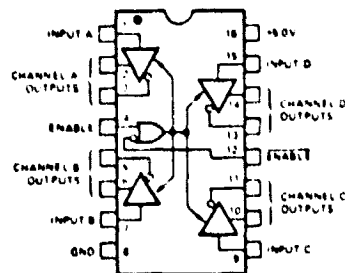
## LOGIC DIAGRAM



## ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	-55°C to +125°C	AM26LS31DM
Flat Pak	-55°C to +125°C	AM26LS31FM
Dice	-55°C to +125°C	AM26LS31XM
Hermetic DIP	0°C to +70°C	AM26LS31DC
Molded DIP	0°C to +70°C	AM26LS31PC
Dice	0°C to +70°C	AM26LS31XC

## CONNECTION DIAGRAM (Top View)



Note: Pin 1 is marked for orientation.



**ABSOLUTE MAXIMUM RATINGS** (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V
Storage Temperature Range	-65°C to +150°C

**ELECTRICAL CHARACTERISTICS** over the operating temperature range

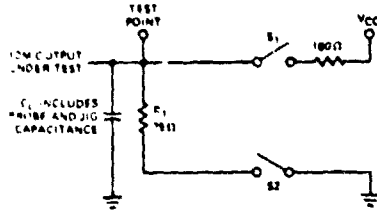
Conditions apply unless otherwise specified:

TA = -55°C to +125°C VCC = 5V ± 10%  
 TA = 0°C to +70°C VCC = 5V ± 5%

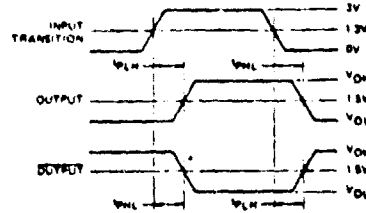
Parameter	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	VCC = Min., I <sub>OH</sub> = -20mA	2.5			Volts
V <sub>OL</sub>	Output LOW Voltage	VCC = Min., I <sub>OL</sub> = 20mA			0.5	Volts
V <sub>IH</sub>	Input HIGH Voltage	VCC = Min.	2.0			Volts
V <sub>IL</sub>	Input LOW Voltage	VCC = Max.			0.8	Volts
I <sub>IL</sub>	Input LOW Current	VCC = Max., V <sub>IN</sub> = 0.4V			-0.36	mA
I <sub>IH</sub>	Input HIGH Current	VCC = Max., V <sub>IN</sub> = 2.7V			20	μA
I <sub>R</sub>	Input Reverse Current	VCC = Max., V <sub>IN</sub> = 7.0V			0.1	mA
I <sub>O</sub>	Off-State (High Impedance) Output Current	VCC = Max., V <sub>O</sub> = 2.5V			20	μA
		V <sub>O</sub> = 0.5V			-20	μA
V <sub>I</sub>	Input Clamp Voltage	VCC = Min., I <sub>IN</sub> = 18mA			-1.5	Volts
I <sub>SC</sub>	Output Short Circuit Current	VCC = Max.	-30		-150	mA
I <sub>CC</sub>	Power Supply Current	VCC = Max., all outputs disabled		60	80	mA
t <sub>PLH</sub>	Input to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, Load = Note 2		12	20	ns
t <sub>PWL</sub>	Input to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, Load = Note 2		12	20	ns
t <sub>SEW</sub>	Output to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, Load = Note 2		2.0	6.0	ns
t <sub>L2</sub>	Enable to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 10pF		23	35	ns
t <sub>L3</sub>	Enable to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 10pF		17	30	ns
t <sub>L1</sub>	Enable to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, Load = Note 2		35	45	ns
t <sub>M</sub>	Enable to Output	VCC = 5.0V, T <sub>A</sub> = 25°C, Load = Note 2		30	40	ns

1. All values are VCC = 5.0V, T<sub>A</sub> = 25°C  
 2. 50pF, V<sub>IN</sub> = 1.3V to V<sub>OUT</sub> = 1.3V, V<sub>PULSE</sub> = 0V to +3.0V. See Below.

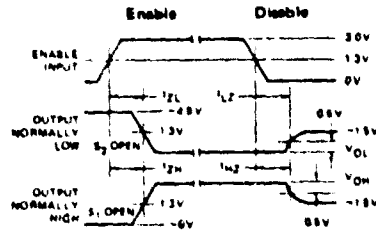
**AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS**



**PROPAGATION DELAY (Notes 1 and 3)**



**ENABLE AND DISABLE TIMES (Notes 2 and 3)**



Notes: 1. Diagram shown for Enable LOW.  
 2. S<sub>1</sub> and S<sub>2</sub> of Load Circuit are closed as shown where shown.  
 3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz, Z<sub>O</sub> = 50Ω, t<sub>r</sub> ≤ 18ns, t<sub>f</sub> ≤ 8.0ns.



**CONNOR-WINFIELD CORPORATION**  
West Chicago, Illinois 60185, U.S.A.

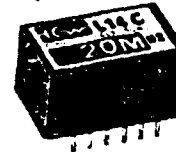
# DIP CRYSTAL OSCILLATORS

BULLETIN 76AAB4

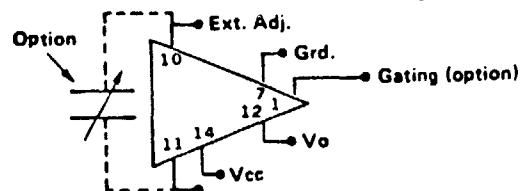
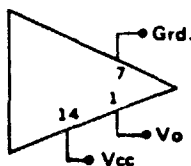
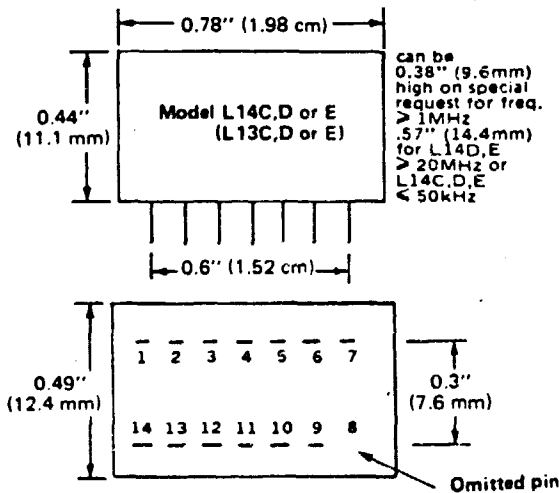
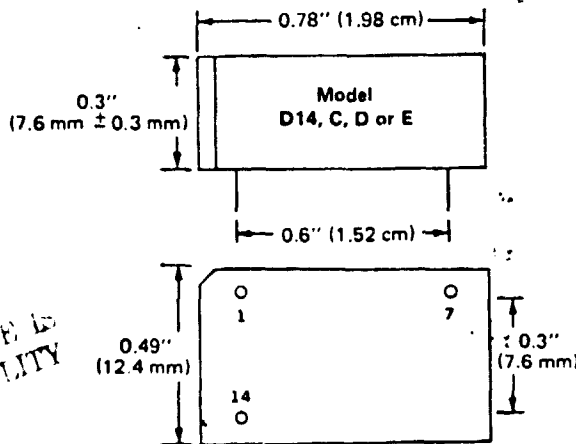
## MODELS

## D14C, D, E

## L14C, D, E (L13C, D, E)



SPECIFICATIONS	MODEL D14C, D or E	MODEL L14C, D or E (L13C, D or E)*
Fixed Frequencies Available	1MHz to 20 MHz	Model L14C (L13C): 0.1 Hz to 25 MHz L14D, E (L13D, E): 0.1 Hz to 60 MHz
Frequency Tolerance	Model D14C: $\pm .005\%$ , 0°C to +50°C D14D: $\pm .0075\%$ , 0°C to +65°C D14E: $\pm .01\%$ , -25°C to +75°C	L14C (L13C): $\pm .001\%$ , 0°C to +50°C L14D (L13D): $\pm .0025\%$ , 0°C to +65°C <b>L14E, L13E</b> : $\pm .005\%$ , -25°C to +75°C External Frequency Adjust Option of $\pm 30$ ppm Tolerances to $\pm .0005\%$ , 0°C to +50°C are available
Output Waveform	Squarewave, Logic 0 < 0.4V, Logic 1 > 2.4V into a 200Ω to 2KΩ Load	
Amplitude and Load	Duty Cycle < 10 MHz, 49/51-51/49 Duty Cycle > 10 MHz, 30/70-70/30	Duty Cycle < 10 MHz, 59/51-51/49 Duty Cycle > 10 MHz, 30/70-70/30
Supply Voltage	5 Vdc $\pm 5\%$	
Supply Current	10 ma to 30 ma depending on frequency	10 ma to 125 ma depending on frequency
Termination	3 pin DIP to plug into single IC socket, with gold plated pins, .017" (0.43mm) diameter	*14 pin DIP to plug into single IC socket with gold plated pins L14C, D or E: Flat Pins, .016" (0.4 mm) x .023" (0.6 mm) L13C, D or E: Square Pins, .017" (0.4 mm) x .017" (0.4 mm)
Availability	2 to 6 weeks ARD, faster delivery possible with premium charge in some cases	
Price Range Special prices available for larger quantities.	Less than \$50 depending on specs & quantity	Unit Price Range: \$61 to \$222 depending on specifications & quantity



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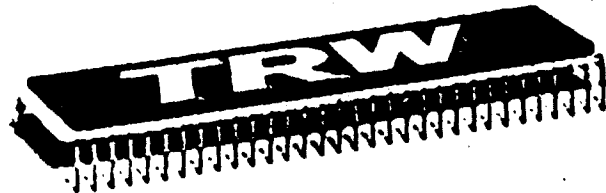
### 3. ANALOG AND DATA CONVERSION COMPONENT DATA

# TRW

## MONOLITHIC VIDEO A/D CONVERTER PRELIMINARY INFORMATION

### MODEL : TDC1007J

The TRW TDC1007J is an 8 bit fully-parallel (flash) A/D converter capable of digitizing an analog signal at rates from dc to 30 megasamples per second (MSPS). It will accurately sample, without an external sample-and-hold circuit, input signals with frequency components up to 7 MHz (comparator 3 dB bandwidth of 40 MHz).



A single convert signal controls the unit operation, which consists of 255 strobed comparators, combining logic, and an output buffer register. Recovery from a full scale step input occurs within 20 nsec. Controls are provided for straight binary or offset 2s complement output coding, in true or inverted sense.

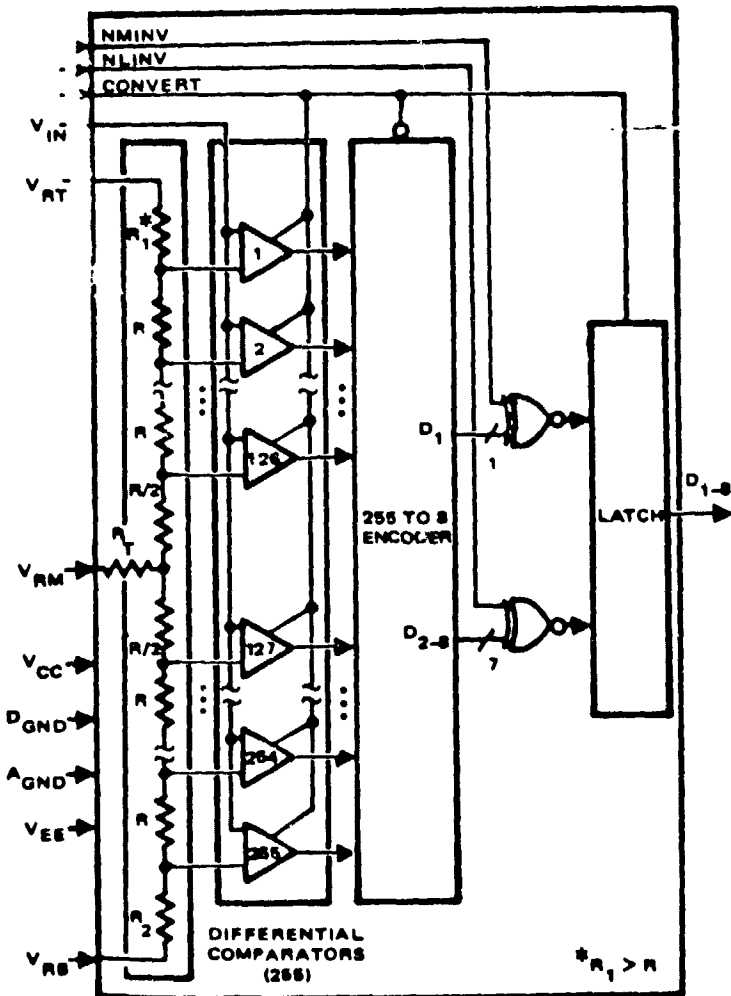
The TDC1007J is patented (No. 3283170), with other patents pending.

#### FEATURES

- 8 bit resolution
- 30 MSPS
- No sample-and-hold circuit required
- Aperture jitter 30 pS
- Differential phase 0.5°
- Differential gain 1.5%
- Binary or 2s complement output
- Monolithic, bipolar, TTL
- 64-pin ceramic DIP
- 2.0 W power dissipation

#### APPLICATIONS

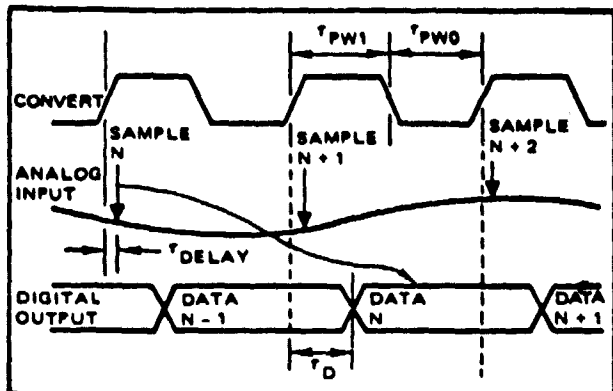
- Video data conversion
  - 3X or 4X NTSC color
  - 3X or 4X PAL color
- Radar data conversion
- High speed multiplexed data acquisition



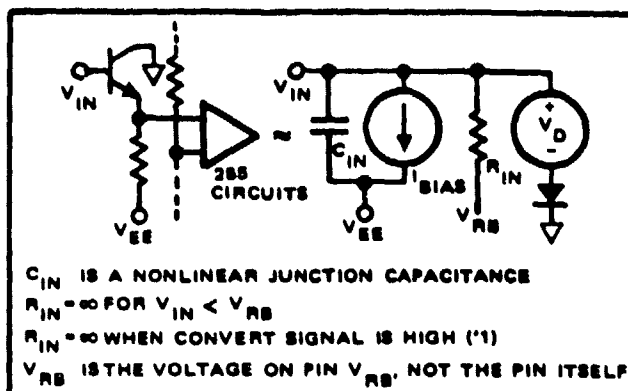
**TRW LSI PRODUCTS**

P.O. BOX 1125, REDONDO BEACH, CALIFORNIA 90278  
(213) 535-1831

# TDC1007J

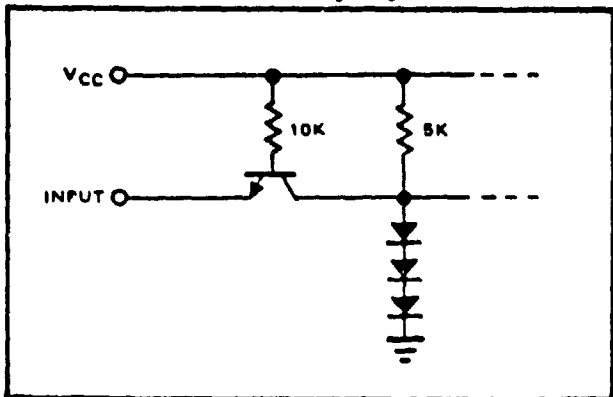


Timing Diagram

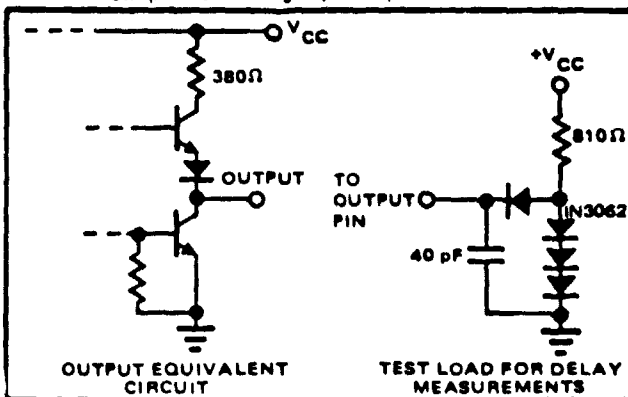


$C_{IN}$  IS A NONLINEAR JUNCTION CAPACITANCE  
 $R_{IN} = \infty$  FOR  $V_{IN} < V_{RB}$   
 $R_{IN} = \infty$  WHEN CONVERT SIGNAL IS HIGH (\*)  
 $V_{RB}$  IS THE VOLTAGE ON PIN  $V_{RB}$ , NOT THE PIN ITSELF

Simplified Analog Input Equivalent Circuit (Note 1)



Digital Input Equivalent Circuit



Output Circuits

performance characteristics, typical over recommended operating temperature range

PARAMETER	TEST CONDITIONS		UNIT
Resolution		8 0.39	Bits %
Dynamic Range		2.0	V
Linearity Error	0 to 20 Msp conversion rate	0.2	%
Offset Error, Top	$V_{RT} = 0V$ $V_{RB} = -2.0V$ (Note 2)	+30	mV
Bottom	$V_{RT} = 0V$ $V_{RB} = -2.0V$ (Note 2)	-24	mV
Aperture Jitter		30	pS
Differential Phase	NTSC or PAL ramp modulated with a 40 IRE color subcarrier (Note 3)	0.5	Deg
Differential Gain		1.5	%
Bandwidth, Small Signal			
3.0 dB		40	MHz
0.1 dB		7	MHz
Transient Response	Recovery from full step input	20	nsec
Signal-to-Noise Ratio	10 MHz bandwidth 25 Msp conversion rate (Note 4)		
Peak Signal/RMS Noise	1.248 MHz input 2.438 MHz input	55 54	dB dB
RMS Signal/RMS Noise	1.248 MHz input 2.438 MHz input	46 45	dB dB
Noise Power Ratio	DC to 8 MHz white noise bandwidth 40 loading 1.248 MHz slot 20 Msp conversion rate (Note 5)	36.5	dB

## SPECIFICATIONS

## absolute maximum ratings

Supply voltage, $V_{CC}$	0.0 to +7.0 V
$V_{EE}$	0.0 to -7.0 V
Input voltage, digital	-0.5 to +5.5 V
analog; signal	+0.5 V to $V_{EE}$
reference	+0.5 V to $V_{EE}$
Output voltage	-0.5 to +7.0 V
Temperature, operating, ambient	0 to +70°C
junction	+175°C
lead, soldering (10 seconds)	+300°C
storage	-65 to +150°C

## recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage, $V_{CC}$	+4.5	+5.0	+5.5	V
$V_{EE}$	-5.75	-6.0	-6.25	V
Reference input, $V_{RT}$	-1.1	0	+0.1	V
$V_{RB}$	-0.9	-2.0	-2.1	V
Convert pulse width, $T_{PW1}$	15			nsec
$T_{PW0}$	25			nsec
Operating Ambient Temperature Range	0	+25	+70	°C

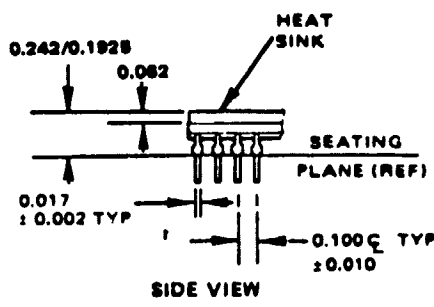
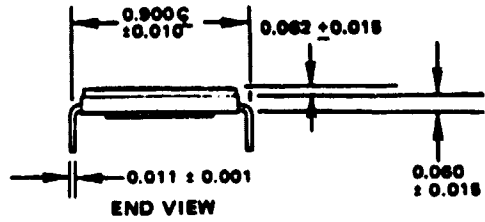
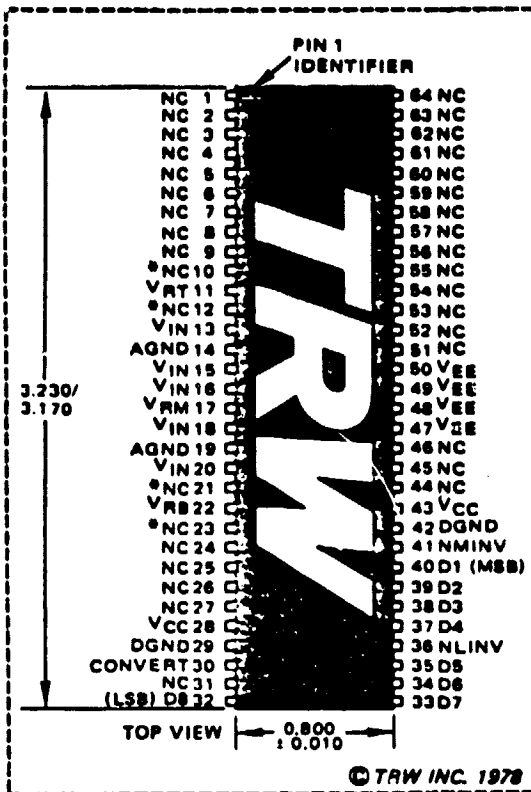
## interface specifications over recommended operating temperature range

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>Power Supply</b>					
$I_{CC}$ Supply Current	$V_{CC} = \text{MAX}$			35	mA
$I_{EE}$ Supply Current	$V_{EE} = \text{MAX}$			-400	mA
<b>Analog</b>					
Signal Input					
$V_{IN}$ Input Voltage Range		0		-2.0	V
$R_{IN}$ Equivalent Input Impedance	$V_{EE} = \text{MAX}$	5		$\infty$	K
$C_{IN}$ Input Capacitance				300	pF
$I_{BIAS}$ Constant Input Bias	$V_{EE} = \text{MAX}$			500	$\mu\text{A}$
$I_B$ Clock Synchronous Bias	$V_{EE} = \text{MAX}$			200	$\mu\text{A}$
Reference Input					
$I_{RT}$ Reference Current, Top	$V_{EE} = \text{MAX}$ $V_{RT} = 0.0 \text{ V}$ $V_{RB} = -2.0 \text{ V}$			+30	mA
$I_{RB}$ Reference Current, Bottom	$V_{EE} = \text{MAX}$ $V_{RT} = 0.0 \text{ V}$ $V_{RB} = -2.0 \text{ V}$			-30	mA
$R$ Reference Resistor		0.26	0.31		$\Omega$
$R_T$ Trim Resistor			15		k $\Omega$
<b>Digital</b>					
Inputs					
$V_{IH}$ High Level Input Voltage		2.0			V
$V_{IL}$ Low Level Input Voltage				0.8	V
$I_{IH}$ High Level Input Current				7.5	$\mu\text{A}$
$I_{IL}$ Low Level Input Current				-1.0	mA
Outputs					
$V_{OH}$ High Level Output Voltage	$V_{CC} = \text{NOM}$ $I_{OH} = -0.4 \text{ mA}$	2.4			V
$V_{OL}$ Low Level Output Voltage	$V_{CC} = \text{NOM}$ $I_{OL} = 4.0 \text{ mA}$			0.4	V

switching characteristics over recommended operating temperature range,  $V_{CC} = 5.0$ ,  $V_{EE} = -6.0 \text{ V}$ 

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$F_s$ Maximum Conversion Rate		20	30		MHz
$T_{DELAY}$ Aperture Delay			10		nsec
$T_D$ Digital Output Delay		15	30	45	nsec

PACKAGE INFORMATION



- NOTES:
- DIMENSIONS IN INCHES
  - ALL POWER AND GROUND PINS MUST BE CONNECTED
  - DGND IS +5V GROUND AND REFERENCES TTL I/O BUFFERS ONLY
  - ALL VIN PINS MUST BE EXTERNALLY CONNECTED

\* RECOMMENDED CONNECTION TO ANALOG GROUND FOR INTERELECTRODE SHIELDING

MATING CONNECTORS INCLUDE:

- Cambion 703-4064-01-04-12
- Robinson-Nugent ICN-649-55-G
- Textool 232-2601-00-0605 (2 required)

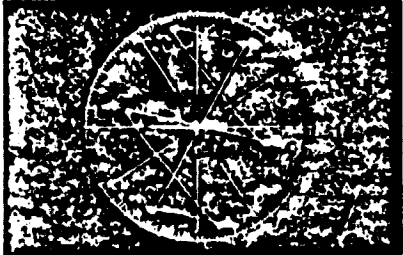
- Low-Profile, Solder Tail, Tin Plate, Jam Socket
- Low-Profile, Solder Tail, Gold Plate, Jam Socket
- Solder Tail, Nickel Plate, Zero Insertion Force Socket



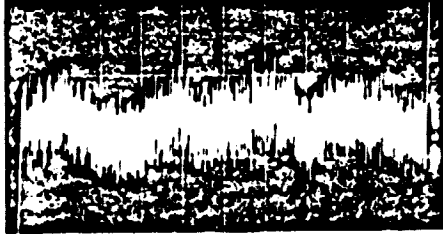
Differential Phase - 40 IRE Modulated NTSC Ramp - 14.3 MSPS Unlocked (Note 3)



Differential Gain - 40 IRE Modulated NTSC Ramp - 14.3 MSPS Unlocked (Note 3)



Vector Diagram - NTSC Color Bars 14.3 MSPS Unlocked (Note 3)



Linearity - 20 MSPS (Note 6)

## OUTPUT CODING

STEP	Range		Binary		Offset 2s Complement	
	-2.0000V FS 7.8431 mV STEP	-2.0480V FS 8.000 mV STEP	True NMINV = 1 NLINV = 1	Inverted 0 0	True 0 1	Inverted 1 0
	000	0.0000V	0.0000V	00000000	11111111	10000000
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	0.9961V	-1.0160V	01111111	10000000	11111111	00000000
128	-1.0039V	-1.0240V	10000000	01111111	00000000	11111111
129	-1.0118V	-1.0320V	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
255	-2.0000V	-2.0400V	11111111	00000000	01111111	10000000

NMINV and NLINV are to be considered D.C. controls. They may be tied to +5V for a logical '1' and tied to ground for a logical '0'.

## NOTES

1. Analog Input. The analog input circuit of Figure 2 is a simplification that is adequate for most interface circuit designs. As shown, the input consists of 255 parallel emitter-follower stages driving voltage comparators.  $C_{IN}$  represents the nonlinear emitter-follower junction capacitance, and  $I_{BIAS}$  is the constant input bias current.  $R_{IN}$  is a linear resistive model of the change in input current due to comparator switching as the input moves through the range. This component does not vary after the input range is exceeded, as no additional comparators can be switched, but do note that the comparator current is zero ( $R = \infty$ ) while the convert signal is high ('1'). The diode voltage in the model represents the base-collector junctions of the emitter-follower transistors, which can conduct if the input exceeds +0.7 V.

The 300 pF maximum input capacitance presents a drive requirement similar to that of a 75 ohm coaxial cable, though its nonlinear nature and dc bias characteristics make it unsuited to being driven directly by a 75 ohm line: a source impedance of less than 10 ohms is indicated for optimal performance. One method of providing this drive is demonstrated on the TDC1007PCB (page 9). This is not necessarily the best or most cost effective technique, but it performs well. The LH0033, or equivalent, buffer amplifier also works, and common analog line driver circuits can be adapted to the task. Through the use of NMINV and NLINV, either inverting or noninverting buffers may be accommodated.

2. Reference Inputs. The resistive divider that provides a reference voltage to each of the 255 comparator circuits has both ends and a midpoint tap available to the user, allowing considerable flexibility in the circuit operation. The nominal operating range is 0 to -2 V, requiring approximately 0 V on  $V_{RT}$  and -2 V on  $V_{RB}$ . This is not to preclude operation over a smaller range, as the circuit will function with a total range of less than 1 volt; but some performance characteristics will change. For example, a quantizer circuit has two major sources of dc linearity error: resistor ladder variations and comparator offset voltages. The former is scaled by a range reduction while the latter is not. The circuit should be operated with  $V_{RT}$  and  $V_{RB}$  within the recommended +0.1 to -2.1 V range, and  $V_{RB}$  at least 800 mV more negative than  $V_{RT}$ .

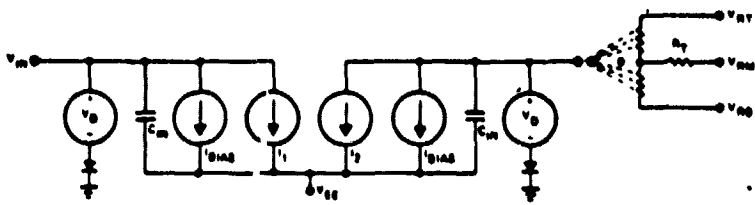
When one of the 255 comparators turns off due to a drop in analog input voltage, its bias current shifts from the analog input to the reference ladder. When the convert signal is high, comparator bias current is zero. This generates clock and signal related current noise on the reference inputs with a maximum amplitude of  $I_B$ , which can be relieved by ensuring adequate bypassing of  $V_{RT}$  and  $V_{RB}$  to analog ground. If the reference inputs are exercised dynamically, as in an AGC circuit, a bypass capacitor would be inappropriate and a low impedance reference source should be employed. The input-reference circuit is modeled on page 6.

Calibration is accomplished by adjusting  $V_{RT}$  and  $V_{RB}$  to set the first and 255th thresholds to the desired voltages. Note that  $R_1$  is greater than  $R_2$ , ensuring that calibration can be achieved with a positive voltage on  $V_{RT}$ . Assuming a 0 to -2 V desired range, continuously strobe the converter with -0.0039 V on the analog input, and adjust  $V_{RT}$  for output toggling between codes 000 and 001. Then apply -1.9961 V and adjust  $V_{RB}$  for toggling between codes 254 and 255. Rather than adjusting  $V_{RT}$ , it may be convenient to connect it to analog ground and calibrate the 0 V end of the range with a buffer offset control.  $V_{RB}$  is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed on the TDC1007PCB (page 7).

A midpoint tap,  $V_{RM}$ , allows the user to parallel the upper or lower half of the ladder with a trim resistor,  $R_T$ . This produces approximately 1/2 LSB adjustment of the linearity midpoint and is included for linearity compensation of an extended temperature version of this part. It is not necessary that adjustment be performed over the commercial temperature range (0 to 70°C). This pin can also be useful as a virtual ground reference for the input buffer amplifier if bipolar conversions are performed. Be aware of the inherent  $R_T$  impedance of this node; any load applied to  $V_{RM}$  will affect linearity.



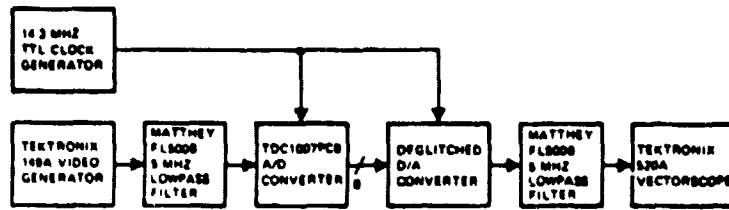
# TDC1007J



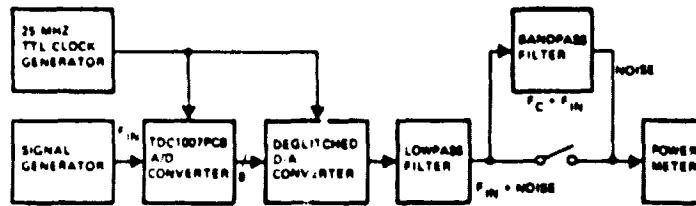
$$\begin{aligned}
 & \text{For } V_{RT} > V_{IN} > V_{RB} \\
 & I_1 = \left[ \frac{V_{IN} V_{RB}}{V_{RT} V_{RB}} \right] I_0 \quad I_2 = \left[ \frac{V_{RT} V_{IN}}{V_{RT} V_{RB}} \right] I_0 \\
 & \text{For } V_{IN} > V_{RT} \\
 & I_1 = I_2 = I_0 \quad \text{For } V_{IN} < V_{RB} \\
 & I_1 = I_2 = 0
 \end{aligned}$$

\*REFERENCE LOAD IS DISTRIBUTED ALONG THE REFERENCE DIVIDER  
 \*\* $I_1$  AND  $I_2 = 0$  WHEN CLOCK IS HIGH (1)

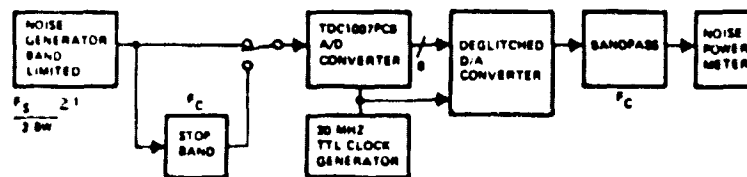
3. **NTSC Video Testing.** Measurement of video test signals is performed using the setup illustrated. The A/D and D/A converters are strobed at 14.3 MHz, unlocked from the color subcarrier, and the full composite signal encoded. No  $\sin(x)/x$  correction is performed. Differential phase and gain, in excess of that inherent in 8 bit quantization, are determined by measuring the deviation of the centerline of the trace on a vectorscope monitoring a reconstructed 40 IRE modulated ramp, sampled asynchronously with the color subcarrier. The small "glitches" in the differential gain photograph are due to color bar feedthrough within the test signal generator.



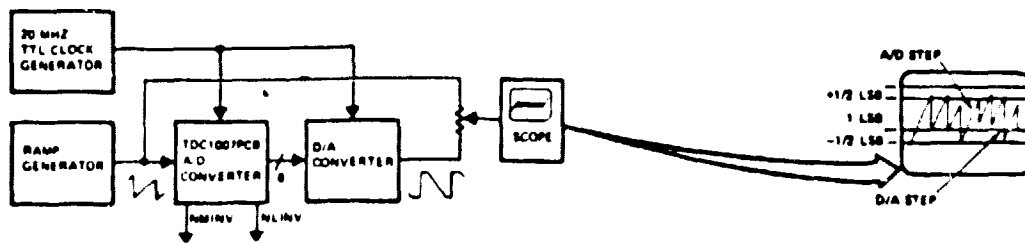
4. **Signal-to-Noise Ratio (SNR) Test.** A block diagram of the SNR test setup is shown below. The analog input to the A/D converter is a single tone with a p-p amplitude equal to the full scale range of the A/D. Power in the reconstructed waveform is measured over a selected bandwidth ( $< f_s/2$ ) and remeasured when the fundamental tone frequency is filtered out at the D/A output. The ratio of the two power readings is the SNR. An ideal A/D converter has a SNR equal to  $6n+1.8$  dB, where  $n$  = number of bits,  $n > 4$ . This is the RMS signal-to-RMS noise value. Peak signal-to-RMS noise theory is approximately 9 dB higher.



5. **Noise Power Ratio Test.** A block diagram of the NPR test setup is given below. Bandlimited gaussian noise is the analog input to the A/D converter. Power in the reconstructed waveform is measured in a selected frequency slot and then remeasured with the same frequency slot notched out of the input signal spectrum. The ratio of the two power readings reflects the noise performance, dynamic nonlinearity of the A/D, and aperture effects. The theoretical NPR for the test performed is 40.5 dB.



6. **Linearity Testing.** Device linearity is readily determined with the test setup below. The A/D output is inverted using the NMINV and NLINV controls. The input is slightly overdriven with a slow ramp, the output and input are summed, and the results displayed on an oscilloscope.





# Operational Amplifiers

LH0032/LH0032C

## LH0032/LH0032C ultra fast FET operational amplifier

### general description

The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

- Low input bias current                    20 pA max
- Offset null with single pot
- Low input offset voltage                2 mV max
- No compensation for gains above 50

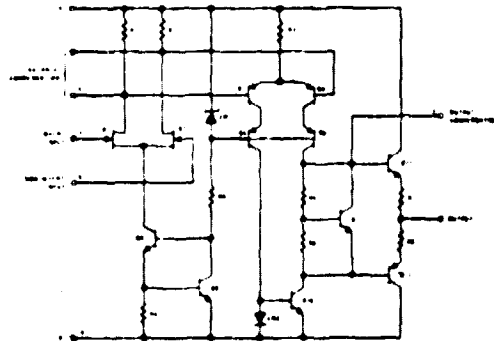
The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range -55°C to +125°C and the LH0032C is guaranteed from -25°C to +85°C.

### features

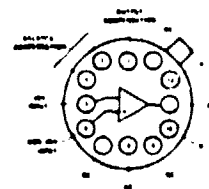
- High slew rate                                500 V/μs
- High bandwidth                              70 MHz
- High input impedance                      10<sup>12</sup>Ω

For information on other National operational amplifiers, see listing on last page.

### schematic and connection diagrams



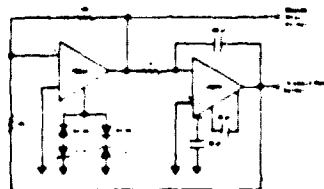
Metal Can Package



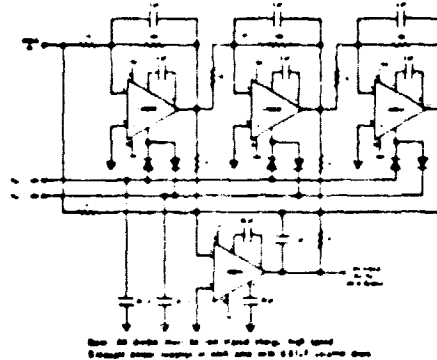
Order Number LH0032G or LH0032CG  
See Package 6

### typical applications

1 MHz Function Generator



DC to Video Log Amplifier



See all other pins to see exact wiring. High speed through-hole package is available with 0.1% accuracy.



**absolute maximum ratings**

Supply Voltage	±18V
Input Voltage	±V <sub>S</sub>
Differential Input Voltage	±30V
Power Dissipation	See curve
Operating Temperature Range LM0032	-55°C to +125°C
LM0032C	-25°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

**dc electrical characteristics (Note 1)**

PARAMETER	CONDITIONS	LM0032			LM0032C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V <sub>S</sub> = ±18V R <sub>L</sub> ≤ 100k T <sub>A</sub> = 25°C V <sub>S</sub> = ±18V R <sub>L</sub> ≤ 100k		2	5		5	15	mV
				10			20	mV
Average Offset Voltage Drift	R <sub>L</sub> ≤ 100k		25			25	μV/°C	
Input Bias Current	T <sub>A</sub> = 25°C		10	100		25	200	pA
				50			150	nA
Input Offset Current	T <sub>A</sub> = 25°C		5	25		10	50	nA
				25			5	nA
Large Signal Voltage Gain	V <sub>S</sub> = ±18V V <sub>OUT</sub> = ±10V f = 1kHz R <sub>L</sub> = 1kΩ T <sub>A</sub> = 25°C V <sub>S</sub> = ±18V V <sub>OUT</sub> = ±10V f = 1kHz R <sub>L</sub> = 1kΩ	60	70		60	70		dB
		57			57			dB
Input Voltage Range	V <sub>S</sub> = ±18V	±10	±12		±10	±12		V
Output Voltage Swing	V <sub>S</sub> = ±18V R <sub>L</sub> = 1kΩ	±10	±13.5		±10	±13		V
Power Supply Rejection Rate	V <sub>S</sub> = ±18V ΔV <sub>S</sub> = ±10V	50	60		50	60		dB
Common Mode Rejection Rate	V <sub>S</sub> = ±18V ΔV <sub>CM</sub> = 10V	50	60		50	60		dB
Supply Current	V <sub>S</sub> = ±18V T <sub>A</sub> = 25°C		15	20		20	22	mA

**ac electrical characteristics (Note 2)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	A <sub>V</sub> = +1, ΔV <sub>IN</sub> = 20V	350	500		V/μs
Settling Time to 1% of Final Value	A <sub>V</sub> = -1, ΔV <sub>IN</sub> = 20V		100		ns
Settling Time to 0.1% of Final Value	A <sub>V</sub> = -1, ΔV <sub>IN</sub> = 20V		300		ns
Small Signal Rise Time	A <sub>V</sub> = +1, ΔV <sub>IN</sub> = 1V		8	20	ns
Small Signal Delay Time	A <sub>V</sub> = +1, ΔV <sub>IN</sub> = 1V		10	25	ns

Note 1: These specifications apply for ±18V ≤ V<sub>S</sub> ≤ ±18V and -55°C to +125°C for the LM0032 and -25°C to +85°C for the LM0032C

Note 2: These specifications apply for V<sub>S</sub> = ±18V, R<sub>L</sub> = 1kΩ and T<sub>A</sub> = 25°C



## +10V PRECISION VOLTAGE REFERENCE

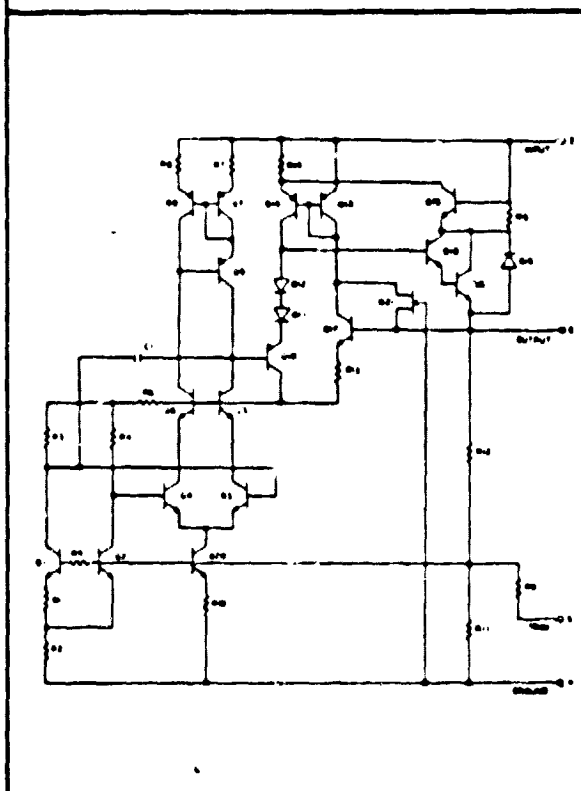
### GENERAL DESCRIPTION

The REF-01 Precision Voltage Reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 12 to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-01 an excellent choice whenever a stable voltage reference is required, such as in D/A and A/D converters, in portable instruments, and in digital voltmeters. Full military temperature range devices with screening to MIL-STD 883A are available.

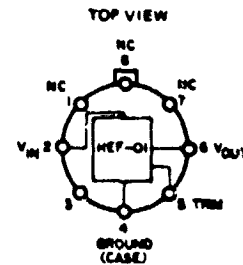
### FEATURES

- Adjustable 10 Volt Output ..... ±3%
- Excellent Temperature Stability ..... 3 ppm/°C
- Low Noise ..... 20µVp-p
- Low Power ..... 15mW
- Wide Input Voltage Range ..... 12 to 40V
- High Load Driving Capability ..... 20mA
- No External Components
- Short Circuit Proof
- MIL-STD-883A Screening Available

### SIMPLIFIED SCHEMATIC



### PIN CONNECTIONS AND ORDERING INFORMATION



TO 99 (J/Juffra)

ORDER REF-01AJ  
REF-01J  
REF-01EJ  
REF-01HJ  
REF-01CJ  
REF-01DI

Military Temperature Range Devices  
with MIL-STD-883A Class B Processing

ORDER REF01-883AJ  
REF01-883J

## ABSOLUTE MAXIMUM RATINGS

Input Voltage REF-01, A, E, H REF-01C, D	40 V 30 V	Operating Temperature Range	
Power Dissipation (see note)	500mW	REF-01A, REF-01	-55°C to +125°C
Output Short Circuit Duration (to ground or $V_{IN}$ )	Indefinite	REF-01E, REF-01H, REF-01D REF-01C.	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	Note: Derate at 7.1mW/°C above 80°C ambient temperature.	
Lead Temperature (Soldering, 60 sec)	300°C		

## ELECTRICAL CHARACTERISTICS

			REF-01A			REF-01			
These specifications apply for $V_{IN} = +15V$ , $T_A = 25^\circ C$ , unless otherwise noted.									
Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Output Voltage	$V_O$	$I_L = 0mA$	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	$\Delta V_{trim}$	$R_D = 10k\Omega$	:3.0	:3.3	-	:3.0	:3.3	-	%
Output Voltage Noise	$e_{n-p}$	0.1Hz to 10MHz (Note 5)	-	20	30	-	20	30	$\mu V_{p-p}$
Input Voltage Range	$V_{IN}$		12	-	40	12	-	40	V
Line Regulation (Note 4)		$V_{IN} = 13$ to 33V	-	0.006	0.010	-	0.006	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to 10mA	-	0.005	0.008	-	0.006	0.010	%/mA
Turn-on Settling Time	$t_{on}$	To :0.1% of final value	-	5.0	-	-	5.0	-	$\mu sec$
Quiescent Current	$I_{SQ}$	No Load	-	1.0	1.4	-	1.0	1.4	mA
Load Current	$I_L$		10	21	-	10	21	-	mA
Sink Current	$I_S$		-0.3	-0.5	-	-0.3	-0.5	-	mA
Short Circuit Current	$I_{SC}$	$V_O = 0$	-	30	-	-	30	-	mA
The following specifications apply for $V_{IN} = +15V$ , $-55^\circ C < T_A < +125^\circ C$ and $I_L = 0mA$ , unless otherwise noted.									
Output Voltage Change with Temperature (Notes 1 and 2)	$\Delta V_{OT}$	$0^\circ < T_A < +70^\circ C$	-	0.02	0.06	-	0.07	0.17	%
		$-55^\circ < T_A < +125^\circ C$	-	0.06	0.15	-	0.18	0.45	%
Output Voltage Temperature Coefficient	$TCV_O$	(Note 3)	-	3	8.5	-	10	25	ppm/°C
Change in $V_O$ Temperature Coefficient with Output Adjustment		$R_D = 10k\Omega$	-	0.7	-	-	0.7	-	ppm/°C/%
Line Regulation ( $V_{IN} = 13$ to 33V) (Note 4)		$0^\circ < T_A < +70^\circ C$	-	0.007	0.012	-	0.007	0.012	%/V
		$-55^\circ < T_A < +125^\circ C$	-	0.009	0.015	-	0.009	0.015	%/V
Load Regulation ( $I_L = 0$ to 8mA) (Note 4)		$0^\circ < T_A < +70^\circ C$	-	0.008	0.010	-	0.007	0.012	%/mA
		$-55^\circ < T_A < +125^\circ C$	-	0.007	0.012	-	0.009	0.015	%/mA

NOTE 1  $\Delta V_{OT}$  is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2  $\Delta V_{OT}$  specification applies trimmed to 10.000V or untrimmed

NOTE 3  $TCV_O$  is defined as  $\Delta V_{OT}$  divided by the temperature range, i.e.  $TCV_O(0^\circ \text{ to } 70^\circ C) = \frac{\Delta V_{OT}(0^\circ \text{ to } 70^\circ C)}{70^\circ C}$   
and  $TCV_O(-55^\circ \text{ to } 125^\circ C) = \frac{\Delta V_{OT}(-55^\circ \text{ to } 125^\circ C)}{180^\circ C}$

NOTE 4 Line and Load Regulation specifications include the effects of self heating

NOTE 5 Parameters not 100% tested, 90% of units meet this specification

# Am124/224/324 Am124A/224A/324A

## Quad Op Amps

### Distinctive Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated
- Internally frequency compensated for unity gain
- Large dc voltage gain – 100dB
- Wide bandwidth (unity gain) – 1MHz (temperature compensated)
- Wide power supply range:  
Single supply – 3V to 30V  
Dual supplies –  $\pm 1.5V$  to  $\pm 15V$
- Very low supply current drain (800 $\mu A$ ) – essentially independent of supply voltage (1mW/op amp at +5V)
- Low input biasing current – 45nA (temperature compensated)
- Low input offset voltage – 2mV and offset current – 5nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing – 0V to  $V^+ - 1.5V$

<p><b>FUNCTIONAL DESCRIPTION</b></p> <p>The Am124 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed primarily to operate from a single power supply over a wide range of voltages. These devices can also operate from split power supplies and the low power supply current drain is independent of the magnitude of the power supply voltage.</p> <p>Functional applications consist of all the conventional op amp circuits which can now be more easily implemented in single power supply systems along with transducer amplifiers and dc gain blocks.</p>	<p style="text-align: center;"><b>CONNECTION DIAGRAM</b> Top View</p> <p style="text-align: center; font-size: small;">Note: Pin 1 is marked for orientation</p>																																																			
<p style="text-align: center;"><b>ORDERING INFORMATION</b></p> <table border="1" style="width: 100%; border-collapse: collapse; font-size: small;"> <thead> <tr> <th>Part Number</th> <th>Package Type</th> <th>Temperature Range</th> <th>Order Number</th> </tr> </thead> <tbody> <tr> <td rowspan="3">Am324</td> <td>Hermetic DIP</td> <td>0°C to +70°C</td> <td>LM324D</td> </tr> <tr> <td>Molded DIP</td> <td>0°C to +70°C</td> <td>LM324N</td> </tr> <tr> <td>Dice</td> <td>0°C to +70°C</td> <td>LD324</td> </tr> <tr> <td rowspan="2">Am224</td> <td>Hermetic DIP</td> <td>25°C to +85°C</td> <td>LM224D</td> </tr> <tr> <td>Hermetic DIP</td> <td>55°C to +125°C</td> <td>LM124D</td> </tr> <tr> <td rowspan="3">Am124</td> <td>Flat Pack</td> <td>-55°C to +125°C</td> <td>LM124F</td> </tr> <tr> <td rowspan="2">Dice</td> <td>55°C to +125°C</td> <td>LM124</td> </tr> <tr> <td>Hermetic DIP</td> <td>0°C to +70°C</td> <td>LM324AD</td> </tr> <tr> <td rowspan="3">Am324A</td> <td>Molded DIP</td> <td>0°C to +70°C</td> <td>LM324AN</td> </tr> <tr> <td rowspan="2">Dice</td> <td>0°C to +70°C</td> <td>LM324A</td> </tr> <tr> <td>Hermetic DIP</td> <td>25°C to +85°C</td> <td>LM224AD</td> </tr> <tr> <td rowspan="3">Am224A</td> <td>Hermetic DIP</td> <td>55°C to +125°C</td> <td>LM124AD</td> </tr> <tr> <td rowspan="2">Dice</td> <td>-55°C to +125°C</td> <td>LM124AF</td> </tr> <tr> <td>Dice</td> <td>-55°C to +125°C</td> <td>LD124A</td> </tr> </tbody> </table>	Part Number	Package Type	Temperature Range	Order Number	Am324	Hermetic DIP	0°C to +70°C	LM324D	Molded DIP	0°C to +70°C	LM324N	Dice	0°C to +70°C	LD324	Am224	Hermetic DIP	25°C to +85°C	LM224D	Hermetic DIP	55°C to +125°C	LM124D	Am124	Flat Pack	-55°C to +125°C	LM124F	Dice	55°C to +125°C	LM124	Hermetic DIP	0°C to +70°C	LM324AD	Am324A	Molded DIP	0°C to +70°C	LM324AN	Dice	0°C to +70°C	LM324A	Hermetic DIP	25°C to +85°C	LM224AD	Am224A	Hermetic DIP	55°C to +125°C	LM124AD	Dice	-55°C to +125°C	LM124AF	Dice	-55°C to +125°C	LD124A	<p style="text-align: center;"><b>SCHEMATIC DIAGRAM (Each Amplifier)</b></p>
Part Number	Package Type	Temperature Range	Order Number																																																	
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ELECTRICAL CHARACTERISTICS (V<sup>+</sup> = +5.0V<sub>DC</sub>, Note 4)

Parameter	Conditions	Am124A			Am224A			Am324A			Am124/Am224			Am324			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>OS</sub> Offset Voltage	T <sub>A</sub> = 25°C (Note 5)		1.0	2.0		1.0	3.0		2.0	3.0		12.0	15.0		12.0	17.0	
I <sub>B</sub> Bias Current (±BI)	I <sub>N</sub> (±) @ I <sub>N</sub> (-); T <sub>A</sub> = 25°C		20	50		40	80		45	100		45	100		45	200	
I <sub>OS</sub> Offset Current	I <sub>N</sub> (+) - I <sub>N</sub> (-); T <sub>A</sub> = 25°C		2.0	10		2.0	15		5.0	20		12.0	120		15.0	150	
V <sub>CM</sub> Common-Mode Voltage Range (Note 7)	V <sup>+</sup> = 30V <sub>DC</sub> ; T <sub>A</sub> = 25°C	0		V <sup>+</sup> - 1.5	0		V <sup>+</sup> - 1.5	0		V <sup>+</sup> - 1.5	0		V <sup>+</sup> - 1.5	0		V <sup>+</sup> - 1.5	
I <sub>Q</sub> Quiescent Current	R <sub>L</sub> = V <sub>CC</sub> = 30V R <sub>S</sub> = ∞		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0		1.5	3.0	
V <sub>OL</sub> Output Voltage Swing	V <sup>+</sup> = 15V <sub>DC</sub> (For large V <sub>O</sub> swing) R <sub>L</sub> = 2.0kΩ; T <sub>A</sub> = 25°C	50		100	50		100	75		100	50		100	25		100	
C <sub>MLT</sub> Milliwatt Dissipation Rate	DC; T <sub>A</sub> = 25°C	70		85	70		85	80		85	70		85	65		75	
P <sub>SD</sub> Supply Current Dissipation Rate	DC; T <sub>A</sub> = 25°C	65		100	65		100	65		100	65		100	65		100	
A <sub>OL</sub> Open-Loop Voltage Gain (Note 8)	f = 10Hz to 20kHz; T <sub>A</sub> = 25°C (Typical)			-120			-120			-120			-120			-120	
I <sub>OL</sub> Output Current	Source	V <sub>IN</sub> = +1.0V <sub>DC</sub> ; V <sub>IN</sub> = -0.5V <sub>DC</sub> V <sup>+</sup> = 15V <sub>DC</sub> ; T <sub>A</sub> = 25°C	20		40	20		40	20		40	20		40	20		40
	Sink	V <sub>IN</sub> = +1.0V <sub>DC</sub> ; V <sub>IN</sub> = -0.5V <sub>DC</sub> V <sup>+</sup> = 15V <sub>DC</sub> ; T <sub>A</sub> = 25°C	10		20	10		20	10		20	10		20	10		20
		V <sub>IN</sub> = +1.0V <sub>DC</sub> ; V <sub>IN</sub> = -0.5V <sub>DC</sub> T <sub>A</sub> = 25°C; V <sub>CC</sub> = 200mV <sub>DC</sub>	12		50	12		50	12		50	12		50	12		50
I <sub>CL</sub> Collector Current (Ground)	T <sub>A</sub> = 25°C (Note 2)		40	60		40	60		40	60		40	60		40	60	
V <sub>IN</sub> Input Voltage	Signal			4.0			4.0			5.0			7.0			10.0	
R <sub>IN</sub> Input Resistance	R <sub>S</sub> = 0Ω		7.0	20		7.0	20		7.0	30		7.0	30		7.0	30	
I <sub>IN</sub> Input Current	I <sub>N</sub> (+) - I <sub>N</sub> (-)			30			30			75			100			150	
I <sub>OP</sub> Output Current	I <sub>N</sub> (+) @ I <sub>N</sub> (-)		10	200		10	200		10	300		10	300		10	300	
I <sub>OS</sub> Offset Current	I <sub>N</sub> (+) @ I <sub>N</sub> (-)		40	100		40	100		40	200		40	300		40	500	
V <sub>CM</sub> Common-Mode Voltage Range (Note 7)	V <sup>+</sup> = 30V <sub>DC</sub>	0		V <sup>+</sup> - 2.0	0		V <sup>+</sup> - 2.0	0		V <sup>+</sup> - 2.0	0		V <sup>+</sup> - 2.0	0		V <sup>+</sup> - 2.0	
V <sub>OL</sub> Output Voltage Swing	V <sup>+</sup> = 15V <sub>DC</sub> (For large V <sub>O</sub> swing) R <sub>L</sub> = 2.0kΩ	25		25		25	25		25	25		25	25		25	25	
V <sub>OL</sub> Output Voltage Swing	V <sub>OL</sub>	V <sup>+</sup> = 10V <sub>DC</sub> ; R <sub>L</sub> = 10kΩ	27		28	27		28	27		28	27		28	27		28
	V <sub>OL</sub>	V <sup>+</sup> = 5.0V <sub>DC</sub> ; R <sub>L</sub> = 10kΩ	5.0		20	5.0		20	5.0		20	5.0		20	5.0		20
I <sub>OL</sub> Output Current	Source	V <sub>IN</sub> = +1.0V <sub>DC</sub> ; V <sub>IN</sub> = -0.5V <sub>DC</sub> V <sup>+</sup> = 15V <sub>DC</sub>	10		20	10		20	10		20	10		20	10		20
	Sink	V <sub>IN</sub> = +1.0V <sub>DC</sub> ; V <sub>IN</sub> = -0.5V <sub>DC</sub> V <sup>+</sup> = 15V <sub>DC</sub>	10		15	5.0		8.0	5.0		8.0	5.0		8.0	5.0		8.0
V <sub>IN</sub> Input Voltage	Note 7			V <sup>+</sup>			V <sup>+</sup>			V <sup>+</sup>			V <sup>+</sup>			V <sup>+</sup>	

- Notes:
- For operating at high temperatures, the Am324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The Am224 and Am124 can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers - use external resistors, where possible to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
  - Short circuits from the output to V<sup>+</sup> can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V<sup>+</sup>. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
  - This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V<sup>+</sup> voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
  - These specifications apply for V<sup>+</sup> = +5V<sub>DC</sub> and -85°C ≤ T<sub>A</sub> ≤ +125°C, unless otherwise stated. With the Am224, all temperature specifications are limited to -25°C ≤ T<sub>A</sub> ≤ +85°C and the Am324 temperature specifications are limited to 0°C ≤ T<sub>A</sub> ≤ +70°C.
  - V<sub>OL</sub> = 1.4V, R<sub>S</sub> = 0Ω with V<sup>+</sup> from 5V to 30V, and over the full input common mode range (0V to V<sup>+</sup> - 1.5V).
  - The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
  - The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is V<sup>+</sup> - 1.5V, but either or both inputs can go to +32V without damage.
  - Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

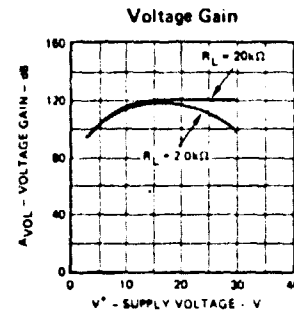
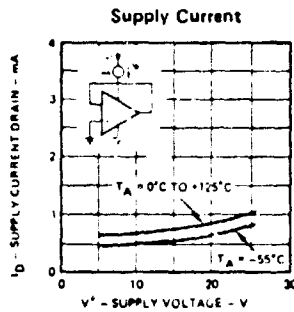
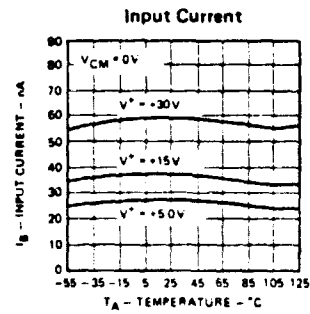
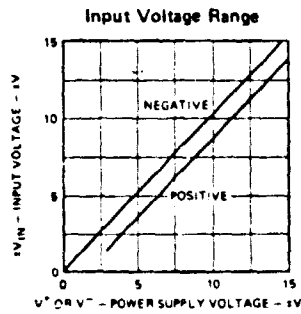


Am124/224/324 • Am124A/224A/324A

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage, $V^+$	32V or $\pm 16V$
Differential Input Voltage	32V
Input Voltage	-0.3V to +32V
Power Dissipation (Note 1)	
Molded DIP	570mA
Cavity DIP	900mA
Flat Pak (Am124F)	800mA
Output Short Circuit to GND (Note 2)	
(One Amplifier) $V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous
Input Current ( $V_{IN} < -0.3V_{OL}$ ) (Note 3)	50mA
Operating Temperature Range	
Am324/Am324A	0°C to +70°C
Am224/Am224A	-25°C to +85°C
Am124/Am124A	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

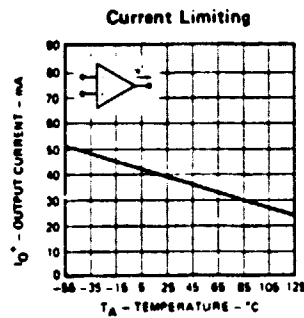
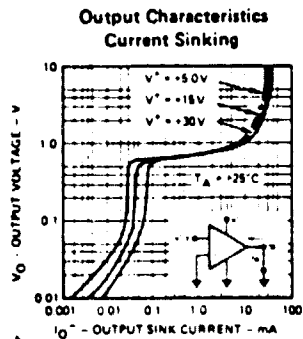
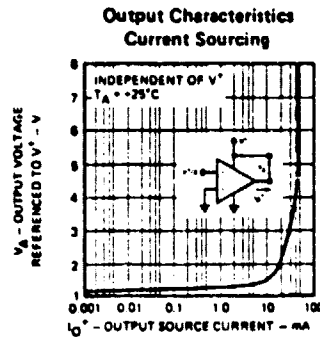
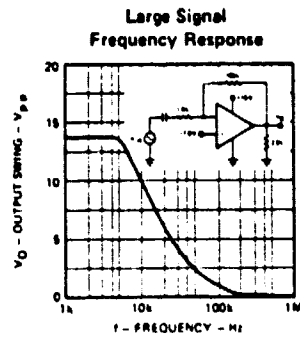
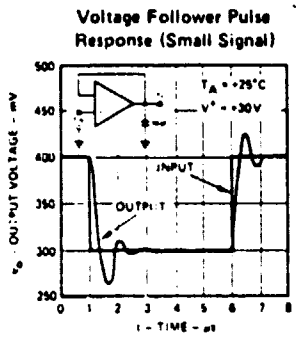
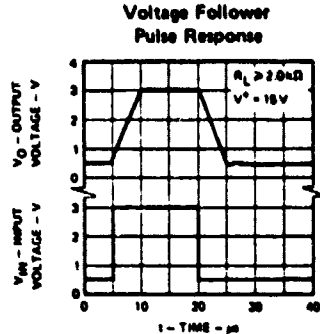
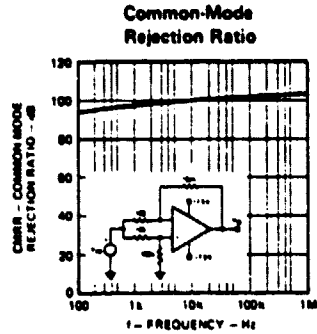
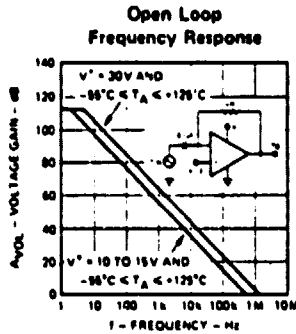
TYPICAL PERFORMANCE CURVES



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TYPICAL PERFORMANCE CURVES (Cont.)



LM139/LM239/LM339,  
LM139A/LM239A/LM339A, LM2901, LM3302

absolute maximum ratings

PARAMETER	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901		LM3302	
	MIN	MAX	MIN	MAX
Supply Voltage, V <sup>+</sup>	30 VDC to 110 VDC		30 VDC to 114 VDC	
Differential Input Voltage	30 VDC		30 VDC	
Input Voltage	-0.3 VDC to +30 VDC		-0.3 VDC to +30 VDC	
Power Dissipation (Note 1)	570 mW		570 mW	
Maximum SFP	500 mW		500 mW	
Output Short-Circuit to GND, (Note 2)	500 mW		500 mW	
Input Current (V <sub>IN</sub> < -0.3 VDC), (Note 3)	50 mA		50 mA	
Operating Temperature Range	0°C to +70°C		-40°C to +85°C	
LM139A	-25°C to +85°C			
LM2901	-65°C to +125°C			
LM139A	-65°C to +125°C		-65°C to +125°C	
Storage Temperature Range	-65°C to +150°C		-65°C to +150°C	
Lead Temperature (Soldering, 10 seconds)	300°C		300°C	

electrical characteristics (V<sup>+</sup> = 5 VDC, Note 4)

PARAMETER	CONDITIONS	LM139A		LM239A LM339A		LM139		LM239 LM339		LM2901		LM3302		UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T <sub>A</sub> = 25°C, (Note 5)	0.10	0.20	0.10	0.20	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	mVDC
Input Bias Current	I <sub>IN(1)</sub> or I <sub>IN(2)</sub> with Output in Linear Range, T <sub>A</sub> = 25°C, (Note 5)	20	100	20	100	20	100	20	100	20	100	20	100	nADC
Input Offset Current	I <sub>IN(1)</sub> - I <sub>IN(2)</sub> , T <sub>A</sub> = 25°C	0.20	1.0	0.20	1.0	0.20	1.0	0.20	1.0	0.20	1.0	0.20	1.0	nADC
Input Common-Mode Voltage Range	T <sub>A</sub> = 25°C, (Note 5)	0	V <sup>+</sup> - 1.5	0	V <sup>+</sup> - 1.5	0	V <sup>+</sup> - 1.5	0	V <sup>+</sup> - 1.5	0	V <sup>+</sup> - 1.5	0	V <sup>+</sup> - 1.5	VDC
Supply Current	R <sub>L</sub> = ∞ or an AC Load, T <sub>A</sub> = 25°C	0.0	2.0	0.0	2.0	0.0	2.0	0.0	2.0	0.0	2.0	0.0	2.0	mADC
	R <sub>L</sub> = ∞ or V <sup>+</sup> - 30V, T <sub>A</sub> = 25°C													mADC
	R <sub>L</sub> ≥ 10kΩ, V <sub>OUT</sub> = 10 VDC, I <sub>IN</sub> = 0	50	200	50	200	200	200	200	200	200	200	200	200	μA/V
Large Signal Slew Rate	V <sub>IN</sub> = TTL Logic Levels, V <sub>OUT</sub> = 10 VDC, V <sub>L</sub> = 5 VDC, R <sub>L</sub> = 5 kΩ, T <sub>A</sub> = 25°C	200	200	200	200	200	200	200	200	200	200	200	200	V/μs
Response Time	V <sub>IN</sub> = 5 VDC, R <sub>L</sub> = 5 kΩ, T <sub>A</sub> = 25°C, (Note 7)	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	ns
Output Short Current	V <sub>IN(1)</sub> = 2.1 VDC, V <sub>IN(2)</sub> = 0, V <sub>O</sub> ≤ 1.0 VDC, T <sub>A</sub> = 25°C	0.0	10	0.0	10	0.0	10	0.0	10	0.0	10	0.0	10	mADC
Breakdown Voltage	V <sub>IN(1)</sub> = 2.1 VDC, V <sub>IN(2)</sub> = 0, I <sub>IN(1)</sub> = 5 mA, T <sub>A</sub> = 25°C	700	400	700	400	700	400	700	400	700	400	700	400	mVDC
Output Voltage Swing	V <sub>IN(1)</sub> = 2.1 VDC, V <sub>IN(2)</sub> = 0, I <sub>IN(1)</sub> = 5 mA, T <sub>A</sub> = 25°C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	mADC

electrical characteristics (con't)

PARAMETER	CONDITIONS	LM139A		LM239A LM339A		LM139		LM239 LM339		LM2901		LM3302		UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	mVDC
Input Offset Current	I <sub>IN(1)</sub> - I <sub>IN(2)</sub>	100	100	100	100	100	100	100	100	100	100	100	100	nADC
Input Bias Current	I <sub>IN(1)</sub> or I <sub>IN(2)</sub> with Output in Linear Range	200	400	200	400	200	400	200	400	200	400	200	400	nADC
Input Common-Mode Voltage Range		0	V <sup>+</sup> - 2.0	0	V <sup>+</sup> - 2.0	0	V <sup>+</sup> - 2.0	0	V <sup>+</sup> - 2.0	0	V <sup>+</sup> - 2.0	0	V <sup>+</sup> - 2.0	VDC
Breakdown Voltage	V <sub>IN(1)</sub> = 2.1 VDC, V <sub>IN(2)</sub> = 0, I <sub>IN(1)</sub> = 5 mA, T <sub>A</sub> = 25°C	700	700	700	700	700	700	700	700	700	700	700	700	mVDC
Output Leakage Current	V <sub>IN(1)</sub> = 2.1 VDC, V <sub>IN(2)</sub> = 0, V <sub>O</sub> = 30 VDC	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	nADC
Differential Input Voltage	Keep at V <sub>IN</sub> ≤ 2.0 VDC for V <sup>+</sup> = 5 VDC (Note 5)	V <sup>+</sup>	V <sup>+</sup>	V <sup>+</sup>	V <sup>+</sup>	30	30	30	30	V <sup>+</sup>	V <sup>+</sup>	V <sup>+</sup>	V <sup>+</sup>	VDC

Note 1: For operation at high temperatures, the LM139/LM139A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device mounted in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON/OFF" characteristics of the outputs make the chip dissipation very small (P<sub>D</sub> < 100 mW) provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V<sup>+</sup> can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V<sup>+</sup>.

Note 3: The input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward-biased and thereby acting as input diode clamps. In addition to the diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V<sup>+</sup> voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output stages will re-establish when the input voltage, which was negative, again returns to a voltage greater than -0.3 VDC.

Note 4: These specifications apply for V<sup>+</sup> = 5 VDC and -85°C < T<sub>A</sub> < +25°C, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to -25°C ≤ T<sub>A</sub> ≤ +85°C, the LM139/LM139A temperature specifications are limited to 0°C ≤ T<sub>A</sub> ≤ +70°C, and the LM2901, LM3302 temperature range is -40°C ≤ T<sub>A</sub> ≤ +85°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. The current is essentially constant, independent of the state of the output to no loading change seen on the reference or input lines.

Note 6: The input common-mode voltage or other input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V<sup>+</sup> - 1.5V, but either or both inputs can go to +30 VDC without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overshoot. For larger overshoot signals, 300 ns can be obtained. See typical performance characteristics section.

Note 8: Excessive overshoots of input voltage may exceed the power supply level. As long as the other voltage returns within the common-mode range, the comparator will provide a proper output state. The low input voltage level must not be less than -0.3 VDC (or 0.3 VDC below the magnitude of the negative power supply, if used).

Note 9: At output switch point, V<sub>O</sub> = 1.4 VDC, R<sub>g</sub> = 0Ω with V<sup>+</sup> from 5 VDC, and over the full input common-mode range 10 VDC to V<sup>+</sup> - 1.5 VDC.

Note 10: For input signals that exceed V<sub>CC</sub> only the differential comparator is affected. With a 5V supply, V<sub>IN</sub> should be limited to 20V max, and a limiting resistor should be used on all inputs that might exceed the absolute supply.



LM139/LM239/LM339,  
LM139A/LM239A/LM339A, LM2901, LM3302

**FEATURES**

**3-Terminal Device:**

**Voltage In/Voltage Out**

$V_{out} = 2.5V \pm 1\%$ ;  $4.5V < V_{in} < 30V$

**Excellent Temperature Stability:**

10ppm/ $^{\circ}C$  (AD580M)

10ppm/ $^{\circ}C$  (AD580U)

**Excellent Long Term Stability: 250 $\mu$ V**

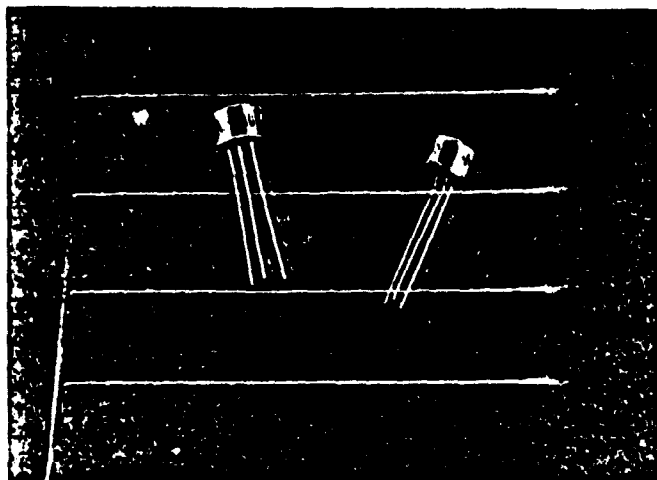
(25 $\mu$ V/month)

**Low Quiescent Current: 1.0mA max**

**Small IC Package: TO-52 Can**

**10mA Current Output Capability**

**Low Cost: \$2.00 (100's, AD580J)**



**PRODUCT DESCRIPTION**

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output voltage for inputs between 4.5V and 30V. A unique combination of advanced circuit design and sophisticated thin film resistor processing capability provides the AD580 with a temperature stability of better than 10ppm/ $^{\circ}C$  and long term stability of better than 250 $\mu$ V. In addition, the low quiescent current drain of 1.0mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8, 10, and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580, allowing operation with 5 volt logic supplies, makes the AD580 a good choice for all digital panel meter applications.

The AD580J, K, L and M are specified for operation over the 0 to +70 $^{\circ}C$  temperature range; the AD580S, T and U are specified for operation over the extended temperature range of -55 to +125 $^{\circ}C$ .

**PRODUCT HIGHLIGHTS**

1. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.

2. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for panel meter applications.
3. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities below 10ppm/ $^{\circ}C$  and long term stability better than 250 $\mu$ V.
4. The low quiescent current drain and fast turn-on time of the AD580 make it ideal for CMOS and other low power system applications.
5. Every AD580 is baked for 48 hours at +200 $^{\circ}C$ , temperature cycled 10 times from -65 to +150 $^{\circ}C$ , and receives a high impact shock test.

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Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062  
 Tel: 617/329-4700 TWX: 710/394-6577  
 West Coast Mid-West Texas  
 213/595-1733 312/394-3300 214/231-5094

# SPECIFICATIONS

(typical @  $E_{in} = +15V$  and  $25^{\circ}C$  unless otherwise specified)

MODEL	ADS80J	ADS80K	ADS80L	ADS80M	ADS80S	ADS80T	ADS80U
<b>ABSOLUTE MAX RATINGS</b>							
Input Voltage	40V $E_{in}$						
Power Dissipation @ $+25^{\circ}C$	350mW						
Ambient Temperature	2.8mW/ $^{\circ}C$						
Derate Above $+25^{\circ}C$	-55 to $+150^{\circ}C$						
Operating Junction Temp Range	-65 to $+175^{\circ}C$						
Storage Temperature Range	$+300^{\circ}C$						
Lead Temperature (soldering, 10 sec)	100 $^{\circ}C/W$						
Thermal Resistance	360 $^{\circ}C/W$						
Junction to Case	0 to $+70^{\circ}C$						
Junction to Ambient							
Operating Temperature Range	2.425V min (2.575V max)	2.450V min (2.550V max)	2.475 min (2.525 max)	2.475 min (2.525 max)	2.425V min (2.575V max)	-55 to $+125^{\circ}C$	-55 to $+125^{\circ}C$
<b>OUTPUT VOLTAGE</b>	2.425V min (2.575V max)	2.450V min (2.550V max)	2.475 min (2.525 max)	2.475 min (2.525 max)	2.425V min (2.575V max)	2.475 min (2.525 max)	2.475 min (2.525 max)
<b>OUTPUT TURN-ON SETTLING TIME*</b>	6.0 $\mu$ sec to 0.04*						
<b>OUTPUT VOLTAGE CHANGE†</b>							
1 min to $t_{max}$	15mV max (85ppm/ $^{\circ}C$ )	7mV max (40ppm/ $^{\circ}C$ )	4.3mV max (25ppm/ $^{\circ}C$ )	1.75mV max (10ppm/ $^{\circ}C$ )	25mV max (55ppm/ $^{\circ}C$ )	11mV max (25ppm/ $^{\circ}C$ )	4.5mV max (10ppm/ $^{\circ}C$ )
<b>LINE REGULATION</b>							
7V $\leq V_{in} \leq 30V$	6mV max (0.6mV typ)	4mV max (0.6mV typ)	2mV max	2mV max	6mV max (0.6mV typ)	2mV max	2mV max
4.5V $\leq V_{in} \leq 7V$	3mV max (0.3mV typ)	2mV max (0.3mV typ)	1mV max	1mV max	3mV max (0.3mV typ)	1mV max	1mV max
<b>LOAD REGULATION</b>							
$\Delta I = 10mA$	10mV max						
<b>QUIESCENT CURRENT</b>							
NOISE (0.1 to 10Hz)	1.5mA max (1.0mA typ)						
STABILITY	60 $\mu$ V (p-p)						
Long Term	250 $\mu$ V						
Per Month	25 $\mu$ V						
<b>PRICE</b>							
(1-24)	\$3.00	\$6.00	\$8.25	\$12.50	\$11.25	\$18.00	\$37.50
(25-99)	\$2.40	\$4.80	\$6.90	\$10.00	\$9.00	\$14.50	\$30.00
(100-999)	\$2.00	\$4.00	\$5.75	\$8.75	\$7.50	\$12.00	\$25.00

NOTE 1: Self-heating time constant will depend on heat sinking, raw supply voltage and load conditions.

\*Specification same as ADS80J

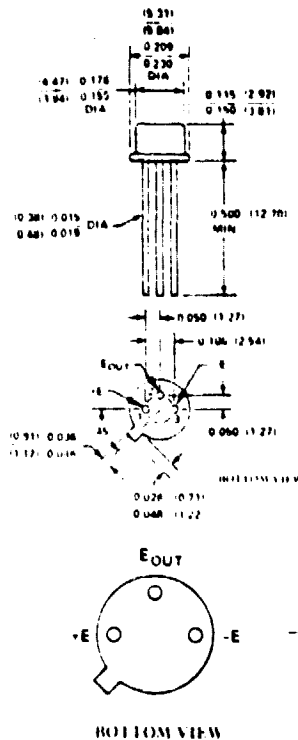
\*\*Specification same as ADS80K.

Specifications and prices subject to change without notice.

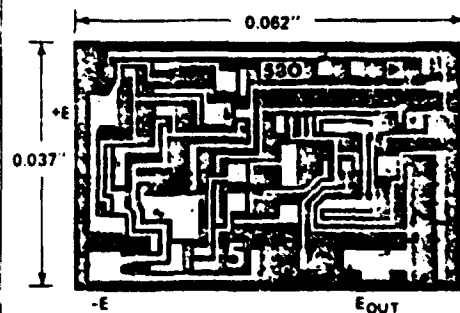
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### CASE 27 TO-52 PACKAGE



### BONDING DIAGRAM



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## Voltage Comparators

**LM139/LM239/LM339, LM139A/LM239A/LM339A, LM2901, LM3302 low power low offset voltage quad comparators**

### general description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters, pulse, squarewave and time delay generators, wide range VCO, MOS clock timers, multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic—where the low power drain of the LM339 is a distinct advantage over standard comparators.

### advantages

- High precision comparators
- Reduced  $V_{OS}$  drift over temperature

- Eliminates need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

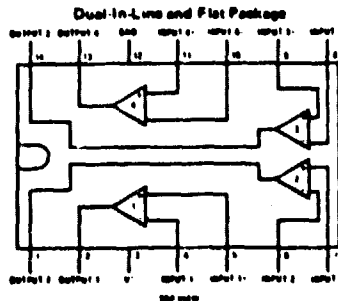
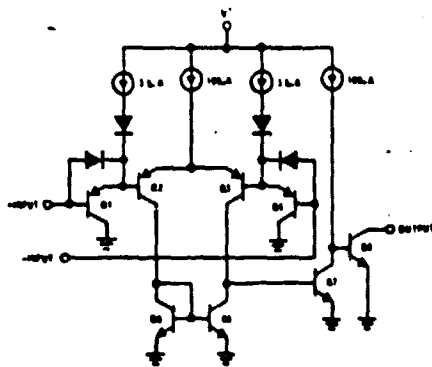
### features

- Wide single supply voltage range or dual supplies
 

LM139 series,	2 VDC to 36 VDC or
LM139A series, LM2901	$\pm 1$ VDC to $\pm 18$ VDC
LM3302	2 VDC to 28 VDC
	or $\pm 1$ VDC to $\pm 14$ VDC
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 VDC)
- Low input biasing current 25 nA
- Low input offset current  $\pm 5$  nA and offset voltage  $\pm 3$  mV
- Input common-mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output 250 mV at 4 mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

LM139/LM239/LM339, LM139A/LM239A/LM339A, LM2901, LM3302

### schematic and connection diagrams



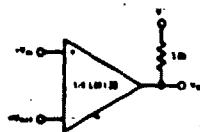
Order Number LM139D, LM139AD, LM239D or LM239AD  
See NS Package D14E

Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J  
See NS Package J14A

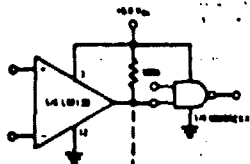
Order Number LM139F, LM139AF, LM239F or LM239AF  
See NS Package F14A

Order Number LM139N, LM339AN, LM2901N or LM3302N  
See NS Package N14A

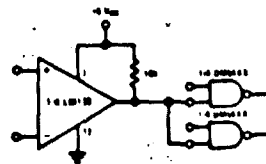
### typical applications ( $V^+ = 5.0$ VDC)



Basic Comparator



Driving CMOS



Driving TTL



LX1600 Series - See Package PX6  
 LX1700 Series - See Package PX7  
 LX1700D Series - See Package PX7D

LX1600A, 1601A, 1602A, 1603A, 1610A, 1620A,  
 LX1700A, 1701A, 1702A, 1703A, 1710A, 1720A, 1730A  
 absolute pressure transducers 10-20 psia to 0-300 psia

LX1601D, 1602D, 1603D, 1604D, 1610D, 1611D, 1612D, 1620D,  
 LX1701D, 1702D, 1703D, 1704D, 1710D, 1711D, 1712D, 1720D  
 differential pressure transducers  $\pm 5$  psid to 0-100 psid

LX1601G, 1602G, 1603G, 1604G, 1610G, 1611G, 1612G, 1620G,  
 LX1701G, 1702G, 1703G, 1704G, 1710G, 1711G, 1712G, 1720G, 1730G  
 gage pressure transducers  $\pm 5$  psig to 0-300 psig

**general description**

These rugged devices are highly accurate, completely field interchangeable, temperature compensated linear pressure transducers.

A fully signal conditioned transducer with a 10 Vdc output is provided in a small ceramic hybrid circuit configuration ready for PC board mounting (LX1600 series) or surrounded by a tough zinc diecast housing with a molded connector. A nylon molded housing is available where metal enclosures are forbidden. All devices include a voltage regulated input and an operational amplifier output. A conformal coating protects all portions of the circuit from most corrosive or conductive fluids.

**features**

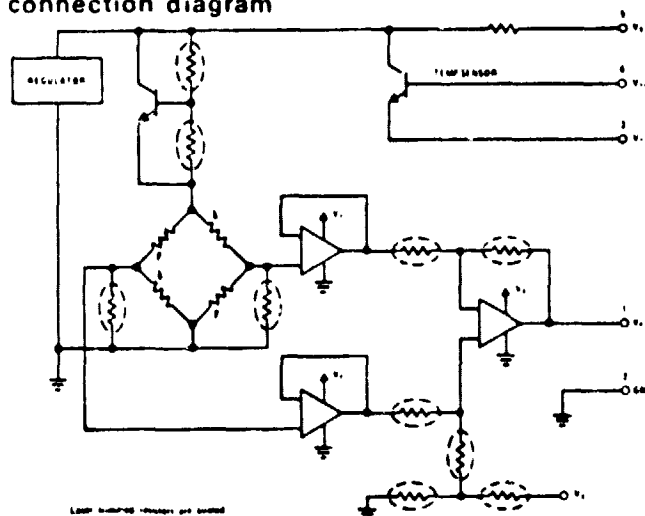
- Field interchangeability within  $\pm 1.5\%$  of span
- $\pm 3\%$  of span overall accuracy

- Temperature coefficients better than  $\pm 0.03\%$  of span/ $^{\circ}\text{C}$  ( $\pm 0.01\%$  of span/ $^{\circ}\text{F}$ )
- Repeatability better than  $\pm 0.5\%$  of span
- Temperature measurement capability at point of pressure sensing
- Available from local National distributors

**applications**

- Food and beverage processing
- Medical electronics
- Computer pneumatics
- Hot bulb thermometry
- Fluid systems proportional control
- Hydraulic and pneumatic controls
- Heating, ventilation, refrigeration and air conditioning controls
- Automotive diagnostic, safety, and control systems

**circuit and connection diagram**



product selection guide Nominal characteristics ( $V_E = 15V$ , $T_A = 21^\circ C$ ) (Notes 1 and 2)					
PRESSURE RANGE	DEVICE TYPE	CALIBRATED OUTPUT VOLTAGE		PROOF PRESSURE	MAX PRESSURES
ABSOLUTE		LOW END	HIGH END	PKG BURST	
0 to 15 psia	LX1600A, LX1700A	2.5 $\pm$ 0.15V	7.5 $\pm$ 0.15V	40 psia	300 psia
10 to 20 psia	LX1601A, LX1701A	2.5 $\pm$ 0.2V	12.5 $\pm$ 0.2V	40 psia	300 psia
0 to 15 psia	LX1602A, LX1702A	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	40 psia	300 psia
0 to 30 psia	LX1603A, LX1703A	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	60 psia	300 psia
0 to 60 psia	LX1610A, LX1710A	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	90 psia	300 psia
0 to 100 psia	LX1620A, LX1720A	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	150 psia	300 psia
0 to 300 psia	LX1730A	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	450 psia	500 psia (Note 3)
DIFFERENTIAL (Note 4)		COMMON MODE			
-5.0 to +5.0 psid	LX1601D, LX1701D	2.5 $\pm$ 0.2V	12.5 $\pm$ 0.2V	40 psid	300 psia
-5.0 to +5.0 psid	LX1611D, LX1711D	2.5 $\pm$ 0.2V	12.5 $\pm$ 0.2V	100 psid	300 psia
-10.0 to +10.0 psid	LX1612D, LX1712D	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	125 psid	300 psia
0 to 15 psid	LX1602D, LX1702D	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	40 psid	300 psia
0 to 30 psid	LX1603D, LX1703D	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	60 psid	300 psia
-15 to +15 psid	LX1604D, LX1704D	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	40 psid	300 psia
0 to 60 psid	LX1610D, LX1710D	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	90 psid	300 psia
0 to 100 psid	LX1620D, LX1720D	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	150 psid	300 psia
GAGE		SEAL			
-5.0 to +5.0 psig	LX1601G, LX1701G	2.5 $\pm$ 0.2V	12.5 $\pm$ 0.2V	40 psig	50 psig
-5.0 to +5.0 psig	LX1611G, LX1711G	2.5 $\pm$ 0.2V	12.5 $\pm$ 0.2V	100 psig	115 psig
-10.0 to +10.0 psig	LX1612G, LX1712G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	125 psig	145 psig
0 to 15 psig	LX1602G, LX1702G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	40 psig	50 psig
0 to 30 psig	LX1603G, LX1703G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	60 psig	70 psig
-15 to +15 psig	LX1604G, LX1704G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	40 psig	50 psig
0 to 60 psig	LX1610G, LX1710G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	90 psig	100 psig
0 to 100 psig	LX1620G, LX1720G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	150 psig	175 psig
0 to 300 psig	LX1730G	2.5 $\pm$ 0.15V	12.5 $\pm$ 0.15V	450 psig	500 psig

**absolute maximum ratings (Note 6)**

Excitation Voltage                    30 V<sub>DC</sub> (Note 2)  
 Output Current, I<sub>o</sub>                    20 mA  
 Operating Temperature Range       -40°C to +125°C  
 Lead Temperature (Soldering, 10 seconds)    300°C

**electrical specifications**

PARAMETER	CONDITIONS	LX16 & 1700 01, 02A LX16 & 1701 02, 11D LX16 & 1701 02, 11G		LX16 & 1703 10A LX16 & 1703 04, 10, 12D LX16 & 1703, 04, 10, 12G		LX16 & 1720, 1730A LX16 & 1720D LX16 & 1720, 1730G		UNITS
		TYP	MAX	TYP	MAX	TYP	MAX	
		Temperature Coefficient Centigrade Fahrenheit	25°C to +75°C V <sub>E</sub> = 15V (Note 2)	+0.04 +0.033	+0.09 +0.050	+0.03 +0.017	+0.06 +0.025	
Temperature Coefficient Centigrade Fahrenheit	40°C to +75°C and +75°C to +125°C V <sub>E</sub> = 15V (Note 2)	+0.04 +0.033	+0.18 +0.039	+0.03 +0.017	+0.12 +0.067	+0.02 +0.011	+0.06 +0.033	% span/°C % span/°F
Linearity and Hysteresis	Best Straight Line	+0.2	+0.5	+0.2	+0.5	+0.2	+0.5	% span
Repeatability	(Note 2)	+1.0	+2.0	+0.75	+1.50	+0.50	+0.75	% span
Output Voltage Sensitivity (ΔV <sub>o</sub> /ΔV <sub>E</sub> )	14.5V < V <sub>E</sub> < 25	+0.3	0.5	+0.3	+0.5	+0.3	+0.5	%
Transducer Bias Current	(Note 2)	15	20	15	20	15	20	mA

Note 1: 70 F = 21 C, 170 F = 78 C, 240 F = 116 C, 512 F = 300 C, 1 mV/°F = 1.8 mV/°C, 1 psi = 51.71 TORR, 1 mmHg = 2.036 in. Hg = 27.67 in. H<sub>2</sub>O = 2.307 ft. H<sub>2</sub>O = 68.95 mmHg

Note 2: All devices in the LX16 and 1700 Series except the LX16 and 1700A are regulated and scaled for excitation 14.5 V < V<sub>E</sub> < 25V. The LX16 and 1700A are regulated and scaled for excitation 2V < V<sub>E</sub> < 25V, so as to be ideal for battery operation. Upon special request, the endpoint scaling and regulation of any LX16 and 1700 Series device can be set for battery operation.

Note 3: Package burst pressures are shown for the LX1600 Series except for the LX1630A, which cannot be purchased as a standard product without the Zinc or Nylon outer package.

Note 4: The LX1700D Series outer package is available in Nylon only.

Note 5: The transducers are coated to protect against most corrosive or conductive fluids. Additional isolation is recommended for *in vivo* medical applications.

Note 6: (1) On special request the end points can be set anywhere between a minimum of one volt and a maximum of 1V<sub>E</sub> - 2.01 volts. Similarly the sensitivity can be set up to a max of 5V/psi.

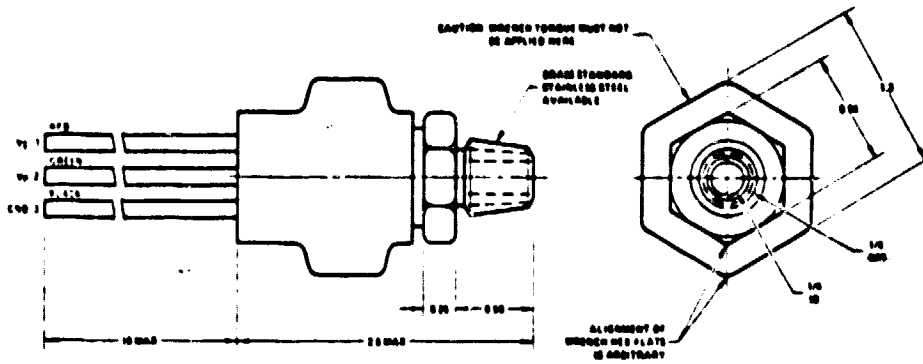
Note 7: This is defined as the output voltage reproducibility over the pressure range from -25°C to +75°C.

Note 8: Caution - Improper constraint of transducer package will be exhibited as parasitic errors in the output voltage.

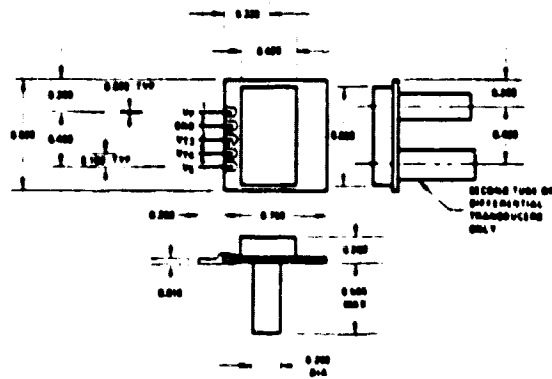




Package Outlines



PX4  
1/4" NPT Pressure Transducer Package



PX6  
0.2" Port, Hybrid Pressure Transducer Package



## LX5600/LX5600A, LX5700/LX5700A temperature transducers

### general description

The LX5600/LX5700 series temperature transducers are highly accurate temperature measurement or control systems for use over a  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range. Fabricated on a single monolithic chip they include a temperature sensor, stable voltage reference and operational amplifier.

The output of the LX5600/LX5700 is directly proportional to temperature in degrees Kelvin at  $10\text{ mV}/^{\circ}\text{K}$ . Using the internal op amp with external resistors any temperature scale factor is easily obtained. By connecting the op amp as a comparator, the output will switch as the temperature transverse the set point making the device useful as an on/off temperature controller.

An active shunt regulator is connected across the power leads to the LX5600/LX5700 to provide a stable voltage reference. In addition to providing a reference, it regulates the operating voltage to  $6\text{ BV}$ . This allows the use of any power supply voltage with suitable external resistors.

The op amp can amplify the  $10\text{ mV}/^{\circ}\text{K}$  from the sensor to almost any desired output. The input bias current is low and relatively constant with temperature, ensuring high accuracy when high source impedance is used. Further, the output collector can be returned to a voltage higher than  $6\text{ BV}$  allowing the LX5600/LX5700 to drive lamps and relays from a  $28\text{ V}$  supply.

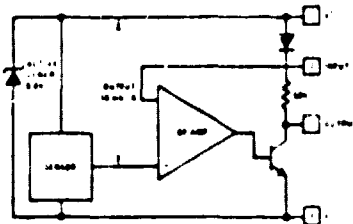
The LX5600 uses the difference in emitter base voltage of transistors operating at different current densities as the basic temperature sensitive element. Since this output depends only on transistor matching the same reliability and stability as present op amps can be expected.

The LX5600 and LX5600A operate over a  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range and are available in 4 lead TO 5 package. The LX5700 and LX5700A also operate over the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range and are available in the 4 lead TO 46 package.

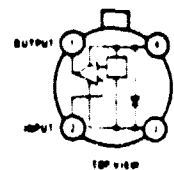
### features

- Calibration accuracy of  $\pm 4^{\circ}\text{C}$  over  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Internal op amp with frequency compensation
- Linear output of  $10\text{ mV}/^{\circ}\text{K}$  ( $110\text{ mV}/^{\circ}\text{C}$ )
- Directly calibrated in degrees Kelvin
- Output can drive loads up to  $35\text{ V}$
- Internal stable voltage reference
- Four lead device—minimizing wiring

### block and connection diagrams

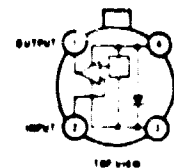


TO 5 Metal Can Package



NOTE: PINS CONNECTED TO CASE  
Order Number LX5600AH or LX5600H

TO 46 Metal Can Package



NOTE: PINS CONNECTED TO CASE  
Order Number LX5700AH or LX5700H

**absolute maximum ratings**

Supply Voltage	Internally Regulated	Output Short Circuit Duration	Indefinite
Supply Current (Externally Set)	10 mA	Operating Temperature Range	-55°C to +125°C
Output Collector Voltage	36V	Storage Temperature Range	-65°C to +150°C
Input Voltage Range	0V to +7.0V	Lead Temperature (Soldering, 10 seconds)	300°C

**electrical characteristics (Note 1)**

PARAMETER	CONDITIONS	LX5600A/LX5700A			LX5600/LX5700			UNITS
		TYP VOLTS	ERROR ±mV	ERROR ±% OF SPAN	TYP VOLTS	ERROR ±mV	ERROR ±% OF SPAN	
Output Voltage (Note 2)	T <sub>A</sub> = +25°C	2.98	40	2.22	2.98	80	4.44	
Output Voltage (Note 2)	T <sub>A</sub> = -55°C	2.18	40	2.22	2.18	80	4.44	
Output Voltage (Note 2)	T <sub>A</sub> = 125°C	3.98	40	2.22	3.98	80	4.44	
Linearity	ΔT ≤ +180°C	0.018			0.018			
Long Term Stability	T <sub>A</sub> = 125°C	±0.002			±0.002			
Repeatability	T <sub>A</sub> = 125°C	±0.002			±0.002			
<b>VOLTAGE REFERENCE</b>		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	1 mA ≤ I <sub>z</sub> ≤ 5 mA	6.88	6.85	7.12	6.55	6.85	7.25	V
Reverse Breakdown Voltage Change With Current	1 mA ≤ I <sub>z</sub> ≤ 5 mA		10	25		10	35	mV
Temperature Stability			20	60		20	85	mV
Dynamic Impedance	I <sub>z</sub> = 1 mA		30			30		Ω
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz		30			30		μV
Long Term Stability	T <sub>A</sub> = +125°C		60			60		mV
<b>OP AMP</b>								
Input Bias Current	T <sub>A</sub> = +25°C		35	75		30	150	nA
Input Bias Current			45	150			250	nA
Voltage Gain	R <sub>L</sub> = 36k, V <sub>cc</sub> = 36V	2000	15000		1500	15000		V/V
Output Leakage Current	T <sub>A</sub> = 25°C (Note 3)		0.2	1.0	2.0	0.2		μA
Output Leakage Current (Note 3)			1.0	5.0	8.0	1.0		μA
Output Source Current	V <sub>OUT</sub> ≤ 4.05	10			10			μA
Output Sink Current	1V ≤ V <sub>OUT</sub> ≤ 36V	2.0			2.0			mA

Note 1: These specifications apply for -55°C ≤ T<sub>A</sub> ≤ +125°C and 0.9 mA ≤ I<sub>SUPPLY</sub> ≤ 1.1 mA unless otherwise specified.  
 Note 2: The output voltage applies to the basic thermometer configuration with the output and feedback terminals shorted and a load resistance of ≥ 10 MΩ. This is the feedback sense voltage and includes errors in both the sensor and op amp. This voltage is specified for the sensor in a rapidly stirred oil bath.  
 Note 3: The output leakage current is specified with ≥ 100 mV overdrive. Since this voltage changes with temperature, the voltage drive for turn-off changes and is defined as V<sub>OUT</sub> (with output and input shorted) - 100 mV. This specification applies for V<sub>OUT</sub> = 36V.

**application hints**

Although the LX5600/LX5700 were designed to be as trouble-free as possible, certain precautions should be taken to insure the best possible performance.

Like any temperature sensor, internal power dissipation will raise the sensor temperature above ambient. Nominal operating current for the shunt regulator is 1.0 mA and causes 7.0 mW of power dissipation. In free, still, air this raises the package temperature by about 1.2°K. Although the regulator will operate at higher reverse currents and the output will drive loads up to 5.0 mA, these higher currents can raise the sensor temperature over 19°K above ambient—degrading accuracy. Therefore, the sensor should be operated at the lowest possible power level.

With moving air, liquid or surface temperature sensing, self heating is not as great a problem since the measured

media will conduct the heat from the sensor. Also, there are many small heat sinks designed for transistors which will improve heat transfer to the sensor from the surrounding medium. A small finned clip-on heat sink is quite effective in free air. It should be mentioned that the LX5600 drifts on the base of the package and therefore conduction to the base is preferable.

The internal reference provides a temperature stable voltage for initiating the temperature output or setting a comparison point in temperature controllers. However, since this reference is at the same temperature as the sensor temperature changes will also cause reference drift. For application where maximum accuracy is needed an external reference should be used. Of course, for fixed temperature controllers the internal reference is adequate.



## 12 BIT MN5210 SERIES ADJUSTMENT-FREE A/D CONVERTERS

### DESCRIPTION

The MN5210 Series Devices are extremely fast 12 Bit Successive Approximation A/D Converters providing both parallel and serial output. These devices have a maximum conversion time of 13  $\mu$ Sec which allows full accuracy with a 1 MHz clock.

These hybrid converters are housed in miniature 24 pin glass/ceramic dual-in-line packages. Miniature size, low power consumption and adjustment free operation contribute to the reasons why these converters provide the user with the best possible selection for compact and efficient systems.

All converters are completely laser trimmed and totally adjustment free. They require only one external component, a non-critical 2.2 $\mu$ f capacitor. Additionally, due to highly stable thin film resistor networks, these converters provide long term maintenance free operation.

These converters are available in three input voltage ranges: 0 to -10 volts (MN5210/13),  $\pm 5$  volts (MN5211/14), and  $\pm 10$  volts (MN5212/15). For each of these input ranges, the user has the option of specifying a model complete with an internal reference or for improved absolute accuracy, a model which uses an external reference.

In all cases  $\pm 1/2$  LSB linearity is guaranteed over the entire operating temperature range. Additionally all units are tested 100% for linearity and accuracy at their temperature extremes as well as at room temperature.

All models of the MN5210 Series may be procured for operation over the entire -55 $^{\circ}$ C to +125 $^{\circ}$ C military temperature range ("H" models) with the same end temperature operating characteristics as the commercial 0 $^{\circ}$ C to 70 $^{\circ}$ C range. In addition, full military temperature operation devices are available processed to the Class B requirements of MIL-STD-883 (inquire about Micro Networks' "Option B").

### FEATURES

- Very High Speed  
1.0  $\mu$ Sec/Bit max.
- Totally adjustment-free  
No full scale or zero adjustment necessary
- Low Power  
700mW
- Small  
24 Pin DIP
- $\pm 1/2$  LSB linearity worst case
- Hermetically sealed package
- Parallel and serial outputs
- Full Mil operation  
-55 $^{\circ}$ C to +125 $^{\circ}$ C ("H" models)  
Available fully screened & processed to the Class B requirements of MIL-STD-883

### APPLICATIONS

- Remote Equipment
- Medical Instrumentation
- Aerospace
- Computer I/O Equipment



**Micro Networks Corporation**

324 Clark Street • Worcester, Massachusetts 01606

Tel: (617) 852-5400 • TWX 710-340-0067

## MN5210 SERIES SUCCESSIVE APPROXIMATION 12 Bit A/D Converters

### ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0 to 70°C (-55°C to +125°C "H" Models)
Storage Temperature	-65°C to +150°C
Positive Supply	+18 Volts
Negative Supply	-18 Volts
Logic Supply	+7 Volts
Analog Input	±25 Volts
Digital Outputs	Logic Supply
Digital Inputs	+5.5 Volts
Reference Supply (Models MN5213, 14, 15 and 16)	-15 Volts

### SPECIFICATIONS (T<sub>A</sub>=25°C, Voltages ±15, +5 unless otherwise stated)

PERFORMANCE:	INPUT RANGE	INPUT IMPEDANCE	HIGH PERFORMANCE		HIGH ACCURACY (Ext. Ref= -10.000V)		UNITS
			MN5210 MN5211 * MN5212 MN5216	TYP. MAX.	MN5213 MN5214 MN5215	TYP. MAX.	
	0 to -10V	6.7k					Bits
	+5V to -5V	6.7k					LSB
	+10V to -10V	13k					LSB
	0 to +10V	6.7k					LSB
Resolution				12		12	Bits
Linearity (0° to 70°C) (Note 1)				±½		±½	LSB
Zero Error				1		1	LSB
Zero Error (0° to 70°C) (Note 1)				2		2	LSB
Absolute Accuracy 25°C (Note 2)				2		2	LSB
Absolute Accuracy (0° to 70°C) (Notes 1 & 2)				±.4		±.1	%
Conversion Time (Note 5)				13		13	µSec
Power Supply Requirements							
Current Drain +15 Volt Supply			23	28	23	28	mA
Current Drain -15 Volt Supply			15	19	5	6.3	mA
Current Drain + 5 Volt Supply			25	42	25	42	mA
Current Drain -10 Volt Reference					1.5	2.0	mA
Power Supply Rejection							
+15 Volts (Note 3)			±.02		±.02		%F.S.R./%Supply
-15 Volts (Note 3)			±.05		±.02		%F.S.R./%Supply
Power Consumption			695	915	567	744	mW

LOGIC RATINGS	MIN.	TYP.	MAX.	UNITS
Input Logic Commands				
Logic "0"			.8	Volts
Logic "1"	2.0			Volts
Loading		.5		TTL Load
Clock Input Pulse Width	100			nSec
Output Logic				
Logic "0"			.4	Volts
Logic "1"	2.4	3.6		Volts
Serial Output				NRZ
Parallel Output (See Timing Diagram)				
Fanout-High	8			TTL Load
Fanout-Low	2			TTL Load

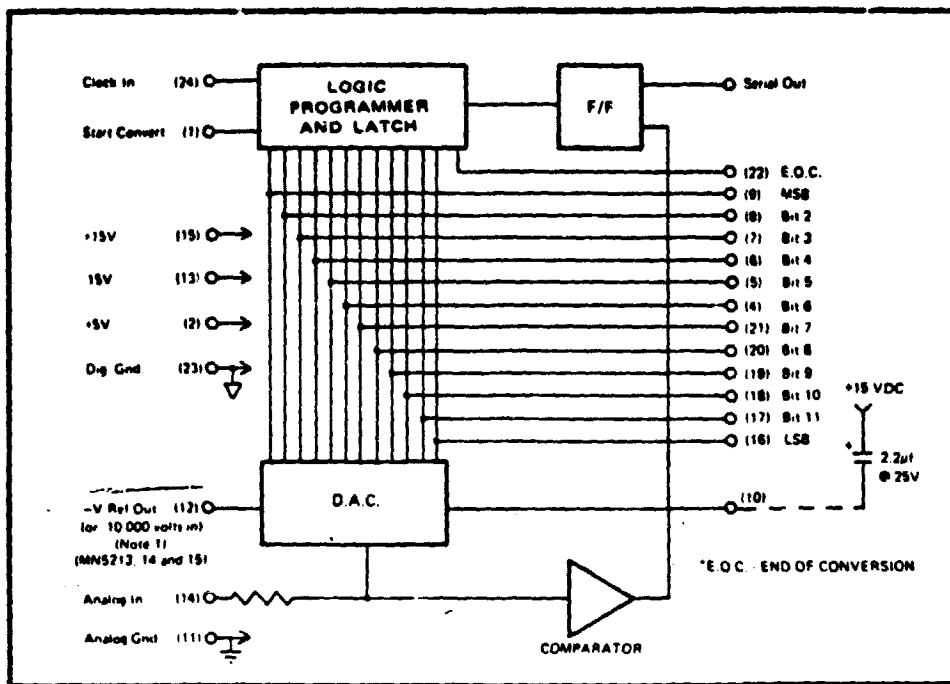
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### LOGIC CODING

MN5210/5213	MN5211/5214	MN5212/5215	MN5216	MSB	LSB
OV	+5.0000	+10.000	+9.9976	0 0 0 0 0 0 0 0 0 0 0 0	0
-5.000V	0	0	+4.9976	1 0 0 0 0 0 0 0 0 0 0 0	0
-9.9976V	-4.9976	-9.995	0	1 1 1 1 1 1 1 1 1 1 1 1	1

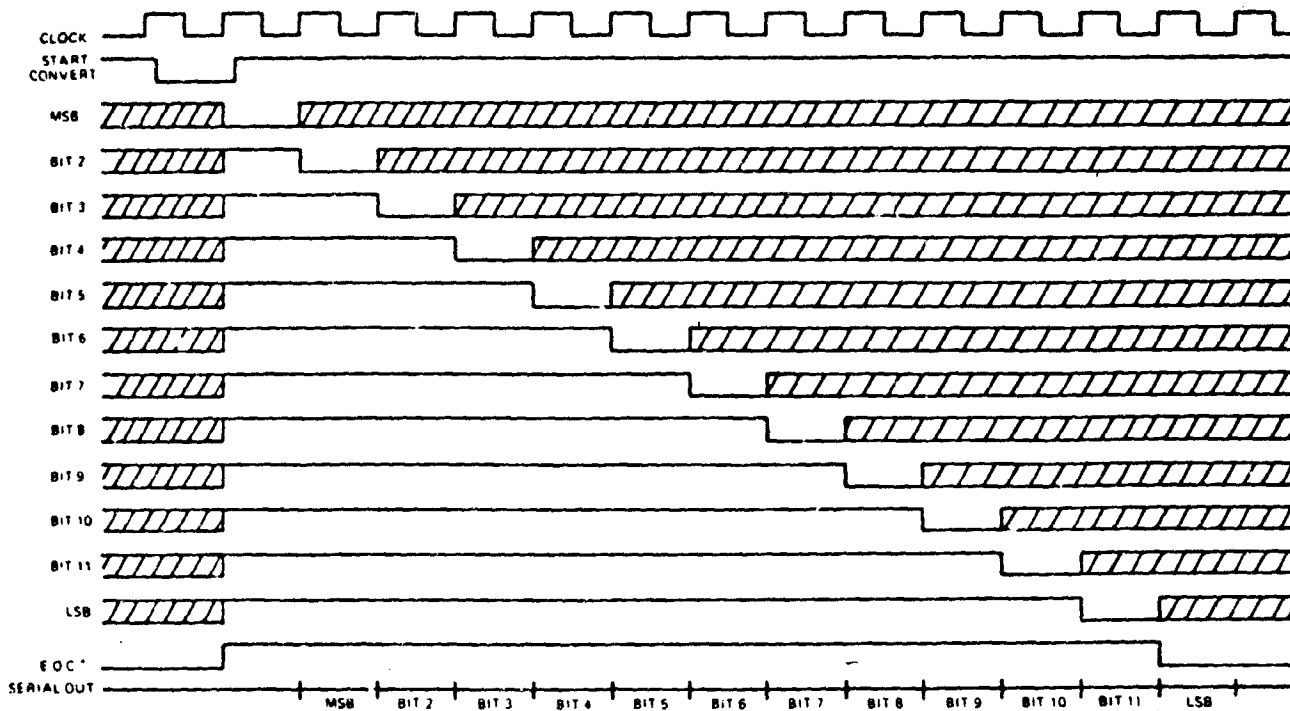
- NOTE 1. For "H" models, the specification applies for operation over the temperature range of -55°C to +125°C.
- NOTE 2. Absolute accuracy includes all errors, gain, zero, and linearity. All converters are tested 100% at the temperature extremes for linearity and absolute accuracy.
- NOTE 3. For proper operation ±15 Volt power supplies tolerance should not be greater than ±3%.
- NOTE 4. FSR is the abbreviation for "Full Scale Range" and is equal to the peak to peak output voltage, i.e. 10 volts for ±5V range.
- NOTE 5. Conversion time is specified with external 2.2µf capacitor (see block diagram). Without this capacitor conversion time is typically 20µ Sec.

## BLOCK DIAGRAM



NOTE 1. The maximum current which should be drawn from the -V Ref output (Available only on internal reference models) is 100  $\mu$ A.

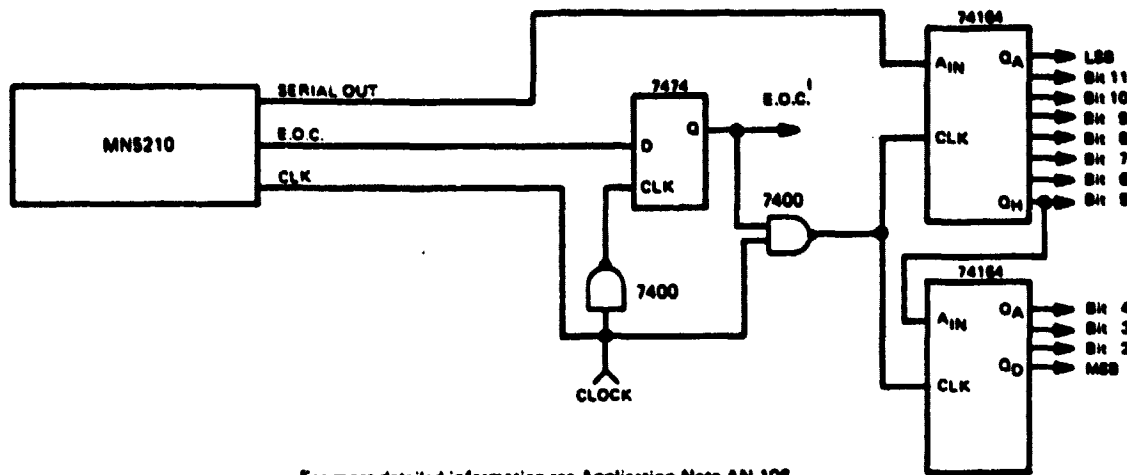
## TIMING DIAGRAM



### NOTES:

1. Shaded areas shown for parallel data outputs denotes states determined by data input immediate prior to shaded area.
2. For continuous operation connect start convert (Pin 1) to end of conversion (Pin 22).
3. Reset the converter by holding the start 'low' during a low to high transition of the clock. The start must be low for a minimum of 25 nSec prior to the clock transition. After the start is again set high the conversion will begin on the next low to high transition of the clock. The start may be set low at any time during a conversion to reset and begin again.
4. At the end of conversion the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
5. The serial output is non-return to zero.
6. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.
7. Micro Networks reserves the right to make design, specification, and process changes and improvements.

## APPLICATION SERIAL TO PARALLEL CONVERSION



For more detailed information see Application Note AN-108.

### PIN DESIGNATIONS

Pin 1 Start	Pin 13 -15V
Pin 2 +5V	Pin 14 Analog in
Pin 3 Serial Out	Pin 15 +15V
Pin 4 Bit 6	Pin 16 LSB
Pin 5 Bit 5	Pin 17 Bit 11
Pin 6 Bit 4	Pin 18 Bit 10
Pin 7 Bit 3	Pin 19 Bit 9
Pin 8 Bit 2	Pin 20 Bit 8
Pin 9 MSB	Pin 21 Bit 7
Pin 10 Ext. Capacitor	Pin 22 E.O.C. (end of conversion)
Pin 11 Analog Ground	Pin 23 DIG Grd
Pin 12 -V ref out (int. ref. models) -V ref in (ext. ref. models)	Pin 24 Clock Input

**MODEL NUMBER** MN521X H/B

Model selection \_\_\_\_\_

Add "H" for -55 to +125°C operation \_\_\_\_\_

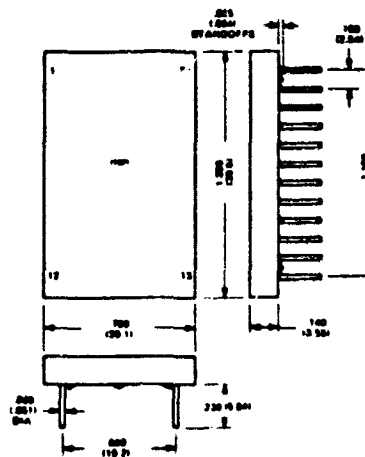
Add "/B" for 100% screened (883 Class B) \*

**Example**

0 to 70°C (±5V, Int. Ref.)	MN5211
-55 to +125°C Operation	MN5211H
-55 to +125°C and 100% screened *883	MN5211H/B

\*Micro Networks Option "B"

#### ORDERING INFORMATION



Outline dimensions in inches (and millimeters).



**Micro Networks Corporation**

324 Clark Street • Worcester, Massachusetts 01606

Tel: (617) 852-5400 • TWX 710-340-0067

FINAL PERFORMANCE DATA  
MODULAR POWER SUPPLIES

PART NO. ASN-MS.5/9V-C5/5V-CA

DATE 10-9-78  
SERIAL NO. A4190

OUTPUT VOLTAGE VS INPUT VOLTAGE AT 74.5 WATTS

INPUT VOLTAGE	E <sub>o</sub> # 1 VDC	E <sub>o</sub> # 2 VDC	E <sub>o</sub> # 3 VDC	E <sub>o</sub> # 4 VDC	E <sub>o</sub> # 5 VDC	E <sub>o</sub> # 6 VDC
24	5.506	5.071				
30	5.509	5.072				
E <sub>o</sub> adj	4.90-5.89	4.58-5.47				

OUTPUT VOLTAGE & RIPPLE VS OUTPUT POWER

OUTPUT POWER	E <sub>IN</sub> = 27 VDC					
100%	5.507	5.072				
50%	5.511	5.077				

RIPPLE ( VRMS )

100%	18 mV	5.1 mV				
50%	18 mV	4.5 mV				

INPUT CURRENT

INPUT VOLTAGE	FULL LOAD	HALF LOAD	NO LOAD
24	5.0	2.5	0.25A
30	4.5	2.4	0.25A

TEST CONDITIONS

1. AMBIENT TEMPERATURE 25° C
2. HEAT SINK: ALUMINUM  
19" X 7" X 1/8" THICK

*Rm*

ARNOLD MAGNETICS CORP.  
11520 W. JEFFERSON BLVD.  
CULVER CITY, CA. 90230  
(213) 870-7014





FINAL PERFORMANCE DATA  
DC INPUT

DATE 10/16/78

MODEL NO. SHU-2/4V

SERIAL NO. A4189

OUTPUT VOLTAGE vs INPUT VOLTAGE AT <u>8</u> WATTS			
INPUT VOLTAGE (VDC)	OUTPUT NUMBER 1	OUTPUT NUMBER 2	OUTPUT NUMBER 2
	<u>2</u> VDC * RED TO-BLACK	_____ VDC * TO-_____	_____ VDC * TO-_____
26	2.000 VDC		
30	1.999 VDC		
OUTPUT VOLTAGE & RIPPLE vs OUTPUT POWER (AT <u>28</u> VDC INPUT)			
OUTPUT POWER (% OF) (RATED)			
100%	2.000 VDC		
50	2.006 VDC		
RIPPLE (mVRMS)			
100%	4.4 mV		
50	3.3 mV		
INPUT CURRENT vs OUTPUT POWER (AT <u>28</u> VDC INPUT)			
100%	.75 Amp.		
50			
N/L	.15 Amp.		

TEST CONDITIONS

1. AMBIENT TEMPERATURE 25°C
2. HEAT SINK: ALUMINUM 19" x 7" x 1/8" THICK

ARNOLD MAGNETICS CORPORATION  
11520 W. JEFFERSON BOULEVARD  
CULVER CITY, CALIFORNIA 90230

