BANDWIDTH COMPRESSION OF COLOR VIDEO SIGNALS

FINAL REPORT

October 1, 1979 - October 31, 1980

NASA - LEWIS RESEARCH CENTER

CLEVELAND, OHIO

NASA Grant: NSG - 5013

Donald L. Schilling

Professor of Electrical Engineering

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COMMUNICATIONS SYSTEMS LABORATORY

DEPARTMENT OF ELECTRICAL ENGINEERING

THE CITY COLLEGE OF THE CITY UNIVERSITY of NEW YORK

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INTRODUCTION

This report summarizes a portion of the research performed under NASA Grant NAG 3-119 from October 1, 1979 - September 30, 1980. The report focusses on different encoder/decoder strategies to digitally encode video using an ADM. The techniques employed : (1) separately encoding the R, G, and B components, (2) separately encoding the I, Y, and Q components, and (3) encoding the picture in a line sequential manner.

The research reported on here forms a portion of the Doctoral Dissertation of Dr. S. Davidovici submitted to the Department of Electrical Engineering in December 1980. Also supported on this Grant were doctoral students: D. Carbonari and J. Barba.

Following a long history of cooperation between NASA, and Dr. Schilling and his students an ADM system operating in each of the three modes has been delievered to NASA/LEWIS for use in their satellite telecommunications system.

DIGITAL ENCODING OF COLOR VIDEO SIGNALS

Introduction

The Color Video Signal

Out of the early days of video development the industry has inherited the NTSC standard. Devised primarily for black and white video transmission it called for a frame update rate of 30 frames/sec. Each frame is made up of two interlaced fields which are displayed at a rate of 1/60th of a second. The video signal has a bandwidth of 4.5 MHz total. Display synchronization is provided by non-displayed portions of the video signal which accomplish vertical (field) and horizontal (line) synchronization. The introduction of color video has called for a signal structure such that full compatibility with the black and white T.V. sets is maintained. This has resulted in a system where the three primary colors R, G and B are transformed into three other signals, I, Y and Q, with Y being the luminance and I and Q the chrominance. Figure 1 shows the spectrum of a typical NTSC video signal.

In terms of the R, G and B signals,

$$Y = 0.3\,R + 0.59\,G + 0.11\,B \tag{1}$$

$$I = 0.6\,R - 0.28\,G - 0.32\,B \tag{2}$$

and

$$Q = 0.21\,R - 0.52\,G + 0.31\,B \tag{3}$$

The I and Q signals are also transmitted and it is the detection of the presence of these I and Q signals in the color monitor, in addition to the Y signal, that enables the decoding of the R, G, and B and the displaying of a color picture.

• The I and Q signals are quadrature amplitude modulated onto a carrier frequency of 3.57 MHz. Thus, the complete color signal is

$$V(t) = Y(t) + I(t) \cos \omega_o t + Q(t) \sin \omega_o t \tag{4}$$

In the color monitor the signal is separated into the luminance and chrominance signals and the R, G and B colors are then extracted using a network which, in essence, solved the matrix

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 0.96 & 1 & 0.62 \\ -0.27 & 1 & -0.65 \\ -1.11 & 1 & 1.7 \end{bmatrix} \cdot \begin{bmatrix} I \\ Y \\ Q \end{bmatrix} \tag{5}$$

The three color signals R, G and B are bandlimited to about 3.3 MHz and the luminance signal has most of its power in this frequency band. However, the inphase signal I is bandlimited to 1 MHz and the quadrature signal Q is limited to 0.5 MHz.

This bandlimiting of the chroma information has the effect of severely distorting the color content of the small picture elements.

However, the psychovisual properties of the eye are such that the color content of small objects is irrelevant and therefore the effect of the distortion is small.

Other approaches to color video encoding have resulted in the development of the PAL and SECAM systems. All three systems are similar in that they all use a luminance and two chrominance channels. While the NTSC provides for the chrominance information to be transmitted via QAM modulation of a color subcarrier, the PAL system alternates the sign of one of the chroma channels every other line while the SECAM system transmits only one of the chroma channels every line. The net result is that in the PAL system the hue value is maintained much better under the effect of equipment misalignment at the expense of the saturation information, while in the SECAM system the vertical resolution of the chroma information is decreased with the color video signal being made simpler by eliminating the QAM of the color subcarrier.

None of the three systems described above have a decisive technical advantage over the other two, and this is one of the reasons why no one standard was universally adopted.

Digital Encoding of Video Signals

Introduction. The desire to encode video signals digitally and then transmit and receive the digital rather than the analog representation of the video information has generated two principal methods of digital encoding. This section will give a brief presentation of the principles underlying the transform and predictive coding methods.

Transform Encoding. Transform encoders perform two distinct operations: 1) The actual transformation and 2) the quantization of the coefficients. A transform encoer is shown in Fig. 2. The transformation from the time domain to the transform domain involves representing the function f(t) by:

$$f(t) = \sum_i A_i \phi_i .$$

where A_i is the i^{th} transform coefficient and the ϕ_i's are the mutually orthagonal basis functions. If the set of functions ϕ_i is properly chosen then only relatively few coefficients A_i will have a substantial magnitude. The quantizer will encode those few coefficients accurately (using enough bits to guarantee a small quantization error) and the rest of the coefficients A_i will be encoded very coarsely (using fewer bits). It is by this unequal importance assigned to the different coefficients A_i that the data reduction is achieved at the expense of negligible picture degradation.

A complete discussion of the various transform encoding techniques, together with a discussion of various fast implementation algorithms and a presentation of their basis functions can be found in reference (23). In general, however, transform encoders are not very widely used in spite of their excellent bit rate reduction capabilities. This is due primarily to enormous computational requirements which are difficult to perform in real time.

<u>Predictive Coding</u>. Predictive encoders are, in general, much simpler to implement and operate than transform encoders. It is for this reason that they are more widely used. The most popular encoders in this category are PCM, DPCM and Delta Modulators. This introduction will give a brief description of each of the above with a slant towards video encoding.

Pulse Code Modulation (PCM). A PCM system is shown in Fig. 3. The input signal $v_i(t)$ is low pass filtered, sampled and quantized. The low pass filter prevents any aliasing errors which may be due to sampling. The quantizer must have a minimum of 64 to 256 levels or 6 to 8 bits per sample. Even though the sampling rate only has to be higher than twice the maximum frequency (or approx. 8 MHz), it is usually set at three times the frequency of the color subcarrier or 10.8 MHz. The PCM bit rate in bits per second is given by:

$$B = M * N * K * F \tag{1}$$

If M = 512 pixels/line

N = 525 lines/frame

K = 6 to 8 bits/pixel

F = 30 frames/second

then the PCM bit rate required to transmit an NTSC video signal is higher than 48 to 64 MBPS.

PCM systems can transmit any conceivable television image because they do not make use of any pixel correlations. This is not of much interest because a human observer will only find meaningful those images where there is a high degree of pixel correlation. Extensive simulations have shown the typical information content of a video image to be on the order of 1 bit/pixel. This indicates that an ideal system would operate well at a bit rate 1/6 to 1/8 of the bit rate required for PCM.

The 6 to 8 pixels form a word. In the transmission process noise is added to the transmitted signal. Because of this it is possible to make an error at the receiver. Even though the errors are random (any bit can be in error), the significance of the error varies from bit to bit. An error in the MSB will be over 100 times greater than an error in the LSB (assuming an 8 bit word). The signal to noise ratio of a PCM system is given by:

$$(S/N)_o = \frac{2^{2K}}{1 + 2^{2(K+1)} P_e} \tag{2}$$

where: K = number of bits/pixel

P_e = probability of error.

Because the human eye does not tolerate this type of error very well, PCM systems are operated in environments where the error rate is 10^{-6} or less. From (2) it is clear that very high S/N ratios can be attained if the P_e is negligible. Because of this high value of the S/N ratio PCM systems are widely used in studio environments.

Delta PCM (DPCM). A DPCM system is shown in Fig. 4. The predictive coder will use the past N samples to generate an estimate of the next pixel by a weighted summation:

$$S_m = \sum_{i=1}^{N} A_i S_{m-1} \tag{3}$$

The estimate is then compared to the incoming pixel and the difference encoded in a number of pits and transmitted. Because now we transmit the difference between the estimate and the pixel rather than the pixel itself, we can use a smaller number of bits per pixel and still obtain good quality video.

The coefficients A_i are chosen in such a manner as to minimize the variance of the error signal. Therefore, the system will perform well only as long as the input signal will maintain the statistics for which the A_i's have been calculated. Because the input signal's statistics can vary widely, some adaptive scheme must be considered if a high quality performance is to be maintained.

DPCM with adaptive predictors. In designing a DPCM system one must either use a predictor with variable parameters such that the parameters would change with the variations in the signal (always generating a stationary differential signal) or one can use a fixed predictor with a variable quantizer to accommodate the resultant nonstationary differential signal.

In a DPCM system with an adaptive linear predictor, the weightings on the adjacent samples used in predicting an incoming sample can change according to variations in the signal value. One way in which these signal variations can be accounted for is to include a delay during which the incoming samples are stored in an input buffer and used to obtain an estimate of the signal covariance matrix. The measured covariance matrix can be used to obtain a set of weightings for the predictor. These values are then used for processing the stored signals. The updated values of the predictor coefficients need to be periodically transmitted to the receiver.

DPCM systems with adaptive quantizers. A DPCM system with a fixed predictor will have a nonstationary differential signal for nonstationary data. Using a fixed quantizer, nonstationary differential signals would cause an abnormal saturation or a frequent utilization of the smallest level in the quantizer. To remedy this situation, the threshold and the reconstruction levels of the quantizer must be made variable to expand and contract according to signal statistics. Adaptation of the quantizer to signal statistics is accomplished using various approaches. One such approach stores k samples of the differential signal to obtain an estimate for the local standard deviation of the signal. Then the stored signal is normalized by the estimated standard deviation and is quantized using a fixed quantizer. Naturally, the scaling coefficient must be transmitted once for every k samples for receiver synchronization. In a similar approach, called Block-Adaptive DPCM, a block of M samples is stored and is normalized by n possible constants. The total distortion for all M samples using each normalizing constant is calculated at the encoder. The normalizing constant giving the smallest distortion is used to scale the samples in the block prior to their quantization and transmission. The system requires $(\log_2 n/M$ binary digits per sample overhead information for receiver synchronization.

Still another approach could utilize a variable set of thresholds and reconstruction levels. This is the self-synchronizing approach used in adaptive delta modulators where the step size increases and decreases depending upon the polarity of sequential output levels. In a DPCM quantizer, the set of threshold and reconstruction levels would contract and expand depending upon the sequential utilization of inner or outer levels of the quantizer. For instance, a variable quantizer can be designed where all reconstruction levels expand by a factor of P (for some optimum value of P) upon two sequential happenings of the outermost level and would contract by a factor of 1/P upon two sequential happenings of the smallest level. This system would have the advantage of being completely adaptive and would not require any overhead information because the receiver would be self-synchronizing.

Delta Modulation (DM). A DM system is shown in Fig. 5. The input signal $v_i(t)$ is low pass filtered and sampled to obtain the $(K+1)^{st}$ sample m_{k+1}. This sample is then compared to the internally generated (K+1) estimate, m_{k+1}, and the sign of the difference is then transmitted. Therefore:

$$e_{k+1} = \mathrm{sgn}(m_{k+1} - m_{k+1}) \tag{4}$$

The estimate is formed by adding the previous estimate m_k to a step size of the proper magnitude and polarity.

$$m_{k+1} = m_k + s_{k+1} \tag{5}$$

The step magnitude can be fixed or adaptive. If the step magnitude is fixed the DM system is said to be linear. If the magnitude of the step size is adaptive, the DM system is said to be adaptive.

Linear DM (LDM). In a linear DM the estimate is being updated by adding or subtracting a fixed voltage, s_0, and the new estimate is given by:

$$m_{k+1} = m_k + s_0 e_k \tag{6}$$

where e_k determines the sign and is the quantity transmitted over the channel. A channel error would change the e_k and now the maximum error would be:

$$m_{k+1} - m'_{k+1} = 2s_0 \tag{7}$$

Because the quantization noise depends on the value of s_0

and in general s_0 is small, the error is not very significant.

Fig. 6 shows a signal which changes very rapidly from a low value to a high value. Because the value of s_0 is small it takes the LDM a number of clock pulses to catch up to the signal. This poor slope tracking characteristic of the LDM is called slope overload and makes LDM units somewhat undesirable. The maximum slope an LDM can track is given by

$$\text{Slope Max} = s_0 * f_s = s_0 f_s \text{ volts/sec} \quad , \qquad (8)$$

This poor tracking performance could be improved at the expense of the quantizing noise by increasing the magnitude of s_0, but that would result in a greatly increased graininess level. A DM capable of combining the good slope tracking capability due to the large value of s_0 together with the good noise figure given by a small value of s_0 is the adaptive DM.

Adaptive DM (ADM). Adaptive algorithms are based on the detection of a number of e_k's of the same polarity occuring sequentially. This condition indicates that the signal is constantly above or below the estimate and the magnitude of the step, sk is increased thus allowing the DM to track a faster rate of change in the input signal.

When the input e_k pattern is alternating 1's and 0's this indicates the signal to be very close in value to the estimate and the magnitude of the step s_k, is decreased such that the granular noise figure is kept at a very low value.

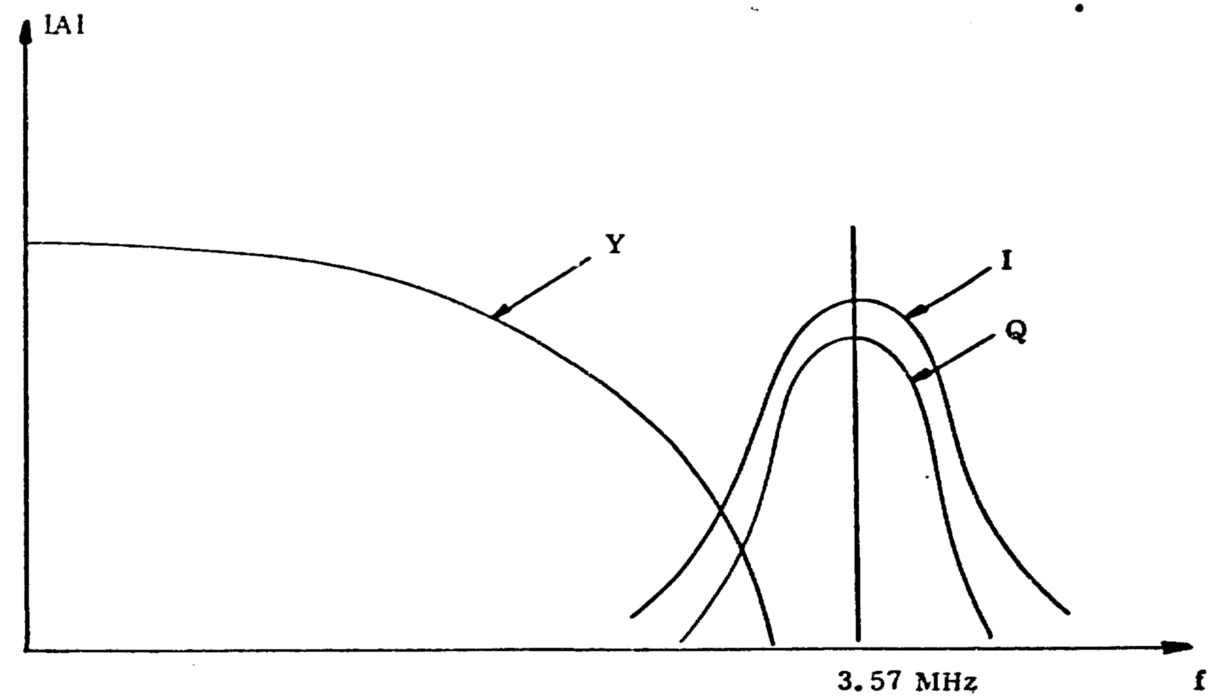

Fig. 1 NTSC Color Video Signal (Spectral Composition)

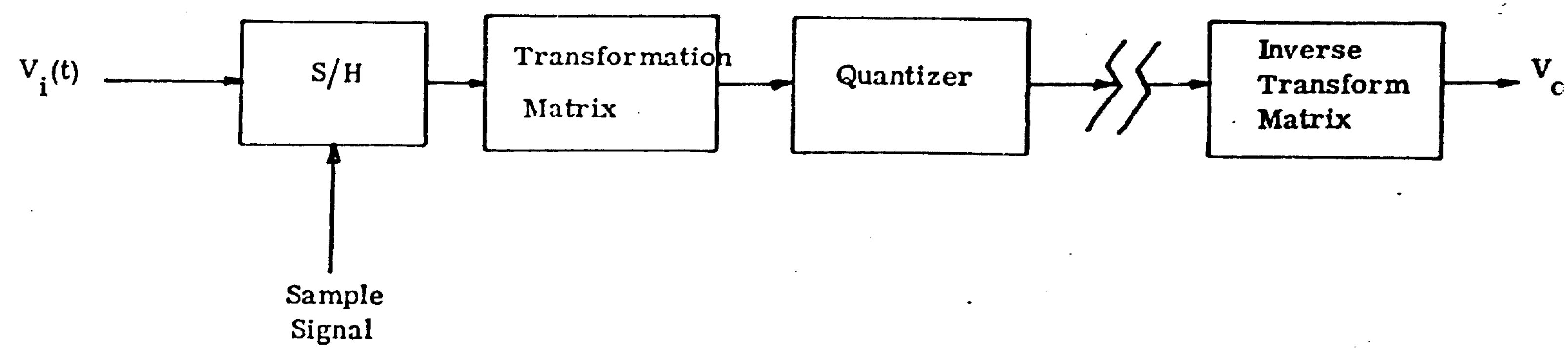

Fig. 2 Transform Encoding System

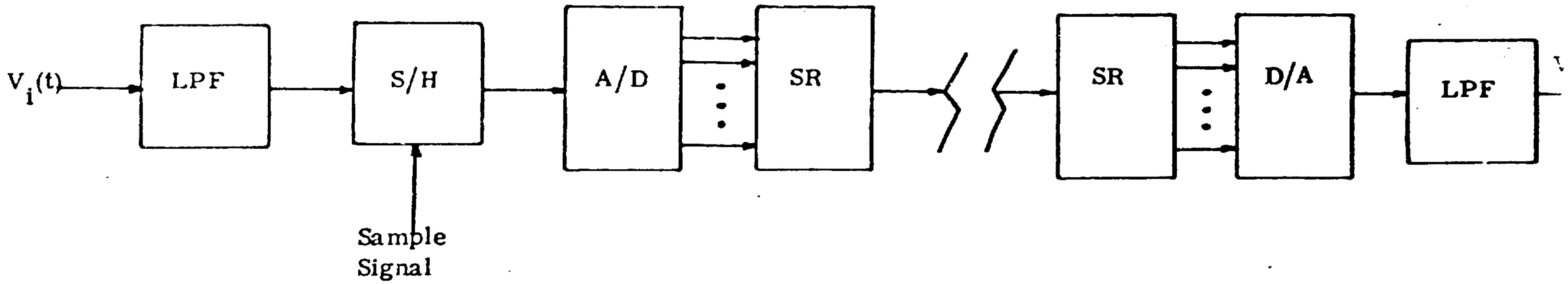

Fig. 3 Pulse Code Modulation System (PCM)

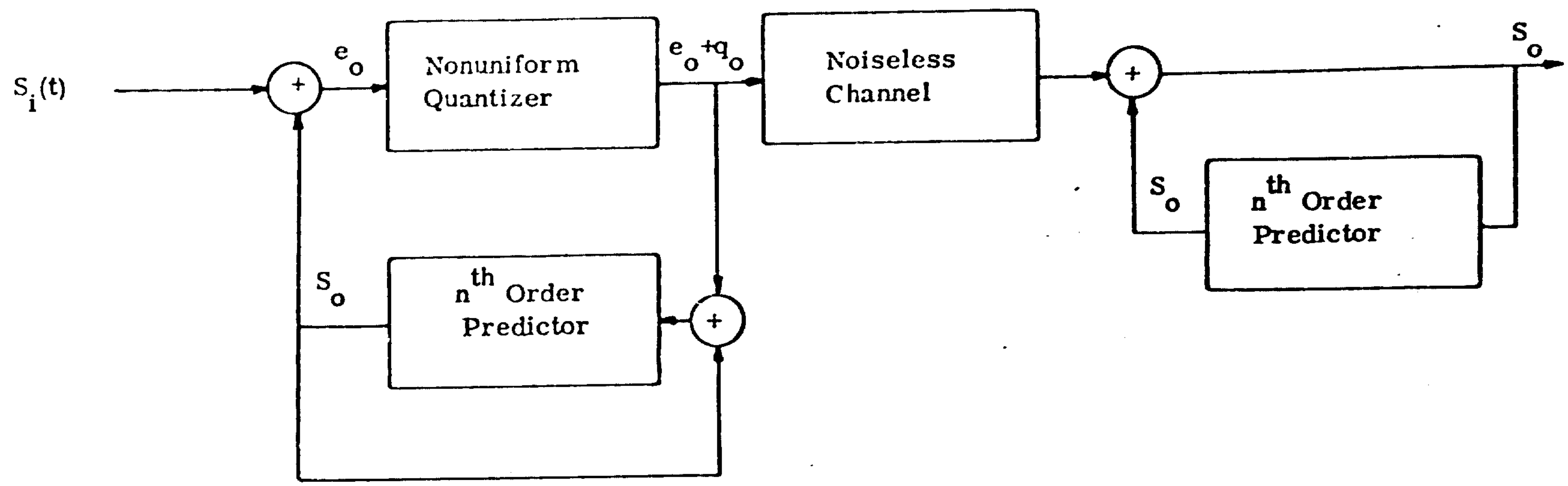

Fig. 4 Delta Pulse Code Modulation System (DPCM)

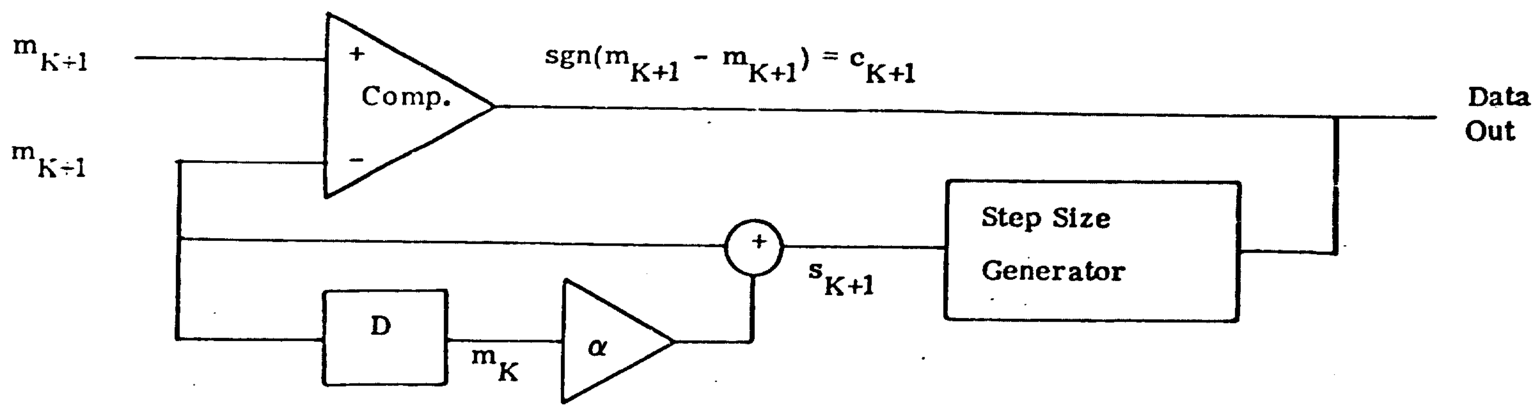

Fig.5 Adaptive Delta Modulation System (ADM)

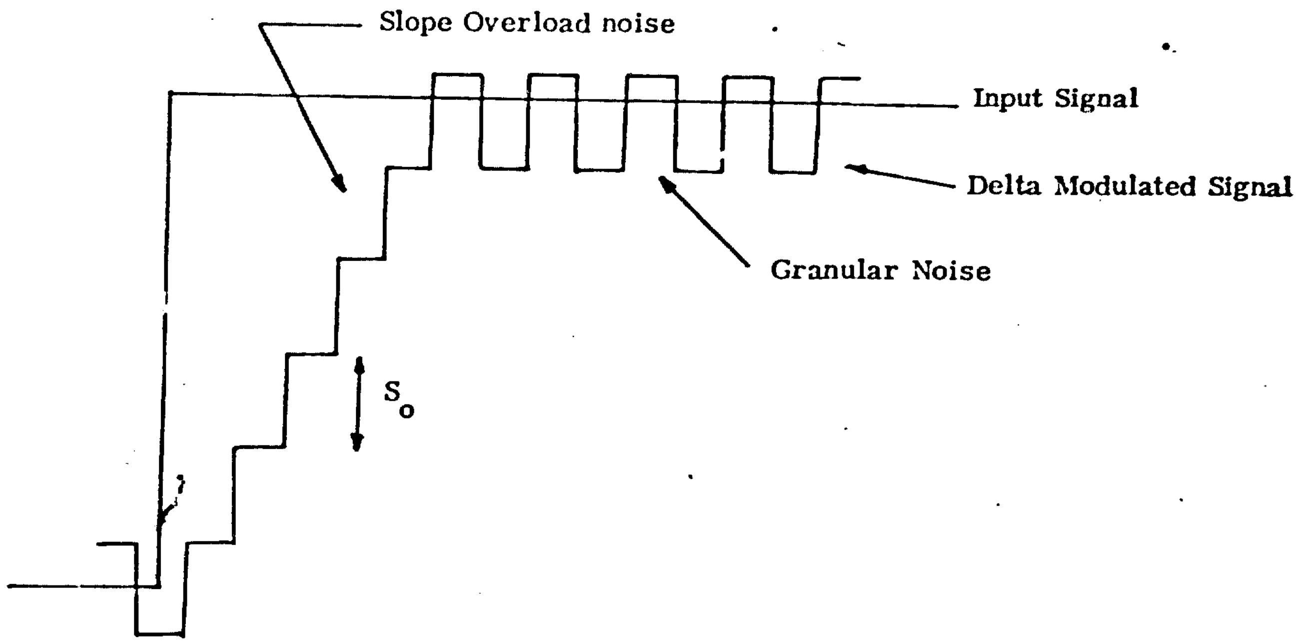

Fig. 6 Slope Overload in Delta Modulation Systems

Applications of ADM to the Encoding of Color Video Signals

NTSC

Our previous experiments have indicated that good video quality can be obtained using ADM encoding of black and white video signals at bit rates of 8 MBPS to 16 MBPS. At a bit rate of 8 MBPS the picture quality was rather poor, suffering from significant edge busyness. As the sampling rate increased, the size of the edge busyness decreased, until at a sampling rate (f_s) of 16 MHz the size of the edge busyness was reduced to approximately pixel size. Even though the edge busyness continued to decrease with an increasing sampling rate, this no longer significantly improved the picture quality. A graph showing subjective picture quality vs. sampling rate is shown in Fig. 7. The encouraging results obtained in the encoding of black and white signals via ADM prompted us to experiment with the encoding of color video signals.

We first attempted to encode the composite signals while compensating for the non-linear low pass filtering effect of the delta modulator. The experimental set up is shown in block diagram in Fig. 8. Our best results were obtained at a bit rate of 24 MBPS (which is identical to the sampling rate) and are shown in Fig. 9. It is clearly seen how the high bit rate manages to transmit a very high quality of luminance information, while somewhat degrading the chrominance information. Our attempts to improve the color quality have shown the poor performance to be due to improper signal construction. Indeed, while the delta modulator has no difficulty tracking the relatively high amplitude luminance information, it shows a very poor performance when attempting to track the low amplitude, high frequency, quadrature AM modulated chrominance information. This has shown no inherent drawback which prohibits the delta modulator from encoding color video signals, but the quality vs. bit rate of the transmitted signal will be heavily dependent upon choosing the proper format on the signal to be encoded.

RGB

Any color video signals can be represented by its red (R), green (G) and blue (B) components. Therefore, if the R, G and B components are to be sent rather than the composite color signals no information would be lost. This experiment uses more hardware (three sets of delta modulators instead of just one) and also operates at a higher bit rate. It is clear from Fig. 10 that the bit rate through the channel is the sum of the bit rates of the R, G and B channels. Based on our black and white experiment results, the similar form of the three color channels and a black and white signal, we expected to obtain good results using 16 MBPS per channel data rate (for a total data rate of 48 MBPS).

The results are shown in Fig.11 for different bit rates. Because the three channels operate independently, the superposition of the three edge busynesses has a cancelling effect which improves the subjective overall quality of the picture. The bit rate can be reduced to 12 MBPS per channel with only minor degradation. It is at this point that the picture begins to degrade more rapidly until it reaches its lower usable limit of 8 MBPS per channel (24 MBPS total data rate). It is interesting to note that as the picture quality decreases, it is basically the luminance information which is deteriorating rather than the color quality. The RGB experiment has proven the delta modulators to be able to transmit good video quality provided the signal has a proper format. This, in turn, suggests that by restructuring the signal to be transmitted, significant savings in bit rates can be achieved with no loss of picture quality.

IYQ

Introduction. The problem faced consisted of taking three full frequency channels (R, G and B at ~ 4 MHz bandwidth each) and somehow obtaining a different signal set which preserves most of the information while significantly reducing the resultant signal's bandwidth. A similar problem has been solved by the committee which created the NTSC color video standard. By forming the proper linear combination of the red, green and blue components they defined a full bandwidth luminance channel and two (greatly reduced in bandwidth) chrominance channels. The lost information defined the exact color of "small" picture elements. This loss was subjectively insignificant due to the psychovisual properties of the human eye.

The block diagram of the experimental set-up is shown in Fig. 12. This is very similar in hardware complexity to the RGB experiment with the exception of the addition of an RGB to IYQ encoder and an IYQ to RGB decoder. The resulting channel bit rate is again equal to the sum of the individual channel bit rates except that now the I and the Q channels require a much smaller bit rate. Sampling at a rate of two samples per pixel, the I channel will require a bit transmission rate of 6 MBPS while the Q channel will acquire a bit transmission rate of 2 MBPS. Furthermore, at this bit rate the color quality is very good. The Y (luminance) channel responds to delta modulation just like any black and white video signal. By varying the bit rate of the luminance channel the luminance (outline) of the picture degrades due to edge busyness, but the color quality remains very good. The results shown in Fig. 13 were obtained by allowing 8 MBPS for the chrominance information and keeping this rate fixed while the rate on the luminance channel is varied from 8 MBPS to 18 MBPS.

This experiment has shown that by proper choice of signals high quality color video information can be sent at bit rates which vary from 26 MBPS for the highest quality, to 16 MBPS for the lowest quality. This total bit rate is lower than the bit rate required for the RGB system which operates at bit rates between 24 MBPS and 48 MBPS while the quality of the transmitted video signal remains approximately the same.

IYQ Encoding in the Presence of Channel Errors. The quality of an IYQ (component) encoded color video signal does not suffer significantly when exposed to channel errors. The I and Q channels are very robust to such errors and are significantly affected only by error rates on the order of 10^{-1}. Figure 14 a,b,c shows a color video signal whose I component is subjected to an error rate of 10^{-1}, 10^{-2} and 10^{-3} respectively, while Fig. 15 a,b,c shows the same signal with the Q channel being subjected to the same error rates. The Y channel is less robust to errors, due principally to the wider bandwidth of this channel as compared to the I and Q channels. The robustness of this channel to errors is the same as expected for a black and white transmission. The effect of channel errors on the black and white ADM encoded video signal has been described in detail by Schilling and Scheinberg (21), for different bit and error rates. Figure 16 a,b,c,d,e shows the effect of channel errors on ADM encoded color video signals at a bit rate of 16 MHz and error rates of 10^{-1}, 10^{-2}, 10^{-3} and 10^{-4} respectively, when these errors occur in the Y channel.

These channel error experiments have shown that a color video signal whose components (IYQ) have been encoded using ADM algorithms, are robust to channel errors. This qualifies the ADM as a robust encoder whether the signal to be transmitted is in black and white or a color video signal.

Hardware Description: RGB to IYQ Converter. The I, Y and Q signals can be obtained from the R, G and B signals by a linear transformation.

$$I = a_1R + a_2G + a_3B$$

$$Y = b_1R + b_2G + b_3B$$

$$Q = c_1R + c_2G + c_3B$$

where the proper values for the a's, b's and c's have been given in the NTSC standard description. Because the transformation is linear, it could have been realized by a resistor weighting matrix. Instead of chosing this approach, an alternate approach was taken which uses active elements and allows buffering of the input signal, thus generating no undesirable side effects such as loading. The first stage buffers the incoming signal via an inverting and noninverting channel obtaining ±R, ±G and ±B. This eases the weighted addition process considerably since it now becomes very simple to add the R, G and B terms multiplied by a negative constant. As Fig. 17 shows, the inverting and non-inverting buffering are done in parallel, which avoids delays between the inverted and non-inverted signal. The second stage acts as an adder stage. By chosing the proper value resistors and passing the proper polarity signals, the I, Y and Q signals are formed at the output of the adders. At this point the converter also adds a fourth signal, the sync, which must be present if the signals are to be compatible with the delta modulators, as the delta modulators use the blanking period to re-initialize all of the internal registers. The negative level of the sync is determined by the clipping level of the diodes and the height of the sync is determined by the DC level adjust on the summers. The devices can operate with or without a 75Ω load impedance resistors and the output signals will be one volt peak-to-peak under full load. This converter will therefore output a commercial quality IYQ signal with the only difference of the sync addition which serves to make the signals compatible with the delta modulator.

IYQ to RGB Converter. The schematic diagram for the IYQ to RGB converter is shown in Fig.18. As it could be expected, the operation of the IYQ to RGB converter is very similar to the operation of the RGB to IYQ converter. The two difficulties encountered in the conversion are due to: 1) The presence of a sync pulse and 2) The difference of the slope of the sync information present on the Y channel and that produced on the I and Q channels which operate at a lower check rate, 3) The phase delay between the luminance and chrominance channels, which is due to the different clock rates.

Again, the first stage serves as a buffer and inverter while the second stage does the actual weighting and addition. Now, however, we are confronted by spikes generated by subtraction of two sync signals of different slope. To eliminate these spikes a slightly wider sync pulse is used, which when used in conjunction with the diode clipping stage manages to eliminate all such spikes.

The reconstructed picture will show severe chrominance misalignment. This effect is due to the much lower sampling rates on the chroma channels. To compensate for this a shift register has been built with 36 stages. A four to one multiplexer selects different delay taps at the output. Fig. 19 shows this tapped delay line. The multiplexer's select inputs are controlled by two switches which are set according to the frequency of the sampling clock on the luminance channel. The four settings will give exact alignment for a sampling frequency of 8, 12, 16, and 20 MBPS. When operating the system with the delay line, the chroma and luminance information will coincide and the displayed picture will have a good quality. A second order effect which is visible at times, is the slow color transition of boundaries. This is caused by the slow sampling rate on the chrominance channels and is not of much concern, unless the video image consists of color stripes or other such specialized, stationary inputs.

The IYQ to RGB converter is very similar to commercially available units except for the special delay and sync cancellation features. The amplifiers used on this unit have a wide enough bandwidth to allow full frequency video operation. When showing typical scenes the amount of movement has no effect upon the picture quality.

Line Sequential (LS)

Introduction. The previous experiments have indicated that by using three pairs of delta modulators and little outside circuitry good quality video can be transmitted provided that the available channel can accomodate a bit rate of at least 16 MHz (the lowest usable quality for IYQ encoding). However, for certain applications a user might be able to tolerate a loss in picture quality, provided the bit rate can be further reduced. A line sequential system attempts to do just that by using an encoding scheme which reduces the bit rate required by the RGB encoding scheme to one third of its value. Figure 20 shows that in order to accomplish this bit reduction we transmit only one of the three color channels for any given line. Assuming that we are encoding the odd field (lines 1, 3,5,7...) we encode and transmit only the red information of line one, and then encode and transmit only the green information of line three and, similarly, we encode and transmit only the blue information of line five. At this point the cycle is completed and the whole color vs. line selection restarts on line seven. In general, the encoder will transmit the red information of line (K-2), the green information of line K, and the blue information of line (K+2). The receiver has available two lines of memory which will store the two previously transmitted colors. To display a video line, the receiver will combine the two stored colors with the presently arriving color, while simultaneously updating its stored information. The results obtained with the line sequential system are shown in Fig.21 . The color quality is seen to be very good throughout with the possible exception of the horizontal edge transitions. Because we encode every other line (i.e., 1, 3, 5, 7, ...) a smearing in the vertical direction occurs which tends to cause some color blending and flicker over small horizontal transition areas. Similarly, this vertical smearing affects small horizontal curvatures and any other small details in the vertical direction which seem to get rather washed out. The effect of this encoding method on slanted lines is to create staircase patterns which even though highly visible do not appear to be very annoying. The color quality remains constant with variations in the bit rate while the horizontal smearing increases at the lower bit rates. Even though a vertical averaging takes place, the amount of movement in the scene has little effect upon the picture quality. This is the result of not operating a field but rather a line sequential system which updates fast enough to adequately represent motion.

This system represents a minimal bit rate color video system. It shows that provided the user can afford a certain amount of picture degradation, it is possible to transmit good color video at low bit rates (larger than or equal to 8 MBPS) and using hardware of medium complexity.

LS Encoding in the Presence of Channel Errors. A line sequential system operates by alternating the color information which is encoded and transmitted on every scan line. At the receiver a video signal is formed and displayed by combining the presently received color channel with the other two previously received color channels. This transmission of only one color at a time ensures a "softening" of the effect of the errors which now can only affect one color component at a time. This is shown in Fig. 22 a,b,c,d where an LS encoded video signal is transmitted at a rate of 8 MBPS and the bit error rates are 10^{-1}, 10^{-2}, 10^{-3}, and 10^{-4}, respectively.

This experiment proves that the LS encoding of color video signals via ADM is a robust, low bit rate video encoding method which could be advantageously used provided the basic system limitations are not an overiding factor.

. <u>LS Hardware Description: Control Unit Hardware</u>. The schematic diagram of the control unit is shown in Fig.23 . The clock input is buffered by a 7404 inverter. This inverter drives four other inverters which share the load. This makes the control unit appear as only one TTL load and, at the same time, it helps preserve the shape and rise time of the clock waveform. This is very important in any synchronous system where a number of operations are occurring concurrently and any mistriggering would have serious consequences upon the system's operation. The two 74164 serial to parallel converters form a delay line. The 74193 counter uses its carryout output to load the converter with a 10 ... 0 pattern. Every clock pulse the high output will shift one position. For example, after the first occurrence of the clock, the new output will be 010 ... 0. The Q_0 through Q_{15} outputs will therefore specify sixteen distinct phases, which will be used to direct set and reset a 7474 flip flop such that its output Q will have the proper timing for the memory write enable ($\overline{WE}$) signal.

A 7495 binary counter is wired up to form a modulo three counter. The horizontal drive activates its "count in" input and.its output indicates which line (R, G, or B) is to be transmitted. Should any power supply noise mistrigger the counter, the error will not propagate to the next frame because at the beginning of every frame the counter is reset by a new frame pulse ($\overline{NFP}$). The $\overline{NFP}$ signal is obtained by transfering the horizontal drive ($\overline{HD}$) data which is present at the input of a D type flip flop to its output Q, on the rising edge of the vertical drive signal ($\overline{VD}$) which is present at the clock input Q will indicate whether the odd or the even field is being transmitted. To create a new frame pulse the field indicator (Q) triggers a 74123 one shot for a duration of approximately 400 nanoseconds (ns).

The outputs of the 7495 modulo three counter are first decoded and then used to enable three AND gates which will generate the $\overline{WE}$ signal for the proper memory bank. Therefore, one memory will always be updated as the other two memories are being read. The memory addresses are provided by two 74193 counters, the first one being driven by the 16 megahertz clock. To insure the proper phase between the data out and clock signals, a tapped delay line is used which provides five taps with a delay of five nanoseconds per tap.

The 7495 counter, which operates in a modulo three mode, drives the select inputs of a four to one multiplexer. The multiplexer chooses one of the input channels (R, G, or B) and outputs it. The output of the multiplexer represents the actual channel. The whole control units fits on a 5" x 5" card and contains all of the logic necessary to generate every control signal. This, in turn, allows the memory storage units to be much simpler, which is a definite advantage in the actual operation of the system.

Memory Unit Hardware. A schematic diagram of the memory unit is shown in Fig. 24. Each memory receives all of its control signals and data inputs from the control unit. The memory data out signal does not go back to the control unit but is outputted directly. The memory uses a "memory multiplexing" scheme. The data in is shifted in the 74164 serial to parallel converter until the shift register is full (16 bits). The contents of the shift register are then latched in a number of 74174 latches. The memory unit which is organized as 64 x 16, will write the data from these latches. When the memory is read, its output is again latched in 74174's and these latches are connected to a parallel to serial converter. The data is read into the converter at a rate of one megahertz and it is shifted out of the converter at a rate of sixteen megahertz. It is readily apparent how this "memory multiplexing" technique allows relatively slow memory units to operate at much faster apparent rates. In this design the memory speed multiplication factor is sixteen. The data out signal is chosen by a two to one multiplexer from two different data paths. When the memory is being updated, the video signal is formed by the present signal and the two previous colors. Therefore, when the R/W signal is in the write mode, the data out comes from the input serial to parallel converter. The extra delay is necessary for the proper alignment of the three channels. While one memory is being updated, the other two memories are being read. When read, the memory's output is latched, converted to serial form, and shifted out via the multiplexer. The maximum speed of operation for the memory units is limited to ~17 MHz by the input shift register. Due to their conceptual simplicity and low chip count, the memory boards have been built with PC boards which made the task of building and debugging the memory units feasible.

Conclusion

A number of color video encoding schemes have been investigated. Even though they all use delta modulators to encode the actual signals, their individual advantages and disadvantages are quite different. This makes an overall comparison extremely difficult. Fortunately, the range of bit rates that the individual systems can operate over are largely non-overlapping. This makes it possible to say that given a requirement for the best possible quality, and given a channel which can accomodate a rate of 24 MBPS to 48 MBPS, an

RBG encoding system would be a proper choice. An IYQ system operates almost as well but requires a substantially lower bit rate. To operate such a system the channel must be able to accommodate a bit rate of 28 MBPS to 16 MBPS. If the channel can only accomodate a bit rate of less than 16 MBPS but higher than 8 MBPS, and if the vertical degradation seems to be unobjectionable, then a line sequential system is the only remaining choice.

We conclude that the above research has accomplished its goal: all of the above methods are able to transmit a video signal with a good color quality. The degradation increases as the available bit rates decrease. In all cases the systems perform better than any PCM system at the same bit rate. Furthermore, when the bit rate is reduced it is not the color but the luminance information which degrades. Given the fact that the ranges of operation are not overlapping, it is possible to specify the best system to be used for any particular application.

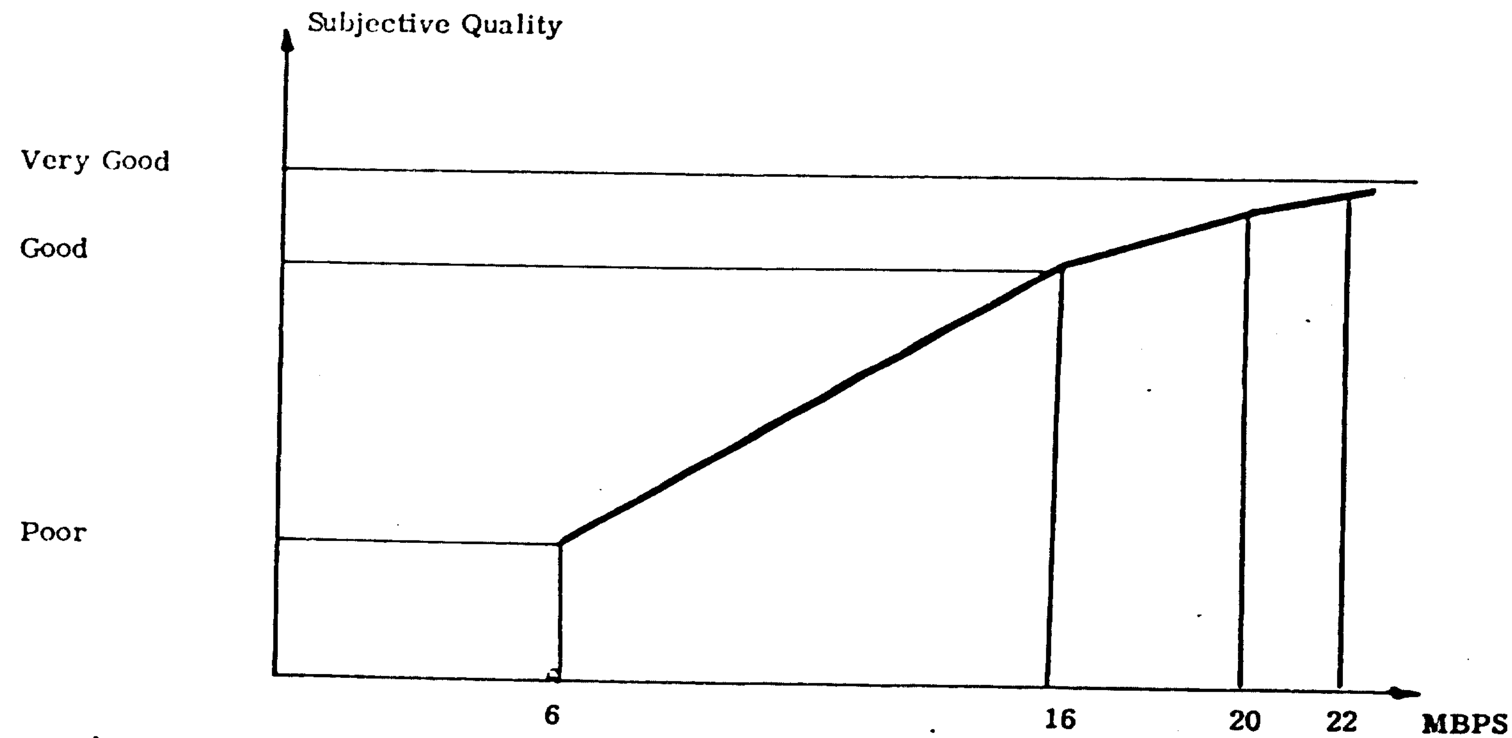

Fig. 7 Subjective Picture Quality versus Bit Rate

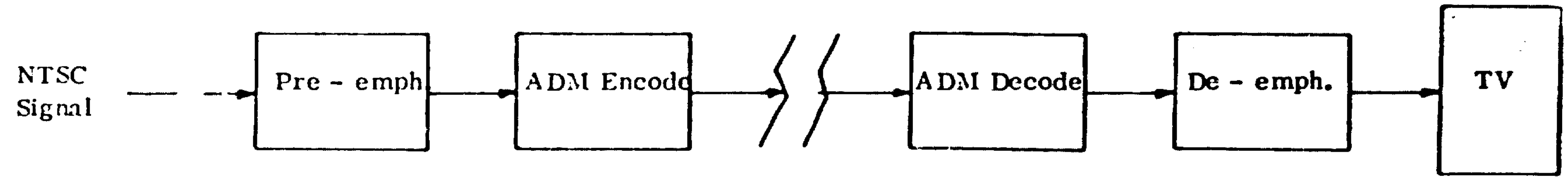

Fig. 8 NTSC Encoding of Color Video Signals

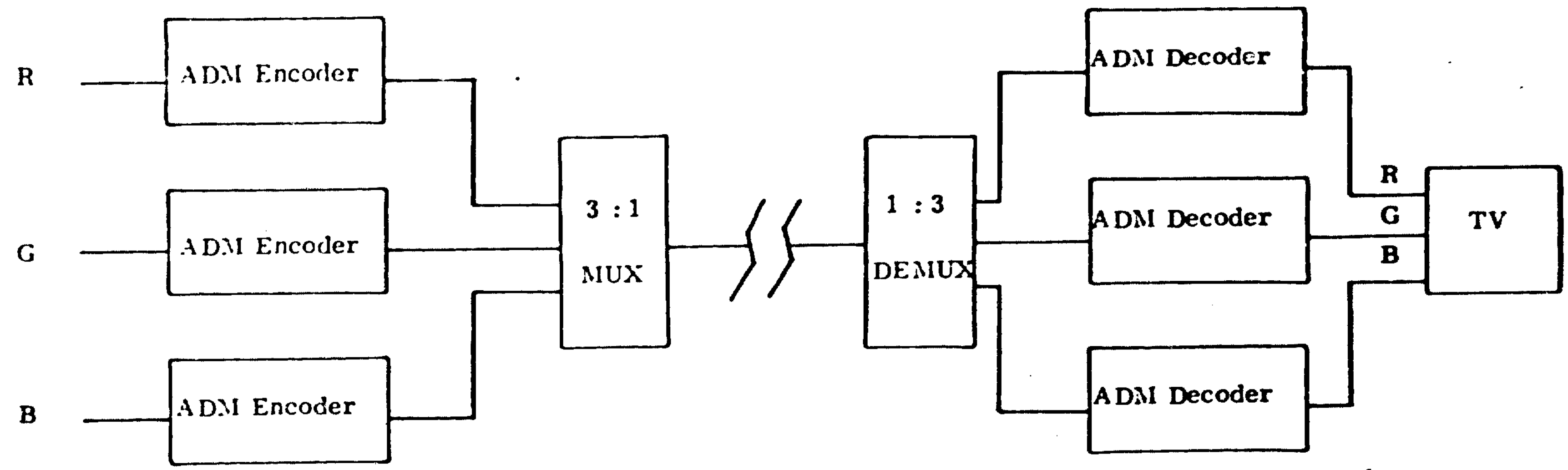

Fig. 10 RGB Encoding of Color Video Signals

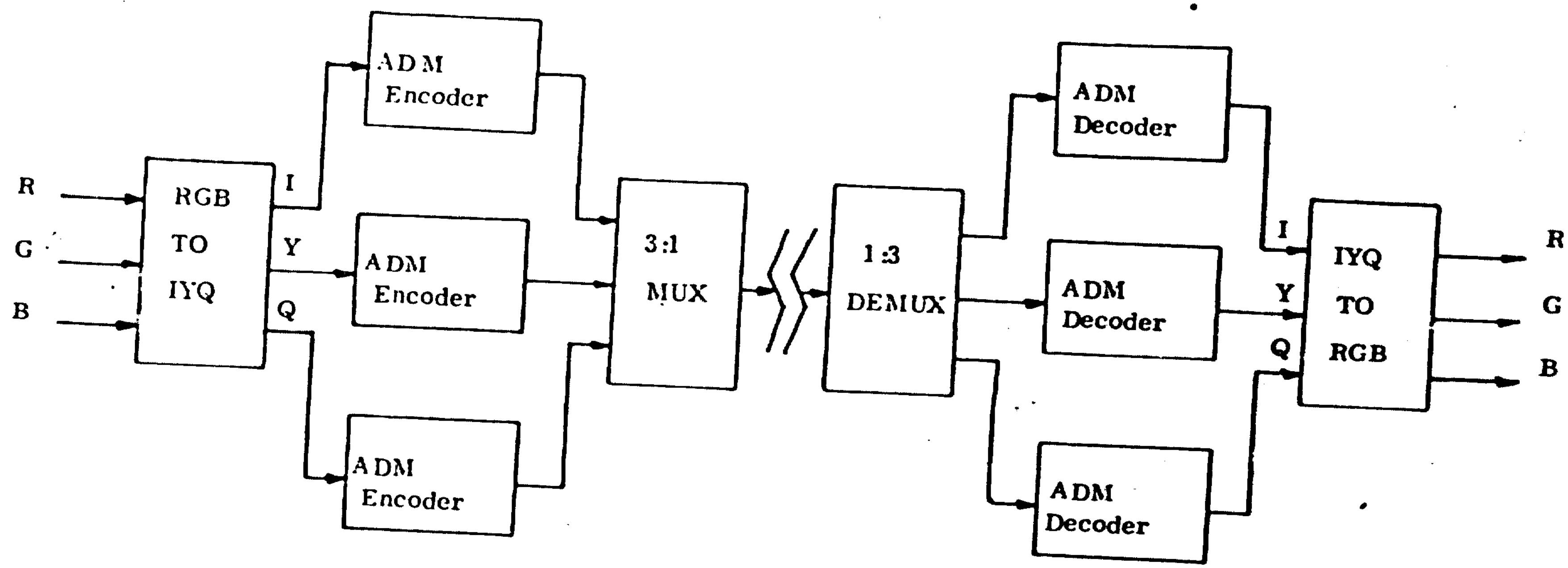

Fig. 12 IYQ Encoding of Color Video Signals

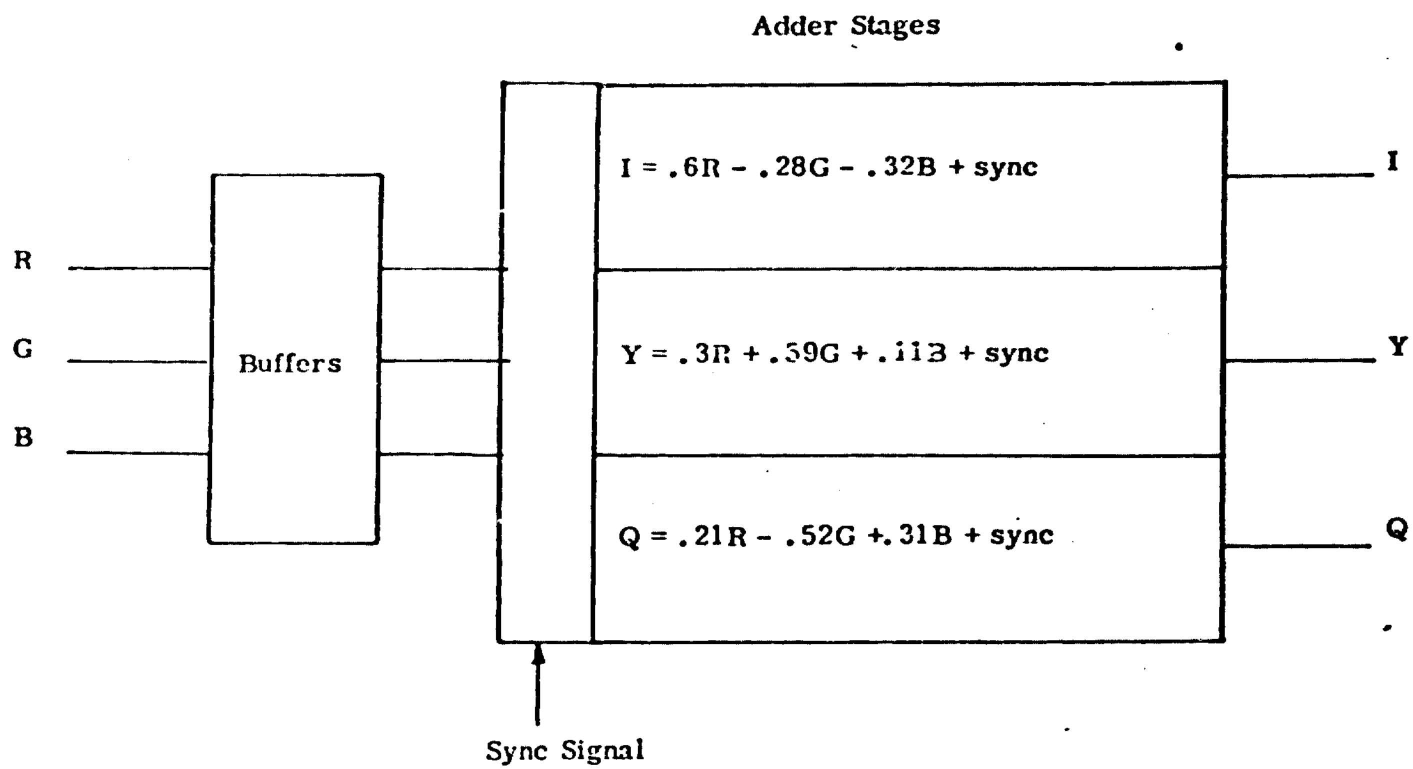

Fig. 17 RGB to IYQ Converter

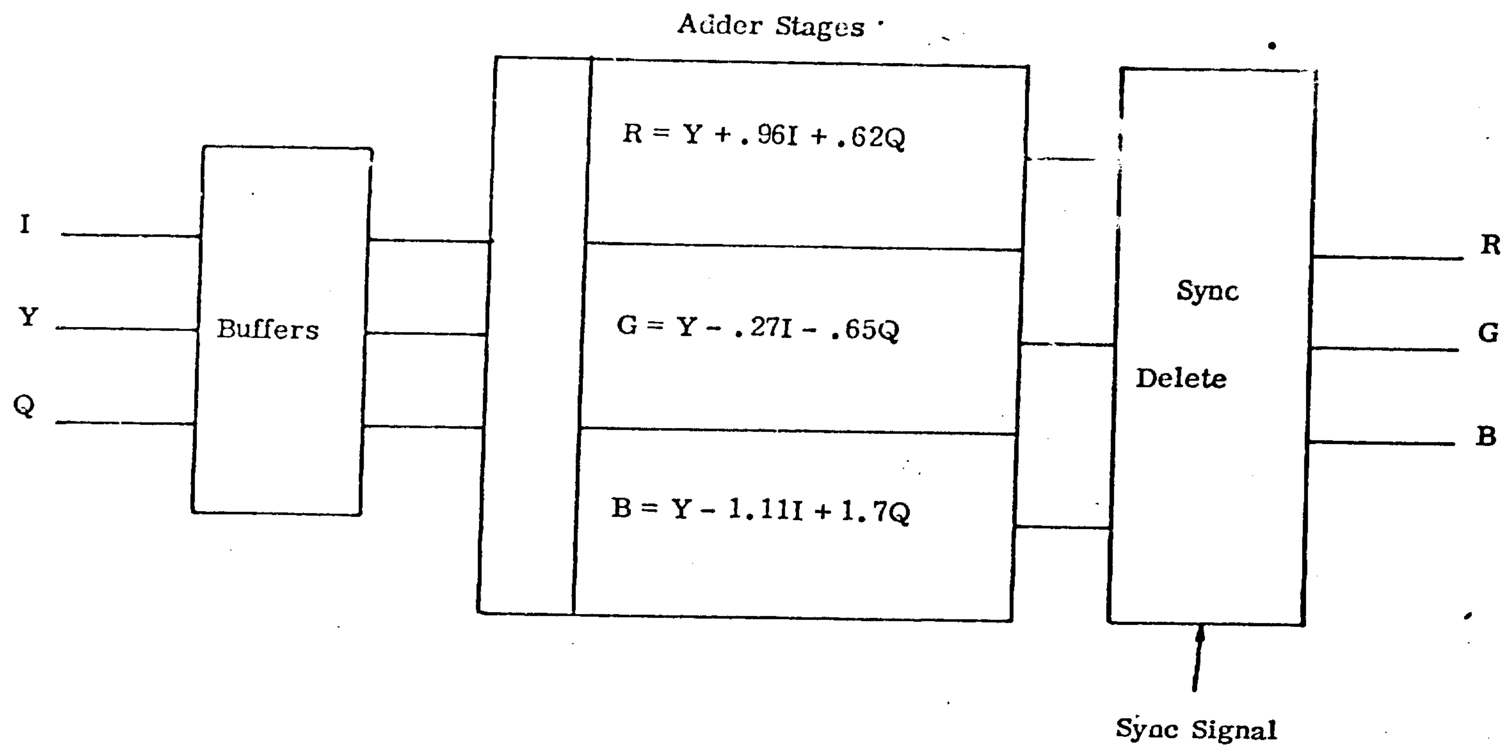

Fig. 18 IYQ to RGB Converter

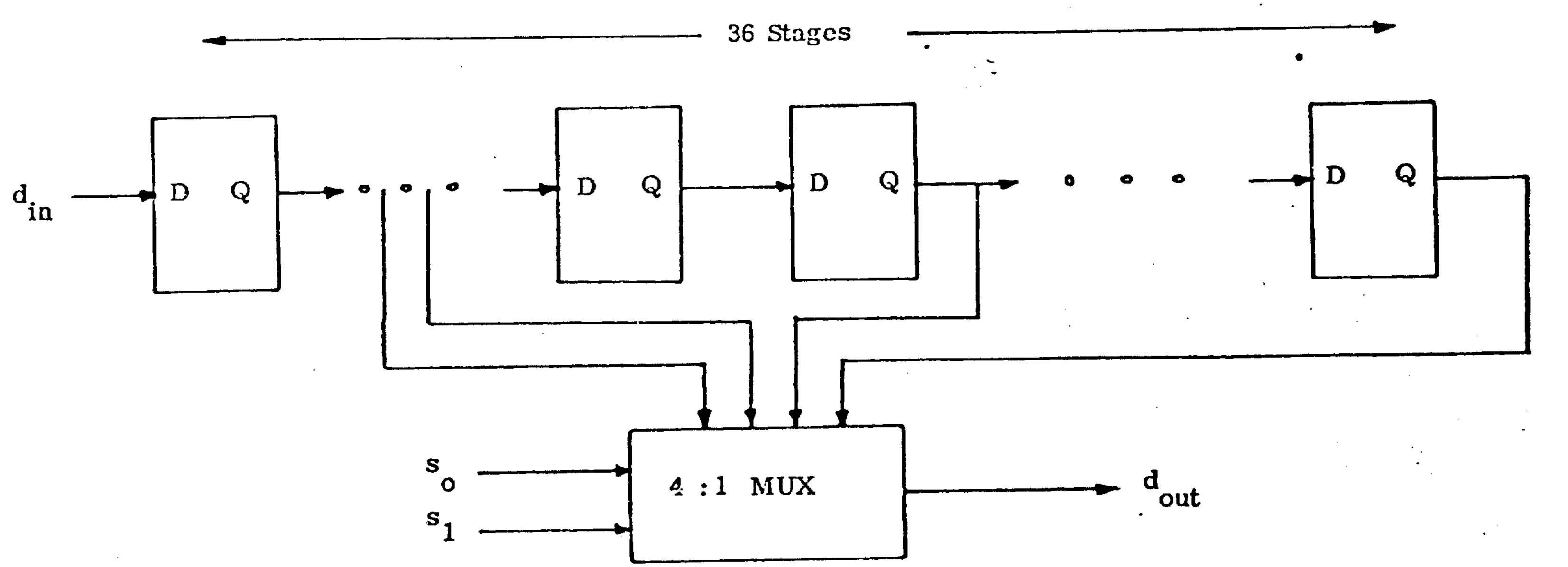

Fig. 19 Tapped Delay Line

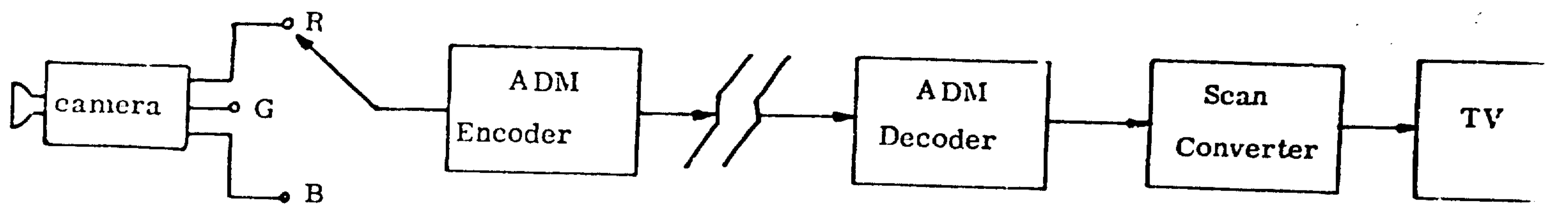

Fig. 20 Line Sequential Encoding of Color Video

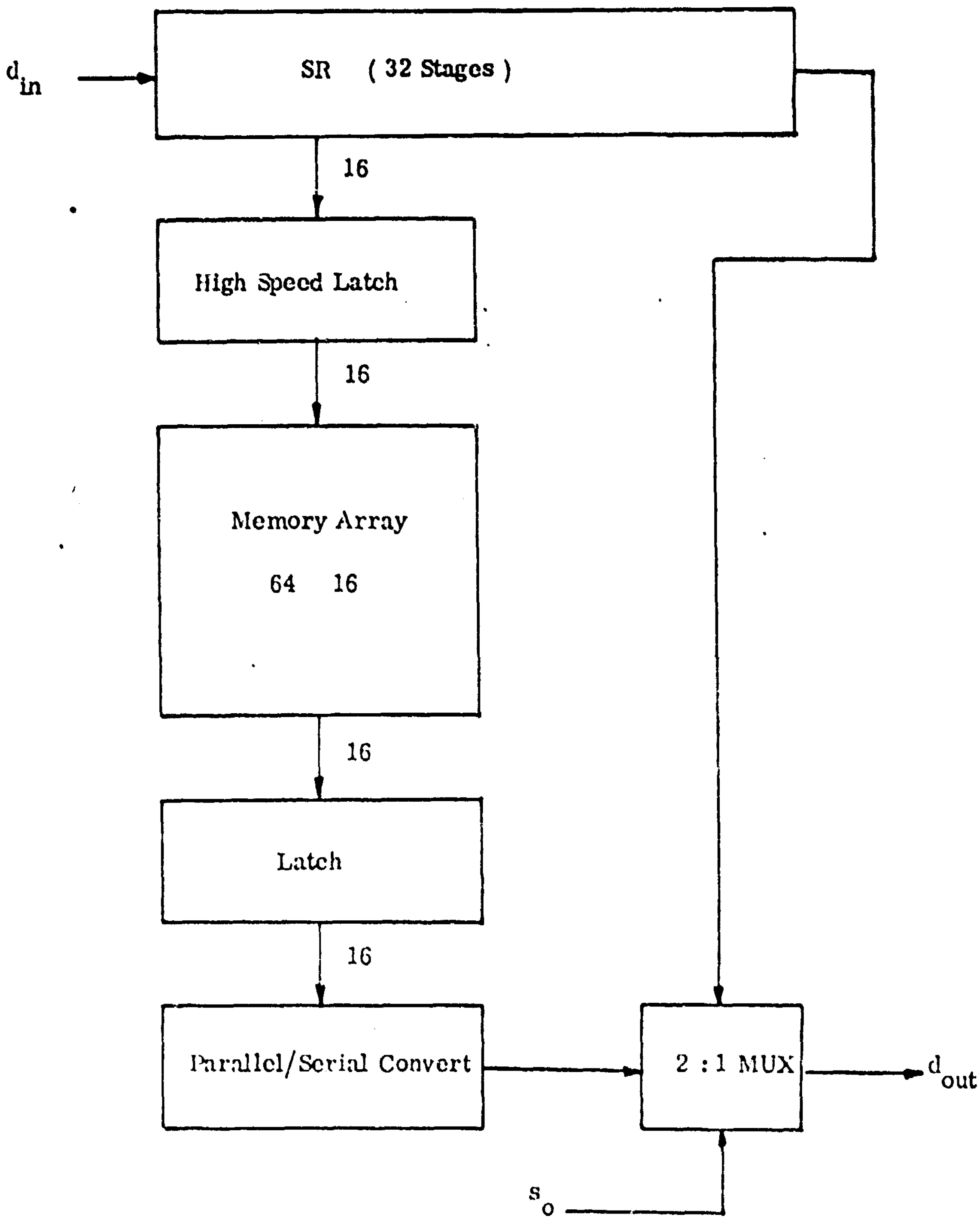

Fig. 24 Line Sequential Memory Unit

APPLICATION OF ADM TO PACKET VIDEO TRANSMISSION

Introduction

The appearance of inexpensive, powerful computers has encouraged their widespread application in almost every conceivable domain. One of their most demanding applications in the communications field is in a traffic supervisory role. Having linked many centers of human activity, the designers next attempt to make the resulting communication process as efficient as possible. As a result, several communication nets came into being which allow direct computer to computer transmissions. For these nets to be effective, new protocols and transmission philosophies had to be created. The need for efficient operation of the net has resulted in computers controlling the local routing and traffic destination in every part of the net. The traffic now consists of messages which are divided into groups of a pre-assigned number of bits, called packets. The local controller adds a destination address and then it proceeds to send the packet via the least busy route.

The largest of these nets is the ARPA net, operated in the U.S. by the Department of Defense.

An investigation was launched to evaluate the kind of quality one could expect from voice and video transmissions over such nets. Reference (22) describes the work done by

Tanaka, Dressler and Chackavarty in the simulation of voice transmission via computer communication nets. The voice was digitally encoded via an ADM scheme which resulted in a much lower bit rate than that corresponding to PCM encoding. Since the. sampling rate involved in voice communications is relatively low, there was no need for much support hardware, as much of the processing was done in real time. Video rates prohibit a direct ADM-computer interface, with the speed of the computer being the limiting factor. Therefore, two methods of video acquisition had to be investigated. One would rely on. vertical scanning to generate the pixels. Fig. 25 shows how a vertical scanner samples all of the n^{th} pixels from every line during a given frame. Every new frame the scanner proceeds to scan the $(n+1)^{st}$ pixels, until the whole frame has been transmitted. By using this scanning method the sampling rate is reduced to less than 16 KHz which is low enough to be handled by a computer directly. The difficulty lies in the video reconstruction process at the receiving end. Even though the receiving computer may have the required memory, it is doubtful that it could sustain the high data rate required for a real time video display. Therefore, the receiver had to have a digital frame storage which had to be controlled by a custom built controller optimized for this application.

Through careful design the same frame storage can be used for both, the transmission and reception of the digital video frame. Due to the high data rates necessary for the transmission of video images, a decision has been made to use an ADM encoder because this would minimize the bit rate while maintaining an acceptable quality level.

Hardware Description

Fig. 26 shows the controller block diagram. Again, inexpensive, relatively slow memories are being used at an apparent rate which is much higher than their maximum read/write frequency. This is accomplished via the memory multiplexing technique which has been described previously. The data stream is stored in groups of 16 bits which are first converted to a parallel format. The maximum data rate is 16 MBPS which corresponds to roughly 1K bits/line of video. Therefore, each line of video requires at most 64 memory locations of 16 bits/location. The total number of lines in a video frame is 525 and, therefore, the total storage capacity for the frame of memory is 32K x 16. 32K locations require a 15 bit address. Because the individual memory chips have a 4Kx1 internal organization, the low order 12 bits of the address are being used to address each individual chip while the three high order bits are decoded and used to select any one of eight rows of memory chips. This memory organization of 8 x 16 chips is shown in Fig. 27. Synchronism with respect to the camera driving signals is achieved by using the $\overline{NFP}$ and $\overline{HD}$ signals. In addition, the chock used with the ADM encoders is synchronized to the $\overline{HD}$ signal. The read/write command is synchronized to the $\overline{NFP}$ pulse and guarantees reading or writing an entire frame. Once the memory unit has been completely filled with one video frame it goes into a read state which performs the continuous memory refresh and enables the operator to inspect its contents visually (via an ADM decoder and a TV monitor). Provided the stored frame is satisfactory provisions have been made for a computer interface which has a random access feature, yet it does not interfere with the refresh cycle.

A block diagram of the computer interface is shown in Fig.28. The computer address is loaded into the upper nine address bits. The remaining six low order bits cannot be jam-loaded from the computer as this would interfere with the refresh cycle. Instead, the low order six address bits are compared to the computer requested address. When a match is made, the data is loaded into the latch. The computer can then load it into its memory and format it for transmission. The maximum waiting time for the data and latch to be loaded (the memory limitation in speed) is given by the maximum time it takes for the address to cycle through $2^6 = 64$ states. At one microsecond per state it takes 64 μs for a complete cycle through and $64 \times 10^{-6} \times 32 \times 10^3 \doteq 2s$ for the loading of a complete video frame (c_k's). The computer can then format and transmit the video information to any other computer on the net. In turn, it can also receive a video frame and use the same hardware to display it. Upon receiving a frame of e_k's, the host computer can, via the interface, load the frame of e_k's into its video memory and the operator can view the video image via an ADM decoder on a TV monitor.

Conclusion

An inexpensive digital storage has been described which serves as an interface/buffer between a high speed digital data stream coming from a video ADM and a computer. The same device acts as an interface/buffer in the opposite direction, allowing the computer to load it with a frame of e_k's and then displaying the video frame in real time via an ADM decoder and a TV monitor. The pictures are either black and white or color, provided that a line sequential technique is being used. The maximum bit rate is 16 MBPS. The technique used is independent of the type of memory used, and a controller could be built to operate with any video display such that a full video feature could be added to any terminal provided it has the required amount of memory (32K × 16).

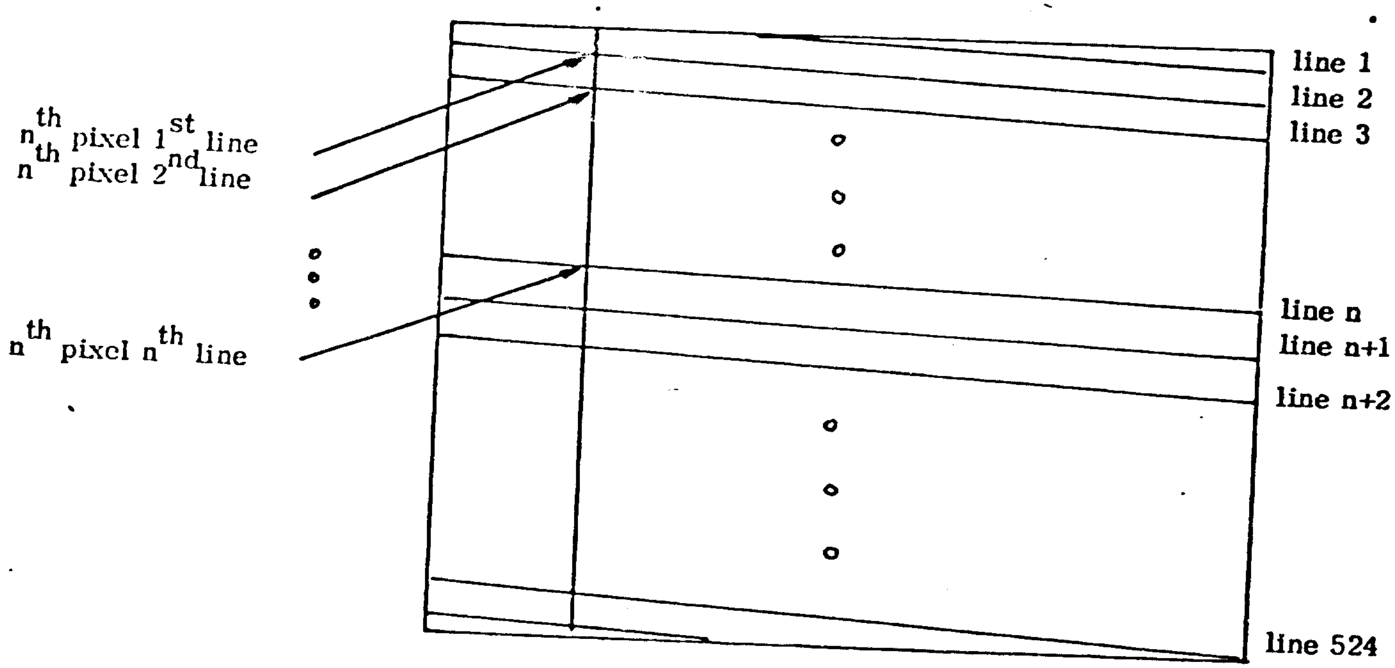

Fig. 25 Vertical Scanning of Video Signals

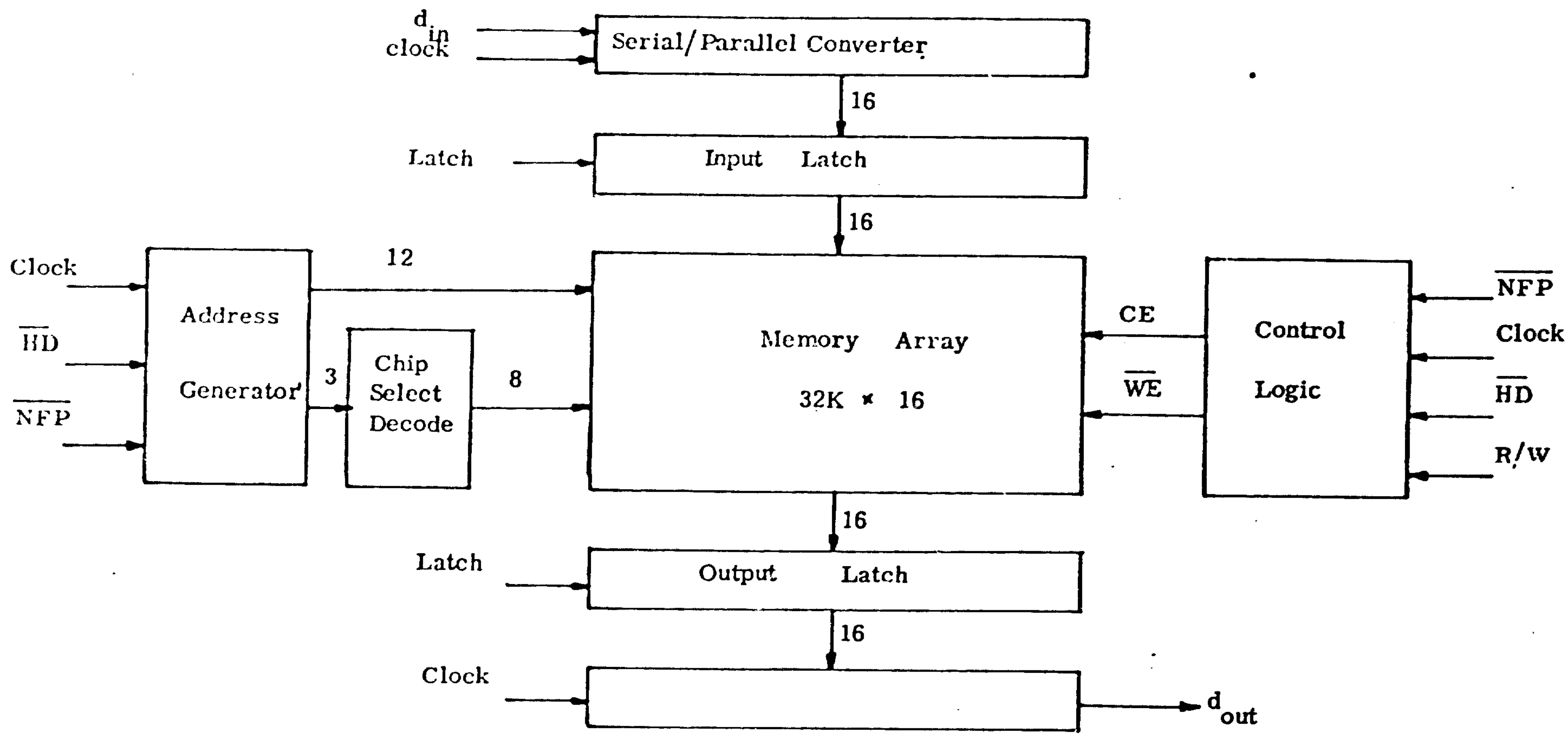

Fig. 26 Slow Scan Controller Block Diagram

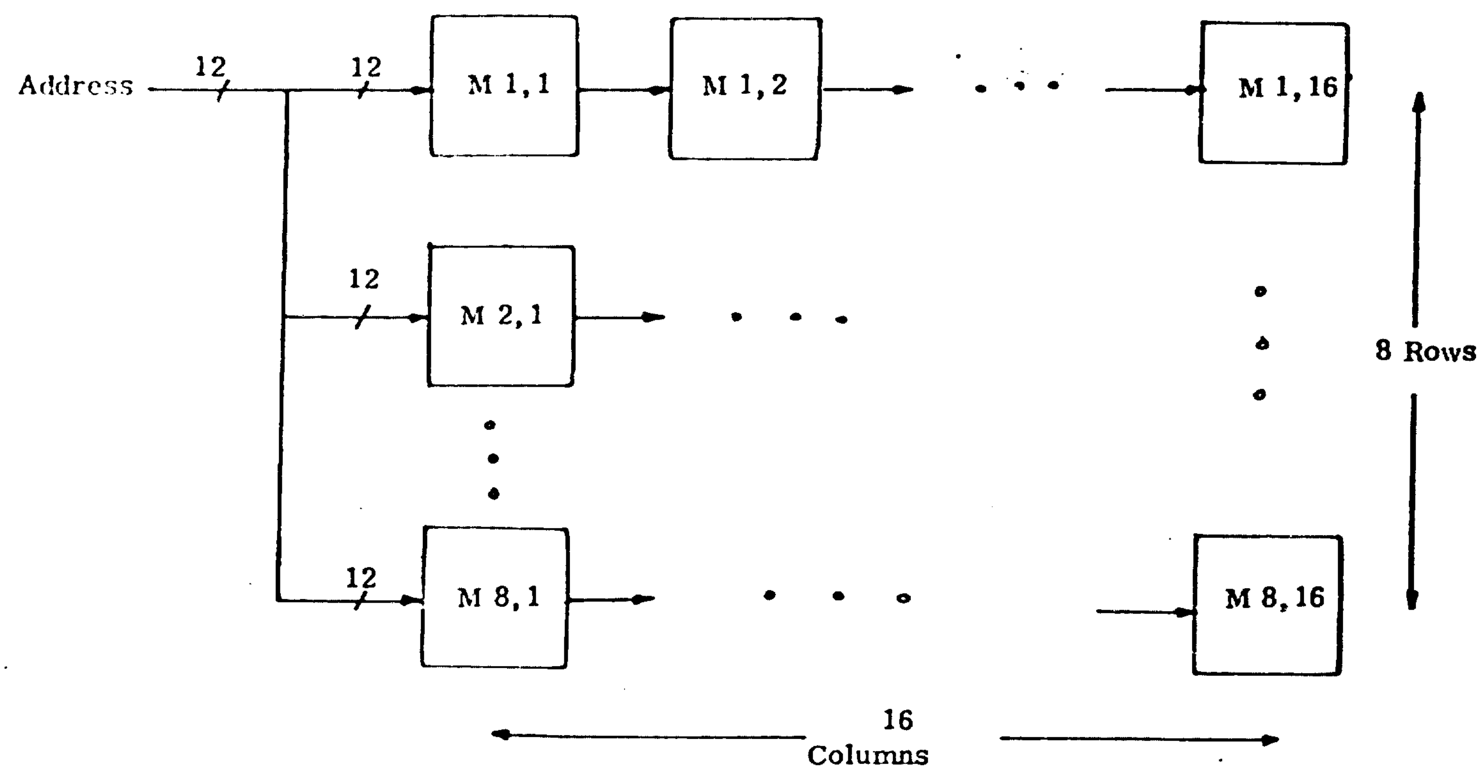

Fig. 27 Memory Array Organization

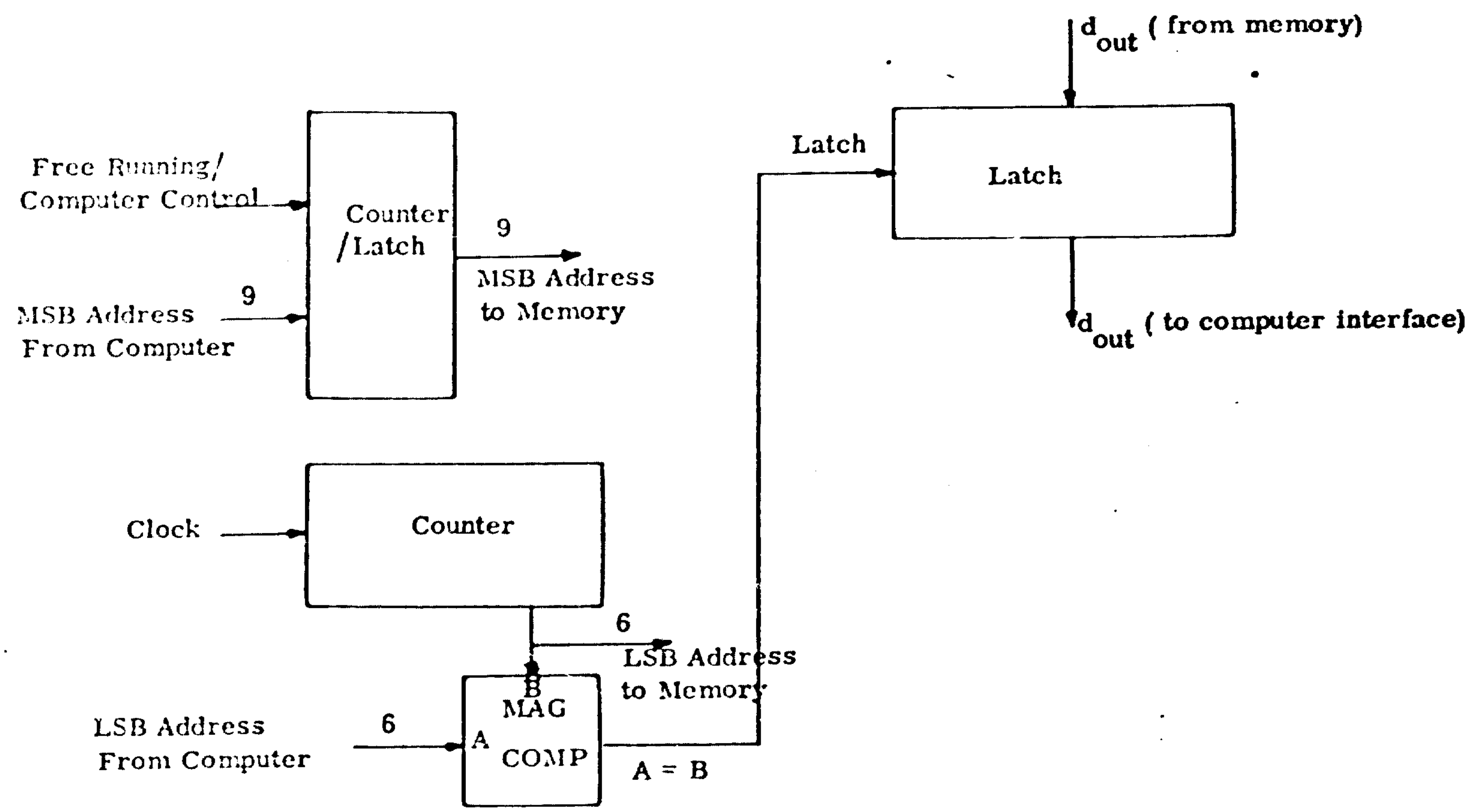

Fig. 28 Computer - Memory Interface

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