DESIGN AND BREADBOARD EVALUATION OF THE SPS REFERENCE PHASE CONTROL SYSTEM CONCEPT

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1. INTRODUCTION

Efficient operation of a very large phased array such as the proposed solar power satellite [1], requires precision focusing and pointing of the power beam; i.e., the power beam must have a planar wavefront directed precisely at the center of the target antenna (rectenna). To maintain such a power beam requires real-time phase compensation at each subaperture in order to adjust for structural deformations and other transitory factors. In the current solar power satellite (SPS) baseline, the spaceborne antenna (Spacetenna) is an active retrodirective array [2], [3]. A pilot signal transmitted from the center of the rectenna is phase-conjugated at each subaperture (power module) of the spacetenna, thereby assuring that the radiated composite wave is focused on the target. This scheme requires a large amount of precision electronic circuitry on the spacetenna. Specifically, pilot receivers must be located at each power module and an adaptive distribution network is required in order to provide a properly phased reference signal at each conjugator [4], [5].

In order to verify theoretical and simulation results, a project was initiated by the Tracking and Communication Systems Department of Lockheed Electronics Company to design, develop, and test a breadboard system comprising a pilot receiver and transmitter, phase distribution system, and power transponder. This breadboard system is to be used in the Electronic Systems Test Laboratory (ESTL) at the Johnson Space Center. The total breadboard system will include one pilot transmitter, one pilot receiver, nine phase distribution units, and

two power transponders. It will be shown in the following sections of this paper that with this complement of equipment, segments of a typical phase distribution system can be assembled to facilitate the evaluation of significant system parameters.

The major objectives of the project are to determine the achievable accuracy of a large phase distribution system, the sensitivity of the system to parameter variations, and the limitations of commercially available components in such applications.

2. ACCOMPLISHMENTS

The design and development of a breadboard Master-Slave Returnable Timing System (MSRTS) was the first objective of the project. Nine units were planned; three were completed and used for prototype evaluation tests. Six remaining units are in final assembly.

2.1 MSRTS BREADBOARD

The MSRTS breadboard system is of a modular design with three major elements. These are the Phase Tracking Unit (PTU), the Interface/Return Unit (IRU) and the Main Frame. Modular construction permits the equipment to be configured in various ways as required to model portions of the proposed SPS phase distribution tree network. A simplified functional diagram of a single MSRTS stage is shown in Figure 1. Figure 2 shows the tree distribution structure for which the breadboard MSRTS is designed.

The major components of the PTU are Voltage Controlled Oscillator (VCO), loop filter, circulator, mixers and a phase detector. The phase lock loop circuitry is used to advance the phase of VCO to compensate for the effect of the delay introduced by the path between nodes of a tree structure.

At the IRU, two functions are performed. First, a portion of the received reference signal is returned to the preceding PTU via the single interconnecting cable. This return signal arrives at the PTU with a phase delay proportional to the line length. The delay is measured in the phase detector

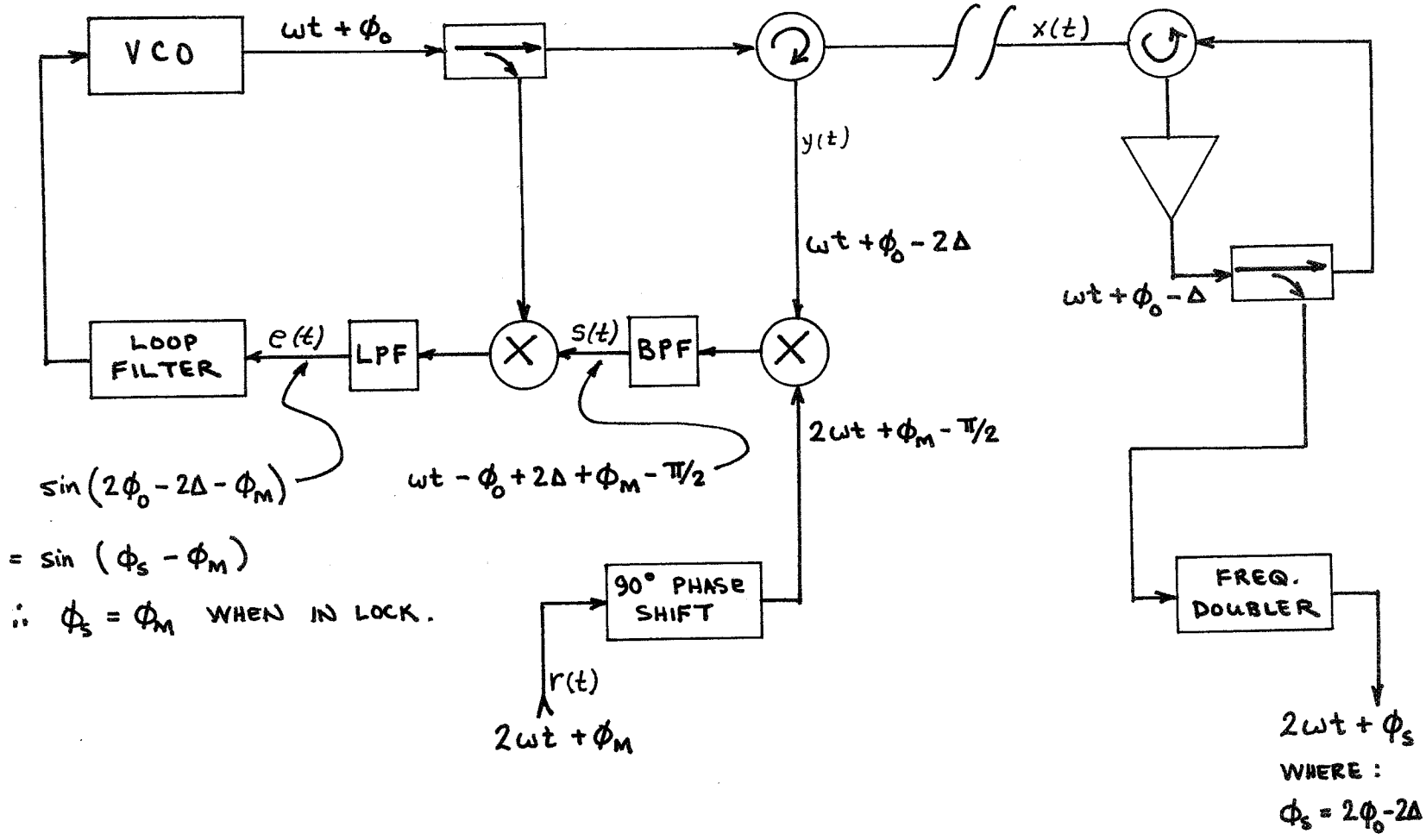

Figure 1. Simplified functional diagram of MSRTS.

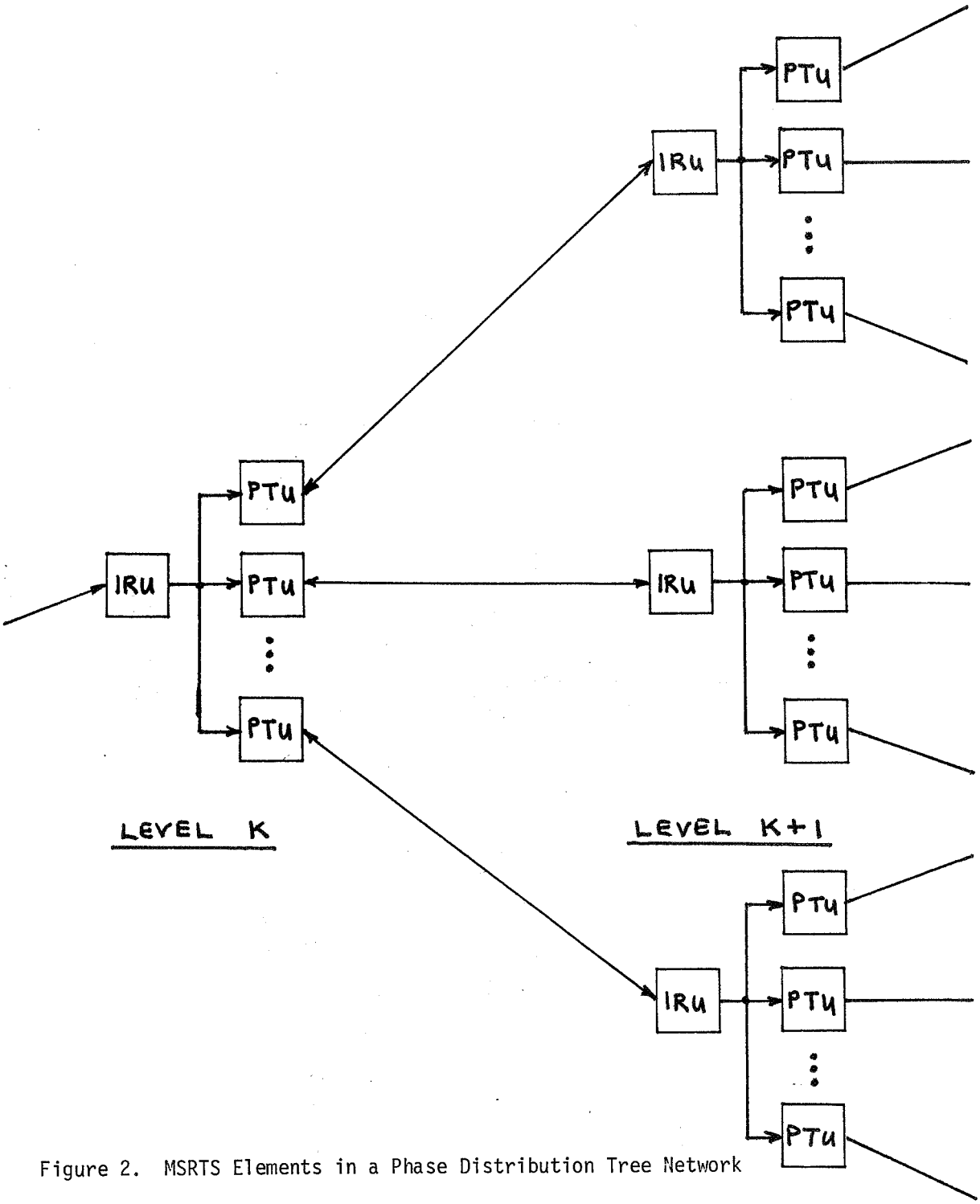

Figure 2. MSRTS Elements in a Phase Distribution Tree Network

of the PTU, and the VCO phase is appropriately adjusted so that the reference phase is correct at the IRU input. Second, the reference signal at the IRU is doubled in frequency to match the reference input to the PTU. When the PTU is phase locked, the phase of the IRU output signal is the same as the phase of the preceding PTU input signal, within the accuracy limitations of the hardware. Each IRU can provide up to four outputs.

The Main Frame contains supplies and a patch panel that facilitates the interconnection between PTU's and IRU's mounted in separate mainframes. Each mainframe is capable of supporting a total of three PTU's and/or IRU's.

2.2 MSRTS BREADBOARD TEST RESULTS

Three prototype MSRTS breadboard units were used in a variety of test configurations to evaluate the accuracy of phase control and the effects of component imperfections. These test configurations included those shown in Figure 3.

For example, the three-node series network of Figure 3c was tested with 30 different cable combinations, using RG-14 coaxial cable in lengths between 200 and 250 feet (60 - 80 meters); that is, after initial adjustment of the test configuration with zero phase error on the vector voltmeter, 30 different combinations of cables were substituted for Test Cables A and B. For each combination, the resulting phase error was measured and recorded. The results are presented in the histogram of Figure 4, which indicates a standard deviation of error of 4.2^{o}. This experiment is intended to demonstrate the accuracy of the breadboard MSRTS with arbitrary cable lengths. It is important to note that the cables were not cut to precise measurements.

Another type of phase error measurement was made with the configuration of Figure 3a. Minor variations in electrical line length were introduced by means of a phase shifter (PS2). The phase error at the vector voltmeter was initially nulled with PS2 set to zero. Then PS2 was varied from 0 to 180^{o}, equivalent to a half-wave variation in cable length. The resulting phase error is shown in Figure 5.

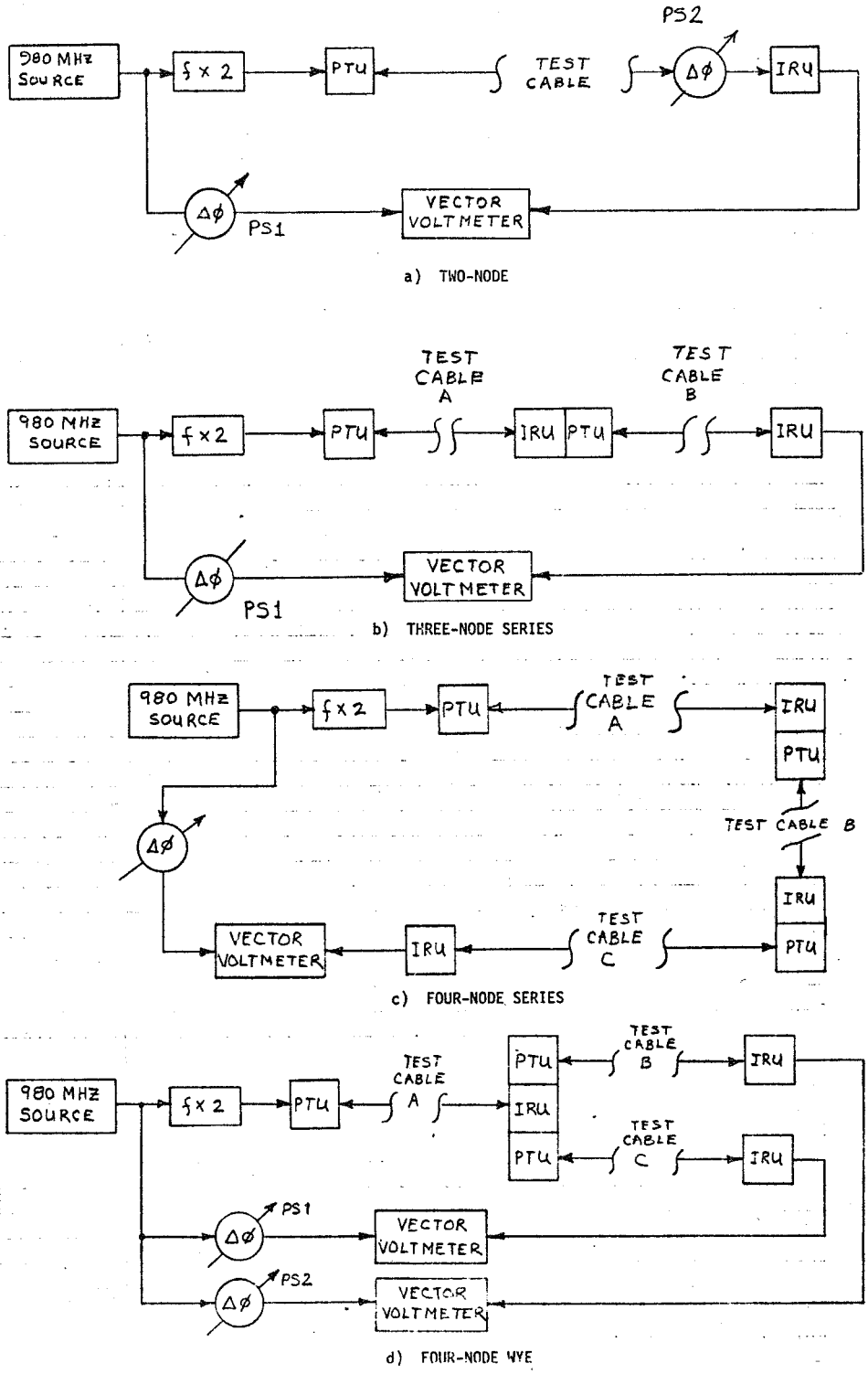

Figure 3. MSRTS Breadboard Test Configuration

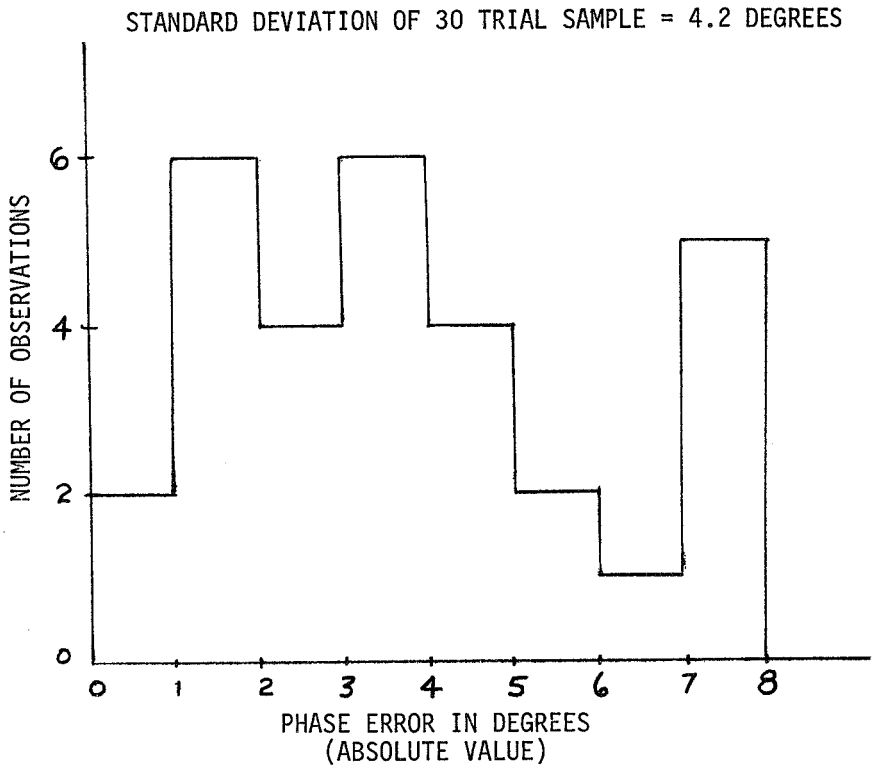

Figure 4. Histogram of Three-Node Test Results

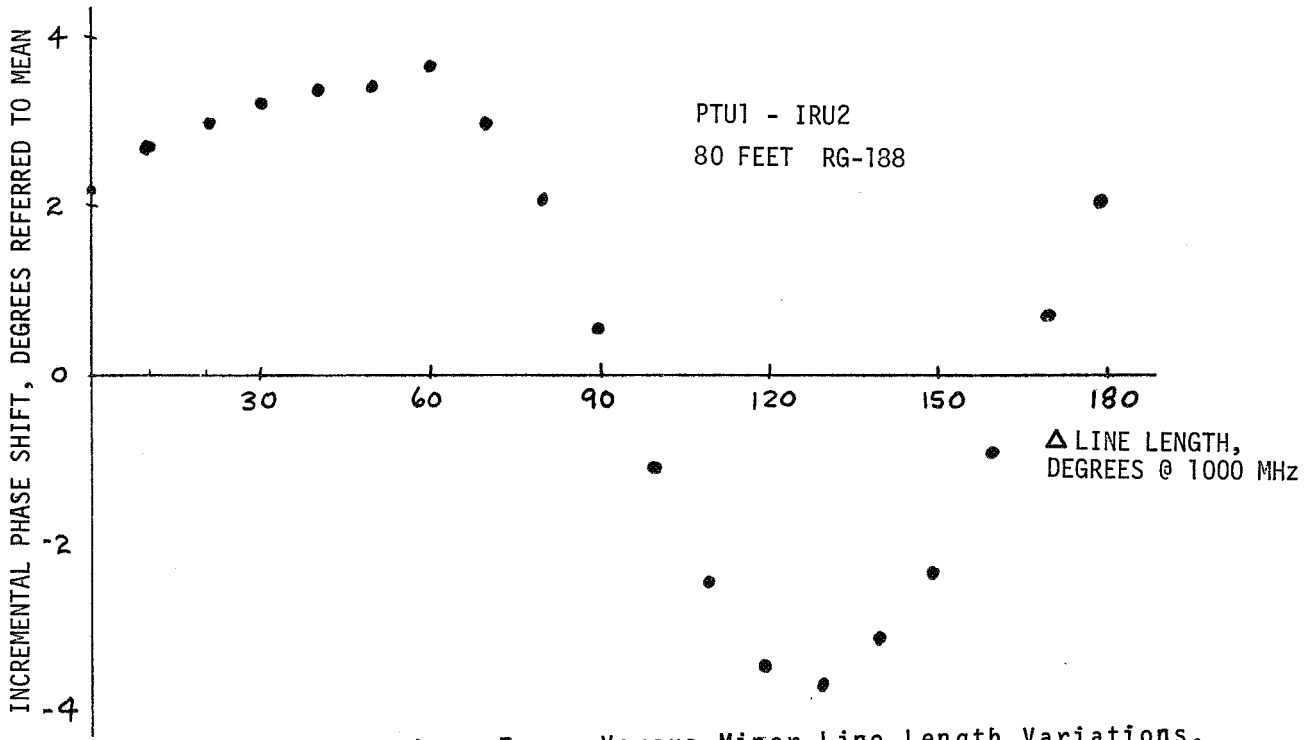

Figure 5. Phase Error Versus Minor Line Length Variations.

2.3 INTERPRETATION OF TEST RESULTS

A detailed report of the MSRTS breadboard test results has been prepared [6]. The conclusions from that report are summarized in the following:

- Satisfactory performance can be obtained using readily available components under closely controlled conditions.
- Commercially available components exhibit non-ideal behavior which is critical to MSRTS performance, e.g. port-to-port isolation of mixers and circulators was not sufficient to prevent extraneous signals which can cause phase errors. These effects can be minimized with compensating networks.

3. CONTINUING DEVELOPMENT

The breadboard MSRTS will be used as part of a larger breadboard system which models the total SPS phase control concept. A pilot transmitter will generate a pseudonoise (PM) code-modulated spread spectrum pilot carrier at 2450 MHz. A central pilot receiver will phaselock to the pilot carrier and provide a reference for the MSRTS. At the final level of the MSRTS tree, each IRU will provide a reference phase signal for a power transponder. Each power transponder will receive the pilot carrier, phase-conjugate, and retransmit. The ESTL breadboard system, shown functionally in a typical test configuration in Figure 6, will consist of the following units.

- One Pilot Transmitter
- One Central Pilot Receiver
- Nine MSRTS Elements
- Two Power Transponders
- One Klystron Power Amplifier

These units can be interconnected in various test configurations. Tests will be performed to evaluate the feasibility of the MSRTS phase control concept and to determine the sensitivity of the phase control system to variations in system parameters. In addition, techniques for suppressing the phase noise of the klystron power amplifier will be investigated.

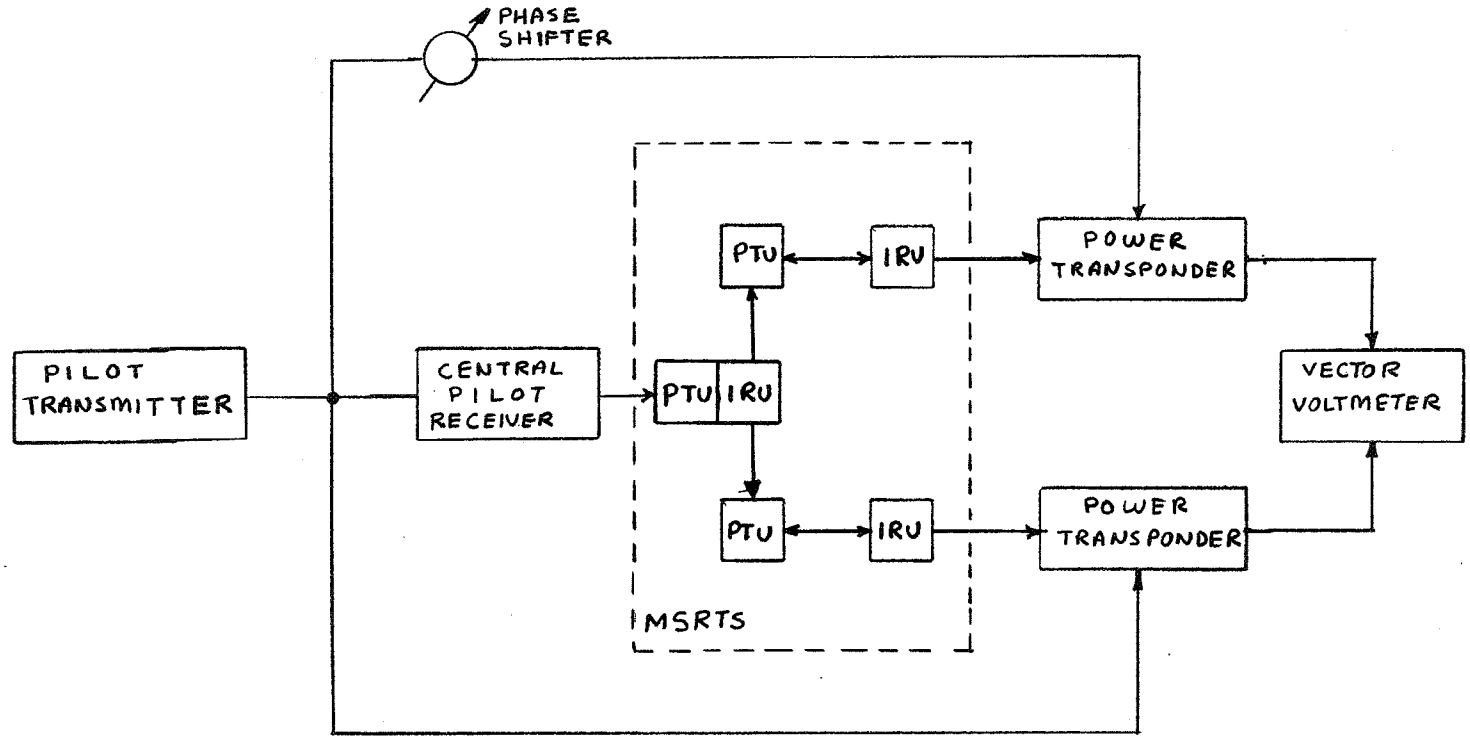

Figure 6. Breadboard SPS Phase Control System in Typical Test Configuration

Design and development of the ESTL breadboard system will be completed by March 1980. The test and evaluation program will be completed by July 1980.

4. ACKNOWLEDGEMENTS

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