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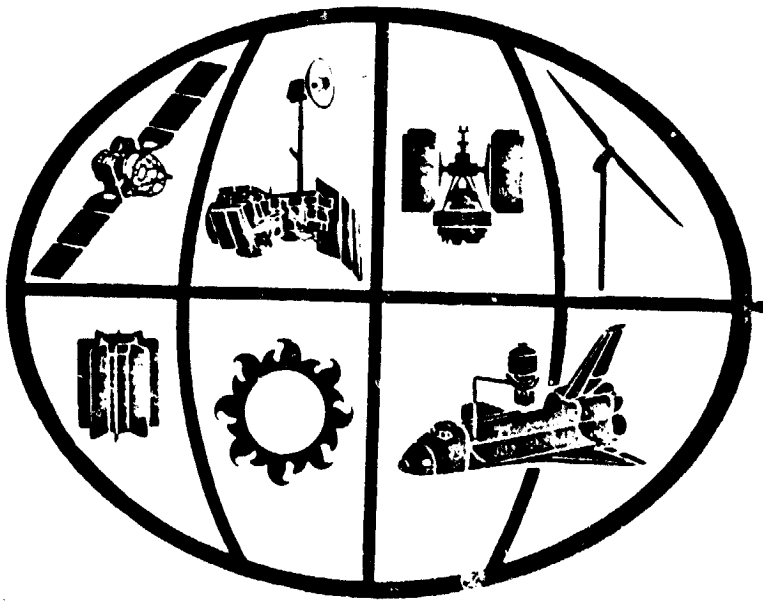
FINAL REPORT

JPL CONTRACT 955785

OCTOBER 27, 1980



space systems division

GENERAL ELECTRIC

INTERNAL ELECTROSTATIC DISCHARGE HAZARD

RISK ASSESSMENT

TO THE

GALILEO ORBITER

FINAL REPORT

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October 27, 1980

JPL Contract 955785

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ABSTRACT

A worst case assessment has been performed on the risk of an internal electrostatic discharge (ESD) on the Command Data System (CDS) multilayer printed circuit board and an output power transformer module in the power subsystem of the Galileo Orbitor.

An estimate of the Jovian environment during the 35 hour orbit insertion was supplied by JPL and used as an input to calculate the electron transport into the Galileo components. A radiation shielding analysis computer code, CHARGE, calculated the electron transport deposition trapped in the anticipated sensitive areas of the multilayer board and transformer module.

Based on these trapped charge calculations electric fields were calculated between the identified isolated areas and the spacecraft ground. These fields were then combined with the characteristic dielectric properties of conductivity and dielectric strength of the materials to assess the risk of an ESD. In most cases, the deposition rate during the 35 hour encounter was neglected and was only included in the analysis of the results where the calculated fields approached the materials dielectric strength.

The results of the assessment of ESD in the CDS multilayer printed circuit board indicate that the probability of ESD in the FR4 is low. The probability of ESD in the components attached to the multilayer board, however, is uncertain based on a lack of prior experimental data. No analysis of any components were performed during this task.

An experiment is recommended using one or two of the CDS prototype multilayer printed circuit boards to assess the risk of ESD in or on the multilayer board components.

The results of the risk assessment of an ESD in the CDS transformer module indicate that if construction of the transformer results in a nominal spacing between the core and the metal posts in the module the probability of ESD after a single orbit is low, but the probability increases as the spacing gets close to 5 mil. This risk can be reduced to zero by the addition of a grounding strap from the core to the spacecraft ground.

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INTRODUCTION

High energy electrons and protons trapped within Jupiter's magnetic fields and incident on the Galileo orbiter during its orbit insertion have the potential of causing interference and possible damage to the spacecraft. The work reported here is a worst case assessment of the risk of an electrostatic discharge (ESD) within the Galileo orbiter due to the accumulation of these energetic particles.

Although the low energy ($\leq$ 40KeV) electron charging process that produces external discharges has received considerable attention over the past five to six years and a significant amount of analytic and experimental data has been generated, a comparable level of understanding of the ESD hazards resulting from the high energy charged particle spectrum has not been achieved.

It was therefore, decided early in the program that a worst case assessment of a limited number of components of special concern would provide the best utilization of resources. This approach was used to most efficiently identify the magnitude of the problem and the need if any, for additional detail. The areas of needed detail were identified as either geometry definition or empirical or material data.

The areas of special concern were identified at the kick off meeting at JPL. The areas were defined according to the current designs, as far as geometry and materials, with support from JPL and GE personnel in the orbiter program. This definition was then used in computer transport calculations at GE to determine the electric charge trapped during the orbit

insertion. The worst case calculations assumed that the performance would be independent of rate or induced conductivity. The experience at GE and Jaycor was then applied to assess the risk of the resulting generated fields leading to internal ESD.

II. TECHNICAL DISCUSSION

2.1 Technical Approach

2.1.1 Task Description

The basic approach of the internal ESD risk assessment was outlined at the kickoff meeting with JPL, GE and Jaycor at JPL. The assessment was defined in seven tasks to track the progress through the effort. These tasks are described below and their interrelation is shown in Figure 1.

Task 1 Identify a limited number (2 - 3) of mission critical or sensitive areas of the spacecraft which in the opinion of the JPL and GE/Jaycor could serve as a first cut or worst case assessment of the potential risks to the Galileo orbiter.

This task will define most probable electron trajectory and the dielectric materials of greatest concern for potential internal ESD to the Galileo Orbiter.

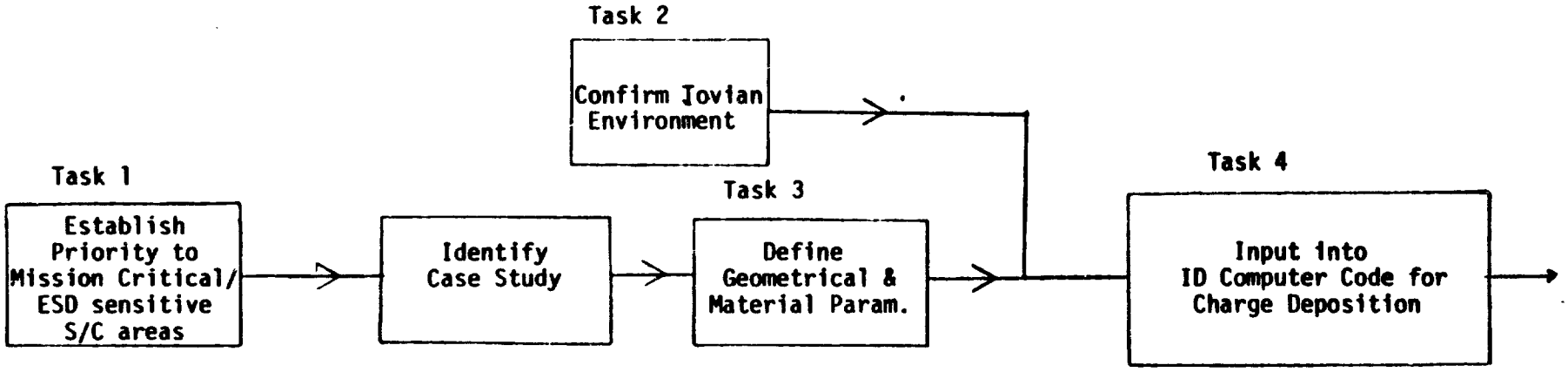
Task 2 Confirm or update the Galileo radiation environment in both energy and temporal dependence to be used as the source of internal charging high energy electrons.

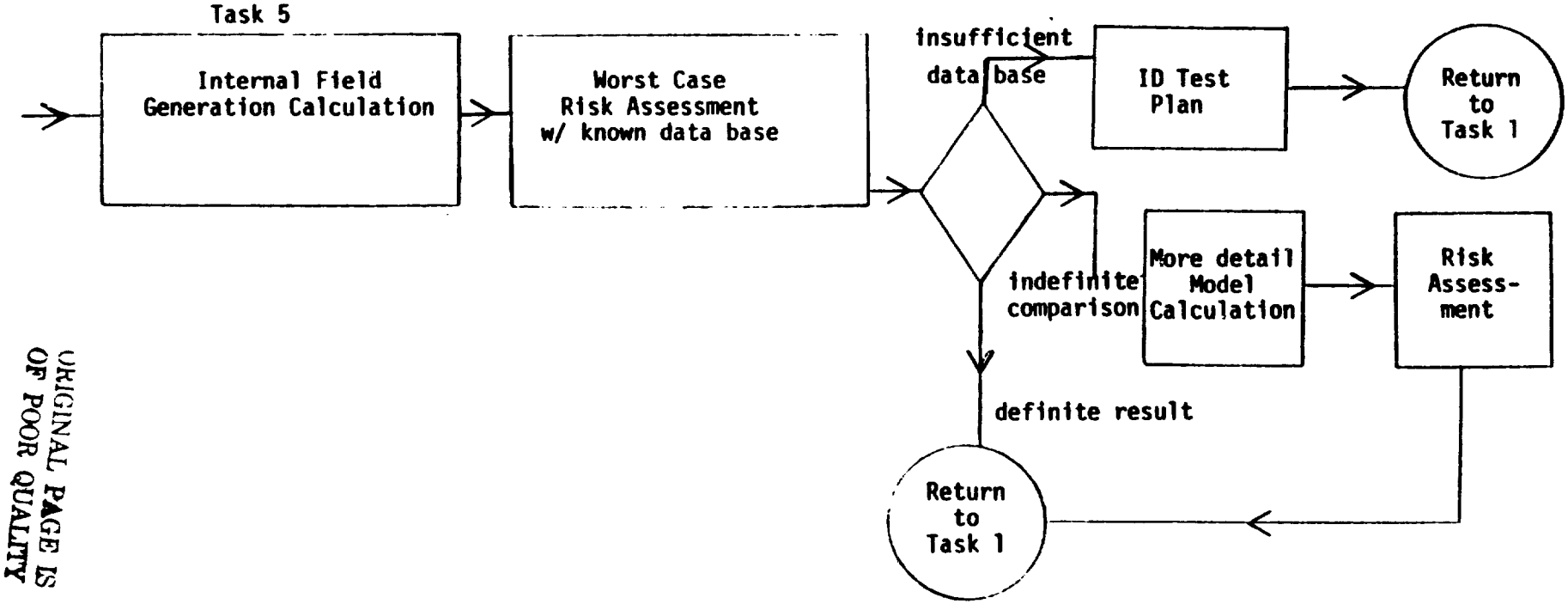
Task 3 Establish a one dimensional geometric shielding and material description for each of the scenarios identified in Task 1. This task will define all the geometries and materials parameters which affect the high energy electrons penetration into the dielectrics defined in Task 1.

Task 4 Results of Task 2 and 3 will be input into the shielding code "Charge" to determine the resultant charge deposition as a function of depth and magnitude.

Task 5 The output of Task 4 will be used to determine the electric fields generated inside the dielectrics and will be compared to the existing materials data and ESD data base.

Task 6 The computer calculations and material properties results of Task 5 will be compared to provide a risk assessment of internal ESD or identify whether additional materials property data is needed or more refined computer calculations.





Task 7 If necessary, as a result of the findings of Task 6, one of three options will be

a) A test plan will be recommended for obtaining required empirical data to complete the risk assessment.

b) A more detailed computer model including radiation induced conductivity effects will be performed on the worst case of Task 6, with a reassessment of the internal ESD risk.

c) An additional case study will be performed following Tasks 1 through 6.

2.1.2 Problem Definition

Discussions held at JPL at the beginning of the program between JPL, GE, and Jaycor personnel were used to identify and prioritize mission critical or sensitive areas. This formed the basis of the Task 1 effort. Based on the initial discussions, the following case studies priorities were established.

- Consider the electron flux to be normally incident to the outboard face of Command Data System Bay 3 with the electron deposition traversing parallel to the face of a typical CDS multilayer board.

- Consider electron trajectory again into a CDS multilayer board except that its approach is oblique to the Bay 3 outboard cover with entrance into the Spun bus section through Bay 4 cover plate.

- Consider electron trajectory into a CDS multilayer board in Bay A or B on the despun platform such that the electron trajectory is normal to the face of the board.

- Consider the electron build-up in the cable insulation between the spun and despun sections.

The cables inside the spun section which sit on the cable rack and interconnect the electronic bays and the slip ring assembly were also identified as an area of concern but was not prioritized.

Additional discussions of prior internal ESD testing performed on the Voyager program and the concerns of possible ESD inside transformer module

in the power subsystem resulted in a reassessment of the priority list. The following list describes the final priority list for internal ESD case studies.

Case 1 The first three areas of initial concern were combined into a single case study of the electron charge deposited in the CDS multilayer board located in Bay A of the despun section where the electron trajectory of most interest would be normal to the print circult board.

Case 2 Consider the electron charge deposited in the core of a transformer in the power circuit in Bay B of the despun section.

Case 3 Consider the electron charge deposited in the cable insulation in the harness bundle between the spun and despun sections.

2.1.3 Environment

From data supplied by Neil Divine of JPL the electron (and proton) flux environment was obtained for $L \leq 16$ ($L \leq 12$) along the proposed Galileo orbit insertion. The flux was for electron and proton energies between 63KeV and 100MeV in logarithmicly spaced energy intervals where $\Delta \log E = 0.2$. Figures 2 and 3 show the temporal dependence of the electron flux (electrons/cm^2 sec) and fluence (electrons/cm^2) for three particular energy levels. As a worse case initial assessment of the hazard from the deposited electron charge, the rate dependence was neglected. The total fluence as a function of energy was used from this Task 2 effort as an input to the charge deposition computer code described in the next section. As part of this code input the total incident charge deposited during the nearly 35 hour encounter was assumed to be deposited in one hour. Table 1 summarizes the total electron fluence (electrons/cm^2) and assumed electron flux and differential electron flux used as input to the computer code CHARGE. Comparison of the assumed electron flux shown in Table 1 assuming all deposition occurs in one hour and the peak electron flux for the

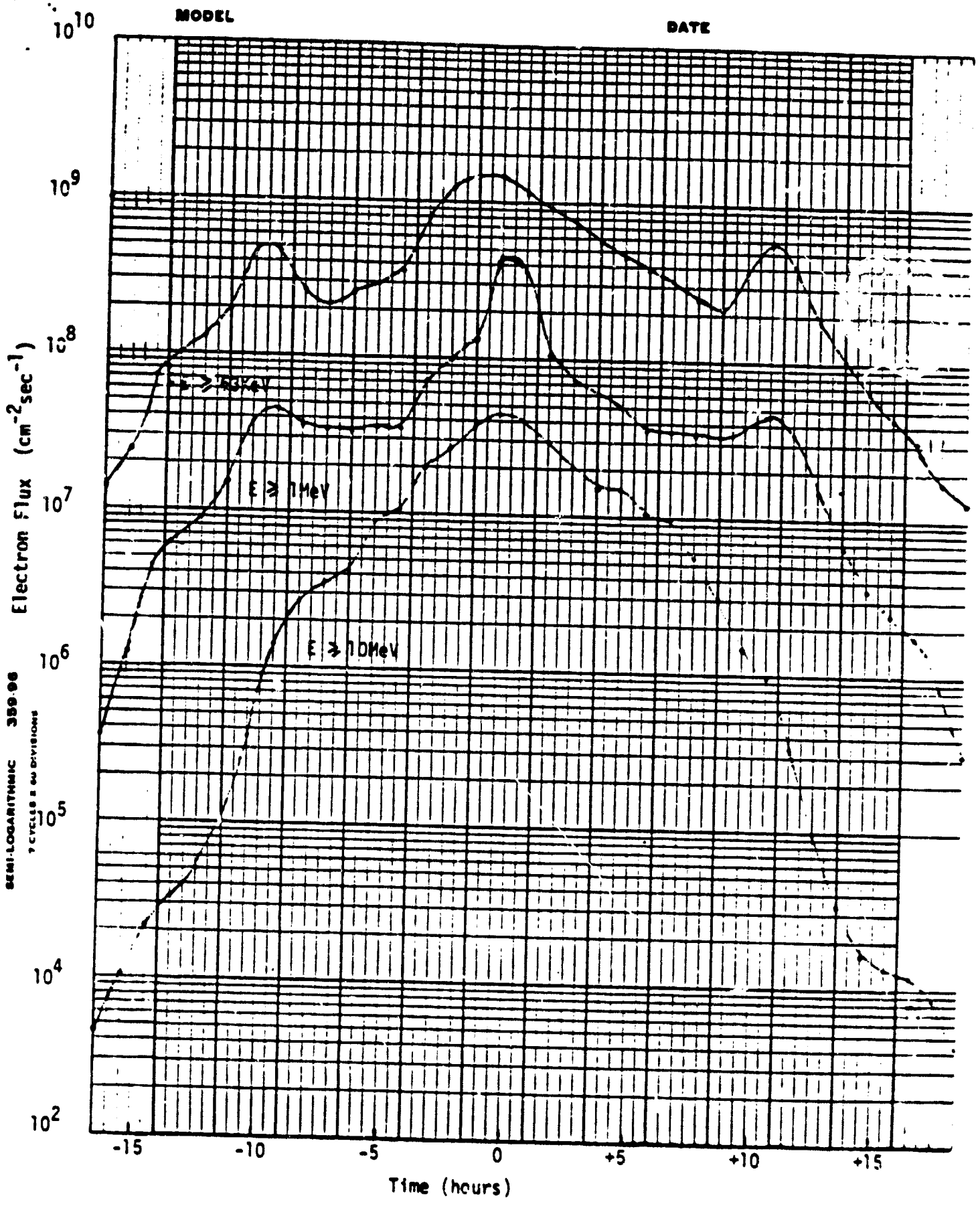


Figure 2

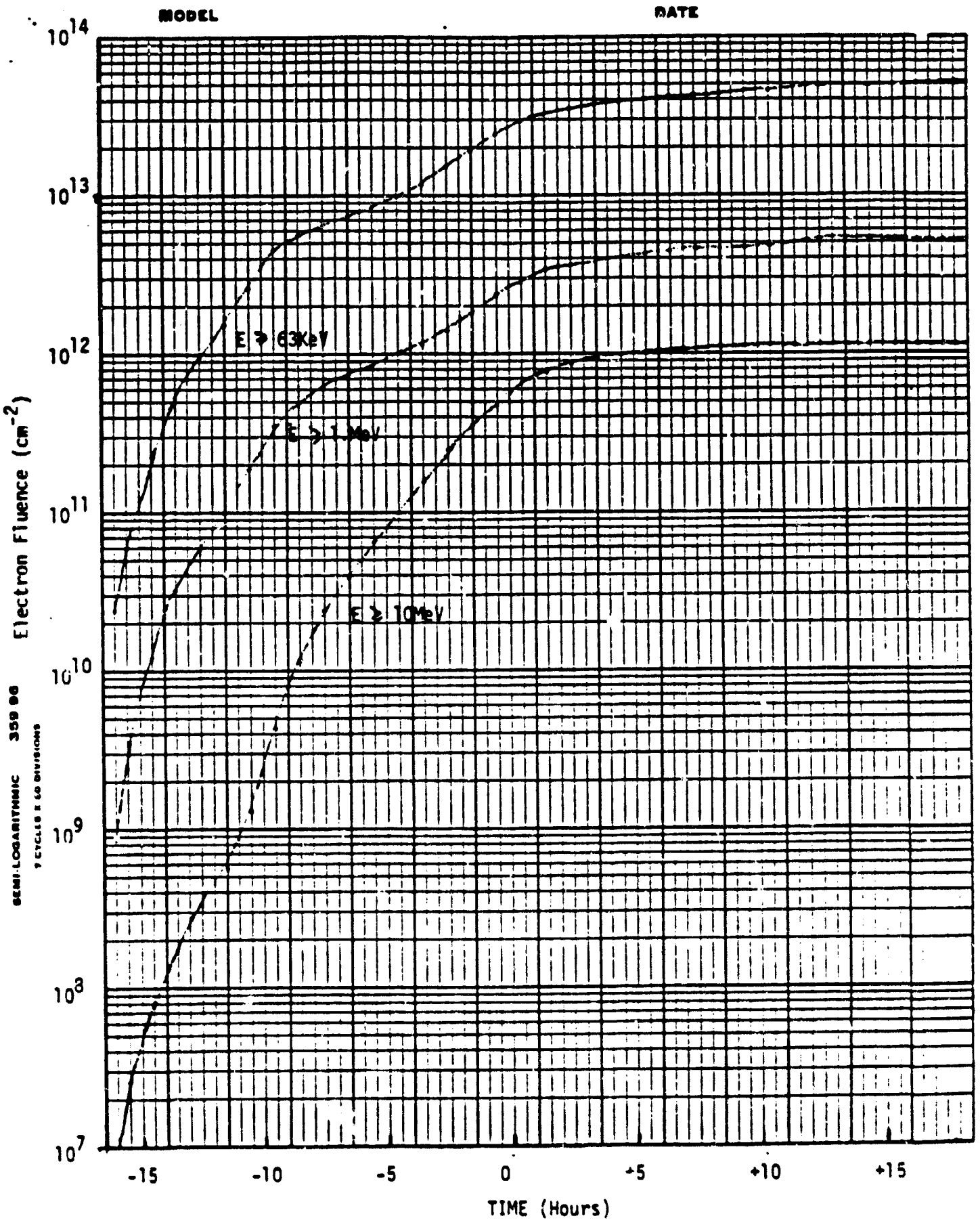

MODEL
RATE
10^{14}
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
E ≥ 63KeV
E ≥ 1 MeV
E ≥ 10MeV
Electron Fluence (cm^{-2})
SEMI-LOGARITHMIC 359 86
7 CYCLES X 50 DIVISIONS
-15
-10
-5
0
+5
+10
+15
TIME (Hours)

Figure 3

TABLE 1

ELECTRON ENVIRONMENT USED IN CHARGE CODE

Energy (E_{MIN}) (MeV)	Fluence (N_E) $N_E > E_{MIN}$ (cm^{-2})	FLUX (J) ($cm^{-2}\ sec^{-1}$)	DIFFERENTIAL ENERGY FLUX (dJ/dE) ($cm^{-2}\ sec^{-1} MeV^{-1}$)
100	1.479 E9	4.108 E5	-6.102 E4
63	8.128 E9	2.258 E6	-1.973 E5
40	4.265 E10	1.184 E7	-1.458 E6
25	1.995 E11	5.542 E7	-6.165 E6
16	5.754 E11	1.598 E8	-1.708 E7
10	1.122 E12	3.117 E8	-3.215 E7
6.3	1.698 E12	4.717 E8	-5.170 E7
4.0	2.239 E12	6.219 E8	-9.411 E7
2.5	2.884 E12	8.011 E8	-1.808 E8
1.6	3.802 E12	1.056 E9	-4.173 E8
1.0	5.138 E12	1.427 E9	-9.381 E8
.63	7.079 E12	1.966 E9	-2.250 E9
.4	1.000 E13	2.777 E9	-5.147 E9
.25	1.412 E13	3.922 E9	-1.260 E10
.16	2.089 E13	5.802 E9	-3.240 E10
.10	3.162 E13	8.783 E9	-8.730 E10
.063	5.138 E13	1.427 E10	-1.371 E11

three energy values plotted in Figure 2 shows that the assumed value is higher than the peak flux by less than a factor of 10.

Figure 4 shows the assumed electron flux given in Table 1 and the differential flux (electrons/cm^2 sec with energies between E_i and E_{i-1}) calculated from Table 1. The differential flux is the difference between fluxes at adjacent energy values. Also shown is the agreement between the calculated ambient differential flux between energy levels and that calculated by the computer based upon the input of the differential energy flux spectrum (dJ/dE) given in Table 1.

2.1.4 Electron Transport Code

The results of Tasks 2 and 3 were used as inputs to the radiation transport code CHARGE. The original intent of CHARGE was the Space Radiation analysis.

The GE Space Division code package is a modification of one developed at Douglas Aircraft Co. in the 1960's.[1] This code package, is reasonably economical in terms of input and computer expense. As one of its outputs the code supplies the incident and exit current densities as a function of energy interval in addition to the total fluence. The differences between these values were used to calculate the charge deposited in a particular layer. The following discussion describes the operation of CHARGE.

The CHARGE code computes response rates and flux spectra behind a multi-layered spherical or planar shield exposed to isotropic fluxes of electrons, protons, and heavy charged particles. The doses or other responses to electron, primary proton, heavy particle, electron Bremsstrahlung secondary proton, and secondary neutron radiations are calculated as a function of penetration into the shield; the materials of each layer may be mixtures of elements contained in the library or supplied by the user. The primary

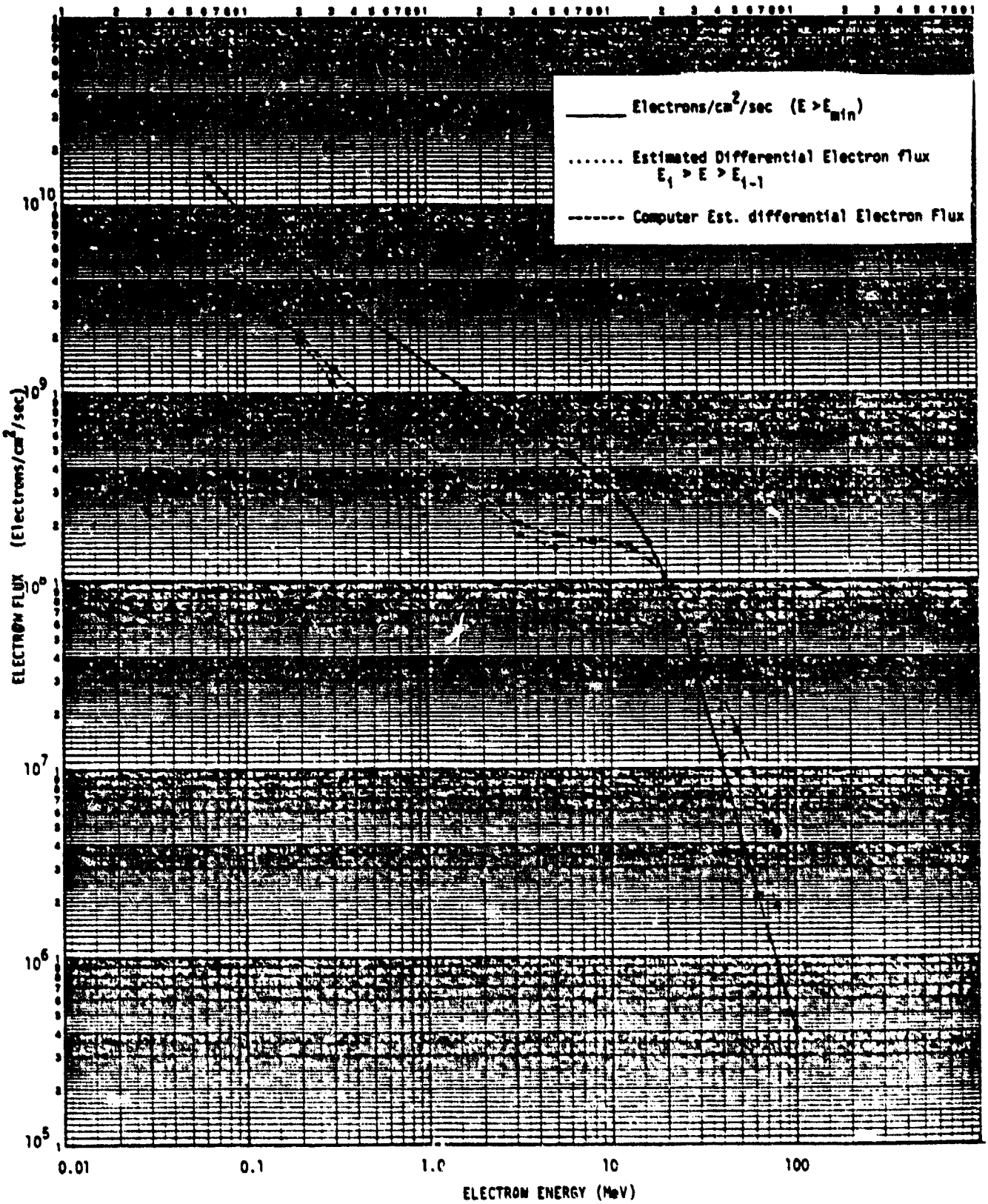


FIGURE 4

results consist of flux responses as a function of penetration.

The ambient electron, proton, and heavy particle spectra may be specified as differential spectra in tabular or functional form. These incident charged particle spectra, which may be viewed as essentially continuous functions of particle kinetic energy, are divided into energy bands or groups, the number and spacing of which are controlled by input data. Each of these groups may be completely described by its upper and lower energy limits and the energy variation of the spectrum within the group.

The variation of the group boundary energies and group spectra as a function of shield penetration uniquely determines charged particle dose rates and secondary particle production rates. Therefore, charged particle shielding calculations reduce to the integration of the equations which express the variation of particle energy with distance in the shield material ("range-energy" equation).

As charged particles penetrate matter, they interact primarily with the orbital electrons of the medium. Incident electrons can undergo quite large deflections in their billiard ball-like collisions with the orbital electrons. In addition to producing electromagnetic radiation (bremsstrahlung X-rays) by the deceleration of these charges, the individual large angle collisions can cause large energy losses and deflections from the original electron path. In order to account for these competing processes, CHARGE uses the basic range-energy relation, normally modified by applying electron transmission factors derived from Monte Carlo calculations. The capability of not using transmission factors is contained, however.

Because of the limited number of materials defined in the computer library and the relative similarity in the elemental breakdown of mylar, Teflon and

solithane, these materials were grouped together under a common description of polyethylene which existed in the code library.

2.2 CDS Multilayer PC Board

2.2.1 Material Definition

The first case studied was the electron charging in the 10 layer multilayer board inside the CDS in Bay A. The trajectory of the electron was defined to be normal to the CDS board. As such, the electron path was defined as passing through a multilayer insulation blanket, the Bay A outboard cover, the board's conformal coating and the multiple layers of the board's dielectric.

The description of the multilayer insulation blanket shown in Figure 5 was supplied by JPL. The description of the outboard cover on Bay A parallel to the PC board was taken from Drwg. No. 10091629, Sheet 2. The construction detail of the multilayer board was taken from JPL Drwg. No. 10064876, Sheet 1 and discussions with JPL during the kickoff meeting. The boards were described to be 10 to 16 layers (typically 10 layers) of FR4 materials with a 20 mil conformal coating of Solithane 113-300. The dielectric spacing is 8 mil between conductor layers. The conductor strip line is 1.4 mil thick and 8 mil wide. The typical lay up is shown in Figure 6. Based upon these descriptions the material profile through which the electron trajectory passes is given in Table 2.

TABLE 2

LAYER NO.	DESCRIPTION	THICKNESS IN. (mm)	
1	Black Paint	0.0015	(0.038)
2	Teflon	0.002	(0.050)
	Mylar	0.001	(0.025)
	15 Layers Mylar (1/4 mil)	0.00375	(0.095)
	Mylar	0.001	(0.025)
3	Tantalum	0.006	(0.152)
4	Aluminum	0.020	(0.508)

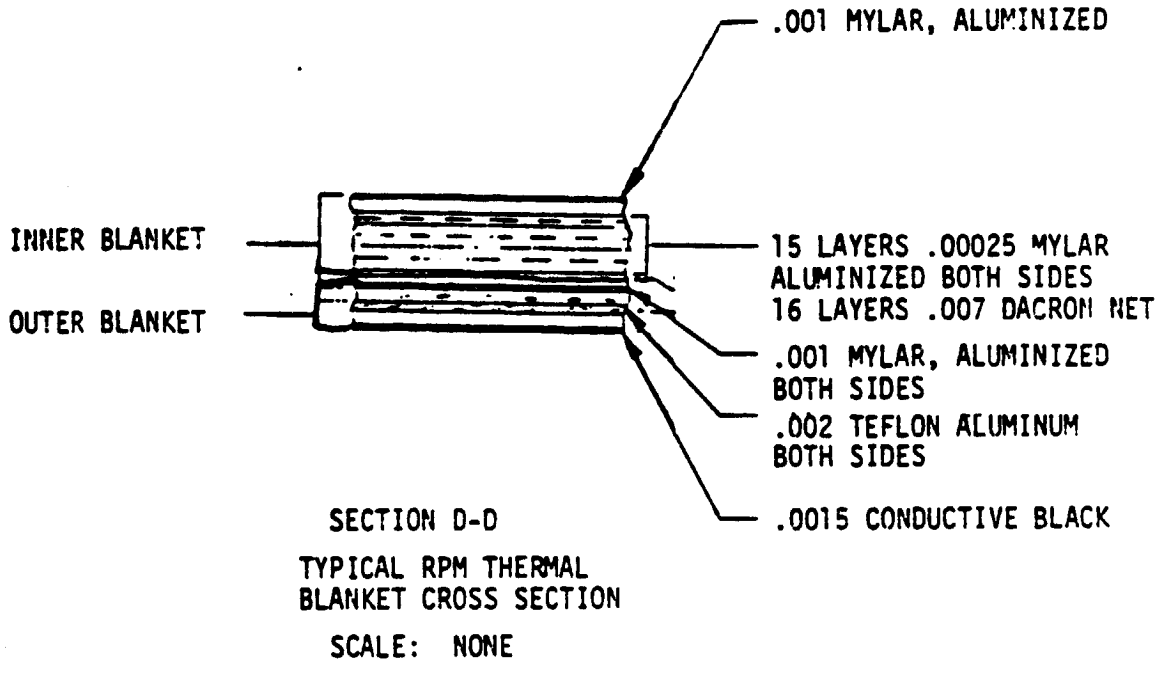


FIGURE 5 THERMAL BLANKET

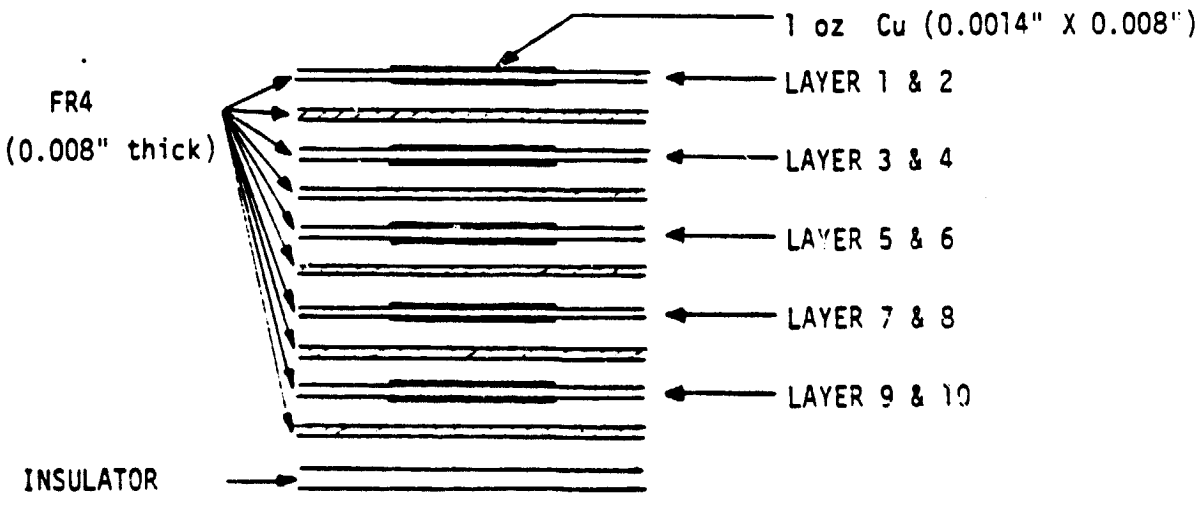


FIGURE 6 MULTILAYER BOARD

LAYER	DESCRIPTION	THICKNESS IN. (mm)
5	Solithane	0.020 (0.508)
6 to 15	FR4	0.008 (0.203)

The vapor deposited aluminum (VDA) on all the teflon and mylar films was neglected in these calculations because of their negligible cross-sectional area for electron capture. The thickness of the tantalum shield was chosen from Drwg. No. 10091629. It is the minimum shield thickness defined over the Bay A cover. The aluminum thickness was assumed to be 0.06 inches but from later discussions with JPL this value may be low by 0.02 inches. Per our discussion with JPL the solithane thickness was assumed to 0.02 inches. The next ten layers were assumed to be FR4 glass epoxy each 0.008 inches thick. The inclusion of a discontinous copper layer about 0.0014 inches thick between layers of FR4 was not included in the analysis because of the lack of a good definition for any "typical" profile of conductor through the board for a given cross section. This analysis allowed a worst case construction assuming a cross section which contained no intermediate ground planes for charge leakage.

The FR4 was described by an elemental breakdown of the largest constituents using Vendor data according to the following table:

TABLE 3

ASSUMED ELEMENTAL COMPOSITION OF FR4

Oxygen	33%
Carbon (+ Nitrogen)	31%
Aluminum (+ Silicon)	19%
Krypton (Bromine)	9%
Calcium	8%

The elements in parentheses were also in the material but were described or combined with the first element because of lack of radiation shield data on these materials. The density of FR4 was assumed to be 1.93g/cc.

2.2.2 Charge Deposition Profile

Since the charge deposition was modeled in a planar geometry the code used one half the isotropic flux given by the dashed line in Figure 4. For each layer described in Table 2 the CHARGE code calculated an incident and exit total fluence and an electron flux as a function of renormalized energy intervals. Figure 7 shows the incident and exit flux as a function of the electron energy for the first FR4 layer. Table 4 sums the total electron fluence incident and penetrating each of the material layers. Differences in these values represent the trapped charge within each metal or dielectric layer assuming no leakage due to its electrical conductivity.

With the exception of the first FR4 layer the charge density is relatively uniform with about 2.6×10^{10} electrons/cm^2 per 8 mils or .2mm of multilayer board. This gives a charge density of 2×10^{-7} Coul/cm^3. The total trapped charge in the 100 mil thick composite board and solithane layer is nearly 3×10^{11} electrons/cm^2.

2.2.3 Internal Field Calculations

The results of the environment transport calculations in terms of the trapped charge density were used by Jaycor as inputs to the PRECHG computer code (See Appendix) to determine the electric fields within the multilayer PC board. Since the electric fields are a function of the relative position and density of the conductors in the multilayer PC board which vary throughout the actual PC board, it was not practical to analyze all configurations that could exist on an operational board. Therefore, two worse case geometrical configurations were assumed, one with a single grounded conductor on the surface of the 10 layered

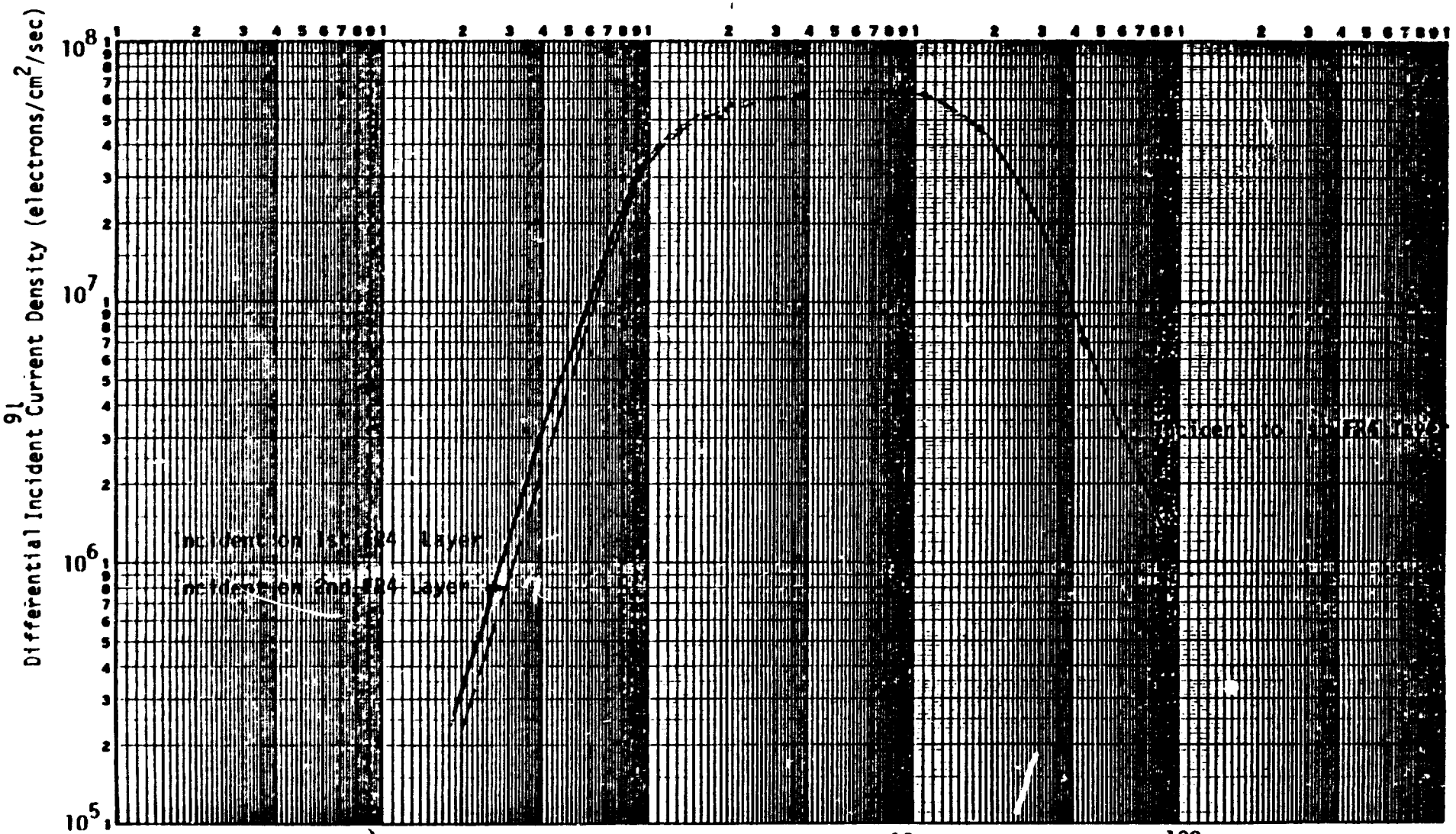


FIGURE 7

TABLE 4

LAYER	DESCRIPTION	INCIDENT ELECTRON DENSITY (e/cm^2)	DEPOSITED CHARGE (e/cm^2)
1	Carbon	2.569 E13	5.857 E12
2	Blanket	1.983 E13	9.943 E12
3	Tantalum	9.889 E12	7.860 E12
4	Al	2.029 E12	6.815 E11
5	Solithane	1.347 E12	4.50 E10
6	FR4	1.302 E12	3.24 E10
7	"	1.270 E12	2.63 E10
8	"	1.244 E12	2.63 E10
9	"	1.217 E12	2.63 E10
10	"	1.191 E12	2.59 E10
11	"	1.165 E12	2.52 E10
12	"	1.140 E12	2.63 E10
13	"	1.114 E12	2.41 E10
14	"	1.089 E12	2.34 E10
15	"	1.066 E12	2.23 E10
16	-	1.044 E12	--

board and one with the grounded conductor buried in the center of the depth of the 10 layer board. Since the electric fields near the conductor strips increase as their separation between conductors increases, a worst case separation of one inch in the plane of the multilayer board was assumed. While this is not representative of the majority of the board, discharges in any portion of the board could couple into other circuit elements on the board. In addition the calculated electric fields can be fairly well scaled linearly as a function of conductor separation and thus the results can be applied to areas with closer spacings.

The configuration was modeled in a toroidal shape as shown in Figure 8, since PRECHG requires an axially symmetric geometry. Figure 8a represents the surface conductor configuration while Figure 8b represents the buried conductor. The width of the dielectric was taken to be equal to one inch, per the above discussion. The radius of the dielectric circle was made large compared to the dielectric width so that the electric fields calculated for these configurations are essentially identical to those that would be calculated if the dielectric "tube" were unfolded into a straight line. The E field on one side of the toroid due to electric charge on the other side is down by a factor of $(r_1/r_2)^2 \approx 0.01$ from the field due to the charge on the same side. The conductor was assumed to be 1.4 mils thick and 10 mils wide which is the anticipated dimensions for the flight boards. The spatial grid for which the fields were computed was on the order of 0.4 mil near the conductor and became progressively larger at distances away from the conductor.

As one would expect, the largest electric fields occurred near the edges of the conductor. Neglecting the conductivity of the FR4, the largest electric field was calculated to be 1.3×10^4 V/mil (5×10^6 V/cm). When the conductor was buried at mid depth in the dielectric and about 4.3×10^4 V/mil (1.7×10^7 V/cm) when the conductor was on the surface. If the corners of the metal strip

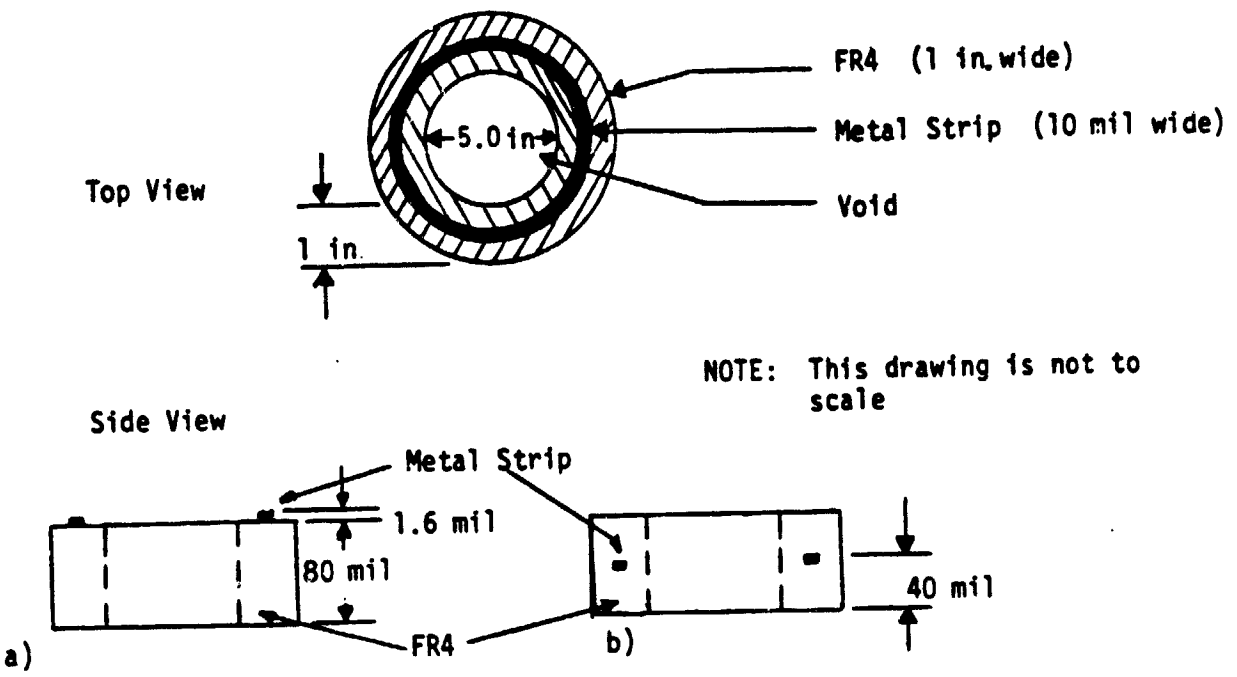


FIGURE 8 TWO CONFIGURATIONS FOR CALCULATION OF E FIELD INSIDE FR4 BOARD

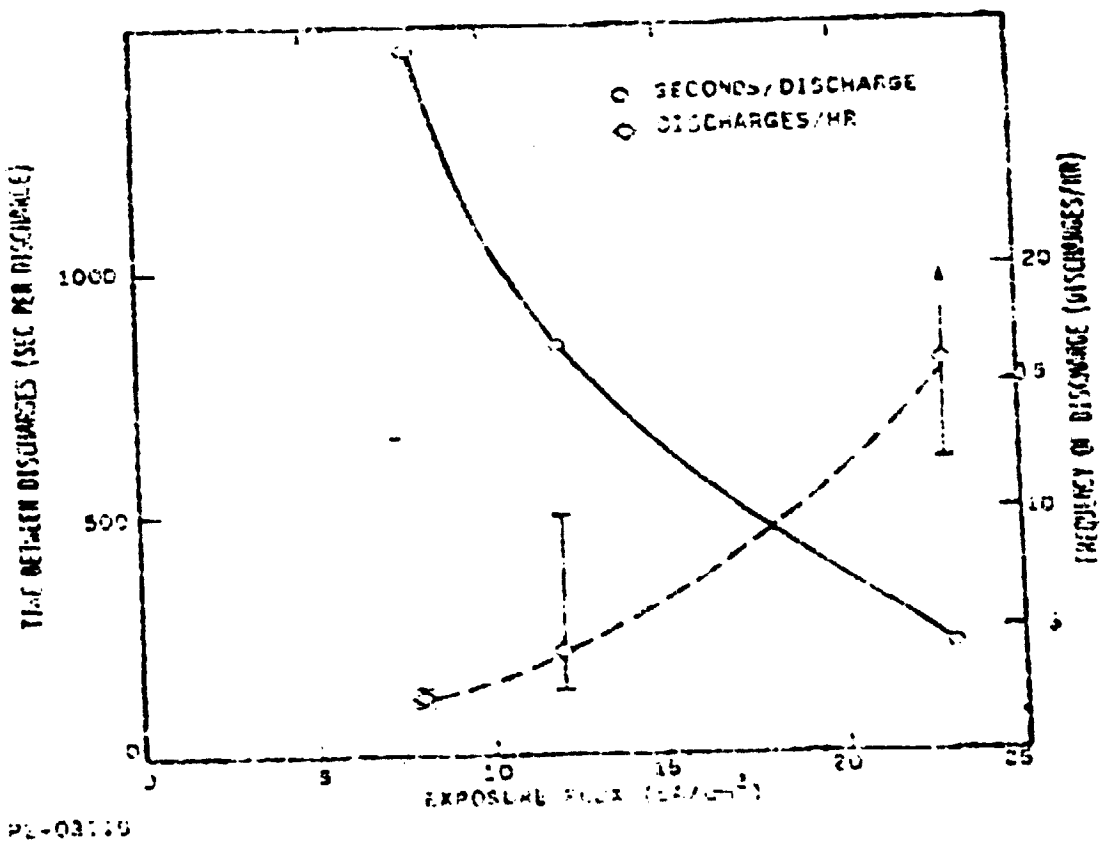


Figure 9 TIME BETWEEN DISCHARGES AND FREQUENCY OF DISCHARGE VS FLUX (MEASUREMENT POINT B ON P.C. BOARD)

were not perfectly sharp as assumed in the code, these two fields would be closer to about 8.9 X 10^3V/mil (3.5 X 10^6V/cm) and 3 X 10^4V/mil (1.2 X 10^7V/cm) respectively, which are approximately the average fields over the surface of the conductor.

When the conductivity of the FR4 is included, a calculation of the conducted current in the plane of the FR4 can be performed and compared to the incident current density. Using an average electric field of 2 X 10^5V/cm, which was calculated assuming no conductivity, and a value of 2 X 10^{-13} $(\Omega\text{-cm})^{-1}$ for the conductivity, one finds that the lateral conducted current is

$$J(A/cm^2) = E(V/m) \cdot \sigma\ [(\Omega\text{-cm})^{-1}];$$
$$= 2 \times 10^5 \cdot 2 \times 10^{-13}$$
$$= 4 \times 10^{-8} A/cm^2$$

To produce this current in the plane of the board, the incident flux normal to the board would have to be 9 X 10^{-9}A/cm^2. This value is roughly 700 times greater than the maximum anticipated incident flux of 13pA/cm^2. Thus with a value for the conductivity of 2 X 10^{-13} $(\Omega\text{-cm})^{-1}$ the maximum fields inside the multilayer board will in reality be roughly 700 times smaller than those calculated with zero conductivity. The maximum fields will then be on the order of 13V/mil. This is close to the value calculated assuming a close packed density of conductors between the layers of FR4 and using the calculated charge density of 2.6 X 10^{-8} electrons/cm^2 in the 8 mil FR4 layer.

2.2.4 Risk Assessment

An assessment of the risk of an ESD occurring in the CDS (Bay A) mulitlayer PC board can be performed in two ways. 1) The results of the environment transport calculations can be used in analytical computer codes to calculate electrical stresses in the multilayer board, and compared to the material electrical stress characterizations. 2) The results of the environment transport calculations in terms of trapped charge in the multilayer PC

board can be compared to existing experimental data on discharges in printed circuit boards. Both approaches are treated here.

Comparison of the calculated rate of charge trapping (the flux of trapped electrons) in the Jovian environment to Figure 9 is one means of assessing the risk of ESD in the multilayer board. From Table 4, roughly 3×10^{11} electrons/cm^2 will be deposited during a 35 hour Jupiter encounter. The deposition time for the calculation was assumed to be one hour, which implies a deposition rate of 8.3×10^7 electrons/cm^2 sec (13pA/cm^2). This flux, however, is artifically high since the 3×10^{11} electrons/cm^2 will be deposited continually during the 35 hour encounter with the Jovian electron environment. The actual flux will be low at initiation of the orbit insertion, will peak near closest encounter and will again decrease as the Galileo moves away from Jupiter. Thus, the majority of the trapped charge will be accumulated during a time between the one hour assumed for calculational purposes and the actual 35 hour encounter time. The value of 8.3×10^7 electrons/cm^2 sec is certainly an upper limit on the flux. A lower limit for assessment of the risk of ESD in the multilayer board should be roughly one-tenth this value or 8.3×10^6 electrons/cm^2 sec (1.3 pA/cm^2). Comparison of these values to Figure 9 indicates that discharges could be expected to occur roughly once every 850 sec (14 minutes) at 8.3×10^7 electrons/cm^2 sec (13pA/cm^2) and once every 17 hours (extrapolated from inverse square fit to the data) at 8.3×10^6 electrons/cm^2 sec (1.3pA/cm^2). Between these two limits based on a comparison of Table 1 and Figure 2 it is anticipated that several discharges could occur during an hour. One the other hand, based upon electron transport calculations and analytical computer code predictions of the electrical stress in the FR4 material the electric fields predicted in the material are very small compared to the dielectric strength of FR4 of roughly 500 volts/mil.

At this time only limited data exists on the charging of internal spacecraft components by high energy, penetrating electrons. The only existing data on the charging of printed circuit boards was obtained by Jaycor during experiments performed for the Air Force Weapons Laboratory (Ref. 2, 3, 4). The energy of the electrons used in these PC boards tests was about 250KeV and resulted in a charge which was distributed throughout the first 33 mils of the PC board. Therefore, these results hold a large significance to the risk assessment.

Briefly stated, the results of these experiments were:

(1) ESD can be induced in or on satellite PC boards by high energy electrons.

(2) During ESD in or on PC boards currents and voltages are often injected into electronic components which are well above those necessary to cause upset in most types of electronic components and sufficiently large in some cases to cause burnout.

(3) Both the magnitude and frequency of the discharges decrease as the flux of incident electrons (rate of charge trapping) decreases. Figure 9 shows the time between discharges (the inverse of the discharge frequency) as a function of incident electron flux. Note that as the electron flux decreases, the time between discharges increases roughly quadratically.

(4) Integrating the incident flux over the time from the start of the electron exposure to the time of the first ESD gives a threshold electron charge layer density for ESD's of 1.5×10^{11} electons/cm^2.

Although the charge calculated for the CDS multilayer PC board in the Jovian environment will be distributed throughout the entire 90 mils of the multilayer board, the resultant electric fields will not differ by more than 10 to 20% from the fields present in the experiments described above where the charge was distributed through only the first 33 mils ($\sim$1/2 the thickness) of the PC board. Thus, a comparison of the calculated charge density in the CDS board to the ESD threshold charge density implied from the experimental data is valid. Comparison of the experimentally determined ESD threshold charge layer density of 1.5×10^{11} electrons/cm^2 to the roughly 3×10^{11} electrons/cm^2

in Table 4, which will be trapped in the solithane/10 layer FR4 PC sandwich is indicative of a high probability of ESD's occurring in or on the CDS multilayer PC board.

In view of the electric field calculations when consideration is given to the relatively high conductivity of FR4, the probability of ESD in the CDS multilayer board itself is very small. The apparent discrepance between the experimental results which indicate that ESD in the test PC board will occur at rates of 13pA/cm^2 and the electric field calculations results for the multilayer FR4 board could be due to one of two things.

> The printed circuit board for which ESD data does exist had a conductivity much lower than that of FR4. The test printed circuit board was fiberglass. Standard varities of printed circuit board fiberglass have conductivities that range from 10^{-13} to 10^{-16} $(\Omega\text{-cm})^{-1}$.
>
> The ESD observed during the printed circuit board tests did not occur in the printed circuit board itself. but in the components on the board. In particular, one could imagine that the ESD occurred in capacitors on the board. This issue has to date not been explored.

The probability of an ESD in the components (possibly capacitors), therefore, should be addressed before drawing a conclusion regarding the probability of an ESD in the CDS electronics.

2.3 Power Transformer Module

2.3.1 Material Definition

The second case studied was the electron transport through the Bay B.

outboard cover and thermal control blanket into a power transformer module. The concern for internal ESD in the transformer module was associated with the electrically floating core. The anticipated thermal control cover of Bay B is a combination of thermal louvers and multilayer insulation (MLI) blanket. The structural support in the Bay B cover required to support the louver and provide other particulate protection was specified as a 192 mil thick wall of aluminum. Therefore, the worst case for electron charging inside Bay B would be to consider an electron trajectory through the MLI blanket similar to the profile used for the multilayer board. For this case the thickness of the aluminum cover was adjusted to 80 mils to reflect the latest information on the shielding description.

As in the previous case the worst case orientation of the transformer module was assumed to be located under the area of the Bay B cover with the minimum of tantalum shielding.

Initial drawings from the Voyager program of the transformer indicated insulation tape between windings. Further discussions with JPL and Jeff Benham of GE about the geometric details of the transformer core and windings resulted in the analyses being redirected to consider the anticipated new design for the Galileo output power transformer. Transformer dimensions and materials were obtained from the preliminary transformer Drwg. No. (GE-47E248720). Figure 10 shows the orientation of transformer core in the encapsulate module.

The electron transport through the MLI blanket and metal cover is similar to Table 2 with layer 4 becoming 80 mils thick. The normal electron path is then through a nominal 2[illegible] mil coating of solithane over the module,

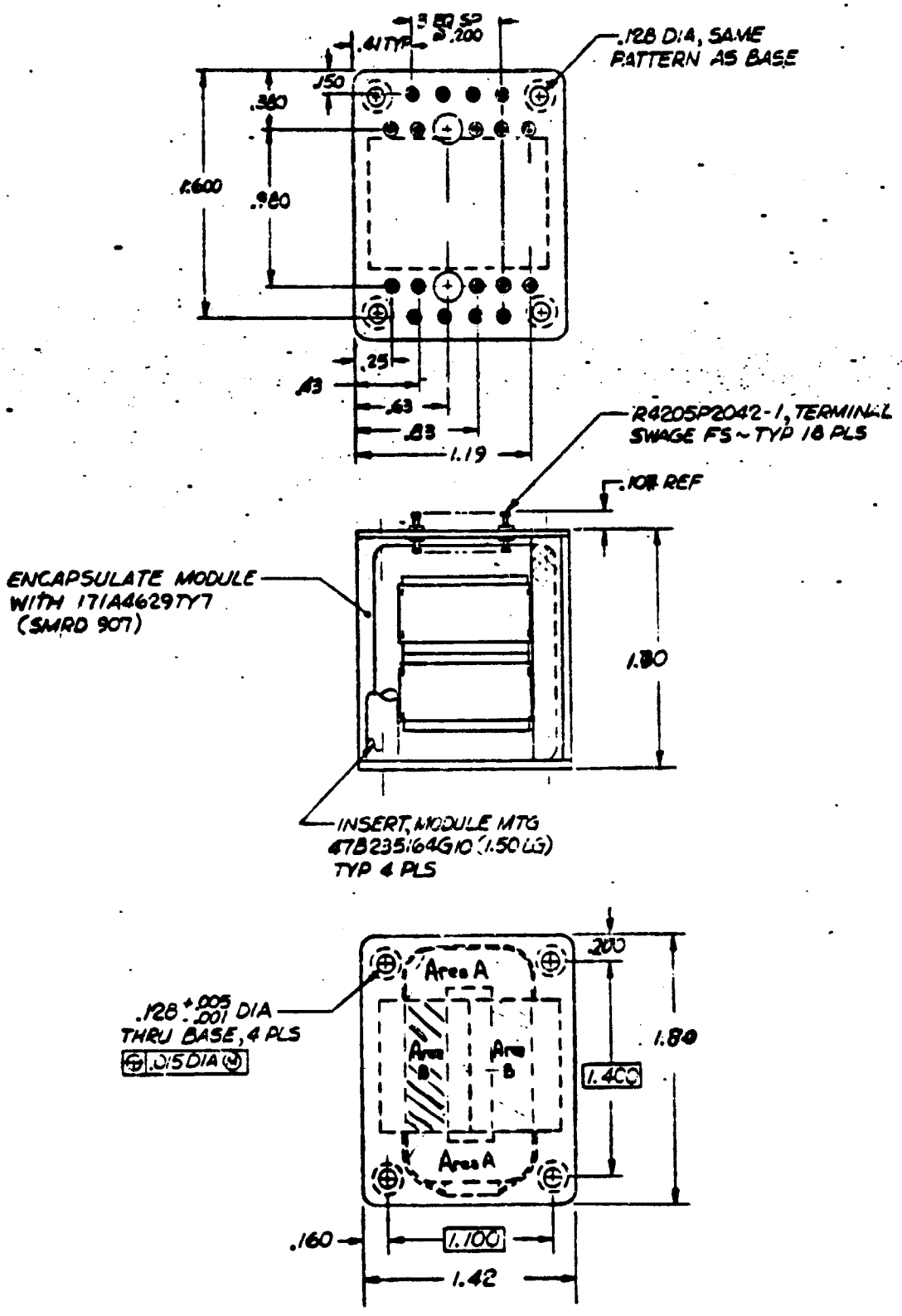


FIGURE 10 POWER TRANSFORMER

through a 31 mil fiberglass mounting board and into the potting compound of solithane or SMRD above the transformer. To calculate the amount of charge trapped in the core, two cases were treated for the electron path to the core. 1) The electrons traversed parallel to the edge of the windings through 287 mils of potting compound between the fiberglass connector plate and the area of the core marked as A in Figure 10. 2) The electrons traversed through 107 mils of potting compound between the fiberglass and the windings, through 11 mils of fibrous tape, through 6 layers of magnetic wire, through 15 mils of paper press board bobbin and into the core. The ratio of these two areas is about 3.08cm^2 (area A) to 2.90cm^2 (area B). These two profiles are described in detail in Table 5.

TABLE 5

LAYER NO.	DESCRIPTION	THICKNESS IN (mm)	
1	Black Paint	0.0015	(0.038)
2	MLI	0.0077	(0.195)
3	Ta	0.006	(0.152)
4	Al	0.080	(2.032)
5	Solithane	0.020	(0.508)
6	FR4	0.031	(0.787)
7	Solithane	0.107	(2.718)
Case 1			
8	Fibermat Tape	0.011	(0.279)
9	6 Layers of Wire	0.154	(3.912)
10	Paper Pressboard	0.015	(0.380)
11	Core	1.000	(25,400)
Case 2			
8	Solithane	0.180	(4.570)
9	Core	1.000	(25.400)

2.3.2 Charge Deposition Profile

Since the charge deposition into the power transformer was modelled in a planar geometry the code used one half of the isotropic flux given in Figure 4 for the incident flux on Bay B. For each layer described in Table 5 the CHARGE code calculated an incident and penetrating total fluence and electron flux as a function of a set of renormalized energy intervals.

Since the current design of the output power transformer in the power subsystem in Bay B of the Galileo orbitor has the core effectively isolated from the spacecraft ground, the analysis concentrated on the charge deposited and trapped in the transformer core. Table 6 sums the total electron fluence incident and penetrating each of the material layers. Differences in these values represent the trapped charge within each metal or dielectic layer assuming no leakage due to electrical conductivity.

2.3.3 Internal Field Calculations

The potential, V, which will develop across the transformer core and the spacecraft is given by $V = \frac{Q}{C}$ where Q is the amount of charge trapped in the conductive core and C is the capacitance between the core and the nearby metal. From Figure 10 it can be seen that the closest metal to the transformer core is the transformer windings and the metal posts which are used to package the transformer. Since the widnings are much closer to the core than the four metal posts and since the surface area projected to the core by the windings is much larger than that projected by the posts, the capacitance of the core to the spacecraft will be dominated by the presence of the windings. This capacitance was approximated by considering each portion of the core covered by windings as a parallel plate capacitor. The capacitance is given by $C = \frac{\epsilon A}{d}$ where d is the spacing between the winding and the core, A is the surface area of the winding and ϵ is the dielectric

TABLE 6

LAYER	DESCRIPTION	INCIDENT ELECTRON DENSITY (e/cm^2)		DEPOSITED CHARGE (e/cm^2)	
		Case 1	Case 2	Case 1	Case 2
1	Carbon Paint	2.569E 13		5.857E 12	
2	Blanket	1.983E 13		9.941E 12	
3	Tantalum	9.889E 12		7.860E 12	
4	Aluminum	2.029E 12		8.15 E 11	
5	Solithane	1.214E 12		3.80 E 10	
6	FR4	1.176E 12		1.07 E 11	
7	Potting	1.069E 12		1.68711	1.557E 11
8	Winding	9.003E 11		1.375E 11	
	Potting		9.133E 11		
9	Insulation	7.628E 11		2.100E 9	
10	Winding	7.607E 11		5.540E 11	
11	Pressboard	2.067E 11		2.500E 9	
12	Core	2.042E 11	7.452E 11	2.039E 11	7.440E 11
13	--	2.803E 8	1.194E 9	--	--

constant of the paper pressboard and wire insulation between the core and the winding. Using the dimensions shown in Figure 10, the capacitance was calculated to be 2.6×10^{-10}f, assuming a value of 4 for the dielectric constant of the pressboard/wire insulation combination. The relative dielectric constant for most cellulose based compounds ranges from 2 to 6 at 1MHz. From the results of the environment transport calculations in Table 6, 4.6×10^{-7} Coul are anticipated to be trapped in the core during one 35 hour encounter with the Jovian electron environment. Ignoring the conductivity, the potential which will develop between the core and the windings will be

$$\frac{4.6 \times 10^{-7} \text{ coul}}{2.6 \times 10^{-10} \text{ f}}$$

$$= 1{,}769\text{V}$$

The electric field across the pressboard/wire insulation (total thickness 17 miles) will be

$$\frac{1{,}769}{17}$$

$$= 104\text{V/mil}$$

Subsequent encounters with the Jovian electron environment will possibly increase the electric field if no conductivity is assumed for the dielectric between the core and winding. However, at this point, one must consider conductivity effects since the time between consecutive orbits will be greater than 35 hours. If a conductivity of 10^{-15} $(\Omega\text{cm})^{-1}$ is assumed, the leakage current after a single orbit using a maximum field of 100V/mil, can be calculated to be

$$I = E \cdot \sigma \cdot A$$

$$= 4 \times 10^{-10} A$$

Since this value is roughly 3 times larger than the anticipated peak current stopped in the core of 1.3×10^{-10} amperes, the peak fields will be reduced

by the conductivity by at least a factor of three, i.e. the fields resulting from a single encounter will be on the order of 30V/mil. The effects on the electric field of multiple orbits can be assessed by calculating a dielectric relaxation time which is give by

$$\tau = \epsilon / \sigma$$

$$= 308 \text{ sec}$$

Since this relaxation time is very short compared to the times between encounters with the intense electron fluxes ($\geq$ 35 hours) the effect of multiple encounters will be negligible.

Recognize however, that if the conductivity were on the order of $10^{-16}(\Omega\text{cm})^{-1}$ then the peak fields would be on the order of that calculated assuming no conductivity. This point is significant because the value of $10^{-15}(\Omega\text{ cm})^{-1}$ is representative of this type of material, however the physical construction of the tranformer may result in the actual conductivity between the core and the windings being lower due to poor surface contact, etc.

Additionally, the possibility of the flight geometry varying from that shown in Figure 10 must be considered. In particular, if the transformer core is not positioned symmetrically with respect to the four metal posts and is closer to one post than to the others, the capacitance of the core to the spacecraft will be altered as will the spacing across which the core potential will have to be stood off. From Figure 10 the nominal spacing between the core and the metal post was calculated as 37 mils. The capacitance of the post to the core can be calculated as the capacitance of a wire above a ground plane which is given by

$$C = \frac{2\pi L \epsilon}{\ln\left(\frac{h}{a} + \sqrt{\frac{h}{a}^2 - 1}\right)}$$

where L is the length of the wire, h is the height of the center of the wire above the ground plane and a is the radius of the wire. If it is assumed that the core is packaged such that one post is only 5 mils from the core, then the capacitance of the core to the post can be calculated to be

$$1.6 \times 10^{-11} \quad f$$

assuming a relative dielectric constant of 3.5. Since this is much smaller than the capacitance of the core to the windings, the capacitance of the core to the spacecraft is still dominated by the capacitance of the core to the windings. The potential which develops between the core and the spacecraft will have to be stood off by only 5 mils of the potting epoxy which corresponds to an electric field of 340V/mil. Consideration of the effect of the conductivity of the pressboard could possibly reduce this field by a factor of 3 as discussed above, thus the electric field may be only 113V/mil; however the same consideration discussed above regarding the accuracy with which the conductivity of the pressboard is known must be kept in mind.

2.3.4 Risk Assessment

The dielectric strength of most acetate-based materials ranges from 200 to 600V/mil. Thus it appears that the risk of ESD due to charge trapped in a transformer core on one encounter with the Jovian electron environment is relatively small, since the field across the pressboard will be only about 30 to 100V/mil.

In the case of an assymmetrical placement of the core in the transformer module where the core is close to one of the metal posts as discussed in the previous section, the potential which develops between the core and the spacecraft will now have to be stood off by 5 mils of the potting epoxy which corresponds to an electric field of 113 to 340V/mil depending upon the conductivity value assumed. The dielectric strength of common epoxies is

between 350 to 500V/mil. Thus, if the fabrication control specifications are such that the core can conceivably be within 5 mils of the mounting post, there is a risk of ESD's occurring from the transformer core to the metal posts during a single encounter. Although such an arc will not involve direct current injection into the transformer windings, the arc will couple a current into the windings. If the 1769 V potential is reduced to zero, i.e. 100% of the charge trapped in the core arcs to the metal post, the current induced in the windings can be calculated by

$$I = C_W \frac{dV}{dt}$$

If it is assumed that the arc has a risetime of 10nsec

$$I = 2.6 \times 10^{-10} \cdot \frac{1769}{10^{-8}}$$

$$= 46 \text{ A}$$

In summary, if the transformer is fabricated as indicated in Figure 10, the probability of an ESD during a single encounter with the Jovian electron environment is relatively low. If the configuration control on fabrication of the transformers is such that the core may be positioned within several mils of the metal posts, the probability of an ESD is significantly increased. If a path for draining the charge trapped in the transformer core to the spacecraft ground were provided, the risk of ESD from the transformer core would be effectively reduced to zero.

3.0 CONCLUSIONS AND RECOMMENDATIONS

A worst case risk assessment has been performed on the hazard of an internal ESD on a CDS multilayer printed circuit board and an output power transformer core in the power subsystem of the Galileo Orbiter.

An estimate of the Jovian environment during the 35 hour orbit insertion was supplied by JPL and used as an input to calculate the electron transport into the Galileo components. A radiation shielding analysis computer code, CHARGE calculated the electron transport deposition trapped in the anticipated sensitive areas of the multilayer board and transformer module.

Based on these trapped charge calculations electric fields were calculated between the identified isolated areas and the spacecraft ground. These fields were then combined with the characteristic dielectric properties of conductivity and dielectric strength of the materials to assess the risk of ESD. In most cases, the deposition rate during the 35 hour encounter was neglected and was qualitatively included in the analysis of the results where the calculated fields approached the materials dielectric strength.

3.1 Multilayer Board

The results of the risk assessment of ESD in the CDS multilayer printed circuit board indicate that

1. The probability of ESD in the FR4 is low
2. The probability of ESD in the components attached to the multilayer board is uncertain.

Since the existing experimental data on printed circuit board ESD does not distinguish between ESD in the printed circuit board or in the components on the board and since the data does indicate that potentially damaging ESD did occur either in or on the printed circuit board, the risk of ESD in the Galileo CDS multilayer printed circuit board components should be examined further. Two methods of addressing this issue are by analysis and by experiment. An analysis could make use of the previously performed environment transport calculations to calculate the electric fields inside selected components. An experiment would require exposure in a vacuum of a represent-

ative multilayer printed circuit board to high energy electrons (200 - 300KeV and possibly higher) at realistic fluxes, with measurements of ESD currents and voltages at select locations. Both approaches have advantages and disadvantages. An analysis is in general less expensive, but however, the results are generally limited to the availability of accurate materials property data. An experiment is in general more costly, however, the results are generally more conclusive and convincing.

The recommended approach is to perform an experiment using one or two of the CDS prototype multilayer printed circuit boards. The experiment should be relatively straightforward and could possibly be performed using an electron source available at the Jet Propulsion Laboratory.

3.2 Power Transformer Module

The results of the risk assessment of ESD in the CDS transformer cores indicate that

1. If quality control on construction of the transformers results in a nominal spacing between the core and the metal posts on the order of 37 mil, the probability of ESD during a single encounter with Jovian electron environment is low.
2. If quality control on construction of the transformer is such that the spacing between the transformer core and the metal posts may be as small as 5 mils, the probability of ESD during a single encounter is significantly increased.
3. An ESD in the transformer could result in coupled currents in the transformer on the order of 46A with pulse widths on the order of 20ns. If the injection of currents on the order of 46A for times on the order of 20ns into the transformer windings are judged to be potentially deleterious to the functioning of the Galileo spacecraft, the probability of ESD due to charged trapped in the transformer core can be reduced to zero by the addition of a grounding strap from the core to the spacecraft ground. Since the highest rate at which charge will be trapped in the core corresponds to a

current somewhat less than 130pA, the grounding strap could be extremely light weight. On the basis of the results of the risk assessment, the addition of such a grounding strap is recommended, if ESD induced currents in the transformer winding on the order of 46A are judged potentially hazardous to mission performance.

4. The primary uncertainties in this risk assessment result from a lack of dielectric properties data and a firm knowledge of the transformer tolerances.

REFERENCES

1. Charge Code for Space Radiation Shielding Analysis, W. R. Yucker and J. R. Lilley, DAC-62231, April, 1969.

2. E. P. Wanaas et al., "High Energy Electron Induced Discharges in Printed Circuit Boards," JAYCOR Report to Computer Sciences Corporation, JAYCOR #200-79-140/2073, May 1979

3. E. P. Wenses, et al., "High Energy Electron Induced Discharges in Printed Circuit Boards," IEEE Trans. Nucl. Sci., NS-26, No. 6, December 1979.

4. M. J. Treadaway, et al., "High Energy Electron Induced Discharges in Printed Cirucit Boards at Realistic Fluxes." JAYCOR Report to computer Sciences Corporation, JAYCOR #200-80/234/3176, July 1980.

APPENDIX

THE PRECHG CODE

The PRECHG CODE was developed in 1978 by JAYCOR as an analytical tool for the calculation of electric field distributions around cylindrically symmetric charged bodies consisting of conductors and/or dielectrics. The PRECHG code is essentially a Poisson-solver which computes the steady state electric fields on a finite-difference mesh grid inside a cylindrical, conducting can due to a cylindrically-symmertic distribution of charge on dielectric or conducting bodies inside the can. The outer conducting can can represent either a real outer conductor or a boundary at inifnity if the can dimensions are made large compared to the internal bodies. The charge distribution can either be fixed in space, as in a dielectric, or it can reside in internal conducting bodies or in the conducting can walls. The charge in any conductor is automatically adjusted by the code over the surface of the conducting object to make the surface equipotential. The total net charge inside the can is always zero. In other words, if electrons are trapped in a dielectric or a conducting body, there is an identical amount of positive image charge somewhere else inside the can.

A calculation with the PRECHG code is started by specifying an initial distribution of electric fields (E) along some, or all, of the mesh grid lines inside the conducting can. This distribution of electric flux lines specifies the charge distribution of the problem. A positive and negative amount of charge ($\pm \Delta Q$) is assumed to be located at the two ends of the flux line. The magnitude of each ΔQ is the integral of the flux over the cross sectional area (ΔA) that is associated with the flux line.

$$\Delta Q = E\varepsilon \Delta A,$$

where ε is the permittivity of the medium in which the flux line exists. If one end of the flux line starts at a conductor, ΔQ is part of the total charge on that conductor. If the end of a flux line is not on a conductor, that ΔQ is assumed to be fixed at the position in space.

This initial distribution of flux lines is somewhat arbitrary because there is an infinite number of distributions that could be chosen to produce the desired charge distribution. In principle, any flux distribution that is consistent with the desired charge distribution could be used but usually the simplest arrangement is chosen. This distribution of flux lines satisfies conservation of charge (and electric flux) but it normally will not satify $\nabla \times E = C$, which is necessary condition for satisfying Poisson's equation. The primary computational process in the PRECHG code is an iteration of the magnitudes of $\nabla \times E$ at every mesh point inside the conducting can in such a way that $\nabla \times E$ tends toward zero everywhere while conserving charge at each mesh station and in each conducting body. The iteration process is terminated when the largest magnitude of $\nabla \times E$ at any place in the volume is below some preselected value or when the values of E are no longer changing significantly with successive iterations. This final distribution of E is the solution of Poisson's equation for the chosen distribution of charge, within the accuracy of iterating $\nabla \times E$ to zero.

The validity of the PRECHG CODE has been checked numerous times by comparison of the results of calculations with simple geometrics that can be solved in closed form and by comparison to the results of other analytical computer codes such as the Arbitrary Body of Revolution Code (ABORC) which themselves have been previously verified.