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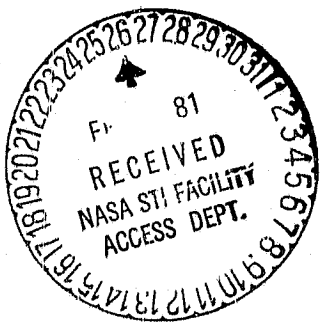
AUTOMATED ARRAY ASSEMBLY TASK DEVELOPMENT OF LOW-COST POLYSILICON SOLAR CELLS

Final Report
November, 1980

JPL Contract No. 955265



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2414 West 14th Street
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Final Report
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Gregory T. Jones

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Photowatt International, Inc.
2414 West 14th Street
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The JPL Low-Cost Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

PREFACE

The information presented in this final report on the Development of Low-Cost Polysilicon Solar Cells represents the work performed from January 1979 through June 1980 by Sensor Technology, Inc. in Chatsworth, California and Photowatt International, Inc., in Tempe, Arizona. This program was directed by Sang S. Rhee and Gregory T. Jones. Principal investigator was Gregory T. Jones. Contributors included Kimberly L. Allison, Sang S. Rhee, Sanjeev Chitre and Priscilla Marlowe.

The JPL Technical Program Manager was Dale Burger.

ABSTRACT

Development of low-cost, large area polysilicon solar cells was conducted in this program. Three types of polysilicon material were investigated. Included in the study was the Wacker cast polysilicon, Crystal Systems HEM material, and Exotic Materials FAST-CZ polysilicon.

The influence of crystal grains on solar cell efficiency was studied. A theoretical and experimental comparison between single crystal silicon and polysilicon solar cell efficiency was performed. Significant electrical performance differences were observed between types of wafer material, i.e. fine grain and coarse grain polysilicon and single crystal silicon. Efficiency degradation due to grain boundaries in fine grain and coarse grain polysilicon was shown to be small.

The feasibility of applying an anisotropic sodium hydroxide etching process to polysilicon wafers was investigated. The texture etching rate, time and solution concentration were evaluated.

Several optional low-cost solar cell processes were investigated. They included $POCl_3$ gettering, spray-on n^+ polymer dopants, and printed aluminum. It was demonstrated that 10% efficient polysilicon solar cells can be produced with spray-on n^+ dopants. This result fulfills an important goal of this project, which is the production of batch quantity of 10% efficient polysilicon solar cells.

TABLE OF CONTENTS

Section	Title	Page No.
1.0	INTRODUCTION	1
2.0	POLYSILICON MATERIAL DESCRIPTION . . .	3
	2.1 Wacker Material	3
	2.2 Crystal Systems Material. . . .	6
	2.3 Exotic Materials Material . . .	9
3.0	INITIAL PROCESS STUDIES.	11
4.0	INFLUENCE OF CRYSTAL GRAINS ON SOLAR CELL EFFICIENCY.	14
	4.1 Theoretical Comparison between Polysilicon and Single Crystal Silicon Solar Cell Efficiency .	14
	4.2 Experimental Comparison between Polysilicon and Single Crystal Silicon Solar Cell Efficiency .	15
5.0	GRIDLINE PATTERN DESIGN CONSIDERATIONS	20
	5.1 Generalized Equation for Computing Fractional Power Loss. .	21
	5.2 Gridline Spacing Sensitivity Analysis.	25
	5.2.1 Crystal Grain Size Distribution.	25
	5.2.2 Gridline Spacing for Minimal Fractional Power Loss	25
	5.2.3 Gridline Spacing for Significant Fractional Power Loss. .	28
	5.3 Experimental Data and Results .	30
6.0	WAFER SURFACE TEXTURIZING PROCESS. . .	35
	6.1 Basic Wafer Surface Texturizing Process	35
	6.2 Surface Characteristics of Texture Etched and Texturized Polysilicon Wafers.	50
	6.3 Optimized Texturizing Process .	54

TABLE OF CONTENTS

Section	Title	Page No.
7.0	DIFFUSION PROCESS CONSIDERATIONS . .	56
8.0	OTHER PROCESS EFFECTS.	59
	8.1 $POCl_3$ Gettering Study	59
	8.1.1 Pregettering Effects.	59
	8.1.2 Intermediate Gettering Effects	61
	8.2 Spray-on Dopant Junction Formation.	66
	8.3 Printed and Evaporated Aluminum Effects on $POCl_3$ Diffused Polysilicon and Single Crystal Silicon Solar Cells	69
	8.4 Printed and Evaporated Aluminum Effects on Spray-on n^+ Doped Polysilicon and Single Crystal Silicon Solar Cells	70
9.0	SELECTED PROCESS AND RESULTS	75
10.0	PROCESS/EQUIPMENT COST ANALYSIS. . .	85
	10.1 Description of the Industry. .	85
	10.2 Company Description.	87
	10.3 Price Computation.	90
	10.4 Discussion of Results.	92
11.0	CONCLUSIONS	93
12.0	RECOMMENDATIONS.	97
13.0	REFERENCES	99

LIST OF FIGURES

Figure No.	Title	Page No.
2.1	Picture of Wacker Coarse Grain Polysilicon Material with Metallization Pattern.	4
2.2	Picture of Crystal System HEM Material with 100% Single Crystallinity with Metallization Pattern.	7
2.3	Picture of Crystal Systems HEM Material with 44% Single Crystallinity and with Metallization Pattern	8
2.4	Picture of Exotic Materials Coarse Grain Polysilicon Material with Metallization Pattern.	10
3.1	Block Diagram of the Standard Polysilicon Solar Cell Processing Sequence . .	12
4.1	Electrical Performance Curves for Isotropic Surface Etched Wacker Polysilicon and Single Crystal Silicon Solar Cells.	17
5.1	A Depiction of the Three Regions between Two Parallel Gridlines where the Midpoint of the i^{th} Crystal Grain may be Located within a Distance of x = 0 to x = s.	22
5.2	Gridline Pattern for Wacker Polysilicon Solar Cells.	27
6.1	Silicon Texture Etching in 20% $NaOH/H_2O$ with 1.0 Minute Cold Water Rinse . . .	39
6.2	Silicon Texture Etching in 20% $NaOH/H_2O$ with 1.0 Minute Hot Water (80°C) Rinse	42
6.3	Silicon Texture Etching in 10% $NaOH/H_2O$	45
6.4	Silicon Texture Etching in 20% $NaOH/H_2O$ followed by Texturizing in 2% $NaOH/H_2O$.	48

LIST OF FIGURES

Figure No.	Title	Page No.
6.5	Silicon Texture Etching in 20% NaOH/H_2O followed by Texturizing in 2% NaOH/H_2O with Isopropyl Alcohol	51
8.1	Block Diagram of Polysilicon Solar Cell Process with Several New Optimal Process Steps.	60
8.2	Electrical Performance of Pregettered Wacker Polysilicon Solar Cells Batch P-101.	62
8.3	Electrical Performance of Pregettered Wacker Polysilicon Solar Cells with SiO, Batch P-102.	62
8.4	Electrical Performance of Spray-on n^+ Doped Wacker Polysilicon Solar Cells with SiO AR Coating, Batch P-400 . . .	67
9.1	Block Diagram of Selected Polysilicon Cell Process	76
9.2	Electrical Performance Curve of Average Wacker Polysilicon Solar Cell Produced from the Selected Process.	80
9.3a	Electrical Performance Curve of Average Crystal System's HEM Solar Cell (100% single crystallinity) Produced from the Selected Process	81
9.3b	Electrical Performance Curve of Average Crystal Systems HEM Polysilicon Solar Cell (44% single crystallinity) Produced from the Selected Process.	82
9.4	Electrical Performance Curve of Average Exotic Materials Polysilicon Solar Cell Produced from the Selected Process . .	83
10.1	Photowatt International CELLCO Production Line	88

LIST OF TABLES

Table No.	Title	Page No.
4.1	Electrical Performance Data for Isotropic Surface Etched Wacker Polysilicon and Single Crystal Silicon Solar Cells.	18
5.1	Data for Determining Crystal Grain Size Distribution in Wacker Polysilicon Wafer Material	26
5.2	Summary of the Contributions of all Crystal Grains to the Fractional Power Loss Q for $g_i < s - t_o = 0.115$ inches in Wacker Polysilicon Material	29
5.3	Gridline Spacing and Electrical Performance Data for Wacker Large Area Fine and Coarse Grain Polysilicon Full Solar Cells	31
5.4	Gridline Spacing and Electrical Performance Data for Wacker Large Area Fine and Coarse Grain Polysilicon Quarter Solar Cells. . . .	33
6.1	Texture Etch Rate for Fine Grain and Coarse Grain Polysilicon and Single Crystal Silicon in 20% $NaOH/H_2O$ with Cold Water Rinse. . . .	40
6.2	Texture Etch Rate for Fine Grain and Coarse Grain Polysilicon and Single Crystal Silicon in 20% NaOH in Hot Water Rinse	43
6.3	Texture Etch Rate for Coarse Grain Polysilicon and Single Crystal Silicon in 10% $NaOH/H_2O$ with Cold Water Rinse.	46
6.4	Texture Etch Rate and Texturizing Etch Rate for Fine and Coarse Grain Polysilicon and Single Crystal Polysilicon	49
6.5	Texture Etch Rate and Texturizing Etch Rate for Fine and Coarse Grain Polysilicon and Single Crystal Polysilicon in Isopropyl Alcohol.	52
7.1	Effect of $POCl_3$ Diffusion Time and Temperature Schedules for Wacker Polysilicon Solar Cells	57
8.1	Pregettering Effects on Large Area Polysilicon Solar Cells	63

LIST OF TABLES

Table No.	Title	Page No.
8.2	Intermediate Gettering and Pregettering Effects on Large Area Polysilicon Solar Cells.	65
8.3	Spray-on n^+ Dopant Junction Formation Effects on Large Area Polysilicon Solar Cells	68
8.4	Printed and Evaporated Aluminum Effects on $POCl_3$ Diffused Polysilicon and Single Crystal Silicon Solar Cells.	71
8.5	Printed and Evaporated Aluminum Effects on Spray-on n^+ Doped Polysilicon and Single Crystal Silicon Solar Cells.	73
9.1	Electrical Performance Data on Three Types of Large Area Polysilicon Solar Cells Produced from the Selected Process.	84
10.1	CELLCO Process Cost Summary in 1975 Cents per Peak Watt.	91

APPENDICES

TABLE OF CONTENTS

Title	Page No.
APPENDIX I	
ABSTRACT	ii
INTRODUCTION	1
DESCRIPTION OF THE INDUSTRY	1
CELLCO COMPANY DESCRIPTION	3
PROCESS DESCRIPTION	6
1. Wafer Surface Preparation	6
2. Junction Formation	10
3. Front Surface Pattern Printing	13
4. Electroless Nickel Plating	17
5. Resist Removal	21
6. Laser Trimming Process	24
7. Solder Flow and Flux Removal	29
8. Antireflective Coating	34
9. Cell Testing	39
PRICE COMPUTATION	43
DISCUSSION OF RESULTS	45
CONCLUSIONS AND RECOMMENDATIONS	47
REFERENCES	48
INDUSTRY DESCRIPTION, Format C	49
APPENDIX II- COMPANY DESCRIPTION, Format B and PROCESS DESCRIPTION, Format A for CELLCO	51
APPENDIX III - TEMPORARY CATALOG FOR EXPENSE ITEMS	71

APPENDIX I

LIST OF FIGURES

Figure No.	Title	Page No.
C-0	Photowatt International CELLCO Production Line.	4
C-1	Automatic Texturizing System	7
C-2	Conceptual Design of Spray-on Dopant Junction Formation System	12
C-3	Schematic Layout of Automatic Wafer Printing System.	14
C-4	Schematic Layout of Nickel Plating System.	18
C-5	Schematic Layout of Wet Chemical Resist Removal System	22
C-6	Serial Flow Laserscribe Trimming System for 7200 wafers/hr..	25
C-7	Conceptual Solder Coating and Flux Removal System	30
C-8	LFE 8000 System for Silicon Nitride Antireflective Coating	35
C-9	Conceptual Design of Automatic Solar Cell Test System	40

APPENDIX I
LIST OF TABLES

Table No.	Title	Page No.
1	CELLCO Process Cost Summary.	44

1.0 INTRODUCTION

The production of low-cost, large area, high efficiency polysilicon solar cells is the overall goal of this program. The major tasks which comprise this project include: (1) development of a low-cost polysilicon solar cell process sequence which achieves ten percent (10%) efficient large area polysilicon solar cells in batch quantities, (2) development of a front surface grid pattern optimized with respect to crystal grain size, (3) investigation of a polysilicon wafer surface macrostructure or texturizing process suitable for large-scale production, (4) study of junction formation techniques, (5) investigation of antireflective coatings (AR coatings) and, (6) exploration of other processes, as necessary, to obtain high efficiency or low-cost polysilicon solar cells.

All the tasks were performed on a production scale as opposed to a laboratory scale. Production equipment was utilized throughout the investigations. The data was examined primarily to determine general trends and process characteristics which are applicable for near-term implementation in large-scale production.

It was concluded from a detailed SAMICS process cost analysis that the solar cell process costs are in-line with the 1986 JPL/LSA cost goals. The total 1986 solar cell selling price was 33 cents per peak watt in 1975 cents which included 13.2 cents per peak watt for the polysilicon wafer material and 19.8 cents per peak watt manufacturing cost for the solar cell. Additional work to significantly reduce metallization costs and AR coating costs were recommended.

2.0 POLYSILICON MATERIAL DESCRIPTION

Three types of large-area polysilicon material were investigated in this program. The Wacker Chemical Corporation from Santa Clara, California supplied 3.94 inch (10 cm) square by 18 mil (0.457 mm) thick polysilicon wafers grown by their SILSO process; Crystal Systems, Inc. from Salem, Massachusetts supplied 3.94 inch (10 cm) square by 20 mil (0.508 mm) thick polysilicon wafers grown via their Heat Exchanger Method; Exotic Materials, Inc. from Costa Mesa, California supplied 4.0 inch (10.16 cm) round by 25 mil (0.635 mm) thick polysilicon wafers grown via their fast pull Czochralski (FAST) process.

A study was conducted to determine the average crystal grain size in the Wacker, Crystal Systems and Exotic Materials wafers. A discussion of the measurement technique and results for the three polysilicon materials follows.

2.1 Wacker Material

Two types of Wacker polysilicon wafers were studied. The first type is characterized by a "coarse" grain structure with varying crystal grain sizes. A picture of a typical Wacker coarse grain polysilicon wafer with a metallization pattern is shown in Figure 2.1. The second type of Wacker polysilicon material is characterized by a "fine" grain structure with varying crystal grain sizes.

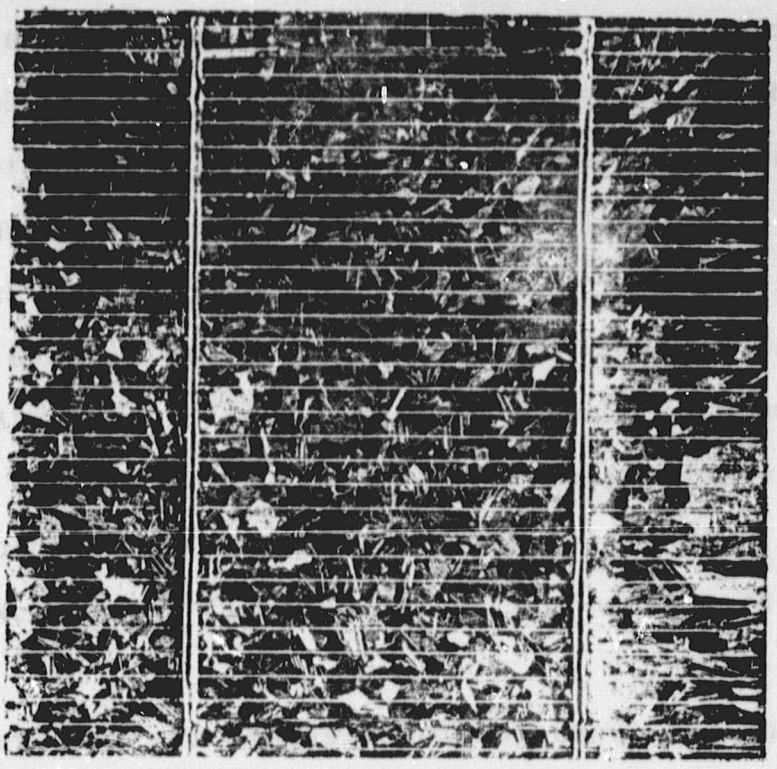


Figure 2.1. Picture of Wacker Coarse Grain Polysilicon Material with Metallization Pattern.

The average crystal grain size, d_g, in a sample lot of Wacker polysilicon wafers was computed on the basis of a statistical analysis of crystal grain size measurements. A total of 200 individual grains were measured from a random sampling of grains from four polysilicon wafers. A complete measurement consisted of visually measuring both the longest and shortest grain dimensions. After the completion of two hundred such measurements, the average crystal grain size, d_g, was computed from the statistically averaged values of the longest, d_l, and shortest, d_s, grain dimensions.

The statistically averaged value of the longest and shortest coarse grain dimensions for the Wacker material are:

$$d_l = 0.212 \text{ inches}$$

$$d_s = 0.105 \text{ inches}$$

$$d_g = \tfrac{1}{2} (d_l + d_s) = 0.16 \text{ inches}$$

The average crystal grain size for the coarse grain material was found to be 0.16 inches. Elongated crystal grains extending to one-half inch from the edge of the wafer are a characteristic feature of this polysilicon material. The crystal grains are fibrously oriented and extend from the front to the back surface of the polysilicon wafer.

Four Wacker "fine grain" wafers were selected and grain sizes measured. The statistically averaged value of the longest and shortest fine grain dimension are:

$$d_l = 0.071 \text{ inches}$$

$$d_s = 0.040 \text{ inches}$$

$$d_g = 0.055 \text{ inches}$$

The averaged crystal grain size for the fine grain material in this study was found to be 0.055 inches. The crystal grains are randomly oriented out to the edges of the polysilicon wafers.

2.2 Crystal Systems Material

Two types of Crystal Systems material were examined. The first type is 100% single crystal silicon (non-polysilicon) as a part of the same ingot as the polysilicon second type. The second type is 44% single crystal silicon and 56% polysilicon. These wafers are characterized by a single crystal circular region, surrounded by predominantly large crystal grains. Small crystal grains lie at the boundary between the single crystal region and the large grain polysilicon region. Pictures of the solar cells made from the two types of Crystal Systems material are shown in Figures 2.2 and 2.3.

Fifty individual grains were measured from a random sampling of grains from a typical Crystal Systems polysilicon wafer. The statistically averaged value of the longest and shortest grain dimensions are listed below.

$$d_l = 0.095 \text{ inches}$$

$$d_s = 0.057 \text{ inches}$$

$$d_g = 0.076 \text{ inches}$$

Figure 2.2 Picture of Crystal System HEM Material with 100% Single Crystallinity with Metallization Pattern.

Figure 2.3 Picture of Crystal Systems HEM Material with 44% Single Crystallinity and with Metallization Pattern

The average small crystal grain size for the Crystal Systems wafer examined in this study was 0.076 inches. Approximately five percent of the active area occupied was determined to have small crystal grains.

2.3 Exotic Materials Material

The Exotic Materials polysilicon is similar in general appearance to the Wacker material and also has a coarse grain structure with varying crystal grain size, as shown in Figure 2.4. The statistically averaged value of the longest and shortest grain dimensions are:

$$d_l = 0.210 \text{ inches}$$

$$d_s = 0.108 \text{ inches}$$

$$d_g = 0.16 \text{ inches}$$

The average crystal grain size for the Exotic Materials wafer examined in this study was 0.16 inches. This value is identical to the average crystal grain size obtained for the coarse grain Wacker material

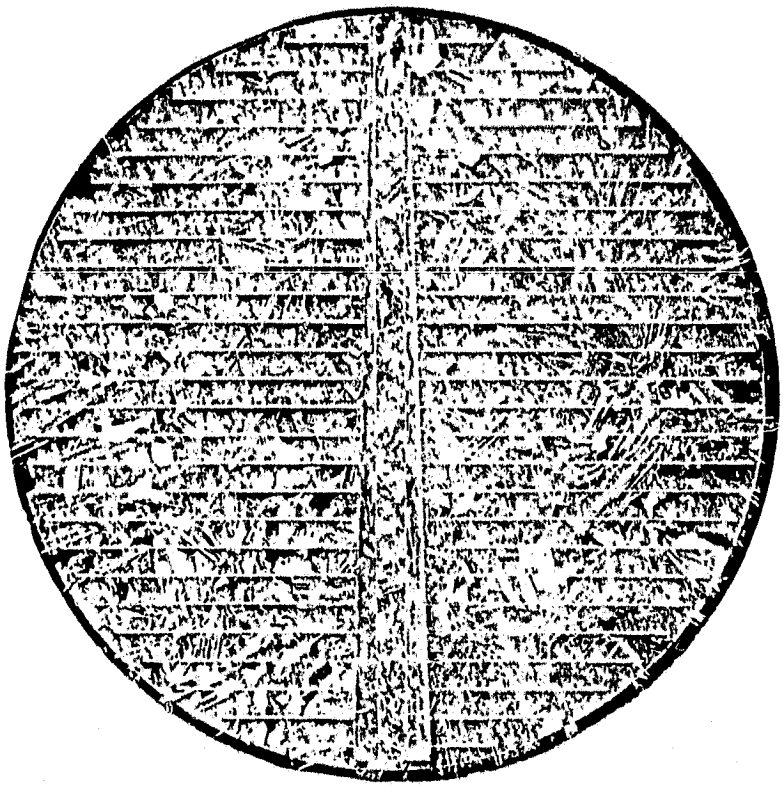


Figure 2.4. Picture of Exotic Materials Coarse Grain Polysilicon Material with Metallization Pattern.

3.0 INITIAL PROCESS STUDIES

Process studies were initiated to identify directions which lead to low-cost, high efficiency polysilicon solar cells. Initial experiments proceeded by utilizing Wacker polysilicon material in Photowatt's standard three-inch diameter single crystal solar cell process sequence which is outlined in Figure 3.1. Ten centimeter square wafers were processed. The wafers were texturized with a two-stage process,[1] diffused in $POCl_3$, aluminum evaporated, nickel plated, solder dipped and AR coated with SiO. The solar cells were cut by laser into 3" x 2.9" cells.

Representative electrical performance data from this first polysilicon solar cell (Batch P-100) are as follows:

$I_{SC}(A)$: 1.48

$V_{OC}(V)$: 0.535

$I_{pp}(A)$: 1.11

$V_{pp}(V)$: 0.385

$\eta(\%)$: 7.61

FF : 0.540

*An unacceptable number of wafers was broken. Texturized polysilicon wafers were observed to have poor mechanical strength at a thickness of about 11 to 12 mils. Special care in wafer handling and processing during solar cell fabrication was found to be essential.

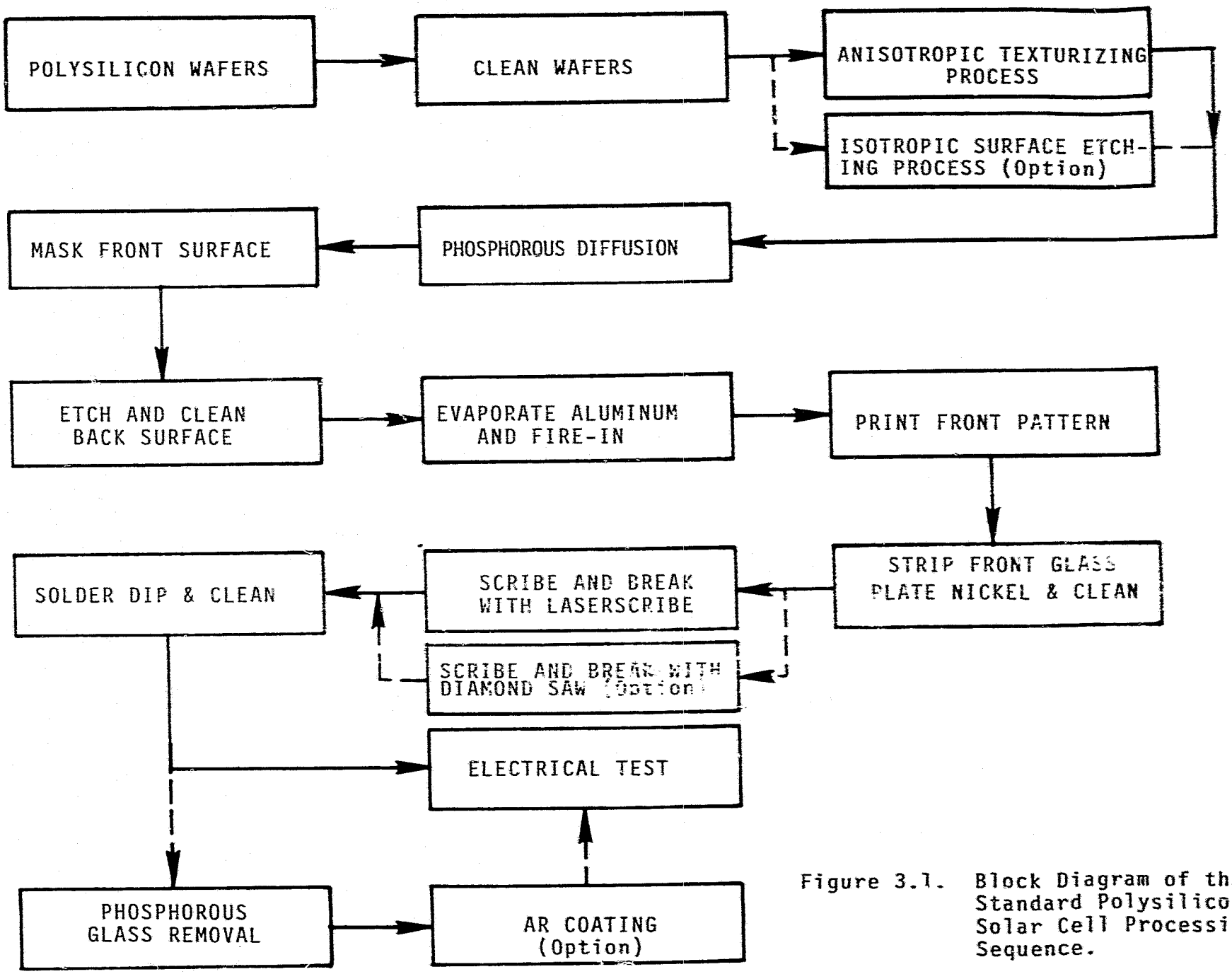


Figure 3.1. Block Diagram of the Standard Polysilicon Solar Cell Processing Sequence.

The primary motivation for performing the preliminary tests was to investigate the applicability of current standard single crystal silicon solar cell process methods to polysilicon material. Current production of single crystal solar cells with AR coatings have efficiencies in the range of 11% to 14%. The significantly lower overall electrical performance data presented above indicates a need to explore polysilicon material characteristics, and solar cell process methods for achieving improvements in the electrical performance of polysilicon solar cells.

4.0 INFLUENCE OF CRYSTAL GRAINS ON SOLAR CELL EFFICIENCY

The influence of the structural properties of polysilicon material on solar cell efficiency can be approximated with the use of the diffusion length model.[2] The diffusion length model for polysilicon was utilized to obtain a theoretical comparison between single crystal and polysilicon solar cell efficiencies. The major reason for performing this comparison was to determine whether the lower efficiencies obtained for polysilicon solar cells, relative to single crystal solar cells, were due primarily to grain boundary effects, other material effects, or to processing inadequacies. A discussion of the results achieved from the theoretical and experimental comparison between polysilicon and single crystal silicon solar cell efficiencies is given below.

4.1 Theoretical Comparison Between Polysilicon and Single Crystal Silicon Solar Cell Efficiency

The diffusion length model for polysilicon material[2] contends that the influence of a crystal grain boundary extends one diffusion length, L_d. Assuming fibrously oriented crystal grains with square cross-section, the effective size of each crystal grain is reduced by 2 L_d. Consequently, an approximate expression for the ratio of the efficiencies of polysilicon solar cells, η_p, with the efficiencies of single crystal solar cells, η_s, of the same geometrical area is as follows:

$$\frac{\eta_p}{\eta_s} = \left(1 - \frac{2L_d}{d_g}\right)^2 \qquad \text{Eq. (4.1)}$$

where d_g is the average geometrical grain size of a polysilicon solar cell.

This simple theoretical expression indicates that for fine crystal grain sizes, the efficiency of polysilicon solar cells shall be appreciably lower than the efficiency of single crystal solar cells. For example, for a typical diffusion length equal to 50 microns and an average crystal grain size of 1000 microns (0.039 inches), the efficiency ratio is approximately 0.810. Theoretically, the efficiency of coarse grain polysilicon solar cells is expected to be close to the efficiency of single crystal solar cells according to Equation (4.1.). That is, for a typical diffusion length equal to 50 microns and an average crystal grain size of 4064 microns (0.16 inches), the efficiency ratio is approximately 0.951.

4.2 Experimental Comparison Between Polysilicon and Single Crystal Silicon Solar Cell Efficiency

An experimental comparison between polysilicon and single crystal silicon solar cell efficiency was made to check the validity of the theoretical efficiency ratio from the diffusion length model for polysilicon material. Four inch square Wacker polysilicon wafers and three inch diameter single crystal wafers were utilized in the study. The average diffusion length for both types of wafers was 50 microns. The average crystal grain size for the Wacker material was 4064 microns (0.16 inches).

The baseline fabrication sequence given in Figure 3.1 was used to process the isotropic surface etched polysilicon Batch P-311 and single crystal Batch S-311. Following the nickel plating step, the single crystal wafers were cut by laserscribe into 1.90" x 1.90" squares and the 4" x 4" square Wacker polysilicon wafers were cut into four 1.90" x 1.90" squares to facilitate comparison of their electrical performances and comparison of their efficiency ratios.

The electrical performance curves for the polysilicon and the single crystal silicon solar cells are shown in Figure 4.1. The electrical performance parameters are given in Table 4.1.

The experimental efficiency ratio was determined to be 0.738. This experimental efficiency ratio was found not to be in agreement with the theoretical efficiency ratio of 0.951 obtained earlier. These results may bring into question the validity of the diffusion length model for polysilicon material, however, other efficiency loss mechanisms may also be operative.

Recent work[3] indicates that if the diffusion length model is modified such that, as the generation point of a minority carrier becomes increasingly distant from the grain boundary, the probability of its absorption at the grain boundary decreases and becomes negligible at a distance equal to the bulk diffusion lenth. At this point predicted

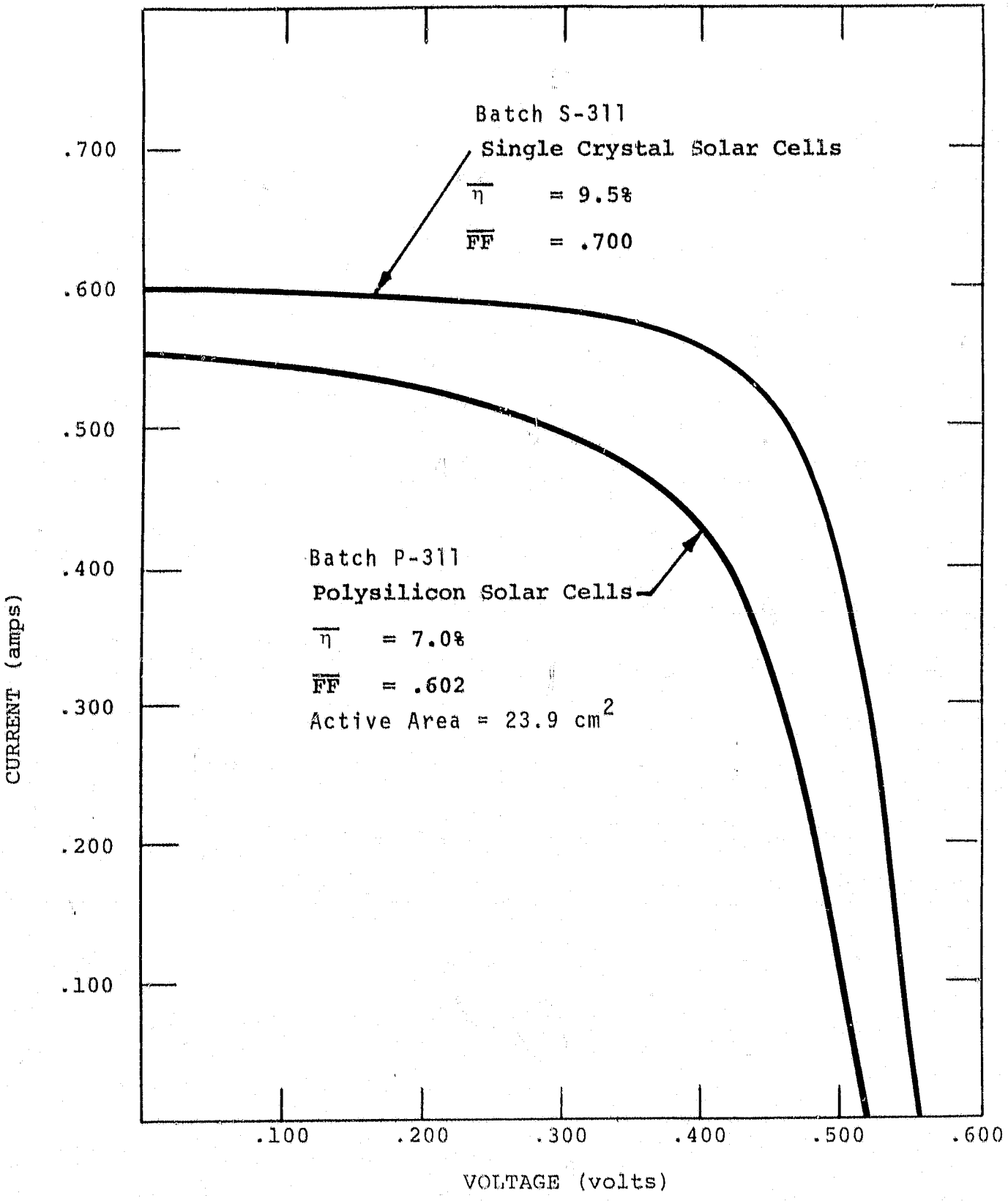


Figure 4.1. Electrical Performance Curves for Isotropic Surface Etched Wacker Polysilicon and Single Crystal Silicon Solar Cells.

Table 4.1. Electrical Performance Data for Isotropic Surface Etched Wacker Polysilicon and Single Crystal Silicon Solar Cells (25 cells per batch).

BATCH	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF	$\frac{\Delta\eta}{\eta}$(%)	$\frac{\Delta FF}{FF}$(%)
P-311 Polysilicon Solar Cells, Isotropic Surface Etched, Standard Process, Active Area 23.9 cm^2.								
High	0.630	0.525	0.570	0.405	9.41	0.698	+34.1%	+45.9%
Low	0.490	0.510	0.350	0.375	5.35	0.525	-23.7%	-12.8%
Wt.Ave.	0.555	0.515	0.425	0.405	7.02	0.602		
S-311 Single Crystal Silicon, Isotropic Surface Etched, Standard Process, Active Area 23.9 cm^2.								
High	0.665	0.560	0.590	0.440	10.58	0.700	+11.30%	+0.0%
Low	0.595	0.550	0.500	0.420	8.56	0.642	-10.00%	-8.29%
Wt.Ave.	0.600	0.555	0.530	0.440	9.51	0.700		

and measured generation currents are in close agreement. Gridline pattern design is another potential cause of sub-optimum polycrystal cell performance, and is discussed in the next section.

5.0 GRIDLINE PATTERN DESIGN CONSIDERATIONS

A study was conducted to identify the necessary criteria which must be satisfied to optimize the gridline pattern design for polysilicon solar cells. It was shown in Section 4.0 that polysilicon material exhibits lower energy conversion efficiences than single crystal solar cells, and that a contributing factor to this result may be due to crystal grain boundary effects.

The amount of power dissipated at each crystal grain boundary is not known. However, if the spacing between successive gridlines is less than the average crystal grain size, one should be able to avoid most of the power losses due to insufficient gridline coverage. This constraint can be explained qualitatively by noting that each crystal grain will have a high probability of being contacted if the gridline spacing is less than the average crystal grain size. If this condition is not met, a large number of grains may not be contacted by gridlines, which implies that a portion of the power generated at these grains will be lost at the grain boundaries due to minority carrier recombination.

A generalized first order equation for computing the fractional power loss due to insufficient gridline coverage of polysilicon crystal grains is derived below. It is used to perform a gridline spacing sensitivity analysis. Data was taken to check the theory and is given along with a discussion of the results.

5.1 Generalized Equation for Computing Fractional Power Loss

The derivation of a first order generalized equation for computing the fractional power loss due to insufficient gridline coverage of polysilicon crystal grains resides in four assumptions which are listed below:

1. All crystal grains within a given grain size distribution are randomly distributed throughout the polysilicon wafer.
2. All crystal grains are square.
3. All crystal grains are aligned so that one side of each grain is parallel to a gridline.
4. All crystal grains not contacted by a gridline have zero power output.

Consider a succession of parallel gridlines in a polysilicon sample, each with a width, t_o, and a spacing, s, between center lines. Attention will now be focused on a set of two parallel gridlines and a one dimensional coordinate system used for reference to indicate the random location, x, of the i^{th} crystal grain of size g_i, as shown in Figure 5.1. On the basis of assumption (1) above, the midpoint of a crystal grain of size g_i is equally likely to be located at any point between x = o and x = s in Figure 5.1. The probability that the i^{th} crystal grain will contact a gridline can now be determined.

There are three regions in Figure 5.1 in which the midpoint of the i^{th} crystal grain can be located. If the midpoint of the i^{th} crystal grain is located anywhere along the x-axis in Region I or III, the i^{th} crystal grain will touch

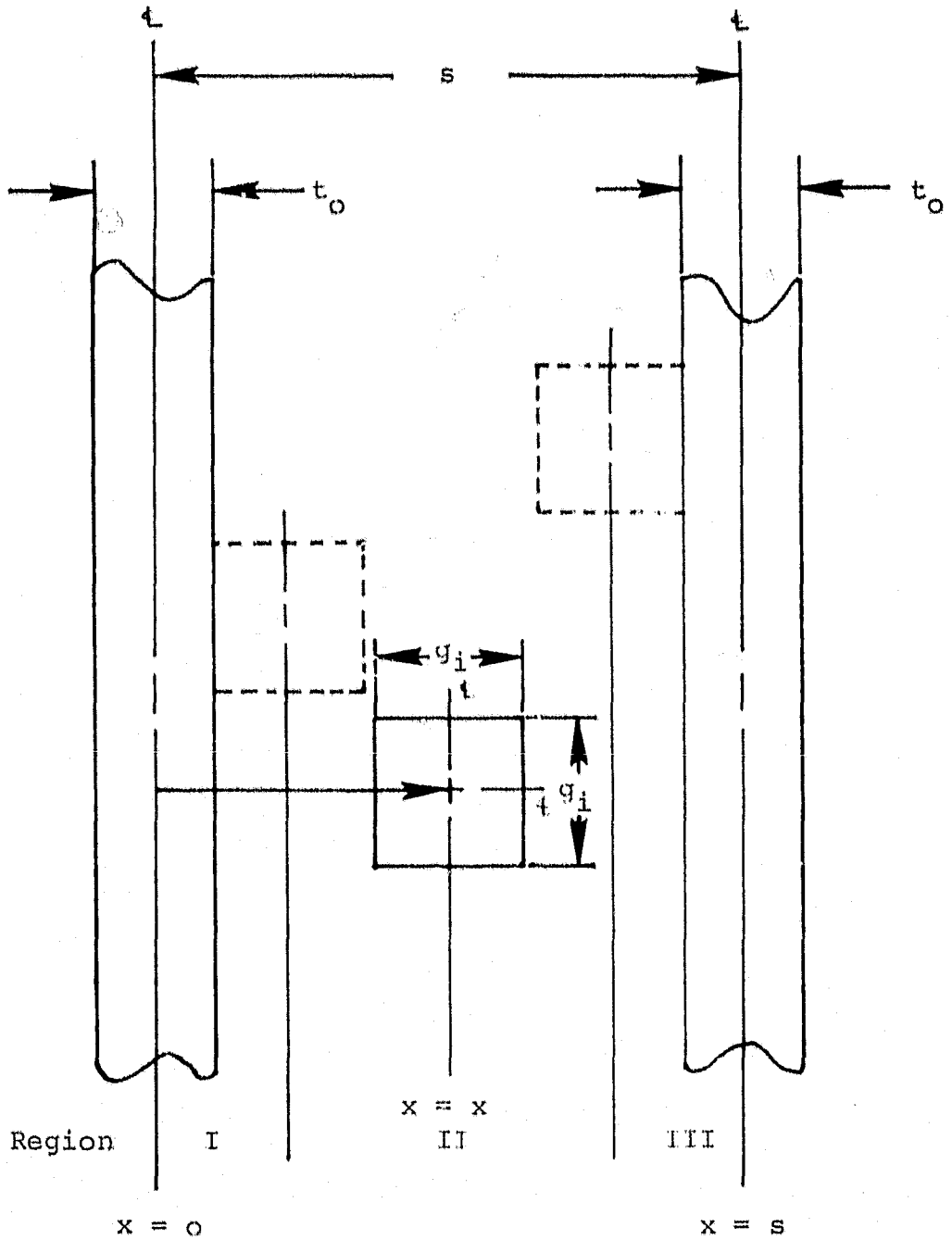


Figure 5.1. A Depiction of the Three Regions between Two Parallel Gridlines where the Midpoint of the i^{th} Crystal Grain may be Located within a Distance of x = 0 to x = s.

a gridline. If the midpoint of the i^{th} crystal grain is at any location along the x-axis in Region II, the i^{th} crystal grain will not touch a gridline. Thus, the three regions locating the midpoint of the i^{th} crystal grain are represented as follows:

$$\text{Region I} \qquad 0 \leq x \leq (g_i + t_o)/2$$

$$\text{Region II} \quad (g_i + t_o)/2 < x < s - (g_i + t_o)/2$$

$$\text{Region III} \quad s - (g_i + t_o)/2 \leq x \leq s$$

From the above discussion, it is clear that the fractional length of s for which the i^{th} crystal grain may contact a gridline is just the summation of the x distances in Regions I and III divided by, s, which is $(g_i + t_o)/s$. This fractional length represents the probability that the i^{th} square crystal grain of size g_i will hit a gridline within a distance s between the center lines of two parallel gridlines.

The probability, p, that the i^{th} square crystal grain of size g_i will not hit a gridline is given by:

$$p = 1 - (g_i + t_o)/s. \qquad \text{Eq. (5.1)}$$

It follows that for an arbitrary crystal grain of size g_i, where $g_i + t_o \geq s$, this grain will touch a gridline with 100% probability. On the other hand, for an arbitrary crystal grain of size g_i, where $g_i + t_o < s$, there is a probability that this grain will not hit a gridline.

The probability of the i^{th} crystal grain not hitting a gridline implies the existence of a power loss on the basis of assumption (4), which assumes zero power output from a crystal grain not contacted by a gridline. Since the power output of a given crystal grain of area g_i^2 is directly proportional to its area, the fractional power loss, q, in a distribution of grain sizes due to crystal grains of size $g_i < s - t_o$ not hitting gridlines is given by:

$$q = \left(1 - \frac{g_i + t_o}{s}\right) \frac{g_i^2 \; n_i}{A} \qquad \text{Eq. (5.2)}$$

where:

g_i^2 = area of i^{th} crystal grain

$\left(1 - \frac{g_i + t_o}{s}\right)$ = probability of i^{th} crystal grain not hitting a gridline

n_i = number of grains with area g_i^2 in a given grain size distribution

A = the total area encompassed by all grains in a given grain size distribution

This assumes negligible grain boundary effects. If there are a total of "K" different grain sizes in a particular crystal grain size distribution, for which $g_i < s - t_o$, and i = 1 to K, the fractional power loss, Q, in this crystal grain size distribution, due to all grains of size g_i (i = 1 to K) is given by:

$$Q = \frac{1}{A} \sum_{i=1}^{K} \left(1 - \frac{g_i + t_o}{s}\right) g_i^2 \; n_i \qquad \text{Eq. (5.3)}$$

This result may be used to compute the fractional power loss in a polysilicon solar cell due to insufficient gridline coverage of those crystal grains for which $g_i < s - t_o$. If the fractional power loss, Q, is significant, this is an indication that the gridline spacing, s, is not optimized.

5.2 Gridline Spacing Sensitivity Analysis

5.2.1 Crystal Grain Size Distribution

The crystal grain size distribution in a given polysilicon material must be determined prior to calculating the fractional power loss for a given grid pattern design. In this study, four sample Wacker polysilicon wafers were chosen. Two hundred crystal grains were measured (g_i), grouped (i^{th} group) and counted (n_i). The total area, A, of the sample was determined. The average crystal grain size was computed. These data are given in Table 5.1. The average crystal grain size for the Wacker polysilicon material was found to be 0.16 inches. It was assumed for convenience that the crystal grain size distribution obtained from these measurements is characteristic of the Wacker coarse grain polysilicon material.

5.2.2 Gridline Spacing for Minimal Fractional Power Loss

The gridline spacing, s, and width, t_o, for the solar cells made from the Wacker coarse grain polysilicon material are 0.125 inches and 0.010 inches, respectively, as shown in Figure 5.2. The only crystal grain sizes which have a probability of not hitting a gridline in this case are for those grains where $g_i < s - t_o$ or $g_i <$ 0.115 inches. Within the two

Table 5.1. Data for Determining Crystal Grain Size Distribution in Wacker Polysilicon Wafer Material.

Group $i = 1$ to K	Grain Size g_i (inches)	Number n_i	Area $g_i^2 n_i$ (in^2)	Total Grain Size $g_i n_i$ (inches)
1	.07	1	.0049	.07
2	.08	8	.0512	.64
3	.09	6	.0486	.54
4	.10	10	.1000	1.00
5	.11	11	.1331	1.21
6	.12	14	.2016	1.68
7	.13	16	.2704	2.08
8	.14	16	.3136	2.24
9	.15	31	.6975	4.65
10	.16	7	.1792	1.12
11	.17	12	.3468	2.04
12	.18	11	.3564	1.98
13	.19	5	.1805	.95
14	.20	8	.320	1.60
15	.21	17	.7497	3.57
16	.22	3	.1452	.66
17	.23	3	.1587	.69
18	.24	3	.1728	.72
19	.25	10	.6250	2.50
20	.26	3	.2028	.78
21	.27	4	.2916	1.08
22	.28	1	.0784	.28
TOTAL NUMBER		200	--	32.08
Sample Area			5.63	
Average Grain Size				0.16

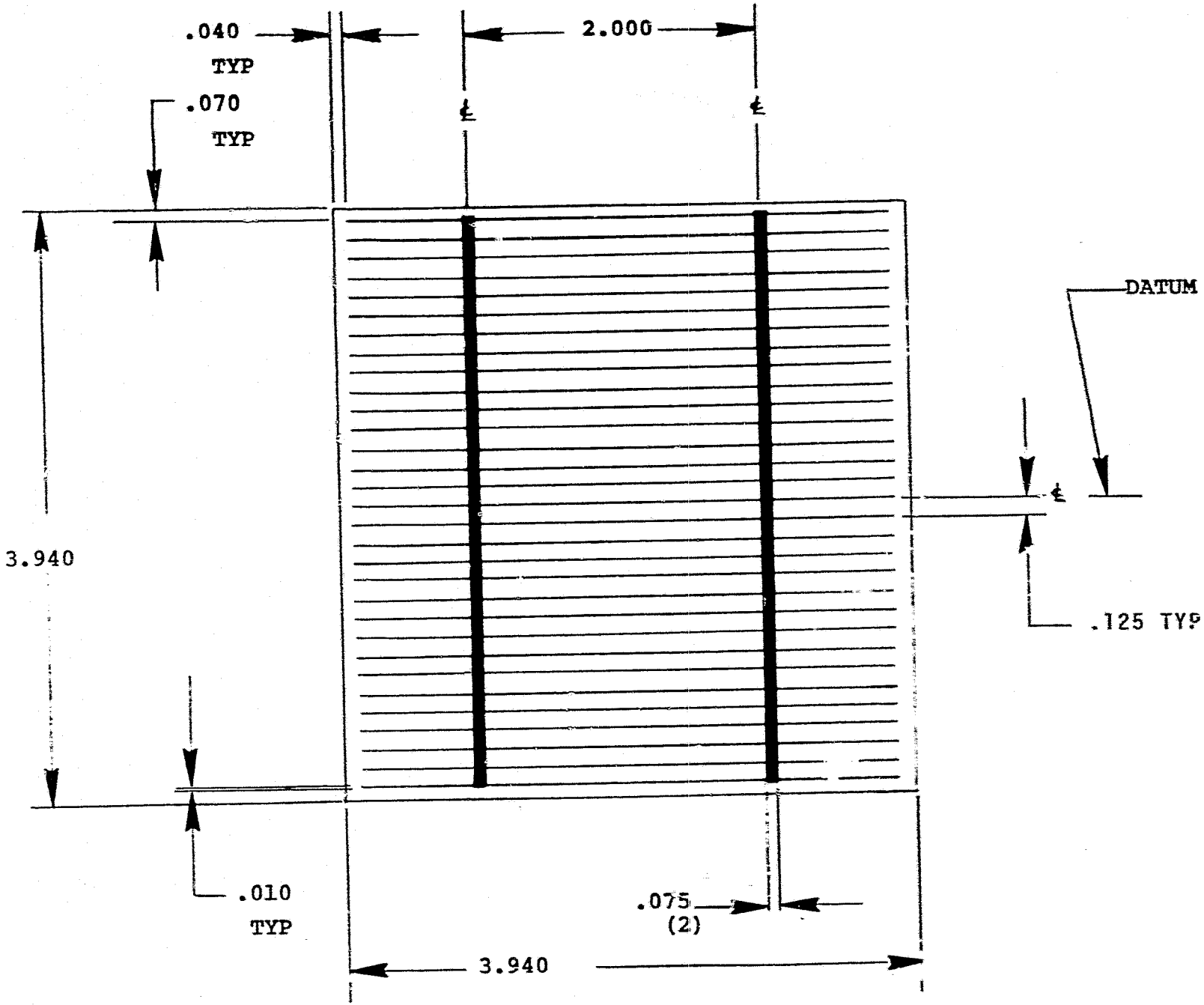


Figure 5.2. Gridline Pattern for Wacker Polysilicon Solar Cells.

hundred random crystal grain size measurements, there was a total of 36 crystal grains which fell into this category. These 36 crystal grains were divided into five groups (i.e. K = 5) ranging in size from 0.07 inches to 0.11 inches. The contribution of each group to the fractional power loss, Q, (in the 200 crystal grains) is tabulated in Table 5.2.

The fractional power loss, Q, was found to be 0.77%. For this case, the power loss associated with insufficient gridline coverage of polysilicon crystal grains is minimal. This result shows that a 0.125 inch gridline spacing is close to the fully covered value for the Wacker polysilicon coarse grain material.

5.2.3 Gridline Spacing for Significant Fractional Power Loss

The fractional power loss, Q, may be a significant factor to consider for gridline spacing optimization. For example, consider a gridline pattern with spacing, s, and width, t_o equal to 0.250 inches and 0.035 inches, respectively, for the Wacker coarse grain polysilicon material. The model shows that grain sizes which provide non-zero contributions to the fractional power loss, Q, are those for which $g_i < s - t_o$ or $g_i < 0.215$ inches. The fractional power loss for this case is 17.8 percent. This result indicates that for a wide gridline spacing, a significant power loss may occur due to insufficient gridline coverage of the crystal grains. This loss would be over and above any sheet resistance losses due to wider grid spacing, I^2R losses in the grid and also neglects shadow loss effects.

Table 5.2. Summary of the Contributions of all Crystal Grains to the Fractional Power Loss Q for $g_i < s - t_o = 0.115$ inches in Wacker Polysilicon Material.

ith Group	g_i	n_i	$\frac{g_i + t_o}{s}$	$1 - \frac{g_i + t_o}{s}$	$\left(1 - \frac{g_i + t_o}{s}\right) g_i^2 n_i$
1	.07	1	.64	.36	.0018
2	.08	8	.72	.28	.0143
3	.09	6	.80	.20	.0097
4	.10	10	.88	.12	.0120
5	.11	11	.96	.04	.0053
				TOTAL	.0431 in^2

$$Q = \frac{1}{A} \sum_{i=1}^{5} \left(1 - \left(\frac{g_i + t_o}{s}\right)\right) g_i^2 n_i = \frac{.043}{5.63} = 0.77\%$$

$A = 5.63$ in^2 (Area of 200 sampled crystal grains)

$s = 0.125$ in

$t_o = 0.010$ in

(g_i) max $= 0.11$ in

(g_i) min $= 0.07$ in

$K = 5$

5.3 Experimental Data and Results

Wacker polysilicon solar cells were processed as a means of checking the grid pattern spacing sensitivity analysis results predicted by the model. Fine and coarse grain large area polysilicon material were processed together using the standard process (texturization, $POCl_3$ diffusion, evaporated aluminum back, nickel plating and solder) with the phosphorous glass removed. The average fine and coarse grain sizes were found to be 0.05 inches and 0.16 inches, respectively. The active area of the cells was 14.4 $in.^2$ (92.7 cm^2). Narrow and wide gridline spacing metallization patterns were utilized. The spacing and thickness of the fine gridlines were 0.125 inches and 0.010 inches, respectively. The spacing and thickness of the wide gridlines were 0.250 and 0.035 inches, respectively.

The gridline spacing and electrical performance data for the Wacker large area fine grain and coarse grain polysilicon solar cells are given in Table 5.3. The wide gridline spacing pattern has six percent higher shadowing area coverage than the narrow gridline spacing pattern; and the short circuit current, I_{sc}, peak power current, I_{pp}, and the efficiency, η have been multiplied by the factor 1.06 to account for this difference and to allow for a comparison. The open circuit voltage, V_{oc}, peak power voltage, V_{pp}, and fill factor, FF, were not adjusted. The percent difference is given in Table 5.3 and is discussed below.

Table 5.3 Gridline Spacing and Electrical Performance Data for Wacker Large Area Fine and Coarse Grain Polysilicon Full Solar Cells.

Cell No.	Gridline Spacing / Grain Size	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF
Fine Crystal Grain ($\overline{g_f}$ - 0.05 inches), Active Area = 92.7 cm^2, Standard Cell Process, Glass Removed.							
1A	Narrow	2.20	0.500	1.75	0.360	6.8	0.573
1B	Wide	2.13*	0.495	1.75*	0.365	6.9*	0.605
	%Difference	3	1	0	-1	-1	-6
Coarse Crystal Grain ($\overline{g_f}$ - 0.16 inches), Active Area - 92.7 cm^2, Standard Cell Process, Glass Removed.							
1A	Narrow	1.90	0.540	1.55	0.425	7.1	0.642
2B	Wide	1.95*	0.535	1.53*	0.405	6.7*	0.592
	%Difference	-3	1	1	5	6	8
Narrow Gridline Spacing (s = 0.125 inches), Active Area - 92.7 cm^2, Standard Cell Process, Glass Removed.							
1A	Fine Grain	2.20	0.500	1.75	0.360	6.8	0.573
1B	Coarse Grain	1.90	0.540	1.55	0.425	7.1	0.642
	%Difference	14	-8	11	-18	-4	-12
Wide Gridline Spacing (s = 0.250 inches), Active Area - 92.7 cm^2, Standard Cell Process, Glass Removed.							
2A	Fine Grain	2.13*	0.495	1.75*	0.365	6.9*	0.605
2B	Coarse Grain	1.95*	0.535	1.53*	0.405	6.7*	0.592
	%Difference	8	-8	13	-11	3	2

*Effective current which equals (1.06) Times Actual Measured Current to Account for Higher Shadowing from the Wide Gridline Pattern.

The gridline spacing observations are not in accordance to the fractional power loss model discussed earlier. The model predicts significant electrical performance differences between the polysilicon solar cells made with the narrow and wide gridline spacings. Very little difference between the electrical performance parameters was observed.

The crystal grain size material observations show large differences in the electrical performance parameters for narrow and wide gridline spacing patterns. These results indicate possible differences in polysilicon material characteristics and energy loss mechanisms at their grain boundaries.

Before proceeding further in this discussion, it is important to check out possible large area polysilicon solar cell deficiencies, i.e. nonhomogeneous electrical performance, metallization, and edge effects.

The large area polysilicon solar cells were cut by diamond saw into quarters. Each cell was cut on three sides, the fourth side retained the etch ring. The total active area (excluding the etch ring) of each quarter cell was 21.1 cm^2.

The electrical performance data for the quarter cells were averaged and are given in Table 5.4. A comparison of fill factors indicates a significant difference between the large area polysilicon full cells and the large area polysilicon quarter cells. This difference is primarily due to the difference in peak power voltages, which was higher for the quarter

Table 5.4 Gridline Spacing and Electrical Performance Data for Wacker Large Area Fine and Coarse Grain Polysilicon Quarter Solar Cells.

Cell No.	Gridline Spacing / Grain Size	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF
Fine Crystal Grain ($\overline{gi}$ = 0.05 inches), Active Area = 21.1 cm^2, Standard Cell Process, Glass Removed.							
1A	Narrow	0.510	0.500	0.435	0.370	7.6	0.631
1B	Wide	0.500*	0.500	0.419*	0.400	7.9*	0.670
	% Difference	2	0	4	-8	-4	-6
Coarse Crystal Grain ($\overline{gi}$ = 0.16 inches), Active Area = 21.1 cm^2, Standard Cell Process, Glass Removed.							
1B	Narrow	0.450	0.540	0.365	0.445	7.7	0.668
2B	Wide	0.461*	0.540	0.371*	0.455	8.0*	0.678
	% Difference	-2	0	-2	-2	-4	-1
Narrow Gridline Spacing (s = 0.125 inches), Active Area = 21.1 cm^2, Standard Cell Process, Glass Removed.							
1A	Fine Grain	0.510	0.500	0.435	0.370	7.6	0.631
1B	Coarse Grain	0.450	0.540	0.365	0.445	7.7	0.668
	% Difference	12	-8	16	-20	-1	-6
Wide Gridline Spacing (s = 0.250 inches), Active Area = 21.1 cm^2, Standard Cell Process, Glass Removed.							
2A	Fine Grain	0.500*	0.500	0.419*	0.400	7.9*	0.670
2B	Coarse Grain	0.461*	0.540	0.371*	0.455	8.0*	0.678
	% Difference	8	-8	11	-14	1	-1

*Effective current which equals (1.06) times actual measurement current to account for higher shadowing from the wide gridline pattern.

cells than for the full cells. The improvement in peak power voltage was greater for the wide gridline spacing pattern than for the fine gridline spacing patterns. This indicates a possible deficiency in the main gridline (or trunk line) of both patterns. Thus, the main gridline resistive losses are higher for the full cells than for the quarter cells. An increase in the width of the main gridlines (which increases the shadowing losses, or addition of a copper strip across the entire length of the main gridline, should reduce the resistive losses. The latter method is preferred as it is utilized for cell-to-cell interconnection with the most recent PV solar module designs.

The four quarter cells from each wafer exhibit, in general, similar electrical performance characteristics. Edge effects were also similar for each of the four quarter cells of each full wafer. Most of the electrical performance characteristics of the large cells were exhibited by the smaller solar cells.* The notable exception is the peak power voltage which can be corrected as discussed above.

The experimental results discussed above show that the power degradation effects due to grain boundaries are considerably less than initially conceptualized for both the fine and the coarse grain polysilicon material. Other recently reported results[4] agree with this conclusion.

*Quarter cells were used in most of the experiments performed in the remainder of this report.

6.0 WAFER SURFACE TEXTURIZING PROCESS

Wafer surface texturizing involves the use of crystal orientation dependent etches that reduce front surface solar cell reflection losses. The surface macrostructures produced by anisotropic sodium hydroxide etching have been found to significantly improve single crystal solar cell photovoltaic energy conversion efficiency.[1,5,12] The feasibility of applying these process techniques to polysilicon wafers was investigated in this task. The texture etching rate, time and solution concentration were evaluated. The surface characteristics of the processed wafers were observed. An optimized texturizing process was developed.

6.1 Basic Wafer Surface Texturizing Process

The basic wafer surface texturizing process utilized in the experiments performed in this task consists of five steps. They are, (1) wafer surface cleaning, (2) wafer surface texturizing, (3) four stage cascade rinse, (4) final cleaning and (5) final rinse/spin dry.

(1) Wafer Surface Cleaning - The first step in the process consists of a two-stage wafer surface cleaning procedure. The wafers are placed into the first tank of an ultrasonic vapor degreasor containing boiling recycled Freon TMS[1] for five minutes. This is followed by a five minute placement in a second ultrasonic tank containing boiling Freon TMS with vapor zone to remove any remaining organic wafer surface contaminants which might otherwise impede the surface macrostructure etching step.

(2) Wafer Surface Texturizing - The second step in the process is wafer surface texturizing. The silicon wafers are introduced into an ultrasonic stainless steel tank which has been filled with sodium hydroxide and deionized (D.I.) water at 85°C to 90°C. Suspended in the tank is a clean, dry air bubbler system which is designed to agitate the solution in addition to the ultrasonics. Ten liters per minute of clean air are required for the bubbler. Experiments were performed to evaluate the texture etching rate, time and solution concentration. This will be discussed later.

(3) Four-Stage Cascade Rinse - The silicon wafers are removed from the surface macrostructure etching tank and placed into the first ultrasonic stage of a four-stage cascade rinse system which comprises the third step in the process. The wafers remain for five minutes in each of the four rinse stages.

Hot D.I. water flows at a rate of 3.8 liters per minute from the fourth stage where the D.I. water input temperature is 80°C $\pm$ 5°C to the first ultrasonic stage where the D.I. water output temperature is 72°C $\pm$ 5°C. The silicon wafers get progressively cleaner as they move from the first stage to the fourth stage of the cascade rinse system.

(4) Final Cleaning - The fourth step in the wafer surface texturizing process is final cleaning. The wafers are removed from the cascade rinse and introduced into concentrated sulfuric acid at $70^{o}C + 5^{o}C$ for five minutes. This solution removes any remaining contaminants that may be trapped on the wafer surface. The wafers are then rinsed off in running D.I. water for five minutes. This cleaning step is essentially a precautionary step used in the solar cells processed in this program to ensure the cleanliness of the texturized wafers. Under an optimized wafer surface texturizing process, the final cleaning step shall not be necessary provided the D.I. water is continuously replenished and the resistivity of the fourth cascade rinse is maintained at a high level (i.e. above 14 $M\Omega$).

(5) Final Rinse/Spin Dry - The last step in the wafer surface texturizing process is the final rinse/spin dry. The last remaining wafer surface contaminants are removed in this five minute cycle. The final rinse shall not be necessary in an optimized process (as was discussed in Step 4). The spin dry system can be replaced by a low-cost clean air tunnel drying system which is discussed in detail in reference (1).

(6) Texture Etching Rate, Time and Solution Concentration
Five experiments were performed to evaluate the texture etching rate, time and solution concentration for large area fine grain and coarse grain polysilicon and single crystal

silicon wafers. The experiments were designed around previous work performed on single crystal silicon solar cells.[1,5,10,12] The goal was to develop an optimized two-stage texturizing process for polysilicon solar cells.

Fine grain and coarse grain Wacker polysilicon wafers 5 cm x 5 cm were procurred along with Czochralski (100) as-cut four inch diameter round silicon wafers. Two wafers of each type were placed in a wafer carrier for each experiment. The single crystal (Cz) wafers served as the control wafers. The wafers were placed in the etching solutions for two minute time intervals. The polysilicon wafer thickness was measured in ten places with a micrometer caliper and the single crystal wafer thickness was measured in three places. The two wafer thicknesses of each type were averaged and the silicon removal calculated. The silicon removal versus time was plotted for each experiment and a discussion is given below.

The first two experiments were designed to evaluate the texture etching rate and time in a 20% NaOH by weight D.I. water solution, and to check the effect of a hot water and cold water rinse on the etching rate and time. Figure 6.1 gives the data for silicon removal versus time for wafers etched in 20% $NaOH/H_2O$ at 90^oC with a one minute rinse in cold water (15^oC) after every time interval. The initial etch rates are faster for all three types of wafers than for the intermediate and final etch rates as shown in Table 6.1.

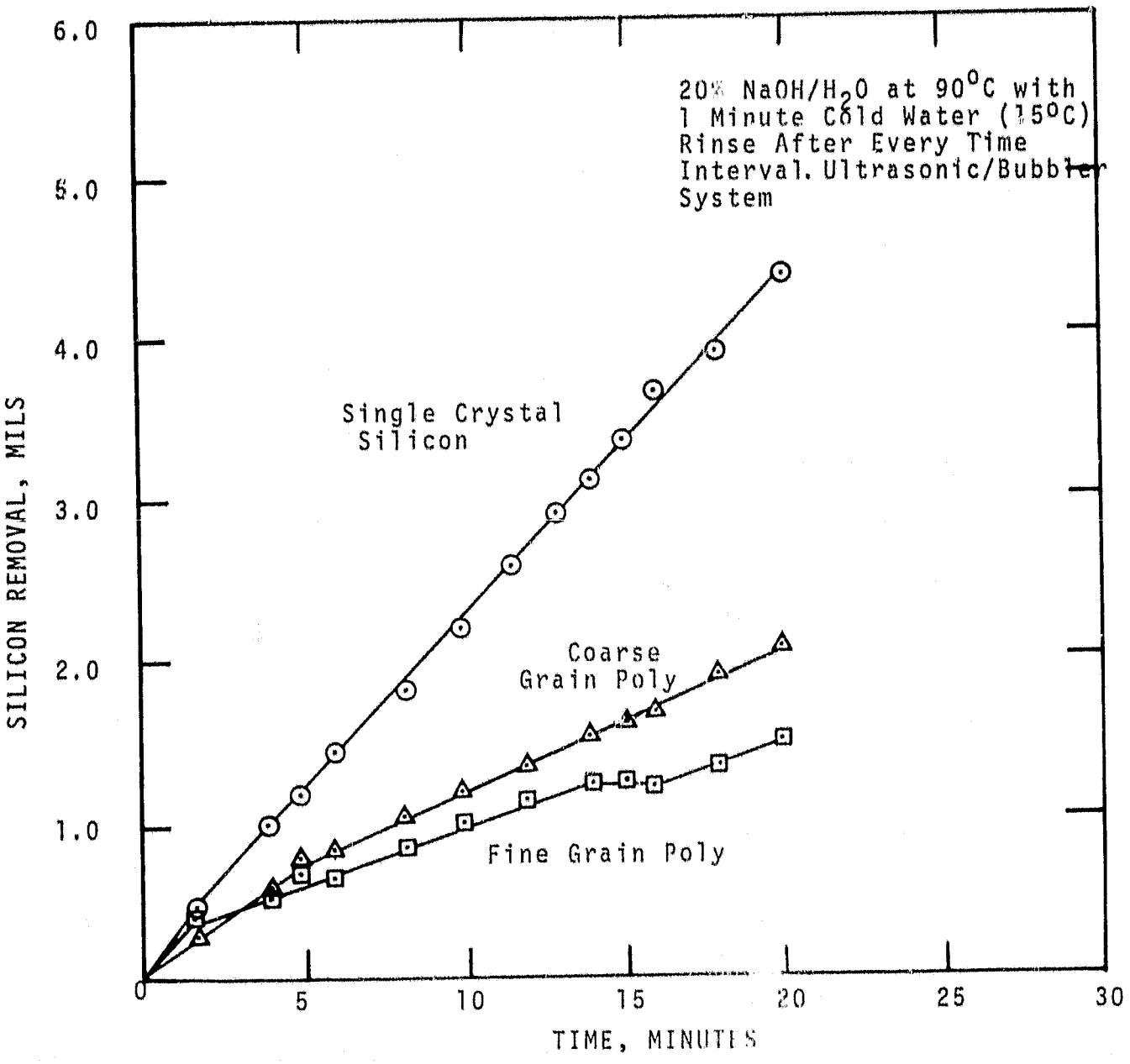


Figure 6.1 Silicon Texture Etching in 20% $NaOH/H_2O$ with 1.0 Minute Cold Water Rinse.

Table 6.1. Texture Etch Rate for Fine Grain and Coarse Grain Polysilicon and Single Crystal Silicon in 20% $NaOH/H_2O$ with Cold Water Rinse.

Category	Etch Rate in Mils/Min.		
	Fine Grain	Coarse Grain	Single Crystal
Initial	0.235	0.136	0.285
Intermediate	0.070	0.090	0.214
Final	0.067	0.090	0.214

The initial etch rate for fine grain polysilicon is faster than for coarse grain polysilicon, but it is slower than the etch rate for single crystal silicon. The intermediate and final etch rates are the same for each type of wafer. The etch rates increase from fine grain, to coarse grain, to single crystal silicon. At fourteen minutes the polysilicon wafers stopped etching while the single crystal wafers continued to etch. Etching started again after about sixteen minutes. This process characteristic may be due to placement of the wafers with respect to the bubbler and ultrasonic.

Figure 6.2 gives the data for silicon removal versus time for wafers etched in 20% (by weight) $NaOH/H_2O$ at 90^oC with a one minute rinse in hot water (80^oC) after every time interval. As shown in Table 6.2, the initial etch rates are faster for all three types of wafers than for the intermediate and final etch rates, and the initial etch rates are significantly faster for all three types of wafers placed into the hot water rinse than those put into the cold water rinse. The initial etch rate for the fine grain polysilicon is equal to the etch rate of the single crystal silicon and is higher than the coarse grain polysilicon.

After the first two minutes the etch rates change for all three types of wafers. The intermediate and final etch rates for the coarse grain and single crystal wafers are the same for each type of wafer. The coarse grain and single

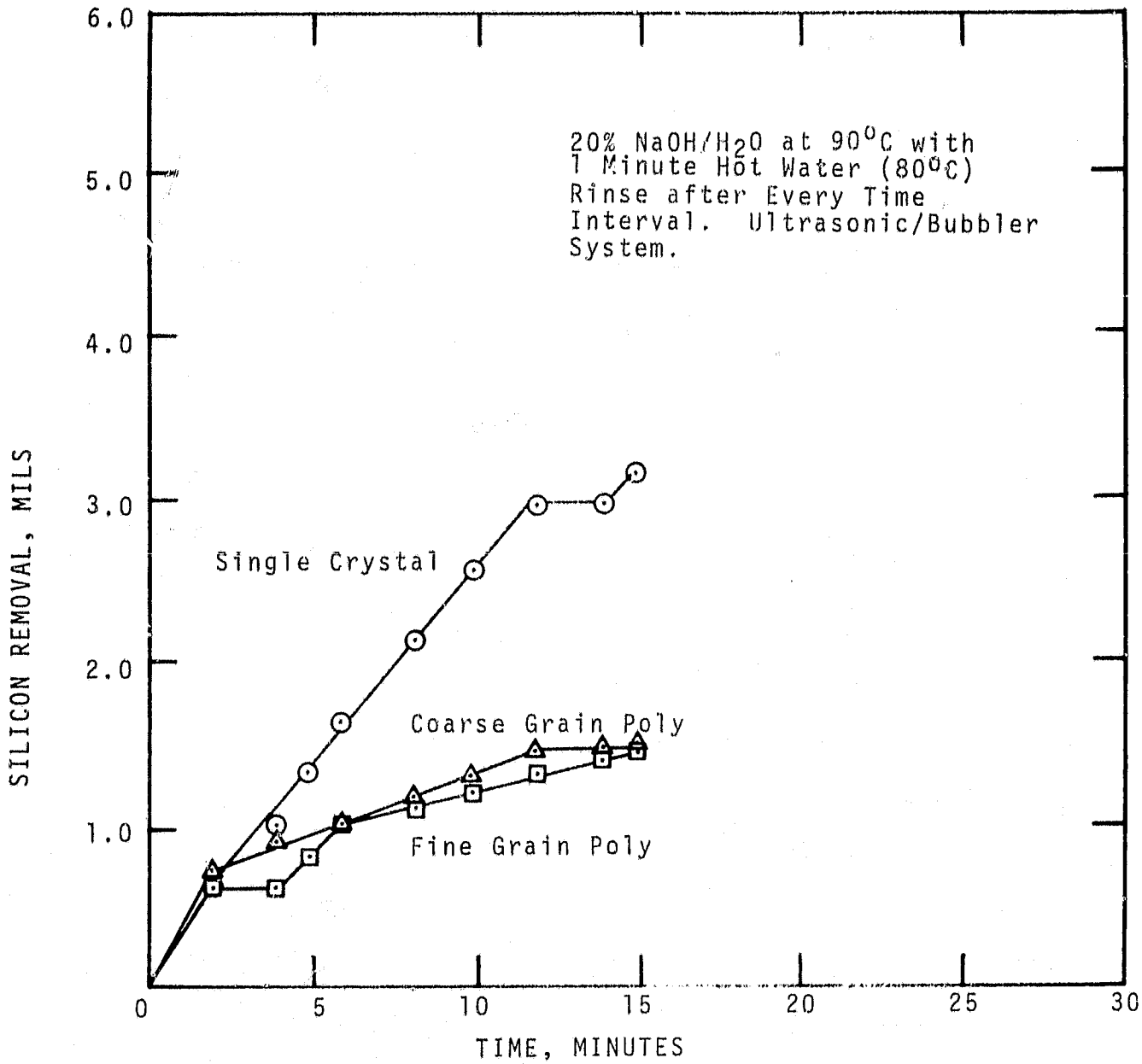


Figure 6.2 Silicon Texture Etching in 20% $NaOH/H_2O$ with 1.0 Minute Hot Water (80°C) Rinse.

Table 6.2. Texture Etch Rate for Fine Grain and Coarse Grain Polysilicon and Single Crystal Silicon in 20% NaOH in Hot Water Rinse.

Category	Etch Rate in Mils/Min		
	Fine Grain	Coarse Grain	Single Crystal
Initial	0.343	0.304	0.353
Intermediate	*	0.074	0.233
Final	0.055	0.074	0.231

*Insufficient data to determine meaningful amount.

crystal etch rates settled at their final etch rate after fourteen minutes.

The polysilicon and single crystal silicon intermediate and final etch rates are respectively slower and faster for the hot water rinse than for the cold water rinse. It can be said that the change in etch rates is more erratic for the polysilicon wafers using the hot water rinse than for the cold water rinse and, therefore, the data has a larger uncertainty. The difference between the hot and cold water rinse single crystal etch rates is small (about 8%) and could be considered nearly the same within the uncertainty limits of the data.

The third experiment examined the polysilicon and single crystal silicon texture etch rates in a solution of 10% NaOH by weight to D.I. water. Figure 6.3 gives the silicon removal data. The etch rates are listed in Table 6.3 for coarse grain polysilicon and single crystal silicon wafers. The initial etch rate for the polysilicon was faster than the intermediate and final etch rates. The single crystal etch rates did not change during the experiment.

The initial coarse grain polysilicon texture etch rate was slightly faster in the 10% $NaOH/H_2O$ solution than in the 20% $NaOH/H_2O$ solution, but the intermediate and final etch rates were nearly 30% slower. The initial single crystal silicon texture etch rate was 25% faster in the 20% $NaOH/H_2O$

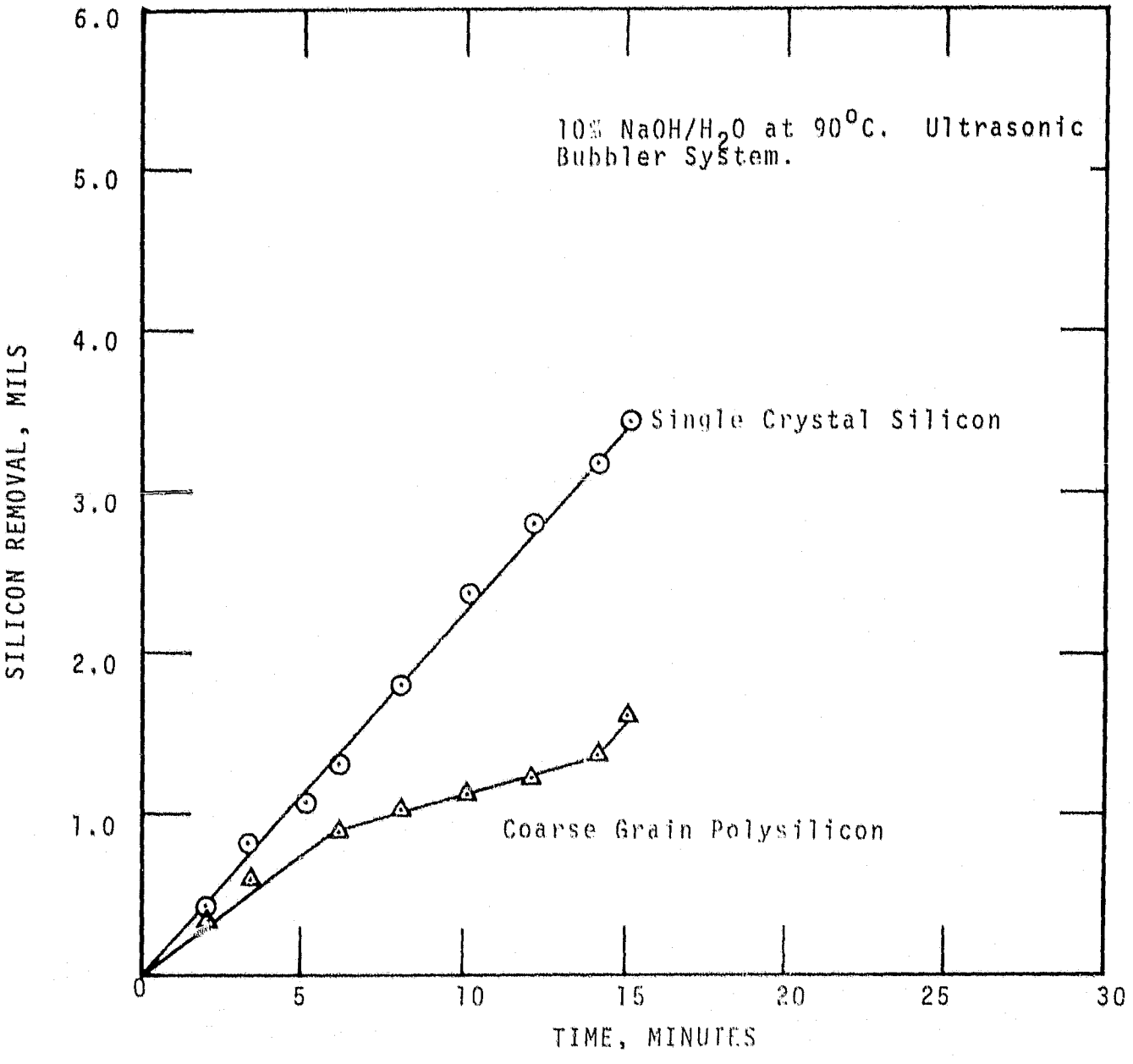


Figure 6.3 Silicon Texture Etching in 10% $NaOH/H_2O$

Table 6.3. Texture Etch Rate for Coarse Grain Polysilicon and Single Crystal Silicon in 10% $NaOH/H_2O$ with Cold Water Rinse.

Category	Etch Rate in Mils/Min	
	Coarse Grain	Single Crystal
Initial	0.153	0.228
Intermediate	0.064	0.228
Final	0.064	0.228

solution than in the 10% $NaOH/H_2O$ solution, but the intermediate and final etch rates were slightly slower. These results indicate that the 10% $NaOH/H_2O$ and the 20% $NaOH/H_2O$ texture etching solutions are suitable for removing surface damage and initiating pryamid formation with polysilicon and single crystal silicon. A five minute etching time is sufficient to assure the removal of surface damage (about 0.7 mils per wafer or 0.35 mils per wafer side) from the polysilicon wafers with either the 10% $NaOH/H_2O$ solution or the 20% $NaOH/H_2O$ solution. A solution of 20% $NaOH/H_2O$ was used in other polysilicon experiments to assure that the production solution was not depleted and that the proper thickness of silicon was removed in the five minute etching time.

The fourth and fifth experiments were designed to evaluate the texturizing rate and time for a two-stage texturizing process. The first stage served to texture etch saw damage (to remove saw damage and start pyramid formation) from the silicon wafers. The second stage served to texturize (to make sharp well defined and uniform pyramids) the silicon surface.

Figure 6.4 shows the data for silicon removal versus time for wafers texture etched in 20% $NaOH/H_2O$ at 90^oC and then texturized in 2% by weight $NaOH/H_2O$ at 95^oC. The texture etched wafers were processed in an ultrasonic/bubbler tank. Table 6.4 shows the texture etching rates for the

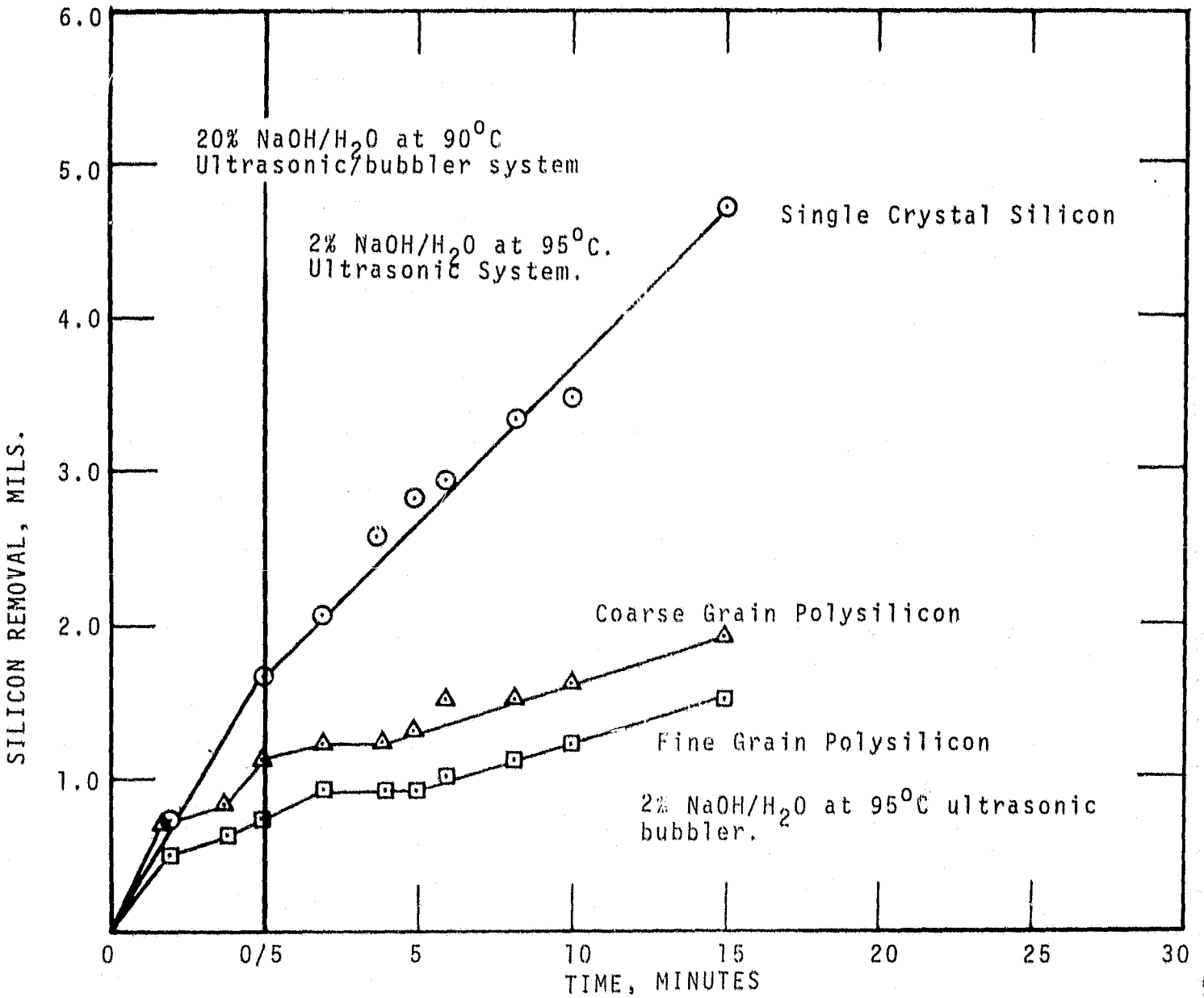


Figure 6.4 Silicon Texture Etching in 20% $NaOH/H_2O$ followed by Texturizing in 2% $NaOH/H_2O$.

Table 6.4 Texture Etch Rate and Texturizing Etch Rate for Fine and Coarse Grain Polysilicon and Single Crystal Polysilicon.

Category	Etch Rate in Mils/Min.		
	Fine Grain	Coarse Grain	Single Crystal
20% $NaOH/H_2O$ Texture Etching Solution for 5 minutes			
Initial	0.267	0.364	0.333
Intermediate	0.067	0.060	0.333
Final	--	--	0.333
2% $NaOH/H_2O$ Texturizing Solution + 1.0 minute cold water rinse per time interval.			
Initial	0.063	0.063	0.204
Intermediate	0.062	0.061	0.204
Final	0.062	0.061	0.204

wafers in the two solutions. Removal of 0.7 mils was achieved in the five minute step. The texturizing etch rates for both the polysilicon wafers and the single crystal wafers were very consistent and remained essentially unchanged during the fifteen minute process time. The fine grain and coarse grain polysilicon had identical texturizing rates in the 2% $NaOH/H_2O$ solution. The single crystal silicon had a significantly faster texturizing etch rate.

Figure 6.5 shows the data for silicon removal versus time for wafers texture etched in 20% $NaOH/H_2O$ at 90°C and then texturized in a solution of 2% $NaOH/H_2O$ with isopropyl alcohol at 95°C. Table 6.5 shows the etch rates for the wafers in the two solutions. The initial, intermediate and final texturizing etch rates for both the polysilicon and single crystal silicon wafers were very consistent during the thirty minute process time.

6.2 Surface Characteristics of Texture Etched and Texturized Polysilicon Wafers

The 20% $NaOH/H_2O$ and 10% $NaOH/H_2O$ solutions produced texture etched silicon wafers which are characterized as follows:

1. The fine grain and coarse grain polysilicon wafers, after five minutes in the texture etch solution were distinct and well defined. Most crystal grains were either shiny or light gray in appearance. The crystal grains were more distinct with a three dimensional appearance and were either shiny, light gray, or gray after fifteen to twenty minutes in the texture etch solution.

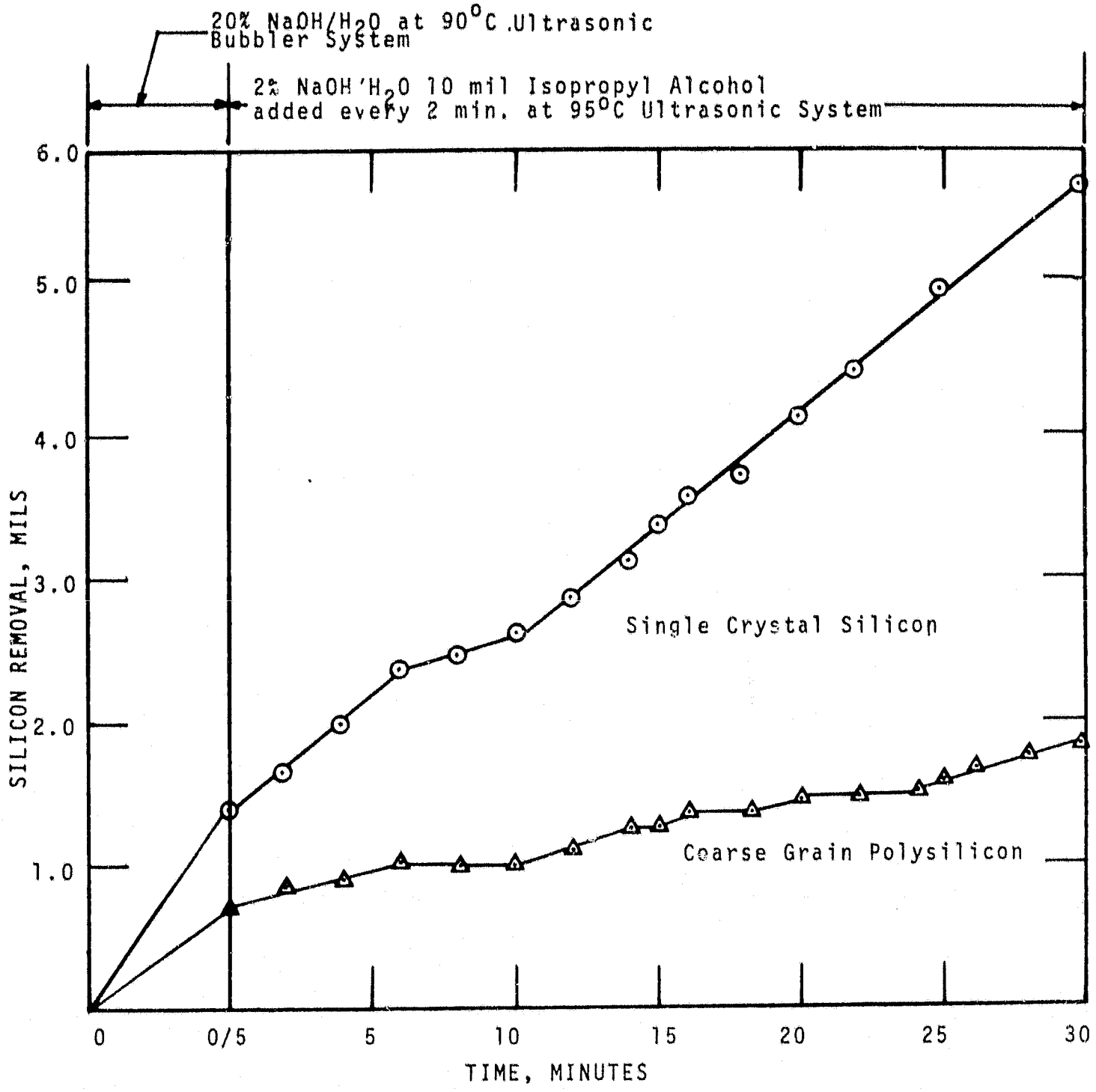


Figure 6.5 Silicon Texture Etching in 20% $NaOH/H_2O$ Followed by Texturizing in 2% $NaOH/H_2O$ with Isopropyl Alcohol.

Table 6.5 Texture Etch Rate and Texturizing Etch Rate for Fine and Coarse Grain Polysilicon and Single Crystal Polysilicon in Isopropyl Alcohol.

Category	Etch Rate in Mils/Min.	
	Coarse Grain	Single Crystal
20% $NaOH/H_2O$ Texture Etching Solution for 5 minutes.		
Average	0.133	0.289
2% $NaOH/H_2O$ + isopropyl alcohol + 1.0 min. cold water rinse per time interval.		
Initial	0.055	0.160
Intermediate	0.048/0.052	0.159
Final	0.053	0.159

2. The single crystal silicon wafers, after five minutes in the texture etch solution, were light gray in appearance and had a uniform distribution of surface macrostructures. The wafers were darker gray in appearance, after fifteen to twenty minutes in the texture etching solutions, and had uniform surface macrostructures.

The two-stage surface macrostructure process that utilized 20% $NaOH/H_2O$ and 2% $NaOH/H_2O$ produced texture etched silicon wafers which are characterized as follows:

1. After fifteen minutes in the 2% $NaOH/H_2O$, the polysilicon wafers were texture etched, except at the edges of the wafers. The polycrystals were well defined and varied in appearance from gray to shiny and were three dimensional from grain-to-grain.
2. The single crystal wafers were texturized after fifteen minutes in the 2% $NaOH/H_2O$ solution. The surfaces were dark gray and had uniform pyramidal surface macrostructure.

The two-stage surface macrostructure process, that utilized 20% $NaOH/H_2O$ and 2% $NaOH/H_2O$ with isopropyl alcohol, produced texturized silicon wafers which are characterized as follows:

1. After ten minutes in the 2% $NaOH/H_2O$ with isopropyl alcohol, some of the polycrystals were black, some dark gray, and some gray.
2. After ten minutes in the texturizing solution, the single crystal wafers were gray and getting dark.

3. After fifteen minutes, about 15% to 20% of the polycrystals were dark gray and were well defined. Most of the texturized polysilicon crystal grains were located in the center region of the wafer. The elongated crystal grains located on the outer edges of the wafer (about 45% of the surface area) were texture etched dark gray and gray indicating a different crystal orientation than (100) which is not suitable for NaOH texturization.
4. After fifteen minutes, the four inch diameter single crystal wafers were uniformly texturized and were dark gray in appearance.

6.3 Optimized Texturizing Process

An optimum polysilicon texturizing process was developed from the work performed and reported in other studies[1,5,10,11,12] and from the work performed in this program. The basic wafer surface texturizing process is detailed in Section 6.1. The optimized texturizing process is given below with specific detail given to the two-stage wafer surface texturizing step.

Wafer Surface Cleaning

5 minutes in ultrasonic vapor degreaser with boiling Freon TMS.

5 minutes in second degreaser tank with vapor zone.

Two-Stage Wafer Surface Texturizing

5 minutes etch in 20% $NaOH/H_2O$ at $90^oC \pm 2^oC$ with ultrasonics and clean air bubbler[2] ($10 \ell/m^2/min$).

15 minute texturizing in 2% $NaOH/H_2O$ with 20% isopropyl alcohol at $95^oC \pm 2^oC$ with ultrasonics.

Four-Stage Cascade Rinse

5 minutes in each of four stages with cascade D.I. water with resistance monitor and replenishment control (this eliminates additional cleaning step and final spin rinse).

Hot Air Tunnel Drying

5 minutes in clean air blow drying tunnel system. (See reference 1. This eliminates the spin dry system.)

7.0 DIFFUSION PROCESS CONSIDERATIONS

The purpose of this task is to investigate the feasibility of improving the polysilicon solar cell, short-circuit current I_{sc} with variation of the $POCl_3$ diffusion process. Six batches of Wacker polysilicon solar cells were processed to investigate the electrical performance for various diffusion parameters. The solar cells were processed with the standard production process, Figure 3.1, which includes isotropic surface etching, $POCl_3$ diffusion, aluminum evaporation and nickel plating. The phosphorous glass was removed from the cells prior to testing. Electrical performance results are given in Table 7.1. The diffusion time and temperature for each batch are listed below:

Batch 3A	$POCl_3$	800°C	70 min.
3B	"	800°C	35 "
3C	"	875°C	35 "
3D	"	875°C	25 "
3E	"	900°C	35 "
3F	"	925°C	30 "

Batch 3A exhibited the highest average I_{sc}, V_{oc}, I_{pp} and η. It also exhibited a high sheet resistance and a low peak power voltage. Batch 3D exhibited a slightly

Table 7.1 Effect of $POCl_3$ Diffusion Time and Temperature Schedules for Wacker Polycrystalline Cells. (25 Cells per Batch)

	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF	R(Ω/□)
Wacker Polysilicon, 3A, S.E., $POCl_3$, 800°C 5-60-5.							
High	0.400	0.550	0.355	0.415	6.5	0.670	
Average	0.390	0.545	0.345	0.415	6.3	0.674	69.2
Wacker Polysilicon, 3B, S.E., $POCl_3$, 800°C 5-25-5.							
High	0.386	0.550	0.325	0.417	5.9	0.638	
Average	0.378	0.540	0.275	0.415	5.0	0.559	75.3
Wacker Polysilicon, 3D, S.E., $POCl_3$, 875°C, 5-15-5.							
High	0.384	0.550	0.352	0.430	6.6	0.717	
Average	0.378	0.545	0.330	0.430	6.2	0.689	24.0
Wacker Polysilicon Batch 3C, $POCl_3$, 875°C 5-25-5, Glass Removed .2-3 Ωcm. Active area=22.8 cm^2.							
High	0.373	0.540	0.320	0.450	6.3	0.715	
Average	0.370	0.525	0.315	0.430	6.1	0.719	26.8
Wacker Polysilicon, 3E, S.E., $POCl_3$, 900°C 5-25-5.							
High	0.365	0.540	0.325	0.435	6.2	0.717	
Average	0.353	0.520	0.315	0.435	6.0	0.746	16.0
Wacker Polysilicon Batch 3F, S.E., $POCl_3$, 925°C, 5-20-5.							
High	0.340	0.535	0.300	0.430	5.7	0.709	
Average	0.325	0.525	0.275	0.425	5.1	0.685	10.2

lower I_{sc}, I_{pp} and η. It also exhibited a high sheet resistance and a low peak power voltage. Batch 3D exhibited a slightly lower I_{sc}, I_{pp} and η and had a much lower sheet resistance which led to a higher V_{pp} and fill factor.

These trends in specific electrical characteristics are similar to those generally observed when single crystal CZ material is utilized. The major difference is a reduction in the overall I-V characteristic of polycrystalline as compared to single crystal material. The reduced generation currents (versus expected single crystal equivalant diffusion schedule values) are not unexpected when viewed from the perspective of the modified diffusion length model as discussed earlier. Similarly, the obtained open circuit voltage values are less than those of similar base resistivity single crystal material, when subjected to equivalent diffusion schedules.

This initial grouping of data indicates that the optimum $POCl_3$ diffusion schedule is similar (if not identical) for polycrystalline and single crystal materials.

8.0 OTHER PROCESS EFFECTS

Several other solar cell process methods were investigated for the purpose of identifying low-cost techniques and procedures which might improve polysilicon solar cell efficiencies. Figure 8.1 shows a block diagram with several new optional process steps including gettering, spray-on n^+ polymer dopants, and printed aluminum. A brief discussion of each of these process steps and their effects are presented below.

8.1 $POCl_3$ Gettering Study

Phosphosilica glass gettering has been used for some time to remove unwanted electrically active impurities from silicon wafers.[13] The grain boundaries in polysilicon wafers are planar crystallographic defects which may contain a large amount of residual impurities. For this reason, it appeared worthwhile to investigate the usefulness of including a gettering treatment in polysilicon solar cell fabrication.

8.1.1 Pregettering Effects

Two batch experiments were performed with 3.94 inch square, 15.7 mil thick Wacker polysilicon wafers. Batch P-101 was processed using the sequence given in Figure 8.1 with pregettering, phosphorous diffusion, aluminum evaporation, edge grinding, and no antireflective coating (but with a phosphorous glass which has an antireflective effect). A second Batch P-102 was processed with the same sequence as Batch

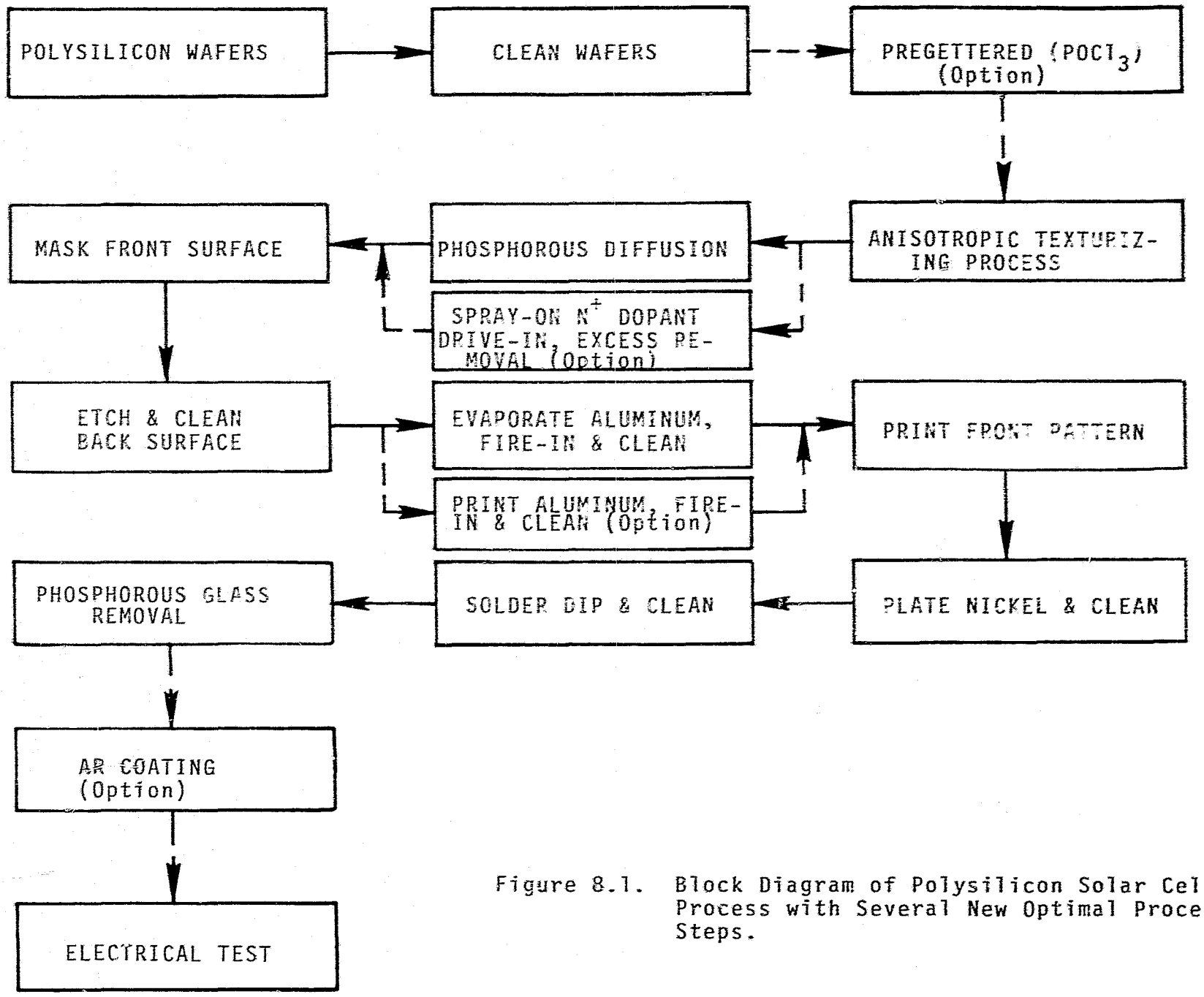


Figure 8.1. Block Diagram of Polysilicon Solar Cell Process with Several New Optimal Process Steps.

P-101 except that the phosphorous glass was removed and an SiO antireflective coating added. The electrical performance for Batches P-101 and P-102 are shown in Figures 8.2 and 8.3, respectively, and the pregettering effects are given in Table 8.1

The pregettering effects are apparent when compared to the electrical effects of non-gettered polysilicon solar cells. For example, by comparing the pregettered Batch P-102 with the nongettered Batch P-100 (see Section 3.0) one observes a significant improvement in efficiency, peak power voltage, and fill factor. The gettered surface was removed by the texture etching step; the etching time (20 minutes) was sufficiently long to remove the entire gettered surface as shown in Section 6.0. The gettering (removal of impurities) effect is apparent. It appears that the inclusion of a pregettering step in the process sequence will enhance the polysilicon solar cell power output.

8.1.2 Intermediate Gettering Effects

A $POCl_3$ gettering treatment in combination with a two-stage texturizing process sequence was shown to be an effective method for producing high efficiency single crystal silicon solar cells.[1] In particular, it was found that the placement of a $POCl_3$ gettering step between the two sequential texturizing steps (intermediate gettering) provides a higher efficiency improvement than gettering prior to the texturization process for single crystal silicon solar cells. Since

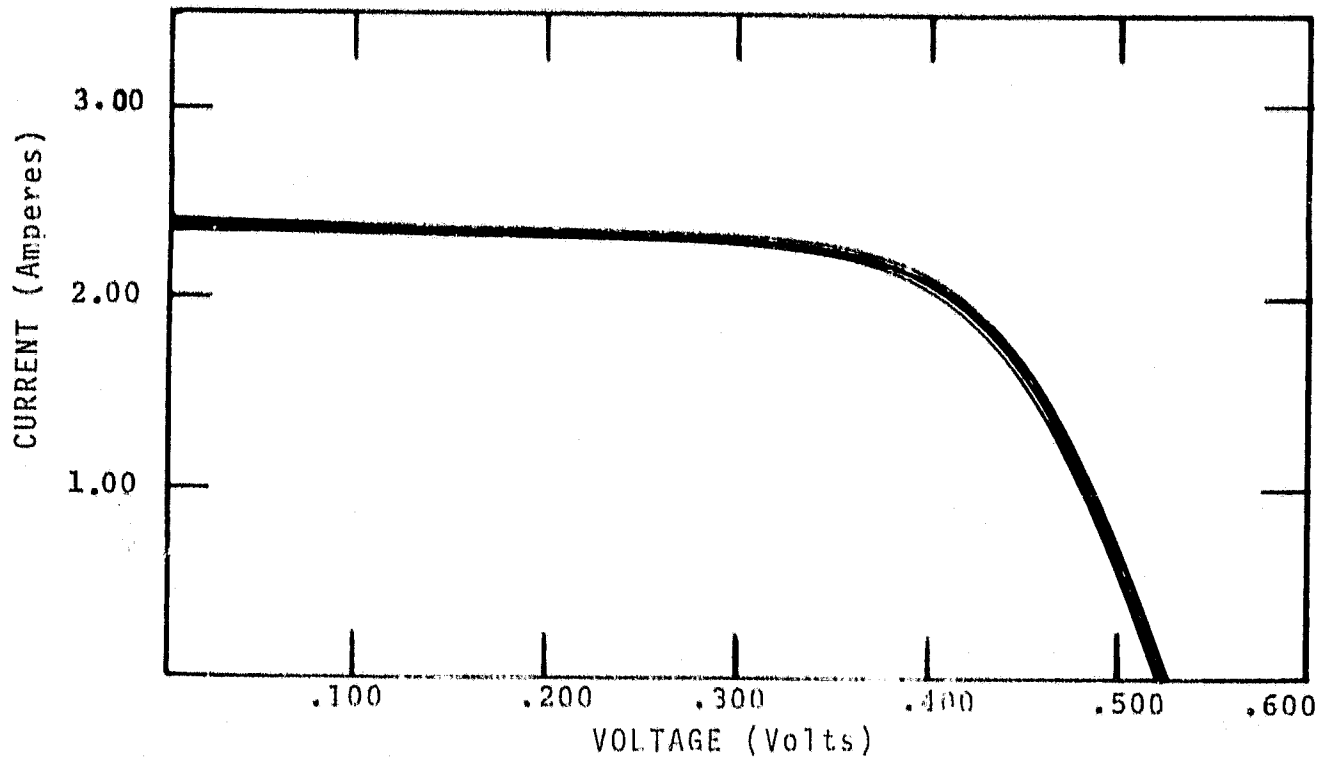


Figure 8.2 Electrical Performance of Pregettered Wacker Polysilicon Solar Cells Batch P-101.

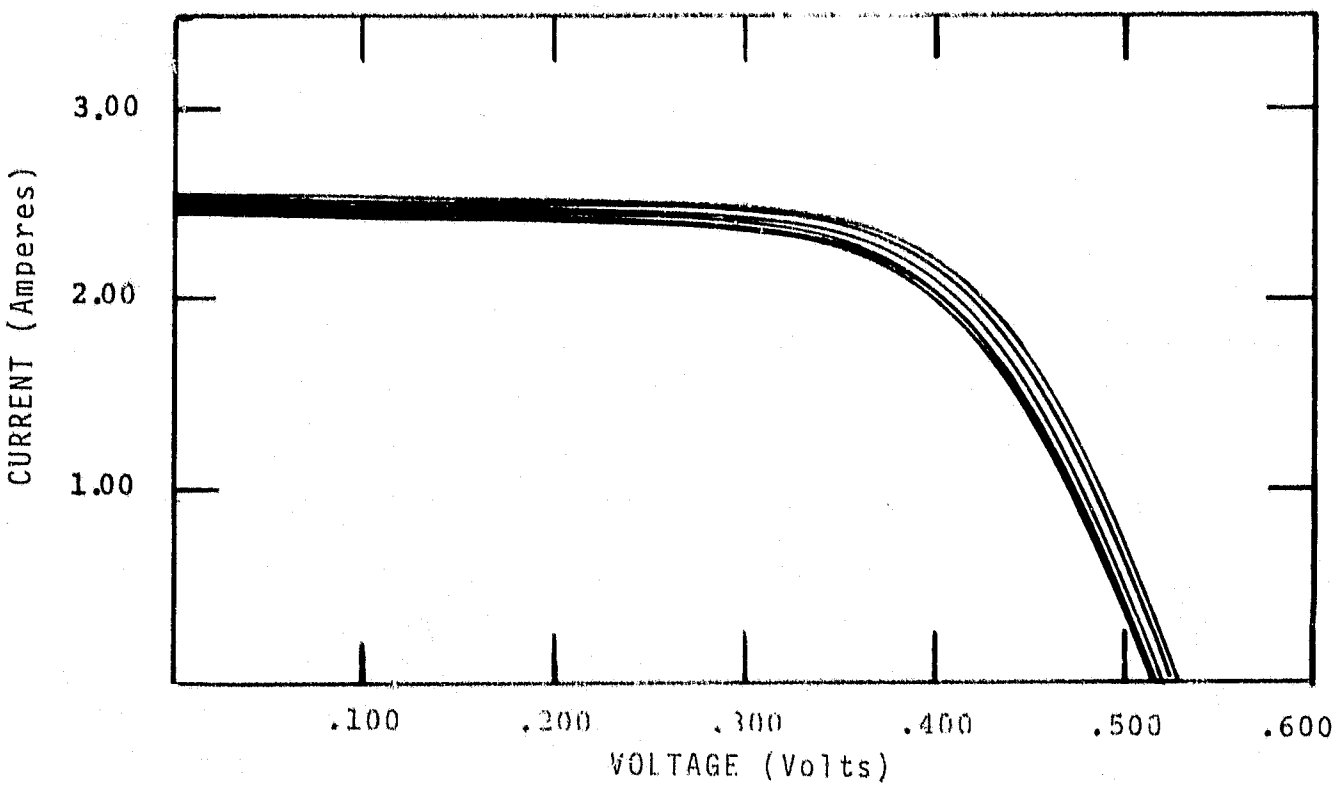


Figure 8.3 Electrical Performance of Pregettered Wacker Polysilicon Solar Cells with SiO, Batch P-102.

Table 8.1 Pregettering Effects on Large Area Polysilicon Solar Cells (25 Cells per Batch).

BATCH	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF	$\frac{\Delta\eta}{\eta}$(%)	$\frac{\Delta FF}{FF}$(%)
P-101	Wacker Polysilicon-Pregettering ($POCl_3$, 900°C, 45 min.), Texture Etch (20% $NaOH/H_2O$, 20 min.), $POCl_3$ Diffusion (900°C, 35 min.), Phos. glass on, Active area 92.7 cm^2.							
1	2.4	0.525	2.10	0.400	9.10	0.667	+1.70%	+1.37%
2	2.4	0.525	2.10	0.390	8.83	0.650	-1.30%	-1.22%
Ave.	2.4	0.525	2.10	0.395	8.95	0.658		
P-102	Wacker Polysilicon Pregettering Texture Etch, Diffusion (see P-101), Phos. Glass Removed, SiO AR Coating Added, Active Area 92.7 cm^2.							
High	2.60	0.525	2.20	0.410	9.73	0.661	+3.50%	+0.61%
Low	2.50	0.515	2.10	0.400	9.06	0.652	-3.51%	-0.761
Wt.Ave.	2.55	0.520	2.15	0.405	9.40	0.657		

the attainment of high efficiency polysilicon solar cells is a vital component of this program, an intermediate gettering study was performed on polysilicon wafers. This study proceeded by comparing intermediate gettering with pregettering.

Three batch tests were performed in this task. Batches P-230 and P-231 were processed using the baseline solar cell fabrication sequence shown in Figure 8.1 with $POCl_3$ pregettering. Batch P-220 was processed using the baseline fabrication sequence with intermediate gettering. The electrical performance data for each batch test is shown in Table 8.2. The average efficiency, 8.69%, of the pregettered Batch P-230 is slightly higher than the average efficiency, 8.39%, of the intermediate gettered Batch P-220. The current collection (I_{sc} and I_{pp}) also appears to be slightly higher for the pregettered solar cells than for the intermediate getter solar cells; the average peak power voltage remained essentially the same. One possible cause could be that the texturizing process does not adequately remove and/or texture the diffused surface in the time allotted for the 2% NaOH/H_2O solution in the intermediate gettering process for the polysilicon material.

An investigation of the texture etching rates for a diffused surface of a polysilicon wafer was not explored in this program. It is recommended that an indepth study be made in this area which could lead to a substantial improvement in polysilicon solar cell efficiency.

Table 8.2 Intermediate Gettering and Pregettering Effects on Large Area Polysilicon Solar Cells.

BATCH	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF	$\frac{\Delta\eta}{\eta}$(%)	$\frac{\Delta FF}{FF}$(%)
P-220 Wacker Polysilicon-Texture Etch (20% NaOH/H_2O, 10 min.), Intermediate Gettering ($POCl_3$, 900°C, 45 min.), Texturize (2% NaOH/H_2O, 10 min.), $POCl_3$ Diffusion (900°C, 35 min.), Phos. Glass on, Active Area 92.7 cm^2.								
1	2.40	0.525	2.05	0.400	8.85	0.651	+5.48	+1.88
2	2.25	0.525	1.90	0.385	7.89	0.619	-5.95	-3.13
Ave.	2.32	0.525	1.98	0.393	8.34	0.639		
P-230 Wacker Polysilicon-Pregetter ($POCl_3$, 900°C, 45 min.), Texture Etch (20% NaOH/H_2O, 20 min.), $POCl_3$ Diffusion (900°C, 35 min.), Phos. Glass on, Active Area 92.7cm^2.								
1	2.55	0.525	2.10	0.410	9.29	0.643	+6.90	+6.11
2	2.55	0.520	2.05	0.385	8.51	0.595	-2.07	-1.82
3	2.55	0.520	2.00	0.385	8.31	0.580	-4.37	-4.29
Ave.	2.55	0.522	2.05	0.393	8.69	0.606		
P-231 Wacker Polysilicon-Pregetter ($POCl_3$, 900°C, 35 min.), Texture Etch (20% NaOH, 15 min.), $POCL_3$ Diffusion (900°C, 25 min.), Phos. Glass on, Active Area 92.7 cm^2.								
1	2.45	0.530	2.15	0.410	9.51	0.679	--	--

8.2 Spray-on Dopant Junction Formation

Spray-on dopant junction formation was shown to be a low-cost solar cell processing technique for single crystal silicon solar cells.[12] This process method was found to yield solar cell efficiencies comparable to the efficiencies of $POCl_3$ diffused solar cells. Since the fabrication of low-cost polysilicon solar cells is an important goal of this project, the spray-on dopant junction formation process was evaluated for polysilicon material.

The solar cells produced in this task followed the process sequence given in Figure 8.1 with pregettering ($POCl_3$, 900°C, 45 minutes), texture etching (20% $NaOH/H_2O$, 20 minutes), spray-on n^+ dopant junction formation, and SiO antireflective coating. The electrical performance curves for the spray-on doped 3.85 inch square Wacker polysilicon solar cells, Batch P-400 are presented in Figure 8.4 and the parameter data are given in Table 8.3.

The highest efficiency achieved from the n^+ spray-on-doped polysilicon solar cell batch was 10.87%. The average efficiency in this batch of thirteen solar cells was 10.41%. For comparison, the average efficiencies of all previous batch tests ranged from 7.61% for the baseline fabrication sequence to 9.4% for the pregettered, $POCl_3$ diffused Batch P-102, with SiO AR Coating. It is clear that the use of spray-on-dopant junction formation has led to a significant efficiency improvement for Wacker polysilicon solar cells.

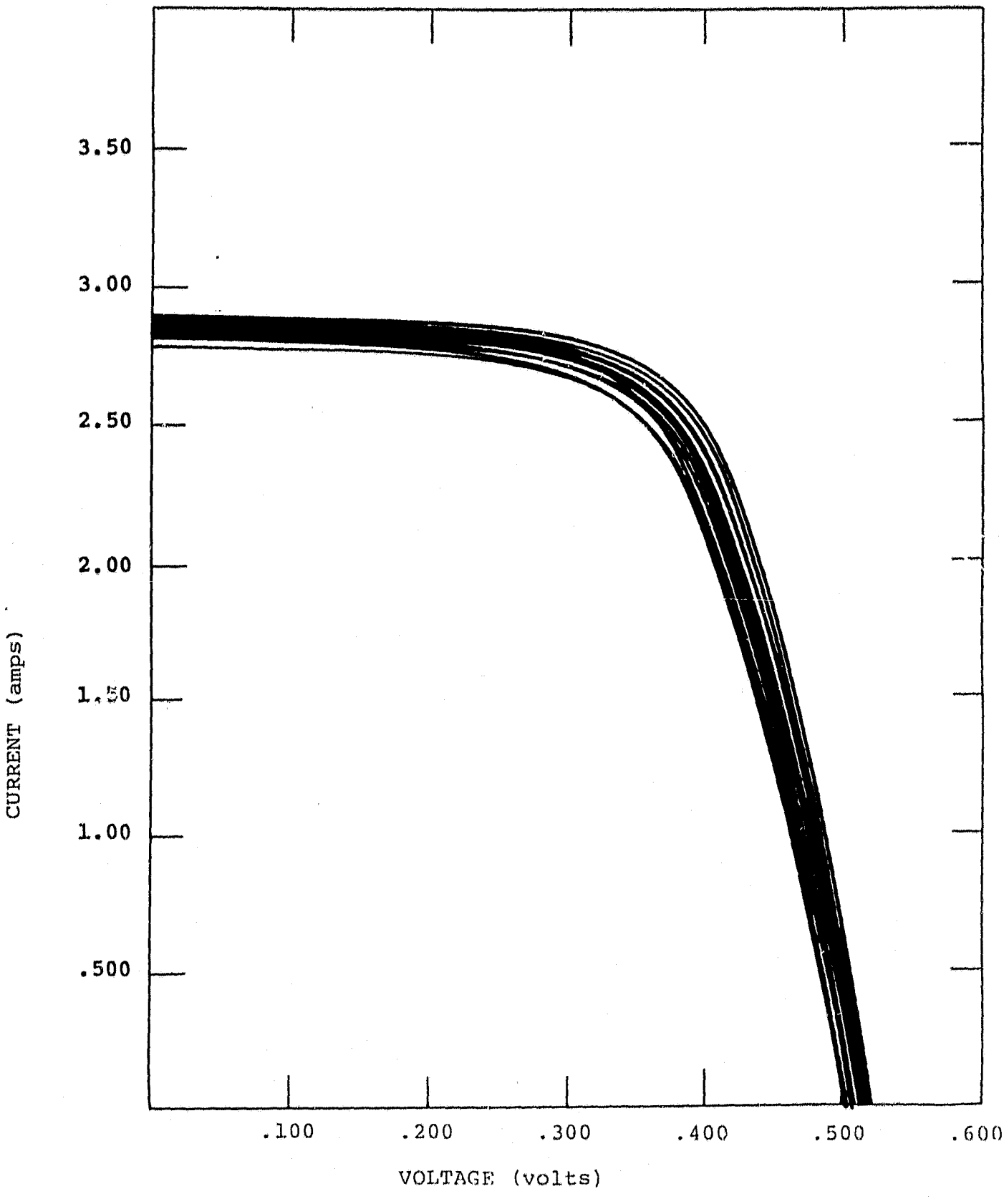


Figure 8.4 Electrical Performance of Spray-on n^+ Doped Wacker Polysilicon Solar Cells with SiO AR Coating, Batch P-400.

Table 8.3. Spray-on n^+ Dopant Junction Formation Effects on Large Area Polysilicon Solar Cells. (25 Cells per Batch)

BATCH	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η (%)	FF	$\frac{\Delta\eta}{\eta}$(%)	$\frac{\Delta FF}{FF}$(%)
P-400	Wacker Polysilicon-Pregettering ($POCl_3$, 900°C, 45 min.), Texture Etch (20% $NaOH/H_2O$, 20 min.), Spray on n^+ Dopant, SiO Coating. Active Area 92.7 cm^2.							
High	2.875	0.525	2.55	0.395	10.87	0.667	+4.42	+1.52
Low	2.800	0.510	2.45	0.375	9.91	0.643	-4.80	-2.13
Average	2.825	0.520	2.475	0.390	10.41	0.657		

The outcome of the spray-on dopant junction formation study with Wacker polysilicon material provided several encouraging results. It was demonstrated that 10% efficient polysilicon solar cells in batch quantity can be achieved by utilizing the fabrication sequence in Figure 8.1 with pregettering, spray-on n^+ dopant junction formation, and SiO AR coating. This result fulfills one of the goals of this program, which is, the production in batch quantity of 10% efficient polysilicon solar cells. In addition, the low cost of the spray-on-dopant junction formation process[12] provides yet another advantageous reason for its use with Wacker polysilicon material.

8.3 Printed and Evaporated Aluminum Effects on $POCl_3$ Diffused Polysilicon and Single Crystal Silicon Solar Cells

Printed aluminum has been shown to be an effective low-cost technique for producing a p+ back surface field for single crystal solar cells.[14,15,16] Experiments were performed in this task to observe the effects of printed and evaporated aluminum on $POCl_3$ diffused polysilicon and single crystal silicon solar cells.

Two Batches (2B and 3B) of polysilicon wafers and one control Batch 2D of single crystal wafers were processed together except for the printed and evaporated steps. The wafers were processed according to the block diagram in Figure 8.1 with pregettering ($POCl_3$, 900°C, 45 min.), diffusion ($POCl_3$

875°C, 30 min.), the appropriate aluminum metallization step, and phosphorous glass removal (no AR coating). The evaporated aluminum was fired-in at 800°C for 10 minutes, which was 50°C higher than for the standard process. The printed aluminum used the Spectrolab process[17, 18] and was fired in a diffusion tube at 875°C for one and one-half minutes. The active area of the polysilicon solar cells was 22.8 cm^2. The active area of the single crystal solar cells was 42.6 cm^2.

The printed and evaporated aluminum effects on $POCl_3$ diffused polysilicon and single crystal silicon solar cells are shown in Table 8.4. The electrical parameters for the evaporated aluminum solar cells were in general higher than for the printed aluminum cells. The printed aluminum solar cells were characterized by shunting and low fill factor. This indicates a lack of sufficient control during the printed aluminum process step. Both metallization processes improved the open-circuit voltage and peak power voltage of the polysilicon solar cells over the standard processed cells. The polysilicon voltage parameters remain significantly lower than the single crystal control solar cells. The efficiency of the polysilicon solar cells was observed to be about 40% lower than the efficiency of the single crystal solar cells.

8.4 Printed and Evaporated Aluminum Effects on Spray-on n^+ Doped Polysilicon and Single Crystal Silicon Solar Cells

Experiments were performed on this task to observe the

Table 8.4 Printed and Evaporated Aluminum Effects on $POCl_3$ Diffused Polysilicon and Single Crystal Silicon Solar Cells (25 Cells per Batch).

BATCH		I_{sc}(a)	V_{oc}(V)	I_{pp}(a)	V_{pp}(v)	η(%)	FF
2B	Poly Evaporated Aluminum	0.408	0.525	0.330	0.430	6.2	0.662
3B	Poly Printed Aluminum	0.410	0.515	0.300	0.420	5.5	0.596
	% Difference	+0.5	-1.9	-9.1	-2.3	-11.3	-10.0
2D	CZ Evaporated Aluminum	1.160	0.570	1.020	0.460	11.0	0.710
2B	Poly Evaporated Aluminum	0.408	0.525	0.330	0.430	6.2	0.662
	% Difference	--	+7.9	--	+6.5	+43.6	+6.7

effects of printed and evaporated aluminum on spray-on n^+ doped polysilicon and single crystal silicon solar cells. Two Batches (2A and 4A) of polysilicon wafers and two Control Batches (2C and 4C) of single crystal wafers were processed together except for the printed and evaporated steps. The wafers were processed according to the block diagram in Figure 8.1 with pregettering ($POCl_3$, 900°C, 45 min.), spray-on n^+ (drive-in, 925°C, 20 min.) the appropriate aluminum metallization step, and phosphorous glass removal (no AR coating). The evaporated aluminum was fired-in at 800°C for 10 minutes. The printed aluminum used the Spectrolab process[17, 18] and was fired in a diffusion tube at 875°C for one and one-half minutes.

The printed and evaporated aluminum effects on the spray-on n^+ polysilicon and single crystal silicon solar cells are shown in Table 8.5. The electrical performance parameters for the evaporated aluminum and printed aluminum solar cells were in close agreement. Both metallization processes improved the open-circuit voltage and peak power voltage of the polysilicon solar cells over the standard processed cells. The polysilicon voltage parameters remained significantly lower than the single crystal control solar cells. The efficiency of the polysilicon solar cells was observed to be about 40% lower than the efficiency of the single crystal solar cells.

Table 8.5. Printed and Evaporated Aluminum Effects on Spray-on n^+ Doped Polysilicon and Single Crystal Silicon Solar Cells(25 Cells per Batch).

BATCH		I_{sc}(a)	V_{oc}(V)	I_{pp}(a)	V_{pp}(v)	η(%)	FF
2A	Poly Evaporated Aluminum	0.385	0.525	0.320	0.415	5.8	0.657
4A	Poly Printed Aluminum	0.400	0.510	0.320	0.410	5.8	0.643
	% Difference	-3.9	+2.9	0	+1.2	0	+2.1
2C	CZ Evaporated Aluminum	0.950	0.565	0.840	0.465	9.2	0.728
4C	CZ Printed Aluminum	1.080	0.570	0.900	0.465	9.8	0.680
	% Difference	-13.7	-0.9	-7.1	0	-6.5	+6.6

The electrical performance results from this section and section 8.3 show that the use of a p^+ material for forming an effective back surface field improves the voltage parameters of polysilicon solar cells. The use of spray-on n^+ dopants was also shown to be a very effective junction formation technique.

9.0 SELECTED PROCESS AND RESULTS

A polysilicon solar cell process sequence was selected from the results of the work discussed in previous sections of this report. The selected process is outlined in Figure 9.1. The process flow is indicated by solid arrows. Alternative process steps are indicated by dashed arrows. A discussion of the selected manual process is given below.

The large area polysilicon wafers were sample inspected and then cleaned in a two-stage ultrasonic vapor degreaser which utilizes recycled Freon. The clean wafers were pre-gettered in the second step in the process sequence. This optional step may not be necessary if the "quality"[1] of the polysilicon material is improved in the future. The pre-gettering process included a diffusion step followed by a texture etching step. The diffusion was performed with $POCl_3$ at $900^{o}C$ for 45 minutes. The anisotropic etching step utilized 20% $NaOH/H_2O$ at $90^{o}C$ in an ultrasonic/bubbler system for 5 minutes. A 10% $NaOH/H_2O$ solution was shown in Section 6.2 to have nearly the same etch rate as 20% $NaOH/H_2O$ and is preferred because of lower material cost. A five minute texture etch was shown to be adequate to remove the gettered surface. However, the etch rate was not tested in large-scale polysilicon production.

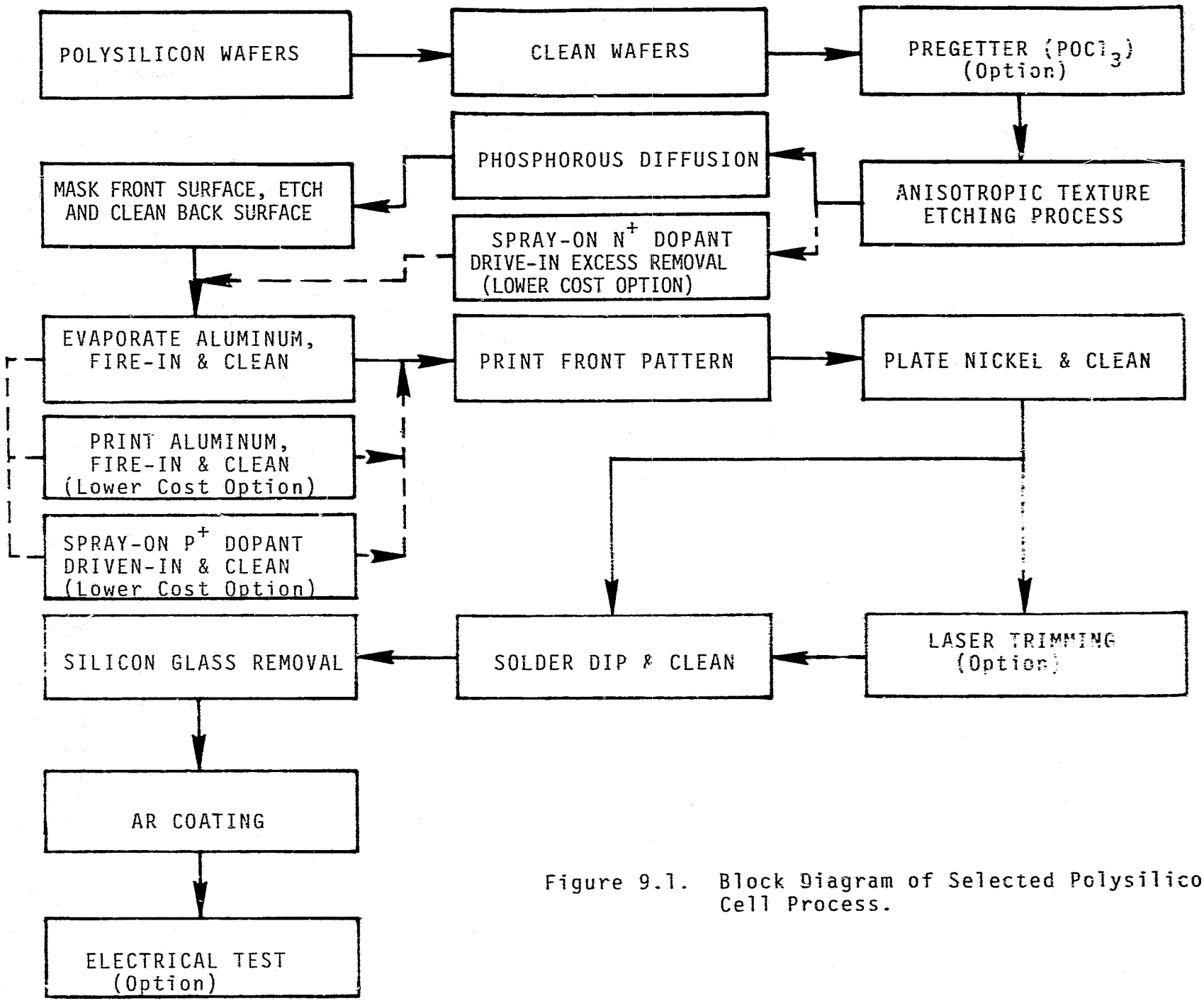


Figure 9.1. Block Diagram of Selected Polysilicon Cell Process.

A p-n junction was formed in the next step in the selected process sequence. Two methods were found to be suitable. They are $POCl_3$ diffusion and spray-on n^+ polymer dopants. The diffusion step is a standard technique. The diffusion was carried out in $POCl_3$, at 900°C for 35 minutes. Diffusion forms an n^+-p-n^+ structure which requires removal of the back surface. Therefore, the front surface was masked with a resistive ink and the back surface was removed in an HNO_3/HF/water solution. These two steps add to the cost of the process and are not desirable for a low-cost process sequence. A potential process substitution is plasma edge etch (to delineate the n^+-p junction and use of the aluminum back layer to neutralize the back n^+ layer.

The spray-on n^+ polymer dopant process step is preferred over the diffusion process due to lower cost. Emulsitone's N-250 polymer dopant with a concentration of 2×10^{18} atoms/cm^3 was utilized. The spraying technique is discussed in detail in reference.[19] The dopant was driven-in with the furnace at 925°C in an oxygen-nitrogen atmosphere for 20 minutes. The excess dopant was removed in an HF/water solution. Dopant material that may overlap the edges of the wafer can be removed (after nickel plating) by laser trimming,[12] edge grinding, or plasma etching.[20] Front surface masking and the back etch are eliminated with the spray-on dopant process.

A p+ back surface can be produced with any one of four techniques: evaporated aluminum, printed aluminum, spray-on p+ polymer dopant;[12] and spray-on aluminum.[21] For control purposes, evaporated aluminum was used in the development process. It was fired-in at 800°C in a hydrogen-nitrogen atmosphere. The three other processes are much lower in cost and are preferred in a large-scale production sequence.

A thick film resist printing step is performed prior to metallization. Metallization pattern printing of the front surface is followed by a standard drying process. The grid-line pattern metallization was produced in an electroless nickel plating process sequence. An optional junction edge clean-up can be added after nickel plating. This can be done by edge grinding, laser trimming[12] or plasma etching.[20] This is a necessary step if spray-on dopants are utilized. The solar cells are dipped in lead/tin solder to complete the metallization.

The phosphorous glass is removed and an antireflective coating is applied to the solar cell to enhance the current collection efficiency. A significant improvement (30% to 35%) has been observed on single crystal wafers.[12, 22, 23] An SiO antireflective coating was evaporated onto the polysilicon solar cells used in the selected process. Other less expensive AR coatings, such as silicon nitride[12] and spray-on films[12,22,23] are preferred for a low-cost, large-scale production.

The process sequence outlined in Figure 9.1 and discussed above, without the optional steps, was followed for four types of polysilicon material received from three suppliers. The electrical performance results for Wacker-SILSO, Crystal System - HEM and Exotic Materials - FAST CZ are given in Figures 9.2, 9.3a, 9.3b and 9.4, respectively and the electrical parameter data are given in Table 9.1. The solar cells were tested under a tungsten light source (G.E. Quartzline Lamp DWY, 2800^{o}K calibrated at 100 mw/cm^{2} at 28^{o}C).

The average efficiencies achieved respectively for the Wacker, Crystal Systems (HEM) and Exotic Materials large area polysilicon solar cells are 9.4% (with SiO), 9.6% (without AR coating) and 6.58% (without AR coating), respectively. These efficiencies are short of the 10% efficiency program goal, but with the exception of the Exotic Materials wafers, are not far off. This work indicates that polysilicon material process improvements and polysilicon solar cell production process improvements can increase the polysilicon solar cell efficiency. One batch of large area Wacker polysilicon material processed with the selected process with the spray-on n^{+} dopant option and SiO antireflective coating resulted in an average batch efficiency of 10.41% as shown in Section 8.2. This batch efficiency exceeded the 10% efficiency program goal and gives a good indication that more work can be done to improve the efficiency of polysilicon solar cells.

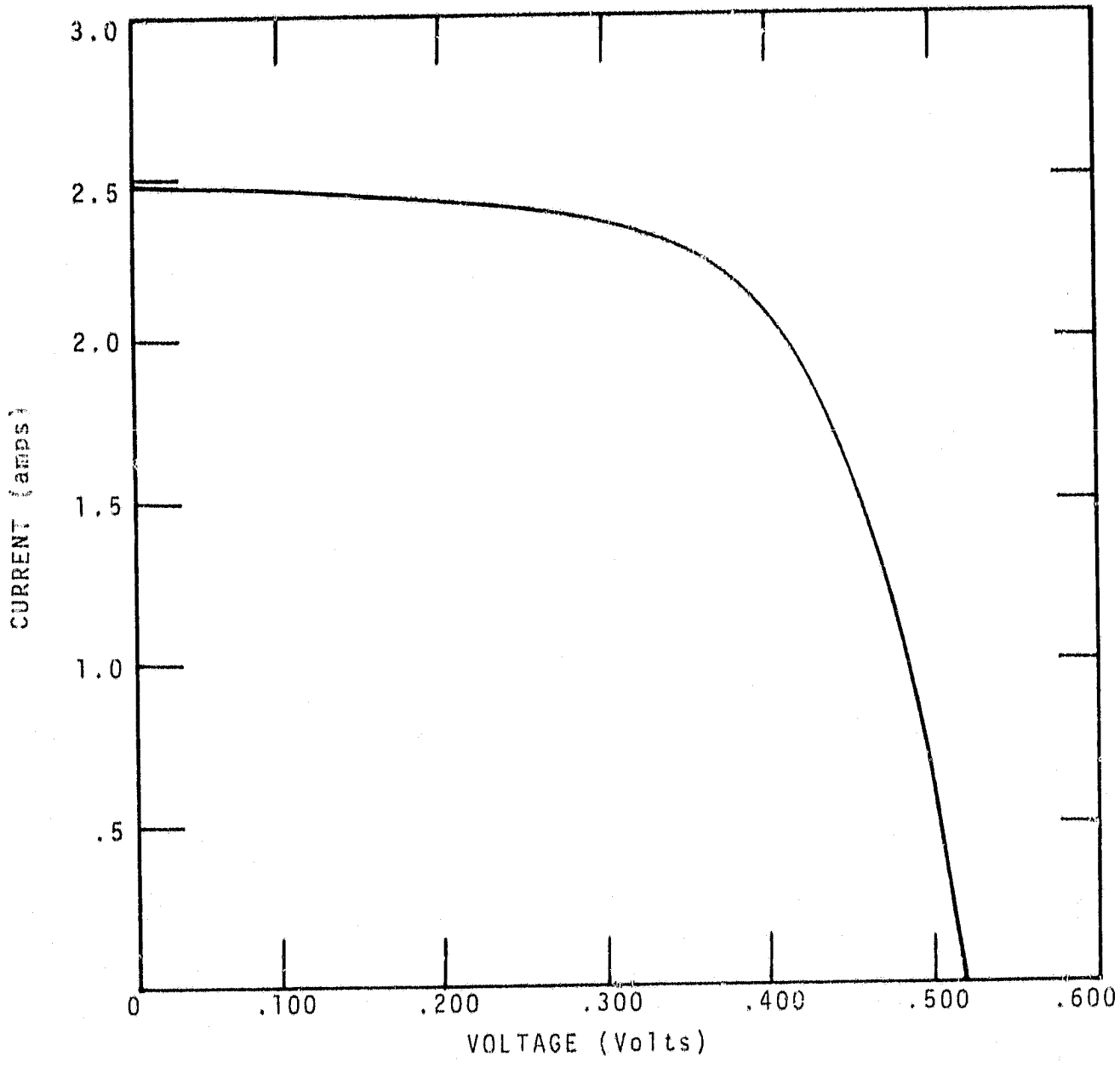


Figure 9.2 Electrical Performance Curve of Average Wacker Polysilicon Solar Cell Produced from the Selected Process.

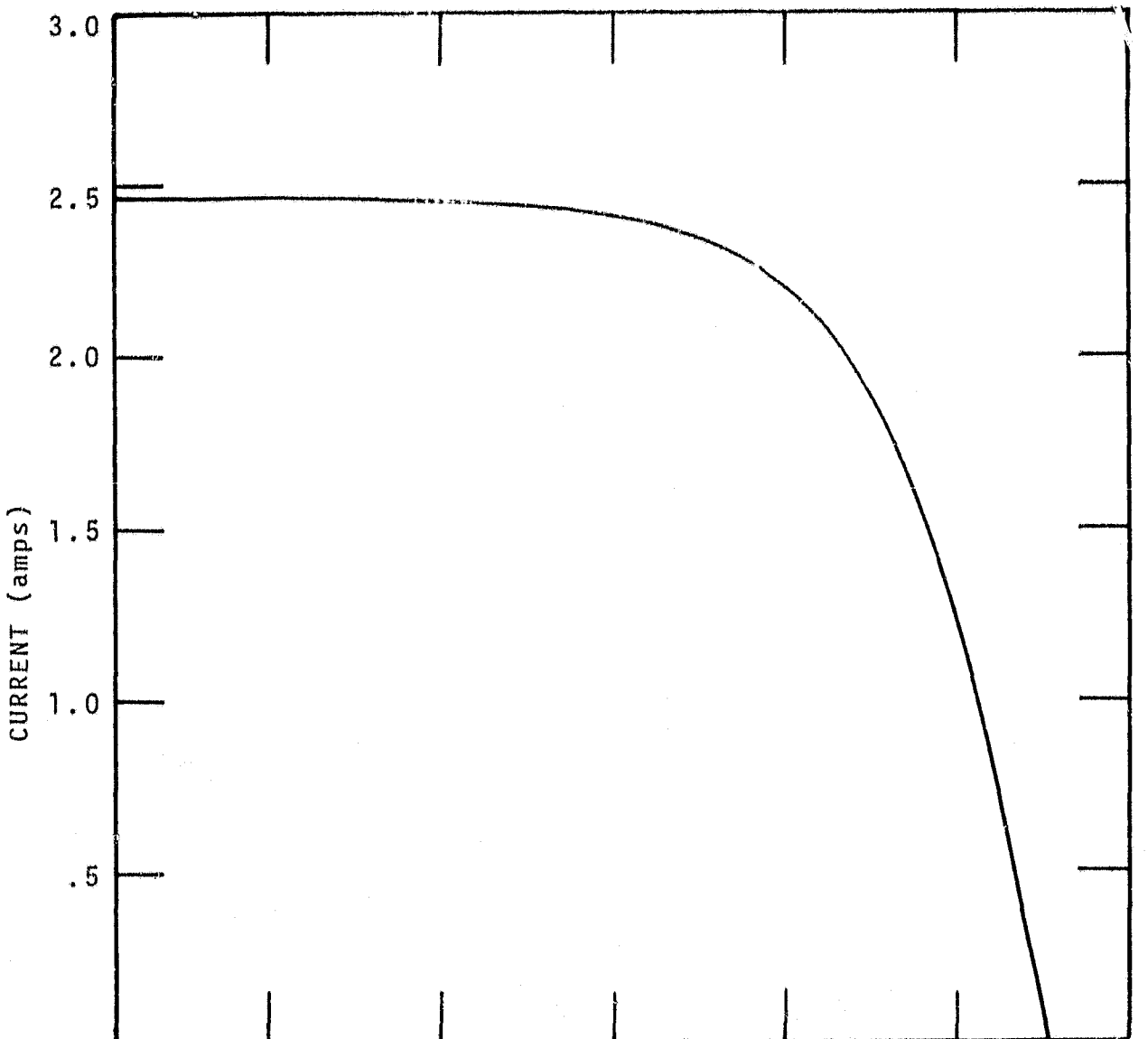


Figure 9.3a Electrical Performance Curve of Average Crystal System's HEM Solar Cell (100% single crystallinity) Produced from the Selected Process.

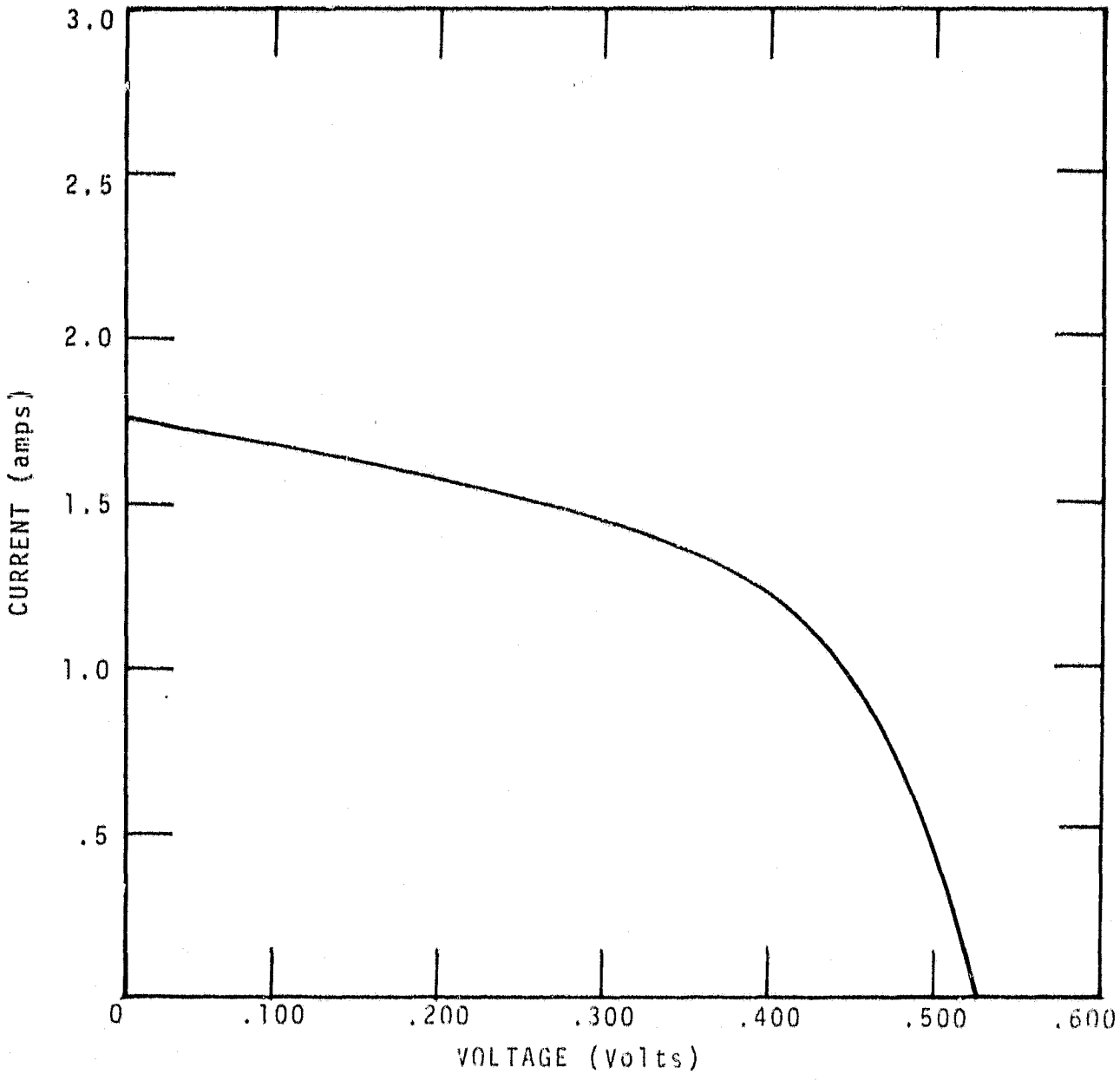


Figure 9.3b Electrical Performance Curve of Average Crystal Systems HEM Polysilicon Solar Cell (44% single crystallinity) Produced from the Selected Process.

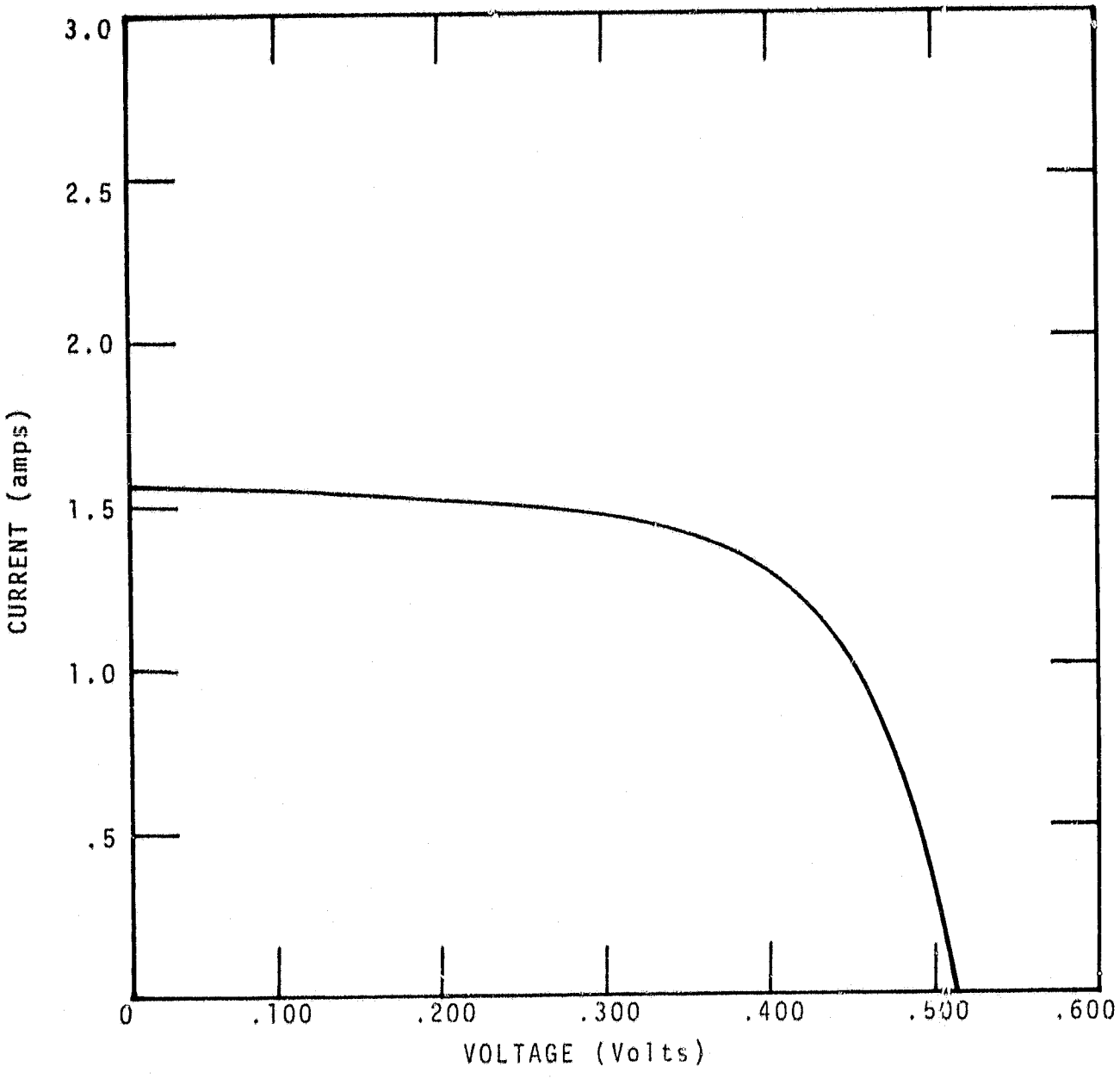


Figure 9.4 Electrical Performance Curve of Average Exotic Materials Polysilicon Solar Cell Produced from the Selected Process.

Table 9.1 Electrical Performance Data on Three Types of Large Area Polysilicon Solar Cells Produced from the Selected Process.
(26 Cells per Batch)

BATCH	I_{sc}(a)	V_{oc}(v)	I_{pp}(a)	V_{pp}(v)	η(%)	FF	$\frac{\Delta\eta}{\eta}$(%)	$\frac{\Delta FF}{FF}$(%)
P-102 Wacker-Silso, Selected process with SiOAR Coating. Active Area 92.7 cm^2.								
High	2.60	0.525	2.20	0.410	9.73	0.661	+3.50	+0.609
Low	2.50	0.515	2.10	0.400	9.06	0.652	-3.51	-0.761
Ave.	2.55	0.520	2.15	0.405	9.40	0.657		
P-500 Crystal Systems-HEM*, (100% crystallinity) selected process with Phosphorous glass (no AR Coating), Active Area 92.7 cm^2.								
High	2.55	0.566	2.03	0.445	9.74	0.626	+1.46	+0.76
Low	2.48	0.563	1.95	0.445	9.36	0.621	-2.50	-0.48
Ave.	2.5	0.565	2.00	0.445	9.60	0.624		
P-501 Crystal Systems-HEM (44% crystallinity) selected process with Phosphorous glass (no AR Coating), Active Area 92.7 cm^2.								
1	1.74	0.565	1.10	0.440	5.22	0.492	+1.75	+1.23
2	1.72	0.565	1.05	0.440	5.00	0.475	-2.53	-2.26
Ave.	1.73	0.565	1.08	0.440	5.13	0.486		
P-600 Exotic Materials-Fast CZ, selected process with phosphorous glass and no AR Coating. Active area 77.1 cm^2.								
High	1.61	0.515	1.45	0.383	7.21	0.670	+9.60	+3.08
Low	1.42	0.495	1.25	0.365	5.92	0.649	-10.03	-0.15
Ave.	1.54	0.508	1.39	0.365	6.58	0.650		

*HEM material utilized for these experiments exhibited larger than average grain sizes, and a macrostructure appearance similar to single crystal CZ material.

10.0 PROCESS/EQUIPMENT COST ANALYSIS

A cost analysis was performed on a conceptualized automated solar cell process sequence. The polysilicon solar cell selected process (See Section 9.0) was used with several suitable low-cost options considered appropriate for the 1986 industry. The Solar Array Manufacturing Industry Costing Standards (SAMICS) procedure was followed in the cost analysis. A standard Format A was prepared according to JPL Document No. 5101-44, Revision A[24] and JPL Document No. 5101-59[44] for each process step in the sequence. The process costs for each step were computed manually according to the SAMICS Workbook, JPL Document No. 5101-15.[26] The unit prices for the direct material cost elements were obtained from the Interim Price Estimation Guidelines, JPL Document No. 5101-33.[27]

10.1 Description of the Industry

The structure of the industry was assumed to be the 1986 standard industry as defined in reference (1). The model industry is composed of a sequence of companies, each of which is an independent financial entity. A total of five successive companies constitute the model industry. This study focused on only one of these companies; the cell manufacturing company.

It was assumed that all remaining companies of the model industry operate under the current price goals defined in reference (28). The company under consideration in this study will hereby be designed as CELLCO which manufactures photovoltaic solar cells.

The basic assumptions utilized in the standard industry are listed below:

1. CELLCO is a vertically integrated company which shares 33.3% of the market. CELLCO will purchase wafers from WAFERCO at the price of 13.2 cents per peak watt in 1975 cents as set forth in reference (28).
2. A double burden was not charged for silicon wafers since they were assumed to be vertically integrated as defined in reference (25).
3. CELLCO requires 4.7 shifts per day (24 hours), for 345 operating days per year. All remaining modifications specified in reference (25) were utilized in the analysis.
4. CELLCO maintains a production yield of 96.3%.
5. The solar cell cost is based upon its electrical performance. The product description presented in this final report can be summarized as follows:

   Material Types: Polysilicon wafers or single crystal wafers.

   Initial Wafer Size: Nominal wafer area is 64 cm^2. Wafer shape can be 90 mm diameter round or 8 cm square or other shapes that have the same nominal area.

   Final Cell Size: Minimum cell area is 51.3 cm^2. Cells can be trimmed to suit the module design.

   Usuable Silicon: 81% of cell area (minimum)

   Solar Cell Efficiency: 10% (minimum)

   Power Output: 0.636 watts per cell at 28°C and at 100 mW/cm^2 insolation and 64 cm^2 area.

In view of the above specifications, the anticipated annual production quantity for CELLCO is expected to be 278 million solar cells per year or 176.8 MW per year. These output rates are utilized in the SAMICS analysis.

10.2 Company Description

CELLCO is a model company in the 1986 standard industry which produces solar cells from polysilicon or single crystal silicon wafers. The annual production quantity for this company is 278 million solar cells per year which is equivalent to 176.8 MW.

The selection of a solar cell fabrication process sequence for CELLCO was based on the selected process given in Section 9.0 and on the results of the SAMICS cost analysis. A fully automated production line consisting of nine solar cell processes was selected for CELLCO. A conceptual layout of the model plant is given in Figure 10.1.

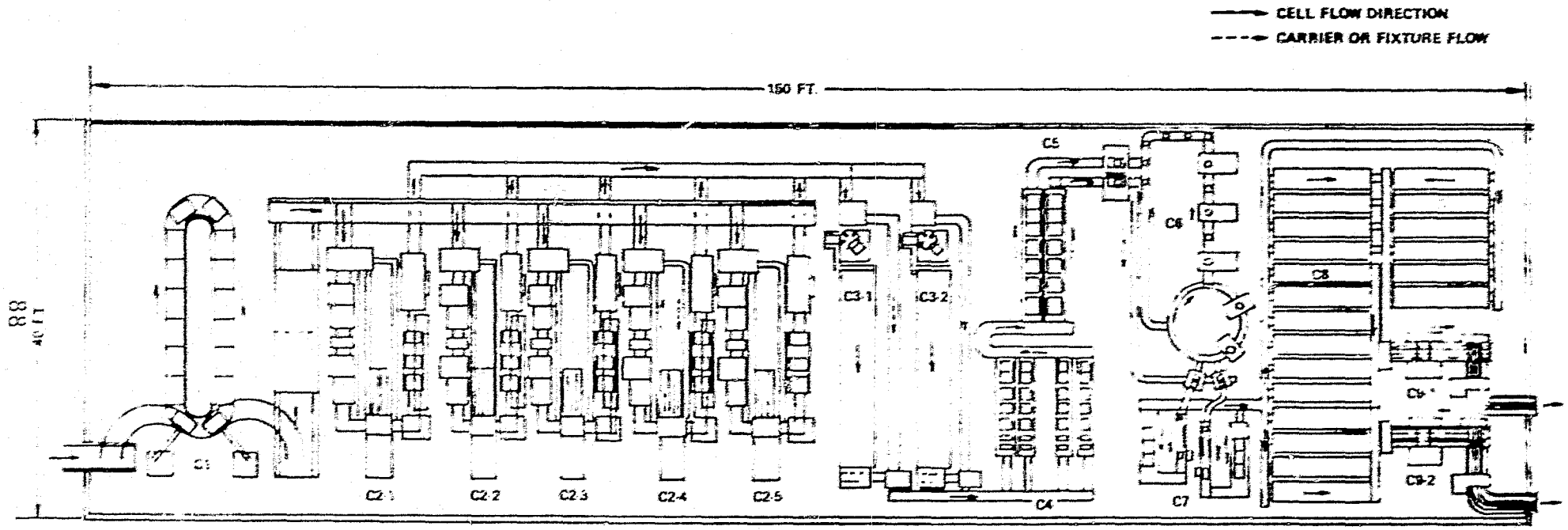
Each Photowatt International CELLCO production line was designed to produce approximately 35 MW per year, or about 6900 wafers per hour. Six production lines* will be required to produce 176.8 MW per year, which is 33.3% of the total market.

A brief description of each of the nine processes selected for use in the CELLCO model plant is given below:

*The sixth line will allow for system back-up and down-time.

Photowatt International CELLCO Production Line

35 Megawatt per year capacity
7200 wafers per hour
CELLCO needs six lines for 176.8 megawatt per year plant



C1 WAFER SURFACE PREPARATION (1 UNIT)
C2 JUNCTION FORMATION (5 UNITS)
C3 FRONT SURFACE PATTERN PRINTING (2 UNITS)
C4 ELECTROLESS NICKEL PLATING (4 UNITS)
C5 RESIST REMOVAL (2 UNITS)
C6 : LASERSCRIBING (1 UNIT)
C7 SOLDER FLOW (2 UNITS)
C8 PLASMA A-R COATING (20 UNITS)
C9 CELL TESTING & GROUPING (2 UNITS)

Figure 10.1 Photowatt International CELLCO Production Line.

(C-1) Wafer Surface Preparation (WFSURPR)

This process step consists of wafer surface cleaning, wafer surface texture etching, and final cleaning and drying.

(C-2) Junction Formation (JUNCF)

The junction formation process sequence includes: spray-on n^+ dopant onto the front surface with a subsequent IR bake, spray-on p^+ dopant onto the back surface with a subsequent IR bake, dopant drive-in of both surfaces, followed by excess dopant removal.

(C-3) Front Surface Pattern Printing (FSPP)

An initial process step prior to metallization is thick film resist printing by means of a negative mask. Metallization pattern printing of the front surface is followed by a standard drying process.

(C-4) Electroless Nickel Plating (ELNIPL)

This is an active metallization process. Nickel is plated onto the front surface gridline pattern, as well as the entire back surface. A cleaning step after plating completes this process step.

(C-5) Resist Removal (RESREM)

This process consists of wet chemical resist removal followed by a standard wafer cleaning and drying procedure.

(C-6) Laser Trimming (LAST)

An automatic laserscribing system for large volume production performs the trimming and shaping of the solar cells.

(C-7) Solder Flow (SLDFLW)

The front surface grid pattern and back surface are solder coated in this process. The complete solder flow process consists of preheating, flux application, solder dipping, and flux removal.

(C-8) Antireflective Coating (ARCT)

The solar cell antireflective coating is applied by silicon nitride plasma deposition.

(C-9) Cell Testing and Grouping (Celltest)

Solar Cells are automatically tested, analyzed and grouped according to electrical performance.

10.3 Price Computation

The price of a solar cell was determined after all the data required for each Format A was compiled. The cost computation proceeded in accordance with the procedure outlined for the process worksheet and company worksheet described in reference (26). Additional expense item information, which was not included in the cost account catalog in reference (29) was found in currently available market price literature.

The total cost incurred at each solar cell process step was manually calculated and can be found in Table 10.1. The cost for each process was further subdivided into independent elements which consist of the cost in terms of 1975 cents per peak watt for space, labor, materials and utilities.

Table 10.1 CELLCO Process Cost Summary in 1975 Cents per Peak Watt.

Process Numbers	Process Referent	Equipment	Floor Space	Labor	Material & By-Products	Utilities	TOTAL
C-1	WFSURPR	.200	.072	.440	.780	.190	1.682
C-2	JUNF	.550	.174	.570	1.200	.641	3.135
C-3	FSPP	.128	.110	.270	.424	.050	.982
C-4	ELNIPL	.084	.038	.430	3.810*	.138	4.500*
C-5	RESREM	.027	.017	.220	1.636	.109	2.009
C-6	LAST	.270	.030	.350	.004	.123	.777
C-7	SDFLW	.050	.021	.210	1.900	.213	2.394*
C-8	ARCT	1.861*	.124	.940	.800	.274	3.999*
C-9	CELLTEST	.100	.018	.185	0	.018	.321
TOTAL		3.270	.604	3.615	10.554	1.756	19.80

*Highest Cost Element

10.4 Discussion of Results

The total added value for CELLCO is 19.8 cents per peak watt in 1975 cents. This value is slightly higher than the PAG[10] price goal of 18.3 costs per peak watt. As shown in Table 10.1, metallization and AR coating processes claim a disproportionate share of the total cost for CELLCO.

The major shortcoming of the current electroless nickel plating metallization process is its use of costly materials. This process sequence requires the use of front surface resist pattern printing (Step C-3), electroless nickel plating (Step C-9), resist removal (Step C-5) and solder flow (Step C-7), which adds up to 9.885 cents per peak watt or more than 50% of the cell processing cost. A process sequence that utilizes, for example, a low-cost printed metallization pattern would eliminate the resist application and resist removal steps and would reduce direct material costs. A lower cost conductive material to replace solder would significantly reduce the cost of Step C-7. It is recommended that future efforts be directed toward these areas to reduce the costs of the metallization process sequence.

The major shortcomings of the silicon nitride plasma deposition AR coating process resides in its high equipment cost. One candidate procedure exhibiting high potential for success in this task is spray-on AR coating. An in-depth study of the application of low-cost spray-on AR coating techniques to polysilicon solar cells is recommended.

11.0 CONCLUSIONS

The work performed in the development of low-cost polysilicon solar cells led to a number of conclusions which are listed by task below.

Influence of Crystal Grains on Solar Cell Efficiency

1. The diffusion length model,[3] which describes the effects of crystal grain boundaries on polysilicon solar cell efficiency, was not able to account for the large differences observed between single crystal silicon and coarse grain polysilicon solar cell efficiencies.

Gridline Pattern Design Considerations

1. The fractional power loss model, which describes the effects of gridline spacing on polysilicon solar cells, was not able to account for the small electrical performance differences observed between narrow and wide gridline spacings on polysilicon solar cells with similar crystal grain characteristics.

2. The gridline spacing data indicates that the electrical performance effects due to crystal grain boundaries are not dominate and are not a strong function of grain size.

3. Polysilicon wafer material data show large differences in electrical performance parameters between two types of wafer material (fine and coarse grain) with the same gridline spacings. These data indicate probable differences in polysilicon material characteristics and energy loss mechanisms.

4. Most of the electrical performance parameters of the large area (100 cm^2) Wacker polysilicon solar cells were exhibited by the smaller area (21.1 cm^2) quarter cells which indicates general homogeneity of the samples studied.

Wafer Surface Texturizing Process

1. The initial etch rate (first 5 minutes) was faster than or equal to the intermediate and final etch rates for all the polysilicon and single crystal silicon wafers studied in this program. This conclusion was valid regardless of the sodium hydroxide solution concentrations utilized.

2. Single crystal silicon in general etches faster than fine grain or coarse grain polysilicon. Coarse grain polysilicon in general etches slightly faster than fine grain polysilicon.

3. The single crystal silicon etch rate is generally constant with residence time in the etchant. The fine grain and coarse grain polysilicon etch rates are subject to erratic changes for the particular etchant concentrations studied during this program.

4. The 10% $NaOH/H_2O$ solution and the 20% $NaOH/H_2O$ solution were both found to be sufficient to assure the removal of surface damage (about 0.7 mils/wafer or 0.35 mils/wafer side) from polysilicon or single crystal silicon wafers in a five minute etching time.

5. The two-stage texturizing process consisting of isotropic texture etching in 20% $NaOH/H_2O$ followed by texturizing in 2% $NaOH/H_2O$ with isopropyl alcohol produced a uniform fully texturized surface on single crystal silicon wafers. The same two-stage texturizing process without the isopropyl alcohol produced uniform surface macrostructures, but the surfaces were not as fully and completely texturized as the process with the isopropyl alcohol (20% by weight isopropyl alcohol was utilized).

6. The two-stage texturizing process with isopropyl alcohol texturized 15% to 20% of the Wacker polysilicon wafer surfaces. Most of the texturized polysilicon grains were located in the center region of the wafers. The elongated crystal grains located along the outer edges of the wafers (about 45% of the surface area) were etched, but not texturized indicating a different crystal grain orientation than (100), which is not suitable for NaOH anisotropic texturization.

Diffusion Process

A $POCl_3$ diffusion time-temperature study indicated that the polycrystalline nature of the starting material had little if any effect on the optimum diffusion schedule.

Other Process Considerations

1. The inclusion of a $POCl_3$ pregettering step in the polysilicon solar cell process sequence enhanced the solar

cell power output and efficiency for the three types of polysilicon solar cell material investigated in this program.

2. It was demonstrated that 10% efficient polysilicon solar cells in batch quantity can be produced with low-cost spray-on n^+ dopants. This result fulfills an important goal of this project, which is the production in batch quantity of 10% efficient polysilicon solar cells.

3. An improvement in open circuit voltage and peak power voltage was achieved with printed and evaporated aluminum back surface metallization on polysilicon and single crystal silicon solar cells.

Process/Equipment Cost Analysis

1. It can be concluded from a detailed SAMICS process cost analysis that the solar cell process costs are in line with the 1986 JPL/LSA cost goals.

2. The total 1986 solar cell selling price was determined to be 33 cents per peak watt in 1975 cents. This includes an assumed polysilicon wafer selling price of 13.2 cents per peak watt and a solar cell manufacturing cost of 19.8 cents per peak watt. Additional work to significantly reduce metallization costs and AR coating costs was recommended.

12.0 RECOMMENDATIONS

In the development of low-cost polysilicon solar cells a number of recommendations were made and are listed below.

1. A five minute anisotropic texture etching step in 10% $NaOH/H_2O$ or 20% $NaOH/H_2O$ is preferred over the two-stage texturizing process with or without the isopropyl alcohol due to lower cost, surface damage removal effectiveness, and suitability for an antireflective coating.

2. A cold water cascade rinse following the texture etching step is preferred over the hot water D.I. water rinse due to lower utility cost.

3. A $POCl_3$ gettering step (prior to the texture etching step) is highly recommended for incorporation into a near-term polysilicon solar cell production process sequence. This wafer treatment significantly improves polysilicon solar cell efficiencies. If the quality of the polysilicon wafer material improves, (impurities and recombination center sites reduced) then the gettering step may not be necessary for the 1986 automated solar cell process sequence.

4. The peak power voltage was found to be lower for the large area (100 cm^2) polysilicon solar cells than for the small area (21.1 cm^2) quarter cells which indicates a probable deficiency in the main gridlines of the large area solar cells due to resistive losses. An increase in the width of the main gridlines, which increases the cell shadowing losses, or the addition of a copper strip across the entire length of the

main gridlines will reduce the resistive losses. The latter method is recommended. It will improve the cell peak power voltage without sacrificing the current losses due to shadowing and will aid in the solar cell interconnection scheme in module assembly.

5. The spray-on n^+ dopant junction formation results and the printed aluminum results on polysilicon wafers were very encouraging. Application of low-cost spray-on techniques for junction formation, aluminum back surface field and anti-reflective coating for single crystal solar cells[21] are also very encouraging. An indepth study of the application of these low-cost techniques to polysilicon solar cells is highly recommended.

6. The major shortcoming of the current electroless nickel plating metallization process is the use of costly materials. A process sequence that utilizes for example a printed metallization pattern would reduce process steps and direct material costs. A lower cost conducting material to replace solder would significantly reduce costs. The reduction of the metallization process costs through efforts directed along these lines is highly recommended.

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APPENDIX I

The following section originally produced as a "stand alone" report, is included as a referenced source for confirmation purposes.

ABSTRACT

A through cost analysis was manually performed with the updated version of the standard SAMICS method for each process utilized in this program for the "Development of Low-Cost Polysilicon Solar Cells," part of the Production Process and Equipment Task, a JPL/LSA project. One model company, CELLCO, which produces solar cells from polysilicon wafers, was emphasized in this study. The process sequence utilized was selected on the basis of the SAMICS cost analysis performed in this program.

The SAMICS results included an assumed silicon wafer selling price of 13.2 cents per peak watt and a calculated solar cell manufacturing cost of 19.8 cents per peak watt. The total 1986 solar cell selling price was determined to be 33 cents per peak watt in 1975 cents.

It was concluded from the SAMICS process cost analysis that the solar cell process costs were in line with the 1986 JPL/LSA cost goals. Additional work to reduce metallization costs and AR coating costs were recommended.

APPENDICES
TABLE OF CONTENTS

Title	Page No.
APPENDIX I	
ABSTRACT	ii
INTRODUCTION	1
DESCRIPTION OF THE INDUSTRY	1
CELLCO COMPANY DESCRIPTION	3
PROCESS DESCRIPTION	6
1. Wafer Surface Preparation	6
2. Junction Formation	10
3. Front Surface Pattern Printing	13
4. Electroless Nickel Plating	17
5. Resist Removal	21
6. Laser Trimming Process	24
7. Solder Flow and Flux Removal	29
8. Antireflective Coating	34
9. Cell Testing	39
PRICE COMPUTATION	43
DISCUSSION OF RESULTS	45
CONCLUSIONS AND RECOMMENDATIONS	47
REFERENCES	48
INDUSTRY DESCRIPTION, Format C	49
APPENDIX II- COMPANY DESCRIPTION, Format B and PROCESS DESCRIPTION, Format A for CELLCO.	51
APPENDIX III - TEMPORARY CATALOG FOR EXPENSE ITEMS	71

APPENDICES
TABLE OF CONTENTS

Title	Page No.
APPENDIX I	
ABSTRACT	ii
INTRODUCTION	1
DESCRIPTION OF THE INDUSTRY	1
CELLCO COMPANY DESCRIPTION	3
PROCESS DESCRIPTION	6
1. Wafer Surface Preparation	6
2. Junction Formation	10
3. Front Surface Pattern Printing	13
4. Electroless Nickel Plating	17
5. Resist Removal	21
6. Laser Trimming Process	24
7. Solder Flow and Flux Removal	29
8. Antireflective Coating	34
9. Cell Testing	39
PRICE COMPUTATION	43
DISCUSSION OF RESULTS	45
CONCLUSIONS AND RECOMMENDATIONS	47
REFERENCES	48
INDUSTRY DESCRIPTION, Format C	49
APPENDIX II- COMPANY DESCRIPTION, Format B and PROCESS DESCRIPTION, Format A for CELLCO.	51
APPENDIX III - TEMPORARY CATALOG FOR EXPENSE ITEMS	71

APPENDIX I

LIST OF FIGURES

Figure No.	Title	Page No.
C-0	Photowatt International CELLCO Production Line.	4
C-1	Automatic Texturizing System	7
C-2	Conceptual Design of Spray-on Dopant Junction Formation System	12
C-3	Schematic Layout of Automatic Wafer Printing System.	14
C-4	Schematic Layout of Nickel Plating System.	18
C-5	Schematic Layout of Wet Chemical Resist Removal System	22
C-6	Serial Flow Laserscribe Trimming System for 7200 wafers/hr..	25
C-7	Conceptual Solder Coating and Flux Removal System	30
C-8	LFE 8000 System for Silicon Nitride Antireflective Coating	35
C-9	Conceptual Design of Automatic Solar Cell Test System	40

APPENDIX I
LIST OF TABLES

Table No.	Title	Page No.
1	CELLCO Process Cost Summary.	44

INTRODUCTION

A cost analysis was performed on a conceptualized automated solar cell process sequence. This polysilicon solar cell selected process (see Section 9.0) was used with several suitable low-cost options considered appropriate for the 1986 industry. The Solar Array Manufacturing Industry Costing Standards (SAMICS) was followed in the cost analysis. A standard Format A was prepared according to JPL Document No. 5101-44, Rev. (1), and JPL Document No. 5101-59(2) for each process step in this sequence. The process costs for each step were computed manually according to the SAMICS Workbook, JPL Document No. 5101-15.(3) The unit prices for the direct material cost elements were obtained from the Interim Price Estimation Guidelines, JPL Document No. 5101-33.(4)

DESCRIPTION OF THE INDUSTRY

The structure of the industry was assumed to be the 1986 standard industry as defined in reference (4). The model industry is composed of a sequence of companies, each of which is an independent financial entity. A total of five successive companies constitute the model industry. This study focussed on only one of these companies; the cell manufacturing company.

It was assumed that all remaining companies of the model industry operate under the current price goals defined in reference (5). The company under consideration in this study will hereby be designated as CELLCO which manufactures photovoltaic cells.

The basic assumptions utilized in the standard industry are listed below:

1. CELLCO is a vertically integrated company which shares 33.3% of the market. CELLCO will purchase wafers from WAFERCO at the price of 13.2 cents per peak watt in 1975 cents as set forth in reference (5).

2. A double burden was not charged for silicon wafers since they were assumed to be vertically integrated as defined in reference (2).

3. CELLCO requires 4.7 shifts per day (24 hours) for 345 operating days. All remaining modifications specified in reference (2)were utilized in the analysis.

4. CELLCO maintains a production yield of 96.3%.

5. The solar cell cost is based upon its electrical performance. The product description presented in reference (6) can be summarized as follows:

Material Type: Polysilicon wafers or single crystal wafers.

Initial Wafer Size: Nominal wafer area is 64 cm^2. Wafer shape can be 90 mm diameter round or 8 cm square or the shapes that have the same nominal areas.

Final Cell Size: Maximum Cell Area is 62 cm^2. Minimu cell area is 51.3 cm^2. Cells can be trimmed to suit the module design.

Usuable Silicon: Maximum usable cell area is 96% and and minimum (reasonable) usable area is 81% of starting substrate area.

Solar Cell Efficiency: 10% (minimum)

Power Output: 0.636 watts per cell (at minimum usable area) at 28°C and at 100 mw/cm^2 insolation.

In view of the above specifications, the anticipated annual production quantity for CELLCO is expected to be 278 million solar cells per year or 176.8 MW per year. These output rates are utilized in the SAMICS analysis.

CELLCO COMPANY DESCRIPTION

CELLCO is a model company in the 1986 standard industry which produces solar cells from polysilicon or single crystal silicon wafers. The annual production quantity for this company is 278 million solar cells per year which is equivalent to 176.8 MW.

The selection of a solar cell fabrication process sequence for CELLCO was based on the selected process given in reference (6) and on the results of the SAMICS cost analysis. A fully automated production line consisting of nine solar cell processes was selected for CELLCO. A conceptual layout of the model plant is given in Figure C-0.

The Photowatt International CELLCO plant was designed to produce approximately 35 MW per year, or about 7200 wafers per hour. Six production lines* will be required to produce 176.8 MW per year, which is 33.3% of the total market.

A brief description of each of the nine processes selected for use in the CELLCO model plant is given below:

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* The sixth line will allow for back-up system and down-time.

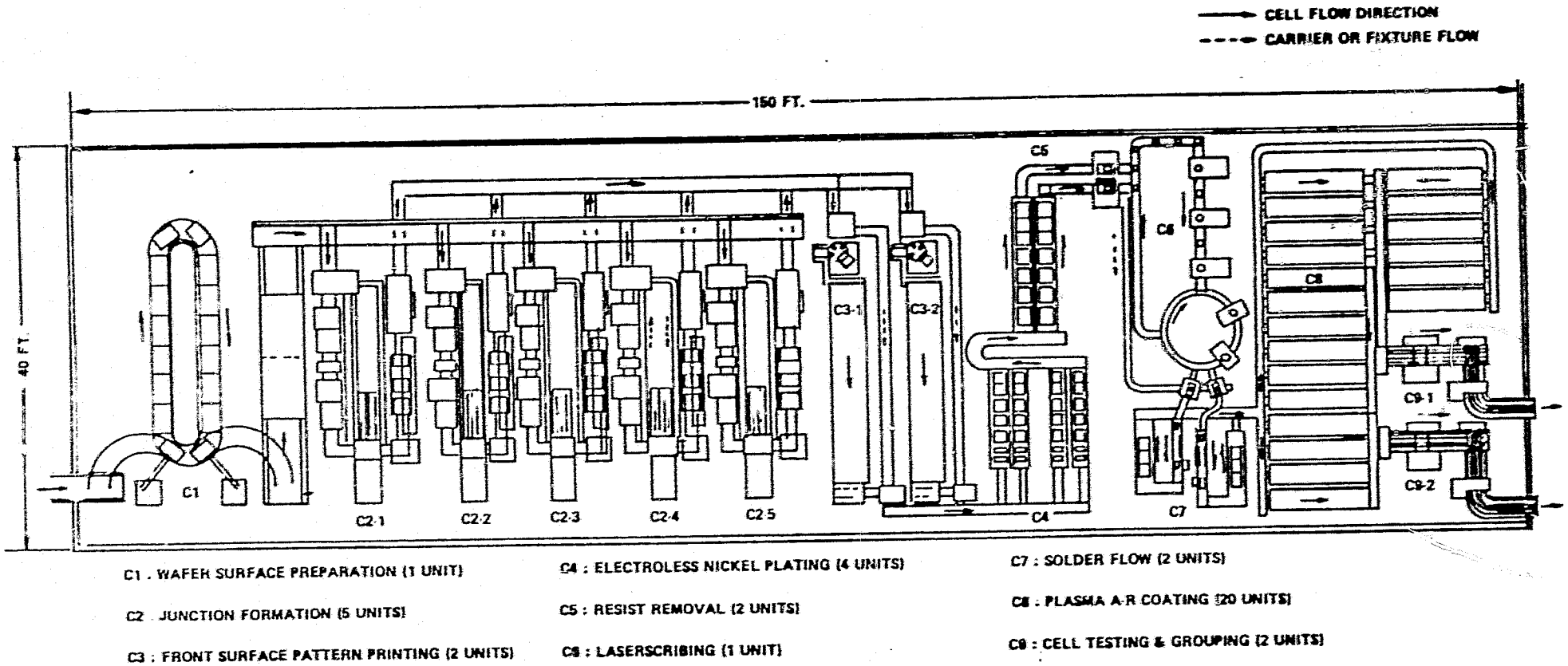


Figure C-0 Photowatt International CELLCO Production Line - 35 MW Per Year Capacity 7200 Wafers Per Hour. CELLCO Needs Six Lines for 176.8 MW Per Year Plant

(C-1) Wafer Surface Preparation (WFSURPR)

This surface step consists of wafer surface cleaning, wafer surface texture etching, and final cleaning and drying.

(C-2) Junction Formation (JUNCF)

This junction formation process sequence includes: spray-on n^+ dopant onto the front surface with a subsequent IR bake, spray-on p^+ dopant onto the back surface with a subsequent IR bake, dopant drive-in of both surfaces, followed by excess dopant removal.

(C-3) Front Surface Pattern Printing (FSPP)

An initial process step prior to metallization is thick film resist printing by means of a negative mask. Metallization pattern printing of the front surface is followed by a standard drying process.

(C-4) Electroless Nickel Plating (ELNIPL)

This is an active metallization process. Nickel is plated onto the front surface gridline pattern, as well as the entire back surface. A cleaning step after plating completes this process step.

(C-5) Resist Removal (RESREM)

This process consists of wet chemical resist removal followed by a standard wafer cleaning and drying procedure.

(C-6) Laser Trimming (LAST)

An automatic laserscribing system for large volume production was developed and utilized in this program. The laserscribe performs the scribing and shaping of the solar cells.

(C-7) Solder Flow(SDFLW)

The front surface grid pattern and back surface are solder coated in this process. The complete solder flow process consists of preheating, flux application, solder dipping, and flux removal.

(C-8) Antireflective Coating (ARCT)

The solar cell antireflective coating is applied by silicon nitride plasma deposition.

(C-9) Cell Testing and Grouping (Celltest)

Solar cells are automatically tested, analyzed and grouped according to electrical performance.

PROCESS DESCRIPTION

1. Wafer Surface Preparation

   a. Design for High Volume Production

A wafer surface texturizing study was performed with the use of Photowatt International's existing texturizing equipment. On the basis of the resulting process cost computation, the conceptual design for the large volume production line shown in Figure C-1 was devised.

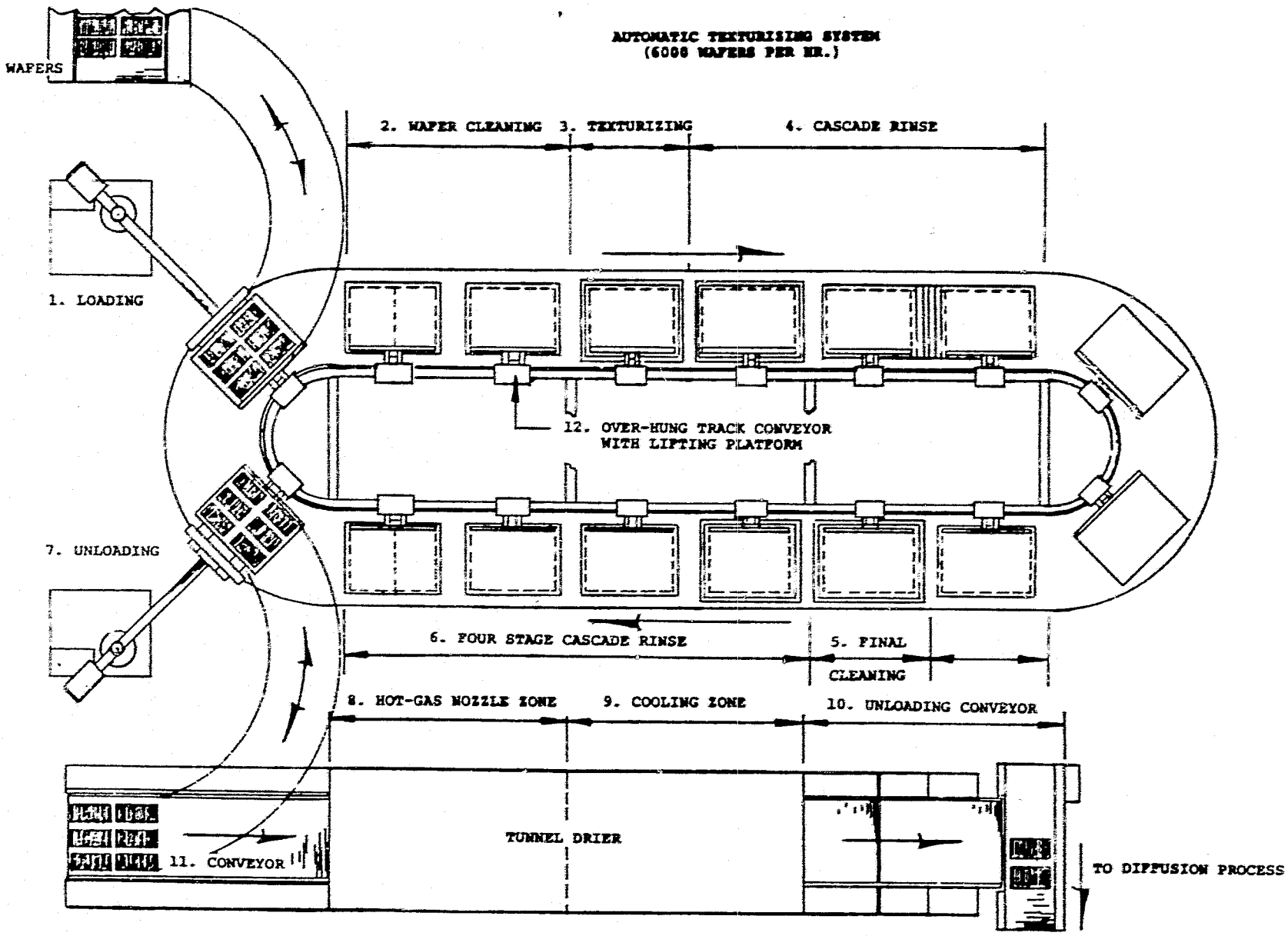


Figure C-1Automatic texturizing system, 6000 wafers per hour.

This fully automated system consists of twelve equally spaced indentical tanks. Each tank is capable of holding twelve wafer carriers situated on a platform lift. Since each wafer carrier can hold up to 50 wafers, 600 wafers constitute one batch.

Each batch remains in its corresponding process tank for five minutes and then transfers to the next station during a one minute time period. The transfer mechanism utilized in this process step consists of a lifter at each station and an over-hung track conveyor. The conveyor transfers each platform to its corresponding station, and lifters move the platforms up and down within the tank. The function of each tank is specified in Figure C-1.

b) Supporting Data For Format A

The process cost estimation for the wafer surface preparation task entailed the following cost elements.

(1) Equipment Costs

TEXTURIZING SYSTEM

Frame and tanks	$24,000
Supporting tanks	$4,000
Ultrasonic and Other Accessories	$12,000
Moving hoist lifter and conveyor	$14,000
Main drive system	$6,000
Control system including gauges	$10,000
Engineering and design	$10,000
Burden (50%)	$40,000

DRIER SYSTEM	
Tunnel chambers and conveyor	$10,000
Nozzle, Heater and fan control	$11,000
Burden (50%)	$10,000
LOADER AND UNLOADER SYSTEM	
Two loaders and one conveyor unloader	$20,000
TOTAL SYSTEM COST	$171,000

(2) Floor Space

The layout for the prototype system depicted in Figure C-1 indicates a floor space requirement of 448.82 ft.

(3) Labor

One operator is sufficient to run the fully automated texturizing system. It was assumed that the remaining labor requirements include 0.1 maintenance man, 0.1 Q.C. inspector, and 0.02 production planner.

(4) Utilities and Commodities

It was assumed that chemical consumption rates are directly proportional to the production throughput rate. Consequently, each chemical consumption rate utilized in the high volume texturizing system is related to its corresponding chemical consumption rate in the actual test model by the throughput ratio between the two systems.

The electrical power consumption rate of 0.289 Kw-hr/minute was estimated on the basis of a thorough design analysis performed on the texturizing system shown in Figure C-1.

2. Junction Formation

a. Design For High Volume Production

The spray-on-dopant junction formation system utilized in the conceptual high volume production line is a modified version of Advanced Concepts Model SC100 (ref. 8, Task 15) with a throughput rate of 1200 wafers/hour. The junction formation process is composed of three distinct process steps. The first process step is spray-on of n^+ and p^+ polymer dopants onto the front and back wafer surfaces, respectively, followed by dopant bake-in. The second process step is dopant drive-in. A readily obtainable, conventional rectangular diffusion furnace with a throughput rate of 1200 wafers per hour is used in this process step. The only additional required equipment utilized for dopant drive-in is an automatic loading device for loading wafers into boats, and then boats into the diffusion furnace. The third process step is excess dopant removal which involves dipping a wafer carrier emerging from the dopant drive-in process, into a hydrofluoric acid etching tank. A three stage cascade rinse and drying procedure completes this process step.

The schematic diagram for the conceptual high volume junction formation system is presented in Figure C-2. The systematic operation of the spray-on-dopant junction formation system can be described as follows: (1) wafers are loaded onto conveyor, (2) n^+ polymer dopant is sprayed onto the front wafer surface, (3) wafers are transported through I-R oven, (4) wafers are flipped over, and the same procedure is repeated with P^+ polymer dopant sprayed on the back wafer surface.

b) Supporting Data For Format A

The process cost estimation for the spray-on-dopant junction formation task entailed the following cost elements.

(1) Equipment

Equipment cost estimations utilized in the SAMICS cost analysis of the spray-on junction formation process are presented below.

SPRAY-ON SYSTEM

2 spray-on units:	$40,000
Loader and unloader:	$ 5,000
Flip over mechanism:	$ 2,500
Pallet return conveyor:	$ 500
Pallets:	$ 200
Total:	$48,000

DRIVE-IN SYSTEM

15 KW, 1500°C. 5" x 7" x 30" Brute diffusion furnace:	$20,000
Loader and unloader:	$ 5,000
Quartz boats and tubes	$ 500
Total:	$25,500

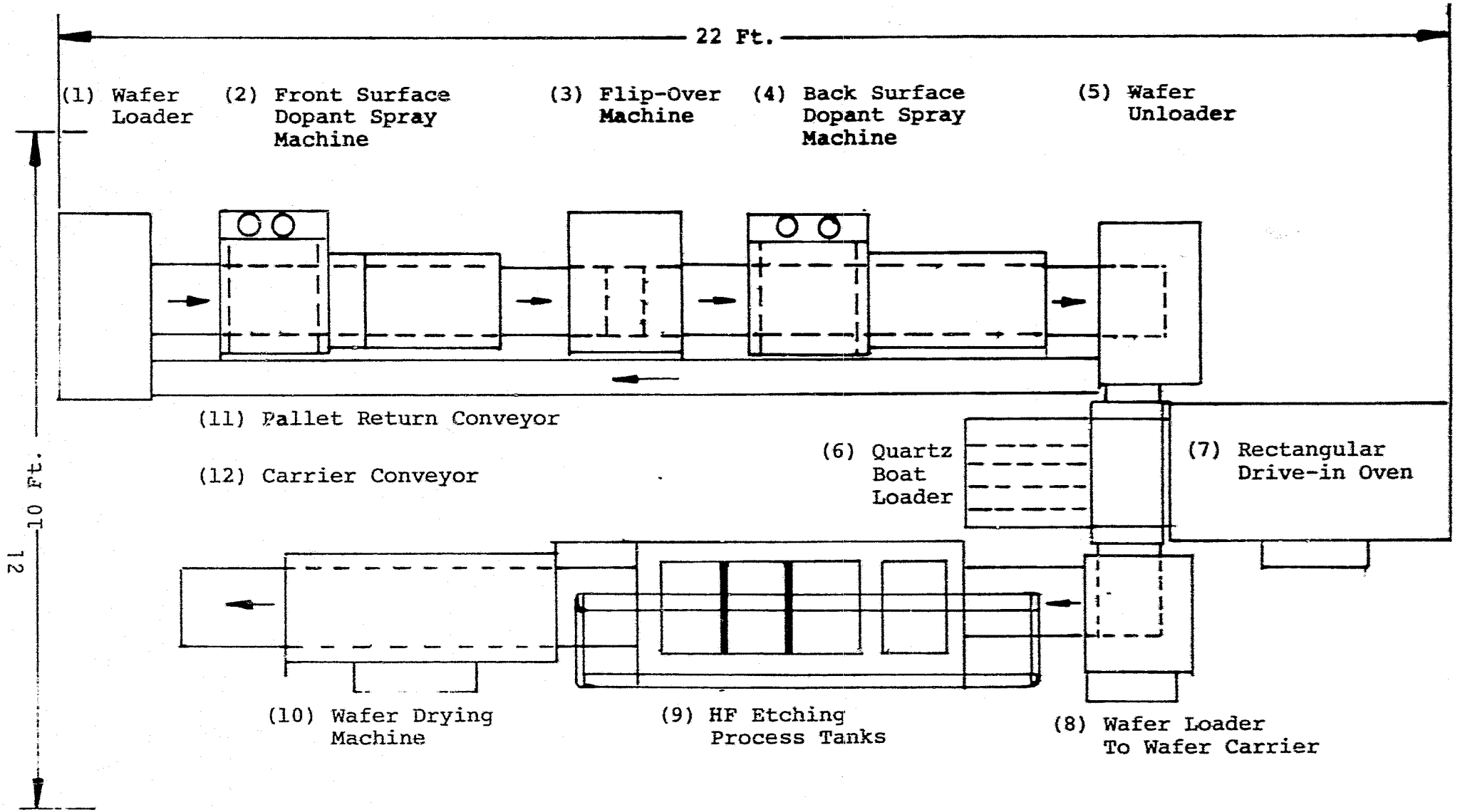


FIGURE C-2 CONCEPTUAL DESIGN OF SPRAY-ON DOPANT JUNCTION FORMATION SYSTEM (1,200 wafer/hr. capacity)

EXCESS DOPANT REMOVAL

HF Tank and Rinse Tank:	$ 4,500
Material handling system:	$ 2,000
Loader:	$ 2,000
Drier:	$ 5,000
Total:	$13,500

(2) Floor Space and Labor

The floor space requirement of 220 sq. ft. was estimated on the basis of the schematic diagram presented in Figure C-2. One operator is sufficient to handle four spray-on-dopant junction formation systems. The remaining labor requirements are identical to the wafer surface preparation task.

(3) Utilities and Commodities

All utility and commodity requirements presented in Format A have been obtained directly from experiment.

The input data utilized for this process cost computation may be located in the appropriate Format A of Appendix II.

3. Front Surface Pattern Printing (FSPP)

a) Design For High Volume Production

Front surface pattern printing is the third process performed in the CELLCO firm. This process received detailed analysis in Task 6 of Phase 2 of the Array Automated

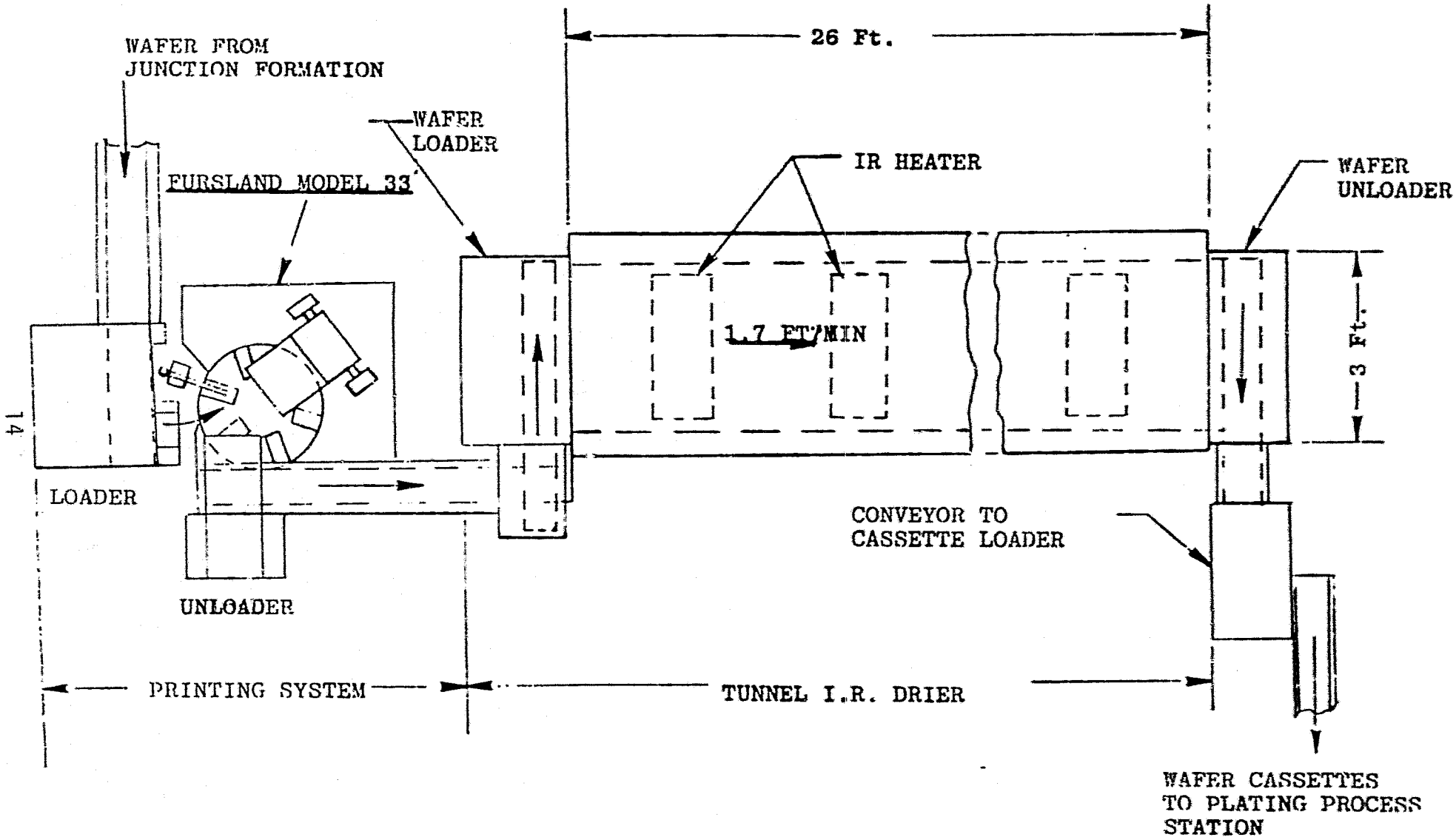


Figure C-3 SCHEMATIC LAYOUT OF AUTOMATIC WAFER PRINTING SYSTEM (3000 WAFER/HOUR).

Assembly Program (Ref. 8). The conceptual design for the high volume front surface pattern printing system is depicted in Figure C-3. The complete system is composed of a printer and an I.R. drier tunnel. The printing unit is a modified version of the Fursland Model 33, and has an expected throughput rate of 3000 wafers per hour. The I.R. drier tunnel is strictly a conceptual design.

The wafers emerging from the junction formation process station are transported by a pick-up arm device to the printer. The printer prints the front surface grid pattern design, and then unloads the printed wafers onto a transfer conveyor. The transfer conveyor is equipped with a hot gas blower for preliminary ink drying, and serves to facilitate easy wafer handling between the wafer loader and the drier tunnel.

b. Supporting Data For Format A

The process cost computation for the front surface pattern printing task entailed the following cost elements.

(1) Equipment Costs:

PRINTER

Main Machine:	$14000
Loader and Unloader:	$ 6000
Total:	$20000

TUNNEL DRIER

Tunnel chamber and conveyor:	$10000
Fans and main driers:	$ 5000
Heater and control:	$ 5000
Total:	$20000

(2) Floor Space:

The floor space estimation of 360 square feet was obtained directly from the layout drawing.

(3) Labor:

One operator is sufficient to operate four complete printing systems. All remaining personnel are assumed to be identical to the wafer surface preparation task.

(4) Materials:

The direct materials needed for this operation are printing ink and thinner. The consumption rates of these materials and their unit prices in terms of 1978 dollars are:

Ink: 4.0×10^{-5} gal/wafer
$36.16/gal.

Thinner: 8.67×10^{-6} gal/wafer
$45.20/gal

(5) Utilities:

The electrical power requirement for each individual unit is as follows:

Printer	0.315kw
Fan motors	0.5 hp x 2 = 1 hp
Loader and unloader	0.5 hp x 2 = 1 hp
Main drive	2 hp
I.R. heaters	3 kw x 5 = 15 kw
Total	18.3 kw

The input data utilized for this process cost computation may be located in the appropriate Format A of Appendix II.

4. Electroless Nickel Plating (ENIPL)

a) Design for High Volume Production

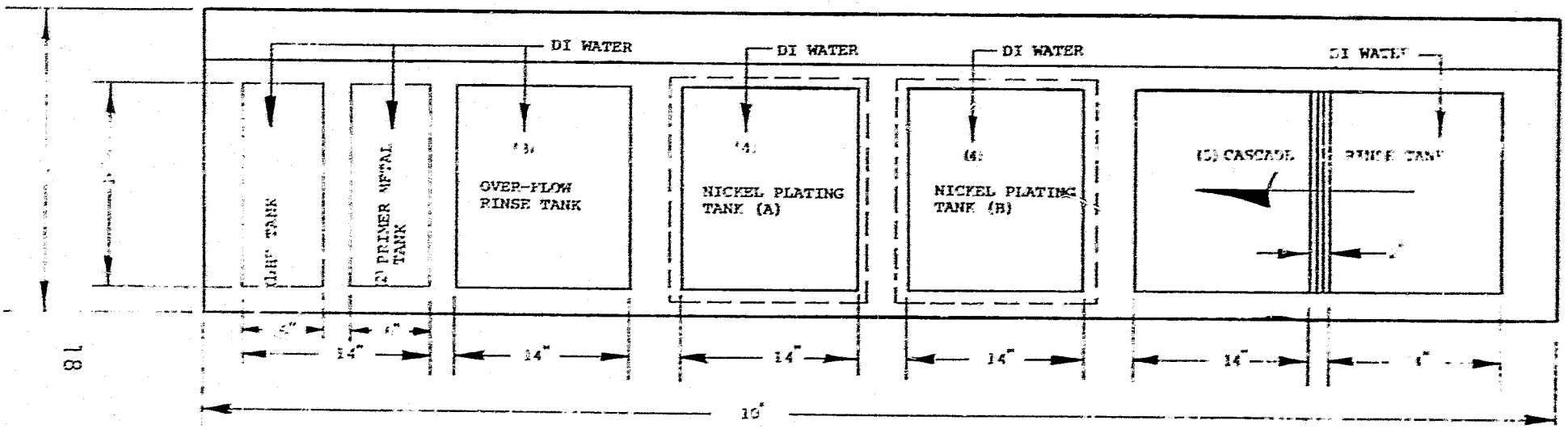
The electroless nickel plating study was performed in Task 9 of Phase 2 of the Array Automated Assembly Program (Ref. 8). The schematic diagram of the complete system is shown in Figure C-4.

Initial operation of this process begins when the wafers are placed into a hydrofluoric acid etchant tank for 30 seconds and then moved to the gold solution primer metal bath for 30 seconds. Next, the wafers are transferred by an automatic lifter to the overflow rinse tank. After repetition of three cycles of this process, a total of six wafer carriers are collected at the overflow rinse tank. These six carriers are then placed into a carrier basket which automatically transfers to the electroless nickel plating tanks where the wafers remain for five minutes in each tank. The wafers are then automatically transferred to a two stage cascade rinse system where they reside for ten minutes (five minutes in each tank).

The throughput rate for the electroless nickel plating system is 1800 wafers per hour. The machine "up" time fraction is 0.875 by assuming one hour per shift of down time.

FIGURE C-4

SCHEMATIC LAYOUT OF NICKEL PLATING SYSTEM
(1500-2500 Wafer Per Hour Capacity)



DESIGN SPECIFICATIONS

(A) DEPTH OF TANK = 18" + (3" EXHAUST OUTLET).

(B) MATERIAL: POLYPROPLENE & CORNING GLASS.

(C) THE DRAIN HOLES OF ALL TANKS ARE CONNECTED TO THE SEWER EXCEPT TANK 2 WHICH IS CONNECTED TO RESERVOIR TANK. (RESERVOIR TANK=14"x 16" x 12").

(D) EXHAUST OUTLETS ARE NEEDED FOR TANKS 1,2 & 4, USE AIR KNIFE OR AIR CURTAIN IF POSSIBLE.

(E) DI WATER LINE SHOULD BE INSTALLED AS SPECIFIED.

(F) TANK 4 REQUIRES INDIRECT DUEL WALL HEATING SYSTEM WHICH CAN HEAT 30 GALLONS OF WATER UP TO 85 C WITHIN 20 MINUTES AND MAINTAIN TEMPERATURES AT 85 C $\pm$ 5 .

(G) BOTH RINSE TANKS 3&5 REQUIRE FLOW METERS AND A CONTROL VALVE FOR WATER FLOW.

b. Supporting Data For Format A

The process cost computation for the electroless nickel plating task entailed the following cost elements.

(1) Equipment Cost

All plating equipment was designed and fabricated at Sensor Technology, Inc. The actual cost of this plating system was $8,232.32. An additional $10,000 must be added to this figure to include the fully automatic material handling system.

(2) Floor Space

Upon taking into consideration operator working space, the floor space requirement is 72 sq. ft.

(3) Labor

One operator can handle four automated systems at full capacity. The remaining labor requirements are identical to the wafer surface preparation task.

(4) Utilities and Commodities

Direct measurements from experimental test runs yielded the following material consumption rates:

a) 49% hydrofluoric acid:

0.5cc/wafer = 15 cc/min. = 0.039 lbs/min.

(sp. gr. of sol. = 1.18)

b) Gold plating solution (premixed commercial item)

0.5 cc/wafer = 15 cc/min.

c) Nickel plating solution (premixed commercial item)

5cc/wafer = 150 cc/min.

d) Nitrogen Gas

10 liters/min. for each rinse tank

Total:20 liters/min. = 0.706 cu. ft./min.

e) D.I. Water

1.5 gal./min for each rinse tank.
Total 3 gal/min = 0.401 cu. ft./min.

(f) Electric Power:

3.12 KW heater unit per tank.
This is used for 30 minutes every three hours. Therefore, the power usage factor becomes 0.1667. Power consumption per minute is 8.66 watts.

The input data used for this process cost computation may be located in the appropriate Format A of Appendix II.

5. Resist Removal (RESREM)

a) Design for High Volume Production

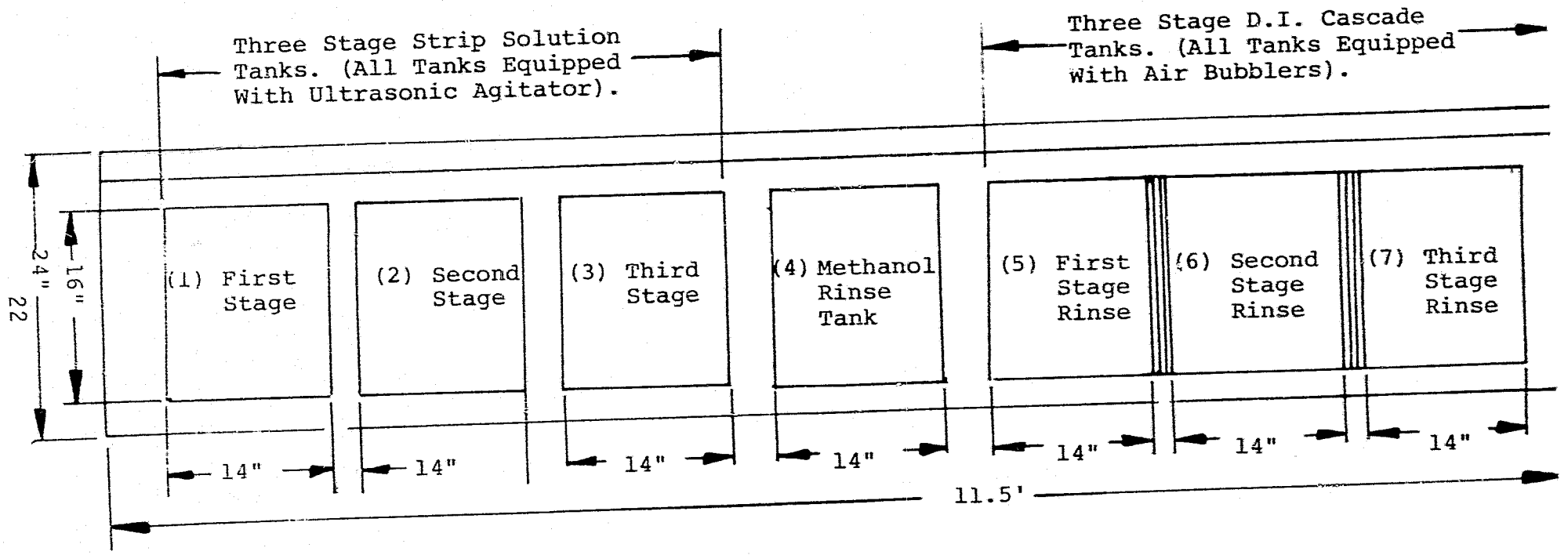
A standard wet chemical resist removal method currently used by Photowatt International, Inc. will be utilized in the large volume production line of CELLCO with the addition of an automatic wafer handling system. The schematic diagram of this system, not including the automatic material handling system, is depicted in Figure C-5. The process equipment consists of chemical solution tanks, and an automated material handling system. This resist removal process is described below.

(1) Three Stage Resist Removal System

Three, 16" x 14" x 10" process tanks are filled with resist removal solution.

After one hour of processing wafers in the three stage resist removal system, the solution in the first tank is drained. The solution in the second tank is transferred to the first tank, and solution in the third tank is transferred to the second tank. Clean resist removal solution is then supplied to the third tank. In this manner, the third process tank always contains clean solution relative to the other two tanks. Each tank can process up to six wafer carriers which each have a 25 wafer capacity. An additional 30 seconds per tank must be alotted for transfer time, which leads to a total process time of 2.5 minutes per tank. The throughput rate for this system is 3600 wafers per hour.

FIGURE C-5: SCHEMATIC LAYOUT OF WET CHEMICAL RESIST REMOVAL SYSTEM
(3,600 wafers per hour capacity)



DESIGN SPECIFICATIONS

(A) Depth Of Tank = 10" + (3 Exhaust Outlet)

(B) Material = Stainless Steel Tanks For (1), (2), (3)
Polyproplene Tanks For (4), (5), (6), (7)

(C) Solution Transfer Pump Between (3) and (2); (2) and (1)

(D) All Tanks Require Drain Cleaning

(2) Methanol Rinse Tank

After the wafers undergo resist removal, they are transferred to a 16" x 14" x 10" methanol rinse tank. The processing time at the methanol rinse tank is identical to that of the resist removal tanks to preserve process continuity.

(3) Three Stage D.I. Rinse Tanks

The final step of this process is a three stage cascade D.I. water rinse. The processing time at each of the three tanks is two minutes. An additional 30 seconds per tank must be alotted for transfer time. Consequently, the total processing time per tank is 2.5 minutes.

b. Supporting Data For Format A

(1) Equipment Cost Factor

The equipment cost of $10,000 for the resist removal process was estimated directly from current equipment prices in the commercial market. The carrier transfer mechanism was estimated to be $2,000. The useful equipment lifetime is seven years as recommended by IPEG.

(2) Labor and Floor Space

The floor space requirement of 64 ft^2. was estimated directly from the schematic diagram shown in Figure C-5. One operator is sufficient

to operate four complete systems without any difficulty, provided that an automated material handling system is included within the resist removal system. The remaining direct labor requirements are identical to the wafer surface preparation task.

(3) Commodities and Utilities

All material and utility consumption rates were estimated on the basis of actual experimental data.

All input data utilized in the process cost computation of the resist removal process may be located in the appropriate Format A of Appendix II.

6. Laser Trimming Process (LAST)

a) Design for High Volume Production

Figure C-6 shows the major components of a serial flow laserscribing system. This unit is comprised of 2 loaders, 2 aligners, 3 dual beam lasers, 2 wafer crackers and a moving surface onto which are mounted, at evenly spaced intervals, wafer holding chucks. One wafer at a time is removed from its storage container and transferred onto a holding chuck which carries the wafer through the scribing process. The wafer is moved along by conveyor to the wafer aligner where the wafer grid lines are oriented in preparation for scribing. The wafer is then passed under a dual beam laser whose beams are aligned and focused so that two parallel sides of a cell

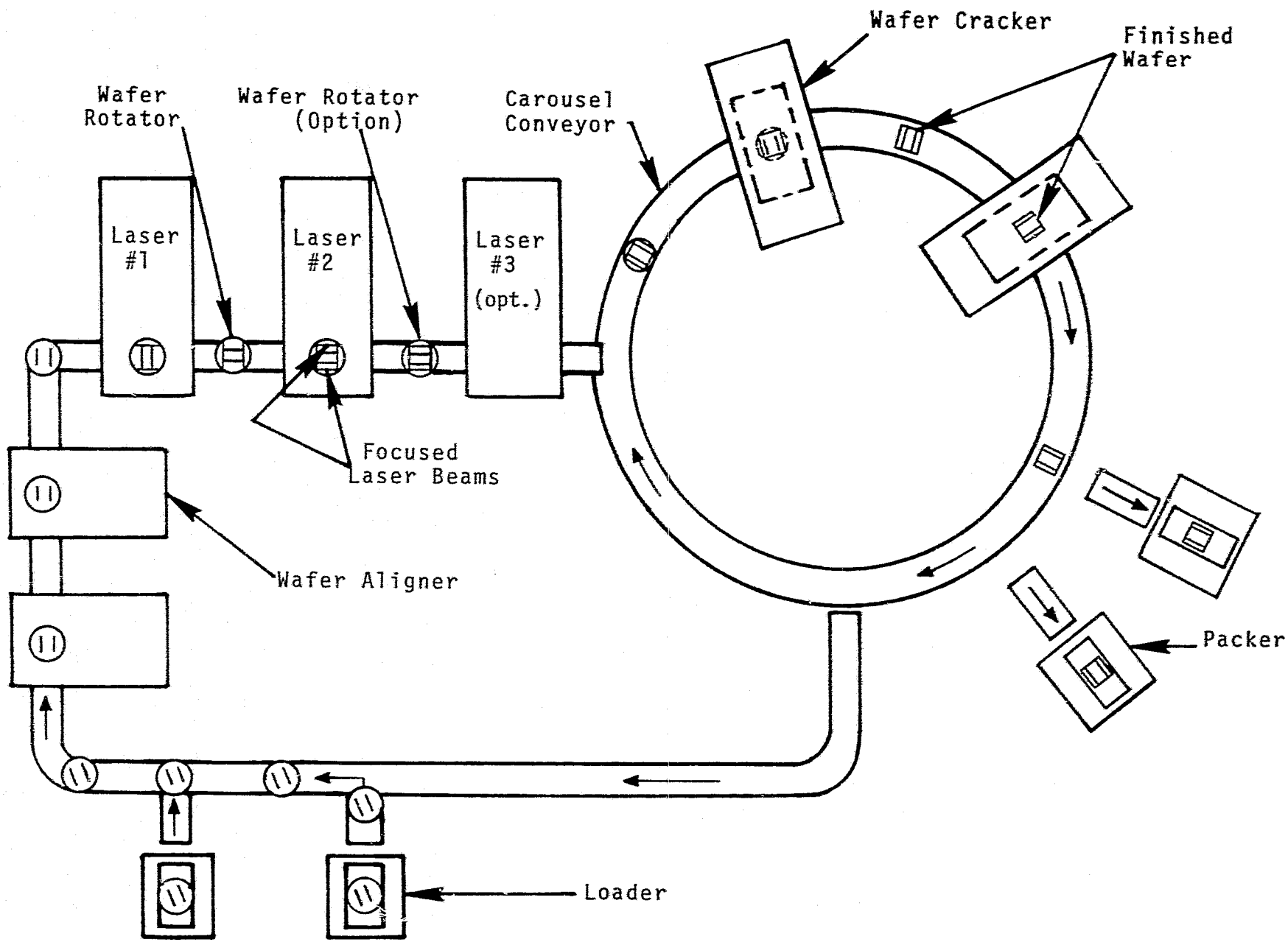


Figure C-6. Serial Flow Laserscribe Trimming System for 7200 Wafers per Hour.

are simultaneously scribed. The wafer is then moved at a constant speed to the rotator chuck where it is indexed to turn the wafer 90° for a square rectangular cell (or 60° for a hexagon). The wafer is next moved to laser number 2 where a second pair of parallel sides are scribed. The scribed wafer then moves along the conveyor to the carousel conveyor (or the optional rotator and laser number 3 can be utilized to scribe a hexagon or utilized during down-time for one of the first two lasers).

The finished wafers are finally off-loaded from the cracker and loaded back onto the carousel conveyor which carries them to the wafer scanner where each wafer is examined for completeness of scribing. Acceptable wafers are returned to storage containers; defective wafers are diverted to the defective wafer packer. The empty chucks are transferred to the return conveyor and to the loader to receive the next wafer. The scrap silicon, meanwhile, is collected and returned to the recycling station.

The serial flow laserscribing system contains several subunits which are utilized for manipulation and transfer of wafers through the scribing operation. These subunits include: (1) two wafer loaders, (2) wafer aligner, (3) wafer cracker, (4) wafer rotator, and finally, (5) wafer distribution unit.

The present state of laser development allows scribing silicon wafers at speeds up to 4 inches/second. It is expected that laser output will improve by 4 times in 1986, so that scribing speeds of 10 in /sec with a dual beam laser will be feasible. The wafer throughput will be 2 wafers per second since the conveyor speed is 10 inches/second and the wafers are spaced on 5 inch centers. Wafer yield is 7200 wafers/ hour.

b) Supporting Data For Format A

The process cost estimation for the Hexagonal Laserscribing Process entailed the following cost elements.

(2) Equipment Cost Factors

The equipment prices are in terms of 1978 cents, and are based on the criterion that 15 complete systems will be manufactured. The subunit costs are given below:

Subunit	Quantity	Unit Price (Thousand Dollars)	Total Thousand Dollars)
Laser	3	30	90
Loader	2	3	6
Aligner	2	3	6
Packer	2	3.5	7
Carousel Conveyor	1	15	15
Rotator	3	2	6
Main Conveyor	1	40	40
Sensor	1	5	5
Wafer Chuck	40	0.5	20
		Total (Thousand Dollars)	195

(3) Labor and Floor Space

The floor space requirement takes into consideration the actual floor space utilized by the entire laserscribing system, and also an additional three feet of clearance around the unit for working space. One operator will operate one unit per shift. The remaining direct labor requirements are assumed to be identical to the wafer surface preparation task.

(4) Commodities and Utilities

a. Spare Parts

Eight percent of the equipment cost is allocated for spare parts. This will cover the spare-part requirement for the lifetime of the unit, which is six years.

b. Cooling Water

7 gallons/minute of cooling water is required for an input of 8 kw of electrical power. For this unit, which requires an input of 24 kw of electrical power, the coolant requirement becomes 42 gallons/minute.

c. Electric Power

The present electrical power conversion efficiency of lasers is 0.29%. The laser power needed to scribe at a rate of 10 in./sec. is 32 watts/beam which implies that an electrical power input of 11.09 kw/beam is required. Since each laserscribing machine utilizes 6 beams, the power requirement is 66.54 kw/machine. By assuming that the laser efficiency will increase to 0.3% by 1986, the required electrical power input will be 64 kw/machine. An additional 3 kw of electrical power must be considered for support electronics, thus bringing the total power requirement per unit to 67 kw.

7. Solder Flow and Flux Removal (SDFLW)

a. Design for High Volume Production

A 3600 wafer per hour conceptual solder dipping and flux removal system was designed for use in the high volume production line of the CELLCO firm. The schematic diagram of the conceptual solder dipping and flux removal system is shown in Figure C-7.

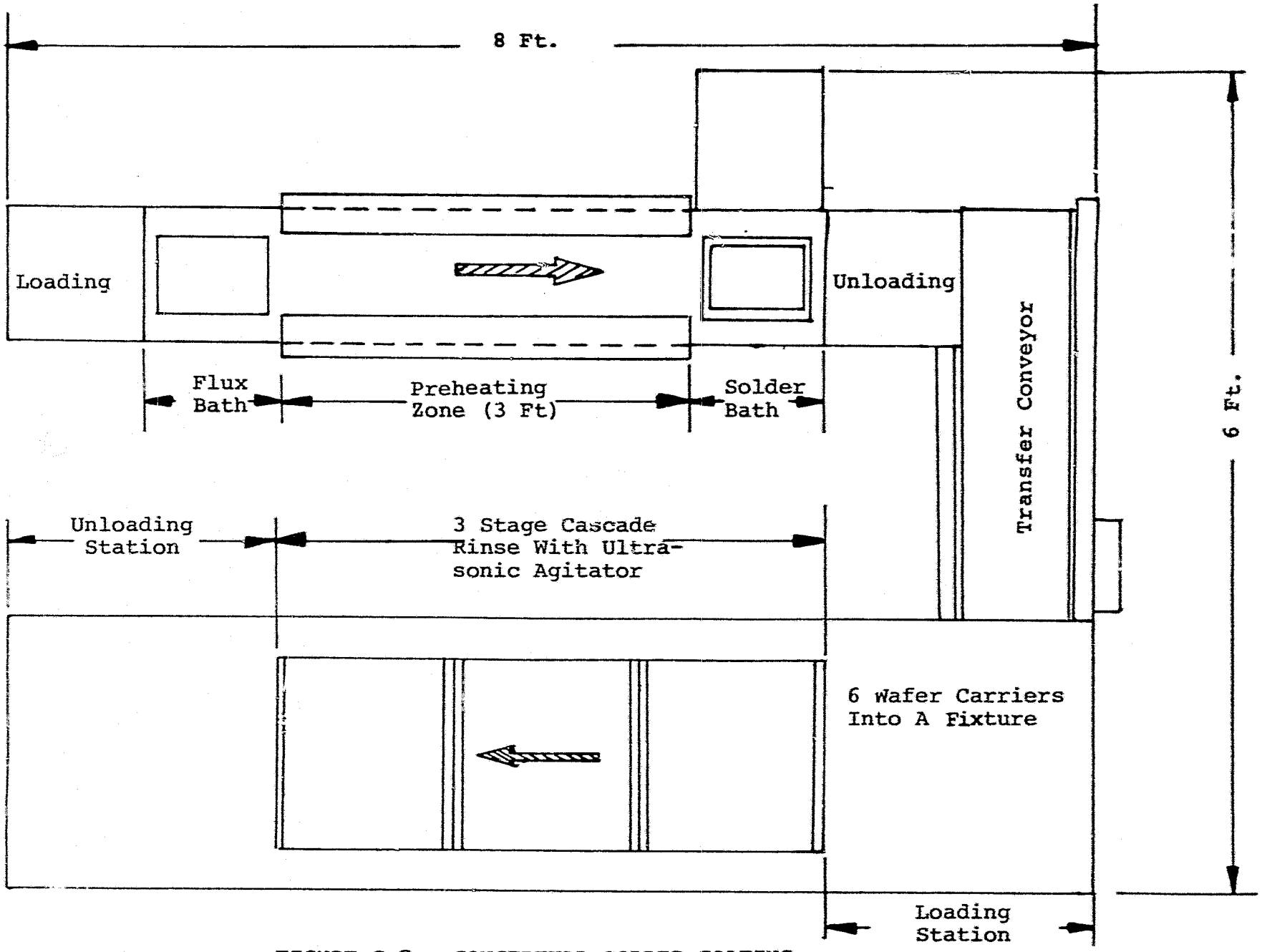


FIGURE C-7: CONCEPTUAL SOLDER COATING AND FLUX REMOVAL SYSTEM (3,600 wafers/min.)

The sequential operation of this system is discussed below:

(1) Flux Application

A standard dipping procedure of silicon wafers into soluble flux is performed initially.

(2) Preheating Silicon Wafers

Preheating silicon wafers prior to immersion into the solder bath is highly recommended as a precautionary measure against thermal shock. The recommended preheating temperature is between 150 and 200.

(3) Solder Dipping

A fully loaded Fluoroware Teflon PFA wafer carrier is submerged into a solder bath which is maintained at a temperature of $475^{o} \pm 25^{o}$F. The duration of this dipping procedure is 5-10 seconds. The solder bath must be an overflow bath in order to achieve steady solder flow at a uniform temperature.

(4) Flux Cleaning

Since the flux utilized in this process is water soluble, a three stage cascade D.I. wafer rinse will suffice for flux removal. It was found experimentally that an ultrasonic agitator in conjunction with a D.I. water rinse will remove flux far more efficiently than D.I. water alone. By considering transfer times, the processing time is 2.5 minutes at each tank in the three stage cascade D.I. water rinse system. The D.I. water temperature should be 90^{o}C, so as to preclude the need for a separate drying cycle.

b) Supporting Data for Format A

The process cost estimation for the solder flow and flux removal process entailed the following cost elements.

(1) Process Characteristics

The throughput rate for this process is 60 wafers/minute. The average time spent at this station is 13.33 minutes. The machine "up" time fraction is assumed to be 0.875 by taking into account one hour of machine down time per shift.

(2) Equipment Cost Factors

The estimated cost of the conceptual high volume throughput solder flow and flux removal system is as follows:

Soldering process:	$ 9,000
Three stage cascade rinse:	$11,500
Material Handling:	$ 5,000
Total	$25,500

(3) Labor and Floor Space

The estimated floor space requirement which includes working space, is 80 ft^2. One operator can operate four units. All remaining direct labor requirements are identical to the wafer surface preparation task.

(4) Commodities and Utilities

The chemical and direct material consumption rates are scaled up proportionately from the values used in the current production line. The electrical power consumption rate for the conceptual high volume

throughput solder flow and flux removal system has been estimated as follows:

Preheater:	3 kw
Solder Bath:	5 kw
Ultrasonic Generator:	3 kw
D.I. Water Heater:	3 kw
Material Handling:	1.5 kw
Total	15.5 kw

All input data utilized for this process cost computation may be located in the appropriate Format A of Appendix II.

8. Antireflective Coating (ARCT)

a) Design for High Volume Production

The LFE system 8000 silicon nitride plasma depositor shown in Figure C-8 was selected for use in this AR coating process sequence.

The LFE System 8000 is composed of a vacuum processing chamber which contains five separate process zones with the wafer receiving 20% of its total film in each zone in a sequential manner. The wafer passes through a vacuum lock at the entrance of the chamber through an identical vacuum lock after it has been processed at all five process locations. Upon completion of this procedure, a fully coated wafer will emerge every 120 seconds. This throughput rate will need to undergo considerable improvement in order to meet the 1986 LSA program goals. During the course of this study, it was concluded that the LFE system 8000 could be utilized for large volume production by simply performing minor equipment modifications.

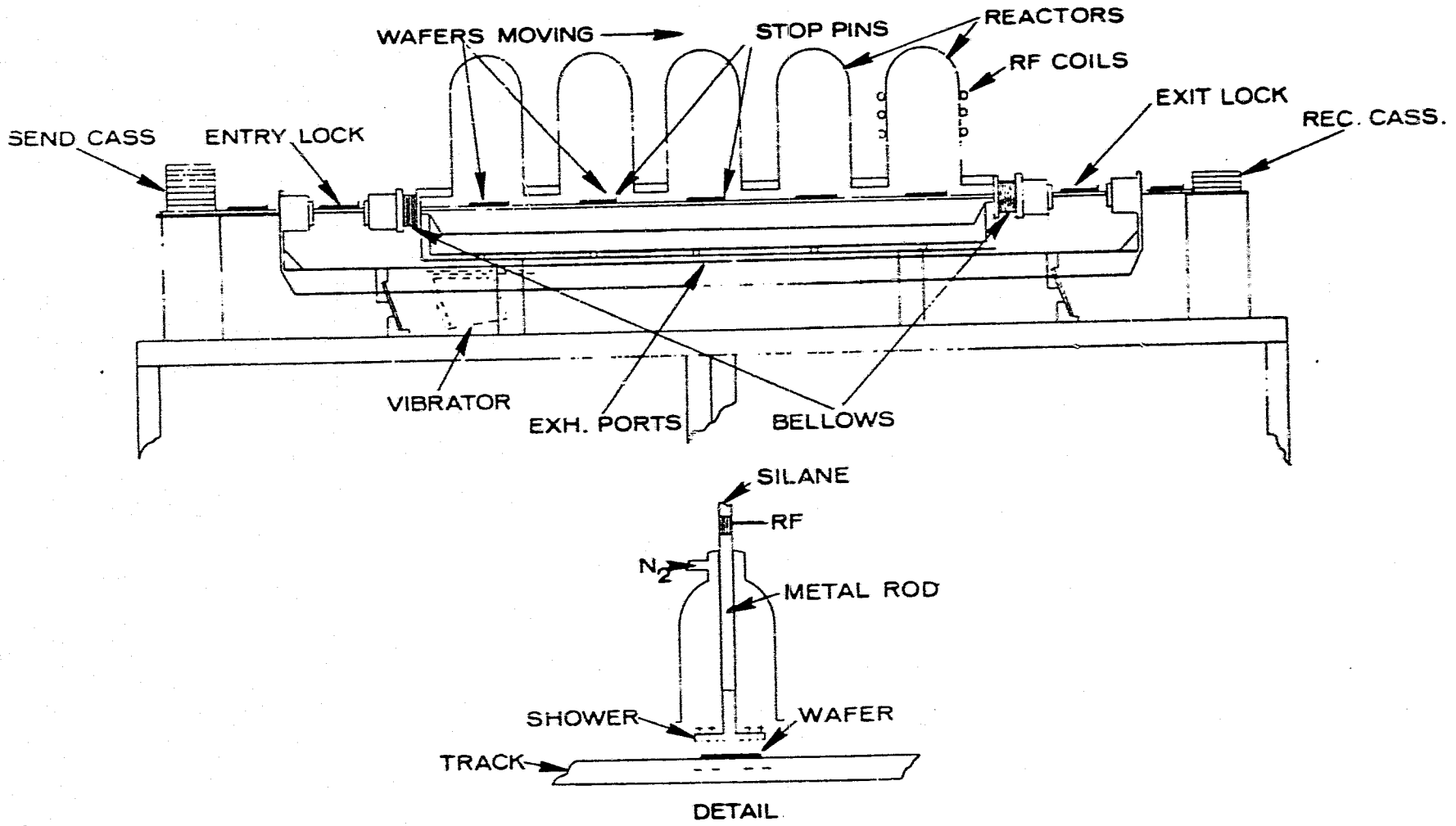


Figure C-8 LFE 8000 system for silicon nitride anti-reflective coating.

The key design modifications which will lead to an enhanced wafer throughout are discussed below:

(1) The wafer velocity on the process track should be increased and the positioning control improved. It is imperative that the wafer velocity on the process track be increased from 2 inches per second to 3 inches per second. This can be achieved by redesigning the vibratory subsystem so that an upper velocity limit is established. Since each wafer must be accurately positioned in the process zone in order to obtain the proper degree of film uniformity, it is necessary to provide a "stop pin" on the process track. The stop-pins retreat into the track during wafer movement and then resurface when the wafer movement ceases. The wafer movement is controlled by a microprocessor which receives wafer positioning data from the capacitive sensors which are imbedded in the process track. The microprocessor controls the turn-on of the vibratory mechanism and the stop-pins in accordance with the particular timing sequence under consideration and wafer positioning information.

(2) The wafer transition time through the vacuum locks should be decreased. The transition time of a single wafer from the sender to the vacuum lock and then from the vacuum lock to the process chamber is 30 seconds for the present system. In order to

move five wafers through this sequential transition operation within a 40 second time period a new design is required. This new design has a cassette mechanism located within the entry lock (and also the exit lock) allowing for a buffer of five wafers in the "ready" zones, namely, the entry and exit locks. As each wafer moves into the lock cassette, the cassette will index up (or down) one notch in preparation for the next wafer until all five wafers are received (or dispatched in the case of the exit lock).

By adopting the above mentioned equipment modifications, a wafer throughput rate of 300 wafers per hour will be achieved. Despite the fact that this enhanced wafer throughput rate is still not suitable for the 1986 standard industry, it is useful to obtain this process cost as a means of comparing competing A.R. coating methods. Consequently, the modified LFE System 8000 was utilized in the high volume production line of the CELLCO firm.

b) Supporting Data For Format A

The process cost estimation for the anti-reflective coating process entailed the following cost elements.

(1) Equipment

The modifications which will take place are: (1) a new vibratory conveyor system, (2) a new buffer cassette at the entry and exit locks, and (3) a larger microprocessor. The estimated cost of the

modified system will be $14,000 provided that more than 20 complete units are ordered.

(2) Floor Space and Labor

The floor space estimation, including working space is 40 ft^2. It is assumed that one operator can handle up to 10 units, since the equipment is fully automated and processing control is exercised exclusively through a microprocessor. Other direct labor requirements are identical to the wafer surface preparation task.

(3) Utilities and Commodities

Utilities: Since the deposition rate will remain unchanged, the power increase will be due exclusively to the wafer handling unit. It was estimated that the total electric power consumption rate will increase by 25%. The power requirement of the modified equipment will therefore be 10.29kw.

Materials: Since the gas consumption rate is contingent upon the film deposition rate, the gas consumption rate will remain identical to that of the current module.

All input data utilized for this process cost computation may be located in the appropriate Format A of Appendix II.

9. Cell Testing (CELTEST)

a) Design for High Volume Production

The conceptual automated solar cell testing system shown in Figure C-9 was designed. This solar cell testing system is able to test and group 3600 solar cells per hour. The sub-units which comprise this system are described below:

(1) Cell Loader

Five cassettes which contain 25 solar cell each, are loaded onto solar cell feeders. One solar cell from each cassette is simultaneously loaded onto one of five pneumatic conveyors. The time for simultaneously loading 5 solar cells is 5 seconds. Therefore, the throughput rate for this process step is 1 solar cell per second.

(2) Light Tower

One, 650 watt Xenon light tower is located at each of the 5 conveyor tracks. Each light tower is equipped with a suitable reflector and power regulator for maintaining uniform light intensity. A stopping mechanism will halt the motion of the conveyor for 5 seconds when the solar cells arrive at the light towers, so that electrical performance tests may be performed.

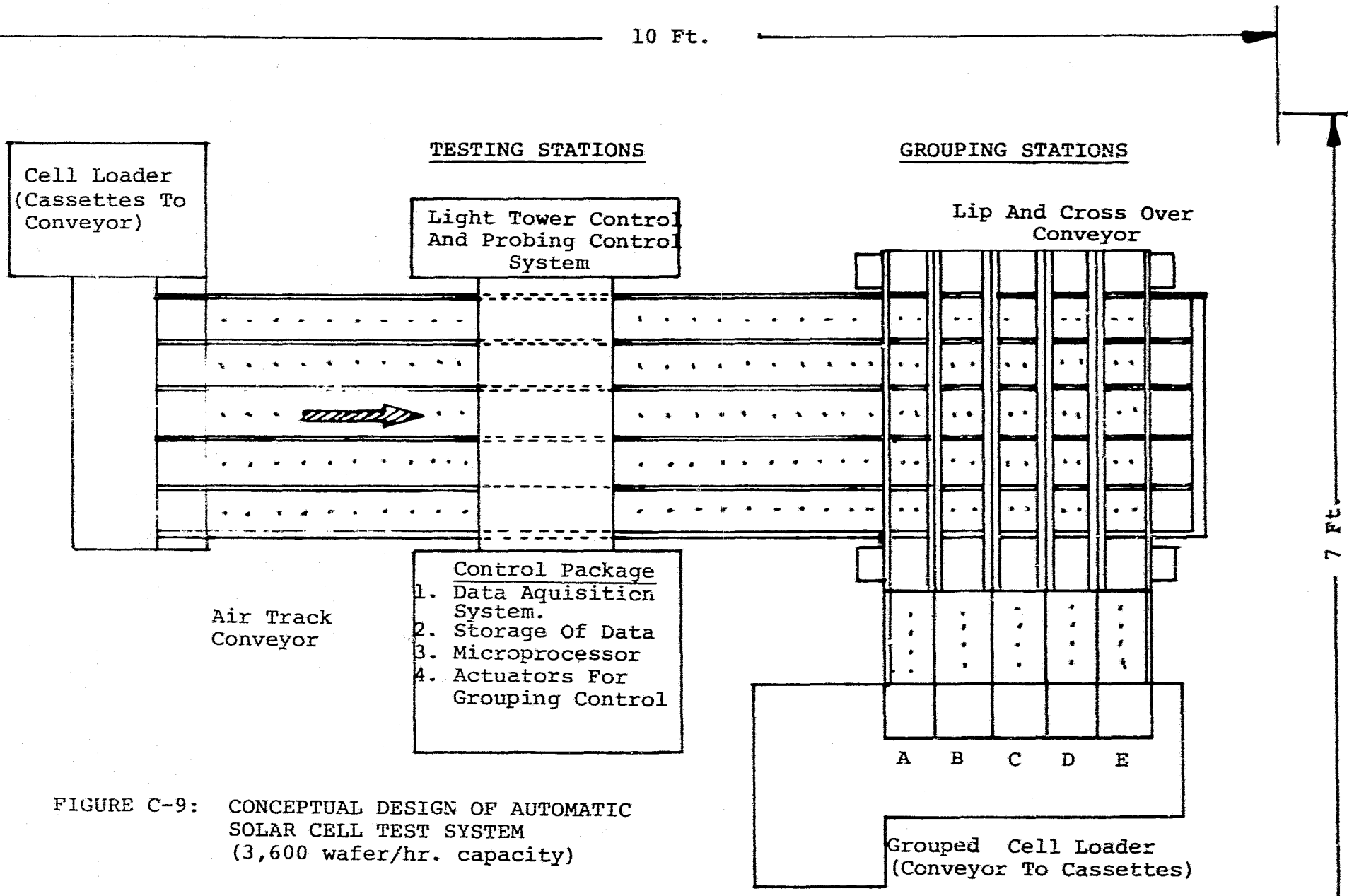


FIGURE C-9: CONCEPTUAL DESIGN OF AUTOMATIC SOLAR CELL TEST SYSTEM (3,600 wafer/hr. capacity)

(3) Probing Mechanism and Data Acquisition

When a solar cell stops at the light tower, a probing mechanism will make contact with it. Electrical performance data is subsequently recorded in the microprocessor unit through electronic simulator sampler circuits. The microprocessor will analyze and store this data, as well as compute the maximum power point. It also exercises control over the stopping mechanism in the grouping station.

(4) Grouping Station

Incoming solar cells will stop at one of five stopping stations on the basis of input data supplied by the microprocessor. A cross pneumatic conveyor will then activate solar cell motion in the transverse direction, until the solar cell arrives at the storage area.

(5) Cell Unloader

Five cassettes are loaded with grouped solar cells at this station. The loaded cassettes are then transported to the module fabrication station. Rejected solar cells are stored at a separate storage area.

b) Supporting Data For Format A

The process cost estimation for the cell testing process entailed the following cost elements:

(1) Equipment

The estimated cost of each machine element is as follows:

Loader:	$ 2,500
Conveyors:	$ 1,000
Light Tower and 2 Probes:	$18,500
Grouping Station:	$ 8,000
Unloader:	$ 2,500
Data Acquisition:	$15,000
Total	$47,500

(2) Floor Space and Labor

Floor space, including work space, was estimated to be 70 $ft.^2$. One operator is sufficient to operate four units. The remaining direct labor requirements are identical to the wafer surface preparation task.

(3) Utilities and Commodities

The electrical power requirement for this process was estimated as 8.25 kw. There are no commodity requirements.

The input data utilized for this process cost computation may be located in the appropriate Format A of Appendix II.

PRICE COMPUTATION

The price of a solar cell was determined after all the data required for each Format A was compiled. The cost computation proceeded in accordance with the procedure outlined for the process worksheet and company worksheet described in reference(3). Additional expense item information, which was not included in the cost account catalog in Reference(7), was found in currently available market price literature.

The total cost incurred at each solar cell process step was manually calculated and can be found in Table 1. The cost for each process was further subdivided into independent elements which consist of the cost in terms of 1975 cents per peak watt for space, labor, materials and utilities.

Table 1 CELLCO Process Cost Summary in 1975 Cents per Peak Watt.

Process Numbers	Process Referent	Equipment	Floor Space	Labor	Material & By-Products	Utilities	TOTAL
C-1	WFSURPR	.200	.072	.440	.780	.190	1.682
C-2	JUNF	.550	.174	.570	1.200	.641	3.135
C-3	FSPP	.128	.110	.270	.424	.050	.982
C-4	ELNIPL	.084	.038	.430	3.810*	.138	4.500*
C-5	RESREM	.027	.017	.220	1.636	.109	2.009
C-6	LAST	.270	.030	.350	.004	.123	.777
C-7	SDFLW	.050	.021	.210	1.900	.213	2.394*
C-8	ARCT	1.861*	.124	.940	.800	.274	3.999*
C-9	CELLTEST	.100	.018	.185	0	.018	.321
TOTAL		3.270	.604	3.615	10.554	1.756	19.80

*Highest Cost Element

DISCUSSION OF RESULTS

The total added value for CELLCO is 19.8 cents per peak watt in 1975 cents. This value is slightly higher than the PAG[5] price goal of 18.3 cents per peak watt. As shown in Table 1, metallization (Step C-4) and AR coating (Step C-8) processes claim a disproportionate share of the total cost for CELLCO.

The major shortcoming of the current electroless nickel plating metallization process is its use of costly materials. This process sequence requires the use of front surface resist pattern printing (Step C-3), electroless nickel plating (Step C-4), resist removal (Step C-5) and solder flow (Step C-7), which adds up to 9.885 cents per peak watt or more than 50% of the cell processing cost. A process sequence that utilizes, for example, a low-cost printed metallization pattern would eliminate the resist application and resist removal steps and would reduce direct material costs. A lower cost conducting material to replace solder would significantly reduce the cost of Step C-7.

It is highly recommended that future efforts be directed toward these areas to reduce the costs of the metallization process sequence.

The major shortcomings of the silicon nitride plasma deposition AR coating process resides in its high equipment cost. One candidate procedure exhibiting high potential for success in this task is spray-on AR coating. An in-depth study of the application of low-cost spray-on AR coating techniques to polysilicon solar cells is recommended.

CONCLUSIONS AND RECOMMENDATIONS

It can be concluded from a detailed SAMICS analysis that the solar cell process costs are in line with the 1986 LSA cost goals.

A significant reduction in the overall solar cell fabrication cost can be achieved by reducing the metallization and antireflective coating costs. Recommended procedures for reducing the cost of these two procedures are printed metallization and spray-on antireflective coating, respectively.

REFERENCES

1. JPL 5101-44A, SAMICS INPUT DATA PREPARATION.

2. JPL 5101-59, SAMICS Usage Update No. 1.

3. JPL 5101-15, SAMICS Workbook.

4. JPL 5101-33, Interim Price Estimation Guidelines.

5. JPL 5101-68, Price Allocation Guidelines.

6. G.T. Jones, Automated Array Assembly Task, Development of Low-Cost Polysilicon Solar Cells, Draft Final Report, June 1980.

7. JPL 954800-77/21, Cost Account Catalog.

8. S.S. Rhee, G.T. Jones and K.L. Allison, DOE/JPL 954865-79/5, Phase 2 Array Automated Assembly Task, Annual Report, JPL Contract 954865, LSA Project, Automated Array Assembly Task, January 1979 by Sensor Technology, Inc.

INDUSTRY DESCRIPTION, FORMAT C

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT C

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

INDUSTRY DESCRIPTION

C1 Industry Referent SAMICS - 86

C2 Description (Optional) 1986 Standard Industry

INDUSTRY OBJECTIVE

C3 Industry Result Lower Cost Polysilicon Solar Cells

C4 Quantity Produced 530.4 Megawatts per year

DESCRIPTION OF THE FINAL PRODUCT OF THE INDUSTRY

C5 Reference PV CELL Name Photovoltaic Cell

C6 Production is Measured in 278 million cells per year

C7 Hardware Performance 0.636 watts per cell (C4 per C6)

C8 Product Design Description (Optional) Polysilicon solar cells with a minimum cell area of 51.3 cm^2 producing 0.636 watts at 100 mw/cm^2, 28^oC insolation.

MAKERS OF THE FINAL PRODUCT OF THE INDUSTRY

C9 Company Reference CELLCO* Market Share 33.3%

Company Reference _____ Market Share _____

Company Reference _____ Market Share _____

*The remaining companies are smaller than CELLCO and are not listed.

Prepared by _____ Date _____

JPL 3039-S 11/77

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APPENDIX II

COMPANY DESCRIPTION, FORMAT B

AND

PROCESS DESCRIPTION, FORMAT A

FOR

CELLCO FIRM

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT B

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

COMPANY DESCRIPTION

B1 Company Referent CELLCO

B2 Description (Optional) Standard 1986, Wafer-To-Cell Company

B3 Product Produced PVCELL

B4		Process	CELTEST
B5	Intermediate Product ARCC	Process	ARCT
	Intermediate Product SDC	Process	SDFLW
	Intermediate Product HEXC	Process	HEXLS
	Intermediate Product CLNC	Process	RESREM
	Intermediate Product NIPLC	Process	ELNIPL
	Intermediate Product FSPPW	Process	FSPP
	Intermediate Product JUNFW	Process	JUNCF
	Intermediate Product SURPRW	Process	WFSURPR
	Intermediate Product	Process	
	Intermediate Product	Process	
	Intermediate Product	Process	

B6 Purchased Product PWAFER

B7 Supplier Company Reference WAFERCO Percent Supplied 100%

Supplier Company Reference Percent Supplied

Prepared by Date

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr / Pasadena, Calif 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] SFSURPR

A2 [Descriptive Name] Wafer Surface Preparation

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] SURPRWF

A4 Descriptive Name [Product Name] Texturized and Surface Cleaned Wafer

A5 Unit Of Measure [Product Units] Wafer

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	99.5	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	96	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	PROTNK	DRTUN	WFHDMC
A9a	Component [Descriptive Name] (Optional)	Process Tanks	Drier Tunnel	Wafer Handling
A10	Base Year For Equipment Prices [Price Year]	1978	1978	1978
A11	Purchase Price ($ Per Component) [Purchase Cost]	$120,000	$31,000	$20,000
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	7
A13	[Salvage Value] ($ Per Component)	$10,000	$3,000	$1,000
A14	[Removal and Installation Cost] ($/Component)	$4,000	$2,000	$500

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

FORMAT A

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California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] JUNCF

A2 [Descriptive Name] Junction Formation by Spray-On Dopant Process Method

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] JUNFW

A4 Descriptive Name [Product Name] Wafer with junction formation and back surface field

A5 Unit Of Measure [Product Units] Wafer

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	19.9	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	107	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	SPRMC	DRFURN	ETCHMC.
A9a	Component [Descriptive Name] (Optional)	Spray-on System	Dopant Drive-in	Excess Dopant
A10	Base Year For Equipment Prices [Price Year]	1978	1978	1978
A11	Purchase Price ($ Per Component) [Purchase Cost]	48200	25500	13500
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	7
A13	[Salvage Value] ($ Per Component)	5000	2500	1000
A14	[Removal and Installation Cost] ($/Component)	1000	500	200

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] FSPP

A2 [Descriptive Name] FRONT SURFACE PATTERN PRINTING

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] FSPPW

A4 Descriptive Name [Product Name] Front Surface Printed Wafer

A5 Unit Of Measure [Product Units] Wafer

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	49.8	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	16	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	Printer	Drier	
A9a	Component [Descriptive Name] (Optional)			
A10	Base Year For Equipment Prices [Price Year]	1978	1978	
A11	Purchase Price ($ Per Component) [Purchase Cost]	20,000	30,000	
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	
A13	[Salvage Value] ($ Per Component)	2,000	3,000	
A14	[Removal and Installation Cost] ($/Component)	200	1,500	

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] ELNIPL

A2 [Descriptive Name] Electroless Nickel Plating.

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] NIPLC

A4 Descriptive Name [Product Name] Nickel Plated Cell

A5 Unit Of Measure [Product Units] Cell

PART 2 – PROCESS CHARACTERISTICS

A6 [Output Rate] (Not Thruput) 29.82 Units (given on line A5) Per Operating Minute

A7 Average Time at Station [Processing Time] 20 Calendar Minutes (Used only to compute in-process inventory)

A8 Machine "Up" Time Fraction [Usage Fraction] 0.875 Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS (Machine Description)

A9	Component [Referent]	NIPLTK	MTLHNDL	
A9a	Component [Descriptive Name] (Optional)	Nickel Plating System	Programable Material Handling system	
A10	Base Year For Equipment Prices [Price Year]	1978	1978	
A11	Purchase Price ($ Per Component) [Purchase Cost]	8232	10,000	
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	
A13	[Salvage Value] ($ Per Component)	800	1,000	
A14	[Removal and Installation Cost] ($/Component)	900	1,000	

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) ELNIPL

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	72	sq. ft.	Factory Space
B 3672 D	0.25	prsn.a yr.	Chemical Operator II
B 3720 D	0.05	" " "	Inspector (Q.C.)
B 3736 D	0.03	" " "	Maintenance Mech. II
B 3688 D	0.02	" " "	Electronic Maint.
B 3256 B	0.01	" " "	Production Planner

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
E 1328 D	0.039	lbs.	Hydrofluoric Acid
ET 1007 D	0.015	liter	Gold Solution
ET 1008 D	0.150	liter	Nickel Solution
E 1416 D	0.706	cu.ft.	Nitrogen gas
C 1144 D	0.401	cu.ft.	D.I. water
C 1032 B	0.0087	Kw.Hr.	Electricity
D 1176 D	0.180	Cell	Rejected Cell

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
FSPPW	0.994	Cell/ Wafer	Front Surface Pat. Print Wafer
		/	
		/	

Prepared by _____ Date _____

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FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] RESREM

A2 [Descriptive Name] THICK RESIST REMOVAL BY WET CHEMICAL METHOD

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] CLNC

A4 Descriptive Name [Product Name] Cleaned Photovoltaic Cell

A5 Unit Of Measure [Product Units] Cell

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	60	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	17.5	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	STRIPTANK	Hoist	
A9a	Component [Descriptive Name] (Optional)	Stripper Tank System	Lifter for basket transfer	
A10	Base Year For Equipment Prices [Price Year]	1978	1978	
A11	Purchase Price ($ Per Component) [Purchase Cost]	10,000	2,000	
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	
A13	[Salvage Value] ($ Per Component)	1,000	500	
A14	[Removal and Installation Cost] ($/Component)	1,000	500	

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method] and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) RESREM

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	64	Sq.ft.	Floor Space (Type A)
B 3672 D	0.25	Prsn.a yr.	Chemical Operator II
B 3736 D	0.05	" " "	Inspector (Q.C.)
B 3720 D	0.03	" " "	Mechanical Maintenance
B 3688 D	0.02	" " "	Electric Maintenance
B 3256 B	0.01	" " "	Production Planner

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
ET 1009D	0.210	l/min.	Strip solution
ET 1002D	0.084	l/min.	Methanol
C 1144 D	0.4813	Cu.ft./min.	D.I.water
C 2032 D	0.0138	Cu.ft./min.	Clean Comp Air.
C 1032 B	0.2064	Kw.hr./min.	Electricity
D 1048 B	3.68	Gal/min.	Polluted water
D 1064 D	0.030	Cell/min.	Rejected cell.

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
NIPLC	0.9995	Cell / Cell	Cleaned cell
		/	
		/	

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REVERSE SIDE JPL 3037-3 R 7/78

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] LAST

A2 [Descriptive Name] Laser Trimming Operation

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] TCELL

A4 Descriptive Name [Product Name] Trimmed Cell

A5 Unit Of Measure [Product Units] Cells

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	119.4	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	0.317	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.95	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	LASERSCRIBE		
A9a	Component [Descriptive Name] (Optional)			
A10	Base Year For Equipment Prices [Price Year]	1986		
A11	Purchase Price ($ Per Component) [Purchase Cost]	520,000		
A12	Anticipated Useful Life (Years) [Useful Life]	6		
A13	[Salvage Value] ($ Per Component)	78,000		
A14	[Removal and Installation Cost] ($/Component)	15,600		

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) LAST

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	250	sq.ft.	Factory Space
B 3704 D	1.0	Prsn.-yr.	Machine Operators
B 3720 D	0.1	Prsn.-yr.	Inspector (Q.C.)
B 3736 D	0.06	Prsn.-yr.	Maintenance
B 3688 D	0.04	Prsn.-yr.	Electronics Main.
B 3256 B	0.02	Prsn.-yr.	Production Planner

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
E 1608 D	0.0079	dollar/min.	Spare parts
C 1016 B	5.615	uA/min.	Cooling water
C 1032 B	1.112	Kw-hr/min.	Electric power
D 1176 D	0.60	Cell/min.	Rejected Cell

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
CLNC	0.995	Cells/Cells	Cleaned cells
		/	
		/	

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FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] SDFLOW

A2 [Descriptive Name] SOLDER COATING AND FLUX REMOVAL

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] SDC

A4 Descriptive Name [Product Name] Solder Coated Cell

A5 Unit Of Measure [Product Units] Cell

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	59.88	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	13.333	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	SDMC	FLCLMC	MATHNOL
A9a	Component [Descriptive Name] (Optional)	SOLDER Coating Machine	FLUX Cleaning Machine	MATERIAL Handling Machine
A10	Base Year For Equipment Prices [Price Year]	9,000	11,500	5,000
A11	Purchase Price ($ Per Component) [Purchase Cost]	1978	1978	1978
A12	Anticipated Useful Life (Years) [Useful Life]	7	7	7
A13	[Salvage Value] ($ Per Component)	1,800	2,000	1,000
A14	[Removal and Installation Cost] ($/Component)	500	300	500

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) SD FLOW

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	80	Sq.Ft.	Factory Space (Type A)
B 3672 D	0.25	Prsn.a yr.	Chemical Operator II
B 3720 D	0.05	Prsn.a Yr.	Inspector
B 3736 D	0.03	" " "	Mechanical Maintenance
B 3688 D	0.02	" " "	Electrical Maintenance
B 3256 D	0.01	" " "	Production Planner

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
ET 1010 D	1.5×10^{-3}	Gal/min.	Solder Flux
ET 1011 D	0.090	lbs/min.	60/40 Solder
C 1144 D	1.069	Cu.ft.	D.I. water
C 1032 B	0.2583	Kw.hr/min.	Electricity
D1048 B	8.0	Gal/min.	Polluted Water
D 1176 D	0.12	Cell/min.	Rejected Cell

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
TCELL	0.998	Cell / Cell	Trimmed Cell
		/	
		/	

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FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] ARCT

A2 [Descriptive Name] Silicon Nitride Anti-Reflection Coating

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] ARCC

A4 Descriptive Name [Product Name] AR COATED CELLS

A5 Unit Of Measure [Product Units]

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	4.98	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	.20	Calendar Minutes (Used only to compute in-process Inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	LFES		
A9a	Component [Descriptive Name] (Optional)	LFE 8000		
A10	Base Year For Equipment Prices [Price Year]	1978		
A11	Purchase Price ($ Per Component) [Purchase Cost]	74,000		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	10,000		
A14	[Removal and Installation Cost] ($/Component)	5,000		

Note: The SAMICS III computer program also prompts for the [payment float interval], the [inflation rate table], the [equipment tax depreciation method], and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) ARCT

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) **OR PER MACHINE PER SHIFT** (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	40	Sq.ft.	Factory Space (Type A)
B 3704 D	.1	Prsn.yr.	Operator
B 3736 D	.01	Prsn.yr.	Maintenance Mech II
B 3256 B	.005	Prsn.yr.	Production Planner
B 3720 D	.005	Prsn.yr.	Inspector

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C 1037 B	.1715	Kw.hrs./min.	Electric Power
ET 1012 D	.069	Cu.ft/min.	1.5% silane/argon
D 1174 D	0.03	Cell/min.	Rejected cell

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
SDC	0.996	Cell / Cell	Solder dipped cell
		/	
		/	

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FORMAT A

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PROCESS DESCRIPTION

Note: Names given in brackets [ ] are the names of process attributes requested by the SAMICS III computer program.

A1 Process [Referent] CELTEST

A2 [Descriptive Name] Cell Electric Performance Test and Grouping Process

PART 1 – PRODUCT DESCRIPTION

A3 [Product Referent] TESTC

A4 Descriptive Name [Product Name] Tested and Grouped Cell

A5 Unit Of Measure [Product Units] Cell

PART 2 – PROCESS CHARACTERISTICS

A6	[Output Rate] (Not Thruput)	59.64	Units (given on line A5) Per Operating Minute
A7	Average Time at Station [Processing Time]	0.33	Calendar Minutes (Used only to compute in-process inventory)
A8	Machine "Up" Time Fraction [Usage Fraction]	0.875	Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS [Machine Description]

A9	Component [Referent]	CTG		
A9a	Component [Descriptive Name] (Optional)	Cell tester and grouping machine		
A10	Base Year For Equipment Prices [Price Year]	1978		
A11	Purchase Price ($ Per Component) [Purchase Cost]	47,500		
A12	Anticipated Useful Life (Years) [Useful Life]	7		
A13	[Salvage Value] ($ Per Component)	5,000		
A14	[Removal and Installation Cost] ($/Component)	2,000		

Note: The SAMICS III computer program also prompts for the [payment float interval] the [inflation rate table], the [equipment tax depreciation method] and the [equipment book depreciation method]. In the LSA SAMICS context, use 0.0, (1975, 4.0), DDB, and SL.

Format A: Process Description (Continued)

A15 Process Referent (From Page 1 Line A1) CELTEST

PART 4 – DIRECT REQUIREMENTS PER MACHINE (Facilities) OR PER MACHINE PER SHIFT (Personnel)
[Facilities and Personnel Requirements]

A16 Catalog Number [Expense Item Referent]	A18 Amount Required Per Machine (Per Shift) [Amount per Machine]	A19 Units	A17 Requirement Description
A 2064 D	70	Sq.ft.	Factory Space (Type A)
B 3768 D	0.25	Prsn.yr.	Tester
B 3720 D	0.05	Prsn.yr.	Inspector
B 3736 D	0.03	Prsn.yr.	Maintenance Mech. II.
B 3688 D	0.02	Prsn.yr.	Electronic Maintenance
B 3256 B	0.01	Prsn.yr.	Production Planner

PART 5 – DIRECT REQUIREMENTS PER MACHINE PER MINUTE
[Byproduct Outputs] and [Utilities and Commodities Requirements]

A20 Catalog Number [Expense Item Referent]	A22 Amount Required Per Machine Per Minute [Amount per Cycle]	A23 Units	A21 Requirement Description
C 1032 B	0.1375	Kw.hr./min.	Electricity
D 1174 D	0.36	Cell/min.	Rejected Cell

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED [Required Products]

A24 [Product Reference]	A26 Usable Output Per Unit of Input Product	A27 Units	A25 Product Name
ARCC	0.994	Cell / Cell	A.R.Coated Cell
		/	
		/	

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REVERSE SIDE JPL 3037-S R 7/78

APPENDIX III

TEMPORARY CATALOG FOR EXPENSE ITEMS

LIST OF TEMPORARY CATALOG ITEMS

NUMBER	ITEM DESCRIPTION	UNIT	PRICE	IC	YEAR
ET 1001D	Trichloroethylene	Liter	2.03	C	77
ET 1002D	Methanol	Liter	1.13	C	77
ET 1003D	Phosphosilica dopant	Liter/min	17.545	C	86
ET 1004D	Borosilica dopant	Liter/min	17.545	C	86
ET 1005D	Resist ink	Gal/min	32.00	C	77
ET 1006D	Thinner	Gal/min	40.00	C	77
ET 1007D	Gold solution	Liter	13.40	C	78
ET 1008D	Nickel solution	Liter	1.210	C	78
ET 1009D	Strip solution	Liter/min	1.178	C	77
ET 1010D	Solder flux	Gal/min	16.50	C	77
ET 1011D	60/40 solder	Lbs/min	6.04	D	77
ET 1012D	1.5% silane/argon	cu.ft/min	.648	C	86