TIROS-N COSMIC RAY STUDY FINAL REPORT

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16. Abstract

An experimental and analytical study was performed on the impact of galactic cosmic rays on the TIROS-N satellite memory in orbit. Comparisons were made of systems equipped with the Harris HM1-6508 1 × 1024 bit CMOS/bulk RAM and the RCA CDP-1821 1 × 1024 bit CMOS/SOS RAM.

Based upon the experimental results at the Cyclotron-88 facility at Lawrence Berkeley Laboratory, the TIROS-N environment provided by GSFC, and the CRIER code, estimated bit error rates were determined. These were at least 8.0 bit errors/day for a 300 kilobit memory with the HM1-6508 and 1.4×10^{-2} bit errors/day with the CDF-1821.

It was also estimated that the HM1-6508 latchup rate in orbit is at least two orders of magnitude less than the bit error rates; the CDP-1821 will not latchup.

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PREFACE

OBJECTIVE

The objective of this study was to provide the TIROS project data, conclusions, and recommendations on the susceptibility in orbit of the Harris HM1-6508 and RCA CDP-1821 memory devices to galactic cosmic rays.

SCOPE OF WORK

Conduct heavy ion experiments at the Cyclotron-88 facility, Lawrence Berkeley Laboratory to determine bit error thresholds and latchup susceptibility.

Using the galactic cosmic ray environment provided by GSFC, determine the bit error rates and latchup susceptibilities of TIROS-N systems equipped with the HM1-6508 and with the CDP-1821.

Provide a test plan, two test reports, a final briefing, and a final report.

CONCLUSIONS

The data provided or obtained provided an adequate basis for comparison of the HM1-6508 and CDP-1821.

The TIROS system bit error rates are at least 8.0 bit errors/day for the HM1-6508 and 1.4×10^{-2} bit errors/day for the CDP-1821.

The latchup rate for the HM1-6508 is estimated to be at least two orders of magnitude less than its bit error rate, while the CDP-1821 will not latch up.

Total dose effects on the galactic cosmic ray-induced bit error rate were not addressed in this study.

SUMMARY OF RECOMMENDATIONS

The RCA CDP-1821, or its equivalent, should be used in lieu of the Harris HM1-6508 in the TIROS-N.

Experimental studies should be performed to determine the dependence of the cosmic-ray-induced bit error rate on total ionizing dose.

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I. INTRODUCTION

This is the final report of the Cosmic Ray Study performed by the Autonetics Strategic Systems Division of Rockwell International, Anaheim, California, under Contract NAS5-26180 for Goddard Space Flight Center, Greenbelt, Maryland, during the period April to September 1980.

Section II describes the galactic cosmic ray tests, simulated with high energy krypton and argon ions at the Cyclotron-88 facility at Lawrence Berkeley Laboratory. Section III discusses the test results and analysis. The galactic cosmic ray environment and the development of the TIROS-N model linear charge deposition spectrum are summarized in Section IV.

Section V provides the analysis of the effect of the space environment on the two device types under study, the Harris HM1-6508 and the RCA CDP-1821, as well as the impact on the TIROS-N systems equipped with these parts. The final two sections contain the Conclusions and Recommendations resulting from the study.

This study claims no new technology within the scope of the contract definition.

II. SIMULATED GALACTIC COSMIC RAY TESTS

A. TEST OBJECTIVE

The objective of the tests conducted at the Cyclotron-88 facility of the Lawrence Berkeley Laboratory, University of California at Berkeley was to determine the bit upset energy thresholds of the Harris HM1-6508 CMOS/bulk RAM (one date code) and the RCA CDP-1821 CMOS/SOS RAM (three date codes) parts provided and to determine if latchup is encountered.

B. TEST APPROACH

The test approach was to write a known pattern into the memory of a delidded device in a vacuum chamber and then continuously monitor the memory for bit errors and latchup while being exposed to a beam of known angle of incidence, ion type, and energy at the Cyclotron-88 facility.

C. IDENTIFICATION OF PARTS TESTED

A total of 21 parts were exposed to either krypton ion beams during the June 9 through 10, 1980, test period or argon ion beams on June 13, 1980 or both, at the Cyclotron-88 facility. The 14 Harris HM1-6508 CMOS/bulk RAM parts tested all had a 7810 date code. Of these, six were exposed to both the krypton and argon ions, two to krypton ions only, and six to argon ions only.

The seven RCA CDP-1821 CMOS/SOS RAM parts tested were exposed to krypton ion beams only; they were from three different date codes. Four of these parts, date code 8008, were of the latest design and met all electrical parameter requirements except for read access time > 260 ns. Two of the parts tested, date code 7812, met all TIROS screening requirements. The seventh CDP-1821 tested, date code 7809, passed all screening requirements except for the +125 °C electrical tests; a second part with this date code was not functioning after installation in the vacuum chamber and, therefore, was not exposed.

D. RADIATION FACILITY

The simulated galactic cosmic ray tests were performed at the Cyclotron-88 facility of the Lawrence Berkeley Laboratory (LBL). The exposure chamber was set up on the Bio-Medical Optical Bench located in Cave 3. (See Figure II-1.) The RAM evaluation equipment was located in Cave 4 for the remote monitor and control of test device functions. Twenty-one 40-foot coaxial cables were installed between the two caves through a conduit of approximately 15 cm diameter near the top of the shielding wall to interconnect the instrumentation.

E. TEST EQUIPMENT

Both the use of an evacuated exposure chamber and active monitoring of the particle flux were required for the tests. Aerospace Corporation provided this equipment and the personnel to operate it. Real time flux monitoring was required to account for beam flux variations. The flux was monitored by a thin (transmission) scintillator foil and photomultiplier tube as provided by Aerospace Corporation. This device takes a minimum of 5 to 6 cm between the beam port and the part. The distance leads to an unacceptable beam degradation in air, particularly for krypton; therefore, the vacuum chamber is required.

The vacuum exposure chamber consisted of a cylinder approximately 40 cm in diameter by 40 cm tall mated to the beam drift tube and evacuated. (See Figure II-2.) The lid of the cylinder was removable and contained two 37-pin Deutsch vacuum feed-throughs, one side male and the other female. The lid also held a positioning rod on which a card was mounted for holding four devices inside the vacuum chamber and positioning them with respect to the ion beams. The devices were inserted in sockets on the cards on the axis of rotation and positioned with respect to the ion beam by raising and lowering the rod and turning angles to the beam.

The flux monitoring equipment had a thin organic scintillator foil which transmitted a krypton beam with a loss of about 17 MeV. The foil was mounted in a lucite light pipe optically coupled to a photomultiplier tube. When a heavy ion particle penetrated, the foil scintillated and the light pulse

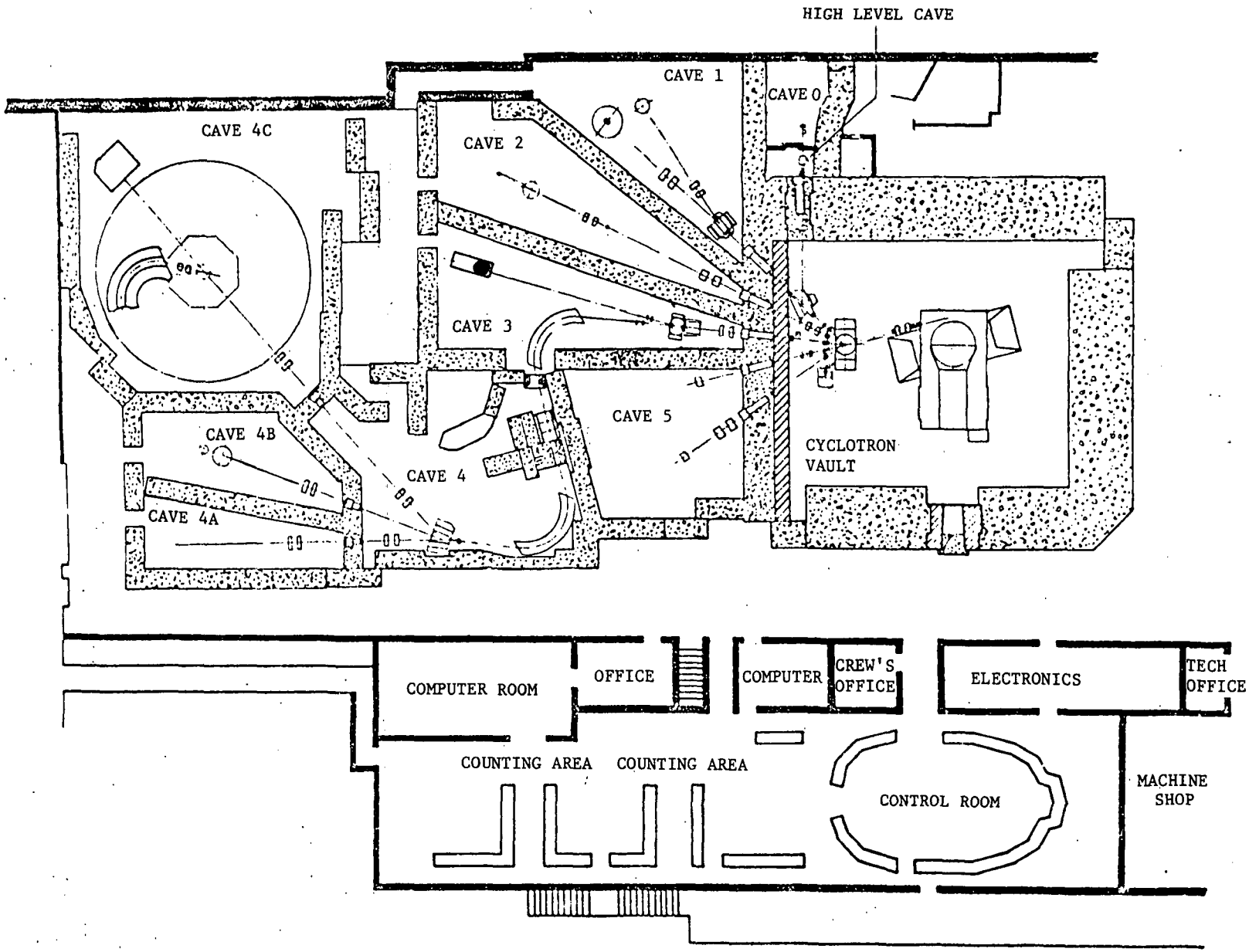


Figure II-1. Cyclotron-88 Facility

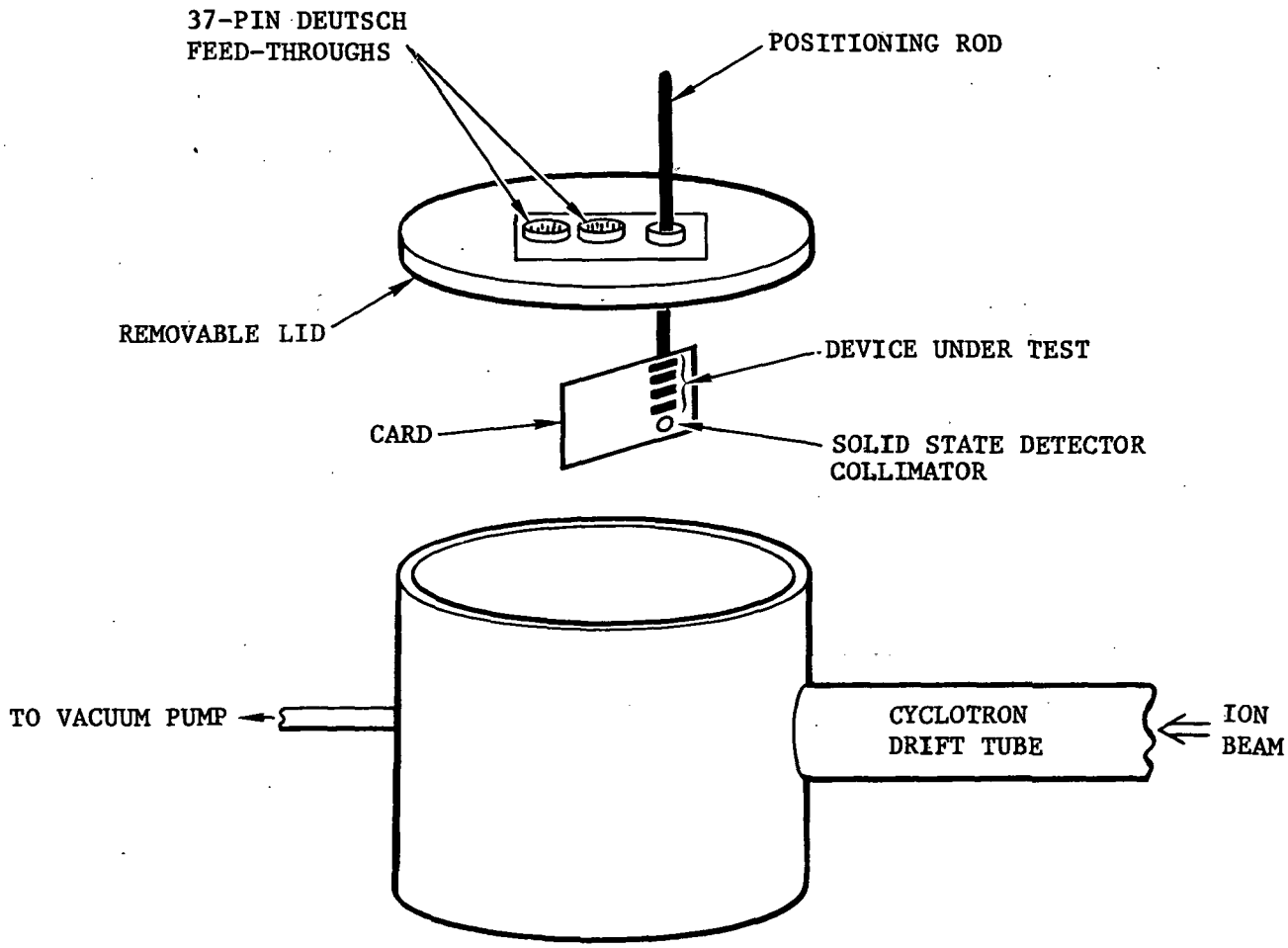


Figure II-2. Vacuum Exposure Chamber (Schematic)

signal was amplified by the photomultiplier and counted by a counter. The scintillator foil was positioned between the beam and the part being irradiated. The hole through the light pipe to the scintillator foil was 2 cm in diameter; however, a collimator is placed in the scintillator to confine the beam to the device under test and to provide a well-defined area for the flux measurement. In addition, a silicon detector was located on the beam-line behind the device card. This detector completely absorbed the ion particles and allows an energy measurement by use of a pulse height analyzer. A collimator for this detector was located at the bottom position of each card on the positioning rod center line.

The beam through the scintillator was collimated to 1.511 cm diameter (1.794 cm^2 area). Being larger than any of the LSI chips, minor malalignments could be tolerated without affecting the experimental results. To ensure accurate flux measurements at each device as well as to assist the Cyclotron-88 control operators in establishing the beam, the silicon detector collimator located on each device board was collimated to 0.356 cm diameter (0.0993 cm^2 area). When the appropriate particle flux energy and intensity was reached and the beam ion density uniform over the area of the collimators as indicated by a scintillator/detector count ratio approached 18 to 1, the beam was considered ready for the tests to proceed.

The electrical test equipment for evaluating the various devices was interfaced to the devices under test through either one or both of two 37-pin feed-throughs on the lid of the vacuum chamber. (See Figure II-2.) The connections from the feed-throughs to the device card and to the "Personality Board" for the Macrodata MD-104 Automatic Memory Tester junction box, adjacent to the vacuum chamber, were made through 24-lead ribbon cables with appropriate connectors.

The MD-104 was commanded to write a selected pattern into the memory of the part being exposed and store the information internally. The tester was then commanded to continuously cycle through the read-only mode at millisecond intervals during irradiation. The read is performed sequentially

through each bit. In the error detection mode, only errors are indicated on an oscilloscope through use of the Macrodata MD 11 CRT display interface. The "SHIPAT" 32 × 32-bit shift pattern shown in Figure II-3, or its complement, was used during all testing due to the uncertainties associated with specific device architecture.

Supply current was limited to preclude device burn-out in case of latchup; it was remotely monitored and controlled through the cabling between caves. The device power supply voltages and currents were checked with an oscilloscope during irradiation; supply line noise pickup was insignificant. The device bit pattern and supply current were both monitored for indications of latchup. Latchup was simultaneously evidenced by an all-error bit pattern and an increase in supply current which was limited by a 100 ohm resistor.

F. TEST ENVIRONMENT

The galactic cosmic ray environment consists of very high energy ions in significant quantities up through Z = 26 (iron). Each ion is characterized by a stopping power which is a function of the particle energy; this is shown in Figure II-4 for iron, argon, krypton, and xenon. The iron particle stopping power is the worst significant case for the natural environment. The argon ion curve shows a stopping power somewhat less than that of iron; thus, iron particles are even more likely to cause bit errors and/or latchup. The ultimate goal of the parts tests and subsequent analysis is to determine which, if any, ion particles in the natural environment could cause bit errors or latchup in the Device Under Test (DUT); this leads to a requirement for simulation particles with a higher stopping power than iron to provide a conservative simulation. That is, the particles from the space environment may be considered incident on the device from all directions with equal probability. There is a finite probability that iron particles of the worst-case energy will travel through a sensitive region along the maximum possible path length (eg, the diagonal across a parallelepiped) through the sensitive region These particles will deposit the maximum energy (neglecting nuclear collisions). Scattering of the heavy ion particles from the Cyclotron along the

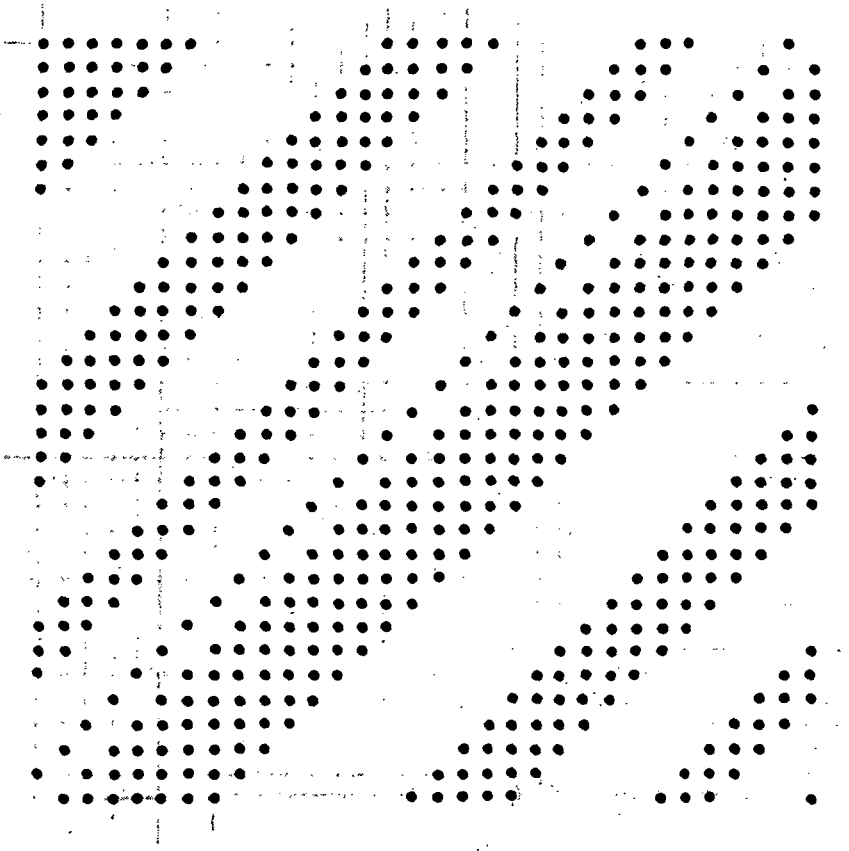


Figure II-3. "SHIPAT" 32 x 32-Bit Shift Pattern Display

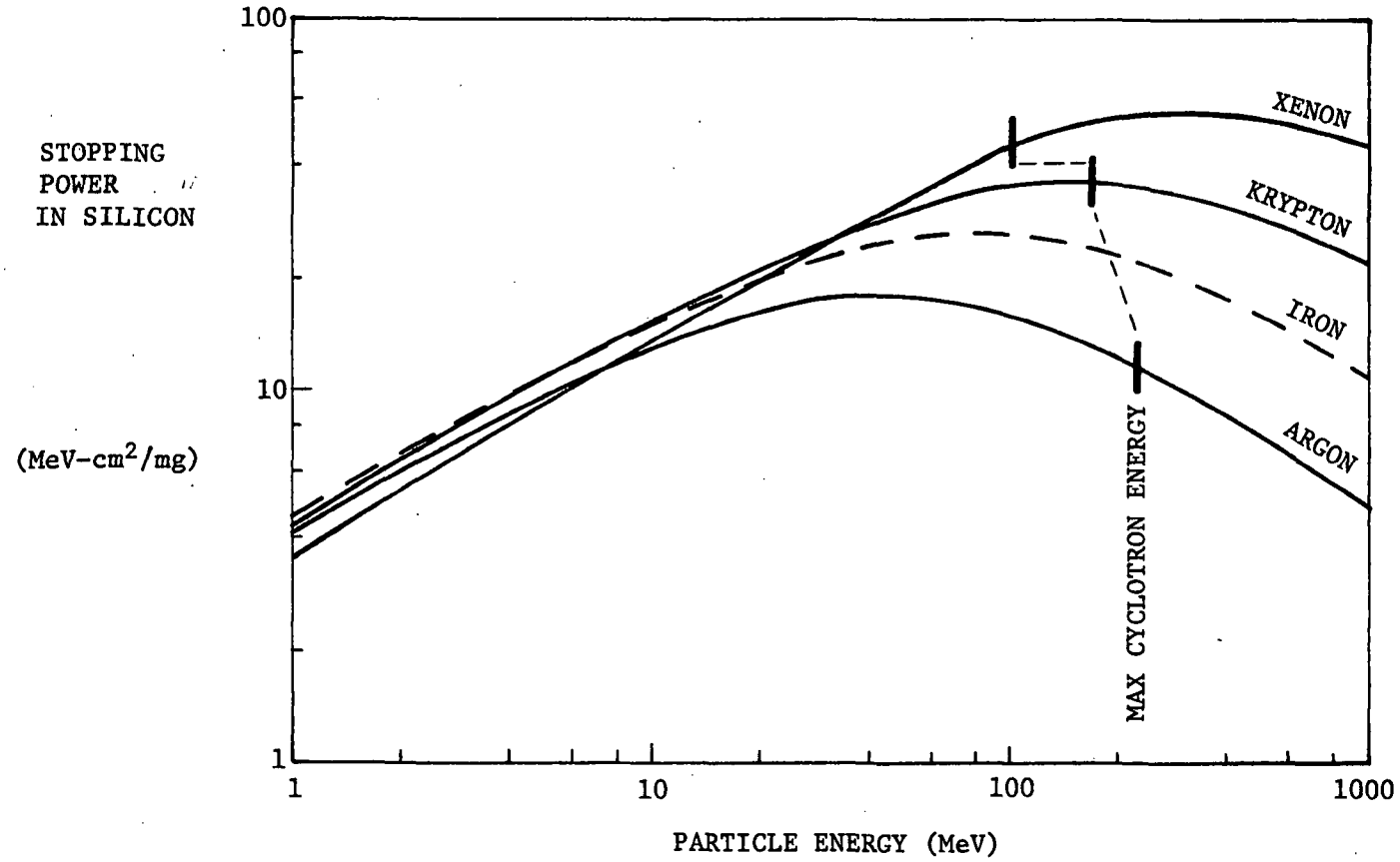


Figure II-4. Heavy Ion Stopping Power vs Energy

maximum path length through the sensitive region presents a formidable experimental problem because the device packaging limits the attainable angle of beam incidence. To at least partially compensate for this limitation, the simulation requires testing with particles which have a higher stopping power than iron.

Generally, gases are preferred as ion sources at the Cyclotron because these are normally used; the advantage to the experimenter is minimum time delays. Either krypton or xenon are potential heavier-than-iron-ion candidates; radon is radioactive and therefore not acceptable. From Figure II-4, xenon is potentially about 40 percent better than krypton in stopping power at the maximum available Cyclotron-88 output energies; however, krypton is an optimum choice for several reasons. First, only argon and krypton ion beams have been used during previous memory testing and Cyclotron-88 operators have gained some familiarity with them; xenon has never been tried. Second, the heavier the particle, the more uncertainty is the effects of recombination; that is, there may be a saturation in the density of the electron-hole pairs which would lead to uncertainties in the analysis. Finally, any degradation in beam energy lessens the advantage of xenon; this can be seen in Figure II-4.

G. TEST PROCEDURES

For each test session the test equipment was installed, checked out, and calibrated, as required. The selected ion beam was then established, and the desired ion type, energy, and count rate were verified with the monitoring equipment and personnel provided by Aerospace Corporation.

Each set of four devices was installed on the device card in the vacuum chamber and then checked for satisfactory operation at the desired supply voltage while the chamber was being evacuated. The "SHIPAT" bit pattern or complement was then written into the memories of the parts and verified in the MD-104 READ mode.

The subsequent test procedures were generally to irradiate one part at a time with selected beam parameters while monitoring for bit errors and latchup symptoms, then terminating the beam at an appropriate time. This

latter was generally after latchup, after a number of bit errors has occurred or after a large ion fluence with no errors. The data were then recorded and the next run undertaken, with adjustment in beam parameters or part change, as required.

The specific test procedures were quite flexible and are described with the test results. With the approval of the GSFC Technical Monitor, who was present for the tests, these changes were made to adjust to the results obtained and expected beam time remaining. The consideration was also present that any data obtained was all that would be available due to potential Cyclotron equipment failure prior to the three-week shutdown scheduled to start at 8:00 AM, June 13, 1980.

III. TEST RESULTS AND DATA ANALYSIS

The first cosmic ray simulation test session was conducted at the Cyclotron-88 facility in accordance with the approved test plan (with changes as approved by the GSFC Technical Monitor) on 9 and 10 June 1980. An $^{84}Kr^{+10}$ (an 84 nucleon isotope of krypton at charge state +10, ie, having lost 10 orbital electrons) ion beam with an E_o = 170 MeV was used exclusively. After an energy loss of 18 meV due to the scintillator, the measured beam energy at the chip, $E_{chip} \approx 152$ meV, as measured by a silicon solid-state detector except when a 15 μm to 30 μm equivalent thickness aluminum beam degrader was used to decrease E_{chip} to the 20 to 40 meV range. For each equivalent degrader thickness the solid state detector was used to measure the particle energy distribution; although some energy spread was noted, there was an acceptably sharp peak in each case. A total of eight Harris HM1-6508 (one lot) and seven RCA CDP-1821 (three lots) 1 k-bit RAMs were irradiated in the vacuum chamber. The raw data sheets are presented in Appendix A.

All five of the HM1-6508s exposed to 152 MeV Kr ions latched rapidly at fluences measuring between 227 and 11,781 p/cm^2 (particles/cm^2). Latch measurements were repeated 10 times with HM1-6508 Serial No. 188; the average fluence to latch was 1978 p/cm^2 with a range from 672 to 4138 p/cm^2. None of the HM1-6508s exposed to the 20 to 40 MeV degraded Kr beam at either a 0° or 60° beam angle to fluences up to 2×10^6 p/cm^2 showed a tendency to latch.

A total of 30 exposures with 4 parts using the krypton ion beam degraded to the 20 to 40 MeV range provided data on the HM1-6508 error rate. TableIII-1 summarizes the results.

Two things are readily apparent from Table III-1. First, there is almost a two order-of-magnitude variation in the error susceptibility of these four parts; and second, the E_{chip} (Kr) bit upset energy threshold is between 20 and 32 MeV at a 60° beam angle.

Table III-1 summarizes the results.

Part No.	Average Error Rate (E/p-cm^{-2})		
	0° Beam Angle 40 MeV E_{chip}	60° Beam Angle 32 MeV E_{chip}	0° & 60° Beam Angle 20 MeV E_{chip}
166	1.5×10^{-4}	2.0×10^{-5}	0
167	3.9×10^{-4}	3.5×10^{-5}	0
168	1.2×10^{-3}	1.2×10^{-4}	0
169	8.0×10^{-5}	2.4×10^{-6}	0

Parts from three different lots of the RCA CDP-1821 RAMs were available for test; they were date coded 7809 (+125°C rejects), 7812, and 8008 (latest design, rejected for access time > 260 ns). Four of the latest design parts were exposed at beam angles of 75° (one was also exposed at 60°) at total corrected fluences from 1.4×10^5 to 7.2×10^5 p/cm^2; no bit errors were observed at the V_{DD} = +5 V level. The four parts were also exposed under the same conditions at V_{DD} = +2 V; three of the parts had no bit errors, and one had three bit errors during exposure. This latter part had an observed bit error rate of about 1×10^{-5} error/p-cm^{-2} at +2 V. Two of the parts were also exposed at the V_{DD} = +3.5 V level, also with no observed bit errors.

The other set of RCA CDP-1821 RAMs installed in the vacuum chamber consisted of two each of date codes 7809 and 7812. One from date code 7809 was not functional after the chamber was evacuated. The three remaining parts were exposed to corrected fluences from 2.2×10^5 to 6.2×10^5 p/cm^2 at a 75° beam angle and V_{DD} = +5 V. The date code 7809 part had a bit error at about 2.2×10^5 p/cm^2 but no additional errors after continuing the exposure to 6.2×10^5 p/cm^2 then rewriting and exposing to 5.6×10^5 p/cm^2. (Note: The one bit error observed was possibly caused by an operation of the Cyclotron at that time causing a noise spike.) The date code 7812 parts had no bit errors at the V_{DD} = +5 V level. One date code 7812 part was also tested at V_{DD} = +10 V (no errors) and V_{DD} = +2 V (two errors, for an error rate of about 7×10^{-6} errors/p-cm^{-2}).

The second cosmic ray simulation test session was conducted at the Cyclotron-88 facility in accordance with the approved test plan as changed with the approval of the GSFC Technical Monitor on 13 June 1980. $A^{40}Ar^{+8}$ ion

beam with an E_o = 224 MeV was used exclusively. E_{chip} = 210 to 212 MeV (as measured by a silicon solid-state detector) except when a 41 μm to 53 μm equivalent thickness aluminum beam degrader decreased E_{chip} to the 7 to 67 MeV range. The raw data sheets are given in Appendix A.

Twelve of the single lot of Harris HM1-6508 1 k-bit RAMs were irradiated in the vacuum chamber in sets of four at V_{DD} = 5 ± 0.5 V. Eight of these parts were exposed at E_{chip} = 210 to 212 MeV; four latched at a 0° beam angle (normal incidence) and three others did not. One part was exposed at 45° only and latched. Of the three parts that did not latch at 0°, one was exposed at 45° and 60°, one at 45° and one at 60° (two times); all latched readily. None of the parts latched at any beam angle from 0° to 65° in the E_{chip} = 7-67 MeV range.

Unfortunately, the stopping power of the E_{chip} = 210 to 212 MeV energy particles proved to be too high to permit determination of the bit error energy threshold. The only method of further decreasing the stopping power in the time available was to decrease the argon particle energy to the other side of the maximum stopping power (at about 50 MeV). This was accomplished by placing the previously installed 41 μm Al degrader in the beam and turning to an angle and measuring the beam energy with the solid-state detector. This was a slow and tedious process, particularly since the degrader angles could only be measured approximately.

A total of 10 HM1-6508 RAMs were exposed at E_{chip} = 41 MeV and 0° beam angle; all but one exhibited errors at rates ranging from 2.3×10^{-5} to 1.2×10^{-2} errors/p-cm^{-2}. The one part having no errors was then exposed at a 60° beam angle and errors at a rate of 3.3×10^{-4} errors/p-cm^{-2} were observed. The beam energy was increased from 41 to 45 MeV for another part (0° beam angle) and the error rate increased by over a factor of three. These latter two measurements indicate, respectively, (1) that the apparent bit error threshold is caused by changes in energy deposition rather than glassivation/passivation layer shielding and (2) that since the error rate is quite sensitive to particle energy, the particle energy is near the bit error threshold for E_{chip} = 40 MeV.

A high priority was given to obtaining the argon beam data for the Harris HM1-6508 by the TIROS Project Office. Therefore, in view of the low probability of obtaining the krypton beam in time to gain meaningful additional data on the CDP-1821, it was agreed to continue with the argon and HM1-6508. Between the two test periods several additional CDP-1821 package edges were ground off so that the beam angle could be increased to at least 80°. Based upon the results of limited previous tests not associated with this contract, it is believed that some or all of the CDP-1821 RAMs would exhibit bit errors at this increased beam angle. Also, a change was made in the relative location of the scintillator and device board in the vacuum chamber to remove the 75° limitation encountered during the first test session. Even though it is believed that the RCA CDP-1821 is at least two orders-of-magnitude less bit-error-prone (and not susceptible to latchup) than the Harris HM1-6508, further experimental confirmation may be desirable.

Figures III-1 through III-3 summarize the various test conditions used during the two Cyclotron-88 sessions, which were required to determine the energy threshold for bit-error and latchup. The ion energy at the surface of the chip passivation layer is shown on the vertical axis for various samples shown on the horizontal axis. Krypton ions are indicated by the heavy lines while argon ions are indicated by the thinner lines. The various angles of incidence are indicated. The specific test condition for each sample (ion type, ion energy, and angle of incidence) are indicated by an "X" or a "O" on the appropriate line corresponding to the ion energy used. The result of bit-error (or latchup) for a particular test point is indicated by an "X" while the result of no bit-error (or latchup) is indicated by an "O".

A. HM1-6508 TEST RESULTS ANALYSIS

1. Bit Error Data

From Figure III-1, we note that the HM1-6508 devices exhibit bit errors for most of the test conditions. The lack of bit-errors in devices 166, 167, and 168 for Kr at 20 MeV and in device 186 for Ar at 7 MeV is caused by the total stopping of the ion in the passivation layer above the sensitive regions. Thus, only two distinct determinations of a bit-error

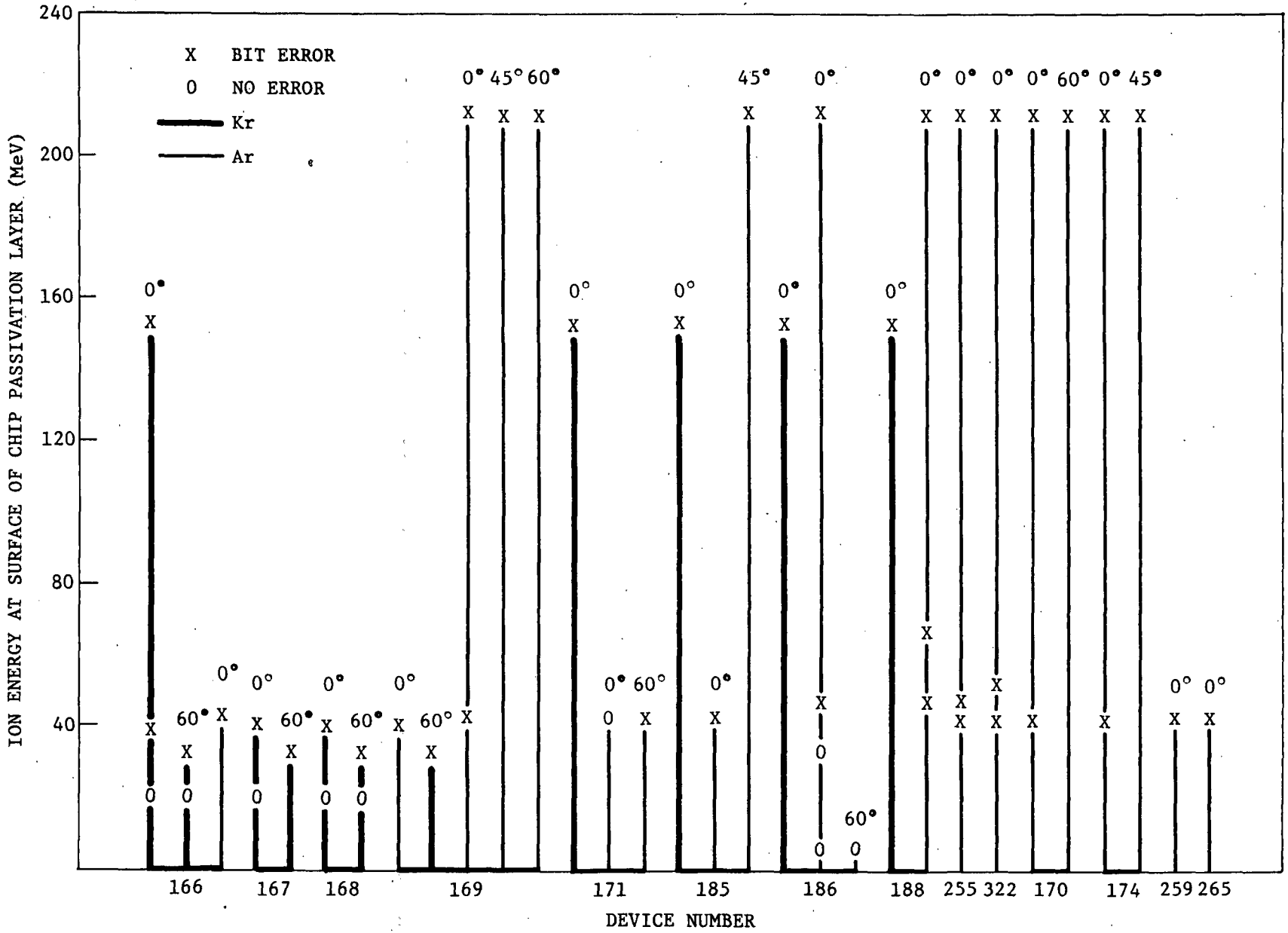


Figure III-1. HM1-6508 Raw Data for Bit-Error Energy Threshold

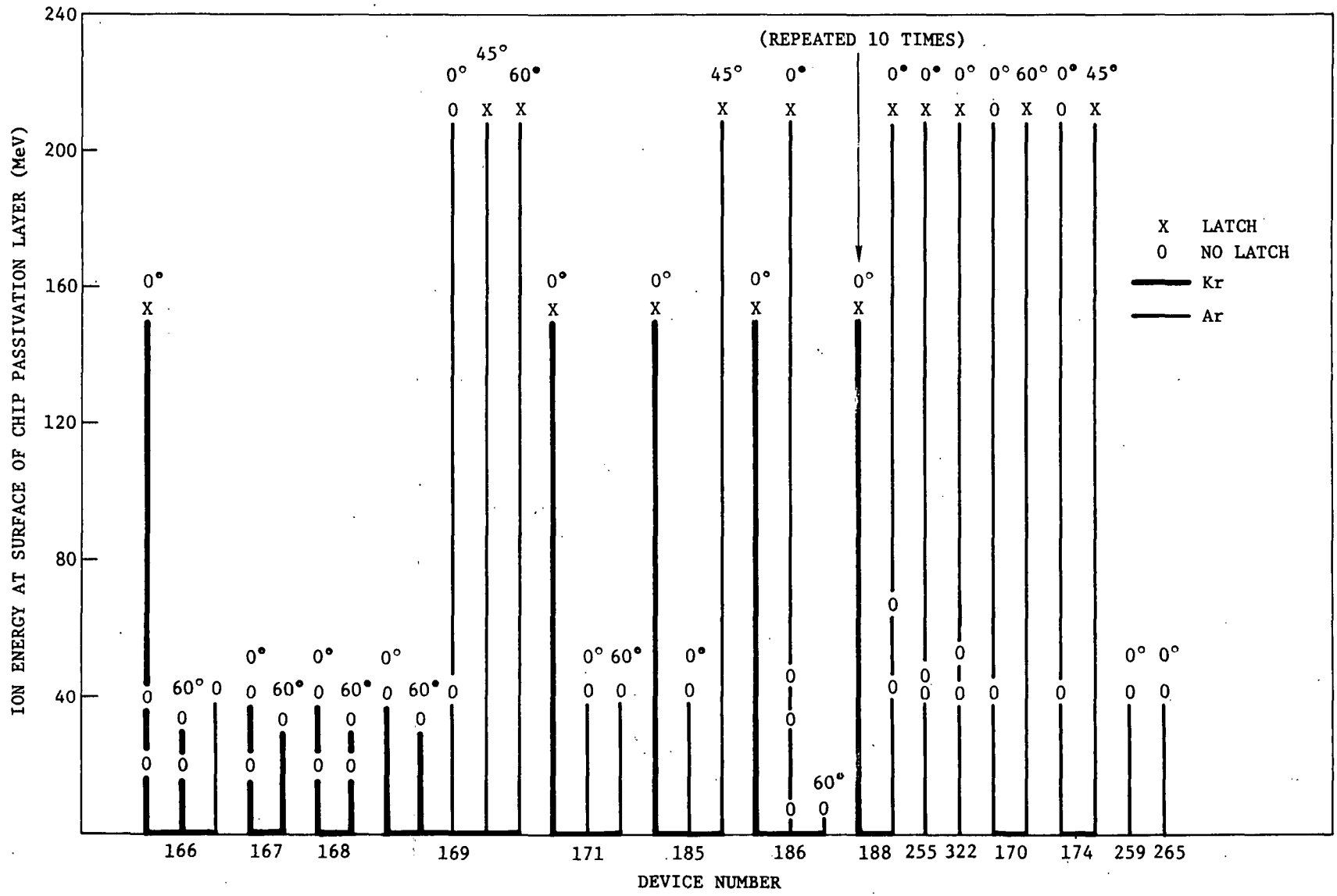


Figure III-2. HM1-6508 Raw Data for Latchup Energy Threshold

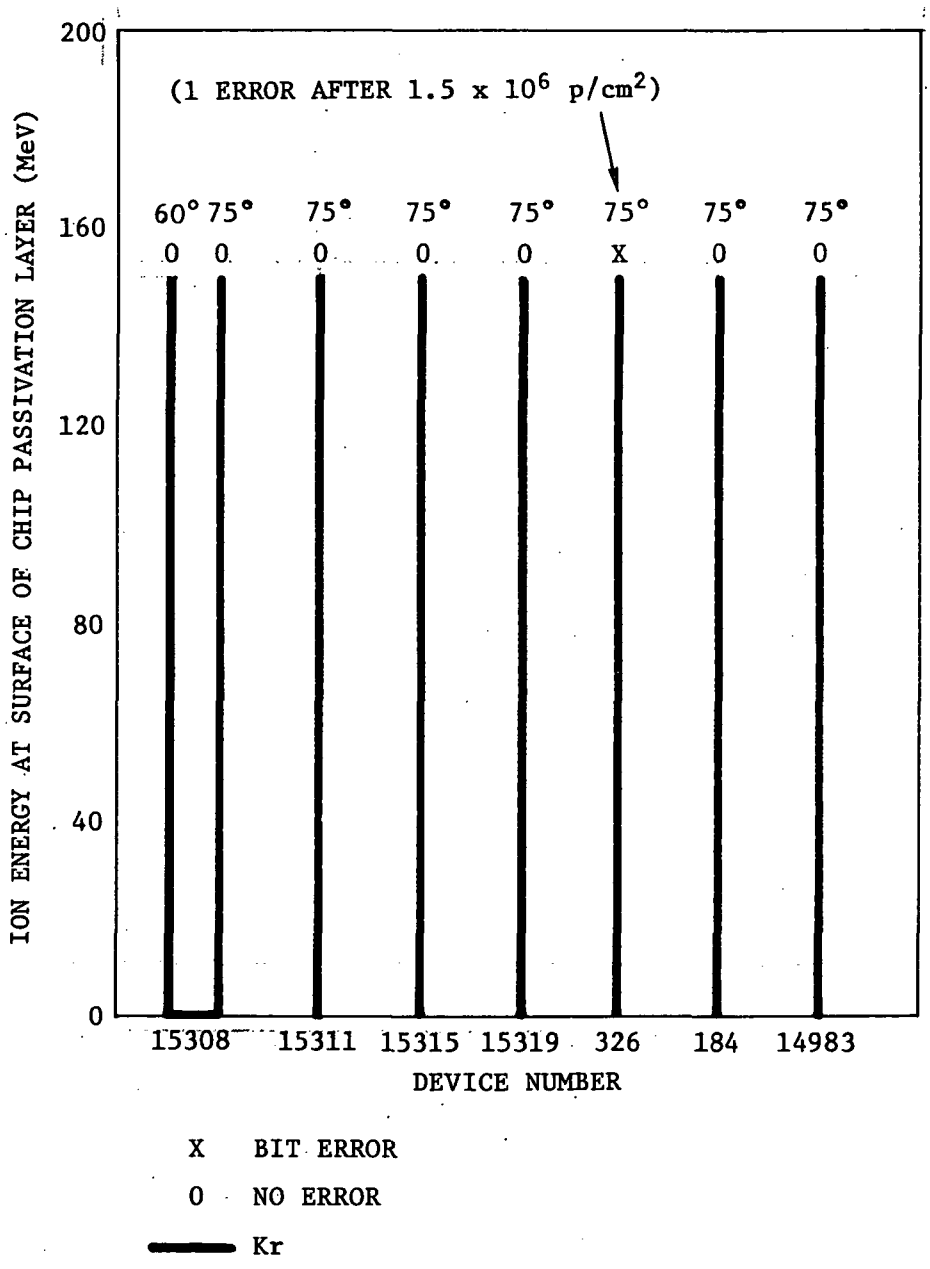


Figure III-3. CDP-1821 Raw Data for Bit-Error Energy Threshold

threshold could be obtained from the data: device 171 with 41 MeV argon at 0° showed no errors but did exhibit errors at 60°; device 186 with 34 MeV argon at 0° showed no errors but did exhibit errors at 45 MeV.

To determine the critical charge (see Appendix B) to cause bit error, it is necessary to establish the energy deposition threshold in the sensitive region of the device. This can be determined from knowledge of the path length of the ions through the sensitive region and the energy (and consequently, stopping power, dE/dx) at the sensitive region for a test condition near the threshold for bit-error or latchup. For bit-error, the path length through the sensitive regions for ions at normal incidence was determined to be 0.78 and 2.1 μm (see Section V.A.1).

To determine the stopping power of the ions at the sensitive region, we must consider the energy loss of the ions in the material covering the sensitive region. Figure III-4 shows the stopping power in units of MeV/μm vs ion energy for krypton and argon ions at the lower energies used in the Cyclotron-88 experiments. At the higher energies used in the experiments, 152 MeV krypton and 210 MeV argon, the energy loss in the covering material is negligible, as can be seen from Figure II-4. Also shown in Figure III-4 is the change in stopping power after passing through a given thickness of material (silicon equivalent), starting at 30 MeV for krypton and at 40 MeV for argon. For example, a 30 MeV krypton ion has a stopping power of 5.8 MeV/μm, but after passing through 4 μm of silicon, the ion has a stopping power of 3.6 MeV/μm. The range vs energy for the two ion types is also shown.

The bit-error threshold for the HM1-6508 was determined with ions at the lower energies; therefore, a careful consideration of the covering material (shielding) on the chip was required. The material shielding the bit-error sensitve regions of the HM1-6508 was determined to be a nominal 5.5 μm (silicon equivalent) as is discussed in Section V.A.1.

To arrive at an estimated critical charge (Q_c) for bit error in the HM1-6508, it is necessary to weigh the uncertainties involved in the experimental data and analytical assumptions. The thickest sensitive region is

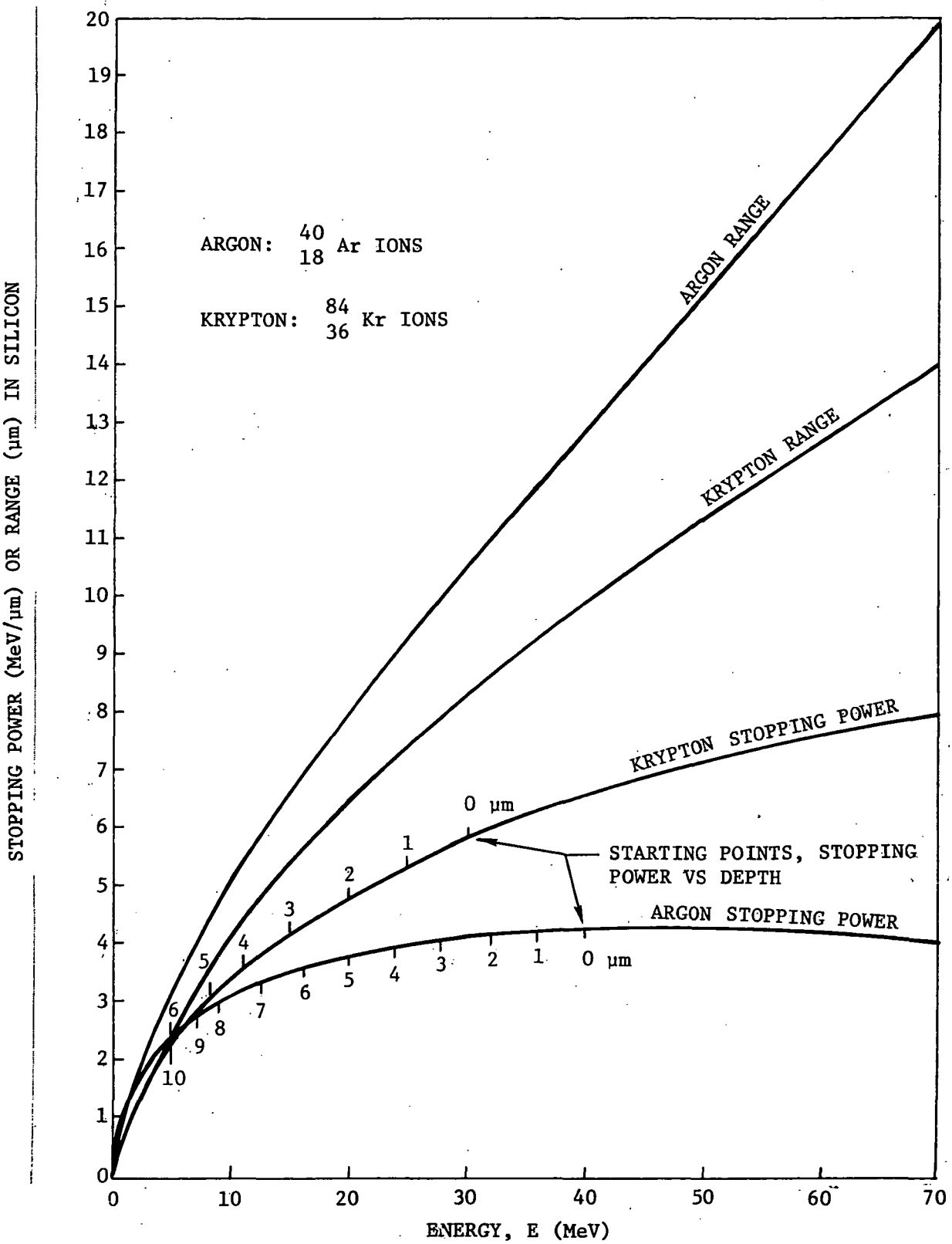


Figure III-4. Range and Stopping Power vs Energy, Argon and Krypton in Silicon

indicated to be 2.1 μm of silicon covered with a 5.5 μm silicon equivalent shield. Considering the 210 MeV argon ion experimental results, where there were many bit upsets at normal incidence, energy deposition calculations lead one to the conclusion that $Q_c \leq 0.28$ pC. Uncertainties in the shield thickness are not significant in this case because the argon ion stopping power changes relatively slowly within the region of interest.

Analysis of the low energy krypton and argon experimental data yields apparently inconsistent results. The argon ion incident energy threshold is estimated to be about 40 MeV at normal beam incidence. Using the 2.1 μm thickness and the argon stopping power data in Figure III-4, it is estimated that $Q_c \leq 0.32$ pC; this supports the high energy argon results of $Q_c \leq 0.28$ pC. However, since 32 MeV krypton ions at a 60° angle of incidence also caused bit upsets, the covering material thickness would be indicated to be less than 5.5 μm. This follows from the fact that a 60° angle of incidence would result in a 11 μm path length, well beyond the range of the 32 MeV krypton ions as shown in Figure III-4.

One possible explanation is that the covering material thickness may be considerably less than 5.5 μm in some areas covering a sensitive region; this is conceivable considering the multilayer fabrication sequence for the device (see Section V.A.1). Another explanation could be that of scattering of the ions from their incident path to a shorter path length through the covering material to the sensitive region. Keeping in mind the objectives of the program, the available resources were not expended in trying to resolve these issues as they do not impact the final conclusions. Based on consideration of all available data, a reasonable upper limit for the critical charge in the HM1-6508 is estimated to be 0.3 pC.

2. Latchup Data

From Figure III-2, we notice that latchup was observed in all 10 samples that were tested with 152 MeV Kr ions or 210 MeV Ar ions. For 32 and 20 MeV Kr ions, and 57 to 7 MeV Ar ions, no latchup was observed. These data indicate that the sensitive region for latchup is considerably deeper into

the Si chip than that for bit-error. The devices latch readily with 210 MeV Ar, which has a dE/dx of 2.8 MeV/μm and should not change significantly, even after passing through several microns of material. However, for 40 MeV Ar, which has a dE/dx of 4.2 MeV/μm, or 32 MeV Kr, which has a dE/dx of 6 MeV/μm, the devices did not latch. Consequently, the stopping power of the lower energy ion must be degraded considerably by the time they reach the sensitive region for latchup. To be degraded to a dE/dx equivalent to the 210 MeV Ar (2.8 MeV/μm), the 32 MeV Kr must pass through approximately 5.5 μm and the 40 MeV Ar must pass through approximately 8.5 μm (see Figure III-4). Thus it is likely, based on the data, that the sensitive region for latchup involves the junction between the P-well and the substrate (see Section V.A.2). This junction is typically several microns below the silicon surface.

Assuming that the sensitive junction for latchup is the P-well to substrate junction, the minimum energy deposition to induce latchup can be estimated, based on the data. The depletion width of the junction, using doping densities obtained from the vendor, is calculated to be 2.3 μm at the 5 V reverse bias. Since latchup was experienced, using Ar at 210 MeV (dE/dx = 2.8 MeV/μm), in four devices at normal incidence and in three devices only at angles from 45° to 60°, it appears that the threshold energy is deposited for near normal incidence. Based on these assumptions, the threshold energy would be estimated to be near 2.3 μm × 2.8 MeV/μm = 6.4 MeV. This is equivalent to approximately 0.3 pC. Thus, with the speculative assumption discussed above, it would appear that the critical charge for latchup is on the same order as that for bit-error.

B. CDP-1821 TEST RESULTS ANALYSIS

Figure III-3 shows the conditions for the CDP-1821 tests. Since the devices exhibited bit errors only with 152 MeV krypton ions, a determination of the thickness of the covering material was not necessary to perform the analysis. With the nominal 5 V bias, only one error was observed in one device out of seven tested. This occurred only after a total particle fluence of 6.2×10^5 p/cm^2 (corrected for angle) with ions incident at 75°. This

condition represents the maximum energy deposition that was available from the test.

To determine the critical charge indicated by the data, we consider the thickness of the sensitive region for the CDP-1821 to be 0.5 μm (see Section V.B). With the Kr stopping power at 8.8 MeV/μm and the path length at 0.5/cos 75° = 1.93 μm, the deposited energy in the sensitive region is 17 MeV, which implies a Q_c of 0.8 pC.

Since only one error was observed after several million particles incident over seven devices, it is likely that the minimum energy deposition and critical charge is greater than that calculated above. The single error could be explained by the scattering of an ion along a path length through the 0.5 μm thick sensitive region that was even longer than that calculated above. In view of these results and data obtained previously on CDP-1821 devices (ref 1), the critical charge for bit error in the CDP-1821 operated at +5 V bias is assumed to be somewhat greater than 1 pC.

IV. PREDICTED GALACTIC COSMIC RAY ENVIRONMENT

Galactic cosmic ray ions incident on the TIROS spacecraft in orbit are predominately protons (hydrogen ions) with lesser components of other relativistic particles, all having energies extending indefinitely upward (within the state-of-the-art measurement capability). The alpha particle (helium ion) flux is about an order-of-magnitude less, while the combined flux of all of the other ions is down about another order again (ref 2).

The particle fluxes of specific interest for this analysis are at any surface of the memory chip under study. These data and their limitations, as provided by E. G. Stassinopoulos for this study, are reproduced in Table IV-1. Within the scope of the specific limitations in Table IV-1, the fluxes listed were reduced by a factor of two for this study, and the undefined effects of solar activity were neglected.

Based on a telephone discussion with E. G. Stassinopoulos, two assumptions were made to adapt the data in Table IV-1 to this study. First, the spectral distribution of each ion was assumed to be flat from 0.3 to 15 MeV/n (MeV/nucleon); the actual spectral distribution is unknown; however, this is considered a reasonable estimate. The second assumption extends the fluxes beyond the 15 MeV/n upper limits of Table IV-1; this was done primarily to accommodate the long pathlengths associated with the CDP-1821 sensitive regions (64 μm maximum). For example, a 400 MeV/n iron particle could deposit enough energy in this pathlength for 1 pC of charge, the approximate bit upset threshold. The extension to the differential spectrum derived from Table IV-1, as indicated above, is a simple power law with exponent -2 to approximate the galactic cosmic ray heavy ion spectra (ref 2).

Previous work (ref 1) found the Linear Energy Transfer (LET) spectrum was much more useful than other techniques for expressing the galactic cosmic ray environment in analyses of its effect on MOS circuits. It assumed that the only aspect of significance for any particle was the rate of energy deposition (dE/dx) or LET. Later, it will be shown that the total energy of a

Table IV-1. Attenuated Cosmic Ray Fluxes of Galactic Origin

Evaluated for a shield thickness (range) of 70 mils Al, at the delidded device level.

Z	Ion	Flux (p/cm^2 day) E (out) = 15 MeV/n
1	H	8933.35
2	He	2324.07
3	Li	5.90
4	Be	2.69
5	B	12.49
6	C	50.00
7	N	11.57
8	O	46.81
9	F	1.16
10	Ne	6.94
11	Na	1.71
12	Mg	9.01
13	Al	1.61
14	Si	6.29
15	P	0.25
16	S	1.03
17	Cl	0.23
18	Ar	0.42
19	K	0.34
20	Ca	0.87
21	Sc	0.20
22	Si	0.73
23	V	0.39
24	Cr	0.74
25	Mn	0.49
26	Fe	4.12

Note: Table is for maximized exposure (deepest penetration into magnetosphere), using E (out) = 15 MeV/n.

Variations in background (on account of solar activity) may be as large as a factor of 20; since flux values used were maxima, any adjustment factor should be leading to lower values only.

Fluxes should be reduced by about a factor of 2 (at least) because omnidirectional incidence has been assumed, which is not the case near the earth (1000 km altitude) at high latitude and polar regions.

Cosmic rays of solar origin ray occasionally exceed the galactic background by factors of 10^3 to 10^5 (for major flare events).

(Source: E. G. Stassinopoulos, NASA-GSFC, 1980)

particle can also have a significant impact; therefore, the technique has been modified in its application to the environment described above.

The ultimate goal of the environment part of the analysis was to develop the TIROS-N model of a linear charge deposition spectrum to be used with the pathlength distribution and device parameters to determine the expected bit error rates in orbit. The methodology used in the development of this model will be described in the following paragraphs. It should be noted that the work was done manually with the indispensable aid of a programmable calculator to test the sensitivities of the various approaches to the development. There was insufficient time to refine the environment model through programming the various steps on a computer; however, the uncertainty associated with the environment does not really warrant this added sophistication.

Initially, the particle counts provided in Table IV-1, reduced by a factor of 2 as discussed earlier, were divided equally among five bins for each ion with Z from 3 to 26 (lithium through iron) and 50 bins each for hydrogen and helium. Each of these bins was then assigned a nominal stopping power based on the Northcliffe and Schilling data (ref 3). The ion fluxes for each of these 220 bins were then listed in order of decreasing stopping power from the maximum (for iron: 26.9 MeV-cm^2/mg) to 0.1 MeV-cm^2/mg, which is about an order-of-magnitude below the expected minimum value of interest for this study. The fluxes were then cumulated in descending order for the preliminary LET-spectrum. This spectrum was then transformed to a linear charge deposition spectrum assuming the ionization rate in silicon is 3.6 eV/carrier pair, 6.24×10^{18} electrons/coulomb, and the density of silicon is 2.33 gm/cm^3 (0.233 mg-cm^{-2}/μm).

The next step in the development of the model was to incorporate the extension beyond the 15 MeV/n upper limit. The technique was similar, except for some simplification based on the earlier results. A total of 19 energy bins were used between 15 and 1000 MeV/n (maximum) with the widths increased in steps in view of the rapidly decreasing differential flux and stopping

power contributions. The ion types were divided into nine groups somewhat arbitrarily based on considering the size of the bin fluxes and similarities in stopping power. As before, nominal stopping powers were assigned to each bin down to the 0.1 MeV-cm^2/mg cutoff; then the bin fluxes were ordered by decreasing stopping power and cumulated as before. These data were changed to a linear charge deposition spectrum and combined with the one for 0.3-15 MeV/n. The resulting linear charge deposition spectrum is the highest-valued one shown in Figure IV-1; it includes all the particles within the charge deposition range indicated.

It became apparent in the course of the analysis that even though some of the particles had the stopping power to lead to a bit upset, they lacked the required kinetic energy. For example, if a device bit upset threshold were 1 pC, at least a 22.5 MeV ion energy would be required. In terms of particle energies per nucleon in this case, for example, the minimum cutoff energies range from 22.5 MeV/n for the hydrogen ion to 0.4 MeV/n for the iron ion.

The effects of eliminating ions with charge depositions with less than 0.5, 1, and 2 pC are shown in Figure IV-1. Within the limits of potential concern to this study, 0.01 to 0.28 pC/μm, the differences are small compared with the uncertainties associated with the environment.

The actual TIROS-N Model Linear Charge Deposition Spectrum from the algorithm used in computer analyses of the devices is shown in Figure IV-2 as the "Extended Spectrum." The dots shown in the vicinity of this curve are selected data points for the 0.5 and 1 pC spectra of Figure IV-1. The corresponding curve for the Table IV-1 ($\leq$ 15 MeV/n) data is also shown for comparison; the differences (in the 0.01 to 0.28 pC region of concern) are significant but they probably would not adversely bias the end results of the analysis substantially.

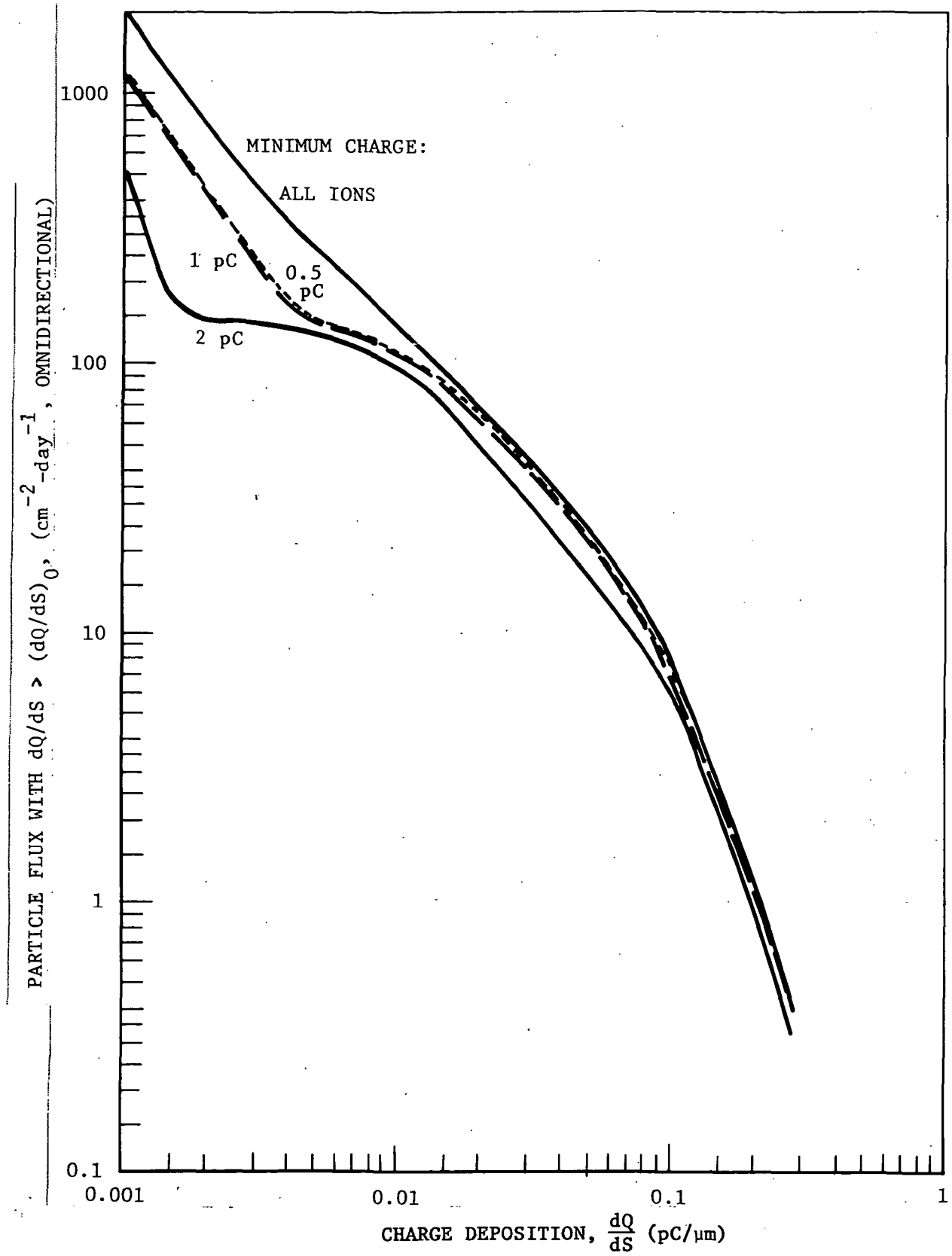


Figure IV-1. Linear Charge Deposition Spectra

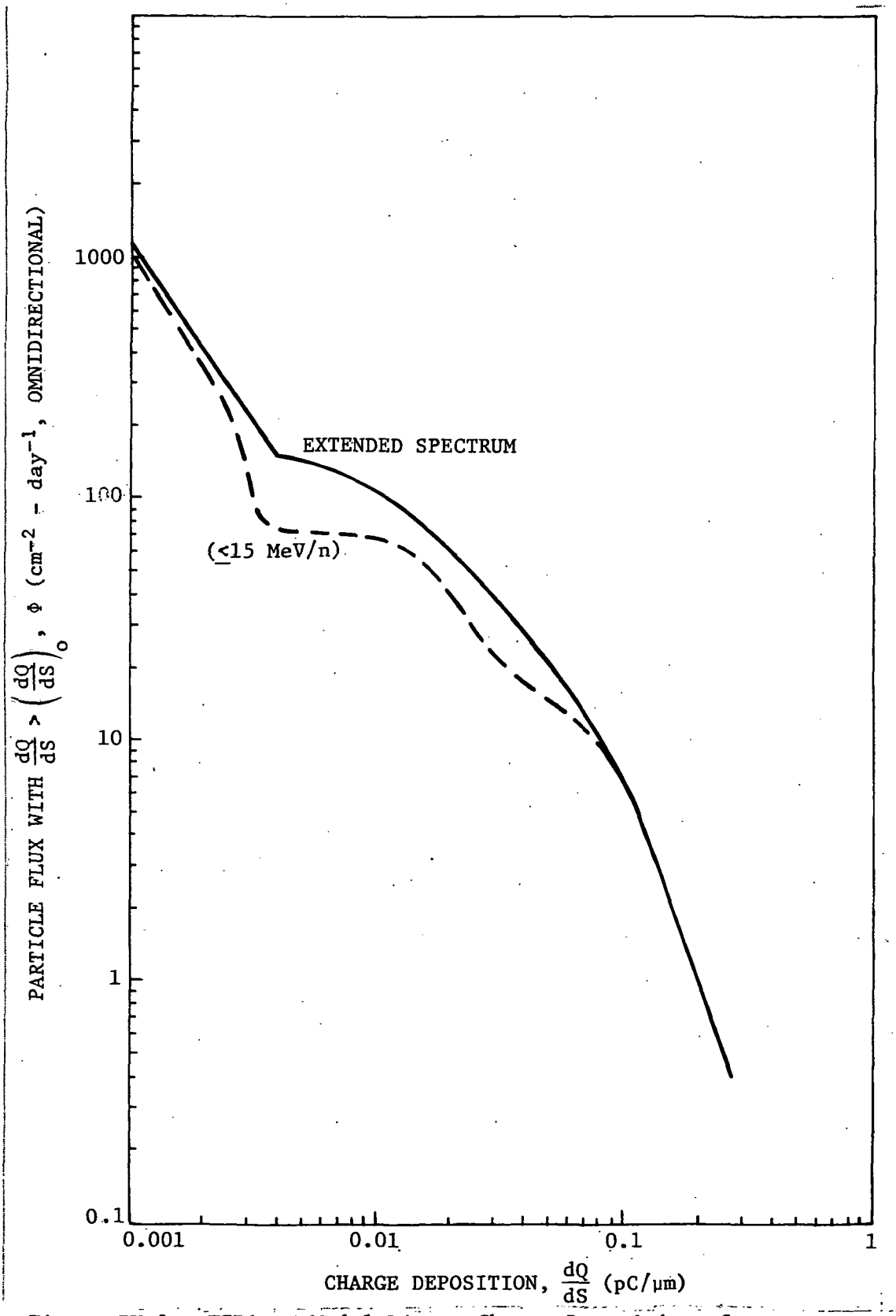


Figure IV-2. TIROS-N Model Linear Charge Depositions Spectrum

V. ANALYSIS AND DISCUSSION FOR SPACE ENVIRONMENTS

A. HARRIS HM1-6508

1. Bit-Error

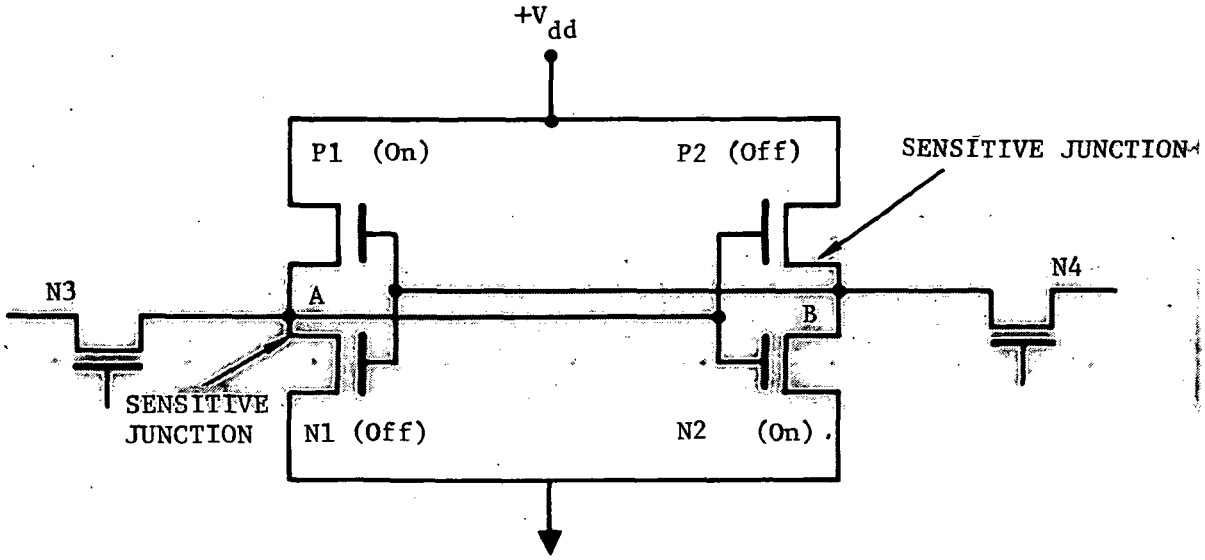
The Harris HM1-6508 CMOS RAM is organized as a 1024 x 1 bit memory device and utilizes silicon gate technology on a bulk silicon substrate. The memory cells are organized as six transistor cells as shown in Figure V-1(a). Specific information required for the cosmic ray analysis was requested from Harris representatives and the information received is shown in Table V-1. To obtain additional required information and to clarify the Harris information, a detailed physical analysis of a HM1-6508 chip was performed at Rockwell.

It is important to know the thickness of material above the sensitive regions to correctly account for energy loss of the ions used in the cyclotron simulation testing. To determine this, a HM1-6508 die was removed from the existing package, mounted in lucite, and cut on a cross-section through a region of transistors in the peripheral circuitry. Figure V-2 shows a microphotograph of the complete die and Figure V-3 shows a close-up view of the die surface in the region where the cut was made. The cut region was then viewed edge-on to show the cross-section. Figures V-4 through V-7 show high magnification (2048X) cross-sectional views of various pertinent regions. From these photographs, the following information was determined:

Aluminum thickness	-	1.33 μm
Glassivation thickness	-	1.12 μm
Field oxide thickness	-	1.54 μm
Poly-silicon gate thickness	-	0.56 μm
Gate oxide thickness	-	<.1 μm
Junction diffusion thickness	-	0.84 μm

The measured thicknesses were in reasonable agreement with the data supplied by Harris.

(A) SCHEMATIC



(B) CROSS-SECTION

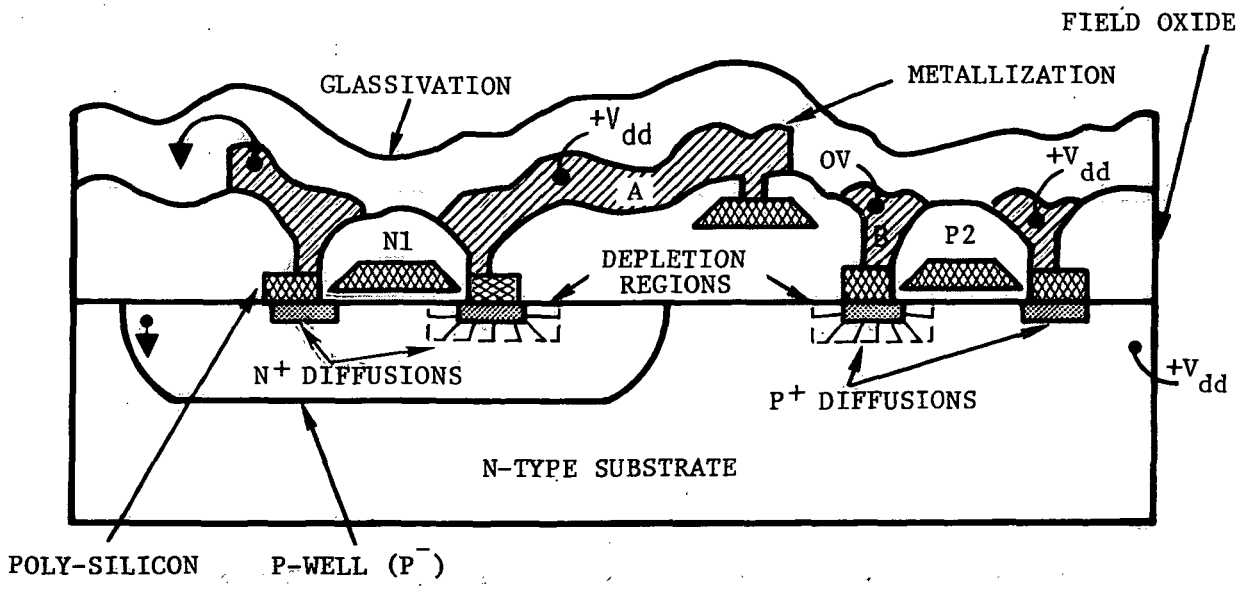


Figure V-1. HM1-6508 Memory Cell

Table V-1. HM1-6508 Device Information Received from Vendor

Substrate Doping	: $N_D = 1.3 \times 10^{15}$ cm^{-3} typical
P-Well Doping	: $N_A = 1.4 \times 10^{16}$ cm^{-3} typical
Glassivation Thickness	: 7 kÅ (?)
Field Oxide Thickness	: Al-Si - 13.5 kÅ Poly-Si 7 kÅ
PolySi Thickness	: 6 kÅ typical
Aluminum Thickness	: 12 kÅ typical
P-Channel Threshold	: -0.8 V typical
N-Channel Threshold	: +0.9 V typical
A_{JP1}	= 0.27 mil^2 (174 $\overline{\mu m^2}$)
A_{JP2}	= 0.3075 mil^2 (198 $\overline{\mu m^2}$)
A_{JN2} & A_{JN3}	= 0.45 mil^2 (290 $\overline{\mu m^2}$)
A_{JN2} & A_{JN4}	= 0.4375 mil^2 (282 $\overline{\mu m^2}$)
P_1 W/L	= 0.2/0.3 mil (5/8 µm)
P_2 W/L	= 0.2/0.3 mil (5/8 µm)
N_1 W/L	= 0.775/0.15 mil (20/4 µm)
N_2 W/L	= 0.875/0.15 mil (22/4 µm)
N_3 W/L	= 0.5/0.15 mil (13/4 µm)
N_4 W/L	= 0.55/0.15 mil (14/4 µm)

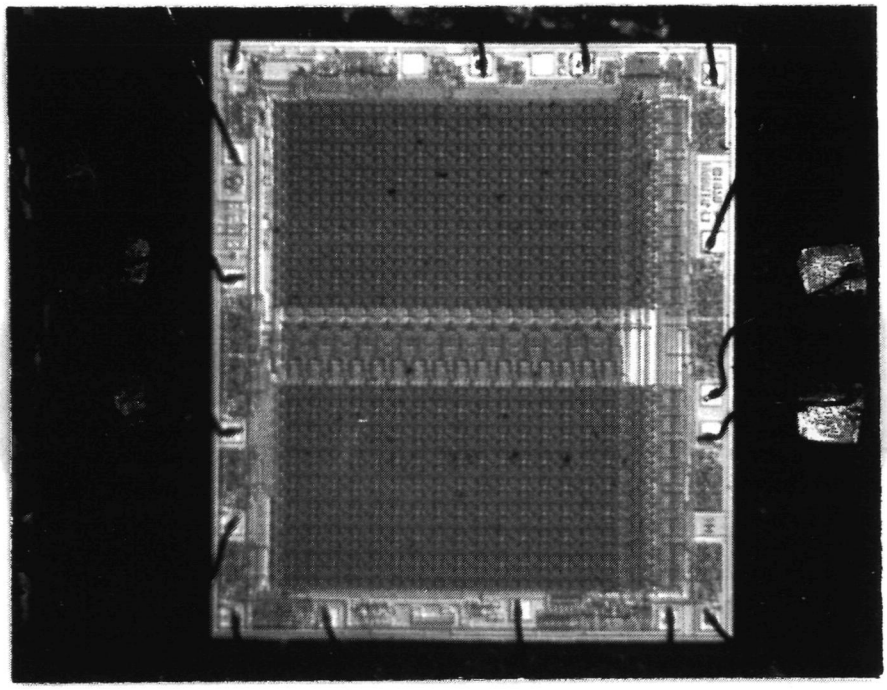


Figure V-2. Die Surface (25X)

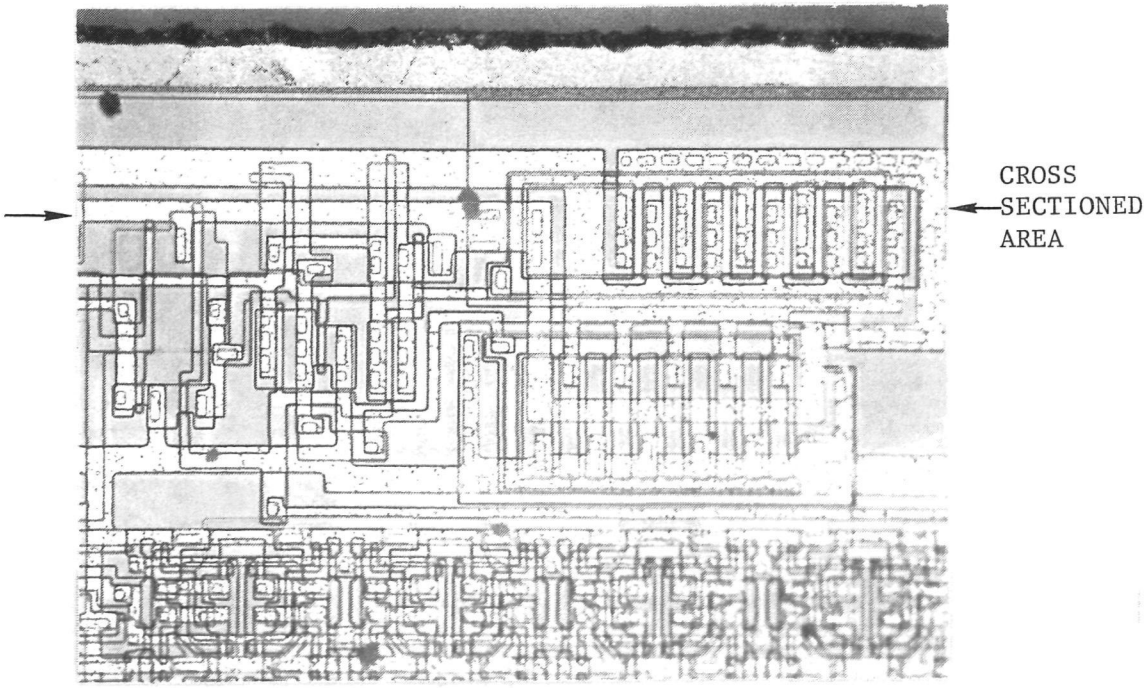
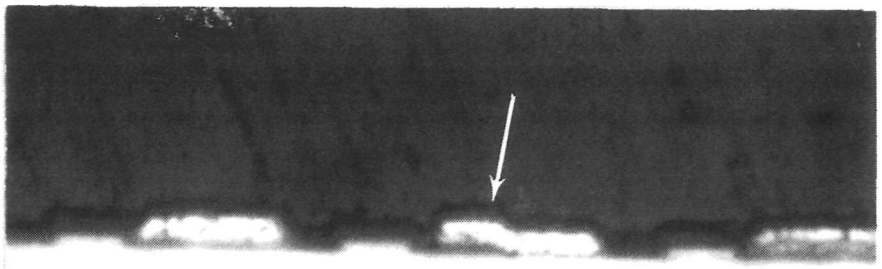
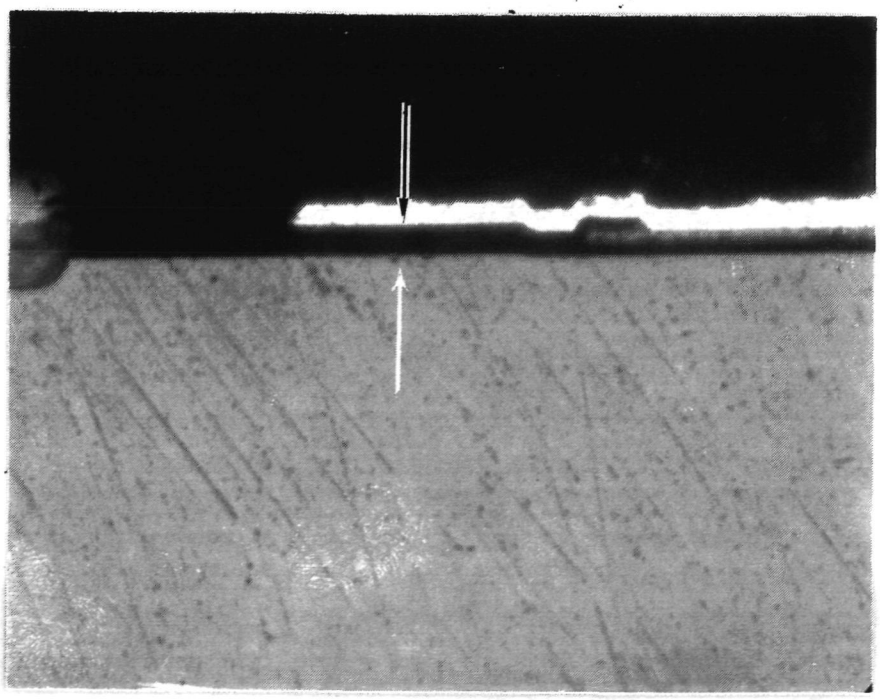


Figure V-3. Region of Cut (100X)



11,200Å
Glassivation

Figure V-4. Glassivation Thickness (2048X)



15,400Å
Field Oxide

Figure V-5. Field Oxide Thickness (2048X)

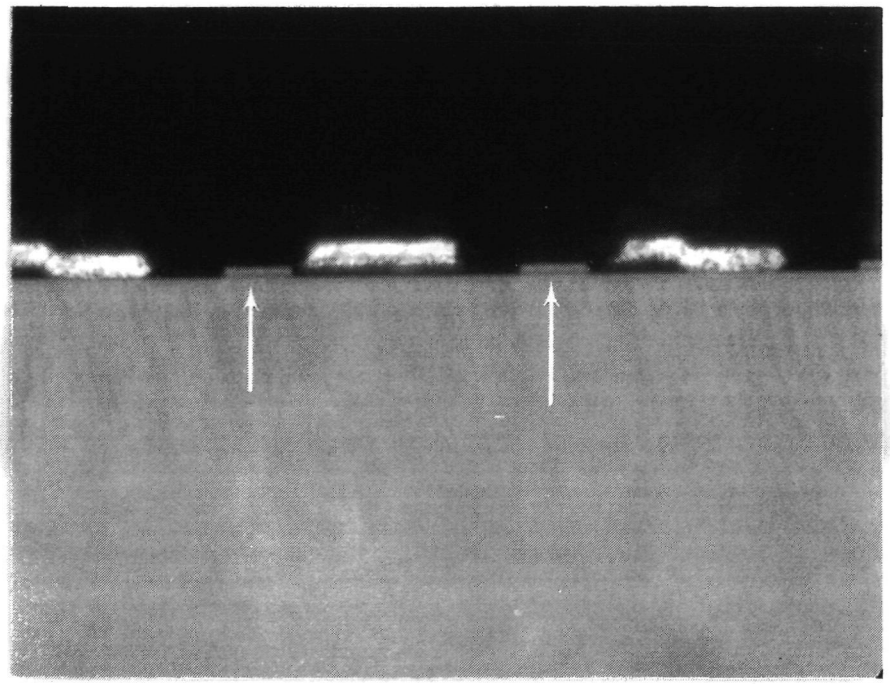


Figure V-6. Polysilicon Gate Thickness (2048X)

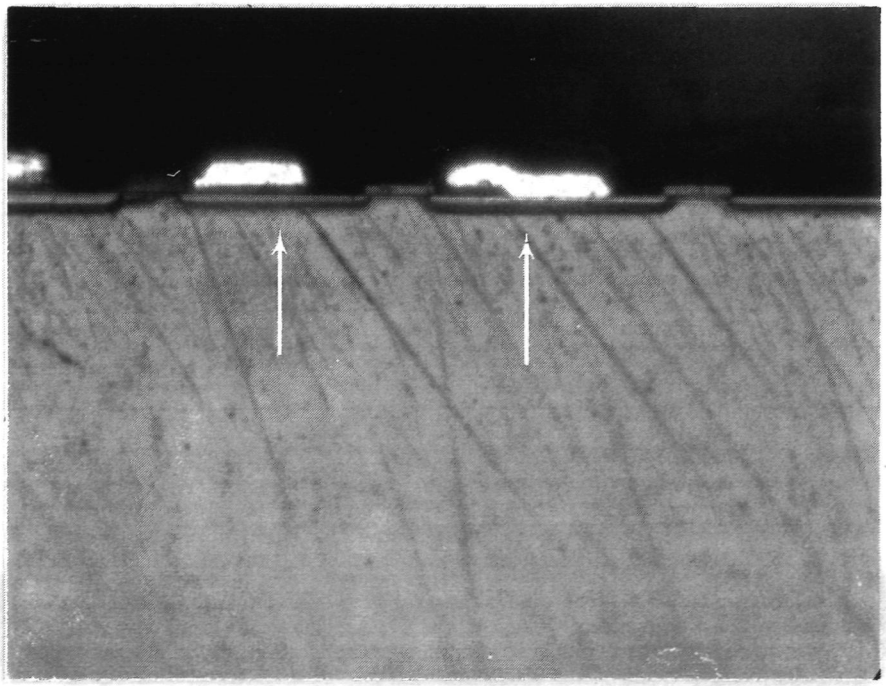
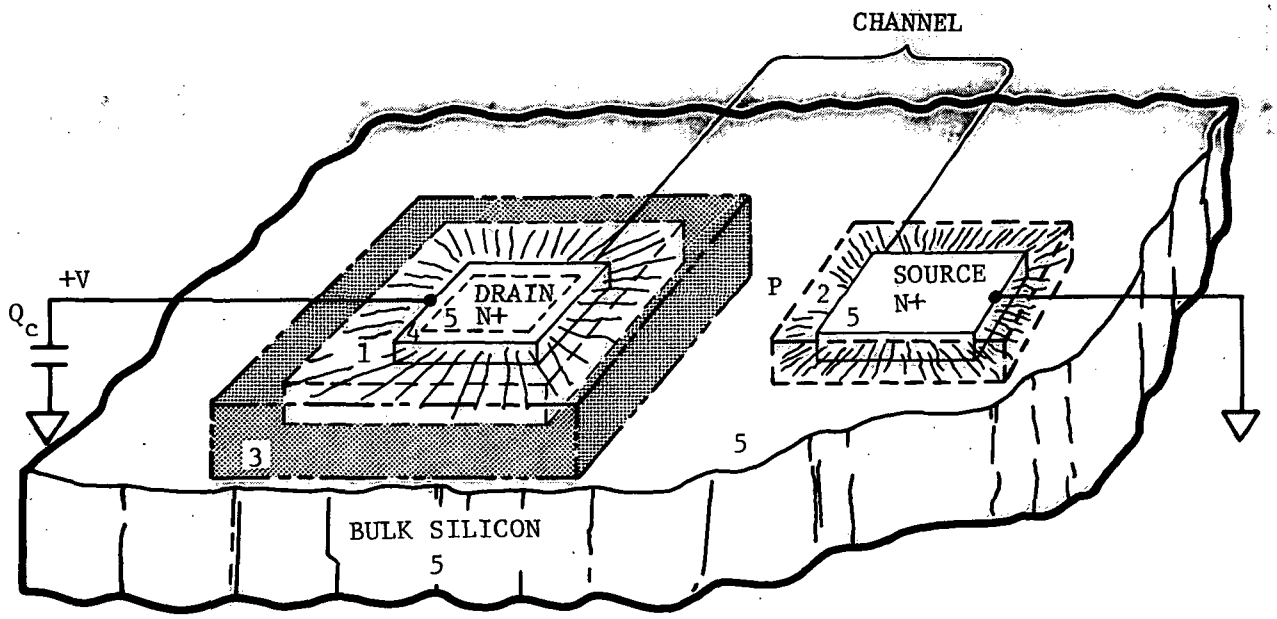


Figure V-7. Drain/Source Diffusion Thickness (2048X)

To determine the thickness of material above the sensitive regions, we start at the depletion region in the bulk silicon under a drain diffusion (see Figure V-1(b)) and work toward the surface. We then must account for 0.84 μm of Si (the heavily doped drain), 0.56 μm of poly-silicon (this serves as contact for the interconnects), 1.54 μm of field oxide (isolates aluminum from polysilicon), 1.33 μm of aluminum (covers approximately 75 percent of diffusions) and 1.12 μm SiO_2 glassivation. The total is 1.40 μm of Si, 2.66 μm of SiO_2 and 1.33 μm of Al. For analysis, we convert to an equivalent thickness of aluminum and determine a total shielding of 4.8 μm (Al equivalent) or 5.5 μm (Si equivalent).

To determine the sensitive regions, we consider the memory cell as shown in Figure V-1. For any particular node in the memory circuit, the associated sensitive regions are those p-n junctions which have a voltage across them; normally, this voltage drop will be the V_{dd} potential. For example, if the logic state is such that node A is biased at $+V_{dd}$ and node B is at ground, the drain junctions of N1 and P2 are sensitive regions. Any ionization in these depletion regions will transfer charge to the affected node. For ionization in the junction of N1, electrons will be collected, resulting in a negative voltage spike at node A. For ionization in the junction of P2, holes will be collected, resulting in a positive voltage spike at node B. If the voltage spikes are of sufficient amplitude and charge, neutrality cannot be established fast enough through the associated "ON" transistor, the flip-flop may regenerate and a bit error will occur.

Figure V-8 illustrates the various charge collection regions in a typical bulk N-channel transistor. Region 1 is the depletion region associated with the drain junction. Since the electric field is relatively high in this region, most carrier pairs generated by ionization will become separated. For positive bias on the drain, the electric field is such that electrons will be swept to the drain and holes will be swept to the bulk substrate.



*RESULTS IN CHARGE DISTURBANCES ON DRAIN CAPACITANCE

REGION 1* ELECTRONS SWEPT TO DRAIN,
HOLES SWEPT TO SUBSTRATE
REGION 2 ELECTRONS SWEPT TO SOURCE,
HOLES SWEPT TO SUBSTRATE
REGION 3* ELECTRONS MAY DIFFUSE TO DRAIN
REGION 4* HOLES MAY DIFFUSE TO SUBSTRATE
REGION 5 ELECTRONS AND HOLES RECOMBINE

Figure V-8. Bulk Transistor Charge Collection Regions

The electrons collected at the drain will result in a negative transient in the charge stored on the capacitance associated with the drain node. Region 2 is the depletion region assiciated with the source junction. For carrier pairs generated in this region, the electric field results in electrons being swept to the source and holes swept to the substrate. Since both are grounded, this has no effect on the charge at the drain node. For carrier pairs created in Region 3, some electrons may diffuse to the edge of the depletion region (1) and then be swept along the field lines to the drain. This results in a charge disturbance on the drain although it will be delayed by the diffusion time in Region 3. For carrier pairs generated within the heavily doped drain near the junction edge (Region 4), it is possible that some holes could diffuse to the junction edge and then be swept along the field lines through the depleted region to the substrate. However, the diffusion length for holes within this region is very small, due to the high concentration of free electrons, and this region can be neglected for most devices. Within the drain and source region and within the bulk substrate at distances more than a diffusion length from the junction, the carrier pairs eventually recombine and have no effect on the drain charge.

For bulk technology devices, the depletion region extends down into the bulk silicon beneath a junction as well as at the edges of the diffusion. Consequently, the sensitive region is generally larger than for Silicon on Sapphire (SOS) technology. The depletion depth depends on the doping densities and the junction bias. The sensitive region may be approximated as a parallelepiped with thickness equal to the depletion depth, and planar dimensions equal to the length and width of the diffused area extended to account for the depletion width. This approximation overestimates the sensitive volume by the volume of the drain/source diffusion.

For ionization within the depletion region, it is assumed that all the induced charge is collected. For ionization in regions within a diffusion length of the depletion regions, the minority carriers may be collected if they diffuse to the edge of the depleted region.

The relative importance of the diffusion current contribution to the critical charge depends on the temporal charge disturbance sensitivity of the device. That is, ionization within the depletion region results in a very fast charge transfer, while minority carriers which must diffuse to reach the depletion region edge will arrive at relatively later times. For the CMOS bistable flip-flop storage element, a recharge path through complementary transistor which is biased "ON" is present; consequently, it is not the total charge collected but rather the temporal distribution and resulting voltage transients that determine a bit-flip. For the HM1-6508 devices, the diffusion current apparently does not make a significant contribution. This fact can be deduced from comparing the calculated bit-error cross-section, based on the area of the depletion regions, and the measured cross-section at the cyclotron using ion at normal incidence to the chip which exceeds the energy threshold for bit-flip. The calculated cross-section is 7×10^{-3} cm^2. The average measured cross-section using 210 MeV argon ions at normal incidence generally ranged from 3×10^{-3} to 9×10^{-3} cm^2.

Neglecting diffusion currents, the sensitive region for a particular sensitive junction is determined by the size of the diffusion and the thickness of the junction depletion region at the operating bias.

A detailed study of the HM1-6508 topology was performed to ascertain the size and shapes of the source and drain diffusions. The study was performed by sequentially removing layers of material and photographing a memory cell region. Figure V-9 shows the region studied before any material has been removed. Figure V-10 shows the same region with the glassivation and metal removed. Figure V-11 shows the region with the poly-silicon removed. In Figure V-11, the N^+ and P^+ diffusion and the P-well for the N-Channel transistors can clearly be seen. Figure V-12 shows a close-up of the diffusions and identifies those associated with the various transistors as defined in Figure V-1.

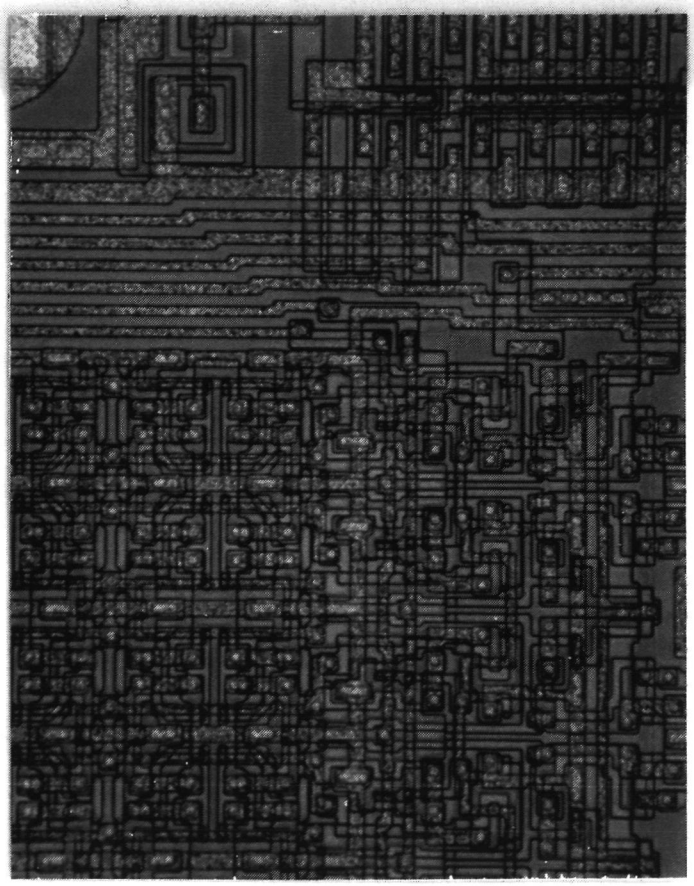


Figure V-9. Die Surface With Nothing Removed (200X)

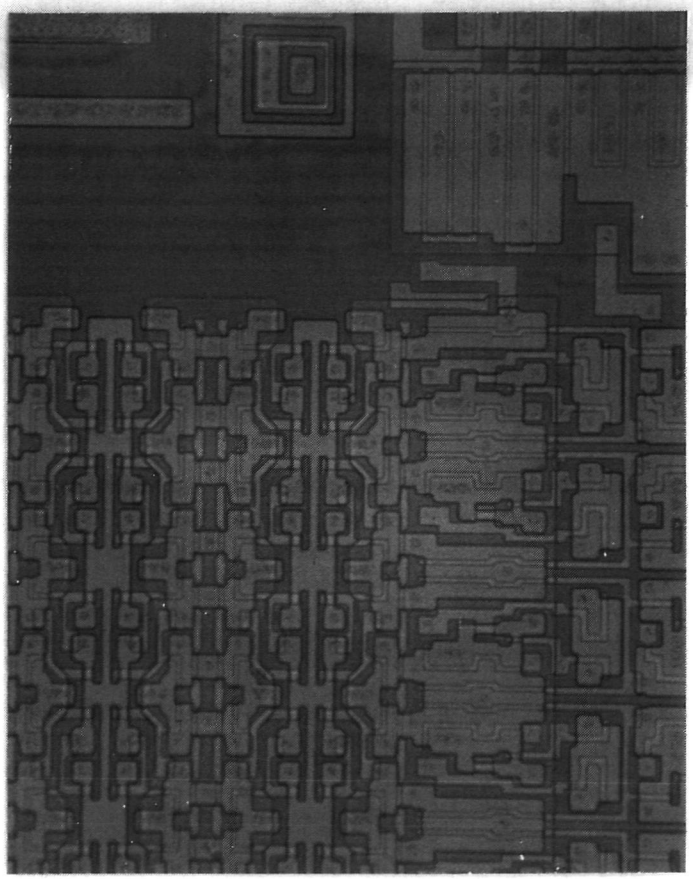


Figure V-10. Die Surface With Metal Removed (200X)

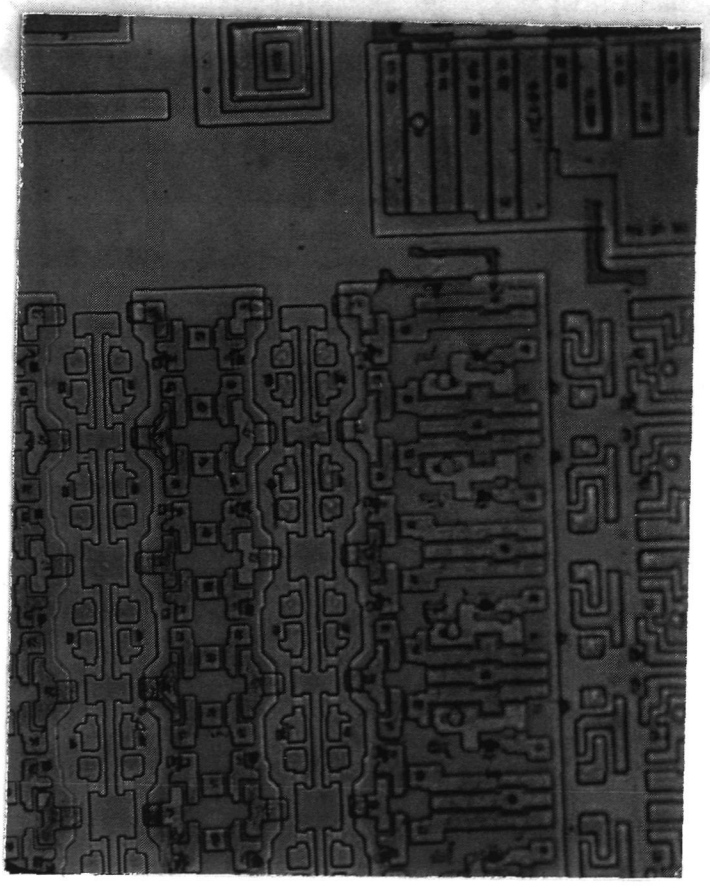


Figure V-11. Die Surface With Metal and Poly-Si Removed (200X)

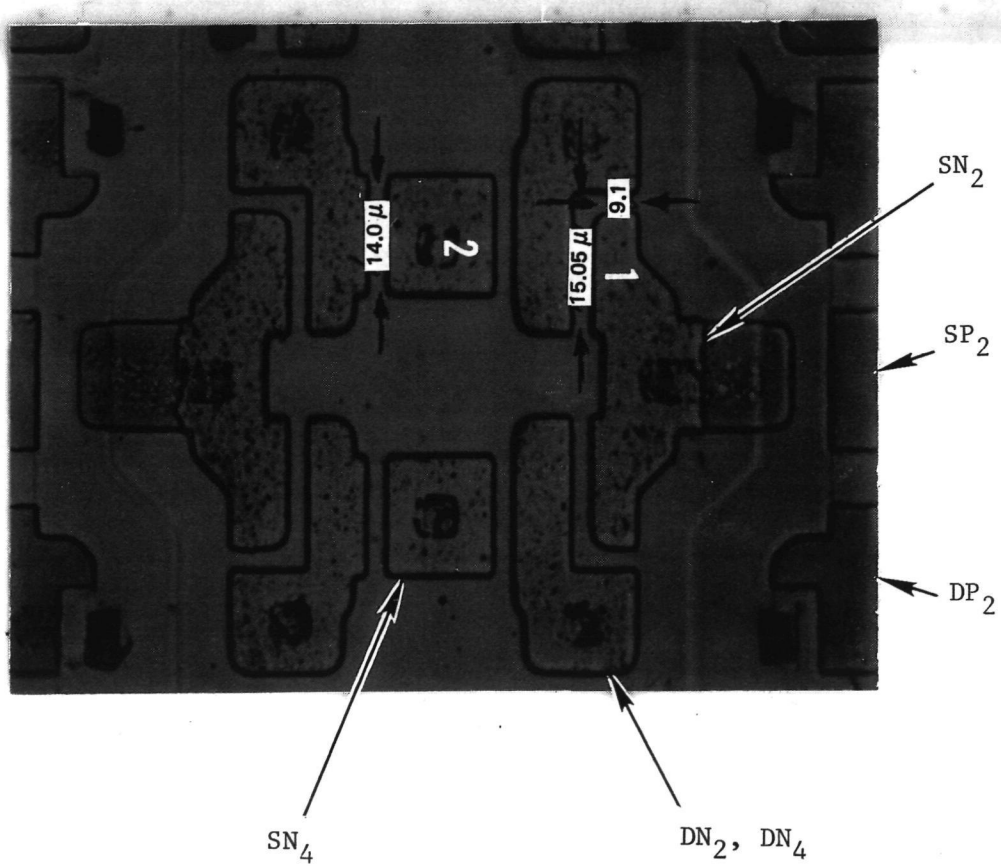


Figure V-12. Memory Cell Transistor Diffusions (1000X)

From a study of these photographs, the size and shape of the transistor diffusions for a memory cell were determined and are drawn in Figure V-13. To predict the bit-error rate using the CRIER code, the sensitive region must be defined as parallelepiped. Thus, rectangular regions were defined as shown in Figure V-14 which simulate the actual regions and have approximately the same area.

To determine the depth of the sensitive regions, we calculate the depletion region width at the operating bias. Using a step junction approximation, the depletion width is given by

$$W = \sqrt{\frac{2K\epsilon_o (\phi_\beta + V_r)}{qN}} \qquad (5\text{-}1)$$

when

$K = 11.7$

$\epsilon_o = 8.86 \times 10^{-14}$ F/cm

$q = 1.6 \times 10^{-19}$ coulomb

$\phi\beta \cong +0.6$ V for P-substrate

$\cong -0.6$ V for N-substrate

V_r = Reverse junction bias [volts]

N = Substrate doping [cm^{-3}]

At $V_{dd} = 5$ V, the depletion width for the N-channel drain junction is 0.72 μm and for the P-channel the junction is 2.1 μm.

Thus, the sensitive regions for a memory all can be approximated by parallelepipeds with dimensions as defined in Table V-2. The depletion width determines H, while W and L are determined by the dimensions of the rectangular region which simulate the drain diffusion with extension to account for the depletion width.

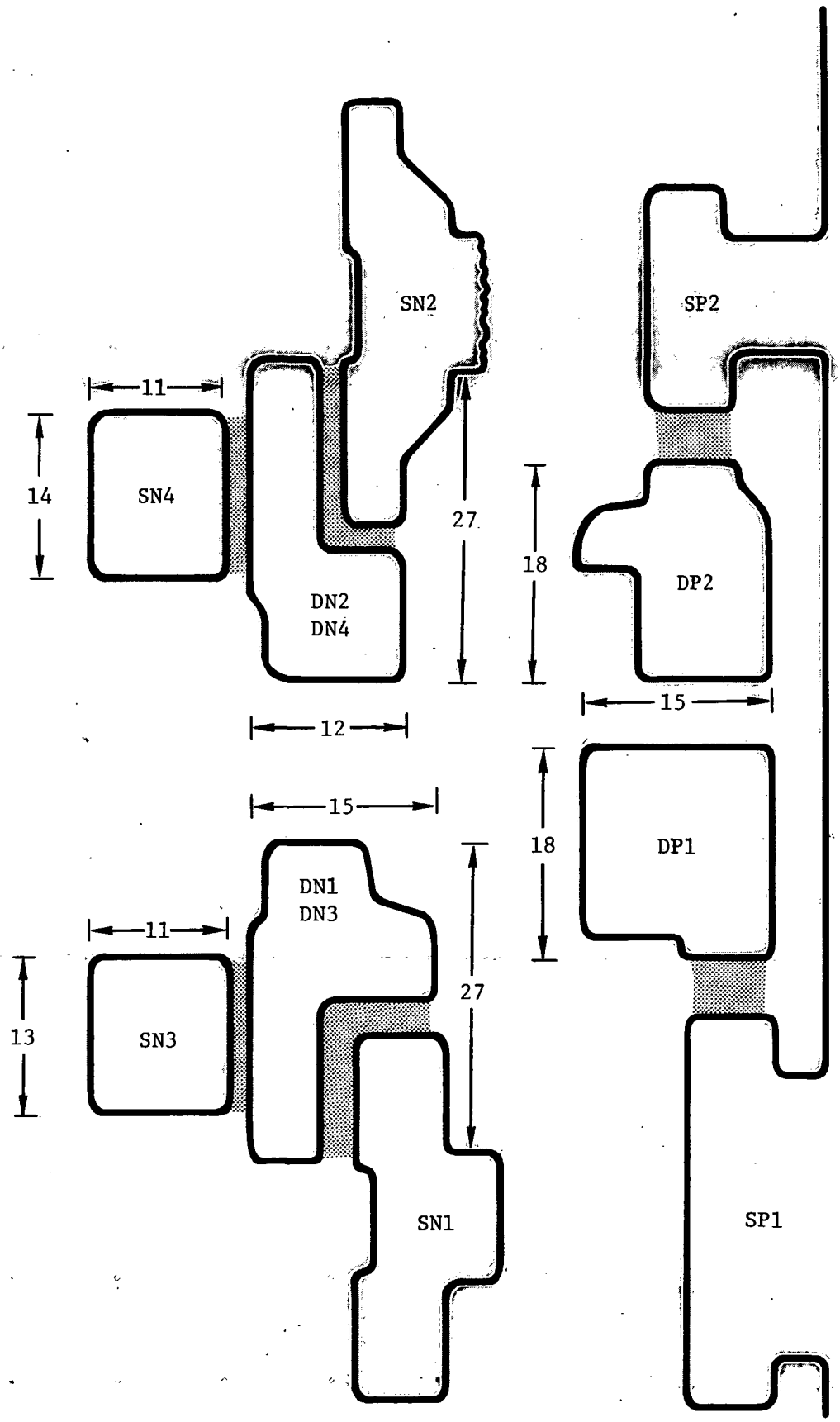


Figure V-13. Area of Sensitive Regions

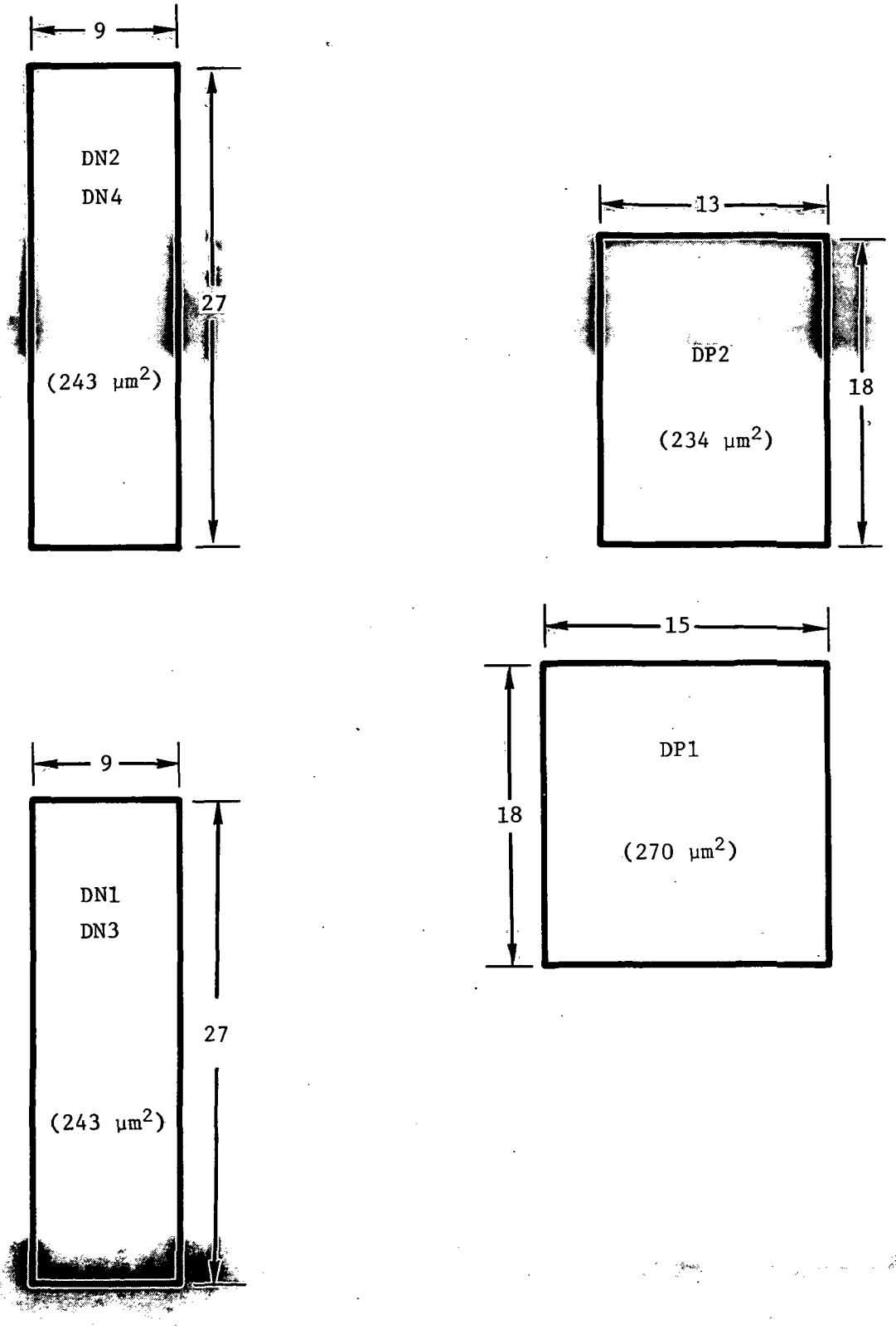


Figure V-14. Simulated Sensitive Region Area For CRIER Analysis

Table V-2. Dimensions of Sensitive Regions

Transistor	H (μm)	W (μm)	L (μm)
N2 and N4	0.72	10.4	28.4
N1 and N3	0.72	10.4	28.4
P2	2.1	17.2	22.2
P1	2.1	19.2	22.2

Note that the input and output transistor N3 and N4 share a common drain with the N-channel devices of the memory cell. Consequently, there are only four regions of concern for each memory cell. Only two of these are sensitive at any given time; that is, N1 and P2 or N2 and P1.

The Cosmic Ray Induced Error Rate (CRIER) code was used to calculate the error rate for each of the sensitive regions defined in Table V-2 using the TIROS II environment model. The results are shown in Figure V-15 and terms of events per day for which charge greater than or equal to a given charge are deposited in a given sensitive parallelepiped volume vs critical charge. Since there are two states possible for the memory cell ("1" or "0"), we consider both states equally likely and calculate the average Error Rate (ER) for a memory cell as:

$$\overline{ER} = \tfrac{1}{2}\left\{\left[ER(N1) + ER(P2)\right] + \left[ER(N2) + ER(P1)\right]\right\} \qquad (5\text{-}2)$$

This result is shown as the dashed line on Figure V-15.

2. Latchup

The HM1-6508 devices were observed to exhibit latchup readily during the cyclotron testing. The latchup could be induced by single ions of either Kr or Ar. Latchup could also be induced electrically by increasing the supply voltage (V_{dd}) above 15 V or by applying voltage to the input/output terminals before application of V_{dd}. Other investigators have also reported latchup in HM1-6508 devices (ref. 4).

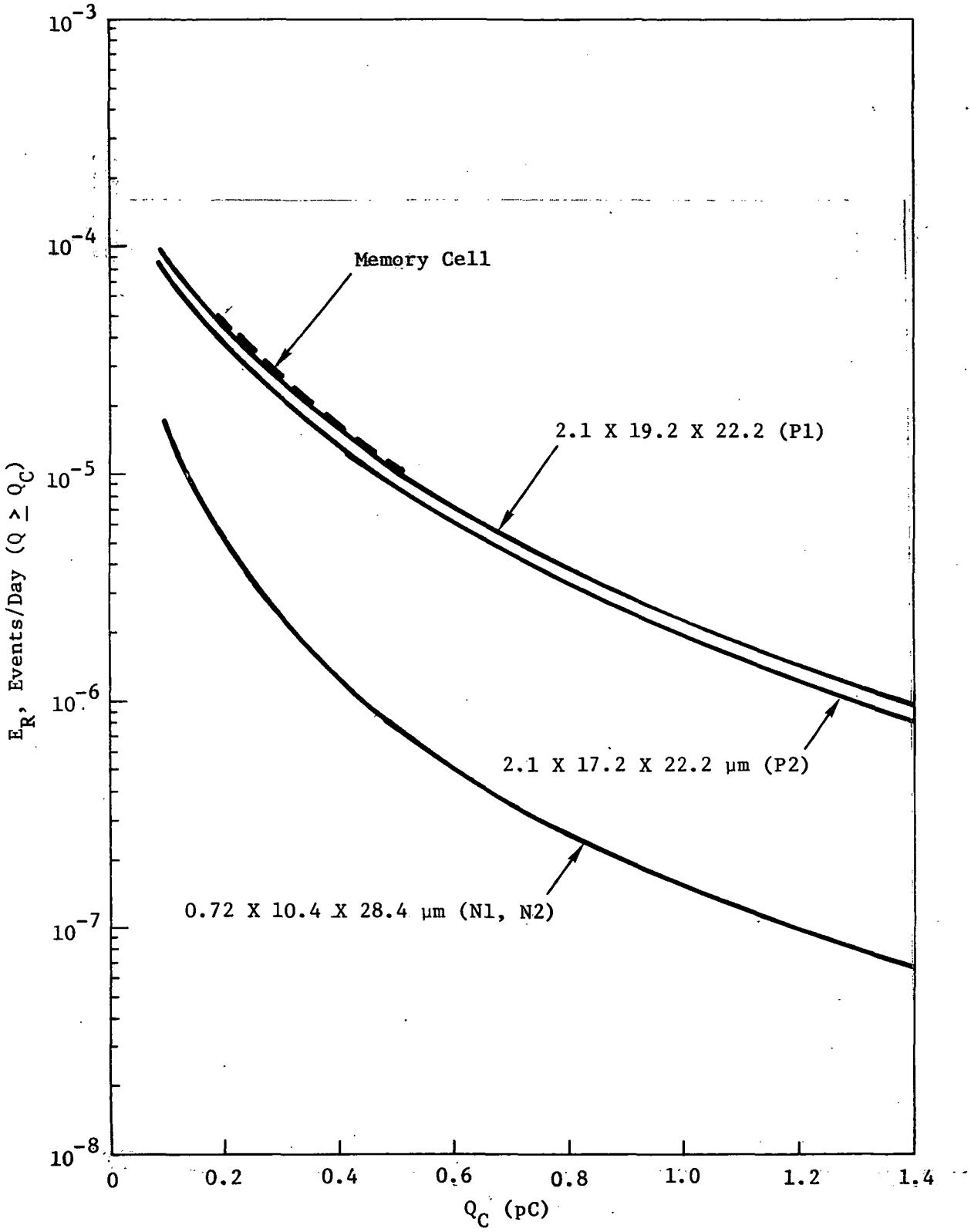
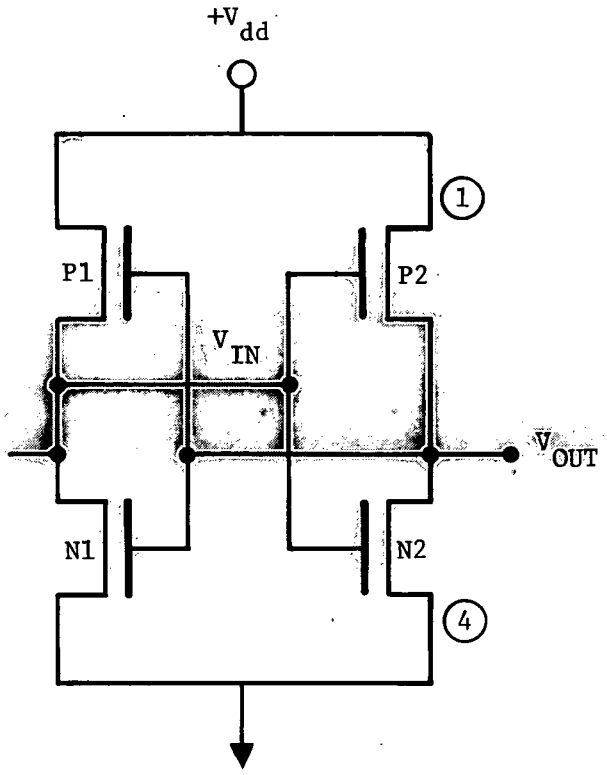


Figure V-15. Error Rate vs Critical Charge For HM1-6508 (TIROS Environment)

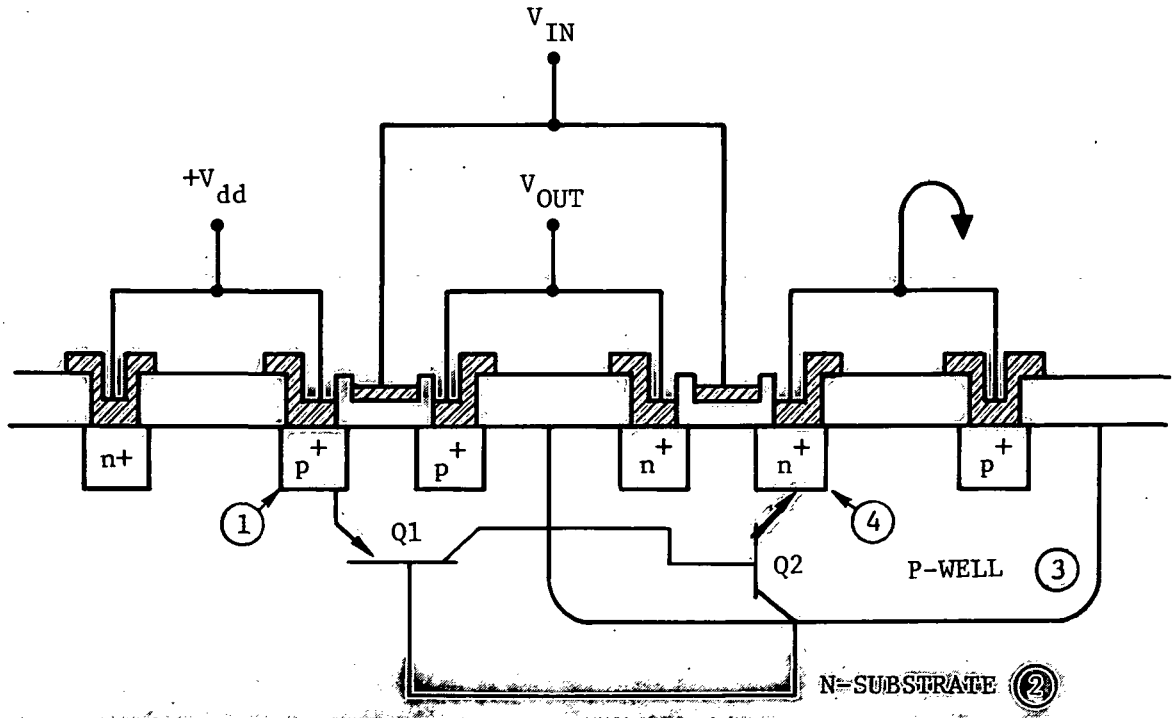
The following paragraphs will discuss the latchup mechanism, in general, for CMOS devices and provide a "rough" estimate of the expected latchup rate in the TIROS environment, based on the cyclotron simulation results and several simplifying assumptions. A detailed examination of the latchup mechanism in this device type or a precise prediction of expected latchup rate in space was beyond the scope of this program and not attempted.

Some CMOS integrated circuits fabricated with bulk silicon technology typically exhibit latchup when exposed to high dose-rate ionizing radiation environments or to voltage overstress conditions. The latchup mechanism has been shown to be caused by regenerative switching, analogous to a Silicon Controlled Rectifier (SCR), in the adjacent parasitic bipolar transistors formed during bulk CMOS fabrication (ref 5). Once latchup has been initiated, it is usually self sustaining and can lead to thermal overstress of the device if the supply current is not limited. Naturally, the circuit is inoperative during latchup, although other areas of circuitry in a large integrated circuit may continue to function under some conditions.

The latchup condition results in the creation of a low resistance path between the power supply (V_{dd}) and ground on a circuit. Latchup occurs due to parasitic four layer pnpn paths. Figure V-16 shows the HM1-6508 memory cell and a cross-section of one inverter. Notice that in going from regions 1 through 4, we have a pnpn structure and that there are parasitic cross-coupled bipolar transistors, Q1 and Q2. The pnpn diode when biased with the anode positive has two stable states. One is a very high resistance state (normal condition) and the other a very low resistance state (latchup condition). From analysis of the four layer structure, it can be shown (ref 6 and 7) that as the sum of the current gains of the two parasitic transistors $\alpha_1 + \alpha_2$ approaches unity the current flow through the structure becomes very large. Such behavior is related to the regenerative manner in which the two parasitic transistors are interconnected. The collector current of Q1 is furnished as the base current of Q2, and vice versa. When the pnpn diode is operated in such a manner that the sum $\alpha_1 + \alpha_2$ is less than unity,



(A) MEMORY CELL COMPOSED OF CROSS-COUPLED INVERTERS



(B) SCHEMATIC CROSS-SECTION OF ONE INVERTER SHOWING PARASITIC PNPN PATH AND BI-POLAR TRANSISTORS

Figure V-16. Latchup Path in HM1-6508 Memory Cell

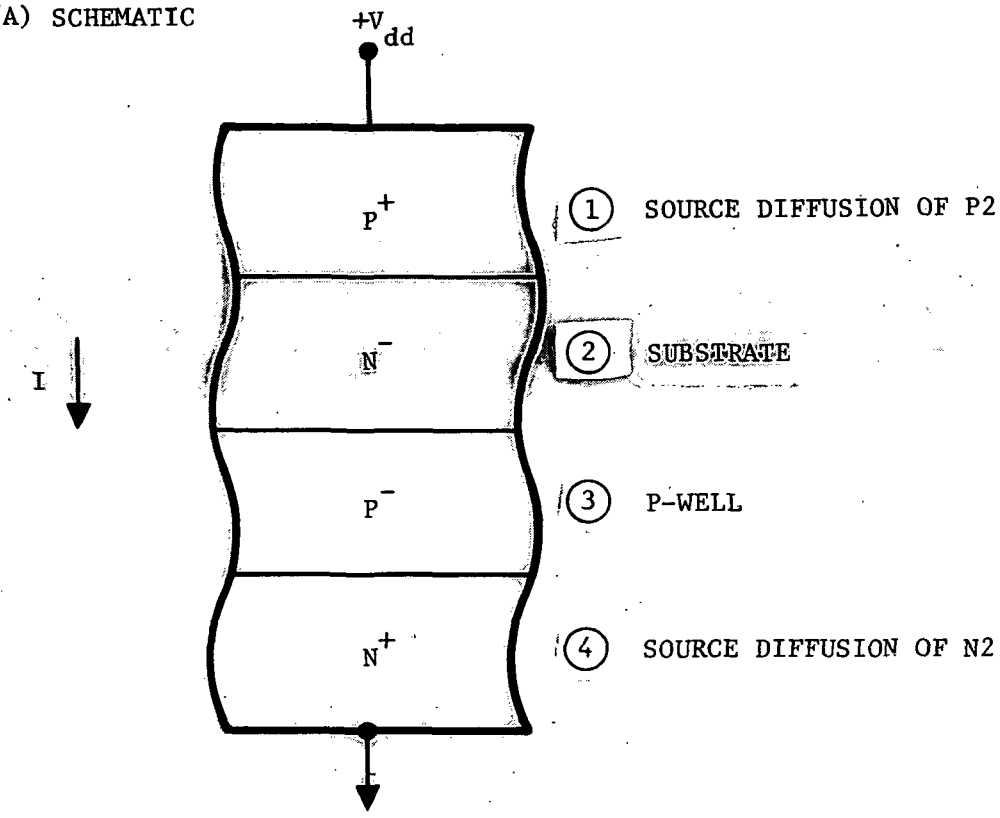
the impedance is high and the current is small. When the condition of $\alpha_1 + \alpha_2 = 1$ is attained, the impedance becomes very low, as all junctions become forward biased and the current reaches a value limited by the power supply internal impedance.

Figure V-17 illustrates a typical pnpn diode and the volt-ampere characteristics. The numbered regions correspond to those of Figure V-16. When a forward voltage is applied, only a small current will flow until the voltage attains the breakover voltage V_{BO}. If the voltage is increased beyond V_{BO}, the diode will switch from its Off (high impedance) state to its On (low impedance) state and will operate in the saturation region; the device is then said to be latched. If the voltage is now reduced, the switch will remain On until the current has reduced to I_H. This current and the corresponding voltage V_H are called the holding current and voltage, respectively. The current I_H is the minimum required to hold the switch in its latched state.

The forward breakover voltage is reduced by current flow through one or both of the outer junctions, ie, region 2 to region 1 or region 3 to region 4. Such behavior is expected on the basis for the requirement for $\alpha_1 + \alpha_2 = 1$ to establish the breakover voltage; the increased current flow increases the α for the affected junction.

The mechanism for an individual cosmic ray ion to induce latchup is believed to be a transient reduction of the holding current for the pnpn diode to a value below the V_{dd} supply voltage, allowing breakover and latchup. The ionization induced photocurrent flows through a junction, increasing the current gain (α), such that the requirement $\alpha_1 + \alpha_2 = 1$ is met at the V_{dd} voltage. From Figure V-16, we observe that current flow from the substrate (region 2) to the P^+ source diffusion (region 1) or from the P well diffusion (region 3) to the N^+ source diffusion (region 4) would increase the current gain of Q1 or of Q2 respectively. Current flow across the junction at the P-well diffusion and the substrate could affect the current gain of both

(A) SCHEMATIC



(B) I-V CHARACTERISTICS

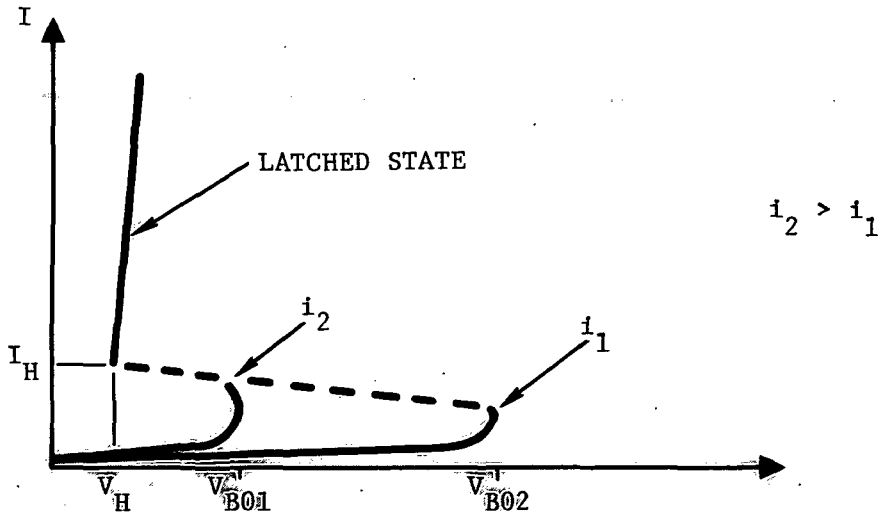


Figure V-17. Parasitic pnpn Diode

transistors. If an ion passes through the depletion region of either of these junctions, the current will be generated by the separation of electron-hole pairs in the presence of the strong electric field. The ion transit time and subsequent charge migration will occur on the order of picoseconds. For a conservative estimate, we assume that the charges are collected within 10^{-10} s. For the Ar and Kr ions used in the experiment, the stopping power resulted in a linear charge deposition rate from about 0.1 to 0.4 pC/μm. For a path length of a few microns, on the order of 1 pC of charge will be deposited within the time of approximately 10^{-10} s, giving a current transient of near 100 mA. From SCR characteristics, the ratio of On state current to the forward gate current required to switch the device On is rarely less than several thousand (ref. 6). Thus, it is conceivable that the current pulse from a single ion could trigger the SCR action of the pnpn path into the low impedance On state.

Based on the experimental data, one is led to the conclusion that latchup can be induced in the HM1-6508 from a single ion that has sufficient energy and stopping power to deposit the threshold energy in the sensitive region for latchup. With 150 MeV Kr ions incident at 0° with a flux of approximately 10^3 p/cm^2-s, the average fluence to latch was approximately 5000 p/cm^2. Thus, the cross-section of the sensitive region is on the order of 2×10^{-4} cm^2. The latchup occurs when sufficient photocurrent is generated within the sensitive region to trigger the regenerative action in a pnpn path. This photocurrent may be generated by one or more ions passing through the sensitive region. For the latchup to be induced by two ions, it is required that the two particles hit the same sensitive region (area target) within an overlapping time frame (time target) such that the photocurrent contributions are additive. Let us consider the probability for such an occurrence. Given that a particular sensitive region has been hit, we consider that region to be a target within area 2×10^{-4} cm^2. For the flux

of 10^3 p/cm^2-s, the probability of a second particle passing through a given area target within a second is

$$2 \times 10^{-4} \text{ cm}^2 \times 10^3 \text{ p/cm}^2 = 2 \times 10^{-1}$$

For the effects to be cumulative, the second particle must follow the first before the charges from the first encounter have recombined. The lifetime for the minority carriers is determined by the density of recombination centers. For typical silicon material used for transistors, the minority carrier lifetime is less than 10^{-6} s. For the photocurrent from a second particle to be additive to that of the first particle, the encounter must occur within 10^{-6} s. Assuming the particles to be randomly distributed in time, the probability of a particle occurring within a given 10^{-6} s time frame is 10^3 p/s $\times$ 10^{-6} s = 10^{-3}. Thus, the probability for a second particle encountering a given sensitive region of area 2×10^{-5} cm^2 within a particular time target of 10^{-6} s is

$$(2 \times 10^{-1}) \ (10^{-3}) = 2 \times 10^{-4}$$

Consequently, at the flux levels used in the experiment, a double encounter would be expected after $\frac{1}{2 \times 10^{-4}} = 5 \times 10^3$ s. It is not likely that any of the observed latchups were due to multiple ions.

The measured cross-section for latchup is seen to be on the order of 10^{-4} cm^2. The measured and calculated cross-section for bit error is on the order of 5×10^{-3} cm^2 or greater. Thus, the sensitive area for latchup is indicated to be approximately two orders-of-magnitude less than that for bit error. Based on highly speculative assumptions, the minimum charge deposition required to induce latchup is estimated to be about 0.3 pC, the same order as that for bit-error. With these assumptions, a rough estimate of the latchup rate in the TIROS-N environment could be as high as only two orders-of-magnitude less than the bit-error rate.

B. RCA CDP-1821

The RCA CDP-1821 CMOS RAM is organized as 1024 × 1 bit memory device and utilizes silicon gate technology on a sapphire substrate. The memory cells are organized as 6 transistor cells as shown in Figure V-18(a). Discussions with RCA representatives yielded the information that the silicon epi thickness is about 0.5 μm ± 10 percent. The maximum loss of silicon during processing was quoted to be 600 Å. Thus, the epi thickness is assumed to be 0.5 μm for the analysis.

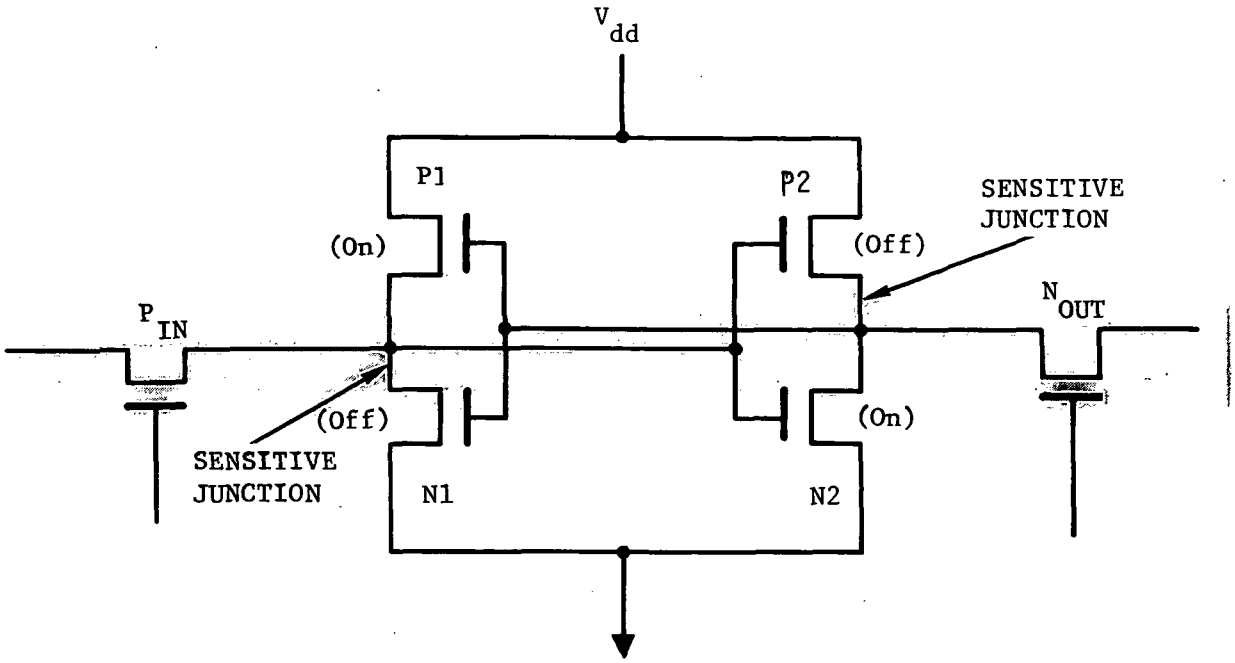
The sizes of the gate regions for the various transistors was determined from RCA representatives and are listed in Table V-3.

Table V-3. Transistor Sizes (L × W) for CDP-1821 (μm)

Transistor	L × W
N_1	5 × 15
P_1	5 × 25
N_2	5 × 5
P_2	10 × 5
P in	5 × 64
N out	5 × 64

For SOS technology, the transistors are confined to thin (approximately 0.5 μm) silicon islands on a sapphire substrate. Virtually none of the carriers that are created in the sapphire are collected before recombination, because of the lack of a strong field and to the low carrier mobility and lifetime in the sapphire. No significant number of carriers are collected from the gate insulator regions because of the thin region (≃ 0.1 μm) and the low carrier mobility and lifetime. Most of the ionized carriers in the drain depletion regions are collected. Some of the carriers in the region adjacent to the drain depletion regions may be collected.

(A) CIRCUIT SCHEMATIC



(B) CROSS-SECTION (SCHEMATIC) OF SENSITIVE TRANSISTORS

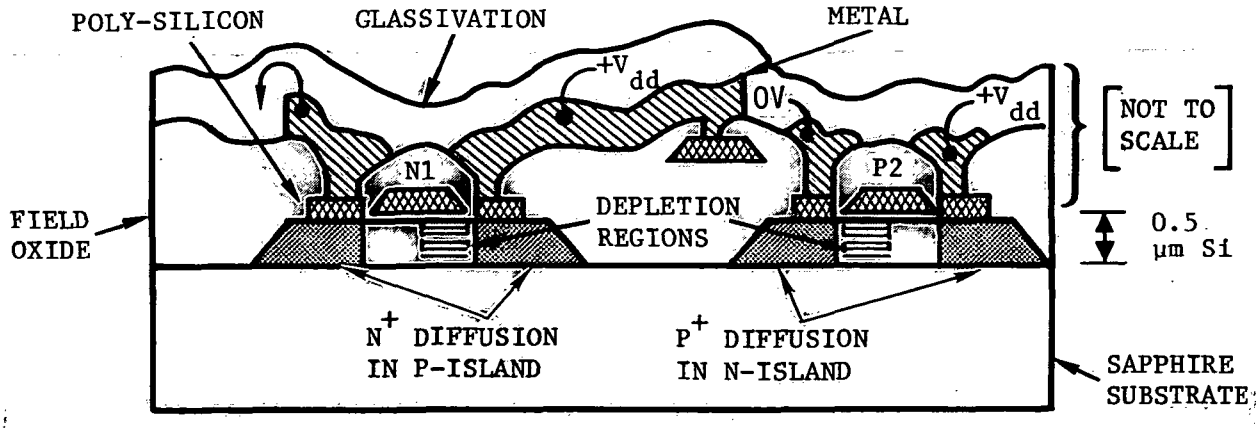


Figure V-18. CDP-1821 Memory Cell

Figure V-19 illustrates the various charge collection regions in a typical SOS N-channel transistor. For charge collected on the capacitance associated with the drain, region 1 is the depletion region and regions 3 and 4 are diffusion regions. Charge transfer through the depletion region 2 does not affect the charge in the drain capacitance. Charges recombine in regions 5. For typical SOS device parameters, diffusion region 4 may be neglected, and diffusion region 3 is taken to be the entire gate region for a conversative calculation.

Thus, for a conservative calculation, the sensitive region for a SOS transistor is taken to be the silicon under the gate area (regions 1, 2 and 3), which results in a parallelepiped with thickness equal to the epi thickness (usually approximately 0.5 μm) and a length and width that are determined by the gate dimension of the device.

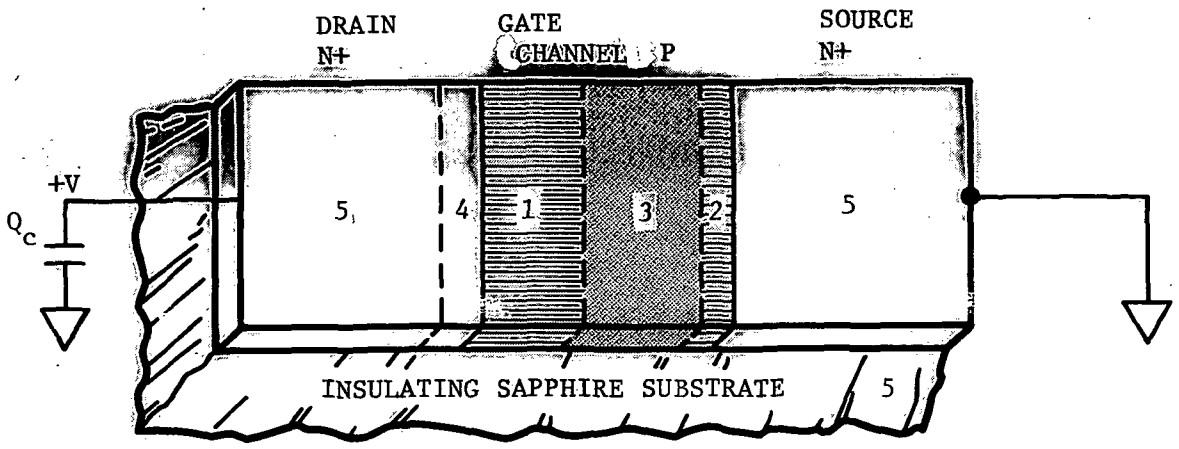
The sensitive transistors depend on the logic state of the cell. Those transistors that have a potential across a junction; that is, those devices which are turned "Off," can transfer charge if an ion passes through the depletion region.

We note that the sensitive transistors for one logic state is P1, N2 and for the other logic state is P2, N1. To be conservative, we consider P_{in} and N_{out} to be sensitive for both states at all times although this will not always be the case.

The CRIER code was used to calculate the error rate for each of the sensitive regions defined in Table V-3 (using h ≈ 0.5 μm, ie, the silicon epi layer thickness) for the TIROS environment model. The results are shown in Figure V-20 in terms of events per day for which charges greater than or equal to a given charge are deposited in a given sensitive parallelepiped volume vs critical charge. Since there are two possible states for the memory cell, we consider both equally likely and calculate the average error rate for a memory cell as

$$\overline{ER} \approx \tfrac{1}{2} \{[ER(N1) + ER(P2)] + [ER(N2) + ER(P1) + ER(PIN) + ER(NOUT)]\} \quad (5\text{-}3)$$

The result is shown as the dashed line of Figure V-20.



REGION 1* ELECTRONS SWEPT TO DRAIN,
HOLES SWEPT TO CHANNEL
REGION 2 ELECTRONS SWEPT TO SOURCE,
HOLES SWEPT TO CHANNEL
REGION 3* ELECTRONS MAY DIFFUSE TO DRAIN
REGION 4* HOLES MAY DIFFUSE TO CHANNEL
REGION 5 ELECTRONS AND HOLES RECOMBINE

*RESULTS IN CHARGE
DISTURBANCE ON DRAIN
CAPACITANCE

Figure V-19. SOS Transistor Charge Collection Regions

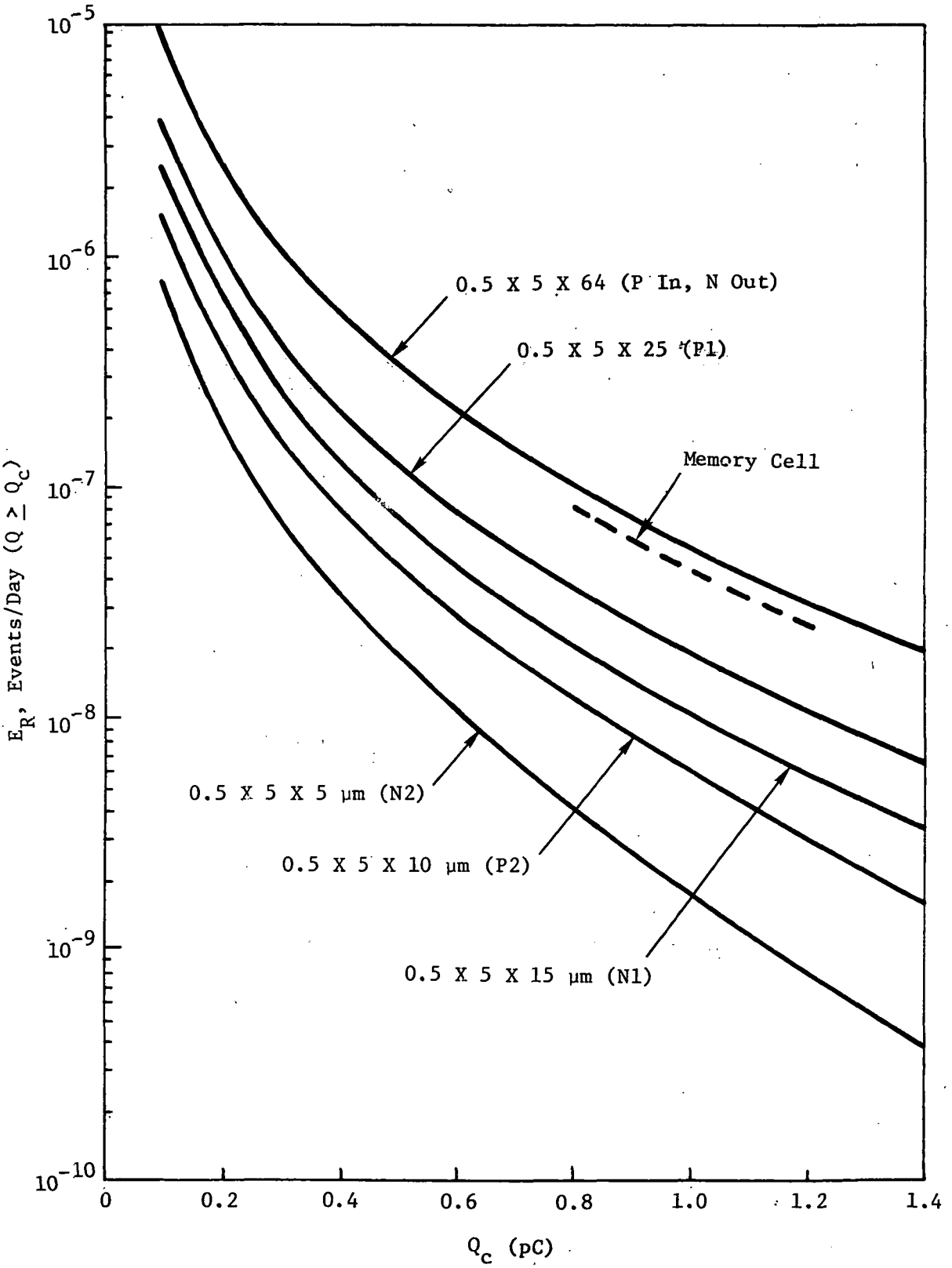


Figure V-20. Error Rate vs Critical Charge for CDP-1821 (TIROS Environment)

C. TIROS-N MISSION IMPACT

Estimates of the error rates for the memory cells (single bits) as a function of Q_c are shown in Figures V-15 and V-20 for the HM1-6508 and CDP-1821, respectively. From the experimental results, it is estimated that $Q_c \leq 0.3$ pC for the HM1-6508. Since the experimental results were limited for the CDP-1821, the results of previous work (ref 1) were also used to derive an estimate of $Q_c \geq 1$ pC. Based upon limited proton test results by other experimenters wherein no upsets were detected, it is estimated that the lower bound for Q_c is about 0.03pC. However, for the overall system analysis, it is assumed that $Q_c = 0.3$ pC for the HM1-6508 and 1 pC for the CDP-1821.

From the above critical charge assumptions, Figure V-15 and V-20 yield error rates of about 2.6×10^{-5} events/day for the HM1-6508 and 4.5×10^{-8} events/day for the CDP-1821 memory cells. Since each chip has 1024 bits of memory, the corresponding device bit error rates are 2.7×10^{-2} and 4.6×10^{-5} bit errors/day for the HM1-6508 and CDP-1821 devices respectively.

The overall TIROS-N mission impact from galactic-cosmic-ray-induced bit errors caused by the orbital environment presented in Section IV are derived from the above bit error rates. There are two 300 kilobit (300 device) memories in the TIROS-N satellite; only one is operational while the other is in a standby mode. It is assumed that each bit of the operational memory has an equal effect on the system. This leads to reasonable worstcase estimates of at least 8.0 bit errors/day (but probably no more than order of magnitude higher) for the HM1-6508 equipped system and less than 1.4×10^{-2} bit errors/day for a CDP-1821 equipped system. In terms of average time between bit errors, less than 3.0 hours for the HM1-6508 and more than 72 days for the CDP-1821. Meaningful error bars cannot be assigned to these data; however, with some confidence it is predicted that a system with the CDP-1821 should experience bit errors in orbit at least three orders-of magnitude less frequently than a similar system with the HM1-6508.

A quantitative estimate of single-particle-induced latchup in orbit can be made, in general terms only, for the HM1-6508; the frequency should be at least two orders-of-magnitude less than for bit errors. The experimental data indicate that the latchup energy threshold is of the same order; however, the cross-section is much less than for bit errors. Both the experimental data and device design lead to the estimate that the CDP-1821 will never experience latchup. Therefore, it is considered that while an HM1-6508-equipped system could experience latchup in orbit, a CDP-1821-equipped system would not.

VI. CONCLUSIONS

The experimental results, available data on the characteristics of the devices, and the CRIER model with the defined TIROS-N environment provided for an adequate comparison of TIROS systems in orbit equipped with the Harris HM1-6508 and RCA CDP-1821 1 × 1024 bit RAM memories.

The resulting comparative bit error rates in orbit for the TIROS-N system are at least 8.0 bit errors/day (and no more than a factor of ten higher) for the HM1-6508 and less than 1.4×10^{-2} bit errors/day for the CDP-1821.

The HM1-6508-equipped TIROS-N system has an expected latchup rate of at least two orders-of-magnitude less than its error rate while the CDP-1821 will never experience latchup.

This study does not address the effect of total dose on the devices and in particular the possible synergistic effect of threshold shift on cosmic-ray-induced bit error rate.

VII. RECOMMENDATIONS

The TIROS-N system should not use the Harris HM1-6508 without taking extensive corrective measures to reduce the effects of bit errors and latchup to an acceptable level.

The RCA CDP-1821, or its equivalent, should be considered the preferred memory device for the TIROS-N system, recognizing the non-zero probability of bit errors.

Experimental studies should be performed to determine the dependence of the cosmic-ray-induced bit error rate on total ionizing dose.

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APPENDIX A

HEAVY ION TEST DATA

DATA SHEET

Part Type: HM 1-6508 Set No. 1-3

Beam: $^{86}Kr^{+10}$, E_o = 170 MeV Date: 6-9-80 Start: 7:45PM

Set/Run No.	Spacer Part No.	Beam Angle (degrees)	Particle Count	Errors/ Latch	Angle Corr. Fluence (p/cm²)	ErrorRate (E/p-cm⁻²)	Beam Energy at Chip (MeV)	Remarks	
1- 1	54/166	0	22,857	Many/L	12,741	Latch	152	V_{DD} = 5V	*
2	"	0	3,114	Many/L	1,736	Latch	"	↓	
3	"	0	408	Many/L	227	Latch	"		
4	"	0	1150	0	641	0	40		
5	"	0	~3000	0	~1670	0	"		
6	"	0	14,293	3	7967	1.26×10^{-4}	"		
7	"	0	11,955	1	6664	1.50×10^{-4}	"		
8	"	0	12,707	0	7083	0	"		
9	"	0	44,048	1	24,553	4.07×10^{-5}	"		
10	"	0	88,210	9	49,169	1.83×10^{-4}	"		
11	"	0	204,623	15	114,060	1.32×10^{-4}	"		
12	"	0	423,721	35	236,188	1.48×10^{-4}	"		
13	55/167	0	178,898	39	99,720	3.91×10^{-4}	"		
14	"	0	290,041	63	161,673	3.90×10^{-4}	"		
15	56/168	0	335,068	Many	186,771	High	"	Doubles, Too many errors	
16	"	0	113,969	78	63,528	1.23×10^{-3}	"		
17	57/169	0	6869	0	3829	0	"		
18	"	0	48,515	1	27,043	3.70×10^{-5}	"		
19	"	0	457,743	19	255,152	7.45×10^{-5}	"		
20	"	0	461,023	22	256,980	8.56×10^{-5}	"		
2- 21	54/166	0	87,523	0	48,787	0	20		
22	"	0	715,432	0	398,792	0	"		
23	"	0	1,792,081	0	998,930	0	"		
24	55/167	0	1,202,380	0	670,223	0	"		
25	56/168	0	1,809,726	0	1,008,766	0	"		
26	54/166	60	1,199,965	0	334,438	0	"		
27	56/168	60	825,151	0	229,975	0	"		
3- 28	54/166	60	67,983	1	18,947	5.28×10^{-5}	32		
29	"	60	1,047,443	5	291,929	1.71×10^{-5}	"		
30	55/167	60	46,064	2	12,838	1.56×10^{-4}	"		
31	"	60	2,252,616	22	627,819	3.50×10^{-5}	"	Double flip	
32	56/168	60	1,003,929	33	279,802	1.18×10^{-4}	"		
33	57/169	60	7.49×10^{6}	5	2.09×10^{6}	2.40×10^{-6}	"		

* NOTE: V_{DD} = +5V, Runs 1-33.

83

FORM 40-Z REV. 12-84

DATA SHEET

Part Type: CDP-1821 Set No. 4-5

Beam: $^{86}Kr^{+10}$, $E_0 = 170$ MeV Date: 6-9-82 Start: 10:30PM

Set/Run No.	Spacer/ Part No.	Beam Angle (degrees)	Particle Count	Errors/ Latch	Angle Corr. Fluence (p/cm²)	Error Rate (E/p-cm²)	Beam Energy at Chip (MeV)	Remarks V_{pp}	
4 – 1	S4/15308	60	5×10^6	0	1.4×10^5	0	152	+5V	
2	S4/15308	75	5×10^6	0	7.2×10^5	0	152	+2V	
3	S5/15311	75	$\sim2\times10^6$	0	2.9×10^5	0	152	+5V	
4	S5/15311	75	$\sim2\times10^6$	3	2.9×10^5	1.0×10^{-5}	152	+2V	
5	S6/15315	75	1×10^6	0	1.4×10^5	0	152	+5V	
6	S6/15315	75	1×10^6	0	1.4×10^5	0	152	+3.5V	
7	S6/15315	75	1×10^6	0	1.4×10^5	0	152	+2V	
8	S7/15319	75	1×10^6	0	1.4×10^5	0	152	+5V	
9	S7/15319	75	1×10^6	0	1.4×10^5	0	152	+3.5V	
10	S7/15319	75	1×10^6	0	1.4×10^5	0	152	+2V	
5 – 1	S4/314	75	—0—	—	—	—	152	+5V Not Functional	
2	S5/326	75	4.3×10^6	1	6.2×10^5	1.6×10^{-6}	152	+5V	
3	S5/326	75	3.9×10^6	0	5.6×10^5	0	152	+5V	
4	S6/184	75	1.5×10^6	0	2.2×10^5	0	152	+5V	
5	S7/14983	75	2×10^6	0	2.9×10^5	0	152	+5V	
6	S7/14983	75	4×10^6	0	5.8×10^5	0	152	+10V (Standby)	
7	S7/14983	75	2×10^6	2	2.9×10^5	6.9×10^{-6}	152	+2V	

84

FORM 40-Z REV. 12-64

DATA SHEET

Part Type: HM1-6508 Set No. 6

Beam: $86Kr^{+10}$, E_a = 170 MeV Date: 6-10-80 Start: 12:06 AM

Set/ Run No.	Spacer/ Part No.	Beam Angle (degrees)	Particle Count	Errors/ Latch	Angle Color Fluence (p/cm²)	Error Rate (E/p-cm⁻²)	Beam Energy at Chip (MeV)	Remarks	
6 - 1	54/171	0	5333	51/Latch	2973	1.7×10^{-2}	152	Latch after	2nd turnon
2	54/171		8376	Latch	4669	—			
3	55/185		21,136	"	11,781	—			
4	56/186		2306	"	1285	—			
5	57/188		3387	"	1888	—			
6			1126	Hundreds	—	High			
7			923	"	—	High			
8			1464	"/Latch	1958	—			
9			4700	Latch	2620	—			
10			7423	"	4138	—			
11			3377	"	1882	—			
12			1825	"	1017	—			
13			1205	"	672	—			
14			6866	"	3827	—			
15			1959	"	1092	—			
16	↓	↓	1231	"	686	—	↓		

(85)

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DATA SHEET

Part Type: HM1-6508 Set No. 7

Beam: $^{40}Ar^{+8}$ $E_o = 224$ MeV Date: 6-13-80 Start: 4:50 AM

Set/Run No.	Spacer/ Part No.	Beam Angle (degrees)	Particle Count	Errors/ Latch	Angle Corr. Fluence (p/cm²)	Error Rate (E/p-cm⁻²)	Beam Energy at Cliff (MeV)	V_{DD}	Remarks
7- 1	54/186	0	31,458	38	17,535	2.17×10^{-3}	210	+5V	
2	"		44,292	83	24,689	3.36×10^{-3}			2 double flips
3	"		151,448	Latch	84,419	—			many " "
4	"		126,694	Latch	70,621	—			
5	55/188		28,785	Latch	16,045	—			
6	"		15,870	Latch	8846	—			
7	56/255		6320	31	3523	8.80×10^{-3}			
8	"		10,598	Latch	5907	—			
9	"		38,839	Latch	21,649	—			
10	57/322		36,603	Latch	20,403	—			
11	"		31,913	Latch	17,789	—			
12	Collimator		—	—	—	—	26		
13	"		—	—	—	—	7		
14	54/186		733,195	0	408,693	0	7	+5.5V	
15	"	65	740,660	0	174,480	0	7		
16	"		1,000,799	0	235,809	0	~15		
17	—		—	—	—	—	~15	+4.5V	Wrong Channel
18	54/186		897,240	0	228,858	0	24		
19	"	0	971,495	0	1.06×10^{6}	0	24		
20	55/188		1,903,034	483	9.21×10^{5}	5.24×10^{-4}	67	+5V (1.6 mA)	
21	"		1,715,770	Many	9.56×10^{5}	High	67		
22	Collimator		—	—	—	—	67		
23	"		—	—	—	—	52		
24	57/322		2,608,436	Hundreds	1.45×10^{6}	High	52		
25	54/186		679,364	0	3.79×10^{5}	0	34		
26	"		1,000,000	0	5.57×10^{5}	0	34		
27	Collimator		—	—	—	—	34		
28	"		—	—	—	—	55		
29	"		—	—	—	—	53		
30	"		—	—	—	—	45		
31	54/186		732,606	9	4.08×10^{5}	2.21×10^{-5}	45		Slotted Plate Pulled
32	"		745,123	10	4.15×10^{5}	2.41×10^{-5}	45		
33	"	60	225,259	45	62,781	7.17×10^{-4}	45		
34	55/188	0	231,060	Hundreds	1.29×10^{5}	High	45		Many double flips
35	56/255	0	43,440	23	24,214	9.50×10^{-9}	45		
36	56/255	0	59,206	39	33,002	1.18×10^{-3}	45		
37	57/322	0	63,310	12	35,290	3.40×10^{-4}	41		
38	56/255	0	172,482	32	96,144	3.33×10^{-9}	41		

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DATA SHEET

Part Type: HM1-6508 Set No. 8,9

Beam: $^{40}Ar^{+8}$ $E_0 = 224$ MeV Date: 6-13-80 Start: ~7AM

Set/Run No.	Spacer/ Part No.	Beam Angle (degrees)	Particle Count	Errors/ Latch	Angle corr Fluence (p/cm²)	Error Rate (E/p-cm⁻²)	Beam Energy at Chip (MeV)	V_{DD}	Remarks
8-1	54/169	0	135,594	11	75,582	1.46×10^{-4}	41	+5V	
2	"	60	55832	21	15,561	1.35×10^{-3}			
3	55/166	0	92,033	20	51,300	3.90×10^{-4}			
4	56/171	0	208,281	0	116,099	0			
5	"	60	174,535	16	48,644	3.29×10^{-4}			
6	57/170	0	546,699	7	304,737	2.30×10^{-5}			
7	"	0	205,718	2	114,670	1.74×10^{-5}	212		
8	"	0	434,943	3	242,443	1.24×10^{-5}			
9	"	60	26,541	Latch	7397	—			
10	"	60	—	—	—	—			Beam Out
11	"	60	11,326	~80/Latch	3714	$\sim2.2\times10^{-2}$			
12	54/169	60	2090	Latch	582	—			
13	"	0	71,226	>250	39,702	$>6.3\times10^{-3}$			Double Flips
14	"	45	21,699	>150/Latch	8553	$>1.8\times10^{-2}$			
9-1	54/259	0	1352	9	754	1.19×10^{-2}	41		
2	55/185	0	16,350	7	9114	7.68×10^{-4}			
3	56/265	0	4922	14	2744	5.10×10^{-3}			
4	57/174	0	6075	20	3386	5.91×10^{-3}			
5	"	0	74,419	>210	41,482	$>5.1\times10^{-3}$	212		Double Flips
6	"	45	9286	~100/Latch	3660	$\sim2.7\times10^{-2}$			
7	55/185	45	22,834	~34/Latch	9000	$\sim3.8\times10^{-3}$			

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APPENDIX B
COSMIC-RAY-INDUCED ERROR RATE MODEL

A. INTRODUCTION

The prediction of the cosmic-ray-induced error rate in space requires an analytical model. The data obtained from simulation experiments cannot be applied directly to predict the space error rate. The space environment of concern consists of various heavy ion particles with a spectrum of energies and stopping powers incident on the semiconductor chip from all angles. However, a simulation such as the cyclotron experiments must necessarily use a limited number of ion species and a few discrete energies. Also, the testing of packaged devices (delidded) limits the angle of incidence for the particles on the chip.

This appendix describes an analytical model for predicting the error rate in MOS digital circuitry operated in the galactic cosmic ray environment of space. The modeling approach is applicable to both memory devices and digital logic circuits. The physical mechanism of "soft" error production in semiconductor devices will be reviewed, followed by a detailed description of the environment modeling, consideration for determining the amount of charge required to cause error, description of the sensitive regions in various device technologies, determination of the path length distribution through the sensitive regions, and the error rate calculation.

B. MECHANISM

Semiconductor digital circuits process binary data as the presence or absence of charge on particular nodes of the device. Both memory devices such as RAMs and digital devices, such as shift registers or counters, may have similar response to the cosmic ray ionization since the interaction time is short compared to clock frequencies. The quantity of charge which differentiates between a binary "1" and "0" is defined as the critical charge, Q_c. The critical charge is determined by total node capacitance, threshold voltages of associated transistors, and circuit sensitivity as determined by RC time constants. The basic mechanism for ionization-induced bit errors is the neutralization of the critical bit charge by the collection of ionization induced electrons or holes at the node.

The resultant effect of all ionizing radiation is the creation of free electron-hole pairs along the path of a charged particle through the material. The charged particles may be electrons (either as primary radiation or secondary radiation from photon interaction), protons, alpha particles, or higher atomic number ions. The heavy ions penetrate through the semiconductor in generally straight line paths. Coulombic interactions with the orbital electrons result in energy transfer to a spectrum of secondary electrons traveling in random directions. These secondary electrons spread from the original ion path for a distance of up to a few microns, losing energy by ionization of the semiconductor material. The result is a cylindrically shaped path of ionization through the crystal with an intense core of heavy ionization that varies approximately as $1/r^2$ with distance away from the core. This process is very fast, being on the order of picoseconds, and may be treated as an instantaneous deposition of energy, and corresponding charge, along the path traveled by the ion.

Electrons and holes that are raised to the conduction band within depletion regions surrounding diffusions or within gate insulators will be separated by the high electric field. Electrons are swept to the positive potential, and holes are swept to the negative potential.

Electrons and holes generated outside the depletion region diffuse through the bulk silicon. Those reaching the edge of the depletion region are swept into the storage region.

To cause a bit error, the charged particle must deposit sufficient energy in the sensitive region of a node, or within a diffusion length of it, to generate the required charge. As the heavy ions pass through the material, they deposit energy along their paths in accordance with an energy loss rate or stopping power, dE/dx. This stopping power is a function of particle type, energy, and material through which it is passing. The ionization-induced charge can be related to the deposited energy by use of the ionization rate in

silicon of 3.6 eV/carrier pair. Specifically, the charge may be calculated by

$$Q \text{ (picocoulombs)} = \frac{f\ E\ (MeV)}{22.5} \qquad \text{(B-1)}$$

where f is a collection efficiency and assumed to be 1 in a depletion region.

For typical diffusions or gate dimensions (a few microns) and typical critical charges (sub-picocoulomb), it may be observed that stopping powers on the order of a few MeV/μm are required to deposit the critical charge in the small path lengths. These requirements restrict the ionizing particle choices to high energy (several MeV and above) and high atomic number (Z > 2). In the natural environment, only the exoatmospheric cosmic rays contain significant quantities of particles which meet these requirements.

C. ENVIRONMENT

Galactic cosmic ray ions incident on the TIROS spacecraft in orbit are predominately protons (hydrogen ions) with lesser components of other relativistic particles, all having energies extending indefinitely upward (within the state-of-the-art measurement capability). The alpha particle (helium ion) flux is about an order of magnitude less, while the combined flux of all of the other ions is down about another order again*.

The particle fluxes of specific interest for this analysis are at any surface of the memory chip under study. These data and their limitations, as provided by E. G. Stassinopoulos for this study, are reproduced in Table IV-1. Within the scope of the specified limitations in Table IV-1, the fluxes listed were reduced by a factor of two for this study, and the undefined effects of solar activity were neglected.

Based on a telephone discussion with E. G. Stassinopoulos, two assumptions were made to adapt the data in Table IV-1 to this study. First, the spectral distribution of each ion was assumed to be flat from 0.3 to 15 MeV/n (MeV/nucleon); the actual spectral distribution is unknown; however,

*L. C. Northcliffe and R. F. Schilling, Nuclear Data A7, Academic Press, 1970.

this is considered a reasonable estimate. The second assumption extends the fluxes beyond the 15 MeV/n upper limits of Table B-1; this was done primarily to accommodate the long pathlengths associated with the CDP-1821 sensitive regions (64 μm maximum). For example, a 400 MeV/n iron particle could deposit enough energy in this pathlength for 1 pC of charge, the approximate bit upset threshold. The extension to the differential spectrum derived from Table IV-1, as indicated above, is a simple power law with exponent -2 to approximate the galactic cosmic ray heavy ion spectra.

Previous work* found the Linear Energy Transfer (LET) spectrum was much more useful than other techniques for expressing the galactic cosmic ray environment in analyses of its effect on MOS circuits. It assumed that the only aspect of significance for any particle was the rate of energy deposition (dE/dx) or LET. Later, it will be shown that the total energy of a particle can also have a significant impact; therefore, the technique has been modified in its application to the environment described above.

The ultimate goal of the environment part of the analysis was to develop the TIROS-N model of a linear charge deposition spectrum to be used with the pathlength distribution and device parameters to determine the expected bit error rates in orbit. The methodology used in the development of this model will be described in the following paragraphs. It should be noted that the work was done manually with the indispensable aid of a programmable calculator to test the sensitivities of the various approaches to the development. There was insufficient time to refine the environment model through programming the various steps on a computer; however, the uncertainty associated with the environment does not really warrant this added sophistication.

Initially, the particle counts provided in Table IV-1, reduced by a factor of 2 as discussed earlier, were divided equally among five bins for

*J. C. Pickel and J. T. Blandford, Jr., IEEE Trans. Nucl. Sci., NS-25, No. 6, Dec. 1978, pp. 1166-1171

Table B-1. Attenuated Cosmic Ray Fluxes of Galactic Origin

Evaluated for a shield thickness (range) of 70 mils Al, at the delidded device level.

Z	Ion	Flux (#/cm^2 day) E(out) = 15 MeV/n
1	H	8933.35
2	He	2324.07
3	Li	5.90
4	Be	2.69
5	B	12.49
6	C	50.00
7	N	11.57
8	O	46.81
9	F	1.16
10	Ne	6.94
11	Na	1.71
12	Mg	9.01
13	Al	1.61
14	Si	6.29
15	P	0.25
16	S	1.03
17	Cl	0.23
18	Ar	0.42
19	K	0.34
20	Ca	0.87
21	Sc	0.20
22	Si	0.73
23	V	0.39
24	Cr	0.74
25	Mn	0.49
26	Fe	4.12

Note: Table is for maximized exposure (deepest penetration into magnetosphere), using E (out) = 15 MeV/n.

Variations in background (on account of solar activity) may be as large as a factor of 20; since flux values used were maxima, any adjustment factor should be leading to lower values only.

Fluxes should be reduced by about a factor of 2 (at least) because omnidirectional incidence has been assumed, which is not the case near the earth (1000 km altitude) at high latitude and polar regions.

Cosmic rays of solar origin ray occasionally exceed the galactic background by factors of 10^3 to 10^5 (for major flare events).

(Source: E. G. Stassinopoulos, NASA-GSFC, 1980)

each ion with Z from 3 to 26 (lithium through iron) and 50 bins each for hydrogen and helium. Each of these bins was then assigned a nominal stopping power based on the Northcliffe and Schilling data*. The ion fluxes for each of these 220 bins were then listed in order of decreasing stopping power from the maximum (for iron: 26.9 MeV-cm^2/mg) to 0.1 MeV-cm^2/mg, which is about an order-of-magnitude below the expected minimum value of interest for this study. The fluxes were then cumulated in descending order for the preliminary LET-spectrum. This spectrum was then transformed to a linear charge deposition spectrum assuming the ionization rate in silicon is 3.6 eV/carrier pair, 6.24×10^{18} electrons/coulomb, and the density of silicon is 2.33 gm/cm^3 (0.233 mg-cm^{-2}/μm).

The next step in the development of the model was to incorporate the extension beyond the 15 MeV/n upper limit. The technique was similar, except for some simplification based on the earlier results. A total of 19 energy bins were used between 15 and 1000 MeV/n (maximum) with the widths increased in steps in view of the rapidly decreasing differential flux and stopping power contributions. The ion types were divided into nine groups somewhat arbitrarily based on considering the size of the bin fluxes and similarities in stopping power. As before, nominal stopping powers were assigned to each bin down to the 0.1 MeV-cm^2/mg cutoff; then the bin fluxes were ordered by decreasing stopping power and cumulated as before. These data were changed to a linear charge deposition spectrum and combined with the one for 0.3-15 MeV/n. The resulting linear charge deposition spectrum is the highest-valued one shown in Figure B-1; it includes all the particles within the charge deposition range indicated.

It become apparent in the course of the analysis that even through some of the particles had the stopping power to lead to a bit upset, they lacked the required kinetic energy. For example, if a device bit upset threshold were 1 pC, at least a 22.5 MeV ion energy would be required. In terms of particle energies per nucleon in this case, for example, the

*S. B. Curtis and M. C. Wilkinson, NASA TM X-2440, Jan. 1972, pp. 1007-1014

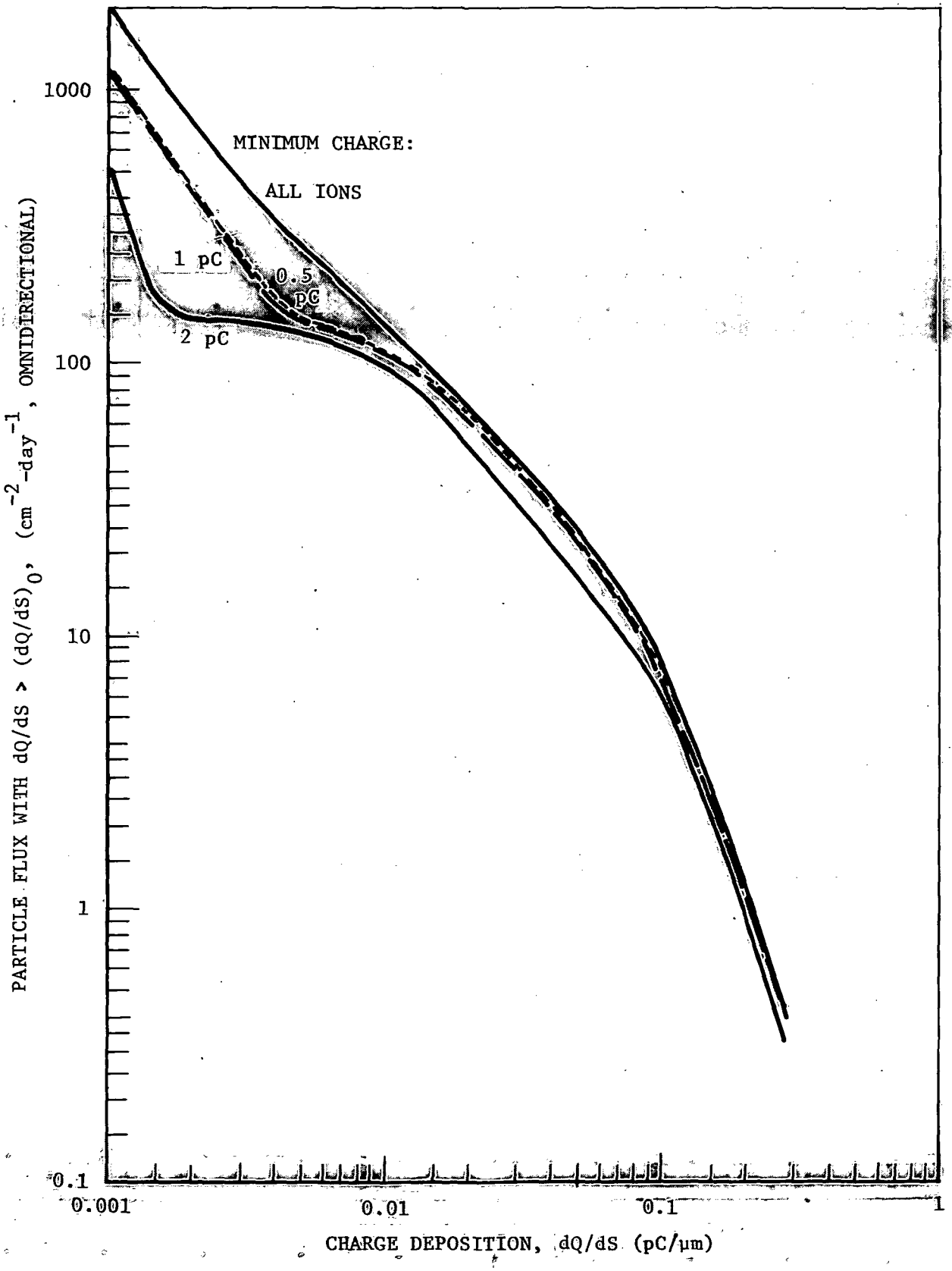


Figure B-1. Linear Charge Deposition Spectra

minimum cutoff energies range from 22.5 MeV/n for the hydrogen ion to 0.4 MeV/n for the iron ion.

The effects of eliminating ions with charge depositions with less than 0.5, 1, and 2 pC are shown in Figure B-1. Within the limits of potential concern to this study, 0.01 to 0.28 pC/μm, the differences are small compared with the uncertainties associated with the environment.

The actual TIROS-N Model Linear Charge Deposition Spectrum from the algorithm used in computer analyses of the devices is shown in Figure B-2 as the "Extended Spectrum." The dots shown in the vicinity of this curve are selected data points for the 0.5 and 1 pC spectra of Figure B-1. The corresponding curve for the Table IV-1 ($\leq$15 MeV/n) data is also shown for comparison; the differences (in the 0.01 to 0.28 pC region of concern) are significant but they probably would not adversely bias the end results of the analysis substantially.

D. MINIMUM CHARGE

Before the error rate for a particular node of a circuit can be calculated it is required that the minimum charge necessary for causing error be determined. The amount of charge present at a node is predominantly determined by the total capacitance of the node and the voltage at the time of the cosmic ray interaction. Capacitance is determined by gate dimensions and stray capacitance caused by overlap regions. The voltage is either V_{dd} or ground for static designs and is a function of time since refresh for dynamic designs.

The amount of charge disturbance required for bit error is determined by the threshold voltage of transistors associated with the node and by the RC time constants of the associated circuits. For example, in a bistable flip-flop, a bit error may occur if the cosmic ray introduces enough charge disturbance to cause "On" transistors to turn "Off" and the supply voltages cannot recharge, due to RC restraints, before the flip-flop regenerates to the other state.

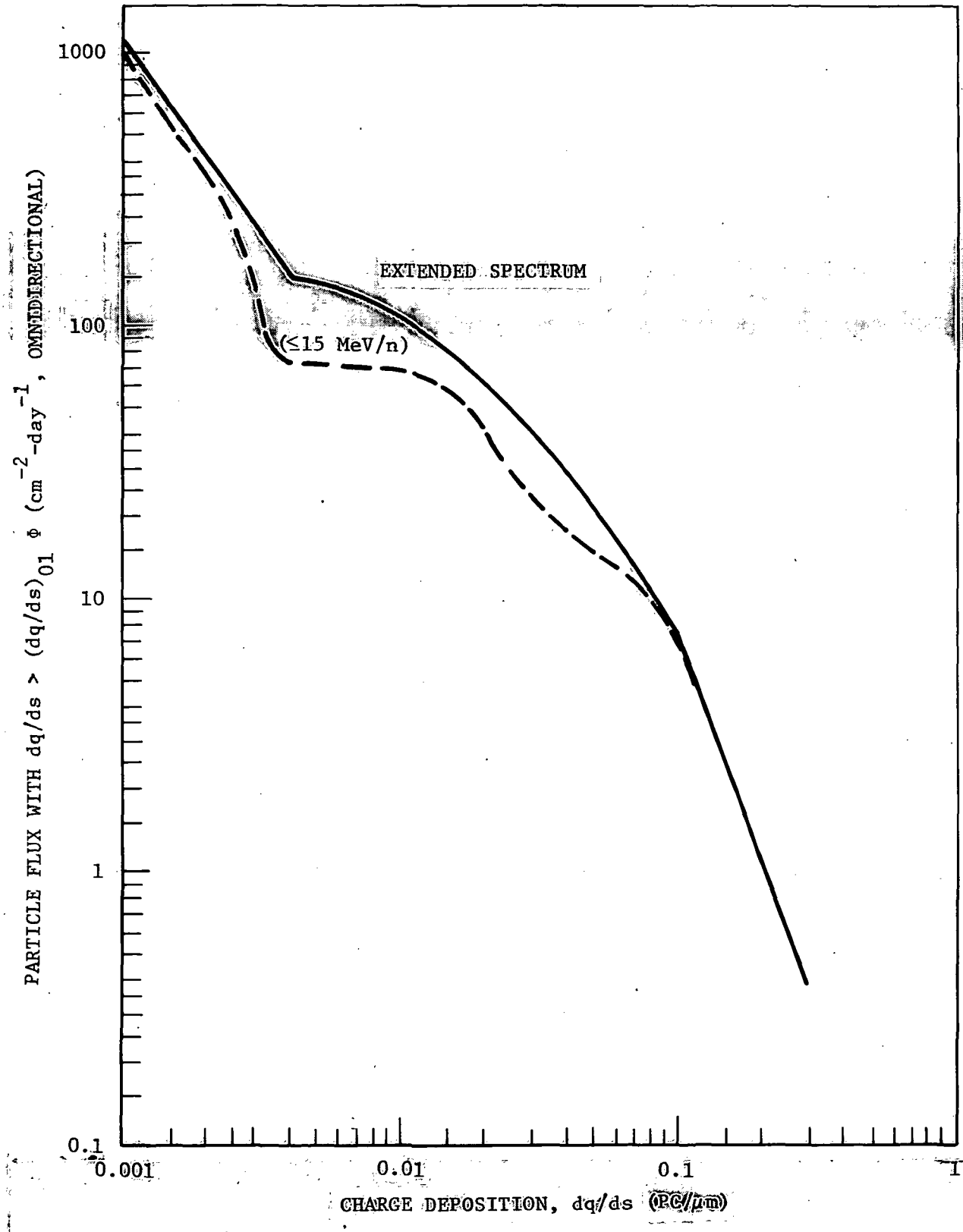


Figure B-2. TIROS-N Model Linear Charge Deposition Spectrum

The determination of minimum charge to cause error can be done analytically or experimentally. The analytical determination can be performed by computer simulation using the TRACAP transient response model. The cosmic ray effect is simulated by applying a pulsed current source at various nodes. The experimental determination can be made at a cyclotron, for example, by finding the minimum angle of incidence of the ions required for upset. By knowing the thickness of the sensitive region, t, the minimum path length to cause error is determined by

$$S_{min} = \frac{t}{\cos \theta_{min}} \tag{B-2}$$

The critical charge is then given by

$$Q_c = S_{min} \left(\frac{dQ}{dS}\right) \tag{B-3}$$

where $\frac{dQ}{dS}$ is in units of pC/μm.

For devices which have errors for ions incident normally, no minimum angle can be determined and it is required to vary the stopping power of the incident ion, either by changing energy or type of ion.

E. SENSITIVE REGIONS

For any particular node in the logic or memory circuit, the associated sensitive regions are those p-n junctions that have a voltage across them. Normally, this voltage drop will be the V_{dd} potential. For example, in the CMOS flip-flop element shown in Figure B-3, if the logic state is such that node A is biased at + V_{dd} and node B is at ground, the drain junctions of N1 and P2 are sensitive regions. Any ionization in these depletion regions will transfer charge to the affected node. For ionization in the junction of N1, electrons will be collected resulting in a negative voltage spike at node A. For ionization in the junction of P2, holes will be collected resulting in a positive voltage spike at node B. If the voltage spikes are of sufficient amplitude and charge neutrality cannot be achieved through the "On" transistor fast enough, the flip-flop may regenerate and a bit error will occur.

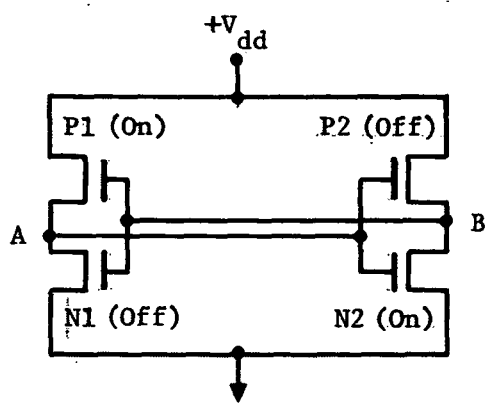


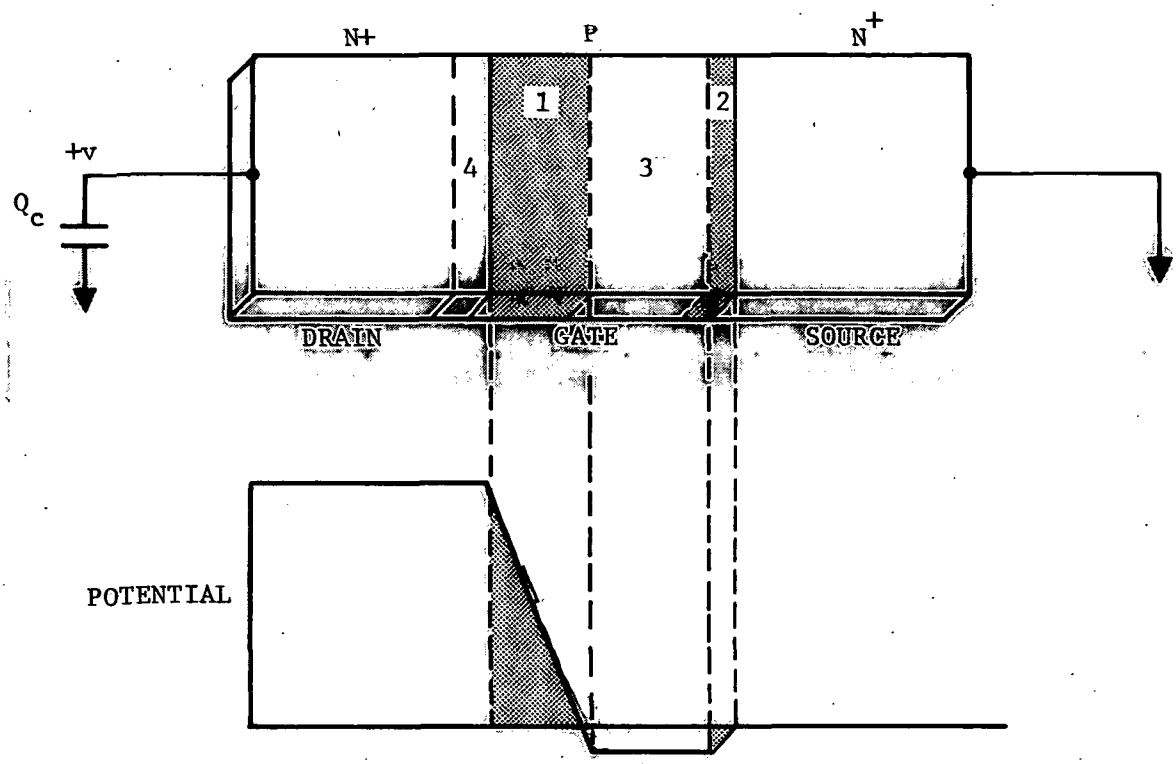
Figure B-3. CMOS Flip-Flop

For ionization within the depletion region, it is assumed that all of the induced charge is collected. For ionization in regions within a diffusion length of the depletion regions, the carriers may be collected if they diffuse to the edge of the depleted region.

For SOS technology, the transistors are confined to thin (approximately 0.5 μm) silicon islands on an insulating sapphire substrate. Virtually none of the carriers that are created in the sapphire are collected before recombination due to the lack of a strong field and the low carrier mobility and lifetime in the sapphire. Most of the ionized carriers in the drain depletion regions are collected. Some of the carriers in the region surrounding the drain depletion region may be collected.

Figure B-4 illustrates the various charge collection regions in a typical SOS transistor. For charge collected on the capacitance associated with the drain, region 1 is the depletion region and regions 3 and 4 are diffusion regions.

Also shown on Figure B-4 is the potential variation across the device and the energy band diagram. For typical SOS device parameters, the diffusion region 4 may be neglected and the diffusion region 3 is taken to be the entire gate region for a conservative calculation.



REGION 1. ELECTRONS SWEPT TO DRAIN
HOLES SWEPT TO CHANNEL
REGION 2. ELECTRONS SWEPT TO SOURCE
HOLES SWEPT TO CHANNEL
REGION 3. ELECTRONS DIFFUSE TO DRAIN
REGION 4. HOLES DIFFUSE TO CHANNEL

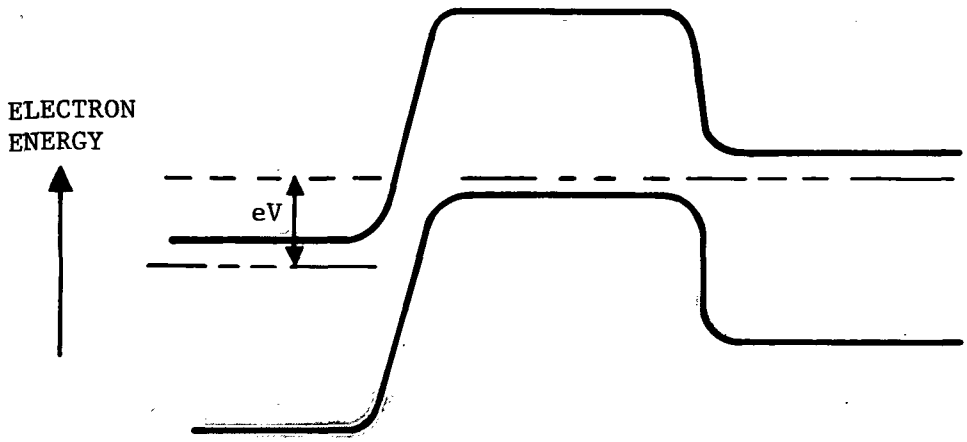


Figure B-4. Charge Collection Regions in SOS Transistor

Thus, the sensitive region for an SOS transistor is taken to be the silicon under the gate area which results in a parallelepiped with thickness equal to the epi thickness (usually approximately 0.5 μm) and a length and width determined by the gate dimension of the device.

F. PATH LENGTH DISTRIBUTION

Since heavy ion particles in space are in an omnidirectional flux, the semiconductor chip will have particles passing through from all directions. It is necessary to consider the distribution of path lengths through a sensitive region to calculate the error rate. A path length distribution function has been derived exactly for a parallelepiped in an omnidirectional flux by M. D. Petroff*. The distribution of path lengths, S, for an omnidirectional flux is derived as the function f(s). The f(s) function is normalized as follows:

$$\int_0^{S_{max}} f(s)\, ds = 1 \qquad \text{(B-4)}$$

Where S_{max} is the maximum path length through the parallelepiped. The key use of the distribution function in the error rate model is to determine the fraction of the average projected area of the sensitive region for which path lengths are between given limits s1 and s2. That is

$$\overline{A}_p \int_{s1}^{s2} f(s)\, ds = \text{fraction of } A_p \qquad \text{(B-5)}$$

$$\text{for which } s1 \leq s \leq s2.$$

G. ERROR RATE CALCULATION

To calculate the error rate, the environment model of Section C is used with the path length distribution of Section F. The sensitive region

*C78-572/201, "SPIRE Program Radiation Transport (SPURT) User's Manual," Rockwell International, May, 1978

for a particular junction is determined as discussed in Section E as a parallelepiped of the dimensions 1, w, and h. The minimum charge, Q_c, is determined as discussed in Section D.

The maximum path length through the sensitive region is given by

$$S_{max} = \sqrt{1^2 + w^2 + h^2}. \tag{B-6}$$

The minimum path length for consideration is that minimum path length for which a particle can deposit the required charge Q_c. This is related to the ion stopping power, in terms of charge deposition rate, pC/μm, by

$$S_{min} = \frac{Q_c}{\left(\frac{\Delta Q}{\Delta S}\right)_{Max}} \tag{B-7}$$

where $$\left(\frac{\Delta Q}{\Delta S}\right)_{max} = 0.28 \text{ pC/}\mu\text{m} \tag{B-8}$$

is the maximum stopping power for any particle in the space environment and is caused by iron particles at 90 MeV. The error rate for a given parallelepiped of dimensions 1, w, h is then given by

$$E_R = \overline{A}_p \int_{S_{min}}^{S_{max}} \phi\ (s)\ f(s)\ ds \tag{B-9}$$

where $\overline{A}_p = \frac{1}{2}\ (1w + wh + h1)$

and is the average projected area of the parallelepiped,

$\phi\ (s)$ = flux for which $\frac{\Delta Q}{\Delta S} \geq \frac{Q_c}{S}$

and is the integral stopping power spectrum derived from the environment model, and

f(s) = distribution of path lengths through parallelepiped of dimensions l, w, h.

For practical solution, the problem is solved numerically by dividing the path length distribution into small bins f_i. The error rate is then determined by

$$E_R = \sum_i \phi_i \, f_i \, \overline{A}_p \qquad \text{(B-10)}$$

where $f_i \, \overline{A}_p$ = fraction of $\overline{A}_p$ for which $S_i \leq S \leq S_i + \Delta S$

and $\overline{\phi}_i$ = number of particle/cm^2-day for which $\frac{\Delta Q}{\Delta S} \geq \frac{Q_c}{S_i}$.

A Fortran program has been written (CRIER) which solves a typical case for minimal computer time. The program has also been coded in "BASIC" and can be operated using a microcomputer. The program takes the geometry of the sensitive region in terms of l, w, and h as an input. The output is error rate (events/day for which charges greater than or equal to Q_c are deposited) vs critical charge Q_c for the modeled galactic cosmic ray environment in terms of a linear charge deposition spectrum.