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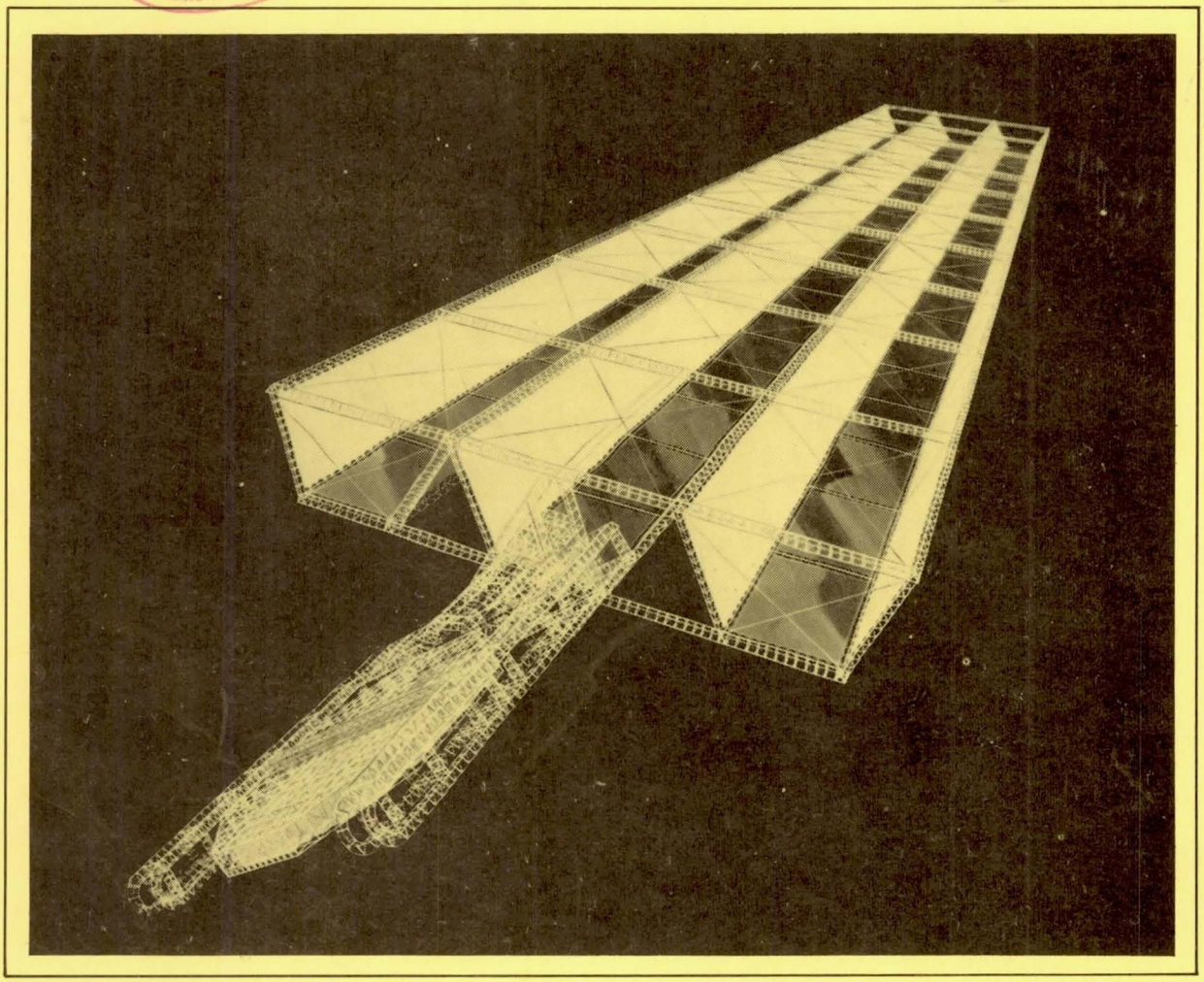

Satellite Power Systems (SPS) Concept Definition Study

FINAL REPORT (EXHIBIT D)

SOLID STATE AMPLIFIER INVESTIGATION

Rockwell International
Space Operations and
Satellite Systems Division

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FOREWORD

This volume, *Solid-State Amplifier Investigation* is submitted by Rockwell International through the Space Operations and Satellite Systems Division and constitutes the final report for Task 6.0 of NASA/MSFC contract NAS8-32475, Exhibit D. Tasks 1.0 through 5.0 are reported in Volumes I through VII of Rockwell document, SSD 80-0108.

This volume presents work accomplished by Space and Secure Communications Systems, Collins Communications Systems Division of Rockwell International, in support of the Space Operations and Satellite Systems Division of Rockwell International, and with subcontractual support from RCA Laboratories, Princeton, New Jersey.

The SPS Program Manager, G. M. Hanley, may be contacted on any technical or management aspects of the report. He can be reached at (213) 594-3911, Seal Beach, California.

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1.0 INTRODUCTION

The Department of Energy (DOE) is currently conducting an evaluation of approaches to provide energy that will meet demands in the post-2000 time period. The Satellite Power System (SPS) is a candidate for producing significant quantities of base-load power using solar energy as the source.

The SPS concept is illustrated in Figure 1.0-1 for a solar photovoltaic concept. A satellite, located at geosynchronous orbit, converts solar energy to dc electrical energy using large solar arrays. The dc electrical energy is conducted from the solar arrays to a microwave antenna. At the microwave antenna, the dc energy is transformed to microwave RF energy utilizing high power klystron vacuum tubes. A large, 1 km diameter, antenna beams the energy to a receiving antenna (rectenna) on the ground. The rectenna converts the RF energy, at very high efficiency, to dc electrical energy which is then connected to the utility network for distribution.

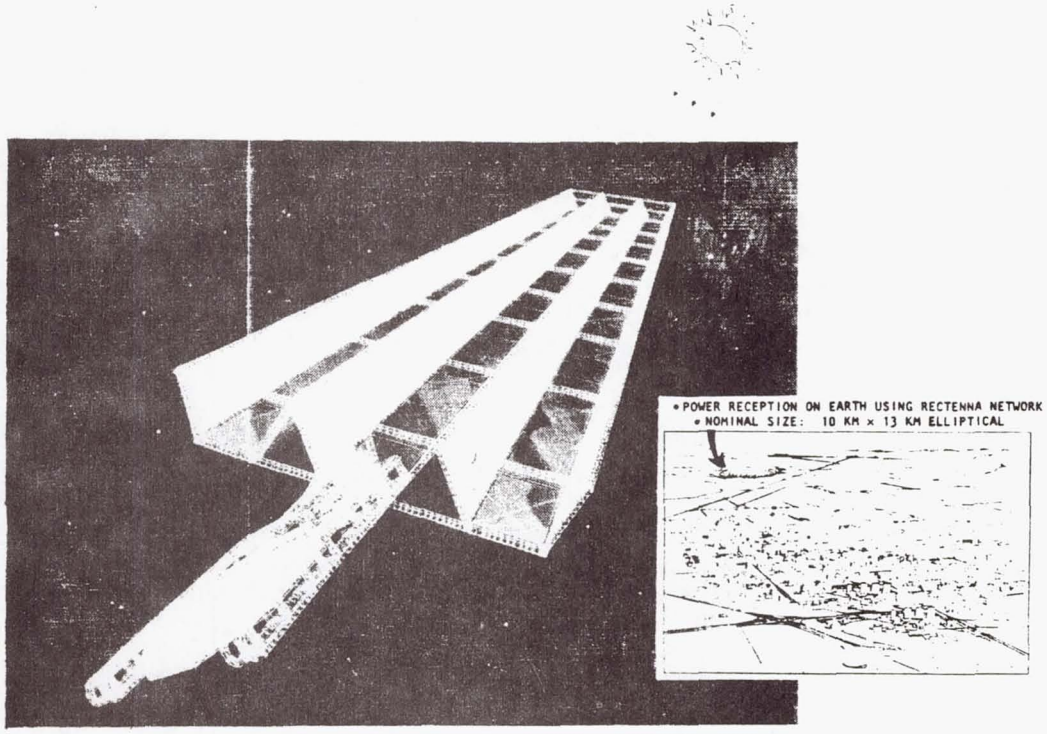


Figure 1.0-1. Satellite Power System Concept

Typically, a single SPS provides 5 GW of power to the utility interface on the ground. Two satellite power systems could provide more power then is needed by large metropolitan areas such as Los Angeles, New York, or Chicago. Because of the large dimensions of the satellite (the solar array area is approximately 30 km^2) and the large mass (approximately 32 million kg), it

is necessary to construct the satellite on orbit where zero-gravity allows very low structural mass. The ground-located rectenna is nominally an elliptical array, 10 km by 13 km. At the earth's surface, the microwave beam has a maximum intensity in the center of 23 mW/cm^2 (less than 1/4 the solar constant) and an intensity of less than 1 mW/cm^2 outside of the rectenna fence line (10 mW/cm^2 is the current United States microwave exposure standard).

This study is part of a continuing effort to provide system definition data to aid in the evaluation of the SPS concept by DOE. The total DOE program includes system definition (of which this study is a part); socioeconomic studies; environmental, health, and safety studies; and a comparative assessment of SPS with other candidate energy concepts. This is the third year of contract effort which is being conducted for NASA Marshall Space Flight Center. One of the major results of the first year of effort was data used by NASA to define two reference concepts which are being used by DOE for their evaluation. The second year's effort concentrated on a more detailed definition of the reference concept, trades relative to the reference concept, conceptual approaches to a solid-state microwave transmission alternative to the reference concept, and further definition of the program. This year's study resulted in an updating of the reference concept, definition of new system options, studies of special emphasis topics, further definition of the transportation system, and further program definition.

A major portion of this year's effort was devoted to the expansion of available data on selected satellites utilizing solid-state amplifiers as the power drivers on the microwave antenna. Solid-state versions of SPS have been investigated by NASA/MSFC, Rockwell, and several other contractors, as an alternative to the present klystron based reference system. Systems using solid-state devices as dc-to-RF converters are attractive in several respects. Solid-state devices generally have a longer MTBF (lifetime). Also, the safety problems caused by the high voltages required for the klystrons and the attendant x-ray radiation are eliminated. A solid-state system also can greatly reduce maintenance requirements.

Analytical studies conducted by Rockwell in prior [NAS8-32475 (Exhibit C, and current Exhibit D)] studies have shown that from a theoretical point of view, a solid state amplifier based antenna could be made competitive with the klystron amplifier based antenna in terms of efficiency, which is one of the key issues in solid state amplifier design. These same studies have shown that gallium arsenide devices would perform better at the high temperatures anticipated in the SPS environment than would equivalent silicon devices.

Although a number of possible solid-state devices can be considered for the SPS solid state power module, only one of them, the gallium arsenide power field effect transistor (GaAs power FET), lends itself to establishing an experimental data point at the present time with respect to solid-state technology for SPS.

Electron beam semiconductor (EBS) devices, and TRAPATT diodes have, at present, an upper efficiency limit of approximately 40-50 percent. This efficiency limitation makes them questionable candidates for the SPS microwave power transmission system. Bipolar transistors which have been shown to have

theoretical efficiency potentials in excess of 80 percent, are presently available only in silicon. GaAs bipolar technology has not yet reached a stage where it would be possible to obtain the necessary devices of this type for the purposes of this program. Several types of FETs, notably the static induction transistor (SIT) and "vertical" FETs, are either still being developed, or have only been developed in silicon.

By contrast, development of the GaAs power FET has been advancing extremely rapidly in the past few years. This device, because of its superior behavior at high frequencies, and because of its desirable low noise characteristics, is being developed as a prime candidate for replacing traveling wave amplifiers in RF transmitters. Commercially available devices have a power output level on the order of 5 watts at the SPS frequency and reported laboratory results have exceeded this performance in some cases. It must be noted, however, that the SPS efficiency requirements are extremely severe and presently available devices have not been designed to meet such requirements.

The factors which affect the power output and the efficiency of GaAs power FETs are well recognized with respect to certain general trends and features, and broad guidelines with respect to several device parameters can be briefly summarized.

- *Device Breakdown Voltage.* The output power capability of the amplifiers is directly related to the magnitude of the voltage which the device is capable of withstanding. Hence, increasing the breakdown voltage is an important factor in increasing the power output capability of the transistor. Improving the quality of the active layer-substrate interface and ohmic contacts will contribute to an improvement in the breakdown voltage. Reducing the doping concentration of the channel also increases the breakdown voltage, but reduces the overall current-carrying capability and, hence, the total output power.

- *Gate Width.* The current-carrying capability is directly related to the total gate width. Increasing the output power capability of the device translates directly into using a larger device, either by increasing the number of cells per device or increasing the size of each individual cell. Increasing the device size can adversely affect the efficiency by increasing parasitic reactances.

- *Device Parasitics.* Minimizing device parasitics has always been a major objective in device design. Such parasitics as the gate metal resistance, the gate capacitance, and the source resistance contribute to lower the efficiency by introducing losses and by limiting the ability of the FET to operate in a "switching" mode which is seen to be a prime requirement when high efficiency modes of operation are analyzed.

- *Thermal Design.* A good heat dissipation capability is also an important factor in attaining the high-efficiency goal. Excessive

device temperatures will contribute to increased losses due to increased resistivity and a reduction in switching speed.

System studies have shown that the efficiency of the SPS dc-to-RF converter has to be on the order of 90%, if that converter is to appear competitive with the current klystron-based system. Because of the different satellite design required by the solid-state concept, as opposed to the klystron approach, the power requirement on each individual converter is not as clearly defined as the efficiency requirement. Estimates of the power required range from 1.5 W per device to 20 W per device.

2.0 OBJECTIVE

The major goal of this study was to investigate the basic feasibility of achieving a very high dc to RF conversion efficiency utilizing solid state amplifiers for power amplification. Identifying specific efficiency limiting factors in order of their importance, specifically with respect to SPS power converter design requirements, represents a task for which no previously accumulated data exist.

The objective was to accumulate such data systematically by making full use of sophisticated measurement techniques which permit the detailed study of current and voltage waveshapes at the terminals of high power transistors as well as other critical points in the circuit. The data derived can be used to achieve a better understanding of operating conditions of high power FET amplifiers, and based thereupon, to arrive at improved circuits and recommendations for changes in the device characteristics to further increase the amplifier efficiency.

The specific goals of this program were addressed in three hardware development phases:

Phase I - This task called for the development of two amplifiers, using GaAs power FETs which are most suited for achieving simultaneously high efficiency and high power output operation. The goals for this development are summarized in Table 2.0-1.

Table 2.0-1. Amplifier Design Goals

Frequency	2.45 GHz
Power Added Efficiency	50%
Power Output	5 watts
Gain	8 dB

Phase II - In this task, a second set of amplifiers were designed using data obtained in Phase I of this effort, as it became available, emphasizing an improvement in efficiency as the prime requirement. The power output and gain are subordinated to the efficiency requirement in this case. These goals are summarized in Table 2.0-2.

Table 2.0-2. Improved Efficiency Amplifier Goals

Frequency	2.45 GHz
Power Added Efficiency	65%
Power Output	Subordinated to efficiency requirement
Gain	Subordinated to Efficiency requirement

Phase III - Concurrent with the above two phases an antenna/rectenna was developed based on antenna concepts described in the major study portion of Exhibit D. This antenna has been and will continue to be used as a demonstration vehicle to demonstrate the operation of the amplifiers developed in Phase I and Phase II of the program.

3.0 PLANNING

3.1 SCHEDULE

The study logic diagram for this program is shown in Figure 3.1-1. The study includes three development phases plus a subcontractor selection phase. The originally proposed schedule is presented in Figure 3.1-2. The milestones for hardware delivery from the subcontractor were postpoined by one month at the request of the subcontractor to provide more time for the completion of the amplifier fabrication.

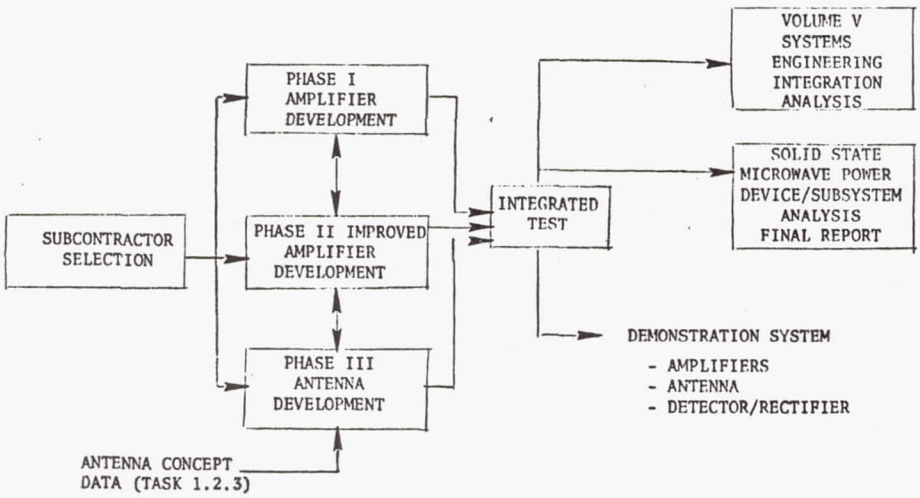
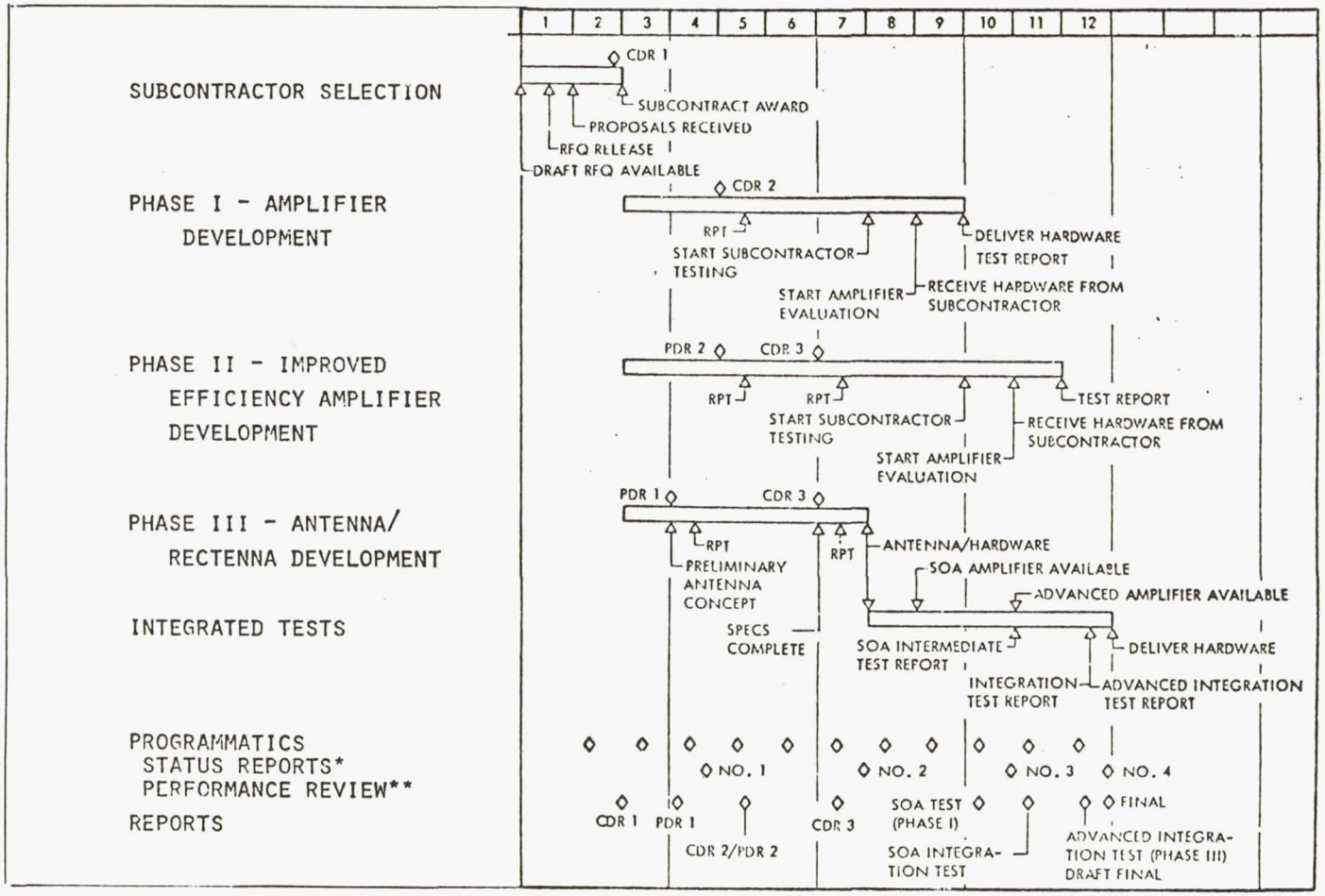


Figure 3.1-1. Study Logic Diagram

3.2 SUBCONTRACTOR SELECTION

The main considerations in the selection of a subcontractor for this program were: expertise in high efficiency power amplifier design, immediately available equipment and instrumentation for device characterization and circuit optimization, a device fabrication capability, and a specific plan to identify efficiency limiting factors.

A critical aspect of the amplifier development program is the capability to analyze each device experimentally while it is operating in a high efficiency circuit. In that respect, RCA has developed a measurement system which permits the detailed study of current and voltage waveforms at any point in the circuit. This has not been generally feasible so far, in the frequency range applicable to this study.



* 1 week prior to 15th
** Briefings

Figure 3.1-2. Schedule

Such a capability offers the advantage of achieving a more detailed understanding of the circuit operation in order to identify the critical parameters of the active device which affect amplifier performance.

RCA Laboratories was selected as the subcontractor for this program, on the basis of the above considerations.

4.0 AMPLIFIER DEVELOPMENT

4.1 APPROACH

The approach followed to accomplish the objectives of this program was based on the study of different FETs, featuring different designs and fabricated using different technologies. The objective was to identify those device parameters that are critical for obtaining high performance; namely, high efficiency and output power. The knowledge so obtained could then be applied toward the design of power FETs optimized to the SPS specifications.

The devices were characterized by means of a unique system which measures the current and voltage waveforms of devices, operating at microwave frequencies. This system is particularly well suited for studying the behavior of active devices operating under large signal conditions. It was found, for instance, that the gate resistance has often the effect of limiting the operating efficiency of the FET for two reasons: One, the resistance causes the channel to partially pinch off during the on-state. This is caused by a build-up of negative gate voltage during forward conduction of the Schottky barrier. Second, the gate resistance slows down the turn-on and the turn-off time which results in added dissipation in the FET and lower operating efficiency. In addition, output power and therefore efficiency is limited by the breakdown voltage of the Schottky barrier, as previously reported[1,2].

A number of FETs were selected from state-of-the-art devices available commercially, which had the potential of operating either at the power or at the efficiency level required by this program. Since little has been experimentally verified about the operation of a GaAs FET under large signal conditions, it was felt that much could be learned from the waveform study on these state-of-the-art FETs.

The driving force behind this effort is the realization that GaAs FETs have the potential of operating at very high efficiency. In effect, recent results were most encouraging: a power-added efficiency of 72% was obtained from a device delivering 1 W of output power at 2.45 GHz. To our knowledge, this is the highest efficiency reported for a solid state device operating at that frequency. In addition to being efficient, these FETs can also be made reliable, therefore they seem well suited for a phased-array SPS transmitter.

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[1] F. N. Sechi, H. C. Huang, and B. S. Perlman, *Waveforms and Saturation in GaAs Power MESFETs*, Digest of the 8th European Microwave Conference, Paris, France, September 1978, pp. 473-477.

[2] D. M. Snider, *A Theoretical Analysis and Experimental Confirmation of the Optimally loaded and Overdriven RF Power Amplifiers*, IEEE Transactions on Electron Devices, Vol. ED14, No. 12, December 1967, pp. 851-859.

4.2 DEVICE EVALUATION

The characterization of the FETs consisted of first measuring the power and efficiency performance at optimized bias and tuning conditions. After this initial characterization, several selected devices were then analyzed with the aid of a system which measures the instantaneous values of voltage and current as a function of time (voltage and current waveforms) at the device's inner contacts (FET contact pads). Computer control was used in both the power-efficiency and the waveform measurement set-ups. This resulted in not only high accuracy and speed, but also made certain measurements possible such as waveform measurements that would otherwise have been impractical. Also, the RF tuning of the device for maximum power-added efficiency—a lengthy and tedious procedure—was greatly facilitated by the availability of a display showing, in real time, the exact value of efficiency and gain.

4.2.1 POWER AND EFFICIENCY CHARACTERIZATION

Measurement System

The measurement system, designed for automatic reading of the operating characteristics of the device, is shown schematically in Figure 4.2-1. The FET is mounted in a test fixture which includes input and output tunable circuits for matching the device to an impedance close to 50 Ω. The circuit losses are minimized by keeping the tuning elements (metal stubs movable along a uniform 50 Ω line) close to the FET. The RF input signal is supplied by a power oscillator tuned to 2.45 GHZ. The RF input power is controlled by a variable attenuator and is measured by a digital power meter (P_{in}), connected to the interface data bus (IB). An automatic tuner, connected to the output of the FET, provides an adjustment of the load impedance. The output power is also measured by a digital power meter (P_{out}).

The dc bias parameters—drain voltage and current (V_D and I_D) and gate voltage and current (V_G and I_G)—are measured by a multichannel scanning DVM. The output of the DVM is read by a BCD input card, located in the multiprogrammer.

The operating data collected by the computer are then used to compute the exact power-added efficiency $\eta_a = (P_{out} - P_{in})/(V_D \times I_D)$ of the device after correcting the data through a calibration of the system. A similar procedure is used for computing the exact gain. The efficiency and gain values set D/A converters whose outputs are read by regular DVMs which provide a convenient efficiency and gain display. In addition, at the command of the operator, the computer prints on a terminal a listing of the device operating conditions such as the dc parameters (V_D, I_D, V_G, I_G), RF parameters (P_{in} and P_{out}), efficiency and gain. A listing of the computer program, including the utility subroutines, is reproduced in Appendix A.

Performance

The tuning of the device is optimized for either maximum power-added efficiency, maximum output power, or at times, a combination of the two. A given device whose physical characteristics define the ultimate efficiency performance, operates in a circuit at an efficiency which is an intricate

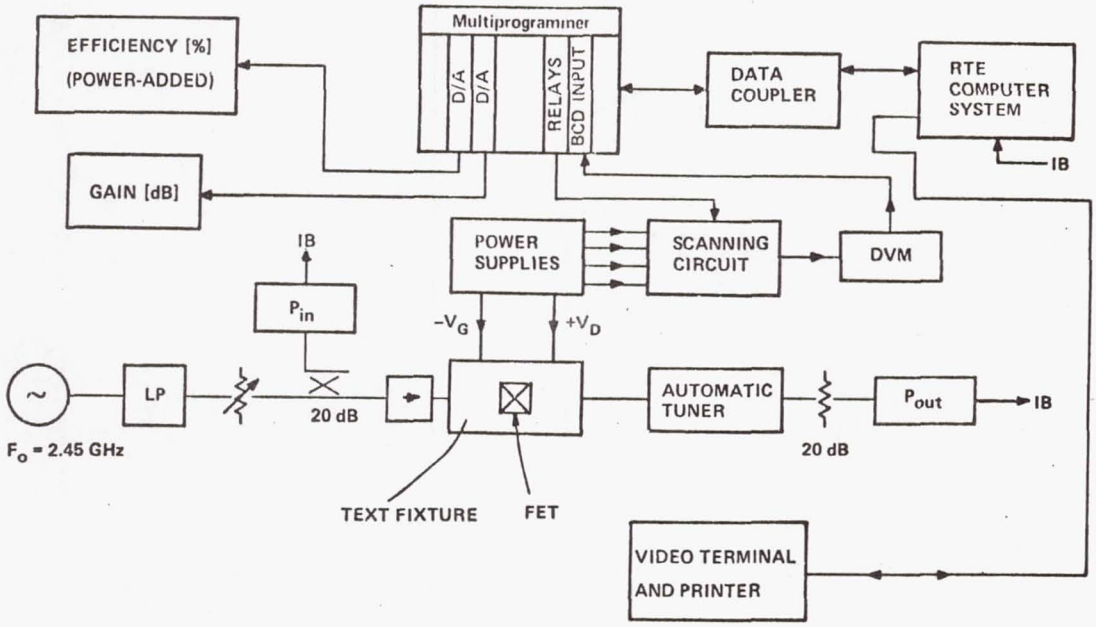

Figure 4.2-1. Power and Efficiency Measurement Set-Up

function of many circuit-dependent and bias-dependent parameters. Therefore a direct procedure for defining the value of each parameter is not practical because of the strong interaction between circuit dependent and bias dependent parameters. The procedure adopted, which is easily implemented with the set-up of Figure 4.2-1, is based on successive approximation, by adjusting the RF tuning and bias until optimum efficiency is reached. Here the automatic tuner is used as a second order adjustment—at low VSWR and in a manual mode—in order to minimize the power loss and achieve highest efficiency.

An example of the performance of an FET, as measured by the automated system, is shown in Table 4.2-1. The RF tuning and the bias of the FET are adjusted for highest power-added efficiency. The input power P_{in} is varied, while the drain and gate bias voltages are kept essentially constant (small variations are caused by voltage drops across the current sampling resistors). For this particular device the efficiency peaks at a value of 59.9% with an output power of 5.1 W and a gain of 9.5 dB. The highest efficiency is always obtained at a substantial degree of gain saturation, 1.9 dB in this case, and for other FETs ranges from 2 to 4 dB.

Table 4.2-2 is a listing of the devices tested in this program and of their performance measured at optimized conditions. The FLS50 and the FLC30 are manufactured by Fujitsu. The MGF2148 and 2150 are manufactured by Mitsubishi. The NEC868400 are devices made by Nippon Electric. The latter were brought in chip form and mounted by us on special low-parasitic carriers. The original plan was to attempt direct paralleling of chips, if the performance was considered satisfactory. However, since their performance was lower than what was obtained from other devices, this approach was not pursued further. The RPC3315 are manufactured by Raytheon. The MSC88010 are manufactured by Microwave Semiconductor Company.

Table 4.2-1. FLS-50 Test Results

FUJITSU FLS-50 #2426 50OHM CKT.
2:39 PM MON., 21 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.66	.713	-1.88	-.164	.567	5.121	59.94	9.56
10.69	.641	-1.94	-.045	.282	3.518	47.24	10.96
10.69	.635	-1.96	-.005	.138	2.036	27.96	11.68
10.70	.603	-1.96	-.002	.059	.863	12.44	11.61
10.70	.603	-1.96	-.001	.048	.696	10.02	11.58
10.70	.603	-1.96	-.001	.038	.543	7.83	11.56
10.70	.598	-1.96	-.001	.031	.440	6.40	11.54
10.71	.598	-1.96	-.001	.024	.335	4.86	11.51
10.71	.598	-1.96	-.001	.017	.244	3.54	11.47
10.71	.601	-1.96	-.001	.012	.162	2.34	11.47
10.70	.598	-1.96	-.001	.007	.101	1.46	11.46
10.71	.601	-1.96	-.001	.002	.031	.44	11.41

20>BR;ETEST

10.67	.690	-2.21	.492	.639	5.100	60.63	9.02

OPTION NUMBER =?4

Table 4.2-2. Summary of Performance of Tested Devices

	DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN dB
FLS50 #2	9.7	385	2.3	+.003	.380	2.740	63.09	8.57
	9.97	583	2.13	-.016	.574	3.959	58.18	8.39
FLC30 #4230	6.12	405	3.39	+.001	.285	1.730	58.2	7.83
	10.4	805	2.3	-.005	.535	4.084	42.3	8.82
MGF 2148	5.51	.744	1.7	.03	.269	1.307	25.31	6.68
MGF 2150 #45477	4.95	.256	1.29	1.88	.071	.971	71.03	11.34
NEC86840C	6.69	.641	3.48	-3.14	.240	1.735	37.39	8.59
LOT 8717-9 #1	8.56	.727	2.92	-3.14	.526	2.435	30.68	6.66
NEC864800 LOT 8717-9 #2	6.85	.770	3.31	-3.14	.214	1.684	27.48	8.91
NEC86400	6.55	.641	3.51	-3.14	.222	1.558	31.82	8.46
LOT 8717-9 #4	8.42	.788	3.08	-3.14	.445	2.151	27.65	6.85
FLS-50 #2426	10.66	.713	1.88	.164	.567	5.121	59.94	9.58
FLS-50 #1333	7.57	.868	2.03	-.472	.694	3.407	41.30	6.91
	11.36	1.256	1.35	-.899	.975	5.574	32.24	7.57
FLS-50 #1336	8.27	.612	1.95	1.611	.575	2.923	46.38	7.08
	11.75	.874	1.51	.779	.847	4.375	34.37	7.13
FLC-30 #6136	10.45	.132	3.97	-.017	.189	1.189	72.45	8.00
FLC-30 #6327	10.71	.698	3.62	-1.90	.476	4.092	48.85	9.34
RPC3315 #1	5.54	.296	2.51	1.35	.101	.864	46.54	9.33
MSC 88101 #1	4.03	.572	2.86	-3.14	.194	.959	33.17	6.93
	10.41	1.187	1.55	2.9555	1.102	3.37	18.41	4.86
MSC 88101 #2	5.40	1.261	1.83	-3.14	.245	1.552	19.20	8.02
	9.70	1.52	1.33	2.542	1.504	3.105	10.86	3.15
FLS-50 #4039	10.43	.675	-2.32	6.788	.583	4.022	48.83	8.39
FLS-50 #4037	11.16	.736	-2.47	12.67	.785	4.838	49.38	7.90
FLS-50 #3734	11.43	.721	-2.08	7.466	.521	5.121	55.79	9.92
FLS-50 #3732	10.53	.825	-2.62	6.816	.760	5.282	52.07	8.42
FLS-50 #3731	10.56	.750	-1.91	8.278	.629	5.080	56.21	9.08
FLS-50 #3726	10.19	.839	-1.65	12.78	.710	5.373	54.53	8.79
FLC-30 #S-009	9.01	.399	-3.19	-.026	.350	2.548	61.09	8.63
FLC-30 #S-008	9.96	.345	-2.60	.301	.258	1.942	54.50	8.76
FLC-30 #S-007	10.27	.483	-2.57	-.089	.404	2.740	47.12	8.31
FLC-30 #S-006	9.60	.336	-2.55	-.016	.326	2.115	55.44	8.12

The best efficiency performance was obtained from an FLC30, which provided a power-added efficiency of 72% with an output power of 1.19 W and an associated gain of 8 dB. To our knowledge this efficiency performance is the highest reported for any solid-state device operating at 2.45 GHz. Similar performance was also obtained from a Mitsubishi-type MGF2150 device. Interestingly, both devices are designed for high frequency operation, C- and X-band, respectively. Their high cut-off frequency (approximately 12 and 19 GHz) allows rapid switching and a mode of operation that is conducive to high efficiency.

The best power performances were obtained from TLS50-type devices that often provided output power in excess of 5 W with power-added efficiency of 50-60%.

The NEC-type 868400 devices delivered the rated output power, but had rather low efficiency. The MSC-type 88010 devices delivered the rated power, but also operated at low efficiency. The Raytheon-type RPC3315 devices delivered low power. More detailed data on the performance of these devices are listed in Appendix B.

4.2.2 WAVEFORM MEASUREMENTS

Measurement System

This system was specifically developed for studying nonlinear effects in GaAs power FETs[1]. It was improved during the course of this program in order to increase its flexibility and convenience. The system, with its main components, is shown in Figure 4.2-2. A source of microwave power at 2.45 GHz feeds the input of a test fixture in which the FET is mounted. The fixture

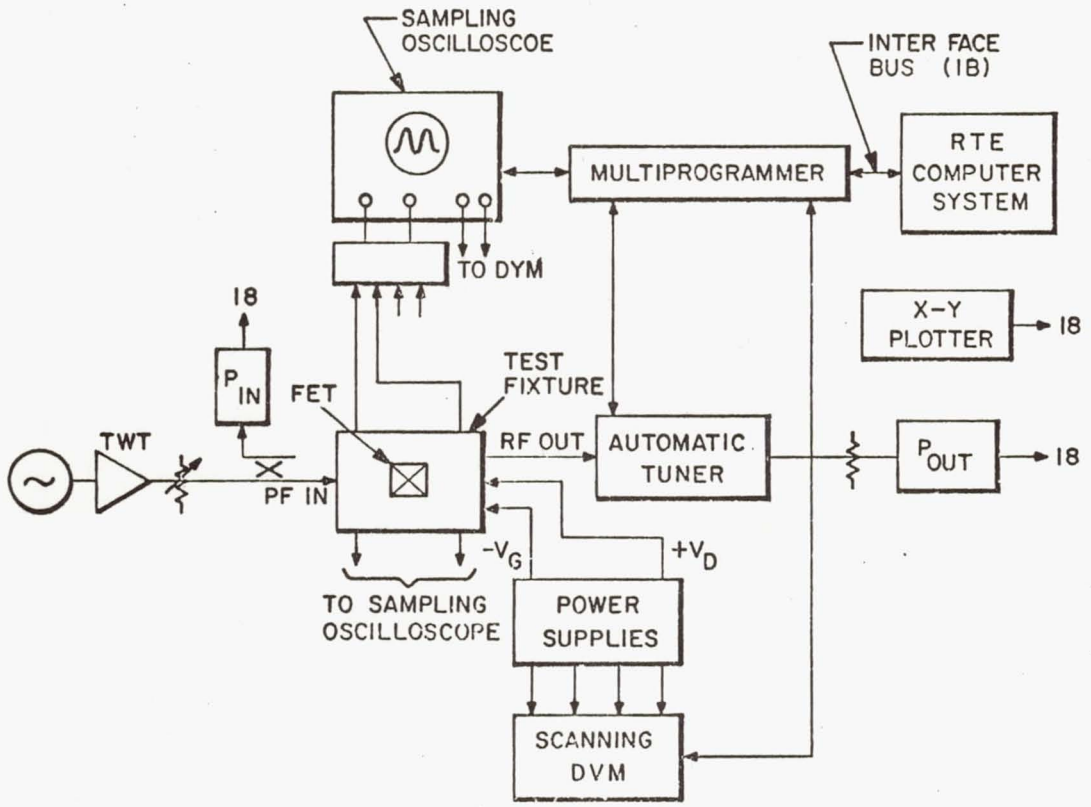

Figure 4.2-2. Waveform Measurement System

[1]Sechi, F.N., Huang, H.C., and B.S. Perlman, *Waveforms and Saturation in GaAs Power MSFETs*, Digest of the 8th European Microwave Conference; Paris, France; September 1978, pp. 473-477.

includes input and output tuning circuits that match the FET to the input generators and to the output load and shape the waveforms for optimum efficiency and power performance. Four very small resistive probes, integrated with microstrip tuning circuits, sample the waveforms at different points in the circuit. The four signals are then routed through switches into a dual-channel sampling oscilloscope. The time axis of the oscilloscope is stepped by the output of a computer-controlled D/A converter. The vertical outputs from the oscilloscope are digitized and the data are stored in the computer. The basic operation is as follows. The measured data are processed with a fast Fourier transform algorithm. The resultant spectral components are then corrected for the amplitude and phase frequency response of the probes, previously characterized over a frequency range covering typically five harmonics. This defines the corrected spectra of the voltage waveforms present in the circuit at the probing points. These spectra are then used, in conjunction with the ABCD parameters of various sections of the circuit, to compute the current spectra and finally, the current waveforms. This procedure, based on Fourier transform and reverse transform of signals, allows the derivation of current waveforms more accurately than could be done by direct current measurements.

With the present hardware, the system has substantially reached its limit speed. The four scans—each one consisting of 256 data points—are executed in approximately 50 seconds. Special computer-controlled RF switches are included in the system for multiplexing the four signals derived from the probes into the two channels of the sampling oscilloscope. This drastically reduces the time required for each experiment (as compared to manually connecting and disconnecting the four RF cables) and improves repeatibility and measurement accuracy.

The time required for setting up the experiment is also kept to a minimum by storing of all of the calibration data in disc files that are recalled after turning on the main program. Thus, it is possible to avoid the lengthy process of repeatably entering the data related to the calibration of probes, the input and output tuning circuits, and the package of the FET. In addition, all of the measured data can be stored in data files, which is a convenient feature for reanalyzing results without having to rerun the experiment. The present formatting of the output data and available operating options make the system very flexible and easy to use.

Waveforms in GaAs FETs

Four different types of devices were analyzed. The first three were higher frequency (C- and X-bands), lower power (2-3 W) types; the fourth was a lower frequency (S-band), higher power (8 W) type.

The waveforms of Figures 4.2-3 through 4.2-8 were measured on an MGF 2150 type device, made by Mitsubishi and specified for an output power of 2 W at 12 GHz. At this frequency, it is the most powerful device commercially available. Both theory and experimental evidence indicated that a high cut-off requency is a necessary, although not the only, requirement for achieving high operating efficiency. Indeed, this device provided some of the best results, specifically a power added efficiency of 71% with an output power of 0.97 W.

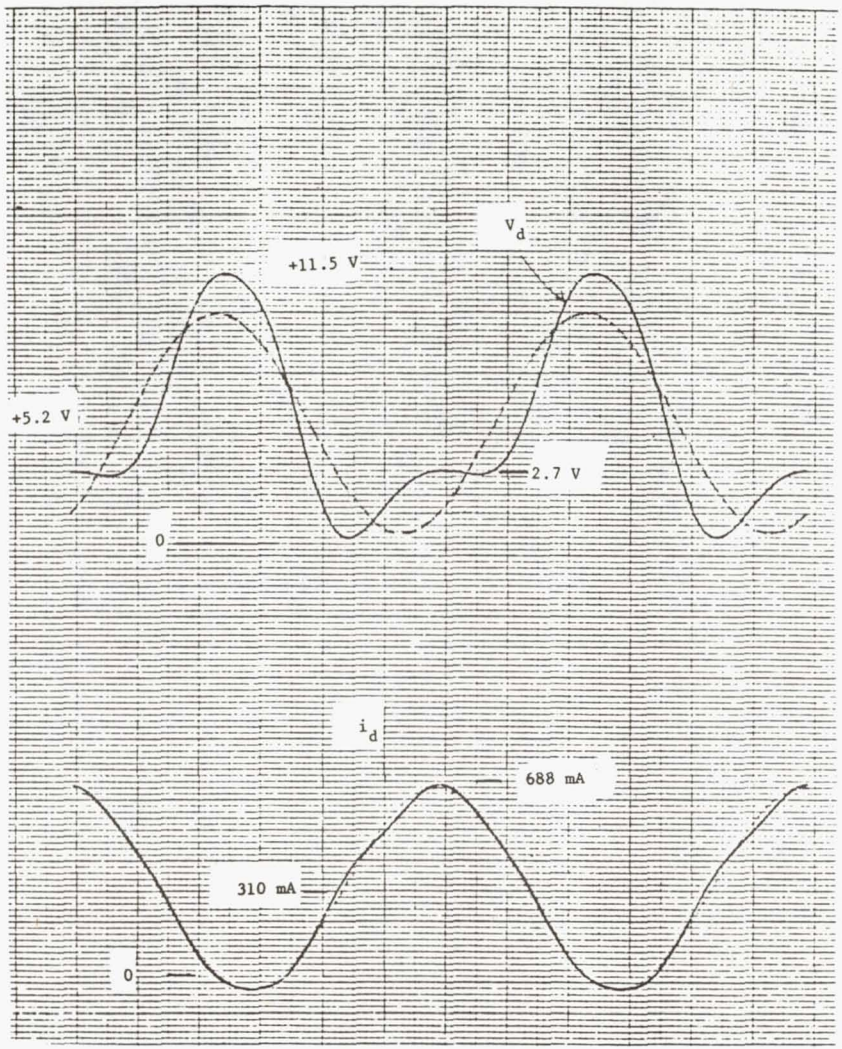

Figure 4.2-3. MGF 2150, Drain Waveforms, Maximum Efficiency Point

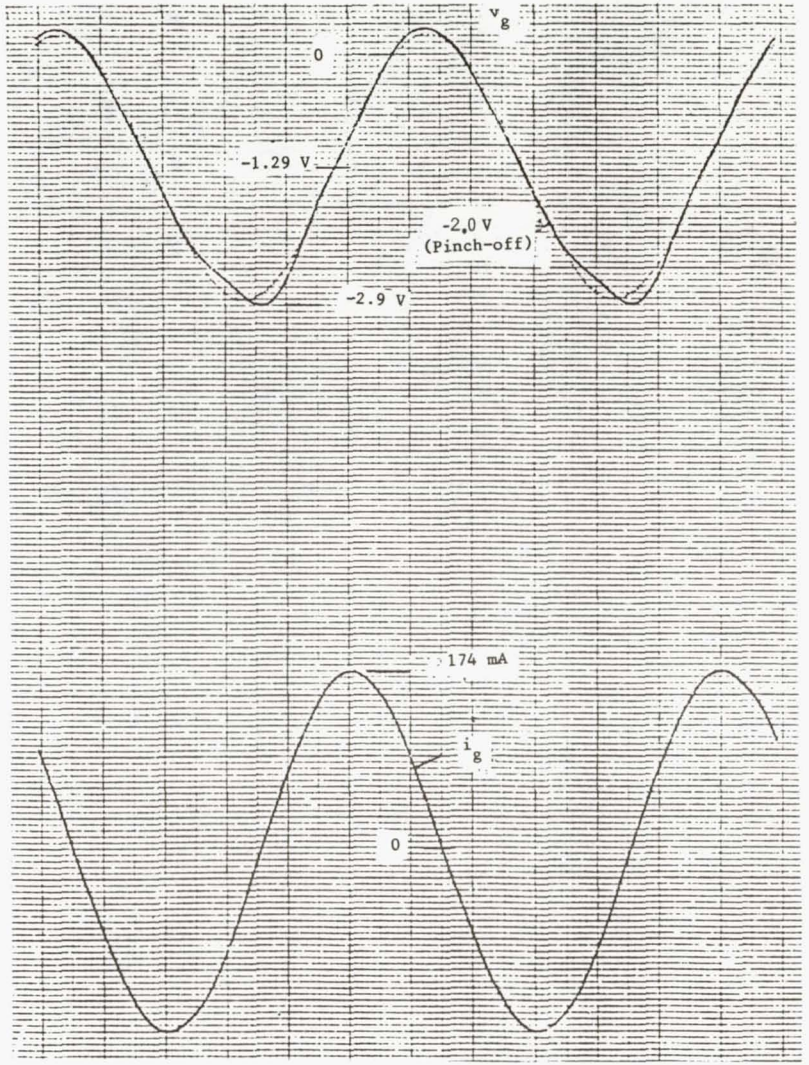

Figure 4.2-4. Gate Waveforms, Maximum Efficiency Points

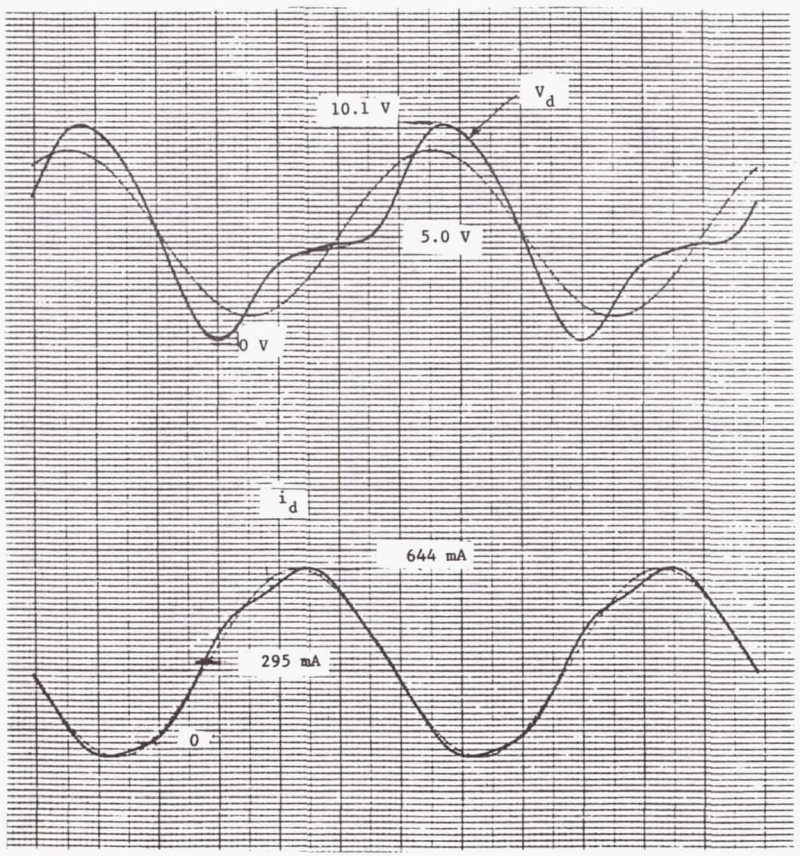

Figure 4.2-5. Drain Waveforms, 1-dB Overdrive

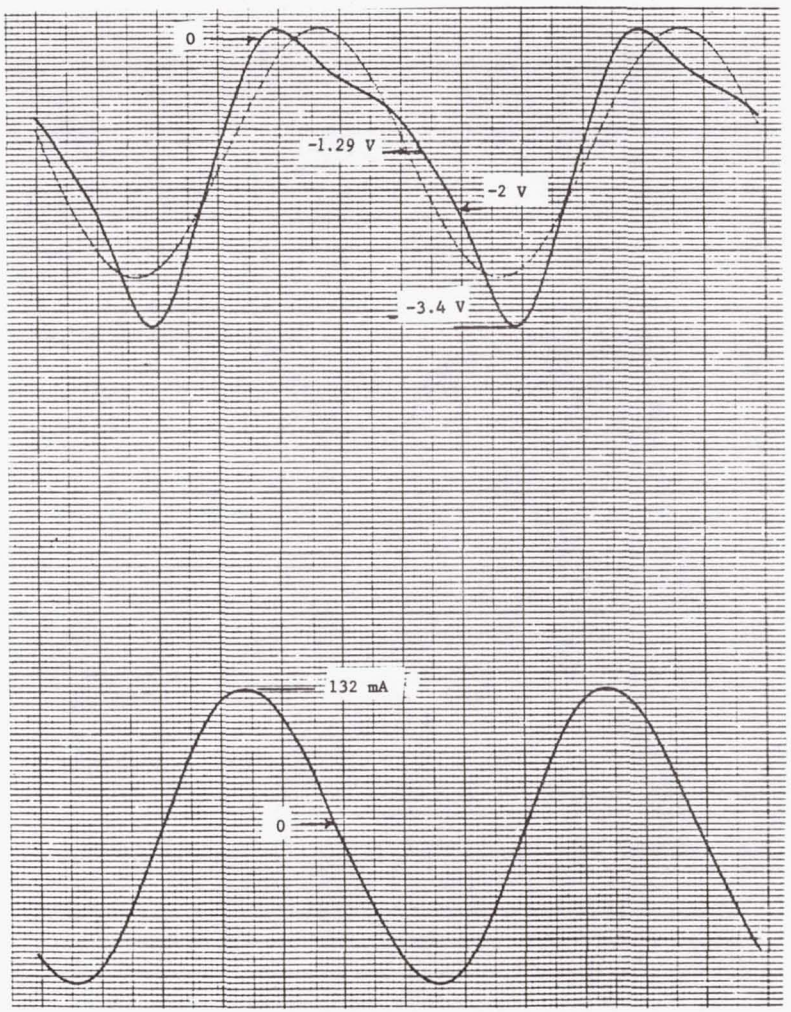

Figure 4.2-6. Gate Waveforms, 1-dB Overdrive

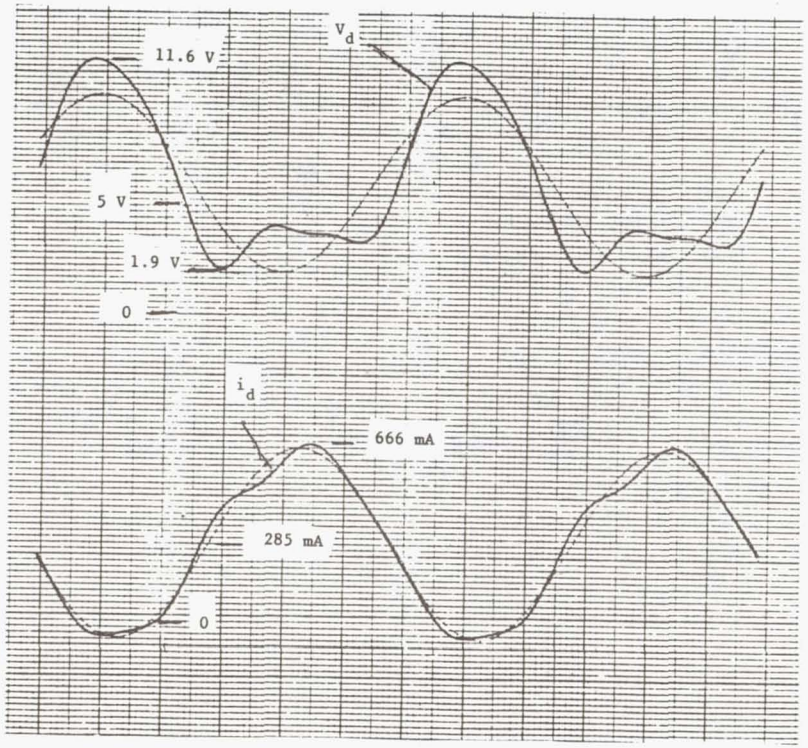

Figure 4.2-7. Drain Waveforms, 2.3-dB Overdrive

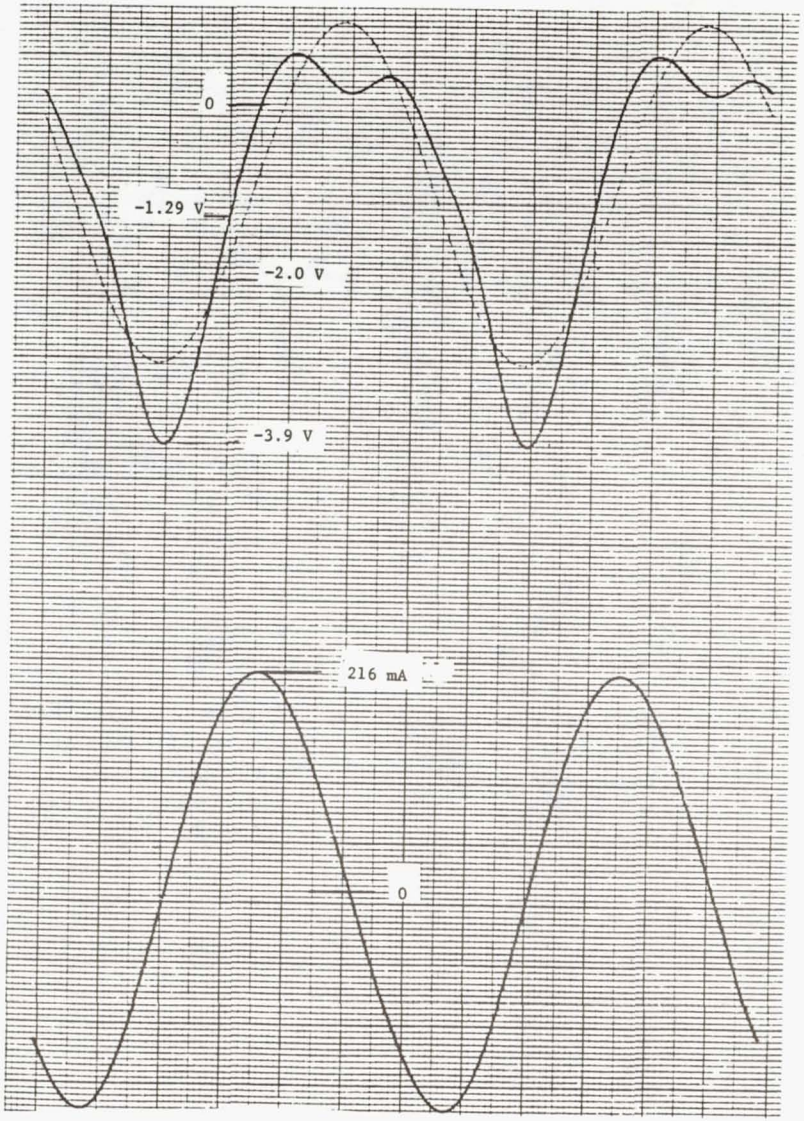

Figure 4.2-8. Gate Waveforms, 2.3-dB Overdrive

The waveforms of Figures 4.2-3 and 4.2-4 were measured under conditions which correspond closely to the condition that provided maximum efficiency. The drain voltage waveform, V_d, approaches a square wave. This is a mode of operation which is conducive to high efficiency. The current is mostly sinusoidal, in agreement with the theory for maximum efficiency[1]. Only a small amount of distortion can be seen near the waveform peak.

The corresponding gate waveforms, at a bias of -1.29 V, are shown in Figure 4.2-4. Because of the high transconductance (630 ms) and low pinch-off voltage (-2 V) of this device, the peak-to-peak voltage swing is low (3 V). Under this condition, the distortion of the waveform is rather small. The gate current is mostly capacitive (70° advanced with respect to V_g) and reaches a high peak value because of the rather high input capacitance, approximately 5.5 pF.

Figure 4.2-3 shows the FET fully turned on ($V_d \approx 0$) only for a small fraction of the cycle, approximtely 60%. During the following 120° of the cycle, V_d rises to a value of approximately 2.7 V. This rather high voltage across the FET during the on-time is detrimental to the efficiency. If, for instance, the voltage were to be maintained at a constant value of 0.7 V—corresponding to a low-field resistance of 1.0 and a peak current of 688 mA—the efficiency could reach a value of approximately 80%.

A seemingly certain way for achieving a full turn-on and turn-off of the device and better approximating a switch mode of operation is to increase the level of RF input drive. The expected result is an increase of the power-added efficiency, provided that the device gain is still sufficiently high to have a net increase of output power. However, our experiments have shown this not to be the case. When the RF input power was increased 1 and 2 dB above the optimum efficiency condition, the drain voltage waveforms (as shown in Figures 4.2-5 through 4.2-8) revealed a significant increase of the "on" voltage. This effect clearly reduces the operating efficiency. The cause of the unexpected result was traced to the presence of forward conduction currents flowing through the resistance of the gate circuit. Specifically, a sufficiently large RF signal overcomes the negative bias of the gate and causes the gate to draw current in the forward conduction direction during part of the RF cycle. This current, flowing in a direction such as to develop a negative resistance in the gate circuit, adds a negative voltage to the gate across the resistance of the gate stripes. This negative voltage constricts the channel, increasing its resistance, at a time when the drain current is at its peak. This causes an increase of the voltage drop across the FET during the "on" time, as it is evident in Figures 4.2-5 and 4.2-7. At the higher overdrive (2.3 dB), the gate voltage waveform of Figure 4.2-8 clearly shows clipping about 0.7 V, due to forward conduction of the Schottky barrier.

In quantitative terms, the additional voltage drop across the FET (ΔV_d) is related to the forward conduction gate current (I_{g_o}) by:

$$\Delta V_d = R_L \, R_g \, g_m \, I_{g_o}$$

[1]D.M. Snider, *A theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifiers*, IEEE Transactions on Electron Devices, Vol. ED14, No. 12, December 1967, pp. 851-859.

where R_L is the output load resistance, R_g is the gate resistance, and g_m is the device transconductance. Output power and gain dictate the values of R_L and g_m, while I_{g_o} is determined by the level of the input RF drive and the degree of saturation. The only free parameter that can be used to control ΔV_d is the gate resistance, R_g, which therefore becomes an important parameter in determining the maximum operating efficiency. To our knowledge, this effect of the gate resistance—limiting the minimum dynamic saturation voltage of the device because of RF rectified by the Schottky barrier—has not been reported before and is considered an important finding in this program.

Other effects, however, might also influence the device and limit the efficiency and output power. One of these, incomplete control of the gate over the drain current, is shown in Figure 4.2-9. These waveforms pertain to an MGF2148-type device (Mitsubishi), similar in construction to the MGF2150-type device of Figures 4.2-3 through 4.2-8. Figure 4.2-9 clearly shows incomplete pinch-off of the channel, leaving a residual current of 200 mA. This effect might be caused either by a defective metallization that left four or five gate stripes disconnected, or by a large nonuniformity in the doping or thickness of the active GaAs layer.

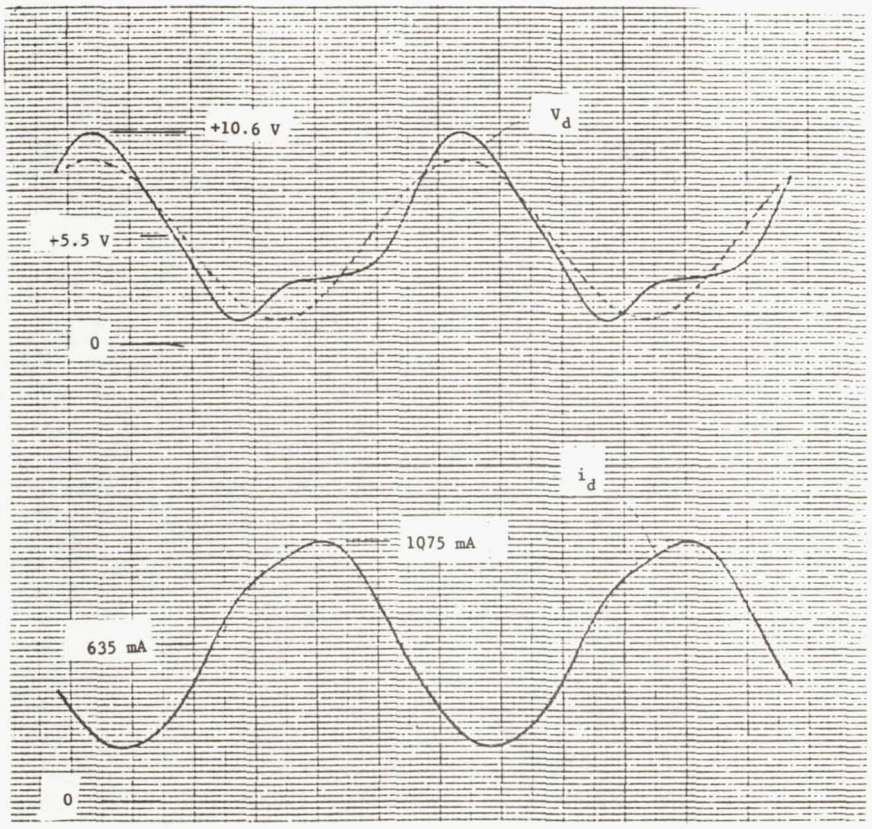

Figure 4.2-9. MGF 2148—Nominal Drive—
Drain Waveforms

Also analyzed was the FLC30-type Fujitsu device, designed for C-band operation, which provided the highest efficiency performance at 2.45 GHZ (72% at 1.1 W of output power). Waveforms were measured over a range of drain voltages from 6 to 10.5 V and a range of gate voltages from -4.0 to -0.5 V, corresponding to a drain bias current range from zero (pinch-off) to 80% of the saturated drain current at zero gate bias (I_{DSS}). The waveforms measured at the operating condition corresponding to the maximum efficiency are shown in Figures 4.2-10 and 4.2-11. The bias level was 10.5 V and 130 mA for the drain and -4.0 V for the gate. The drain voltage waveform shows a pronounced distortion, although it does not clearly indicate the switching mode of operation which would lead to an even higher efficiency.

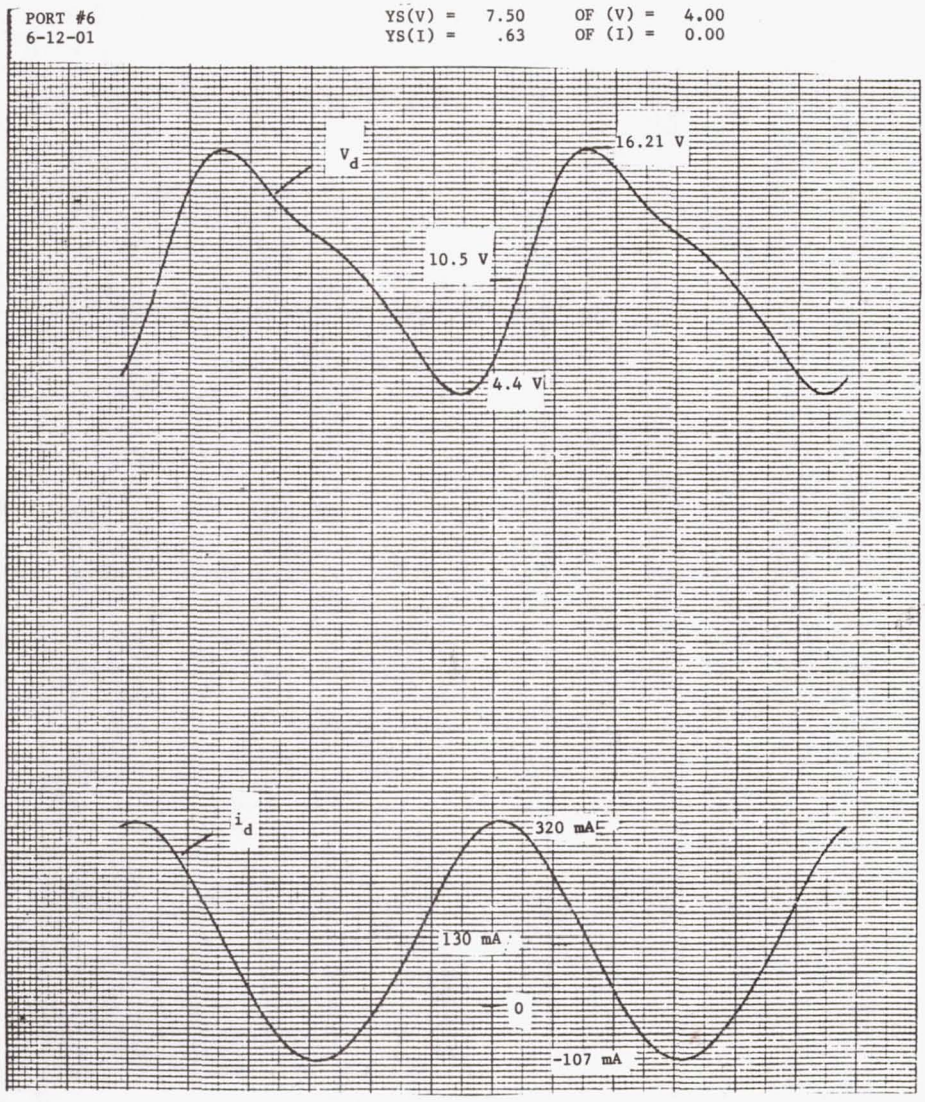

Figure 4.2-10. FLC30—Drain Waveforms, Maximum Efficiency Drive

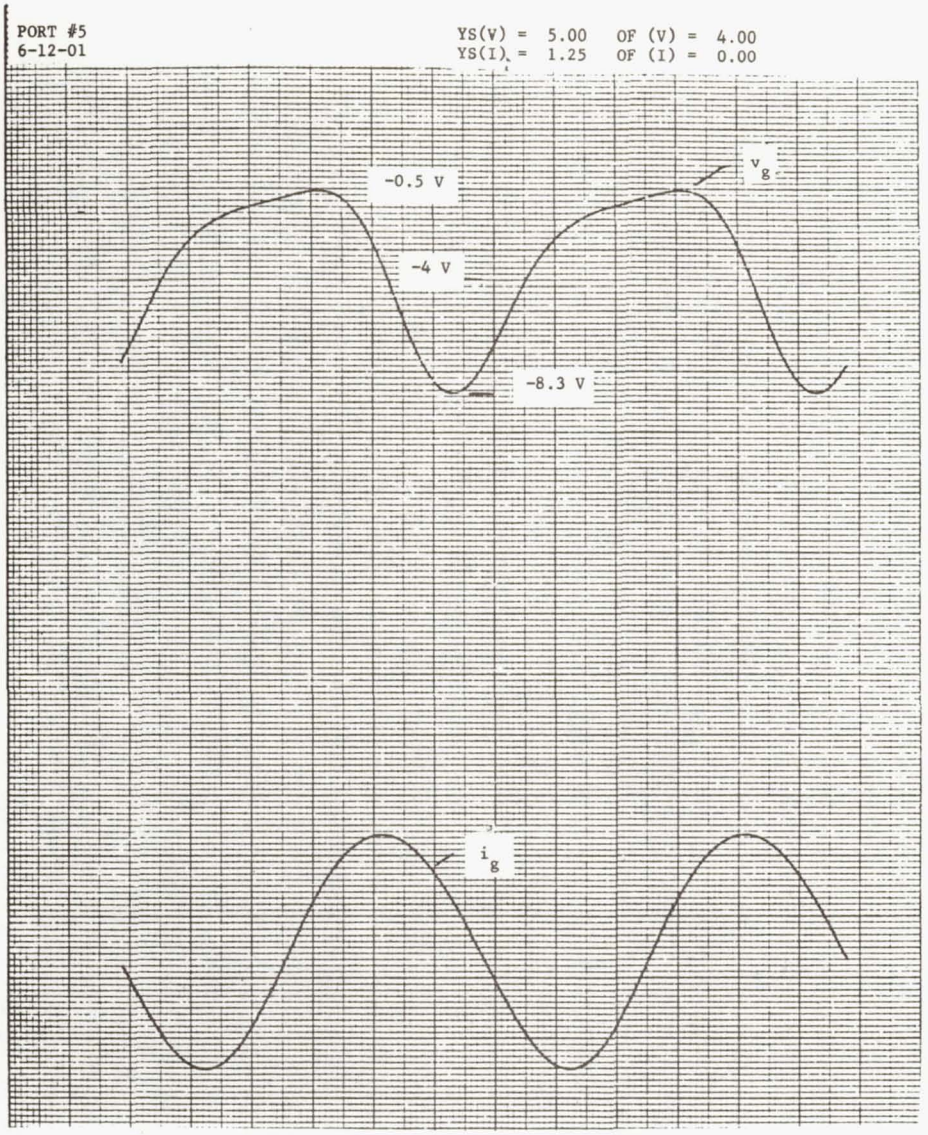

Figure 4.2-11. FLC30—Gate Waveforms, Maximum Efficiency Drive

The drain current is virtually sinusoidal, as it is expected in FETs operating with tuned output circuits. In addition, during approximately 30% of the cycle, the drain current is negative. This is caused by an apparent increase of the amplitude of the current in the active device due to the device output capacitance. The amplitude ratio, K, between the current in the active device and the total current (including output capacitance), is given by:

$$K = 1/(1 - \omega^2 LC + j\omega RC)$$

where C is the output capacitance, and L is the output tuning inductance in series with the output load resistance R. At resonance, K assumes the value

of 0.4 for R = 25 Ω and C = 1 pF, which is consistent with the values of the negative current swing that have been observed during these experiments.

The instantaneous gate voltage V_g varies between -0.5 V and -8.3 V around a dc bias of -4.0 V. The flattening of V_g around -0.5 V is caused by a large change of the gate-to-source capacitance due to the varactor-like behavior of the Schottky barrier. The gate current is mostly capacitive and sinusoidal because of the filtering effect of the high impedance ratio input tuning circuit.

Interestingly, when the device was heavily overdriven (a 7-dB increase in RF input power), the drain waveform remained practically unchanged, as shown in Figure 4.2-12. This indicates that the current saturation is caused by the

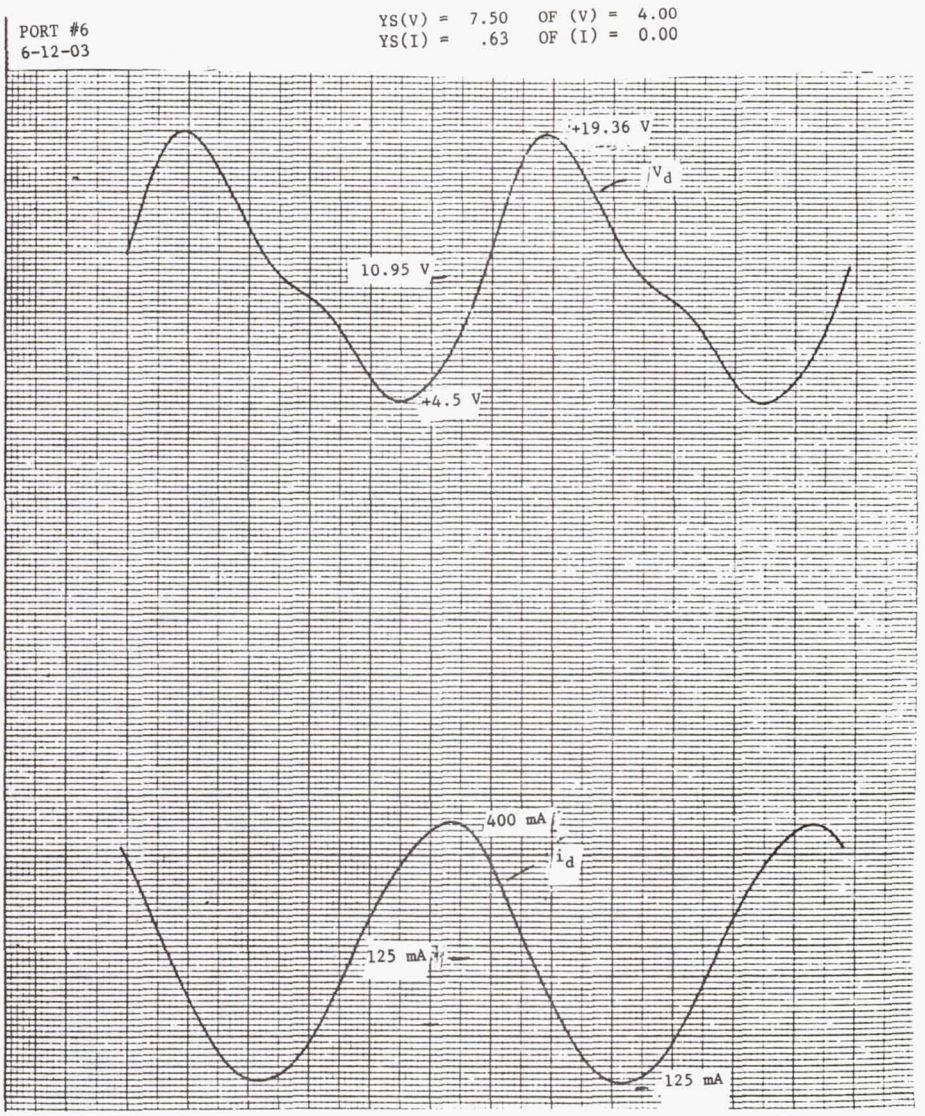

Figure 4.2-12. FLC30—Drain Waveforms, 7-dB Overdrive

gate, which has lost control of the current in the channel. Figure 4.2-13 shows that the large overdrive has the effect of greatly increasing the gate current and voltage peak values, and of heavily distorting the gate voltage waveform. The flattening of V_g above zero volts indicates forward conduction of the Schottky barrier.

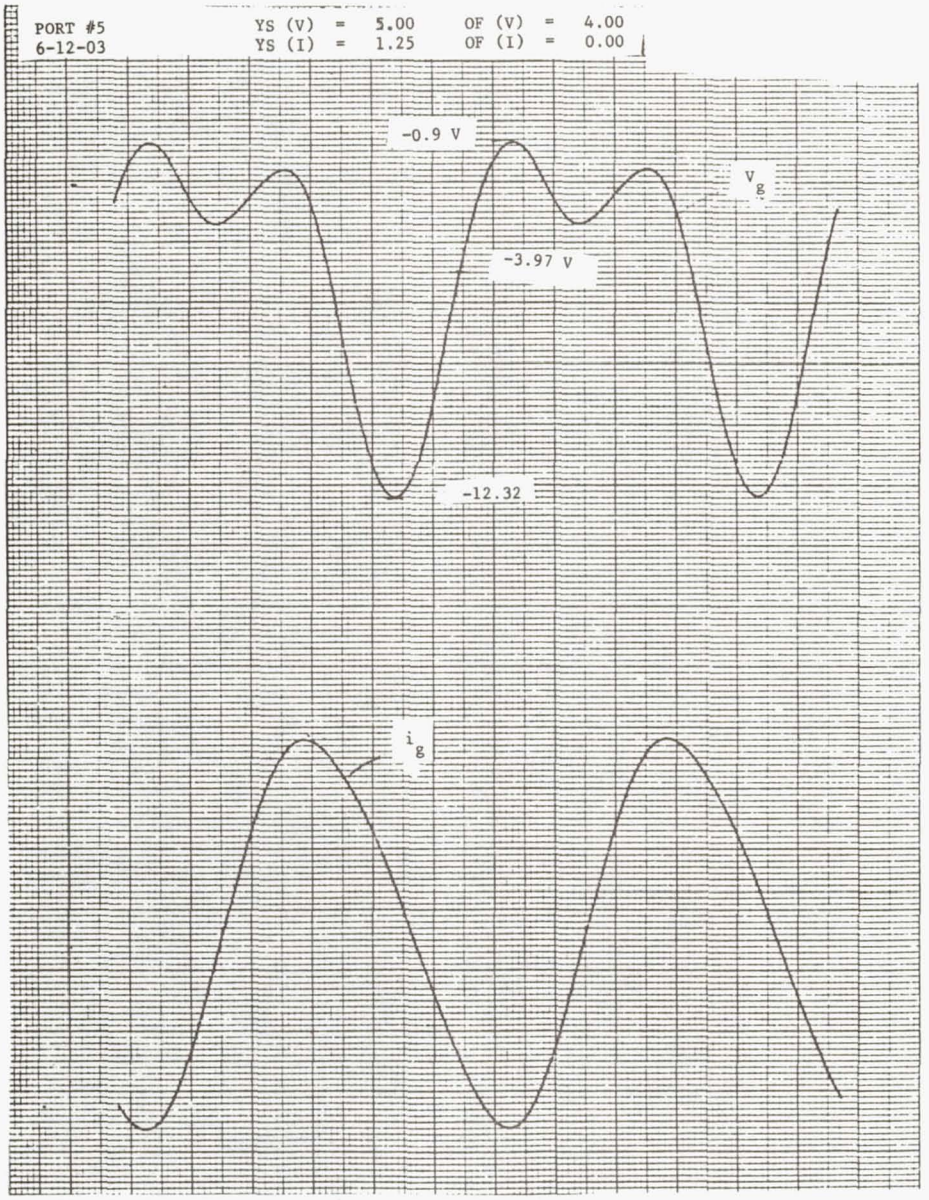

Figure 4.2-13. FLC30—Gate Waveforms, 7-dB Overdrive

When the drain bias voltage was changed from 6.0 to 10.5 V, the drain peak voltage varied from 11.5 to 18.5, as shown in Figure 4.2-14. Also shown in the source figure is the peak voltage computed from a "low frequency model," which includes the dc characteristics of the FET, a lossless resonator, and a 25 Ω resistive load. The actual peak voltages are approximately 1 V higher than

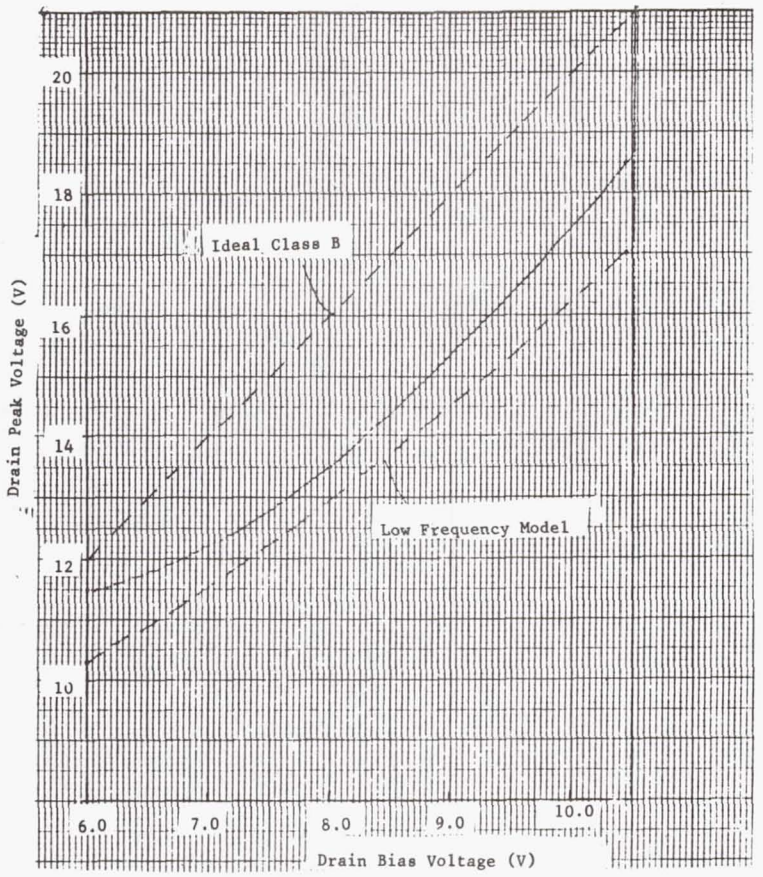

Figure 4.2-14. FLC30 Peak Drain Voltage Vs. Drain Bias

those computed with the model, because the nonlinearity of the gate-to-source capacitance sharpens the peak of the drain voltage waveforms. The upper curve in Figure 4.2-14 pertains to the limit case of an ideal Class B tuned amplifier, which predicts a peak voltage equal to twice the bias voltage.

The minimum voltage during the on-state (saturation voltage) was also derived from the waveform measurements, and the results—as a function of the drain bias voltage—are shown in Figure 4.2-15. The difference with the low frequency model is probably caused by unaccounted reactive parasitic elements in the FET carrier, such as the source inductance.

The drain peak voltage and the saturation voltage were also measured as functions of the gate bias voltage, as shown in Figures 4.2-16 and 4.2-17. The drain peak voltage reaches a maximum value at a gate bias of -1.7 V, which corresponds to approximately $I_{DSS}/2$. A more negative gate bias brings the device closer to the Schottky breakdown, thereby reducing the available voltage swing.

Finally, waveform measurements were carried out on an FLS50-type Fujitsu device, capable of delivering 5 W of output power at S-band. The device was tuned for highest efficiency (50%) at a drain voltage of 10 V and a drain

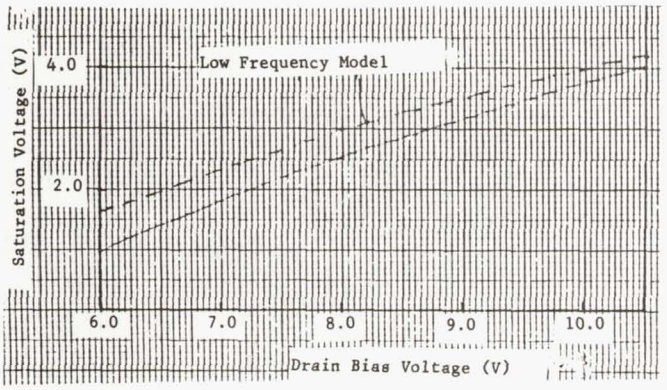

Figure 4.2-15. FLC30 Saturation Voltage as a Function of Drain Bias

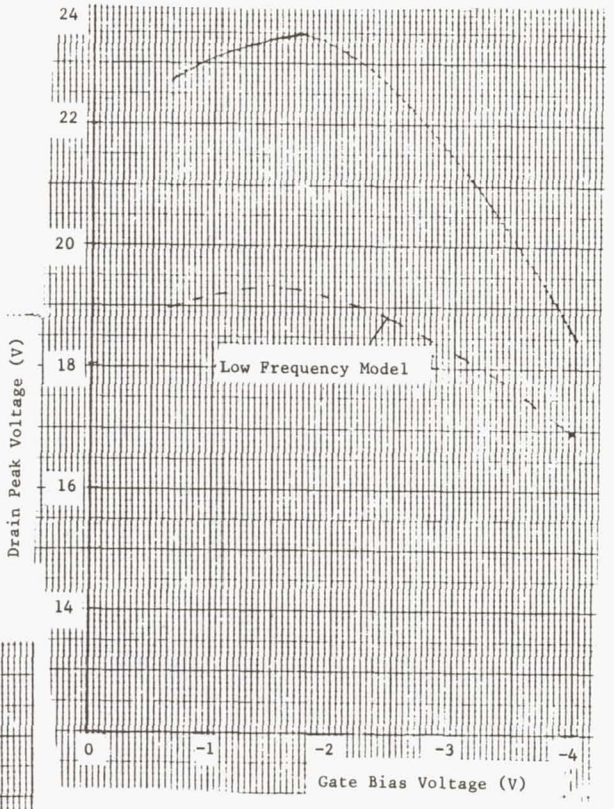

Figure 4.2-16. FLC30 Drain Peak Voltage Versus Gate Bias Voltage

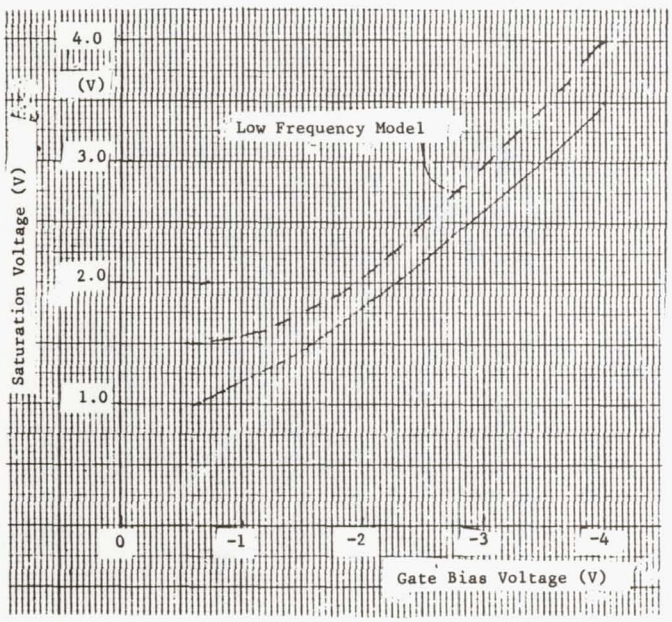

Figure 4.2-17. FLC30 Saturation Voltage as a Function of Gate Bias Voltage

current of 25% of I_{DSS}. Measurements were then taken at drain voltages ranging from 6 to 11 V and drain currents ranging from 16 to 40% of I_{DSS} and at RF drive levels corresponding to 1, 2, and 3 dB of gain compression. The results show that the drain voltage and current are fully modulated. However, even at the higher RF drive as shown in Figure 4.2-18, for the 3-dB compression case, the device did not approach the switching mode of operation which would be conducive to higher efficiency. This behavior may be explained by the slow response of the gate circuit due to the charging of the gate capacitance through the resistance of the gate stripes. The low-pass characteristic of this circuit prevents rapid switching of the device. A supporting piece of evidence is that the measured gate waveforms are also practically sinusoidal, even at this high drive level. Therefore, the rather slow response of the device limits the maximum efficiency to approximately 50% which is the limit value for an unsaturated amplifier.

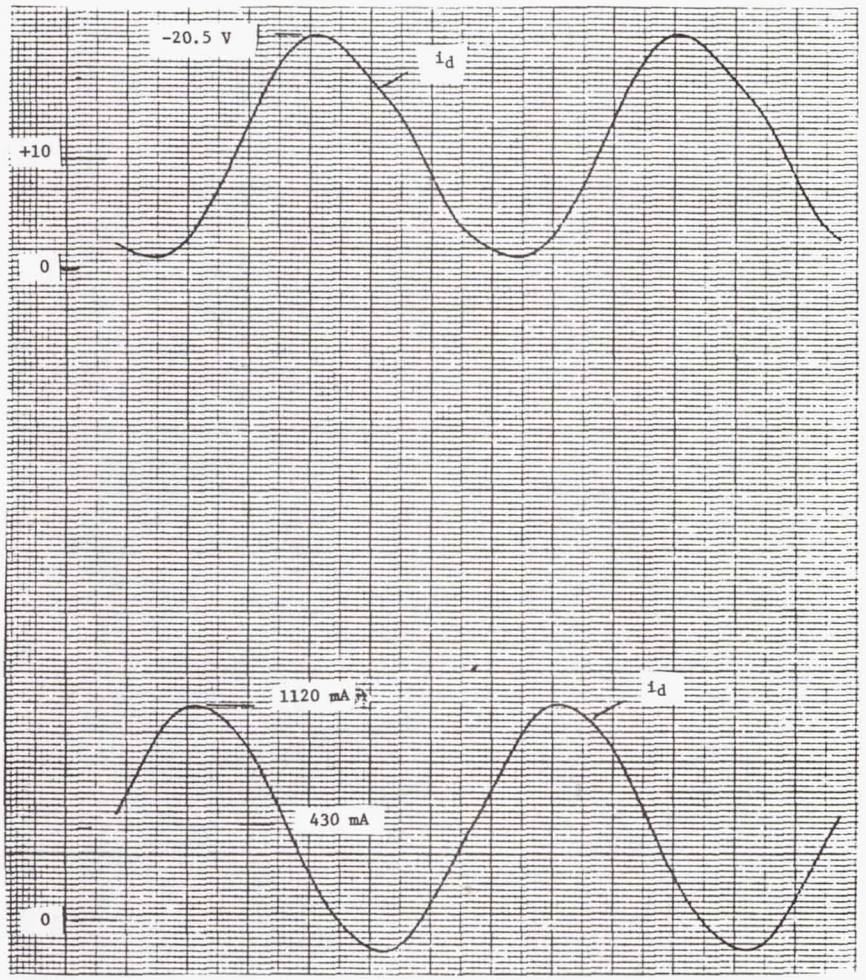

Figure 4.2-18. FLS50—Drain Waveforms, 3-dB Saturation

4.3 POWER AMPLIFIERS

4.3.1 CIRCUIT DESIGN

In view of the requirements of Phase I of this program, FLS50-type FETs were selected for the two amplifiers. The design started by measuring the load impedance for optimum efficiency and power performance, using the automatic tuner that is part of the measurement set-up. At the fundamental frequency, this optimum impedance computed at the FET pallet is $10.5 + j\,6.8\,\Omega$. The parallel equivalent resistance of this load impedance is 15 Ω, which is a value falling between the optimum impedance of an ideal Class B amplifier, equal to V_{CC}/I_S = 10 Ω for a bias voltage, V_{CC}, of 10 V and a saturated current, I_S, of 1 A, and the optimum impedance for a saturated Class B amplifier,[2] equal to $(8/\pi)(V_{CC}/I_S) = 25\,\Omega$. In accordance with the theory for the maximum efficiency case, the admittance for the even harmonics should be zero, while admittance for the odd harmonics should be infinite. These target values for the first three harmonics are listed in Table 4.3-1. The corresponding impedances were approximated by a computer-optimized microwstrip circuit, whose basic elements are two open-ended resonators for tuning the second and third harmonics, and a step transformer for adjusting the impedance ratio at the fundamental frequency. The computed values and the measured values (1) are shown in Table 4.3-1. Clearly, there is good agreement between measured (1), computed, and target values.

Table 4.3-1. FLS50—Output Circuit Impedance

FREQUENCY (GHz)	LOAD IMPEDANCE AT PALLET			
	TARGET (Ω)	COMPUTED (Ω)	MEASURED (1) (Ω)	MEASURED (2) (Ω)
2.45	10.5+j6.8	10.2+j7.6	10.4+j6.7	7.4+j6.3
4.90	∞	272+j448	196+j160	3.1+j62
7.35	0	.55-j1.5	15.9-j27	.66-j4.7

The complete amplifier was then simulated with the FET characterized by its S-parameters (Table 4.3-2), loaded by the output circuit optimized for efficiency and power. The input circuit, essentially a λ/4 transformer, was computer-optimized for highest gain at 2.45 GHz. A diagram of the microstrip circuit with dimensions of the metallization pattern, substrate thickness, and dielectric constant is shown in Figure 4.3-1. The actual circuits include high-Q, metal-oxide-metal capacitors as dc blocks, and small wire coils as RF chokes for the dc bias.

Testing of the amplifier revealed that an increase of approximately 1 dB in output power and efficiency could be obtained by readjusting the tuning of the output circuit. The circuit was then taken apart and the load impedance was remeasured and corrected for the effect of the package. The results are shown as measured values (2) in Table 4.3-1.

[2] *ibid, page 4-1*

Table 4.3-2. FLS S-Parameters

UJITSU FLS-50 #3731 9:56 AM THU., 20 MAR., 1980
VD=8 VG=-1.47

FREQ(MHZ)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2300.000	.920	-174.5	.556	138.9	.009	99.7	.934	15.4
2312.500	.920	-174.6	.553	138.9	.009	99.3	.936	15.2
2325.000	.921	-174.9	.551	138.6	.009	100.4	.935	15.0
2337.500	.922	-174.9	.551	138.5	.010	100.3	.939	14.7
2350.000	.922	-175.0	.557	138.2	.010	100.2	.938	14.7
2362.500	.922	-175.2	.559	138.1	.010	100.4	.935	14.6
2375.000	.921	-175.2	.559	138.2	.010	99.6	.938	14.4
2387.500	.921	-175.5	.561	137.9	.010	99.2	.931	14.7
2400.000	.922	-175.5	.559	137.4	.010	98.3	.928	15.2
2412.500	.920	-175.6	.569	136.5	.010	100.1	.920	15.9
2425.000	.920	-175.8	.570	135.6	.010	100.3	.917	15.6
2437.500	.918	-175.9	.566	134.8	.010	99.0	.911	17.2
2450.000	.920	-176.1	.566	134.5	.010	99.6	.911	17.0
2462.500	.918	-176.2	.565	134.4	.010	99.1	.909	18.1
2475.000	.919	-176.2	.572	134.2	.010	98.6	.907	18.1
2487.500	.920	-176.5	.566	133.2	.010	98.4	.906	17.9
2500.000	.918	-176.6	.580	132.0	.010	98.8	.905	17.3
2512.500	.921	-176.8	.581	130.9	.010	99.5	.905	16.8
2525.000	.918	-176.9	.573	130.1	.011	99.7	.901	16.1
2537.500	.917	-177.0	.572	130.1	.011	99.2	.901	15.4
2550.000	.921	-177.2	.572	130.2	.011	98.7	.899	15.0
2562.500	.918	-177.2	.579	130.2	.011	98.6	.896	14.9
2575.000	.917	-177.4	.585	129.7	.011	98.7	.892	14.9
2587.500	.917	-177.4	.587	129.0	.011	98.7	.892	14.9
2600.000	.917	-177.5	.589	128.3	.011	99.2	.896	15.1
2612.500	.917	-177.7	.586	128.0	.011	98.8	.899	15.5
2625.000	.917	-177.9	.584	127.8	.011	98.7	.901	15.6
2637.500	.919	-178.1	.585	127.6	.011	98.2	.900	15.9
2650.000	.919	-178.2	.590	127.3	.011	98.3	.902	16.3
2662.500	.918	-178.3	.594	127.0	.011	98.3	.900	16.5
2675.000	.920	-178.4	.594	126.5	.011	98.5	.902	16.9
2687.500	.916	-178.7	.594	126.0	.011	98.4	.900	17.1
2700.000	.917	-178.7	.596	125.6	.012	98.5	.902	17.2
2712.500	.919	-178.9	.599	125.3	.012	98.3	.899	17.2
2725.000	.918	-179.0	.602	124.8	.012	98.5	.898	17.0
2737.500	.918	-179.0	.604	124.3	.012	98.6	.897	16.8
2750.000	.916	-179.2	.599	124.0	.012	98.5	.897	16.4
2762.500	.913	-179.4	.598	123.8	.012	98.5	.896	16.2
2775.000	.917	-179.4	.602	124.0	.012	98.1	.894	15.9
2787.500	.913	-179.6	.609	123.8	.012	97.8	.895	15.8
2800.000	.917	-179.7	.615	123.2	.012	97.6	.891	16.0
2812.500	.915	-179.9	.618	122.3	.012	98.0	.890	16.3
2825.000	.917	179.9	.618	121.5	.012	98.4	.885	16.9
2837.500	.917	179.7	.623	121.1	.012	98.5	.879	17.3
2850.000	.916	179.7	.627	121.3	.012	98.1	.878	17.9
2862.500	.917	179.5	.630	121.5	.012	97.6	.872	18.4
2875.000	.917	179.4	.634	121.2	.012	98.5	.879	18.3
2887.500	.916	179.2	.638	120.3	.012	99.8	.885	18.9
2900.000	.911	179.1	.624	118.9	.012	101.5	.868	18.8

Table 4.3-2. FLS S-Parameters (Cont.)

[illegible]	.913	178.9	.607	117.6	[illegible]	[illegible]	.860	18.5
[illegible]	.916	178.8	.610	117.2	.012	[illegible]	.864	18.0
[illegible]	.911	178.7	.611	117.4	.013	[illegible]	.861	17.4
[illegible]	.912	178.6	.616	116.0	.013	102.6	.859	16.7
[illegible]	.910	178.5	.620	116.0	.013	102.4	.856	16.3
[illegible]	.912	178.3	.623	117.3	.013	102.5	.856	16.0
[illegible]	.912	178.2	.624	116.3	.013	103.3	.854	15.8
[illegible]	.909	178.0	.641	115.8	.013	103.9	.850	15.9
[illegible]	.912	177.9	.630	115.0	.014	104.0	.852	16.0
[illegible]	.909	177.8	.633	115.2	.014	103.6	.853	16.2
[illegible]	.910	177.5	.636	115.2	.014	103.3	.852	16.3
[illegible]	.910	177.4	.643	115.2	.014	102.9	.851	16.3
[illegible]	.909	177.3	.651	114.8	.014	103.0	.850	16.5
[illegible]	.909	177.2	.651	114.2	.014	103.1	.852	16.7
[illegible]	.910	177.0	.654	113.7	.015	103.0	.856	17.0
[illegible]	.909	176.8	.652	113.4	.015	102.9	.855	17.1
[illegible]	.905	176.7	.653	113.2	.015	102.5	.847	17.3
[illegible]	.909	176.5	.656	112.8	.015	102.7	.849	17.3
[illegible]	.909	176.4	.661	112.5	.015	101.6	.844	17.3
[illegible]	.905	176.3	.657	112.0	.015	101.6	.842	16.9
[illegible]	.907	176.1	.661	111.8	.015	101.5	.843	16.6
[illegible]	.906	175.9	.666	111.7	.015	101.1	.839	16.2
[illegible]	.905	175.8	.672	111.3	.015	100.6	.837	15.8
[illegible]	.906	175.7	.669	110.7	.016	100.9	.839	15.6
[illegible]	.904	175.4	.661	109.5	.016	101.7	.837	15.6
[illegible]	.905	175.4	.670	108.7	.016	102.1	.836	15.7
[illegible]	.906	175.1	.672	108.4	.015	101.8	.833	16.0
[illegible]	.902	175.0	.672	108.7	.017	101.5	.833	16.4
[illegible]	.903	174.8	.679	108.9	.017	101.3	.827	16.7
[illegible]	.904	174.7	.680	108.5	.017	101.2	.822	17.1
[illegible]	.902	174.5	.690	107.6	.017	101.7	.816	17.5
[illegible]	.905	174.3	.701	106.3	.017	102.3	.814	17.7

REF PLANE(s) are now: 2.150 2.150 TRANS LIN: 4.300

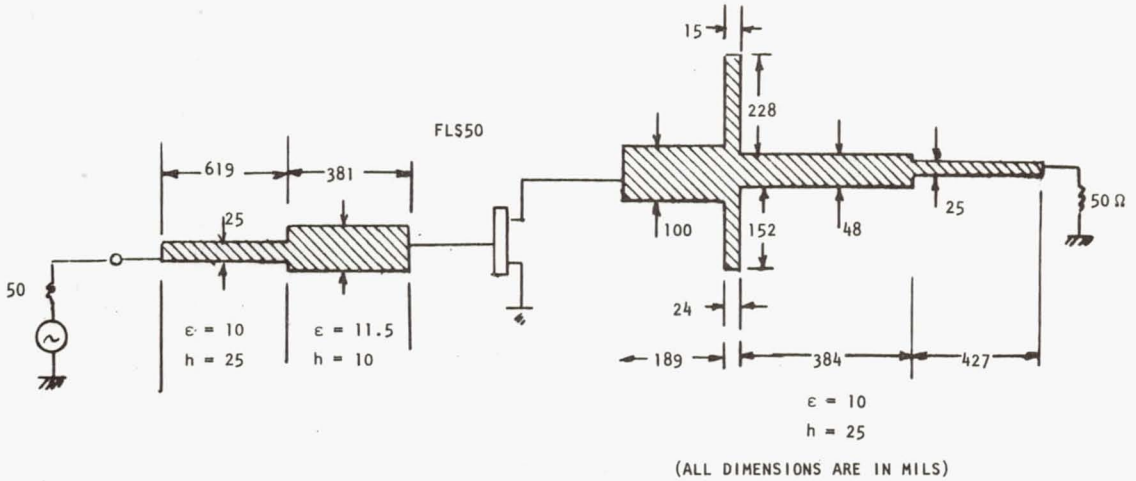

Figure 4.3-1. FLS50—Amplifier Microstrip Circuit

The load resistance at the fundamental frequency is lower than the optimum value, as previously measured—an expected result because the initial device characterization (done with tuners located far away from the device) is relatively lossy and favors lower values of transformation ratios and, in this case, higher impedances.

The impedance at the second harmonic was drastically changed. A closer analysis showed that the value of reactance is correct for resonating an output capacitance of 0.5 pF. This would result in the desired very high load impedance for the second harmonic. Although the device output capacitance is probably closer to 1.5 pF, considering the uncertain nature of the package parasitics, this result was quite encouraging. In addition, the third harmonic impedance is now close to zero, as expected from the theory. These results suggested that an optimized circuit can be designed in accordance to theory when the device capacitance and the package parasitics are properly included.

A revised method was, therefore, used for the design of the Phase II amplifiers. The FLC30-type FETs were chosen for this task because of their high operating efficiency. The design started by estimating the output capacitance of a selected device from the measurement of the device output impedance versus frequency, corrected for the effect of the output section of the package. This allowed the determination of the ideal impedance values (target) at the package terminal. The output circuit was then designed and measured; the agreement between the computed and the measured values, as shown in Table 4.3-3, is considered adequate. The design of the circuit was completed by simulating the entire circuit, with the FET characterized by the S-parameters of Table 4.3-4. A diagram of the overall microstrip circuit is depicted in Figure 4.3-2.

Table 4.3-3. FLC30—Output Circuit Impedance

FREQUENCY (GHz)	LOAD IMPEDANCE AND PACKAGE TERMINAL		
	TARGET (Ω)	COMPUTED (Ω)	MEASURED (Ω)
2.45	14+j0.10	14-j0.19	13-j1.64
4.90	0+j80	28+j71	19+j49
7.35	0+j74	40+j66	33+j52

Measurement of the amplifier showed that the output power and efficiency could still be increased somewhat by further readjusting the output circuit. However, because of time limitations and the difficulties in exactly determining the parasitic parameters of the package, no attempt was made at this time to remeasure the circuit,, correlate the results with the expected values, and redesign the microstrip circuit.

Table 4.3-4. FLC30—S-Parameters

FLC-30 S-009 11:26 AM THU. 26 JUNE, 1980
VG = 3.93 VD = +9.40 @ 150 MA

FREQ (MHz)	S11		S21		S12		S22	
2350.000	.902	-176.5	.741	43.1	.068	-16.7	.555	-168.2
2550.000	.897	-178.5	.699	39.5	.067	-18.0	.566	-170.1
4900.000	.860	153.2	.491	-11.6	.072	-48.2	.661	177.5
7350.000	.668	74.8	.608	-81.7	.092	-80.6	.629	150.4
9800.000	.791	-82.2	.443	167.7	.103	-159.4	.621	74.3
12250.000	.900	-151.3	.180	98.7	.085	156.0	.669	8.5

REF PLANE(S) ARE NOW: 2.083 2.083 TRANS LIN: 4.166

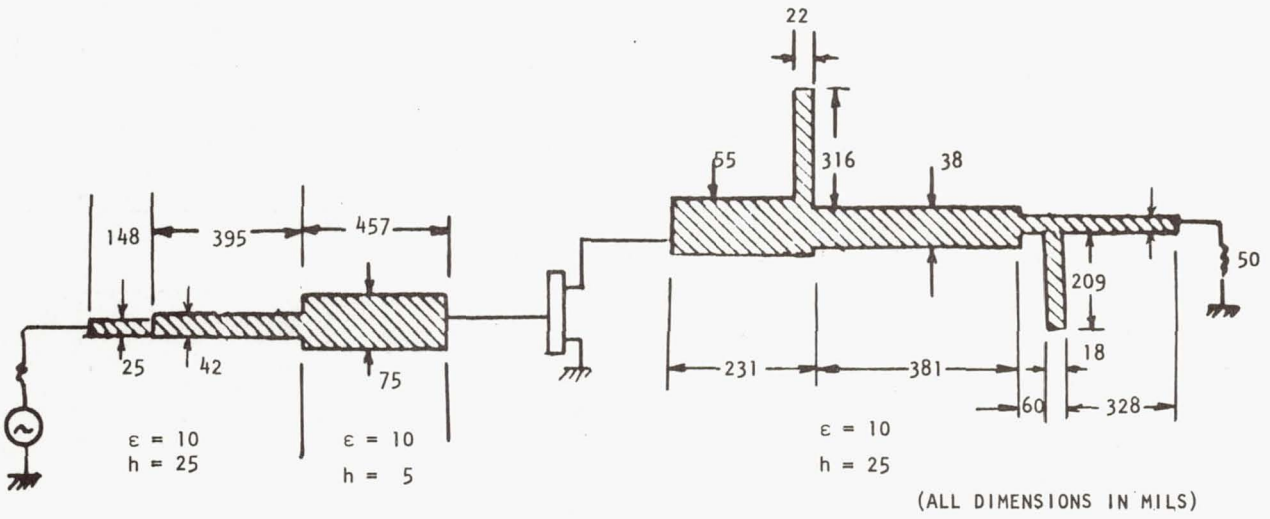

Figure 4.3-2. FLC30—Amplifier Microstrip Circuit

4.3.2 AMPLIFIER PERFORMANCE

Amplifier No. 1, shown in Figure 4.3-3, delivered an output power of 4.7 W with 53% power-added efficiency and 8.7 dB gain. Table 4.3-5 is a list of the operating parameters—drain voltage, drain current, gate voltage, gate current, input power, output power, power-added efficiency and gain—measured

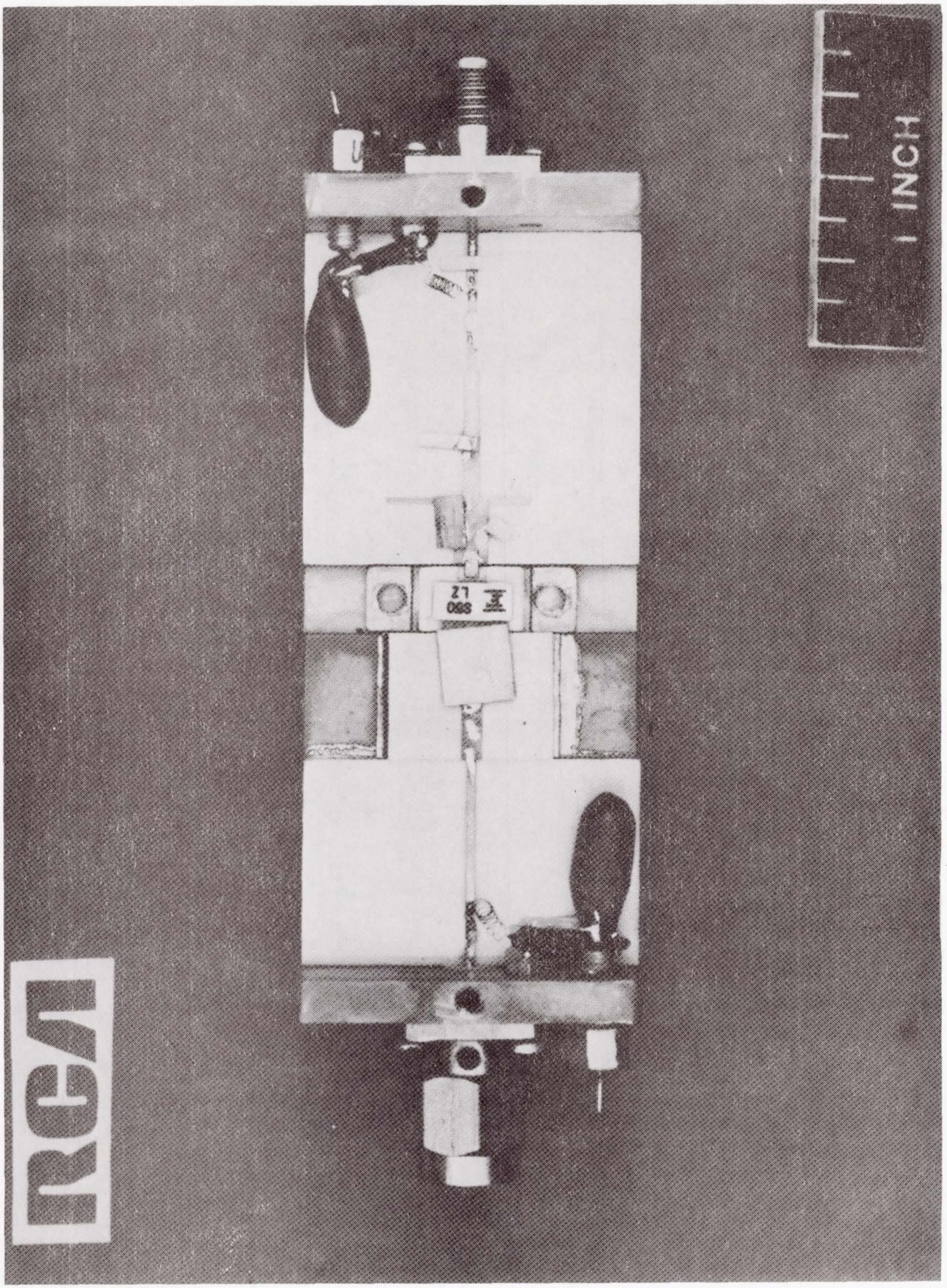

Figure 4.3-3. Amplifier No. 1 (FLS-50)

Table 4.3-5. Operating Parameters Vs. Input RF Power, Amplifier No. 1

SPS AMP.#1 RETUNED #3734,COVER ON
7:18 AM WED., 30 APR., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.97	.713	-2.47	-.710	.636	4.778	52.98	8.76
10.97	.704	-2.46	-1.82	.567	4.644	52.79	9.13
10.98	.684	-2.45	-1.87	.476	4.358	51.69	9.61
10.99	.664	-2.45	-1.85	.377	3.956	49.06	10.21
10.99	.647	-2.46	-1.84	.287	3.456	44.60	10.81
11.00	.612	-2.46	-1.82	.096	1.527	21.25	12.00
11.02	.575	-2.46	-1.81	.056	.877	12.95	11.91
11.02	.563	-2.46	-1.81	.038	.588	8.87	11.92
11.03	.560	-2.46	-1.81	.029	.446	6.75	11.93
11.02	.555	-2.46	-1.81	.019	.302	4.62	11.94
11.03	.552	-2.46	-1.82	.011	.166	2.55	11.93
11.02	.552	-2.46	-1.83	.002	.032	.49	11.84

S=70 COMMAND ?

as a function of the input RF power. As the drive level is increased from a low value to the full drive, the dc drain current increases from 552 mA to 713 mA, a change of 30%. This indicates that the device operates in a Class AB mode. The maximum efficiency is obtained at a gain of 8.7 dB, a compression of 3.3 dB with respect to the maximum gain. The gate current of -1.85 mA is the leakage current of a zener diode, connected in the gate circuit for protection against accidental over-voltages. The phase characteristic, measured as a function of the input RF drive, is shown in Figure 4.3-4. The total phase shift from zero to full drive is 13°.

The small signal performance is described by the S-parameters of Tables 4.3-6 and 4.3-7. The bandwidth is quite large—320 MHz at the 0.5 dB points. However, because of the sensitivity of the output power to mismatch, the 0.5 dB bandwidth at large drive (490 mW) is reduced to 160 MHz. Whereas the input mismatch is rather low (VSWR = 1.5), the output mismatch is quite high (VSWR = 4.0). The latter illustrates the large discrepancy that exists between the load impedance properly designed for maximum power and efficiency, and the load impedance designed, instead, for maximum gain.

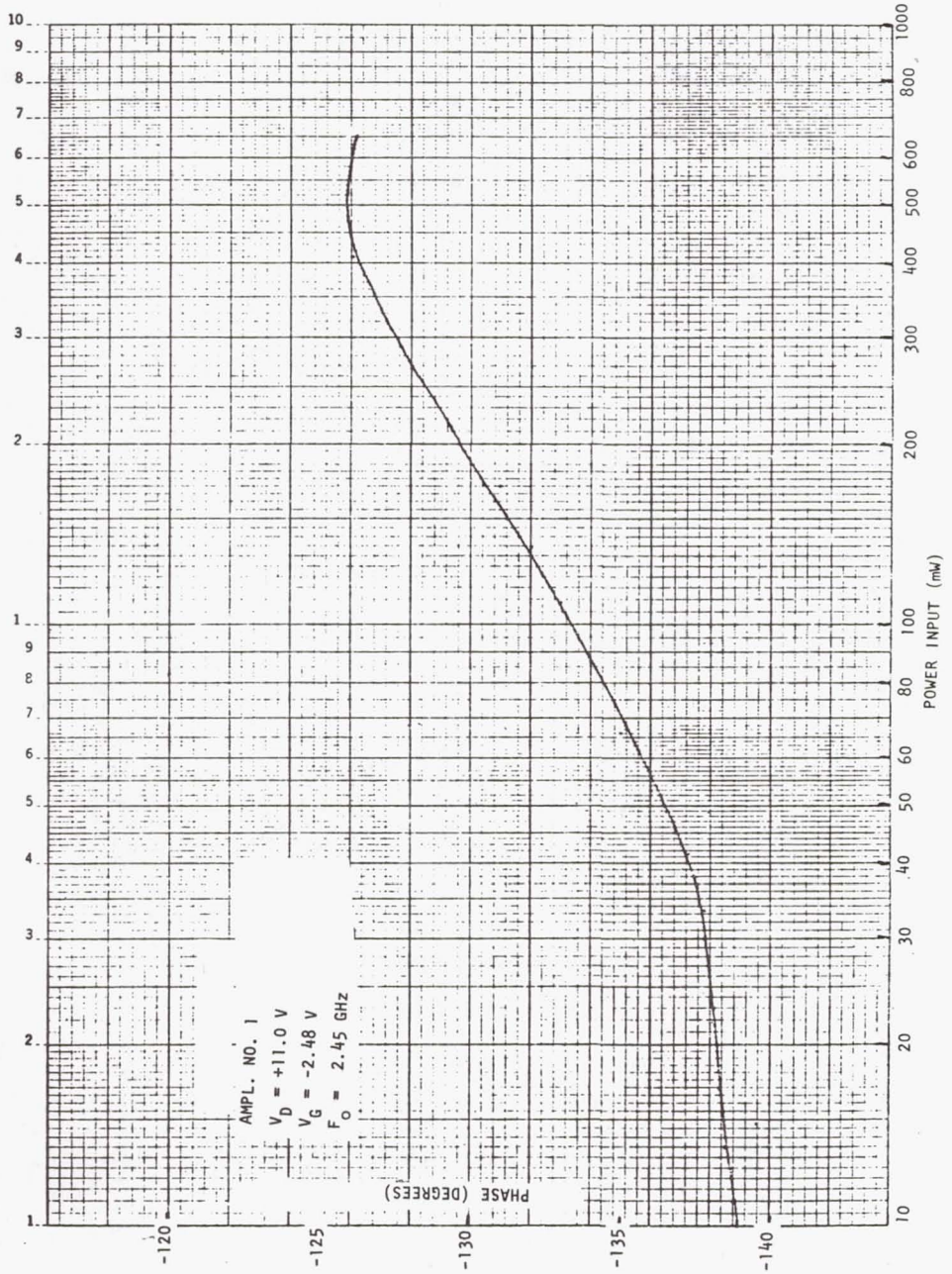

Figure 4.3-4. Phase Characteristics (Amplifier No. 1)

Table 4.3-6. S-Parameters, Amplifier No. 1, Output Port

SPS AMP #1

FREQ(MHZ)	REFL	ANGLE	RTN LS	VSWR	RGAIN(DB)	PHASE	DELAY
2000.000	.543	-170.5	-5.3	3.381	-28.5	-34.2	0.0
2020.000	.551	-175.4	-5.2	3.458	-28.2	-39.2	.7
2040.000	.561	179.3	-5.0	3.555	-28.1	-43.7	.6
2060.000	.568	174.1	-4.9	3.633	-27.9	-48.5	.7
2080.000	.577	169.3	-4.8	3.728	-27.7	-53.5	.7
2100.000	.586	164.3	-4.6	3.835	-27.6	-59.6	.9
2120.000	.595	159.2	-4.5	3.938	-27.5	-65.6	.0
2140.000	.602	154.0	-4.4	4.027	-27.4	-71.6	.8
2160.000	.608	150.7	-4.3	4.107	-27.1	-77.8	.9
2180.000	.613	146.7	-4.2	4.172	-26.9	-84.7	1.0
2200.000	.621	142.6	-4.1	4.281	-26.7	-91.0	.9
2220.000	.624	138.0	-4.1	4.322	-26.5	-96.2	.7
2240.000	.629	132.6	-4.0	4.370	-26.2	-101.5	.7
2260.000	.632	126.8	-4.0	4.433	-26.0	-107.3	.8
2280.000	.632	122.0	-4.0	4.434	-25.9	-113.0	.8
2300.000	.633	118.3	-4.0	4.451	-25.7	-118.2	.7
2320.000	.633	114.7	-4.0	4.443	-25.5	-124.1	.8
2340.000	.634	110.8	-4.0	4.463	-25.4	-130.4	.9
2360.000	.633	106.6	-4.0	4.448	-25.3	-136.4	.8
2380.000	.627	102.2	-4.0	4.367	-25.1	-143.0	.9
2400.000	.626	97.4	-4.1	4.345	-25.0	-150.0	1.0
2420.000	.620	92.9	-4.2	4.264	-24.9	-156.8	.9
2440.000	.609	88.8	-4.3	4.114	-24.7	-163.2	.9
2460.000	.598	86.0	-4.5	3.970	-24.6	-169.8	.9
2480.000	.586	83.0	-4.6	3.833	-24.6	-176.6	.9
2500.000	.575	79.9	-4.8	3.702	-24.7	177.3	.8
2520.000	.561	75.9	-5.0	3.560	-24.6	170.8	.9
2540.000	.546	71.3	-5.3	3.403	-24.7	163.3	1.0
2560.000	.532	66.9	-5.5	3.271	-24.9	155.9	1.0
2580.000	.514	63.2	-5.8	3.117	-24.9	149.1	.9
2600.000	.498	60.5	-6.1	2.984	-24.8	142.3	1.0
2620.000	.483	57.9	-6.3	2.871	-24.8	134.5	1.1
2640.000	.466	55.8	-6.6	2.748	-25.0	128.1	.9
2660.000	.449	53.8	-7.0	2.628	-25.1	122.3	.7
2680.000	.433	51.6	-7.3	2.525	-25.1	116.7	.9
2700.000	.415	48.7	-7.6	2.419	-25.2	109.8	1.0
2720.000	.401	46.0	-7.9	2.339	-25.5	103.4	.9
2740.000	.386	44.2	-8.3	2.257	-25.7	97.6	.8
2760.000	.371	42.8	-8.6	2.182	-25.8	91.8	.8
2780.000	.357	42.3	-9.0	2.109	-25.9	84.6	1.0
2800.000	.343	41.9	-9.3	2.043	-26.2	77.5	1.0
2820.000	.330	41.3	-9.6	1.985	-26.4	71.3	.8
2840.000	.320	39.9	-9.9	1.941	-26.5	66.3	.8
2860.000	.310	38.8	-10.2	1.897	-26.6	60.5	.8
2880.000	.300	37.9	-10.5	1.858	-26.7	55.2	.7
2900.000	.291	37.5	-10.7	1.820	-26.9	49.5	.8
2920.000	.283	37.4	-11.0	1.791	-27.3	45.2	.6
2940.000	.276	37.9	-11.2	1.763	-27.5	40.8	.6
2960.000	.270	38.9	-11.4	1.741	-27.6	35.9	.7
2980.000	.266	38.7	-11.5	1.724	-27.9	29.8	.8

Table 4.3-7. S-Parameters, Amplifier No. 1, Input Port

SPS AMP #1

FREQ(MHZ)	REFL	ANGLE	RTN LS	VSWR	FGAIN(DB)	PHASE	DELAY
2000.000	.715	-152.0	-2.9	6.009	9.1	-3.5	0.0
2020.000	.701	-157.2	-3.1	5.682	9.2	-8.9	.8
2040.000	.690	-162.7	-3.2	5.444	9.3	-14.8	.8
2060.000	.674	-168.1	-3.4	5.130	9.5	-20.7	.8
2080.000	.658	-173.7	-3.6	4.854	9.5	-26.2	.8
2100.000	.644	-179.4	-3.8	4.622	9.6	-31.5	.7
2120.000	.623	174.9	-4.1	4.312	9.8	-38.2	.9
2140.000	.604	168.3	-4.4	4.045	10.0	-45.1	1.0
2160.000	.583	162.9	-4.7	3.801	9.9	-52.0	1.0
2180.000	.562	156.7	-5.0	3.571	10.0	-58.8	.9
2200.000	.541	150.4	-5.3	3.357	10.3	-66.0	1.0
2220.000	.515	143.7	-5.8	3.127	10.4	-73.2	1.0
2240.000	.489	136.7	-6.2	2.910	10.4	-79.8	.9
2260.000	.462	129.7	-6.7	2.719	10.5	-85.8	.8
2280.000	.435	122.0	-7.2	2.539	10.7	-91.6	.8
2300.000	.406	113.8	-7.8	2.366	10.7	-97.9	.9
2320.000	.377	105.2	-8.5	2.212	10.8	-104.3	.9
2340.000	.348	95.8	-9.2	2.069	10.9	-111.0	.9
2360.000	.319	85.2	-9.9	1.937	11.0	-117.9	1.0
2380.000	.290	73.5	-10.8	1.817	11.0	-124.8	1.0
2400.000	.264	60.3	-11.6	1.718	11.0	-131.5	.9
2420.000	.242	45.1	-12.3	1.639	11.1	-139.2	1.1
2440.000	.226	28.0	-12.9	1.585	11.1	-146.9	1.1
2460.000	.219	9.4	-13.2	1.562	11.0	-154.0	1.0
2480.000	.222	-9.8	-13.1	1.570	11.0	-160.9	1.0
2500.000	.234	-28.2	-12.6	1.612	11.0	-167.9	1.0
2520.000	.256	-44.6	-11.8	1.689	10.9	-175.1	1.0
2540.000	.283	-59.1	-11.0	1.791	10.8	178.0	1.0
2560.000	.315	-71.8	-10.0	1.919	10.7	170.4	1.1
2580.000	.348	-83.8	-9.2	2.069	10.7	161.7	1.2
2600.000	.386	-94.0	-8.3	2.256	10.4	153.8	1.1
2620.000	.421	-103.7	-7.5	2.456	10.2	146.7	1.0
2640.000	.458	-112.8	-6.8	2.691	10.2	139.7	1.0
2660.000	.493	-121.2	-6.1	2.948	10.0	132.2	1.0
2680.000	.526	-129.3	-5.6	3.219	9.7	125.6	.9
2700.000	.559	-137.1	-5.1	3.531	9.5	119.4	.9
2720.000	.590	-144.8	-4.6	3.873	9.4	112.7	.9
2740.000	.620	-152.0	-4.1	4.269	9.2	105.4	1.0
2760.000	.649	-159.0	-3.8	4.696	8.9	98.2	1.0
2780.000	.673	-165.7	-3.4	5.120	8.6	91.8	.9
2800.000	.693	-172.3	-3.1	5.631	8.4	85.1	.9
2820.000	.717	-178.6	-2.9	6.072	8.2	78.1	1.0
2840.000	.741	175.1	-2.6	6.728	7.9	70.5	1.1
2860.000	.758	169.3	-2.4	7.261	7.6	64.2	.9
2880.000	.775	163.5	-2.2	7.891	7.3	59.7	.8
2900.000	.792	158.0	-2.0	8.631	7.1	53.4	.7
2920.000	.807	152.7	-1.9	9.357	6.9	47.8	.8
2940.000	.815	147.3	-1.8	9.814	6.6	41.6	.8
2960.000	.828	142.2	-1.6	10.645	6.3	36.1	.8
2980.000	.839	137.3	-1.5	11.445	5.9	30.2	.8

The harmonic content of the output signal was also measured by a broadband spectrum analyzer, and the results are depicted in Figure 4.3-5. The maximum level is reached by the second harmonic, 24 dB below the 5-W fundamental signal. The amplifier small signal noise figure, measured at 2.45 GHz, is 3.28 dB, a value which is considered quite low for a high-power device.

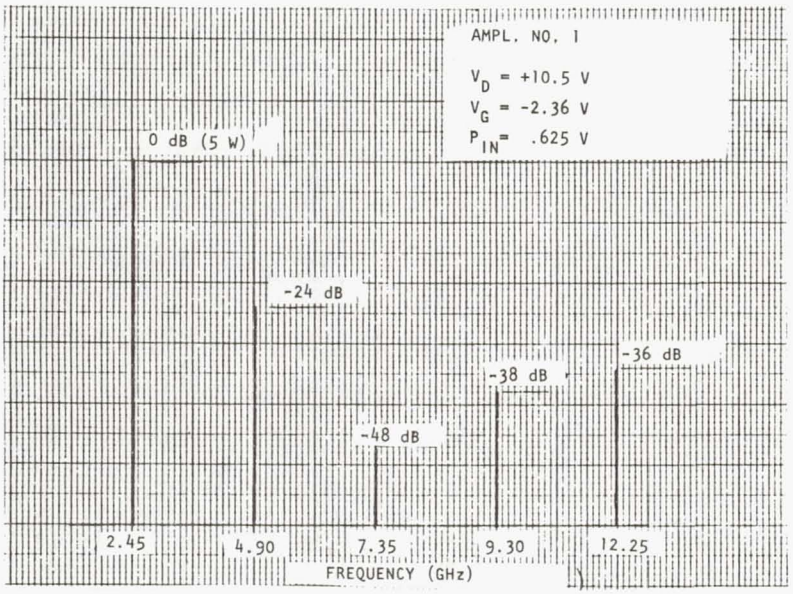

Figure 4.3-5. Harmonic Output—Amplifier No. 1

Similar measurements were performed on Amplifier No. 2, and the results are listed in Tables 4.3-8 and Figure 4.3-6. The amplifier delivered 5.1 W output power with 51% efficiency and 7.8 dB gain. This amplifier also operates in a Class AB mode, with the drain current changing by a factor of 2.2 from zero to full RF drive. The phase characteristic versus RF drive (Figure 4.3-6) is similar to that of Amplifier No. 1. The total phase shift is 18°, not very different from the 13° of Amplifier No. 1. No attempt was made toward matching the phases of the two amplifiers. The small signal noise figure of Amplifier No. 2 is 3.96 dB.

Amplifiers No. 3 and No. 4 were designed around higher efficiency but lower power FLC30-type devices. The performance of Amplifier No. 3 is described in Tables 4.3-9 through 4.3-11. The maximum efficiency is 61.8%, achieved at an output power of 2.37 W and a gain of 9.27 dB. The mode of operation is Class AB. The maximum phase shift at large RF drive is 15° (Table 4.3-9). The AM/PM conversion has a first peak at 1.24°/dB, reaching a value of 5.13°/dB at the maximum RF drive. The small signal noise figure is 4.35 dB.

The performance of Amplifier No. 4 is described in Tables 4.3-12 through 4.3-14. This amplifier features the highest efficiency—71.9% at an output power of 1.27 W and a gain of 8 dB. This value of power-added efficiency is, to our knowledge, unsurpassed by any solid-state device operating in the same frequency range. The mode of operation of this amplifier is Class AB, with a 2.6:1 change in drain current. The total phase shift is 22° and the peak of the AM/PM conversion is -3.0°/dB. The small signal noise figure is 6.5 dB.

Table 4.3-8. Operating Parameters Vs. Input RF Power
(Amplifier No. 2)

SPS AMP#2 #3732 3-HARM.TNG.
8:20 AM THU., 1 MAY , 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.98	.761	-3.14	0.000	.849	5.162	51.58	7.84
10.98	.759	-3.14	0.000	.801	5.081	51.39	8.03
10.98	.756	-3.14	0.000	.783	5.037	51.26	8.09
10.98	.750	-3.14	0.000	.755	4.956	51.01	8.17
10.99	.730	-3.14	0.000	.657	4.572	48.81	8.42
11.00	.704	-3.14	0.000	.562	4.135	46.13	8.67
11.01	.675	-3.14	0.000	.473	3.688	43.24	8.92
11.03	.641	-3.14	0.000	.384	3.170	39.42	9.17
11.04	.595	-3.14	0.000	.293	2.509	33.75	9.32
11.07	.517	-3.14	0.000	.194	1.715	26.55	9.46
11.10	.434	-3.14	0.000	.103	.929	17.15	9.56
11.12	.382	-3.14	0.000	.048	.439	9.22	9.66
11.12	.356	-3.14	0.000	.023	.215	4.86	9.76
11.13	.339	-3.14	0.000	.002	.023	.53	9.83
11.13	.339	-3.14	0.000	DC TEST ONLY			

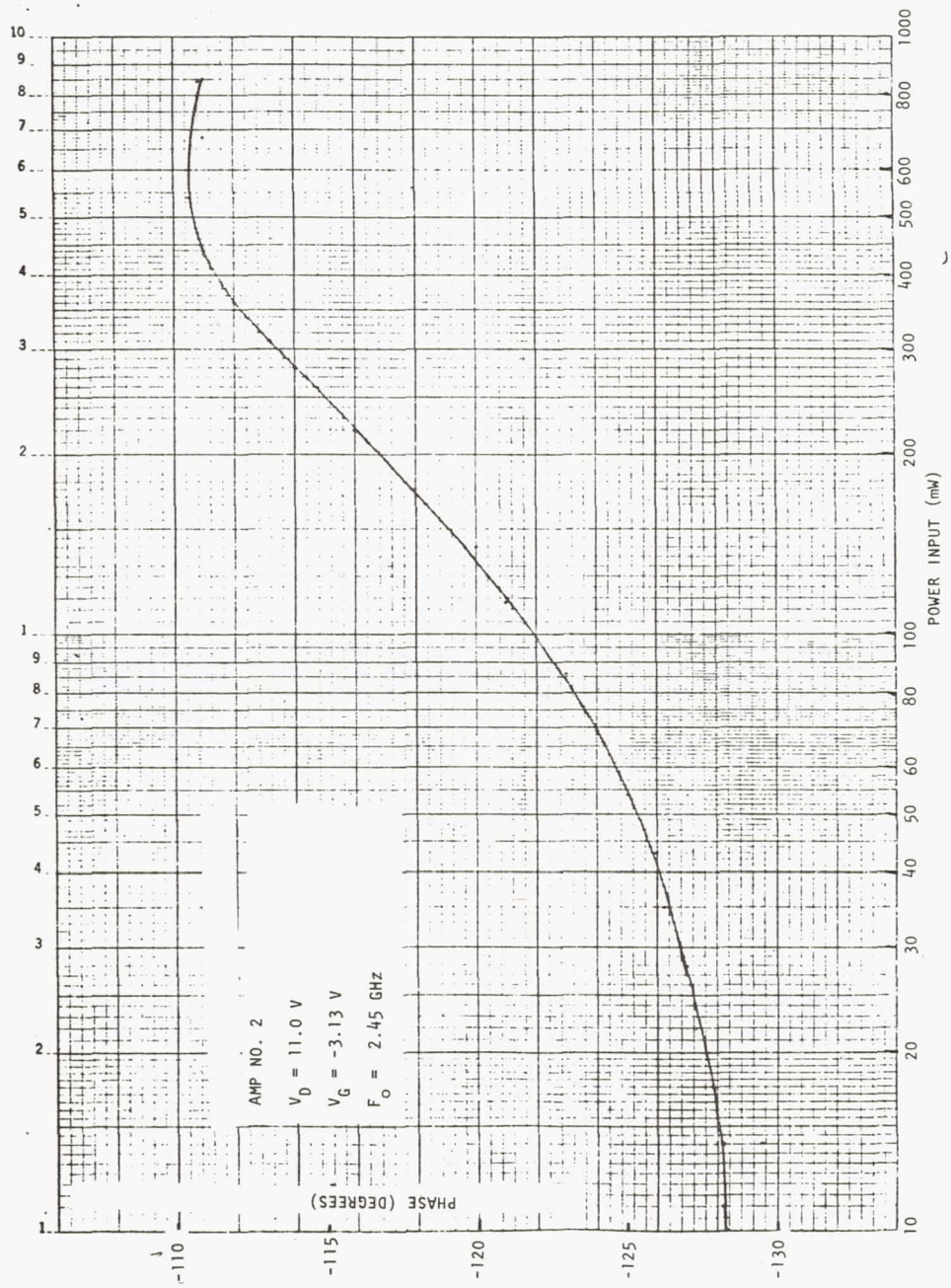

Figure 4.3-6. Phase Characteristics—Amplifier No. 2

Table 4.3-9. Amplifier No. 3 P-Out and Efficiency Vs. P-In

DRAIN VOLT.	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
8.41	.414	-3.36	1.520	.304	2.436	61.26	9.04
8.41	.402	-3.38	.370	.280	2.372	51.83	9.27
8.41	.399	-3.39	.240	.260	2.308	60.99	9.49
8.42	.394	-3.39	.130	.238	2.235	60.27	3.73
8.42	.385	-3.39	.080	.208	2.126	59.15	10.09
8.42	.379	-3.39	.050	.186	2.026	57.59	10.36
8.42	.374	-3.39	.030	.164	1.916	55.69	10.66
8.42	.368	-3.39	.010	.144	1.788	53.11	10.95
8.43	.356	-3.39	0.000	.120	1.615	49.78	11.30
8.43	.342	-3.39	0.000	.096	1.387	44.78	11.50
8.44	.316	-3.39	0.000	.071	1.068	37.35	11.76
8.45	.287	-3.39	0.000	.050	.749	28.81	11.80
8.46	.250	-3.39	0.000	.025	.385	17.01	11.83
8.47	.227	-3.39	0.000	.010	.146	7.05	11.83
8.47	.221	-3.39	0.000	.003	.047	2.32	11.83

Table 4.3-10. Amplifier No. 3 P-Out, Gain, Phase and AM/PM Conversion Vs. P-In

PIN(MW)	MSPAR	PHASE	GAIN(DB)	PO(MW)	AM/PM	PO(DBM)
.29	4.246	93.4	12.58	5.27	0.00	7.21
.39	4.241	93.4	12.55	7.00	-.04	8.45
.48	4.243	93.6	12.55	8.71	.25	9.40
.61	4.235	93.8	12.54	10.85	.14	10.35
.75	4.241	93.9	12.55	13.52	.15	11.31
.96	4.233	94.0	12.53	17.15	.13	12.34
1.20	4.238	94.2	12.54	21.47	.16	13.32
1.50	4.243	94.5	12.55	27.01	.32	14.31
1.86	4.241	94.7	12.55	33.45	.22	15.24
2.35	4.240	95.0	12.55	42.26	.27	16.26
2.93	4.235	95.2	12.54	52.56	.24	17.21
3.89	4.251	95.6	12.57	70.31	.31	18.47
4.86	4.247	96.1	12.56	87.64	.48	19.43
6.06	4.249	96.7	12.57	109.39	.63	20.39
7.56	4.249	97.3	12.57	136.50	.65	21.35
9.61	4.246	98.0	12.56	173.29	.73	22.39
12.00	4.248	98.8	12.56	216.59	.76	23.36
15.00	4.253	99.6	12.59	272.57	.85	24.35
18.70	4.268	100.7	12.60	340.64	1.13	25.32
23.70	4.263	101.8	12.59	430.74	1.05	26.34
29.50	4.262	102.9	12.59	535.92	1.24	27.29
39.70	4.246	104.5	12.56	715.79	1.22	28.55
49.70	4.232	105.5	12.53	896.16	1.07	29.49
61.50	4.209	106.4	12.48	1089.26	.89	30.37
76.90	4.122	107.1	12.30	1308.82	.77	31.16
97.80	3.958	107.7	11.95	1532.16	.59	31.85
122.00	3.755	108.2	11.49	1720.26	.53	32.36
152.00	3.540	108.3	10.98	1904.93	.01	32.80
191.00	3.299	107.7	10.37	2078.49	-.53	33.18
242.00	3.049	104.9	9.68	2249.22	-2.79	33.52
303.00	2.818	99.9	9.00	2405.45	-5.13	33.81

Table 4.3-11. Amplifier No. 3 Small Signal S- Parameters

11:02 AM WED., 23 JULY, 1980

SPS AMP#3 VG=-3.39 VD=+8.48 @ 224MA.

FREQ(MHZ)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000.000	.749	59.1	2.928	-69.8	.144	-132.5	.212	155.3
2050.000	.736	44.4	2.886	-86.7	.144	-148.8	.229	141.6
2100.000	.719	30.4	2.884	-103.1	.146	-166.0	.259	127.3
2150.000	.694	16.7	2.889	-120.2	.153	177.1	.297	111.7
2200.000	.659	2.8	2.988	-138.8	.160	159.9	.343	94.5
2250.000	.599	-12.7	3.142	-157.8	.172	140.8	.395	75.6
2300.000	.503	-30.6	3.354	-179.8	.190	120.9	.454	52.5
2350.000	.360	-54.3	3.639	155.3	.210	98.1	.509	22.7
2400.000	.156	-107.4	3.923	127.1	.229	69.4	.559	-17.3
2450.000	.271	117.1	3.866	93.4	.235	34.9	.586	-67.9
2500.000	.585	72.2	3.301	57.1	.201	-.2	.590	-123.4
2550.000	.787	42.5	2.529	25.4	.150	-31.3	.599	-173.9
2600.000	.877	21.1	1.783	.9	.110	-56.3	.629	148.7
2650.000	.917	5.1	1.287	-21.6	.081	-73.9	.659	121.6
2700.000	.932	-8.0	.962	-38.5	.059	-90.0	.691	100.6
2750.000	.934	-19.0	.709	-54.1	.046	-104.2	.722	83.6
2800.000	.941	-28.8	.549	-67.7	.035	-116.5	.753	69.2
2850.000	.936	-37.7	.425	-79.1	.028	-130.1	.777	56.4
2900.000	.937	-45.7	.333	-91.9	.022	-140.4	.800	45.0
2950.000	.937	-53.5	.272	-102.5	.018	-152.4	.819	34.4
3000.000	.938	-60.6	.215	-113.1	.015	-163.2	.840	24.7

REF PLANE(s) are now: 0.000 0.000 TRANS LIN: 0.000

11:02 AM WED., 23 JULY, 1980

SPS AMP#3 VG=-3.39 VD=+8.48 @ 224MA.

FREQ(MHZ)	S11		S21		S12		S22	
	DB	ANG	DB	ANG	DB	ANG	DB	ANG
2000.000	-2.51	59.1	9.33	-69.8	-16.86	-132.5	-13.49	155.3
2050.000	-2.66	44.4	9.21	-86.7	-16.83	-148.8	-12.81	141.6
2100.000	-2.86	30.4	9.20	-103.1	-16.69	-166.0	-11.74	127.3
2150.000	-3.17	16.7	9.22	-120.2	-16.32	177.1	-10.56	111.7
2200.000	-3.62	2.8	9.51	-138.8	-15.90	159.9	-9.30	94.5
2250.000	-4.45	-12.7	9.94	-157.8	-15.27	140.8	-8.07	75.6
2300.000	-5.97	-30.6	10.51	-179.8	-14.41	120.9	-6.86	52.5
2350.000	-8.88	-54.3	11.22	155.3	-13.56	98.1	-5.86	22.7
2400.000	-16.13	-107.4	11.87	127.1	-12.80	69.4	-5.06	-17.3
2450.000	-11.35	117.1	11.75	93.4	-12.58	34.9	-4.64	-67.9
2500.000	-4.65	72.2	10.37	57.1	-13.93	-.2	-4.58	-123.4
2550.000	-2.08	42.5	8.06	25.4	-16.48	-31.3	-4.45	-173.9
2600.000	-1.14	21.1	5.02	.9	-19.11	-56.3	-4.03	148.7
2650.000	-.76	5.1	2.19	-21.6	-21.81	-73.9	-3.62	121.6
2700.000	-.62	-8.0	-.34	-38.5	-24.57	-90.0	-3.21	100.6
2750.000	-.59	-19.0	-2.98	-54.1	-26.73	-104.2	-2.83	83.6
2800.000	-.53	-28.8	-5.21	-67.7	-29.09	-116.5	-2.46	69.2
2850.000	-.57	-37.7	-7.44	-79.1	-31.07	-130.1	-2.19	56.4
2900.000	-.56	-45.7	-9.54	-91.9	-32.96	-140.4	-1.94	45.0
2950.000	-.56	-53.5	-11.32	-102.5	-34.90	-152.4	-1.74	34.4
3000.000	-.55	-60.6	-13.36	-113.1	-36.40	-163.2	-1.52	24.7

REF PLANE(s) are now: 0.000 0.000 TRANS LIN: 0.000

Table 4.3-12. Amplifier No. 4 P-Out and Efficiency Vs. P-In

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.98	.135	-4.20	0.000	.202	1.268	71.93	7.99
10.98	.135	-4.20	0.000	.196	1.259	71.70	8.08
10.98	.135	-4.20	0.000	.165	1.204	70.06	8.62
10.98	.132	-4.20	0.000	.143	1.150	69.38	9.06
10.98	.129	-4.20	0.000	.119	1.058	66.17	9.50
10.98	.124	-4.20	0.000	.095	.931	61.59	9.91
10.98	.115	-4.20	0.000	.076	.784	56.07	10.13
10.99	.103	-4.20	0.000	.058	.579	45.89	10.02
10.99	.083	-4.20	0.000	.038	.342	33.21	9.54
11.00	.063	-4.20	0.000	.020	.146	18.18	8.72
11.01	.055	-4.20	0.000	.010	.068	9.60	8.28
11.00	.052	-4.20	0.000	.005	.029	4.32	8.01
11.01	.052	-4.20	0.000	DC TEST ONLY			

Table 4.3-13. Amplifier No. 4 P-Out, Gain, Phase, and AM/PM Conversion Vs. P-In

TEST CAL GAIN(DB)= 13
REL GAIN= 3.1623
AT A TEST FREQUENCY OF: 2.4 GHZ
2:45 PM TUE.. 22 JULY, 1980

PIN(MW)	MSPAR	PHASE	GAIN(DB)	PO(MW)	AM/PM	PO(DBM)
1.97	2.517	126.6	8.02	12.48	0.00	10.96
2.60	2.516	126.6	8.02	16.46	.05	12.17
3.25	2.517	126.6	8.02	20.59	-.03	13.14
4.05	2.523	126.6	8.04	25.78	-.02	14.11
5.05	2.531	126.4	8.07	32.36	-.13	15.10
6.43	2.540	126.4	8.10	41.49	-.09	16.18
8.02	2.554	126.1	8.14	52.31	-.21	17.19
10.03	2.573	125.8	8.21	66.40	-.33	18.22
12.50	2.593	125.5	8.28	84.08	-.37	19.25
15.80	2.633	124.9	8.41	109.56	-.64	20.40
19.70	2.682	124.3	8.57	141.69	-.58	21.51
26.50	2.759	122.8	8.81	201.67	-1.14	23.05
33.10	2.840	121.3	9.07	266.91	-1.51	24.26
41.00	2.919	119.4	9.30	349.27	-2.10	25.43
51.00	3.013	117.0	9.58	462.93	-2.49	26.65
65.40	3.093	114.0	9.81	625.70	-2.83	27.96
81.50	3.118	111.1	9.88	792.12	-3.05	28.99
101.60	3.049	108.5	9.68	944.29	-2.68	29.75
126.00	2.913	106.6	9.29	1068.91	-2.07	30.29
161.00	2.713	105.3	8.67	1184.99	-1.20	30.74
201.00	.2.507	104.5	7.98	1263.68	-.76	31.02

Table 4.3-14. Amplifier No. 4 Small Signal S-Parameters

11:08 AM WED., 23 JULY, 1980

SPS AMP#4 VG=-4.20 VD=+11.01 @ 52MA.

FREQ(MHZ)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000.000	.867	89.1	1.518	-58.5	.118	-117.3	.453	-146.8
2050.000	.871	72.8	1.491	-76.4	.116	-133.9	.444	-163.3
2100.000	.873	58.0	1.485	-92.9	.115	-151.5	.440	179.7
2150.000	.865	44.1	1.460	-110.0	.119	-168.0	.436	162.4
2200.000	.860	30.9	1.512	-127.4	.129	175.1	.436	144.9
2250.000	.839	17.6	1.564	-144.6	.139	157.5	.431	126.7
2300.000	.800	3.5	1.687	-164.2	.153	140.4	.421	107.1
2350.000	.737	-12.4	1.884	175.0	.172	120.7	.395	83.9
2400.000	.621	-32.8	2.155	150.0	.205	97.1	.338	50.8
2450.000	.370	-62.8	2.520	118.3	.244	66.1	.250	-12.3
2500.000	.103	119.5	2.618	76.9	.256	24.0	.328	-115.6
2550.000	.531	57.7	2.102	33.9	.203	-18.7	.536	175.9
2600.000	.751	28.7	1.426	.9	.141	-51.6	.645	137.8
2650.000	.842	9.8	.973	-25.9	.098	-73.8	.693	113.6
2700.000	.881	-4.4	.692	-46.0	.069	-93.8	.724	95.8
2750.000	.894	-15.9	.494	-63.4	.051	-110.1	.749	81.5
2800.000	.908	-25.7	.369	-80.8	.037	-125.5	.775	69.3
2850.000	.913	-34.8	.275	-95.3	.028	-142.2	.800	58.1
2900.000	.917	-42.9	.205	-111.4	.022	-156.2	.828	47.6
2950.000	.920	-50.7	.156	-125.7	.016	-171.8	.852	37.4
3000.000	.923	-58.1	.114	-140.3	.013	174.3	.872	27.7

REF PLANE(s) are now: 0.000 0.000 TRANS LIN: 0.000

11:08 AM WED., 23 JULY, 1980

SPS AMP#4 VG=-4.20 VD=+11.01 @ 52MA.

FREQ(MHZ)	S11		S21		S12		S22	
	DB	ANG	DB	ANG	DB	ANG	DB	ANG
2000.000	-1.24	89.1	3.62	-58.5	-18.59	-117.3	-6.87	-146.8
2050.000	-1.20	72.8	3.47	-76.4	-18.73	-133.9	-7.05	-163.3
2100.000	-1.18	58.0	3.43	-92.9	-18.77	-151.5	-7.13	179.7
2150.000	-1.25	44.1	3.29	-110.0	-18.46	-168.0	-7.20	162.4
2200.000	-1.31	30.9	3.59	-127.4	-17.78	175.1	-7.21	144.9
2250.000	-1.52	17.6	3.89	-144.6	-17.12	157.5	-7.32	126.7
2300.000	-1.94	3.5	4.54	-164.2	-16.32	140.4	-7.51	107.1
2350.000	-2.64	-12.4	5.50	175.0	-15.29	120.7	-8.07	83.9
2400.000	-4.14	-32.8	6.67	150.0	-13.75	97.1	-9.43	50.8
2450.000	-8.63	-62.8	8.03	118.3	-12.24	66.1	-12.03	-12.3
2500.000	-19.72	119.5	8.36	76.9	-11.82	24.0	-9.67	-115.6
2550.000	-5.50	57.7	6.45	33.9	-13.84	-18.7	-5.42	175.9
2600.000	-2.49	28.7	3.08	.9	-17.00	-51.6	-3.81	137.8
2650.000	-1.50	9.8	-.24	-25.9	-20.16	-73.8	-3.18	113.6
2700.000	-1.10	-4.4	-3.20	-46.0	-23.20	-93.8	-2.80	95.8
2750.000	-.97	-15.9	-6.12	-63.4	-25.92	-110.1	-2.51	81.5
2800.000	-.84	-25.7	-8.66	-80.8	-28.62	-125.5	-2.21	69.3
2850.000	-.79	-34.8	-11.23	-95.3	-30.97	-142.2	-1.94	58.1
2900.000	-.76	-42.9	-13.77	-111.4	-33.34	-156.2	-1.64	47.6
2950.000	-.72	-50.7	-16.12	-125.7	-35.84	-171.8	-1.39	37.4
3000.000	-.70	-58.1	-18.84	-140.3	-38.04	174.3	-1.19	27.7

REF PLANE(s) are now: 0.000 0.000 TRANS LIN: 0.000

A summary of the most significant results, together with the pertinent specifications, are listed in Tables 4.3-15 and 4.3-16.

Table 4.3-15. Summary of Amplifiers' Performance—Phase I

	UNITS	SPECS	AMPLIFIER NO. 1	AMPLIFIER NO. 2
POWER OUTPUT	W	5.0	4.7	5.1
EFFICIENCY (POWER ADDED)	%	50	53	51
GAIN	dB	8	8.7	7.8
MAXIMUM PHASE SHIFT	DEG	-	13	18
AM/PM CONVERSION	°/dB	-	1.5	2.1
HARMONIC OUTPUT	dB_C	-	24	-
SMALL SIGNAL NOISE FIGURE	dB	-	3.28	3.96

Table 4.3-16. Summary of Amplifiers' Performance—Phase II

	UNITS	SPECS	AMPLIFIER NO. 3	AMPLIFIER NO. 4
POWER OUTPUT	W	(10)	2.37	1.27
EFFICIENCY (POWER ADDED)	%	65	61.8	71.9
GAIN	dB	10	9.3	8.0
MAXIMUM PHASE SHIFT	DEG	-	15	22
AM/PM CONVERSION	°/dB	-	5.1	3.0
SMALL SIGNAL NOISE FIGURE	dB	-	4.3	6.5

5.0 ANTENNA DEVELOPMENT

5.1 APPROACH

The antenna configuration was selected to be compatible with the designs proposed in the solid-state antenna subtask of the Microwave Power Transmission Subsystem study (Task 1.2.3 of Exhibit D, NAS 8-32475). Two variations of an antenna concept proposed for the solid-state "sandwich" are shown in Figures 5.1-1 and 5.1-2. Accordingly, the antenna selected is a two dimensional array of dipoles. In this case, the dipoles are etched on circuit board. The receiving antenna is identical to the transmitting antenna with respect to construction and array elements. The associated circuitry includes RF rectification and provides a dc powered LED display.

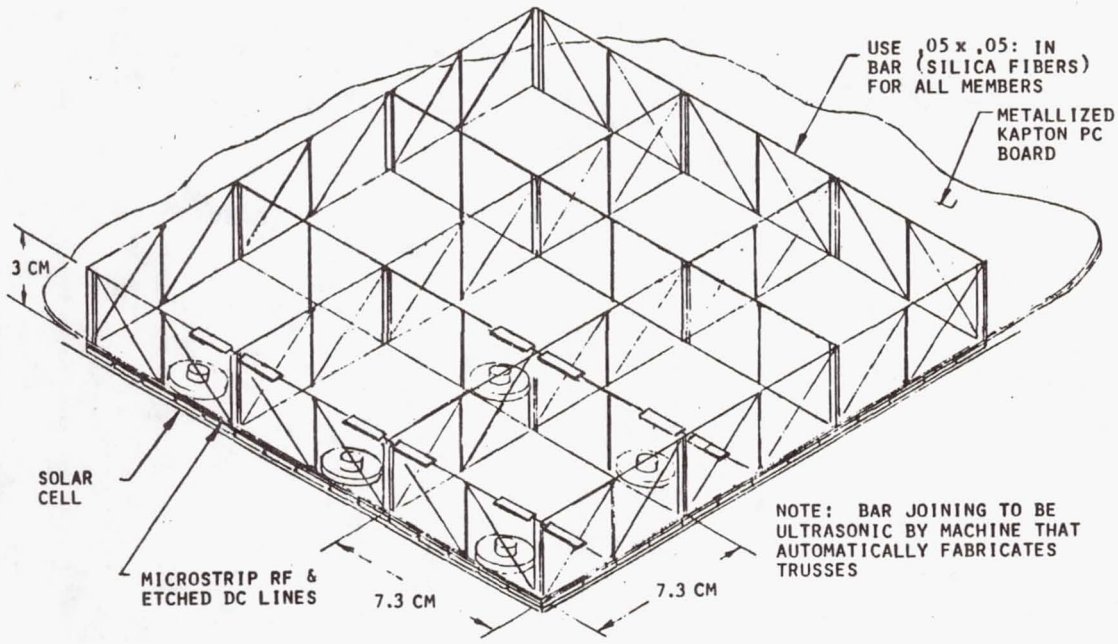

Figure 5.1-1. Sandwich Antenna with Dipoles Over Ground Plane, Ground-Plane Amplifier Mounting

5.2 ANTENNA DESIGN

The antenna is a two-dimensional square array which uses printed circuit dipoles as radiating elements. The dipoles are printed on eight separate 39-inch by 2.5-inch Diclad 527 boards. The properties of this material are summarized in Table 5.2-1. Each board consists of a linear array of eight dipoles, as shown in Figure 5.2-1. Each linear array is inserted vertically into the support structure. The eight linear arrays are fed from a common feed line. (Figure 5.2-2). The assembled array is a standing wave array.

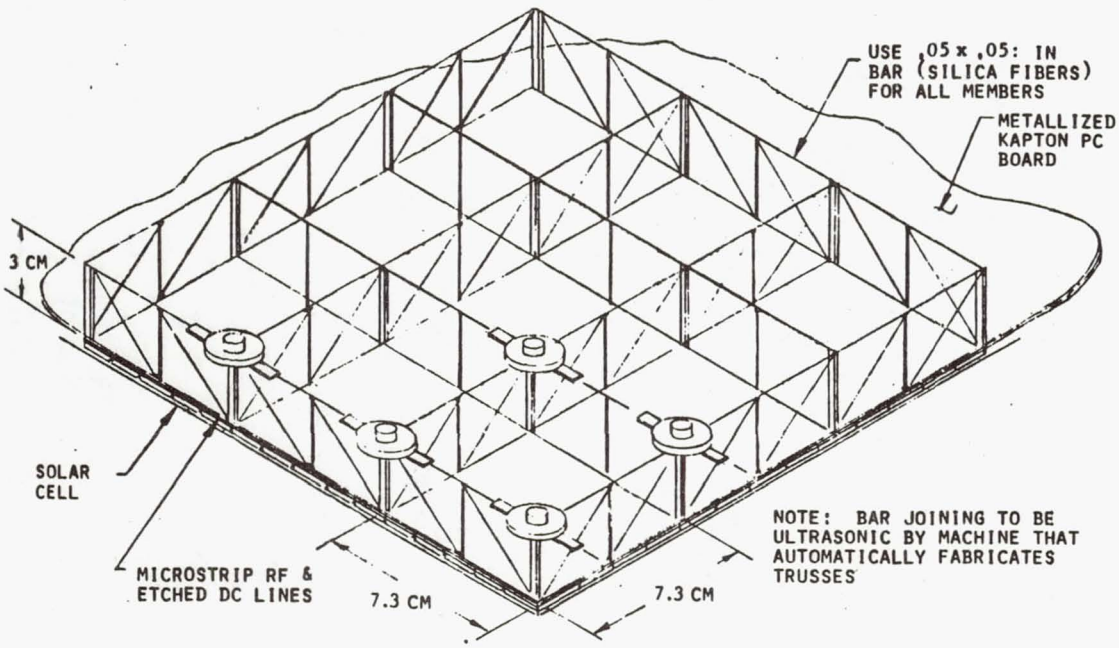

Figure 5.1-2. Sandwich Antenna with Dipoles Over Ground Plane, Dipole Amplifier Mounting

Table 5.2-1. Properties of Diclad 527

ε_r	$2.3 \pm .05$
Thickness	32 mil
Metallization	2 oz. copper (1.4 mil)

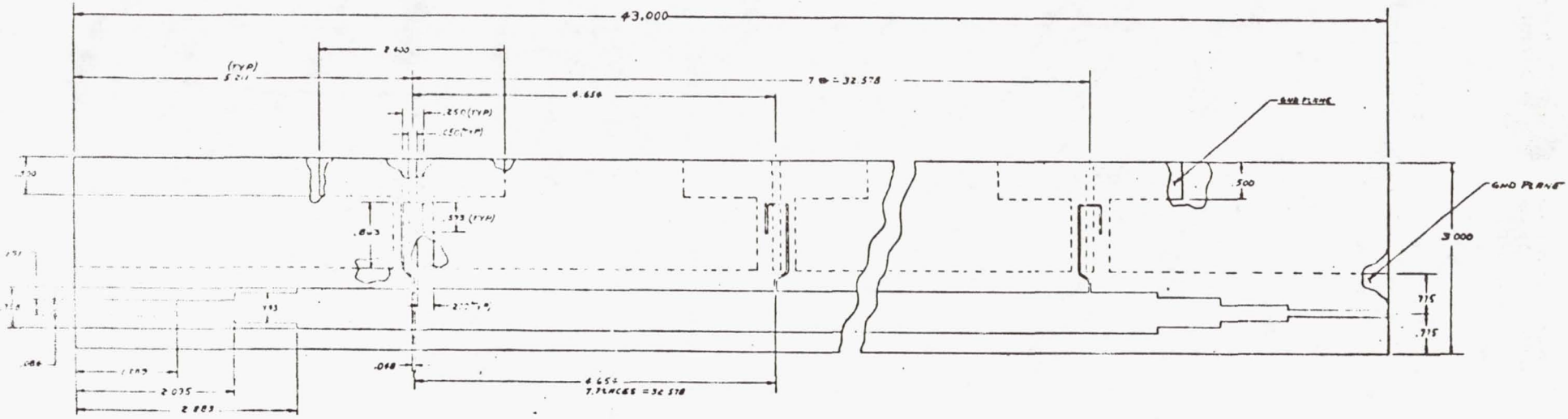

Figure 5.2-1. Antenna Circuit Line

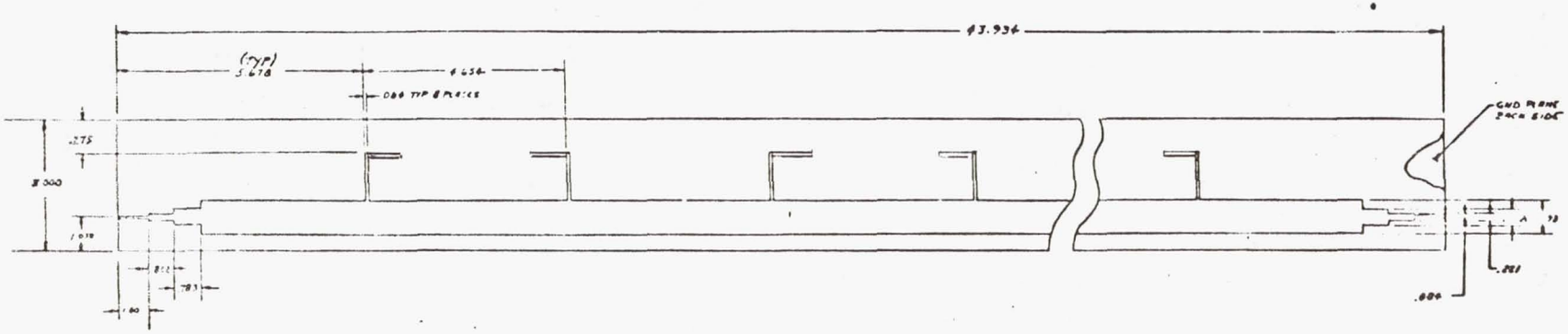

Figure 5.2-2. Antenna Feed Line

The standing wave is generated in each dipole line by terminating the feed lines in an open circuit at the appropriate distance beyond the last dipole of each line. The array is assembled as shown in Figure 5.2-3.

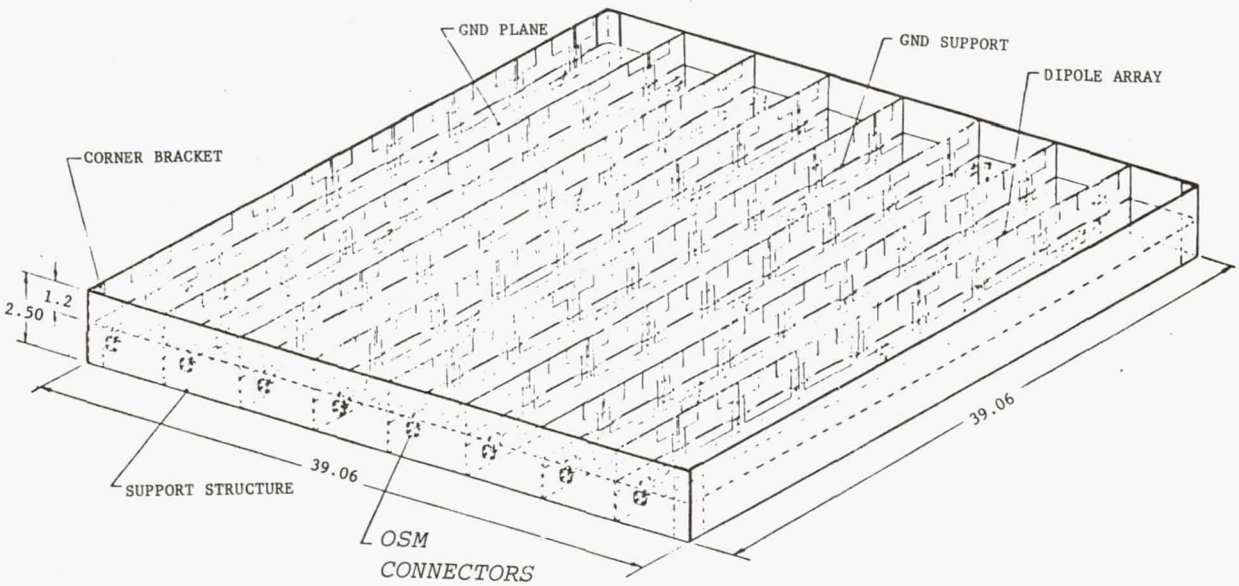

Figure 5.2-3. Antenna Array

5.2.1 THE FEED LINE

The feed line (Figure 5.2-2) is designed such that all inputs and outputs have an impedance of 50 Ω. The main section of the feed line has an impedance of 6.25 Ω. The transition between the 50 Ω input and the 6.25 Ω main section consists of a double λ/4 transformer. The two sections of the transformer have impedances of 25 Ω and 12.5 Ω, the line widths corresponding to these impedances on Diclad 527 are summarized in Table 5.2-2.

Table 5.2-2. Line Width Vs. Impedance for the Main Feed Line

Z (ohms)	Line Width (mils)
50	84
25	221
12.5	508
6.25	1093

The wavelength in free space at 2.45 GHz is λ_o = 12.24 cm (4.82 in.) and in the dielectric it is λ = 8 cm (3.8 in.). The 4.654 in. spacing of the inputs to the linear dipole arrays corresponds nominally to a distance of 3λ/2 along the feed line and 0.96λ in free space. To ensure that all the dipole lines

are fed in phase, every other input line has an additional $\lambda/2$ length of line added to it.

In order to set up a standing wave in the line, the line is terminated in an open circuit at nominally $\lambda/2$ beyond the last dipole. The actual distance for optimum performance was determined experimentally.

5.2.2 THE LINEAR DIPOLE ARRAY

The input to each of the eight dipole lines (Figure 5.2-1) has an impedance of 50 Ω, the main section of the line is 9 Ω, the feed lines to the actual dipoles are nominally 72 Ω. The dipole feed is configured as a Roberts balun. The line widths used and their corresponding impedances are summarized in Table 5.2-3.

Table 5.2-3. Line Width Vs. Impedance for the Linear Dipole Arrays

Z (ohms)	Line Width (mils)
50	85
25	221
12.5	508
6.25	1093

The dipoles themselves are half-wave dipoles ($\lambda_o/2$ = 2.4 in.). The width is arbitrary to a large extent, and was chosen to provide some bandwidth ($\approx$ 20 MHz). A width of 0.5 inch gives a cross reaction of 0.001 in^2 on 2 mil copper. The dipoles are spaced 4.654 in. apart, which again, corresponds to $3\lambda/2$ in the dielectric and 0.96λ in the free space. All dipoles are fed in phase by reversing the balun feed to every other dipole. The result is a square two dimensional array with radiating elements spaced $.96\lambda$ apart.

5.2.3 The Two-Dimensional Array

The resulting two-dimensional broad side array (Figure 5.2-3) has a theoretical performance which is summarized in Table 5.2-4 and plotted in Figure 5.2-4

Table 5.2-4. Antenna Summary

Directivity	29.75 dBi
Beam Width (3 dB)	6.62°
Sidelobe Level	13 dB
Illumination	Uniform
Element Spacing	$.96\lambda$
Radiating Elements	Dipoles

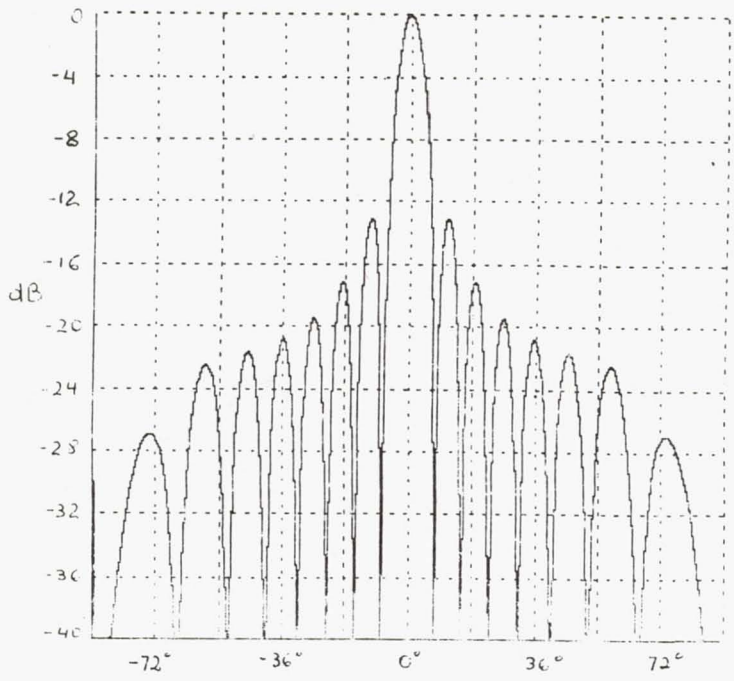

Figure 5.2-4. Calculated E-Plane Array Pattern

The radiation pattern is that of an array of dipoles over ground. The E-plane pattern is:

$$P(\theta) = \left[\frac{\cos\left(\frac{\pi}{2}\cos\theta\right)}{\sin\theta} \sin\left(\frac{\pi}{2}\sin\theta\right) \frac{\sin\{4(2\pi)(.96)\cos\theta\}}{8\sin\{0.5(2\pi)(.96)\cos\theta\}} \right]^2 \quad (5\text{-}1)$$

And the H-plane pattern is:

$$P(\theta) = \left[\sin\left(\frac{\pi}{2}\sin\theta\right) \frac{\sin\{4(2\pi)(.96)\cos\theta\}}{8\sin\{0.5\,(2\pi)(.96)\cos\theta\}} \right]^2 \quad (5\text{-}2)$$

where θ is the elevation angle measured from the plane of the array. The 3 dB beamwidth and sidelobe level are obtained directly from the pattern equations. The directivity estimate is based on the approximate formula

$$D \approx \frac{41{,}253}{\theta^\circ_{3dB}\,\phi^\circ_{3dB}}$$

where θ° and ϕ° are the 3 dB beam widths in the E-plane and in the H-plane respectively.

5.2.4 RECTIFIER DESIGN

Eight full wave rectifiers were fabricated for the purpose of providing a visual display of RF power transmission between the two antennas. For the purposes of this demonstration, no elaborate optimization was performed on the rectifier circuits.

The rectifiers were designed such that the display could be operated with a single amplifier connected to the transmitting antenna. There is one rectifier per linear array. The rectifier is connected to the dipole line with an SMA connector. In this way, the rectifiers are removeable and the antenna can be used for RF measurements without modifications.

On the basis of a maximum output of 5 watts from an amplifier, the power density at the receiving antenna at 55 ft. is 960 mW/m^2 ($\approx .1$ mW/cm^2). This number is based on a measured far field gain of 25.3 dBi. The distance of 55 ft. ensures that the receiver is in the far field where the theoretical analysis is valid. The 1 m^2 receiver array subtends a beam width of 4° which is narrower than the 6.6° 3 dB bandwidth of the main beam. The receiving antenna, therefore, receives maximum power density over most of its area. The maximum amount of power per dipole line is then approximately 120 mW.

The demonstration is likely to be done over a shorter distance than 55 ft. The receiver was tested at 12 ft. from the transmitting antenna. At this distance, the receiving antenna is in the near field, where the beam is not formed and the phase front does not correspond to the uniform in-phase illumination of the theoretical analysis. The phase addition along each dipole line is not easily predicted and the final input to the rectifier unit may differ considerably from theoretical predictions. The results of the short-range transmission tests are discussed in Section 5-4.

The rectifiers selected were Hewlett Packard diodes HP 5082-2835. This diode is a Schottky barrier general purpose diode, optimized for low turn-on voltage. In the absence of a full computer simulation, the device was selected on the basis of favorable dc characteristics which were a low forward resistance and a low junction capacitance ($C \simeq .5$ pf $R = 30\ \Omega$ at 1 mA).

Previous SPS rectenna studies[1] have shown that conversion efficiency is generally poor at low power levels and improves when the incident microwave power exceeds 1 watt. A 50% conversion efficiency was obtained at input levels of 100 mW per rectifier.

The input was matched to 50 Ω experimentally, and was found to require a relatively small amount of matching. The best match (least reflected power) was obtained by adding a capacitive stub to the 50 Ω input transmission line. Both balanced and unbalanced inputs were tried on the RF side of the rectifier.

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[1] William C. Brown, "Optimization of the Efficiency and Other Properties of the Rectenna Element." MTT Symposium Digest, 1976, p. 142.

No noticeable difference in performance was found between the two configurations. In the final version of the rectifiers, the dc side of the full-wave bridge does not have a fixed ground. It was found that the conversion efficiency was improved by smoothing out the output dc voltage by means of two ferrite chokes, one on each side of the rectifier.

The rectified output is fed directly into a load consisting of three LED's in parallel. A fourth LED was added to the rectifiers which were used in the center of the receiving array. The "turn-on" point (visible glow) of the LED's used for the display occurred at 1.48 volts and 0.7 mA, that is, at a dc power of 1.036 mW. The LED's tested operated over a wide range of power from 1.036 mW to 340 mW before burning out. Higher powers can be used if protective circuitry is added around the LED. The operating conditions are summarized in Table 5.2-5.

Table 5.2-5. LED Operating Range

Voltage (Volts)	Current (mA)	Power (mW)
1.48	0.7	1.036
1.5	1.2	1.8
1.55	4.6	7.13
1.6	17.9	28.64
1.65	49.4	81.51
1.7	92	156.4
1.75	138.9	243.1
1.8	189	340.2

A schematic of the rectifier circuit is shown in Figure 5.2-5.

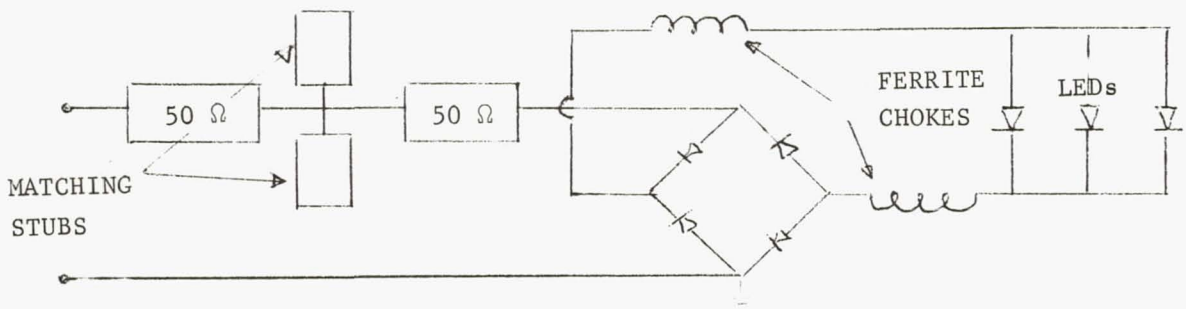

Figure 5.2-5. Rectifier Circuit

5.3 TEST PROCEDURES AND RESULTS

The eight linear dipole arrays were first tested individually. Each linear array was terminated in an open circuit approximately 1.75 inches from the last dipole in the line. The correct distance was determined by testing the line in the automatic Network Analyzer system for minimum VSWR at 2.45 GHz. Typical test data are shown in Figure 5.3-1.

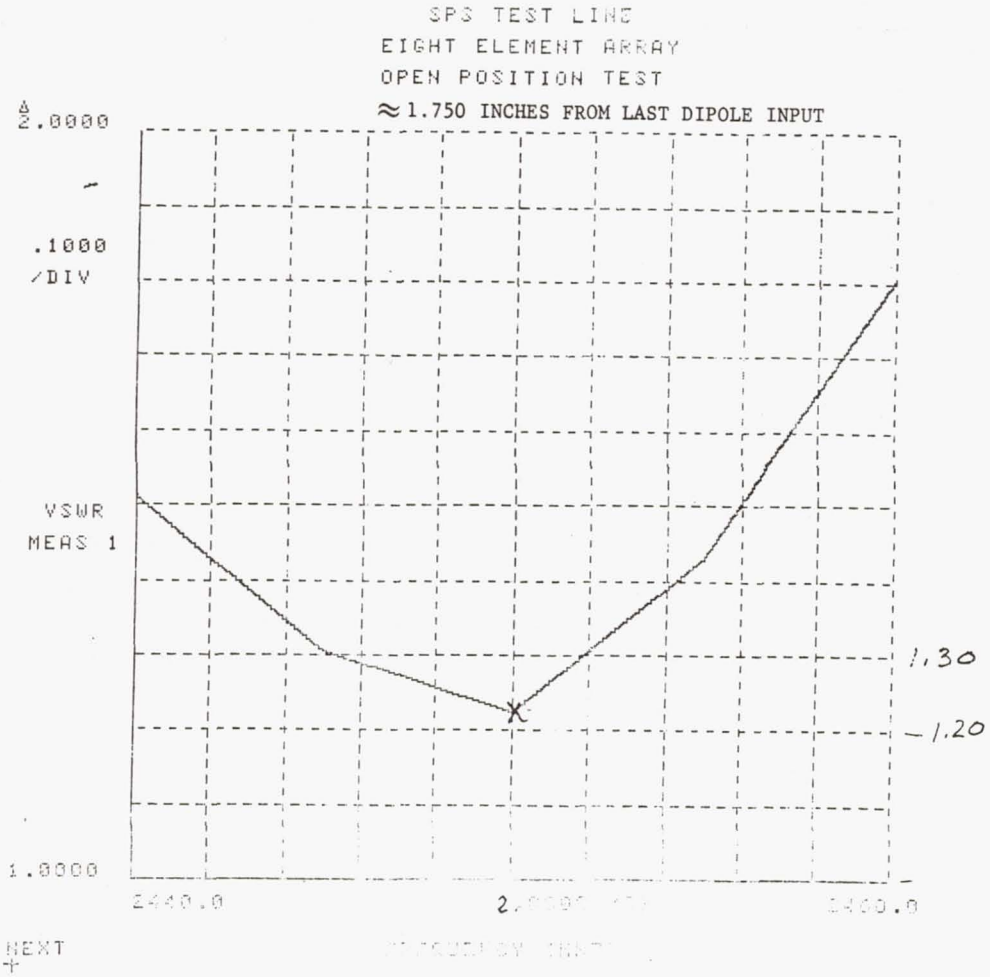

Figure 5.3-1. VSWR Vs. Frequency for Open Circuited Dipole Line

The radiation pattern of a linear array was measured before the antenna was assembled and is shown in Figure 5.3-2. This pattern corresponds to equation (5-1). The measured beam width and sidelobe level correspond very closely to the theoretical design values.

The fabricated parts of the array before assembly are shown in Figure 5.3-3 and the assembled array in Figure 5.3-4. The feed line to the assembled antenna was adjusted for minimum input VSWR by an open-circuit termination. The position of the termination was determined by testing the array in the automatic Network Analyzer system, as shown in Figure 5.3-5.

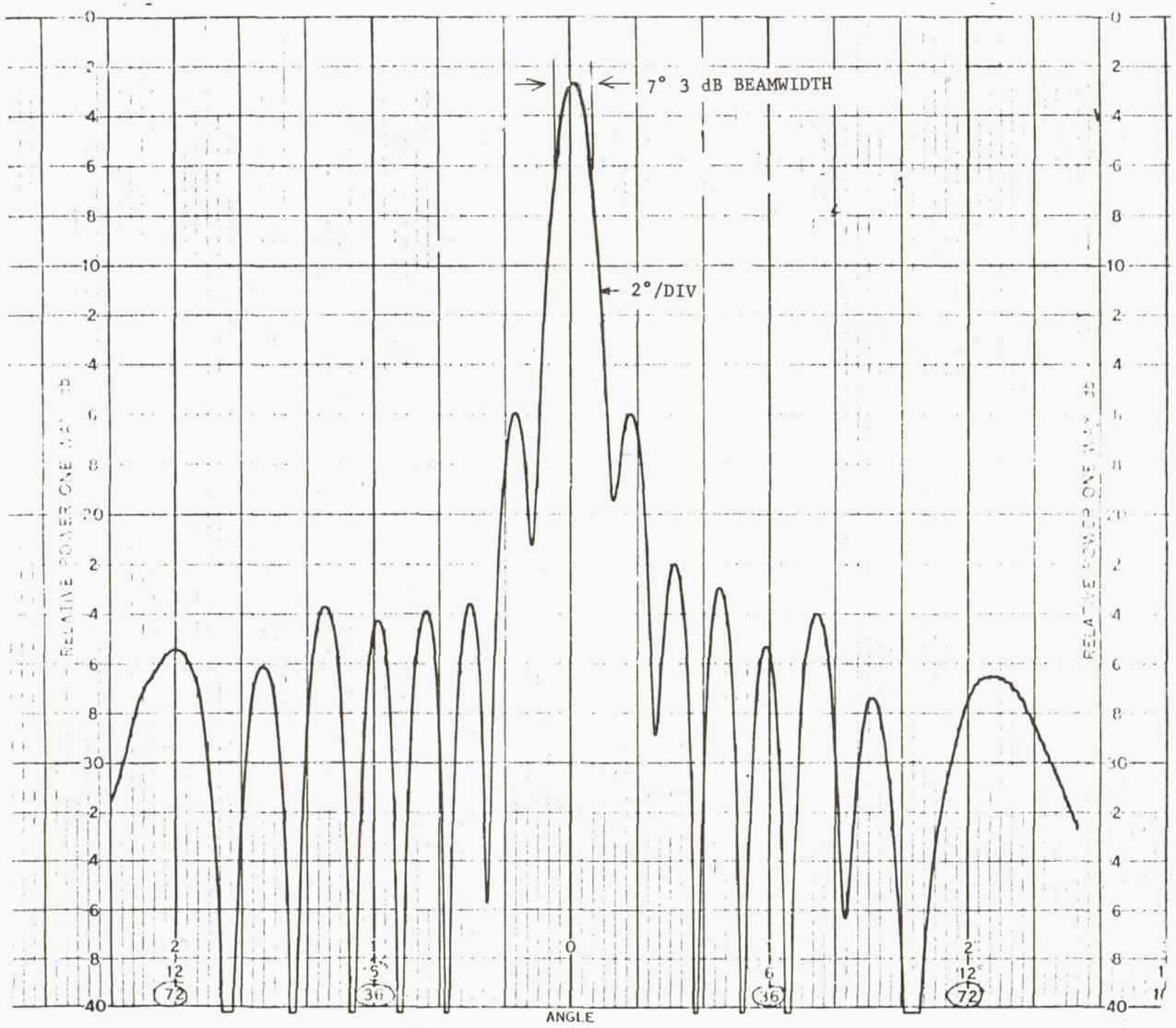

Figure 5.3-2. Measured Radiation Pattern of Linear Dipole Array

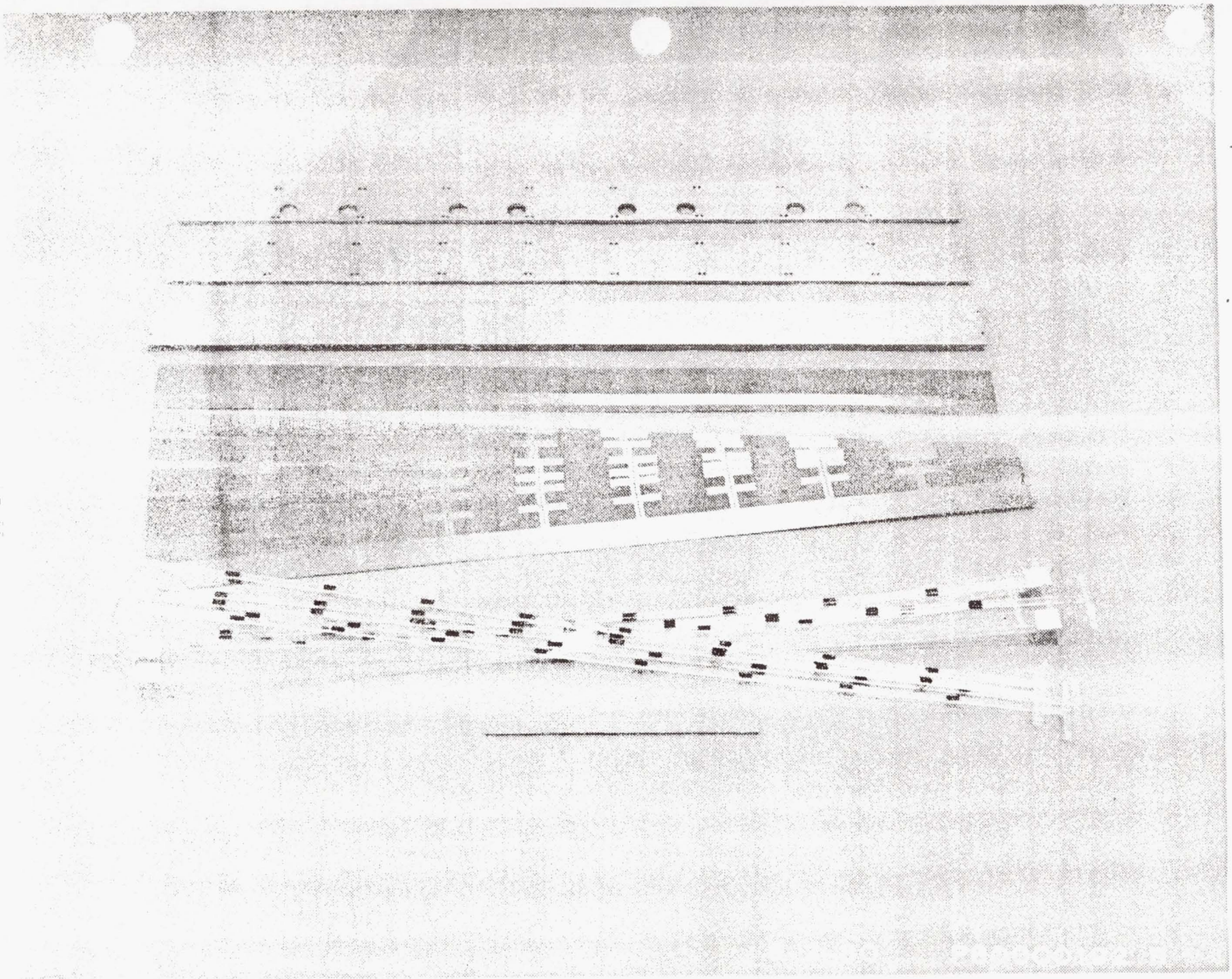

Figure 6-10 - Array parts before Assembly

Fig. 6-11 - Assembled Array

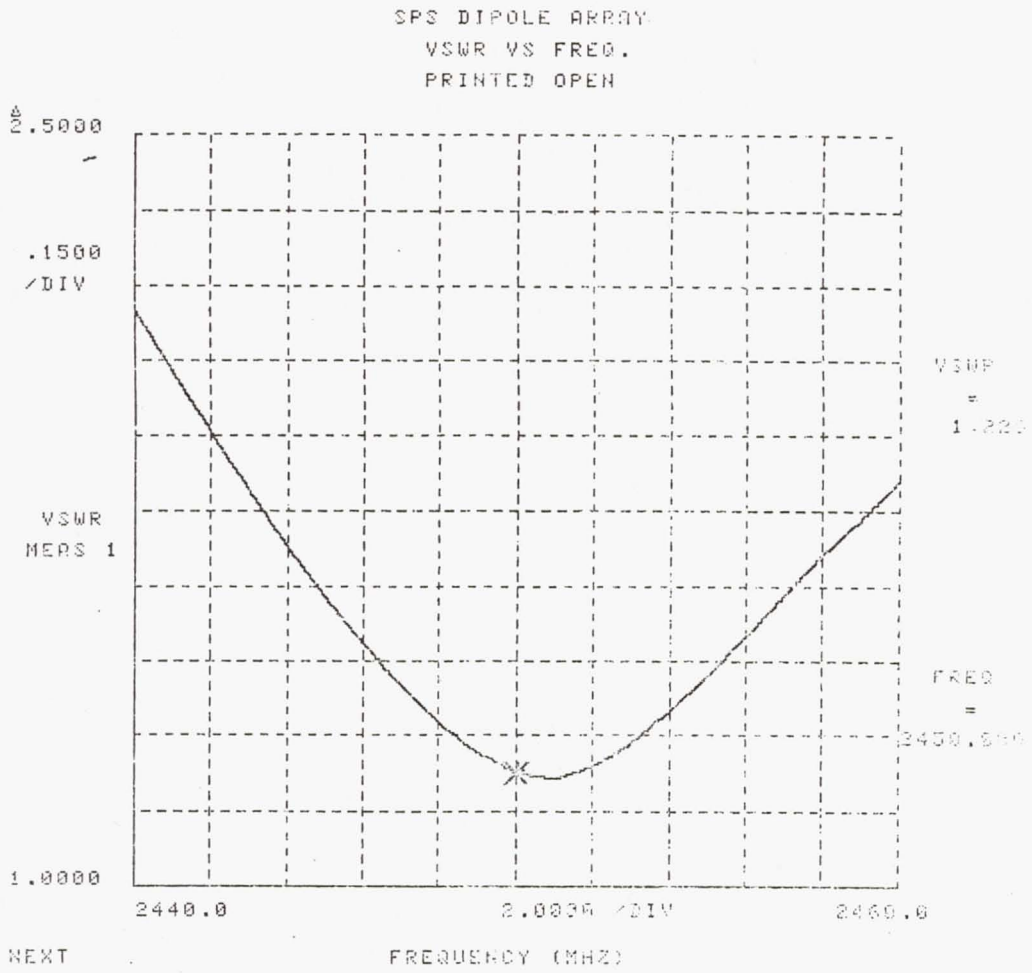

Figure 5.3-5. Input VSWR Vs. Frequency for Assembled Array With Open Circuited Feed Line

The radiation pattern of the assembled array was then measured. The experimental pattern in the E-plane corresponding to equation (5-1) is shown in Figure 5.3-6. The experimental pattern in the H-plane corresponds to equation (5-2) as shown in Figure 5.3-7. The results of the measurements are summarized in Table 5.3-1.

The gain was measured by comparing the power measured at the antenna with that of a calibrated standard gain horn. A phase error loss of .6 dB was estimated because the dimensions of the anechoic chamber where the test was performed limited the range to 22 feet. Therefore, the true far-field gain would be 25.3 dBi. The line losses in the feed line and in each individual dipole line, and the VSWR loss are estimated to amount to a total loss of 2.73 dB, and corresponds to an efficiency of 53%. Without the losses, the gain would be 28.03 dB.

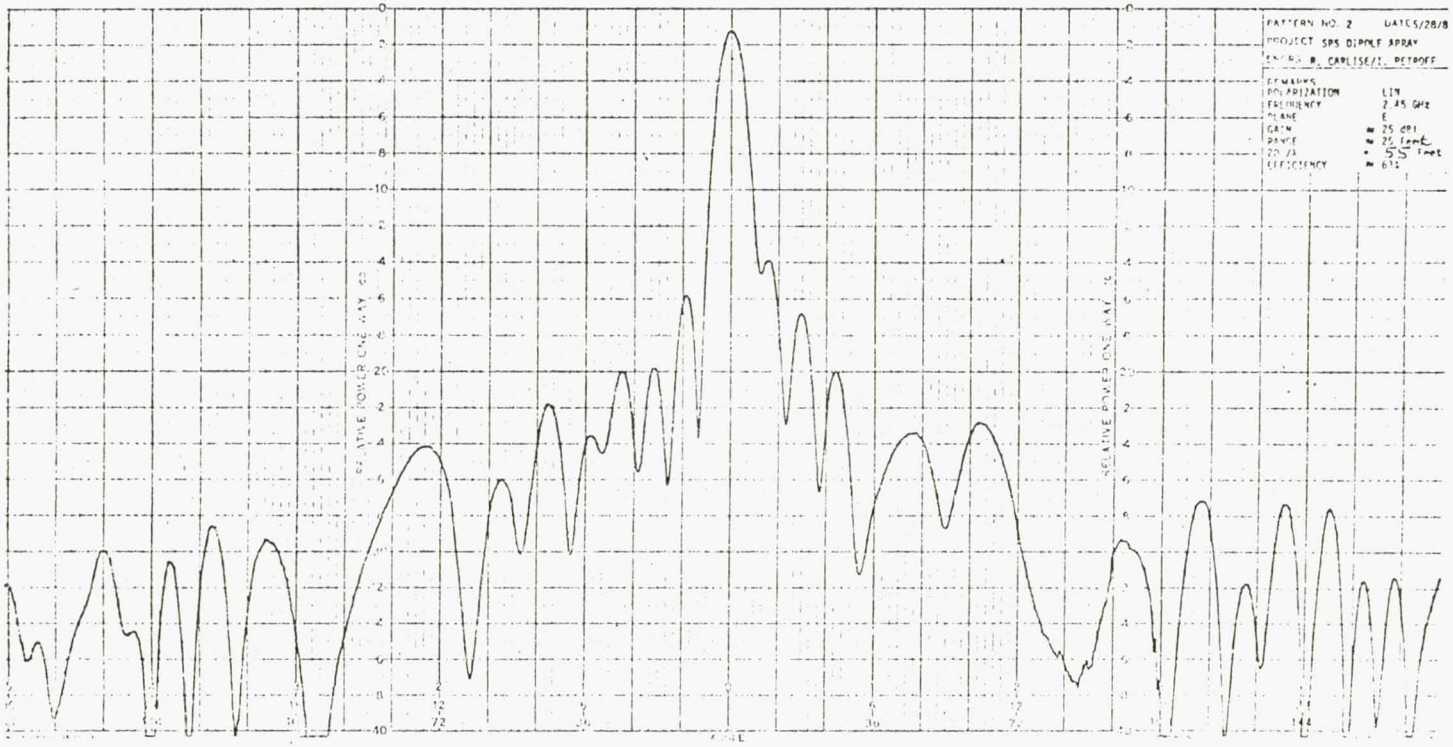

Figure 5.3-6. Measured E-Plane Pattern of Assembled Array

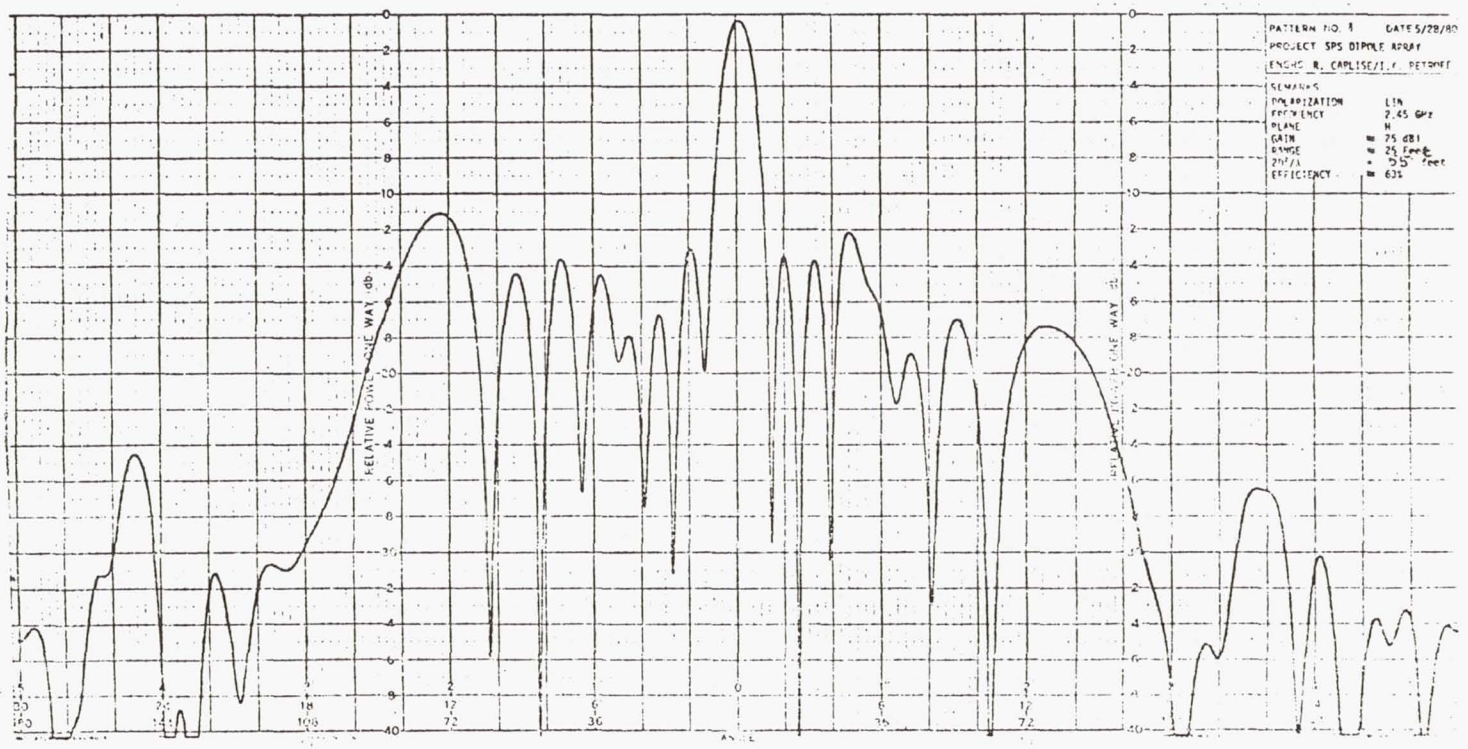

Figure 5.3-7. Measured H-Plane Pattern of Assembled Array

Table 5.3-1. Measured Antenna Parameters

Range	22 ft
Beamwidth (3 dB)	7.3°
Gain	24.7 dBi

The rectifiers were fabricated on 1.5-inch by 3-inch pieces of Diclad 527 printed circuit board and tested in the laboratory as described in Section 5.2.4 before mounting on the antenna.

5.4 INTEGRATED TESTS

The antenna/rectenna combination was used as a demonstration vehicle to demonstrate the operation of the amplifiers developed during this program. The demonstration was carried out in a "conference room" environment where the receiver was tested at 12 ft from the transmitting antenna. At this distance, the receiving antenna is in the near field of the transmitter and the phase front of the beam does not correspond to the uniform phase illumination of the theoretical analysis.

Before mounting the rectifiers on each of the eight linear arrays of the receiving antenna, the RF power collected at the output of each linear array was measured for two levels of input into the transmitting antenna. The results of the measurements are shown in Table 5.4-1

Table 5.4-1. RF Power at Receiving Antenna Vs. Power into the Transmitter

$P_{transmitter}$	Line #	$P_{receiver}$	
		dBm	mW
1 watt (30 dBm)	1	6.0	4
	2	7.0	5
	3	7.0	5
	4	7.0	5
	5	10.2	10.5
	6	9.6	9.12
	7	9.5	8.9
	8	8.6	7.24
	Total	17.4	54.76
4 watts (36 dBm)	1	10.2	10.5
	2	12.2	16.6
	3	12.2	16.6
	4	12.0	15.8
	5	15.2	33.1
	6	15.0	31.6
	7	14.0	25
	8	13.5	22.4
	Total	22.35	171.6

There are two major sources of RF losses in the present transmitter-receiver configuration. Tests on the transmitting antenna alone have shown that line losses are significant (Section 5.3). When the receiver is added to the system, these losses are doubled. The second major source of losses has to do with phase cancellations at the dipoles when the receiver is operating in the near field. The line losses are eliminated if the transmitter is designed as an active array; that is, if the amplifiers are located at each radiating element, so that the power is radiated directly out without having to propagate through a lossy circuit medium. Similarly, at the receiver, RF losses are eliminated by rectifying at the receiving element.

For the purposes of activating the LED display in the case of the demonstration, the power transmitted was sufficient to activate the display with each of the four amplifiers. However, the display was clearly visible only with the two higher power amplifiers (No. 1 and No. 2).

6.0 SUMMARY AND CONCLUSIONS

A total of four high-efficiency amplifiers were fabricated during this program. The two amplifiers required for Phase I substantially met all of the specifications (5 W, 50% efficiency, and 8 dB gain). A third amplifier, for Phase II, operated at the very high efficiency of 72%, with an output power of 1.2 W. The fourth amplifier had lower efficiency (62%), but twice the output power (2.4 W).

The optimization of the various operating parameters - bias voltages, circuit impedances, and RF drive level - was greatly facilitated by the availability of a computer-controlled set-up. Instantaneous voltages and currents (waveforms) at the device terminals were measured by a computer-controlled system specifically developed for studying nonlinear effects in GaAs FETs. It was found, for instance, that the gate resistance has the effect of limiting the operating efficiency because of negative voltage buildup due to forward conduction of the Schottky barrier. Excessive gate resistance also reduces the device cut-off frequency. In addition, the large instantaneous voltages between drain and gate cause breakdown of the Schottky barrier and limit the operating efficiency.

The amplifiers that provided best performance operated in a Class AB saturated mode.

Some of the parameters that limit the efficiency of GaAs FETs are well known such as, for instance, carrier mobility in GaAs, contact resistance, and resistance of the thin-film metallization. Some phenomena, however, have a more subtle effect in limiting the efficiency. One of these phenomena is the voltage breakdown of the Schottky barrier under large RF drive conditions. The onset of the breakdown prevents the device from being fully turned-off for a sufficiently long fraction of the RF cycle. An attempt to overcome this drawback by reducing the drain-bias voltage is not very effective because the saturation voltage assumes a larger fraction of the overall RF voltage.

Waveform measurements of an FET, which was otherwise very efficient, showed another unexpected effect; an increase of saturation voltage when the RF drive was raised above the level required for optimum efficiency. This additional saturation voltage was attributed to the presence of forward conduction current flowing through the resistance of the gate. This made apparent the importance of a low gate resistance for achieving full saturation of the FET.

It should be noted also that forward conduction of the gate is often unavoidable. High-efficiency operation requires full saturation and rapid switching which is obtained by applying large sinusoidal RF signals at the input. It is conceivable that, in the future, high efficiency devices might include low resistance diodes clamping the gate voltage and limiting both the positive and the negative swing of the RF signal. These diodes, however, in

order to be effective, will have to be fabricated on the same substrate as the active device. This would avoid the filtering effect of an intermediate circuit.

Another factor which affects the operating efficiency is the device cut-off frequency. For instance, higher power devices, which have typically lower cut-off frequencies, are sometimes less efficient simply because of their longer switching time. This was exemplified by the waveform measurement results of the FLS50.

Many of the device limitations became apparent that neither the Class C nor the Class E mode of operation was suited for high-efficiency GaAs FET amplifiers. The basic limitation is the Schottky barrier of the gate that, when biased at pinch-off (or beyond for Class C), breaks down at low RF drive before the device is fully saturated. The result is a rather low power and efficiency. Also, since the transconductance is usually low near pinch-off, the gain is also low, which further reduces the power-added efficiency.

Saturated Class B and Class AB modes of operation were found to be better suited for high-efficiency FET amplifiers. Here, a better compromise could be maintained between the conflicting requirements of device bias, RF drive level, and circuit impedances. Indeed, experiments have consistently shown that best efficiency (or a best efficiency/power compromise) could be obtained by operating the devices in Class AB or near Class B (bias current approximately 10% of I_{DDS}).

During the course of this program, it became apparent that maximum efficiency can be obtained only at approximately one half of the maximum power available from the device. Therefore, a device designed for optimum efficiency should be oversized by approximately a factor of two. The inevitable higher input and output capacitance of the device can be overcome by internal matching techniques.

7.0 RECOMMENDATIONS FOR FUTURE TECHNOLOGY ACTIVITIES

An experimental study of FETs operating under high-efficiency conditions has been initiated in this program. The understanding of the waveform results is at present incomplete, and additional analysis must be done in that respect.

As illustrated by the results obtained in Table 4.3-1 and as evidenced in the discussion of Section 4.3.1, on the circuit design of power amplifiers, the package parasitics of the device have a large influence on the correct design of the amplifier circuit and must be accounted for correctly. The iterative process described in Section 4.3.1, where the effect of the parasitics is estimated at first, and the correct output circuit is obtained by iterating the design several times, is very helpful for arriving at a true and correct model of the FET.

If internal matching is to be used, as it must be if high efficiency devices are to yield a relatively high level of power as well, a similar iterative approach of experimental results combined with analysis will have to be used to achieve the optimum matching scheme.

It became evident during the course of the program that a high device cut-off frequency contributes to high-efficiency operation by improving the switching time of the device. The frequency capability of a GaAs FET may be expressed by the figures of merit, f_T and f_{max} at which the current gain and power gain become unity, respectively. A reduction in gate length may be used to increase f_T. In this case, f_{max} increases as a direct consequence of the increase in f_T. Alternatively, the output resistance may be increased at constant f_T to obtain increased gain and higher f_{max}. Each of these parameters will affect the gain, the noise properties, and the parasitics of the device. A study of the tradeoffs of these factors will be necessary before a high-efficiency, high-power device can be properly designed.

The antenna development done in this program for the purpose of the microwave transmission demonstration has served to point out several interesting areas for future study of the optimum antenna configuration for a solid-state SPS system. The possibility of using the active array concept, that is, where relatively low power amplifiers are mounted directly at each of the radiating elements of the array, offers the possibility of avoiding losses which arise when RF power has to be routed over relatively large distances in a transmission line medium. The implementation of such an array must begin with a study of the interactions between the amplifier and the antenna to determine the requirements imposed on the amplifier circuit.

APPENDIX A

LISTING OF POWER AND EFFICIENCY MEASUREMENT PROGRAM

```
$ETEST T=00004 IS ON CR00004 USING 00020 BLKS R=0000

0001   FTN4,L
0002         PROGRAM ETEST
0003   C-----EFFIENCY METER-#USES 2570 DATA COUPLER IN CONJUNCTION
0004   C-----WITH 6936-40 MULTIPROGRAMMER,DANA DVM,436A ASCII BUSS
0005   C-----PWR. METER AND COMPUTES POWER ADDED EFFIENCY AND
0006   C-----DISPLAYS RESULT AS A ANALOG VOLTAGE ON D-A CARD TO BE
0007   C-----READ BY DVM AS AN AID TO TUNING ACTIVE DEVICE
0008   C---------------
0009         DIMENSION IBBF(16),IHDIC(60)
0010   C---------------
0011   C---------------
0012   C---------------
0013         LU=LOCLU(ID)
0014         CALL MINIT
0015         WRITE (LU,3)
0016     3   FORMAT(/"ETEST--J BROWN   21/10,79  REV.02"/
0017        @"OPTIONS ARE"/"1==TERMINATE PROGRAM"/
0018        @"2==RESUME NORMAL PROGRAM OPERATION"/
0019        @"3==REENTER CORRECTION FACTORS"/
0020        @"4==REGENERATE TITLE BLOCK-HEADING"/
0021        @"5==LIFE TEST CHECK"/
0022        @"6==CHANGE TITLE ONLY"/)
0023         LIFCK=10000
0024     7   WRITE (LU,5)
0025     5   FORMAT(/"PWR. INPUT MULT. CORR. FACTOR =? _")
0026         READ (LU,*) CFPI
0027         WRITE (LU,10)
0028    10   FORMAT (/"PWR. OUTPUT MULT. CORR.10  FACTOR =? _")
0029         READ (LU,*)CFPO
0030         WRITE(LU,15)
0031    15   FORMAT (/"VALUE,IN OHMS,OF ID SAMPLING RESISTOR =?_")
0032         READ (LU,*)PIDR
0033         WRITE (LU,16)
0034     16  FORMAT(/"VALUE,IN,OHMS,OF IG SAMPLING RESISTOR=?_")
0035         READ(LU,*)VGR
0036   C------D TO A -AMP-"GAIN" CALIBRATION
0037         EFF=50.
0038         GAIN=20.
0039         CALL VOUT(EFF,GAIN)
0040         WRITE (LU,32)
0041    32   FORMAT(/"ADJUST GAIN D-TO-A AMP FOR 20 DB READING"/)
0042         LEN=30
0043     21  WRITE(LU,22)
0044    22   FORMAT(/"ENTER HEADING-TITLE ,OR SPACE RETURN "/
0045        @ "          _")
0046         CALL BREAD(LU,IHDIC,LEN)
0047         LEN2X=LEN+LEN
0048    19   WRITE (LU,20)
0049    20   FORMAT(/"OPTION NUMBER =?_")
0050         READ(LU,*)OPT
0051         GO TO (50,25,7,24,27,21)OPT
0052   C----------

0053    27   WRITE(LU,23)
0054    23   FORMAT("ENTER LIFE CHECK COUNT=  _")
0055         READ(LU,*)LIFCK
0056         GO TO 19
0057   C-------GENERATE TITLE BLOCK
0058    24   CALL RETIO(2,LU,IHDIC,LEN2X)
0059         CALL FTIME(IBBF)
0060         LEN=16
0061         CALL RETIO(2,LU,IBBF,LEN)
0062         WRITE (LU,6)
0063     6   FORMAT(//,"DRAIN",4X,"DRAIN",5X,"GATE",5X,"GATE",5X,"P-IN",
0064        @5X,"P-OUT",5X,"EFF.",5X,"GAIN",/,"VOLT",5X,"AMP",
0065        @7X,"VOLT",5X,"M-AMP",4X,"WATT",5X,"WATT",7X,"%",7X,"DB"/)
0066         COUNT=0
0067      25  CONTINUE
0068         NIX=0
0069   C------READ DEVICE BIAS VOLTAGE
0070   C---------
```

```
0071          CALL DANM (1,6,VR,5)
0072          VD=VR
0073    C-------READ DEVICE BIAS CURRENT
0074          CALL DANM (2,5,VR,5)
0075          VID=VR
0076          VIDR=VID/PIDR
0077    C-------READ RF PWR INPUT
0078          CALL PRUN(23,LU,PWR)
0079          PWRIR=CFP1*ABS(PWR)
0080    C------READ RF POWER OUTPUT
0081          CALL PRUN (24,LU,PWR)
0082          PWROT=CFPO*ABS(PWR)
0083    C-------COMPUTE EFFIENCY AND GAIN
0084    C--------
0085          EFF=(PWROT-PWRIN)/(VIDR*VD)
0086          GAIN=10.*ALOCT(1.E-8+PWROT/PWRIN)
0087          EFF=EFF*100.
0088          IF (ABS(EFF) .LE. 100.) GO TO 58
0089          WRITE(LU,30)
0090     30   FORMAT("@@_")
0091          IF(IFBRK(IDUMY)) 19,57
0092    C-------DISPLAY DATA ON DVM
0093     57   NIX=5
0094     58   CALL VOUT (EFF,GAIN)
0095    C-------PUSH BUTTON TEST
0096          CALL DANM (3,5,VR,5)
0097          CHECK=VR
0098          LIF=LIF+1
0099          IF(LIF.EQ.LIFCK)CHECK=2
0100          IF(LIF.EQ.LIFCK)LIF=0
0101          IF(CHECK .GT.1.)GO TO 35
0102    C--------------------
0103          IF(IFBRK(IDUMY))35,25
0104     35   CONTINUE
0105    C----------READ DEVICE GATE VOLTAGE(4) AND CURRENT(5)
0106          CALL DANM(4,5,VR,5)
0107          VG=VR
0108          CALL DANM (5,4,VR,5)
0109          VGIR=VR
0110          VIG=(VGIR/VGR)*1000.
0111          IF(NIX.EQ.5) GO TO 46
0112            IF(PWRIN .LT. .002) GO TO 46
0113          WRITE(LU,45)VD,VIDR,VG,VIG,PWRIN,PWROT,EFF,GAIN
0114     45   FORMAT(//F5.2,4X,F5.3,4X,F5.3,4X,F5.3,3X,F5.3,4X,
0115         @F5.3,4X,F5.2,4X,F5.2)
0116          GO TO 90
0117     46   WRITE(LU,47)VD,VIDR,VG,VIG
0118     47   FORMAT(//F5.2,4X,F5.3,4X,F5.3,4X,F5.3,5X,
0119         @"DC TEST ONLY")
0120     90   CALL  DANM(3,5,VR,5)
0121          STAT=VR
0122          IF (STAT .GT.1.) GO TO 90
0123          COUNT=COUNT+1
0124          IF(COUNT .LT. 17.) GO TO 71
0125          WRITE(LU,75)
0126     75   FORMAT("@@@@"///////)
0127          IF(COUNT.EQ.17) GO TO 24
0128    C---------
0129     71   IF(CHECK .GT. 1.) GO TO 25
0130          GO TO 19
0131     50   WRITE(LU,51)
0132     51   FORMAT(/"END OF TEST"/)
0133          CALL WAITB(LU)
0134          END
0135    C---------------
0136    C---------------
0137    C--------------
0138          SUBROUTINE  VOUT (EFF,GAIN)
0139          IV=(200*EFF+SIGN(.5,EFF))*.1
0140          WRITE(10,11)IV
0141     11   FORMAT ("@2117014\@2101"K4"\@")
0142          IGAIN=(200*GAIN+SIGN(.5,GAIN))*.5
0143          WRITE(10,12)IGAIN
0144     12   FORMAT("@2105"K4"\@2117014O\@")
0145          RETURN
0146          END
0147    C------------
```

```
0148          SUBROUTINE BREAD(LU,IBUF,LEN)
0149          INTEGER IBUF(1),IR(2)
0150          EQUIVALENCE (DMY,IR),(LENX,IR(2))
0151          LTU=LU
0152          IF(LU.NE.8)LTU=LTU+400B
0153          DMY=RETO(1,LTU,IBUF,LEN)
0154          LEN=LENX
0155          RETURN
0156          END
0157          ENDS
0158    C-----------
0159    C-----------------
```

APPENDIX B

DEVICE PERFORMANCE DATA

FLC-30 4230 SAMPLE CRKT
4:58 PM TUE., 6 NOV., 1979

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
6.12	.405	-3.39	1.41	.285	1.730	58.26	7.83
6.12	.379	-3.54	.13	.223	1.566	57.88	8.47
6.13	.359	-3.56	.02	.135	1.230	49.75	9.61
6.14	.330	-3.56	.01	.071	.813	36.55	10.56
6.16	.284	-3.56	.00	.036	.431	22.56	10.78
6.17	.259	-3.56	.00	.018	.211	12.13	10.72
6.17	.241	-3.56	.00				

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FLC-30 4230 SAPL CRKT
10:09 AM WED., 7 NOV., 1979

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.41	.822	-1.68	.00	.000	.000	.00	~~382.3~~
10.41	.822	-1.68	.00	.022	.342	3.74	11.90
10.41	.828	-1.68	.00	.044	.701	7.62	11.98
10.41	.848	-1.68	.00	.092	1.490	15.84	12.10
10.40	.882	-1.68	.00	.181	2.777	28.30	11.86
10.42	.807	-2.14	-4.17	.366	3.988	43.05	10.37
10.42	.813	-2.22	-4.91	.456	4.065	42.59	9.50
10.42	.805	-2.30	-5.66	.535	4.084	42.33	8.82

NEC868400 LOT#8717-9 #1
4:40 PM MON., 17 DEC., 1979

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
6.78	.629	-3.14	-3.14	.430	1.978	36.29	6.63
6.77	.641	-3.03	-3.14	.338	1.950	37.16	7.61
6.79	.589	-3.48	-3.14	.240	1.735	37.39	8.59
6.82	.509	-4.10	-3.14	.175	1.446	36.66	9.18
6.86	.371	-4.98	-3.14	.110	.894	30.81	9.09
6.90	.284	-5.47	-3.14	.080	.568	24.87	8.51
6.92	.201	-5.94	-3.14	.054	.292	17.11	7.35
6.95	.138	-6.28	-3.14	.035	.136	10.55	5.89
6.96	.103	-6.47	-3.14	.026	.076	6.98	4.72
6.97	.083	-6.60	-3.14	.019	.044	4.33	3.67
6.98	.066	-6.70	-3.14	.014	.025	2.48	2.64
6.98	.049	-6.80	-3.14	.008	.012	.97	1.43
6.99	.034	-6.87	-3.14	.004	.004	.08	.20
6.99	.032	-6.90	-3.14	DC TEST ONLY			

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NEC868400 LOT#8717-9 #1
4:44 PM MON., 17 DEC., 1979

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
8.56	.727	-2.92	-3.14	.526	2.435	30.68	6.66
8.54	.753	-2.70	-3.14	.220	2.118	29.51	9.82
8.59	.632	-3.48	-3.14	.144	1.642	27.59	10.58
8.65	.448	-4.42	-3.14	.075	.878	20.70	10.68
8.69	.328	-4.97	-3.14	.042	.453	14.41	10.31
8.72	.261	-5.30	-3.14	.026	.259	10.24	10.02
8.73	.218	-5.49	-3.11	.017	.165	7.75	9.76
8.74	.193	-5.64	-2.81	.012	.104	5.51	9.50
8.75	.172	-5.75	-2.60	.008	.067	3.93	9.26
8.75	.155	-5.83	-2.45	.005	.046	2.99	9.27
8.76	.147	-5.88	-2.34	.004	.031	2.10	8.97
8.76	.135	-5.96	-2.20	DC TEST ONLY			

NEC86400 LOT #8717-9 #2
3:19 PM MON., 7 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
6.85	.773	-3.23	-3.14	.399	1.779	26.06	6.49
6.84	.782	-3.15	-3.14	.319	1.770	27.15	7.45
6.84	.784	-3.13	-3.14	.295	1.761	27.32	7.76
6.84	.790	-3.12	-3.14	.253	1.726	27.25	8.34
6.85	.770	-3.31	-3.14	.214	1.664	27.48	8.91
6.86	.744	-3.54	-3.14	.191	1.593	27.46	9.21
6.87	.713	-3.79	-3.14	.168	1.513	27.47	9.54
6.88	.664	-4.13	-3.14	.143	1.372	26.90	9.81
6.92	.555	-4.80	-3.14	.102	1.027	24.08	10.01
6.95	.480	-5.21	-3.14	.080	.788	21.21	9.92
6.96	.397	-5.64	-3.14	.059	.525	16.86	9.46
7.00	.342	-5.92	-3.14	.048	.382	13.98	9.03
7.03	.256	-6.41	-3.14	.029	.180	8.36	7.86
7.05	.201	-6.72	-3.14	.019	.089	4.96	6.71
7.06	.170	-6.89	-3.14	.014	.052	3.17	5.80
7.06	.149	-7.02	-3.14	.010	.031	2.03	5.06
7.08	.115	-7.24	-3.14	DC TEST ONLY			

NEC86400 LOT #8717-9 #4
4:33 PM WED., 16 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
8.44	.701	-3.52	-3.14	.660	2.044	23.39	4.91
8.43	.713	-3.33	-3.14	.577	2.106	25.46	5.62
8.42	.733	-3.08	-3.14	.445	2.151	27.65	6.85
8.42	.750	-2.82	-3.14	.283	2.071	28.31	8.64
8.42	.756	-2.74	-3.14	.206	1.938	27.22	9.73
8.46	.618	-3.67	-2.85	.113	1.363	23.92	10.83
8.47	.595	-4.31	-1.60	.065	.792	14.43	10.86
8.54	.414	-4.58	-1.08	.044	.522	13.54	10.77
8.55	.368	-4.77	-.720	.030	.354	10.31	10.73
8.56	.333	-4.90	-.472	.020	.238	7.64	10.72
8.56	.319	-4.97	-.338	.015	.173	5.79	10.74
8.58	.299	-5.02	-.235	.010	.119	4.24	10.78
8.58	.284	-5.06	-.172	.007	.081	3.05	10.78
8.58	.279	-5.07	-.135	.005	.058	2.22	10.78
8.58	.279	-5.08	-.121	.004	.050	1.93	10.80
8.59	.270	-5.09	-.100	.003	.036	1.41	10.82
8.59	.270	-5.10	-.083	DC TEST ONLY			

NEC86400 LOT #8717-9 #4
4:20 PM WED., 16 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
6.55	.649	-3.59	-3.14	.487	1.628	26.83	5.24
6.54	.667	-3.38	-3.14	.362	1.673	30.06	6.65
6.55	.641	-3.51	-3.14	.222	1.558	31.82	8.46
6.57	.601	-3.88	-3.14	.196	1.416	30.92	8.59
6.60	.503	-4.57	-3.14	.155	1.106	28.66	8.53
6.64	.394	-5.36	-3.14	.117	.712	22.77	7.84
6.68	.276	-6.09	-3.14	.086	.362	14.99	6.25
6.72	.170	-6.67	-3.14	.059	.139	7.05	3.75
6.74	.103	-7.03	-3.14	.039	.049	1.46	1.00
6.76	.060	-7.29	-3.14	.025	.016	-2.13	-1.88
6.77	.043	-7.42	-3.14	.016	.006	-3.31	-3.99
6.77	.032	-7.50	-3.14	.010	.003	-3.44	-5.51
6.77	.026	-7.54	-3.14	.008	.002	-3.33	-6.33
6.77	.020	-7.61	-3.14	DC TEST ONLY			
6.77	.020	-7.61	-3.14	DC TEST ONLY			
6.77	.020	-7.61	-3.14	DC TEST ONLY			
6.77	.020	-7.61	-3.14	DC TEST ONLY			

FIJITSU FLS-50 #1333 50 OHM CKT.
3:36 PM TUE., 22 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
7.57	.868	-2.03	-.472	.694	3.407	41.30	6.91
7.57	.859	-2.01	-.514	.563	3.195	40.47	7.54
7.59	.822	-2.14	-.265	.471	2.923	39.32	7.93
7.60	.799	-2.23	-.096	.373	2.591	36.48	8.39
7.60	.776	-2.26	-.025	.287	2.197	32.40	8.84
7.61	.764	-2.28	-.004	.195	1.653	25.06	9.28
7.61	.753	-2.28	-.001	.138	1.220	18.88	9.46
7.61	.750	-2.28	-.001	.106	.935	14.54	9.48
7.61	.739	-2.28	-.001	.068	.620	9.81	9.57
7.62	.736	-2.28	-.001	.056	.504	8.00	9.56
7.61	.736	-2.28	-.001	.044	.397	6.31	9.57
7.62	.736	-2.28	-.000	.037	.333	5.28	9.55
7.62	.736	-2.28	-.000	.020	.179	2.85	9.55
7.62	.736	-2.28	-.000	.013	.112	1.77	9.51
7.62	.736	-2.28	-.000	.008	.070	1.11	9.53
7.62	.736	-2.28	-.000	.005	.048	.76	9.50
7.62	.741	-2.28	-.000	.002	.020	.32	9.52

FIJITSU FLS-50 #1333 50 OHM CKT.
3:35 PM TUE., 22 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
11.36	1.256	-1.35	-.899	.975	5.574	32.24	7.57
11.37	1.221	-1.27	-1.05	.616	5.100	32.29	9.18
11.41	1.112	-1.54	-.521	.474	4.203	29.39	9.48
11.44	1.034	-1.71	-.205	.382	3.498	26.33	9.62
11.46	.980	-1.78	-.062	.294	2.732	21.71	9.68
11.47	.951	-1.80	-.027	.234	2.187	17.90	9.70
11.48	.934	-1.80	-.015	.185	1.724	14.35	9.69
11.48	.917	-1.80	-.010	.147	1.351	11.44	9.64
11.49	.908	-1.81	-.008	.113	1.038	8.87	9.63
11.49	.897	-1.81	-.006	.073	.669	5.79	9.62
11.49	.894	-1.81	-.005	.047	.427	3.70	9.56
11.49	.885	-1.81	-.005	.030	.273	2.39	9.53
11.49	.885	-1.81	-.005	.021	.183	1.60	9.49
11.49	.882	-1.81	-.005	.015	.137	1.20	9.49
11.49	.885	-1.81	-.005	.011	.096	.84	9.42
11.49	.882	-1.81	-.005	.007	.063	.55	9.46
11.49	.885	-1.81	-.005	.005	.046	.40	9.46

FIJITSU FLS-50 #1336 50 OHM CKT.
10:29 AM WED., 23 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
11.75	.874	-1.51	.779	.847	4.375	34.37	7.13
11.76	.859	-1.41	.584	.674	4.324	36.12	8.07
11.76	.853	-1.36	.471	.564	4.173	35.96	8.69
11.75	.882	-1.16	.107	.462	3.810	32.30	9.16
11.75	.891	-1.08	-.051	.370	3.286	27.86	9.49
11.76	.868	-1.09	-.017	.271	2.540	22.24	9.72
11.76	.851	-1.10	-.008	.204	1.905	17.01	9.71
11.77	.822	-1.10	-.005	.106	.895	8.16	9.28
11.78	.813	-1.10	-.004	.068	.535	4.88	8.97
11.78	.805	-1.10	-.004	.054	.409	3.75	8.79
11.78	.807	-1.10	-.004	.039	.278	2.52	8.56
11.78	.799	-1.10	-.004	.019	.124	1.12	8.20
11.78	.802	-1.10	-.004	.010	.062	.56	8.10
11.78	.802	-1.10	-.004	.006	.038	.34	8.11
11.78	.805	-1.10	-.004	.002	.015	.13	8.07

FIJITSU FLS-50 #1336 50 OHM CKT.
10:28 AM WED., 23 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
8.27	.612	-1.95	1.611	.575	2.923	46.38	7.06
8.25	.664	-1.54	.856	.474	2.903	44.36	7.87
8.22	.761	-1.15	.091	.367	2.691	37.13	8.65
8.20	.793	-1.10	-.006	.276	2.298	31.09	9.20
8.20	.813	-1.10	-.002	.204	1.905	25.52	9.71
8.19	.822	-1.10	-.001	.148	1.502	20.12	10.08
8.19	.825	-1.10	-.001	.097	1.038	13.93	10.29
8.19	.822	-1.10	-.001	.056	.602	8.10	10.29
8.19	.819	-1.10	-.001	.038	.400	5.40	10.24
8.19	.822	-1.10	-.001	.019	.191	2.55	10.02
8.20	.825	-1.10	-.001	.010	.101	1.34	9.96
8.19	.825	-1.10	-.001	.006	.059	.79	10.00
8.19	.822	-1.10	-.001	.002	.023	.31	9.92

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FUJITSU FLC-30 #6327 50 OHM CKT.CKT.
5:20 PM THU., 24 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.71	.701	-3.76	-1.63	.592	4.213	48.22	8.52
10.71	.698	-3.62	-1.90	.476	4.092	48.35	9.34
10.73	.652	-3.88	-1.40	.390	3.649	46.56	9.71
10.76	.578	-4.27	-.669	.286	2.863	41.46	10.01
10.79	.483	-4.52	-.162	.198	1.705	32.77	9.83
10.82	.385	-4.60	-.013	.102	.916	19.55	9.54
10.83	.356	-4.61	-.006	.075	.680	15.68	9.56
10.84	.336	-4.61	-.004	.056	.505	12.32	9.56
10.85	.322	-4.61	-.003	.044	.399	10.17	9.58
10.85	.305	-4.61	-.002	.029	.260	7.00	9.59
10.86	.293	-4.61	-.001	.019	.169	4.74	9.60
10.86	.284	-4.61	-.001	.010	.090	2.59	9.62
10.86	.273	-4.61	-.001	DC TEST ONLY			

RAYTHEON RPC3315 #1 50 OHM CKT.
4:26 PM FRI., 25 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
5.54	.296	-2.51	-1.35	.101	.864	46.54	9.33
5.56	.244	-2.87	-.642	.077	.689	45.12	9.54
5.57	.207	-3.10	-.215	.063	.539	41.37	9.35
5.58	.178	-3.18	-.052	.049	.407	36.02	9.19
5.59	.152	-3.20	-.012	.037	.298	30.71	9.08
5.60	.115	-3.21	-.003	.020	.157	21.37	9.02
5.61	.095	-3.21	-.002	.012	.094	15.43	9.02
5.61	.078	-3.21	-.001	.005	.043	8.58	9.06
5.62	.063	-3.21	-.001	DC TEST ONLY			

MSC 88010 #1 50 OHM CKT.
3:02 PM MON., 28 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.41	1.187	-1.55	2.955	1.102	3.377	18.41	4.86
10.42	1.193	-1.44	2.753	.938	3.377	19.63	5.56
10.41	1.193	-1.37	2.615	.845	3.357	20.23	5.99
10.41	1.195	-1.29	2.469	.734	3.316	20.75	6.55
10.41	1.193	-1.12	2.125	.477	3.135	21.41	8.17
10.41	1.184	-1.06	2.022	.375	2.994	21.24	9.02
10.42	1.161	-.860	1.615	.185	2.248	17.05	10.85
10.39	1.253	-.285	.519	.095	1.250	8.87	11.18
10.38	1.282	-.137	.253	.075	1.028	7.16	11.36
10.37	1.310	-.001	-.012	.058	.795	5.42	11.36
10.37	1.325	.059	-.134	.047	.648	4.38	11.40
10.37	1.325	.079	-.173	.037	.516	3.49	11.41
10.37	1.322	.074	-.164	.028	.391	2.65	11.43
10.37	1.316	.064	-.144	.019	.261	1.78	11.45
10.37	1.305	.056	-.128	.010	.136	.93	11.38
10.38	1.302	.052	-.122	.005	.071	.49	11.46
10.38	1.299	.050	-.117	.002	.031	.21	11.49

MSC 8800 #1 50 OHM CKT.
3:39 PM MON., 28 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
4.03	.572	-2.86	-3.14	.194	.959	33.17	6.93
4.06	.500	-3.54	-3.14	.146	.792	31.85	7.35
4.09	.414	-4.14	-2.23	.096	.550	26.84	7.57
4.10	.368	-4.37	-1.79	.074	.416	22.69	7.49
4.11	.333	-4.52	-1.48	.057	.308	18.35	7.33
4.12	.310	-4.61	-1.32	.047	.244	15.40	7.15
4.13	.290	-4.69	-1.18	.037	.188	12.62	7.04
4.13	.273	-4.74	-1.07	.029	.142	10.01	6.87
4.14	.253	-4.80	-.952	.020	.091	6.85	6.68
4.15	.230	-4.85	-.853	.010	.043	3.49	6.40
4.15	.227	-4.86	-.831	.007	.032	2.63	6.35
4.15	.221	-4.88	-.812	.006	.023	1.96	6.29
4.16	.210	-4.90	-.768	DC TEST ONLY			

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MSC 8801Q #2 50 OHM CKT.
9:28 AM TUE., 29 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
9.70	1.520	-1.33	2.542	1.504	3.105	10.86	3.15
9.70	1.526	-1.26	2.392	1.308	3.074	11.94	3.71
9.69	1.529	-1.18	2.256	1.121	3.034	12.92	4.32
9.69	1.534	-1.11	2.123	.930	2.984	13.81	5.06
9.69	1.540	-.988	1.882	.657	2.843	14.65	6.36
9.69	1.543	-.893	1.687	.462	2.681	14.84	7.63
9.69	1.543	-.734	1.402	.242	2.308	13.82	9.80
9.68	1.578	-.366	.699	.117	1.542	9.33	11.21
9.65	1.635	0.000	-.039	.062	.910	5.37	11.65
9.65	1.652	.160	-.329	.032	.484	2.83	11.75
9.66	1.624	.093	-.202	.014	.214	1.27	11.75
9.66	1.612	.075	-.164	.007	.109	.65	11.83
9.67	1.606	.065	-.146	.002	.033	.20	11.79
9.67	1.606	.062	-.141	DC TEST ONLY			

MSC 88000 #2 50 OHM CKT.
10:50 AM TUE., 29 JAN., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
5.40	1.261	-1.83	-3.14	.245	1.552	19.20	8.02
5.42	1.213	-2.13	-3.14	.188	1.462	19.38	8.91
5.49	1.006	-3.13	-3.14	.139	1.179	18.84	9.28
5.56	.787	-4.14	-3.14	.094	.771	15.46	9.12
5.59	.707	-4.50	-3.14	.077	.598	13.18	8.90
5.63	.586	-5.04	-3.14	.053	.350	9.00	8.22
5.66	.506	-5.42	-3.14	.037	.209	6.01	7.56
5.70	.417	-5.87	-3.08	.019	.081	2.62	6.34
5.71	.376	-6.11	-2.63	.010	.038	1.28	5.60
5.72	.362	-6.19	-2.47	.008	.026	.89	5.34
5.72	.353	-6.24	-2.37	.006	.020	.68	5.16
5.72	.342	-6.32	-2.22	.004	.011	.39	4.91
5.72	.336	-6.36	-2.14	.002	.007	.24	4.80
5.72	.325	-6.44	-1.99	DC TEST ONLY			

FUJITSU FLS-50 #4039 SAMP. CRKT. NO PROBES
10:27 AM TUE., 26 FEB., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.43	.675	-2.32	6.788	.583	4.022	48.83	8.39
10.41	.727	-1.73	1.491	.477	3.941	45.77	9.17
10.41	.739	-1.60	-.009	.373	3.498	40.65	9.72
10.42	.701	-1.60	-.002	.196	2.278	28.50	10.65
10.44	.652	-1.60	-.001	.104	1.250	16.83	10.81
10.45	.624	-1.60	0.000	.055	.662	9.32	10.79
10.45	.618	-1.60	0.000	.038	.458	6.50	10.77
10.45	.615	-1.60	0.000	.027	.325	4.63	10.76
10.45	.609	-1.60	0.000	.018	.217	3.12	10.76
10.45	.609	-1.60	0.000	.010	.117	1.68	10.76
10.45	.609	-1.60	0.000	.005	.065	.94	10.78
10.45	.609	-1.60	0.000	.004	.047	.68	10.80
10.45	.609	-1.60	0.000	DC TEST ONLY			

FUJITSU FLS-50 #4037 SMP. CKT. NO PROBES
1:40 PM TUE., 26 FEB., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
11.16	.736	-2.47	12.67	.785	4.838	49.38	7.90
11.15	.773	-2.18	10.15	.660	4.828	48.36	8.64
11.13	.839	-1.87	7.435	.553	4.738	44.81	9.33
11.07	1.000	-1.36	2.578	.383	4.294	35.33	10.50
11.02	1.144	-1.08	.224	.277	3.709	27.23	11.26
11.01	1.161	-1.06	-.003	.098	1.441	10.51	11.67
11.02	1.129	-1.06	-.003	.054	.767	5.73	11.55
11.03	1.121	-1.06	-.003	.028	.391	2.94	11.46
11.03	1.115	-1.06	-.003	.017	.239	1.80	11.43
11.03	1.115	-1.06	-.003	.011	.147	1.11	11.41
11.03	1.113	-1.06	-.003	.006	.088	.67	11.43
11.03	1.109	-1.06	-.003	.004	.055	.42	11.48
11.03	1.109	-.144	8.27	DC TEST ONLY			

FUJITSU FLS-50 #3734 SMP. CKT #2 NO PROBES
4:20 PM WED., 5 MAR., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
11.43	.721	-2.08	7.466	.521	5.121	55.79	9.92
11.39	.833	-1.58	2.924	.379	4.859	47.19	11.08
11.34	.974	-1.28	.211	.277	4.213	35.63	11.82
10.02	1.017	-1.26	-.002	.188	3.064	28.22	12.13
9.07	1.017	-1.26	-.002	.159	2.550	25.92	12.06
6.22	1.014	-1.26	0.000	.093	1.210	17.69	11.12
3.74	1.014	-1.26	0.000	.055	.349	7.73	7.99
2.41	1.017	-1.26	0.000	.030	.081	2.06	4.25
1.63	1.014	-1.26	0.000	.010	.007	-.19	-1.68
1.45	1.017	-1.26	0.000	DC TEST ONLY			

FUJITSU FLS-50 #3732 SAMP. CRKT. #2 NO PROBES
1:34 PM THU., 6 MAR., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.53	.825	-2.62	6.816	.760	5.282	52.07	8.42
10.52	.856	-2.34	4.470	.660	5.252	50.97	9.01
10.51	.894	-2.09	2.000	.565	5.141	48.72	9.59
10.49	.937	-1.88	.155	.463	4.788	44.01	10.14
10.50	.925	-1.86	-.012	.284	3.457	32.66	10.86
10.50	.914	-1.86	-.007	.197	2.611	25.16	11.22
10.53	.836	-1.86	-.002	.095	1.189	12.43	10.96
10.53	.822	-1.86	-.001	.058	.713	7.57	10.92
10.54	.813	-1.86	-.001	.027	.329	3.52	10.90
10.54	.813	-1.86	0.000	.010	.123	1.32	10.86
10.54	.813	-1.86	0.000	.006	.069	.74	10.84
10.54	.813	-1.86	0.000	.003	.034	.36	10.87
10.53	.816	-1.86	0.000	DC TEST ONLY			
10.53	.816	-1.86	0.000	DC TEST ONLY			

FUJITSU FLS-50 #3731 SAM. CRKT. #2 NO PROBES S
3:44 PM THU., 6 MAR., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.56	.750	-1.91	8.278	.629	5.080	56.21	9.08
10.54	.810	-1.43	3.867	.485	4.919	51.92	10.06
10.50	.905	-1.17	1.438	.385	4.486	43.15	10.67
10.47	.997	-1.01	.038	.276	3.629	32.12	11.20
10.46	1.029	-1.01	0.000	.179	2.611	22.60	11.63
10.47	.997	-1.01	0.000	.095	1.280	11.35	11.28
10.47	.983	-1.01	0.000	.055	.733	6.58	11.21
10.48	.971	-1.01	0.000	.039	.509	4.62	11.19
10.48	.968	-1.01	0.000	.029	.377	3.43	11.16
10.48	.966	-1.01	0.000	.010	.136	1.24	11.14
10.49	.960	-1.01	0.000	DC TEST ONLY			
10.49	.957	-1.01	0.000	DC TEST ONLY			

FUJITSU FLS-50 #3726 SAMP.CRKT.#2 NO PROBES
11:13 AM FRI., 7 MAR., 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT.	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.19	.839	-1.65	12.78	.710	5.373	54.53	8.79
10.17	.902	-1.36	10.21	.561	5.221	50.78	9.69
9.97	1.477	-.269	.291	.100	1.371	8.63	11.37
9.97	1.471	-.240	.020	.057	.735	4.62	11.12
9.97	1.468	-.237	.001	.038	.491	3.09	11.13
9.97	1.460	-.237	0.000	.027	.352	2.23	11.08
9.98	1.443	-.237	-.001	.010	.124	.79	10.98
9.98	1.437	-.237	0.000	.006	.072	.46	10.90
9.98	1.434	-.237	0.000	.004	.046	.30	10.87
9.99	1.434	-.237	0.000	DC TEST ONLY			
9.98	1.437	-.237	0.000	DC TEST ONLY			

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FLC-30 #S-009
12:31 PM FRI., 30 MAY , 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
9.01	.399	-3.19	-.026	.350	2.548	61.09	8.63
9.01	.399	-3.18	.038	.326	2.519	60.95	8.89
9.01	.394	-3.18	.015	.237	2.240	56.48	9.75
9.02	.376	-3.18	.004	.157	1.827	49.18	10.66
9.02	.359	-3.18	.001	.107	1.375	39.13	11.09
9.04	.333	-3.18	0.000	.071	.939	28.83	11.23
9.04	.313	-3.18	0.000	.047	.641	20.98	11.32
9.05	.296	-3.18	0.000	.030	.410	14.18	11.40
9.05	.287	-3.18	0.000	.018	.260	9.27	11.48
9.05	.282	-3.18	0.000	.012	.165	6.04	11.57
9.05	.279	-3.18	0.000	.008	.113	4.19	11.63
9.05	.276	-3.18	0.000	.006	.081	3.02	11.67
9.05	.276	-3.18	0.000	.002	.038	1.41	11.91
9.05	.276	-3.18	0.000	DC TEST ONLY			

FLC-30 #S-008
2:56 PM FRI., 30 MAY , 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
8.96	.345	-2.60	.301	.258	1.942	54.50	8.76
8.95	.333	-2.62	.148	.218	1.856	54.90	9.31
8.95	.328	-2.63	.039	.166	1.711	52.71	10.13
8.95	.336	-2.63	.010	.110	1.442	44.28	11.19
8.95	.342	-2.63	.001	.067	1.106	33.95	12.19
8.95	.339	-2.63	0.000	.044	.789	24.57	12.57
8.96	.328	-2.63	0.000	.028	.517	16.68	12.72
8.95	.322	-2.63	0.000	.020	.378	12.43	12.78
8.95	.322	-2.63	0.000	.015	.281	9.24	12.82
8.96	.319	-2.63	0.000	.011	.205	6.79	12.82
8.95	.319	-2.63	0.000	.008	.147	4.89	12.88
8.96	.319	-2.63	0.000	.005	.106	3.51	12.94
8.96	.322	-2.63	0.000	.002	.048	1.59	13.10
8.96	.328	-2.63	0.000	DC TEST ONLY			

FLC-30 #S-007
10:22 AM MON., 2 JUNE, 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
10.27	.483	-2.57	-.089	.404	2.740	47.12	8.31
10.27	.483	-2.55	.014	.243	2.173	38.93	9.52
10.28	.425	-2.55	.001	.134	1.481	30.81	10.45
10.31	.382	-2.55	0.000	.066	.774	17.96	10.66
10.31	.356	-2.55	0.000	.030	.350	8.72	10.71
10.32	.348	-2.55	0.000	.015	.183	4.66	10.73
10.32	.348	-2.55	0.000	.008	.100	2.55	10.77
10.32	.345	-2.55	0.000	.005	.060	1.54	10.84
10.32	.348	-2.55	0.000	DC TEST ONLY			

FLC-30 #S-006
3:39 PM MON., 2 JUNE, 1980

DRAIN VOLT	DRAIN AMP	GATE VOLT	GATE M-AMP	P-IN WATT	P-OUT WATT	EFF. %	GAIN DB
9.60	.336	-2.55	-.016	.326	2.115	55.44	8.12
9.61	.330	-2.55	.009	.241	1.904	52.36	8.98
9.61	.325	-2.55	.004	.193	1.711	48.66	9.48
9.61	.322	-2.55	.001	.142	1.442	42.05	10.08
9.61	.319	-2.55	0.000	.112	1.250	37.13	10.48
9.61	.307	-2.55	0.000	.081	.961	29.80	10.75
9.61	.293	-2.55	0.000	.063	.766	24.96	10.84
9.62	.279	-2.55	0.000	.048	.590	20.23	10.91
9.63	.270	-2.55	0.000	.036	.443	15.67	10.95
9.63	.261	-2.55	0.000	.026	.332	12.12	10.98
9.63	.256	-2.55	0.000	.020	.251	9.38	11.00
9.63	.250	-2.55	0.000	.014	.184	7.03	11.04
9.63	.247	-2.55	0.000	.010	.132	5.10	11.07
9.63	.247	-2.55	0.000	.008	.099	3.84	11.08
9.63	.244	-2.55	0.000	.003	.036	1.40	11.26
9.64	.247	-2.55	0.000	.003	.036	1.39	11.27
9.63	.250	-2.55	0.000	DC TEST ONLY			