MCDONNELL DOUGLAS CORPORATION

SCIENCE AND APPLICATIONS SPACE PLATFORM (SASP) END-TO-END DATA SYSTEM STUDY

FINAL REPORT

APRIL 1981

MDC G9372

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PREFACE

This document contains material prepared by McDonnell Douglas Astronautics Company on the Science and Applications Space Platform (SASP) End-to-End Data System Study as defined in the Statement of Work for Contract NAS8-33592 by Marshall Space Flight Center where the contact is:

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CONTENTS

FIGURES

FIGURES (Cont'd)

FIGURES (Cont'd)

EXECUTIVE SUMMARY

Science and Applications Space Platforms (SASPs) (Figure 1) offer a cost effective means for performing low earth orbit science and applications space missions. These platforms offer payloads extended duration missions (compared to the Shuttle payload bay), centralized power, command and data acquisition, communications, pointing and environmental control services, and periodic Shuttle visits for maintenance, replenishment of consumables, and payload changeout. By their nature, platforms must be capable of providing data and communications services to groups of payloads in which the individual payloads may or may not have common objectives and operating characteristics, and where the payload mix on a platform changes periodically during the orbital life of the platform.

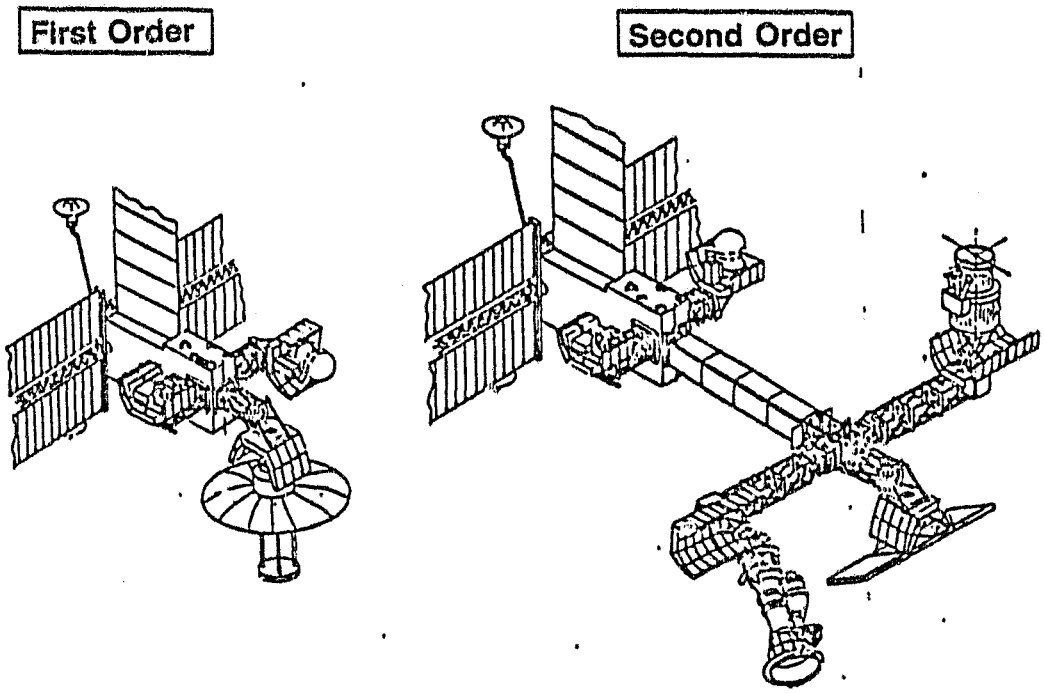


Figure 1. Basic Platform Family

At that same time that platforms are expected to become a basic part of the Space Transportation System, payload sensors are expected to have increasingly larger bandwidths and hence will be capable of producing data at higher and higher rates. Figure 2 shows the past and projected growth in data acquisition for NASA programs with certain data intensive payloads/ programs shown. This chart was presented by Dr. William P. Raney of NASA-HQ at a recent AIAA conference. The data projected for two possible SASP payload groups, identified as SASP-A8 and SASP-F5, have been added to the figure.

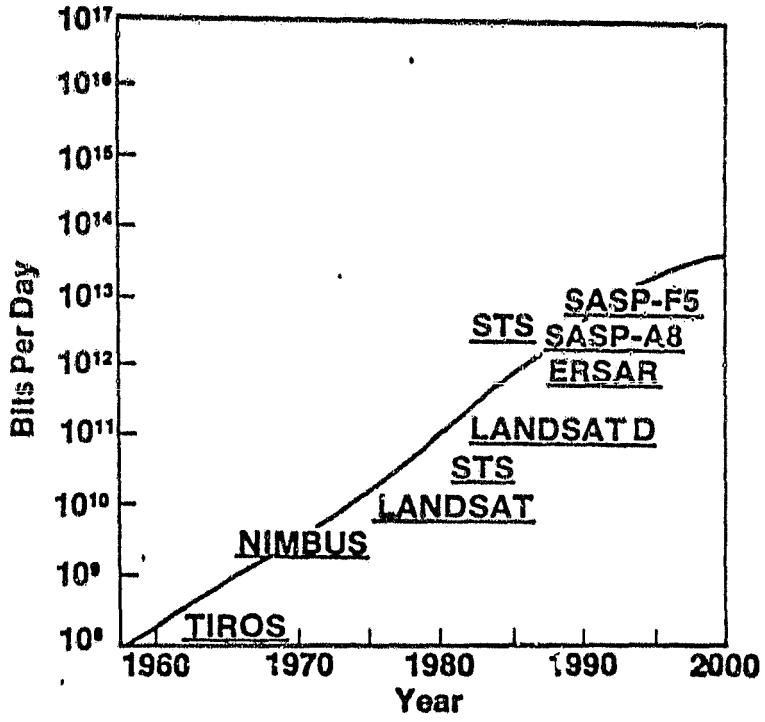


Figure 2. Data Acquisition Growth

The SASP End-to-End Data System Study was initiated to study the data implications of Science and Applications Space Platforms and to achieve three principle objectives:

1. Evaluate the capability of present technology and the Tracking and Data Relay Satellite System (TDRSS) to accommodate SASP Payload User's Requirements.

2. Optimize the SASP Onboard Command and Data Management System (CDMS) to provide the maximum service to the user.

3. Assess the ability and availability of new technology to accommodate the evolution of SASP payloads.

The approach selected to meet these objectives was to start with results generated by earlier Marshall Space Flight Center studies and 1) survey industry and government to determine the status of and projections for key data system hardware elements, 2) configure a SASP data system based on current and near-term technology, 3) evaluate the performance of that data subsystem in support of two selected candidate SASP payload groups using the MSFC Data System Dynamic Simulator Facility, and 4) make recommendations for SASP data system optimization and for data system technology development necessary to support an evolving SASP program.

Two payload groups were selected for analysis on the basis that they were representative of an early first-order platform payload group and a late 1980's second-order platform group. Each group was selected because it appeared to present stressing requirements to the SASP data system. The payload groups, designated A8 and F5, were originally defined in the SASP Payload Accommodations Study[1]. The A8 payload group had a peak composite data rate of approximately 90 Mbps; F5's peak composite rate exceeded 300 Mbps.

Preliminary analysis showed that the key technology items related to accommodating these payload groups on a SASP were on-board storage devices, multiplexers and on-board data processors. The technology survey focused on these items. It was found that the on-board mass storage technology for the 1980s will continue to be based on magnetic tape recorders, with bubble memory devices being possible candidates for specialized applications. The development of space-qualified versions of current ground tape recorder technology could extend the capability to the area of 10^{12} bits of total storage and read/write rates on the order of 300 Mbps. Space tape recorders with this capability will be needed in the late 1980s to support SASP and other space programs but are not currently being developed.

Multiplexer technology is evolving with the higher speed logic development being done for commercial and military application. The capability to provide flexibility within a high rate multiplexer at rates of 300 Mbps is considered to be well within the capability of the technology but is not presently being developed for NASA applications. The SASP Data Management system should be configured to provide this capability.

On-board data processing capability is growing as data processor technology continues to move at a fast pace. Data processing systems to support sensor output data handling (and payload control) tend to have payload-unique software and architecture. The SASP data system should be configured to accommodate payloads that contain dedicated data processors and encouragement should be provided for the development and use of such processors.

The analysis of the SASP data system performance with the A8 payload group showed that the SASP data system and the TDRSS are capable of supporting a payload group of this class. Special attention must be paid to providing an on-board storage capability that is consistent with a realistic TDRSS data dump schedule. Another area that needs special consideration is the accommodation of payloads that seek to acquire high rate, event-driven data. Such payloads should be encouraged to provide on-board, autonomous data-capture-and-save capability.

The F5 payload group data system analysis showed that a large portion of the data would be lost when using foreseeable on-board storage capability and reasonable TDRSS timeline allocations. Two suggestions are made for alleviating the data loss for payload groups such as F5: (1) encourage on-board processing of the data from high rate sensors, such as synthetic aperture radars, so that the amount of data that must be acquired on the ground is minimized, and (2) consider providing a dedicated data acquisition, communication, and ground processing capability for such high rate payloads.

The study identified several potential problems that were not explored in depth. These include: (1) the potential need for increased bandwidth in the real-time, dedicated communications channel available to a SASP payload group, (2) the potential overload of ground data processing, distribution, and

storage facilities, (3) the need to assure understanding in the payload community of SASP data issues and concepts, and (4) the need to develop and enforce standards and protocols for the various interfaces in the SASP data system.

The Science and Applications Space Platform provides a logical next step in space exploration and utilization. Data systems can be provided to support a SASP program. Modest extensions of existing technology will allow the SASP to accommodate the foreseeable evolution of payloads through the 1980s. Careful system planning and extensive coordination is needed to assure that the SASP data system evolves to meet user needs in a cost-effective manner.

Section 1
INTRODUCTION AND STUDY APPROACH

The SASP End-to-End Data System Study was added to the SASP Conceptual Design Study to meet three objectives. They were:

1. Evaluate the capability of present technology and the TDRSS to accommodate SASP payload user requirements.
2. Optimize the SASP Onboard Command and Data Management System (CDMS) to provide maximum service for users.
3. Assess the ability and availability of new technology to accommodate the evolution of SASP payloads.

The study plan that was defined to meet these objectives is shown in Figure 1-1.

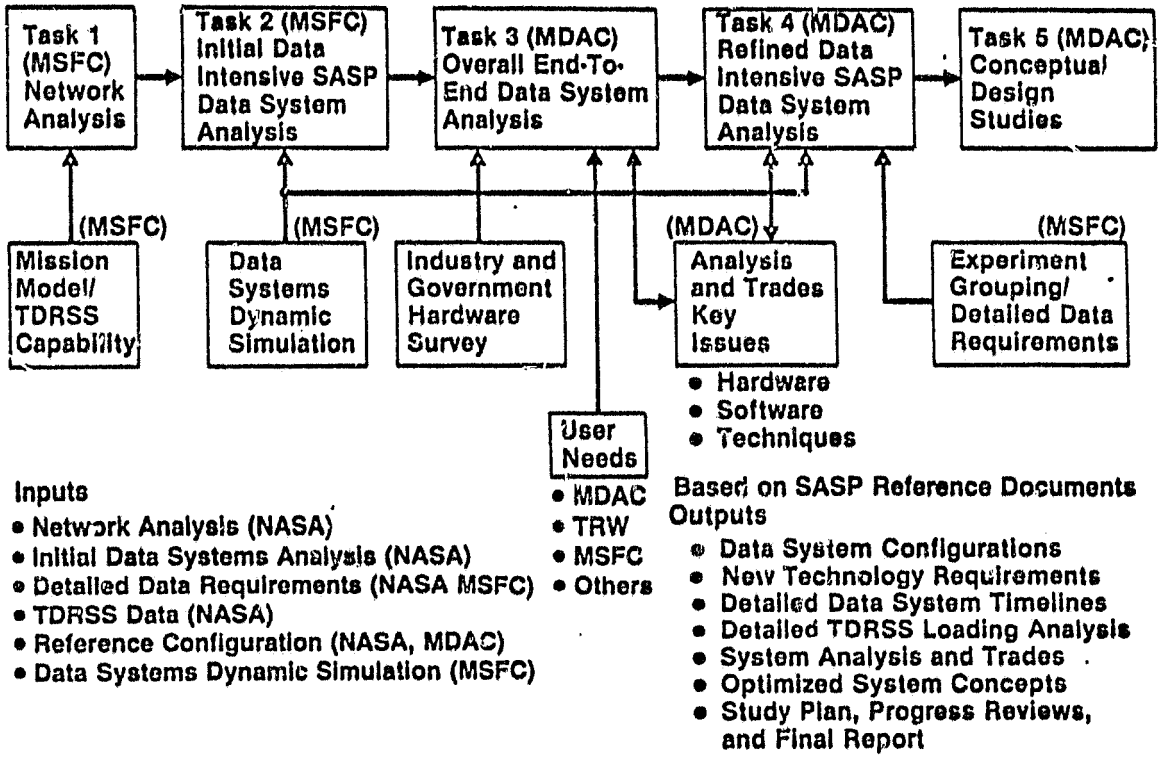


Figure 1-1. SASP End-to-End Data Analysis Study

The study was divided into five tasks as shown. Task 1, Network Analysis and Task 2, Initial Data Intensive SASP Data System Analysis, were performed by the MSFC Data Systems Laboratory. Tasks, 3, 4, and 5 were performed by the McDonnell Douglas Astronautics Company.

Task 3, Overall End-to-End Data System Analysis, included an evaluation and expanded definition of user data requirements, a survey of current and projected technology applicable to SASP data systems, and the identification of hardware that meet SASP needs.

Task 4, Refined Data Intensive SASP Data System Analysis, included the definition of a SASP data system, the selection of two candidate payload groups, the formulation of data flow simulations of each of those payload groups in conjunction with the SASP data system and TDRSS, the running of the simulations on the MSFC Data Systems Dynamic Simulator (DSDS), and the evaluation of the simulation results.

Task 5 included trade studies and user reviews, generation of system description, and the preparation of study documentation.

Task 3 activity is reported in Sections 2 (User Requirements) and 4 (Technology Survey) of this report. Task 4 activity is described in Section 3. Task 5 activity is described in Sections 3 and 5. The study schedule is shown in Figure 1-2.

Features of the MDAC approach to Tasks 3 through 5 are shown in Figure 1-3. User requirements definition and evaluation was based on two selected payload groups. These groups were selected from a larger set of payload groups defined by the SASP Payload Accommodations Study.

The selected payload groups, denoted as A8 and F5, were selected using the criteria shown in Figure 1-4, which also defines the major characteristics of each payload group. It was intended that one group (A8) be representative of a stressing (from a data standpoint) payload group that is a candidate for a first order SASP and that the second group (F5) be representative of a stressing secondary second order SASP payload group.

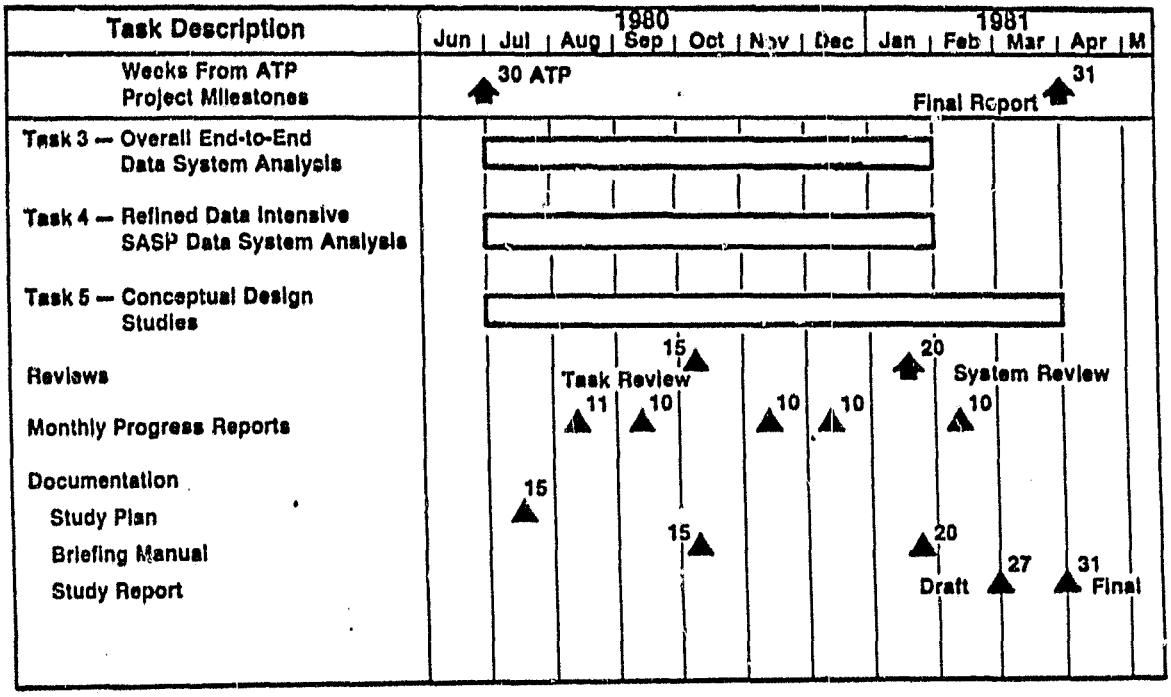


Figure 1-2. End-to-End Data System Study Schedule

- **User Requirements**
  - Select Payload Groups
  - SASP Data Base
  - SASP Payload Accommodations Study
  - User Contact
- **Technology Evaluation**
  - Literature Search
  - Conferences
  - Technical Discussion
  - Peer Group Review
- **Data System Analysis**
  - User MSFC Data System Dynamic Simulation
  - Define Initial Data Subsystem

Figure 1-3. Study Approach

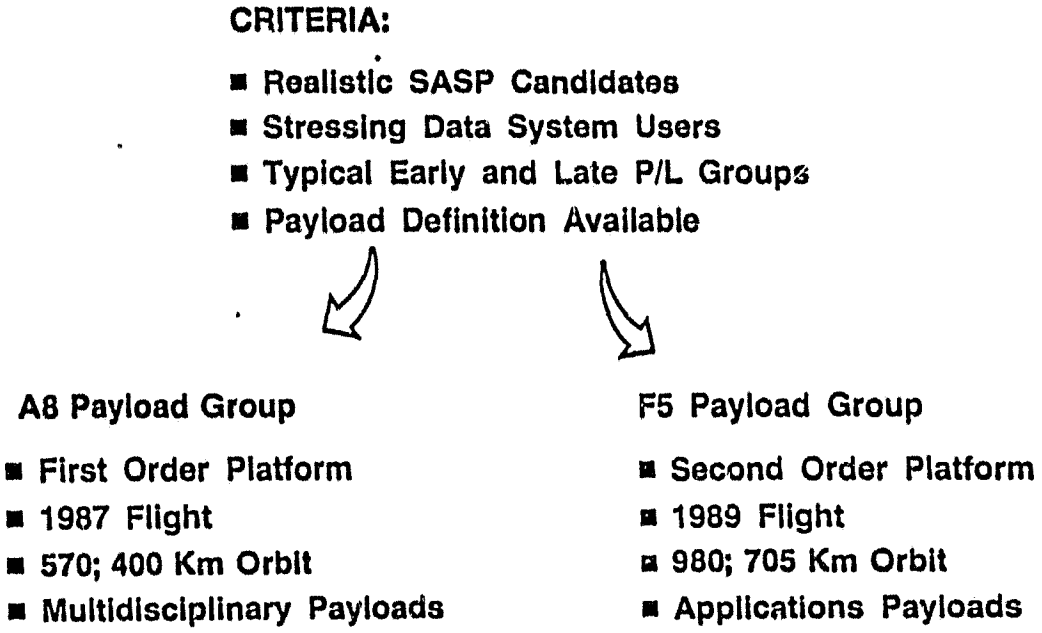


Figure 1-4. Payload Group Selection

Data characteristics and requirements for the payloads within the groups were developed from a variety of sources as shown in Figure 1-5. The MDAC computerized payload descriptive data base was used to define payload data requirements envelopes (using information on approximately 80 payloads) and to provide the initial data requirements for some of the payloads in the A8 and F5 groups. This data was supplemented by information from other sources including contacts with principal investigators and payload developers. These contacts were particularly useful in helping to define payload sensor operating timelines which were important in the data flow simulations.

Data flow analyses were performed using the Data System Dynamic Simulator at MSFC. This simulator facility provides a versatile capability for evaluating data system performance. Figure 1-6 is an overview of this capability showing as inputs the mission parameters and constraints (e.g., orbital parameters of SASP, TDRSS location and availability parameters, sensor target criteria) and the SASP data system model. Outputs include a number of reports on mission model performance, data system performance (Device Utilization Model Report), and operations and cost reports.

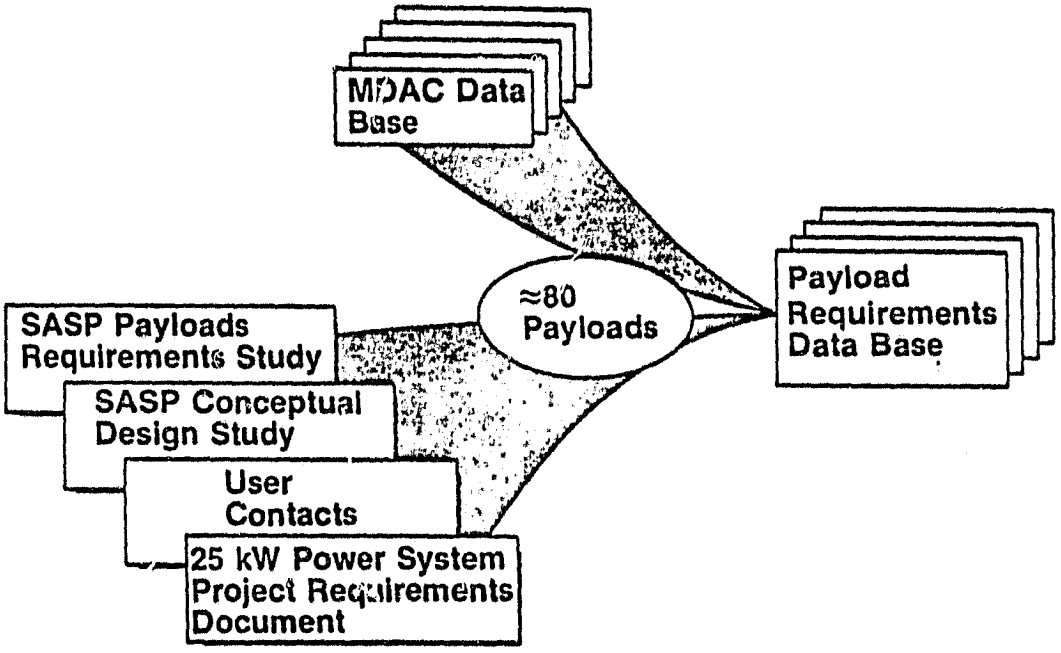


Figure 1-5. User Requirements as Developed for the End-to-End Study

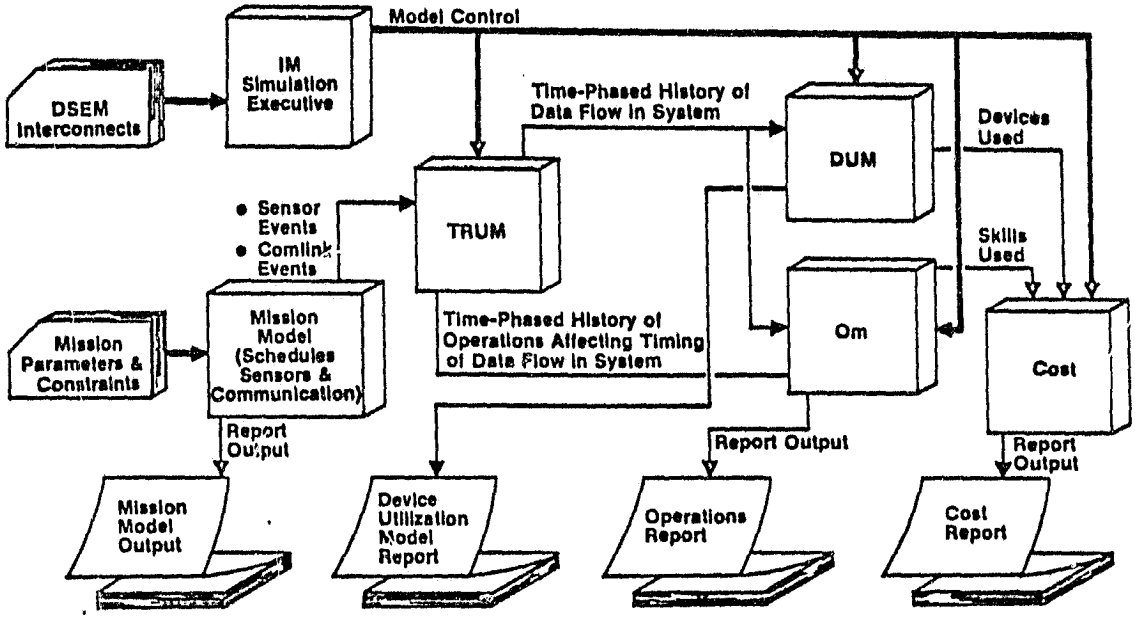


Figure 1-6. DSDS Description

Figure 1-7 depicts the DSDS configuration and functional flow as it was applied in this study.

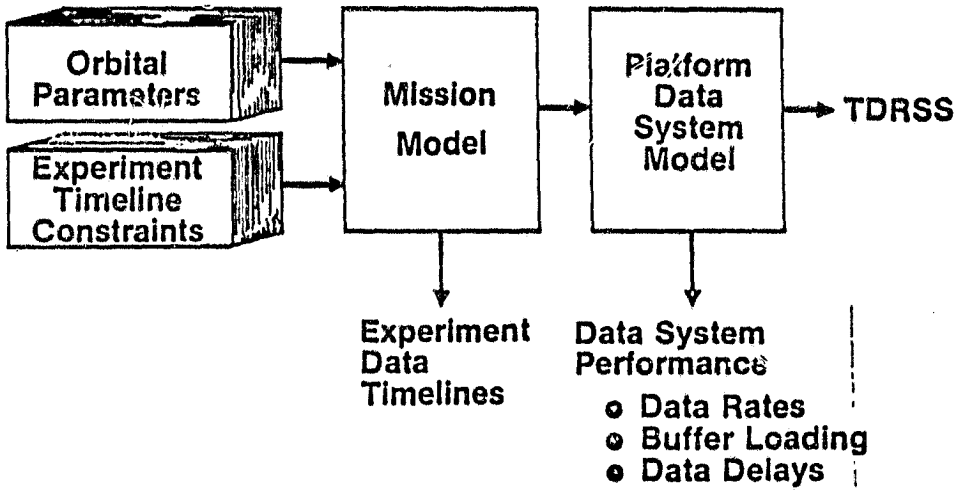


Figure 1-7. Data System Dynamic Simulator

The study approach to assessing the ability and availability of current and projected technology to support SASP needs was fourfold, as shown in Figure 1-8. An extensive literature search through the MDAC engineering library was used to access current literature published by industry, NASA, and DOD. Simultaneously, a survey of leading suppliers and NASA technology groups was conducted. Members of the MDAC study team attended several technical conferences that addressed new technology in the appropriate fields. Finally the summary results of this activity were reviewed and refined by senior technical review groups within MDAC.

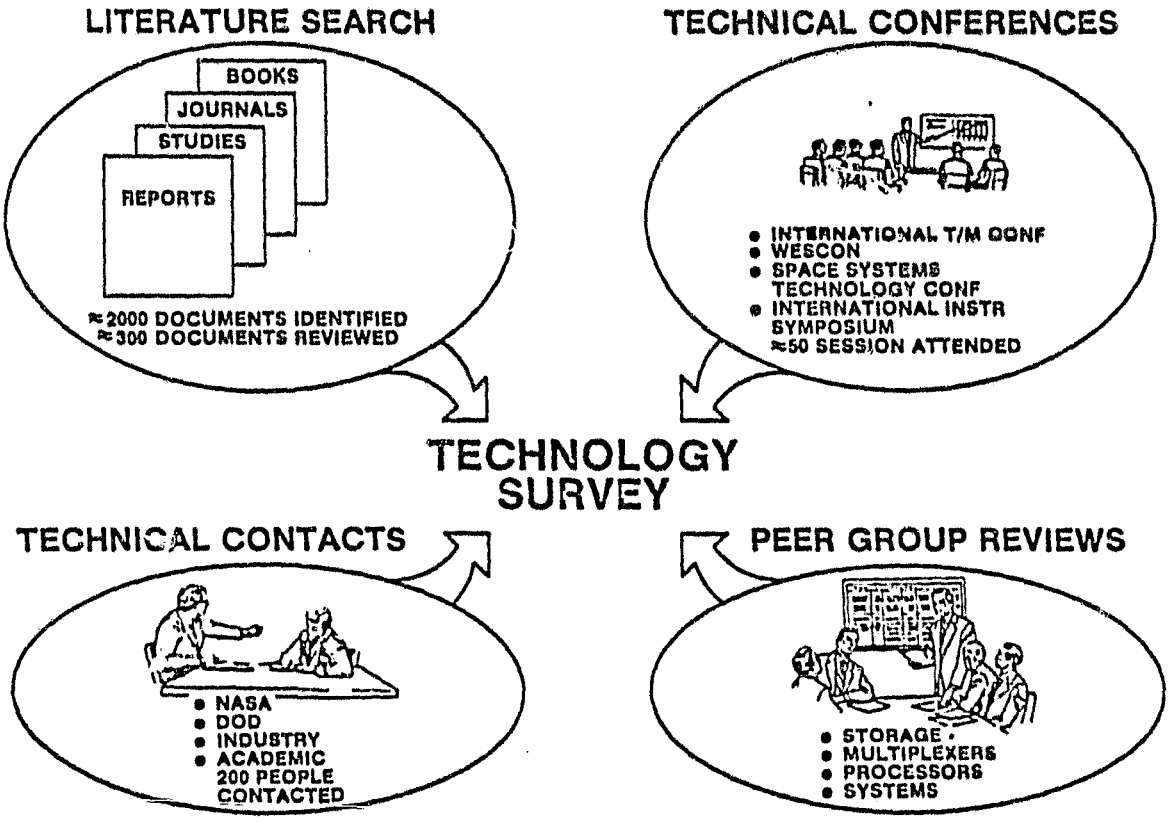


Figure 1-8. Technology Survey

Section 2
USER REQUIREMENTS

The communication and data requirements for space platforms are largely driven by the needs of payloads. The platform CDMS, of course, must be capable of handling several (3-10) payloads during any mission phase and must be able to support periodic payload changeout. Payload data support requirements for the late 1980s were formulated by collecting data requirements for a large set of payloads thought to be SASP payload candidates, or at least thought to be representative.

Many of the approximately 80 candidate payloads that were reviewed are currently planned for Spacelab. Others are only conceptually defined at this time and have broadly stated data requirements. Using Spacelab payloads as design requirements generators for a SASP CDMS requires caution for the following reasons:

1. Spacelab payloads are designed for a 7-10 day mission. Use of the same type payload on a SASP for 3 to 6 months or more would probably result in a much different operating timeline and consequently a (possibly) different data rate.
2. Spacelab payloads may be constrained by the data gathering and communications capability provided by Spacelab and Shuttle. The optimum peak and/or average data rate may be higher than that used in the Spacelab.
3. Spacelab payloads are often designed to take advantage of the on-board payload specialists capabilities to monitor and operate the payload. A different operational approach is required to fly the same payload on an unmanned SASP. This different approach would likely affect the command and downlink data rates.

Payloads in the data base that are not Spacelab payloads are, for the most part, conceptual designs at this time. These payloads do not usually have well-defined data requirements. Often the only requirement available is a peak downlink data rate. Average data rates, data timelines, data descriptions command requirements, and on-board processing support requirements are not readily available.

During the study, the data requirements for the full set of 80 payloads was examined to provide an envelope of peak downlink data rates. A set of 16 Design Reference Missions (DRMs) from the Phase B Power Systems Study was also reviewed for downlink peak rate requirements. These requirements are summarized in Figure 2-1. This figure shows the cumulative percentage distribution of peak downlink data rates for the 80 individual payloads as well as for the 16 Power System DRMs.

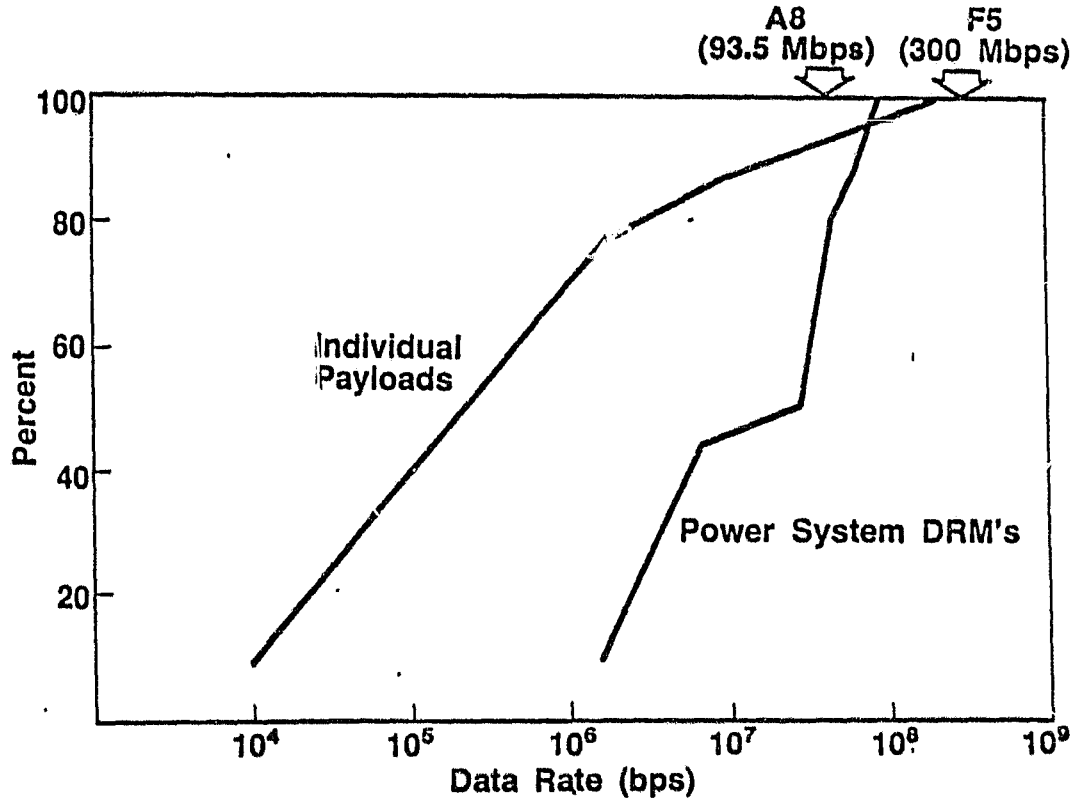


Figure 2-1. Distribution of Peak Data Rates

The median data rate for the individual payloads is approximately 200 Kbps, the 90 percentile level is 30 Mbps, and the highest data rate is 120 Mbps (2 Synthetic Aperture Radar Payloads). For the Power System DRMs, the peak data rate for any DRM was defined as the sum of the peak data rates for the individual payloads in the worst case (from a data rate standpoint) payload group in that DRM. The median DRM peak data rate is seen to be approximately 10 Mbps and the highest DRM peak data rate is just less than 100 Mbps. The DRM did not include all of the 80 individual payloads. This is why the highest DRM data rate is less than the highest individual payload data rate.

Command rates are of concern because of Spacelab experience and because of the scheduling constraints associated with TDRSS forward links. However, examination of the SASP payload data base showed that most payload command requirements are for rates in the 1-2 Kbps range with the highest rate defined as 25 Kbps (see Figure 2-2). Command error-correcting and verification requirements will tend to increase the effective channel bit rate that is needed. In addition, since SASP will carry several payloads and because TDRSS forward link time may be a scarce resource, the SASP CDMS has baselined a 300 Kbps command channel for payload usage. Figure 2-2 shows how time division multiplexing could be used to, in effect, provide a dedicated port with some fraction of the 300 Kbps capability. The payload's use of this channel would be constrained only by TDRSS channel scheduling and overall platform command compatibility restrictions.

Figure 2-1 also shows the peak data rates for the A8 and F5 payload groups, which were the focus of this study. To allow data flow simulations for these two groups it was necessary to define operating timelines for each payload in each group. This was done by reviewing available documentation, contacting principal investigators and payload developers, and in some cases, making educated guesses. Figures 2-3 and 2-4 show the resulting timelines for A8 and F5, respectively.

- **SASP Payload Data Base**
  - Most Defined Requirements are in 1-2 Kbps Range
  - Highest Rate Identified is 25 Kbps
- **Need to Consider Simultaneous Command Requirements**
- **Ample Bandwidth Available**
  - TDRSS MA 10 Kbps
  - TDRSS SSA 300 Kbps
  - TDRSS KSA 25 Mbps
- **Suggest Time Multiplexed Sharing of 300 Kbps SASP Command Link**

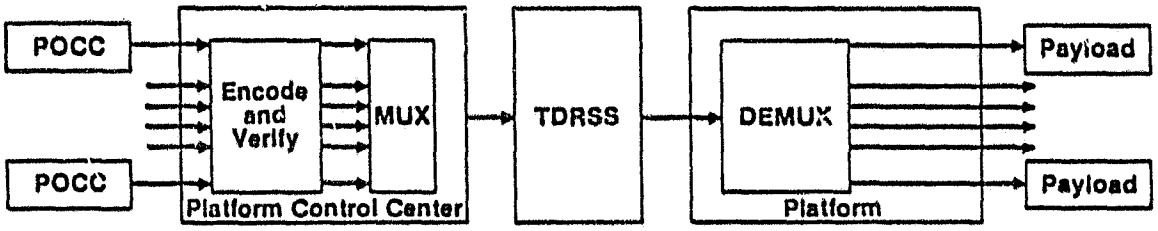


Figure 2-2. Command Link Data Rates

EO-1 Target: Sun
Operates Continuously Except During South Atlantic Anomaly. Instrument is Off When Electrons are >3 MeV With a Flux >10 Particles/cm^2

UARS Target: Earth
Takes 20 Minutes of Data When Activated.
50 Percent Duty Cycle Over Entire Orbit

RO-2 Target: Earth — Daylight Portion of Orbit
20 Kbps of Housekeeping Data Continuously; Additional 320 Kbps Data During Daylight Portion of Orbit

EO-2 Target: Earth
20 Kbps and 4.6 Mbps Continuous Data. 16 Mbps Data has 50 Percent Duty Cycle Over Entire Orbit at 20 Minute Intervals.

SOT Target: Sun
50 Kbps Continuous; 5 Mbps has 4 Percent Duty Cycle (Sun Only). High Rate Data (60 Mbps) is Random Event Driven Occurring 3 Times a Day. 30 Minutes of 60 Mbps Data for Each Event.

Figure 2-3. A8 Data Time Lines

RO-1

Thematic Mapper — Target: Earth
- Data Rate: 85 Mbps
- Duty Cycle: 2 Percent
- Maximum Delay For Data Dump: Realtime if Possible or 1 Orbit
- Specific Targets: Land Mass Over Continental U.S.

Spectroscopic Imaging System — Target: Earth
- Data Rate: 32 Mbps Plus 2 Kbps (Housekeeping at 100 Percent)
- Duty Cycle: 17 Percent
- Maximum Delay for Data Dump: 2 Orbits
- Specific Targets: Land Mass on Sunlit Side

Multispectral Resource Scanner — Target: Earth
- Data Rate: 30 Mbps
- Duty Cycle: 17 Percent
- Maximum Delay for Data Dump: Realtime if Possible or 1 Orbit
- Specific Targets: Sunlit Land Masses

Fraunhofer Line Discriminator — Target: Earth
- Data Rate: 50 Kbps
- Duty Cycle: 21 Six Minute Observations at 10:00 am to 2:00 pm (Standard Time of Nadir Observation)
- Maximum Delay for Data Dump: No Restriction — Anytime
- Specific Targets: Continental U.S. Land Mass

SMR-PA
- Target: Earth
- Data Rate: 8 Kbps
- Duty Cycle: 100 Percent
- Maximum Delay for Data Dump: Realtime with 2 Orbits (Max.)
- Specific Targets: Earth with Land Calibration

LFS
- Target: Earth
- Data Rate: 100 Kbps
- Duty Cycle: 32 Percent
- Maximum Delay for Data Dump: 2 Orbits
- Specific Targets: Dark Side Oceans

MMIRI
- Target: Earth
- Data Rate: 30 Mbps
- Duty Cycle: 50 Percent
- Maximum Delay for Data Dump: Realtime if Possible or 1 Orbit
- Specific Targets: All Land Masses

UARS
- Target: Earth
- Data Rate: 50 Kbps
- Duty Cycle: 61 Percent
- Maximum Delay for Data Dump: 2 Orbits (Max.)
- Specific Targets: Limb Solar Occulation and Earth

OSAR
- Target: Earth
- Data Rate: 120 Mbps
- Duty Cycle: 25 Percent
- Maximum Delay for Data Dump: Realtime if Possible or 1 Orbit
- Specific Targets: Oceans and Artic Ice, Anytime (Day or Night)

Figure 2-4. F5 Data Timelines

Most of the data timelines are driven by predictable target occurrences (e.g., land, sun-lit land, oceans). However, SOT is a notable exception in that the data rates are event-driven. That is, the data rate is higher during a particular event of interest, a solar flare, which is of course not scheduleable. As will be seen in the next section, this type of requirement has significant impact on the data system design and operating concept.

Figure 2-5 depicts the Reference Power System (Reference 1a) CDMS as modified for this study. Modifications to the Reference Power System concept were made to accommodate the payload data requirements envelope and include the following changes:

1. Increase the KSA channel downlink data rate from 226 Mbps to 300 Mbps to match the maximum TDRSS data rate capability.
2. Add one, two, or three Spacelab-type high data rate recorders to provide a scientific data storage resource for payloads.
3. Substitute a current technology high rate multiplexer for the Spacelab HRM included in the Reference Power System CDMS. This last change was suggested because of the requirement to accommodate several payloads with rates at or exceeding 50 Mbps.

A conceptual design of the current technology multiplexer was performed to assure feasibility. The input-output requirements are shown in Figure 2-6. The conceptual design is shown in Figure 2-7. The multiplexer uses a two-tiered multiplexing scheme to accommodate the wide range of input data rates. Format flexibility is provided by using microprocessor control of the multiplexer operation. Formats are defined by instructions in the microprocessor memory, which can be a combination of ROM and RAM, allowing for both pre-defined formats and on-orbit format changes.

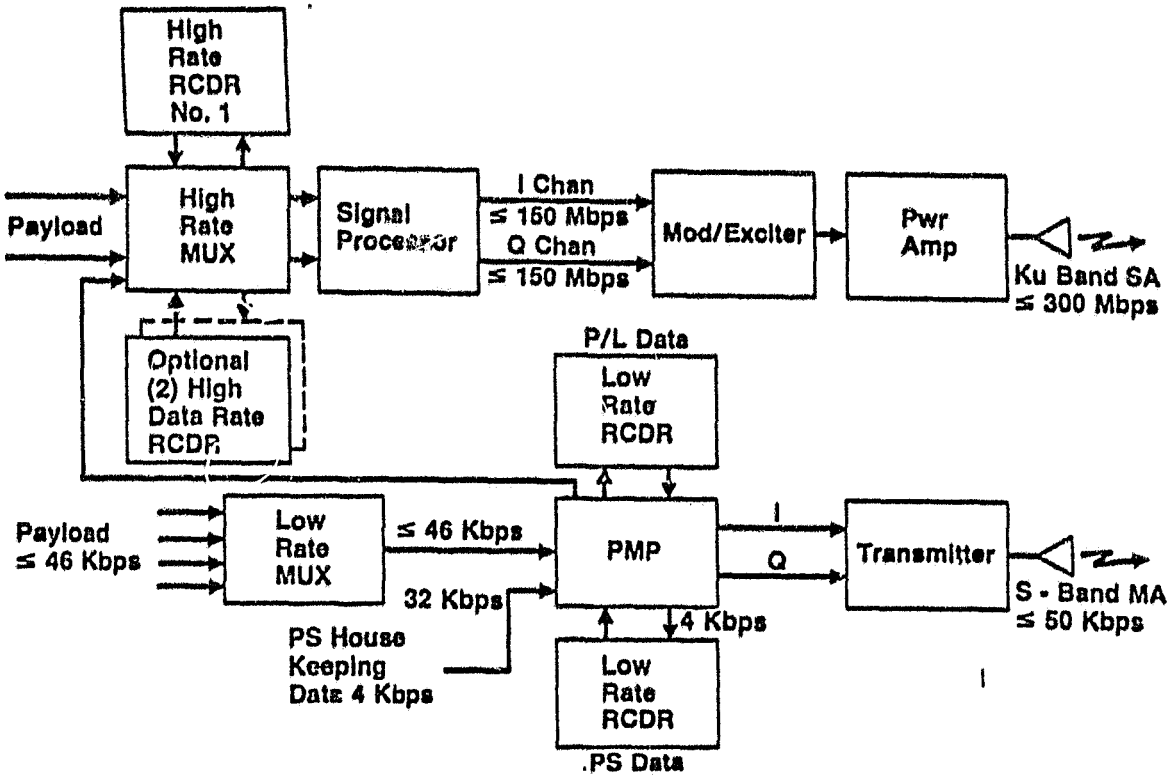


Figure 2-5. Modified NASA Reference Power System Data Subsystem

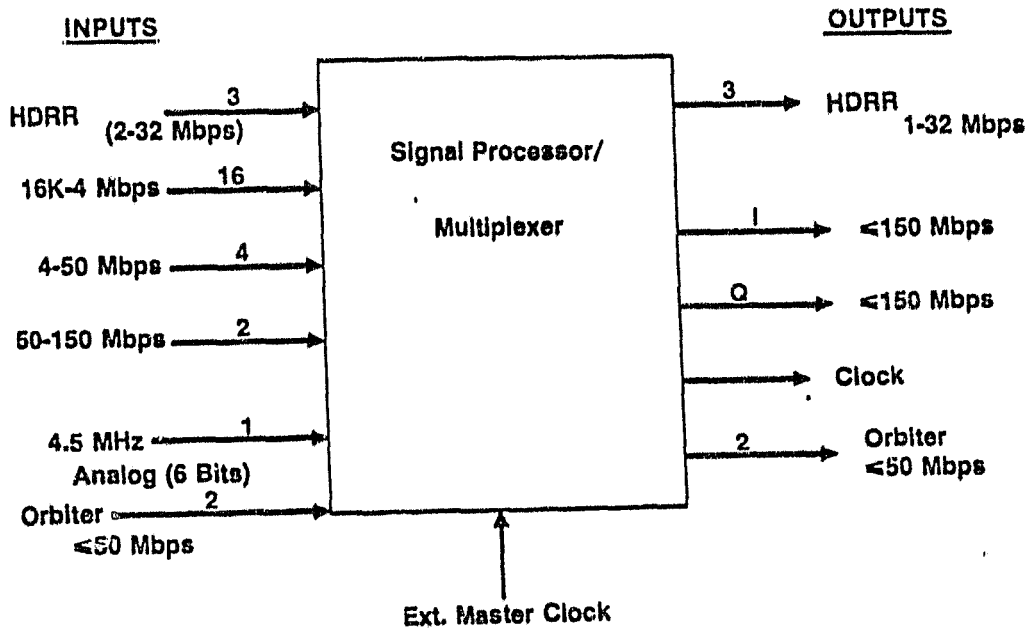


Figure 2-6. Simplified Multiplexer Diagram

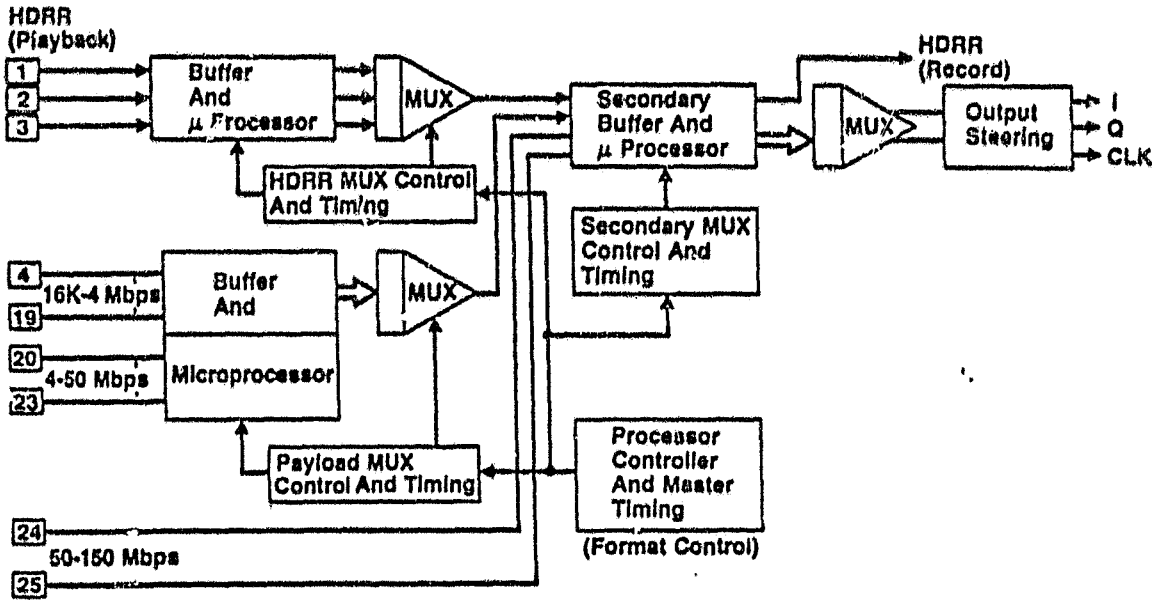


Figure 2-7. Multiplexer Functional Diagram

Section 3
DATA SYSTEM ANALYSES

The data flow in the SASP CDMS and the TDRSS was analyzed for two payloads, designated as A8 and F5. The A8 and F5 payload groups were selected from payload groups defined in the SASP Payload Accommodations Study (Ref. 1). These particular payload groups were selected primarily because they were stressing for the SASP CDMS and were felt to be realistic first-order (A8) or second-order (F5) platform payload group candidates.

A. A8 Payload Group

Payload group A8 was intended to be a data subsystem stressing group that is a candidate for a first-order platform. A8 was defined in the SASP Payload Accommodations Study and includes the individual payloads shown in Figure 3-1. The EO-1 payload is a pallet-size group of instruments whose common objective is environmental observation. The instruments included in EO-1 are: Active Cavity Radiometer, Solar Spectrum Measurement, Variation in Solar Constant, and Solar Ultraviolet Spectral Irradiance Monitor. The Upper Atmospheric Research Satellite (UARS) is currently planned as a free-flyer but was earlier identified as a candidate SASP payload. RO-2 is a pallet grouping of resource observation instruments that includes: Orbiter Large Format Camera, Ocean Color Experiment, Feature Identification and Location Experiment, Spacelab Geodynamic Ranging System, and Time Transfer Experiment. Payload EO-2 is, like EO-1, a pallet of environment observation instruments that includes: Atmospheric Tract Molecules, High Resolution Doppler Imager, Microwave Limb Sounder, and Measurement of Air Pollution from Shuttle. SOT is the Solar Optical Telescope.

The analysis approach for the A8 payload group is shown in Figure 3-2. Peak data rates for each payload in the group were established from published payload requirements documents or from interviews with payload developers.

- First Order Platform
- 57°, 400 km Orbit
- Multidisciplined
  - Solar Physics
  - Resource Observations
  - Environmental Observations
  - ISPM Science Support
- 1987 Flight
- Payload Grouping Includes
  - EO-1
  - UARS
  - RO-2
  - EO-2
  - SOT

Figure 3-1. A8 Configuration

- Establish Experiment Data Rates
- Establish Experiment Data Time Lines Constraints
- Assign Experiment Outputs to MUX Channels
- Establish Simulation Ground Rules
- Run Simulation
- Evaluate

Figure 3-2. A8 Analysis Approach

Experiment data timelines were established similarly by defining the observation opportunities and constraints as shown in Figure 2-3. The payload data outputs were assigned to the SASP high rate mux and low rate mux inputs as shown in Figures 3-3 and 3-4. Simulation ground rules were established that defined a TDRSS timeline generation methodology and the SASP data recorder operating rules.

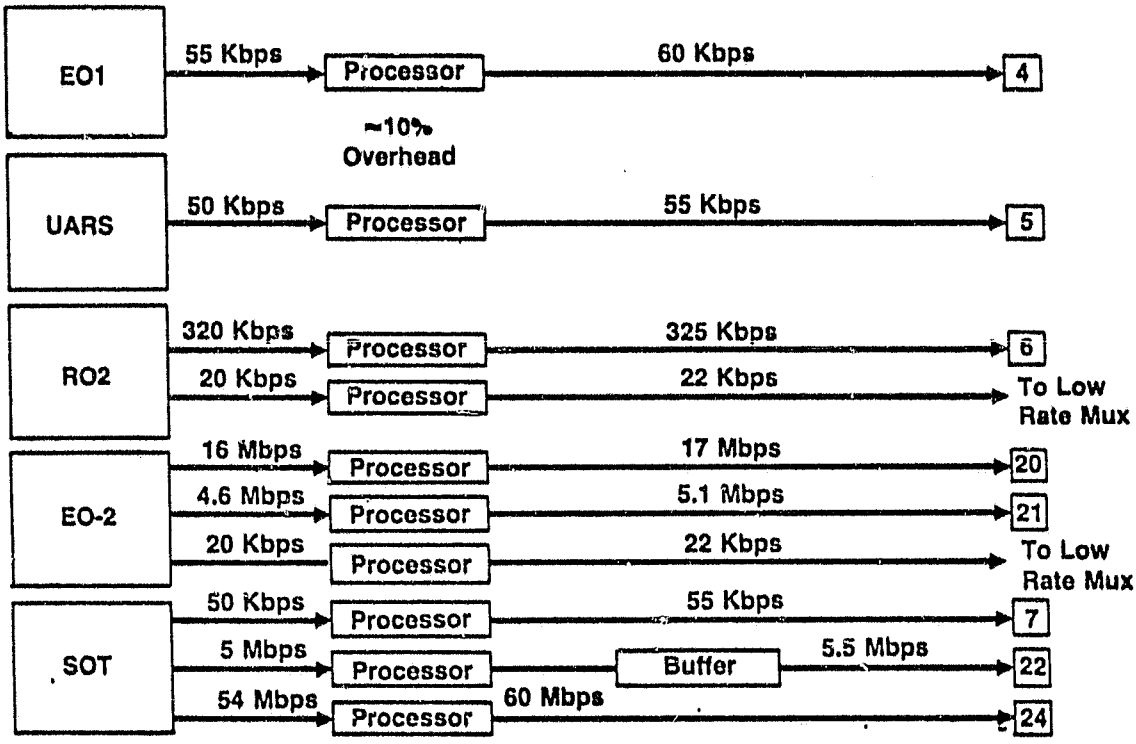


Figure 3-3. A8 Configuration Maximum Data Rates

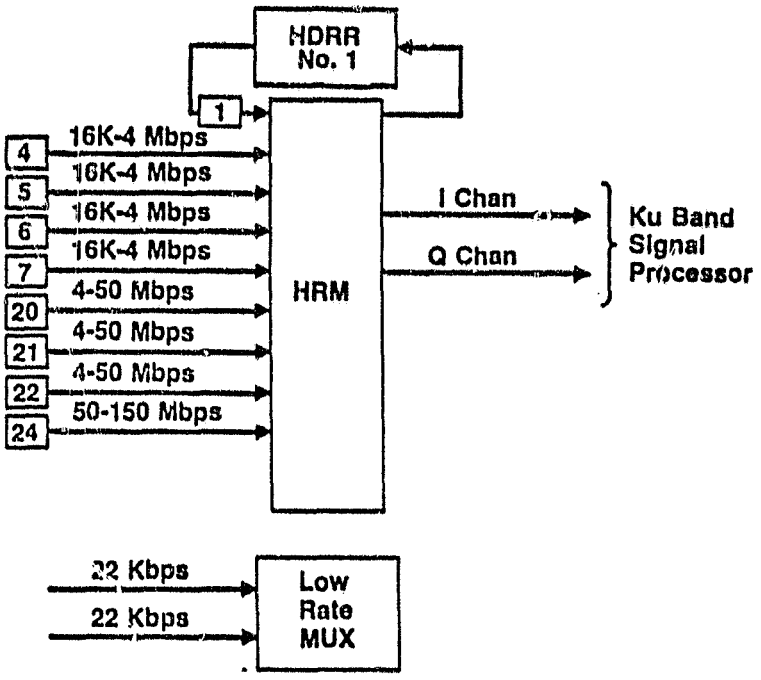


Figure 3-4. MUX Configuration for A8 Payload Group

Figure 3-5 depicts the TDRSS timeline simulation for six (6) hours of the A8 simulation. The TDRS-E and TDRS-W line-of-sight (LOS) timelines for the A8 orbit were generated by the MSFC Resource Scheduler computer program. An A8 schedule block for TDRSS was placed within each LOS timeline block at a fixed time after initiation of LOS and with a fixed duration. For the A8 simulation, each scheduled TDRSS timeline block started 10 minutes after the start of LOS and lasted for 10 minutes. The TDRS-E and TDRS-W timeline allocations were combined to define the total TDRSS timeline allocation for A8. This resulted in two 10 minute blocks for typical orbits.

The A8 mission was simulated on the MSFC Data System Dynamic Simulator. Figure 3-6 shows the nature of the simulation and some of the results of a 24-hour mission. The Experiment MUX function combined the time-varying data streams from the payloads to produce a composite data stream with a mean rate of 15.6 Mbps and a peak of 93.5 Mbps. The switch (SW) function routes the composite data stream directly to the output MUX and then to TDRSS when TDRSS is available (during a TDRSS schedule block). When TDRSS is not scheduled, the data stream is routed to a Rate Switch function. This function compares the data stream peak rate to the on-board recorder peak

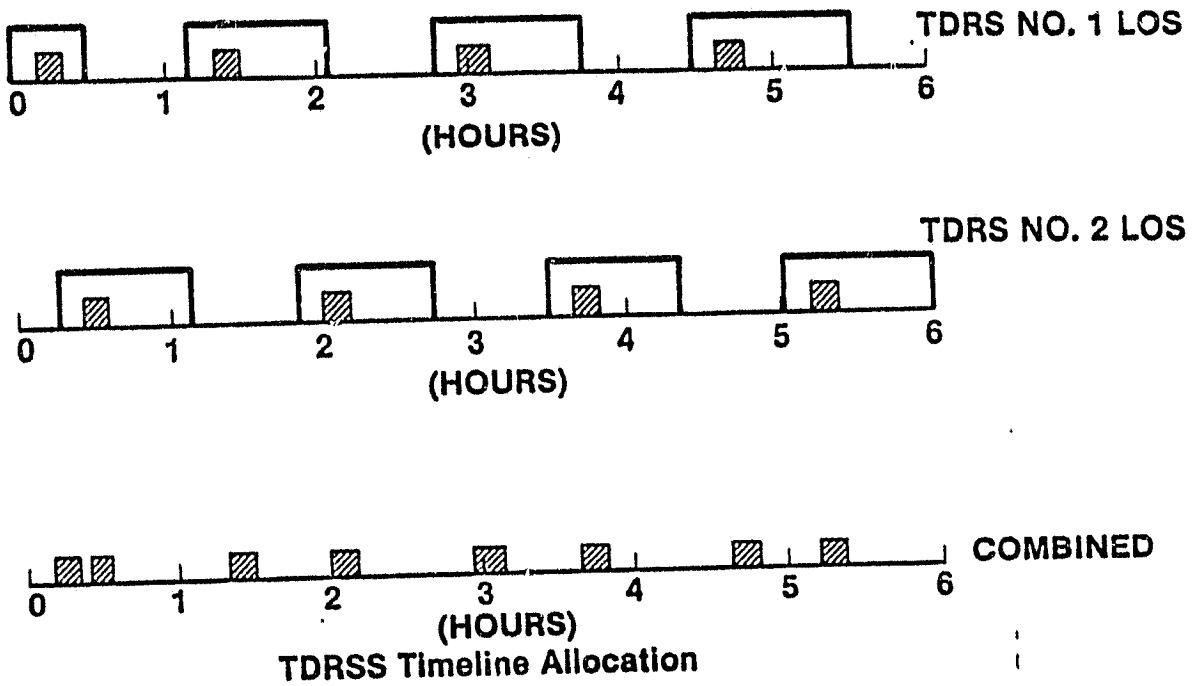


Figure 3-5. A8-TDRSS Scheduling Simulation

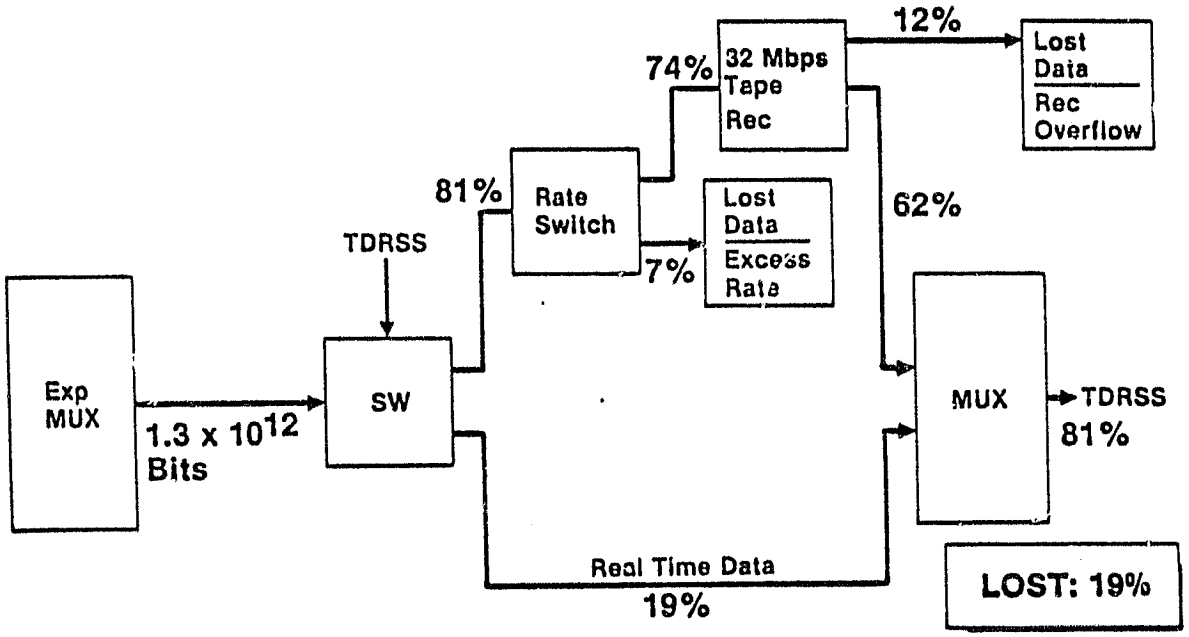


Figure 3-6. A8 Simulation (10 Min/Orbit TDRSS Time)

record rate (32 Mbps in this case). If the data stream rate exceeds the recorder rate, the data represented by the excess rate is considered to be lost; the data at 32 Mbps or less is routed to the tape recorder function.

The data quantity going to the tape recorder is monitored by the simulator program. If the data quantity exceeds the recorder capacity, that excess data is considered lost. When TDRSS schedule blocks occur, the tape recorder is dumped to the output MUX simultaneously with real-time data at the maximum recorder output rate and the data quantity currently stored on tape is reduced accordingly.

As shown in Figure 3-6, 19% of the A8 payload group data in a simulated 24-hour mission was transmitted in real-time. Seven percent of the data was lost because it was acquired when TDRSS was not scheduled and at a rate in excess of the 32 Mbps storage capability. Another 12% of the data was lost because the tape recorder capacity was not sufficient. Sixty-two percent of the data was stored and dumped by the on-board tape recorder. Figure 3-7 summarizes the SASP data system performance with the A8 payload group.

	Peak Rate	Mean Rate	Quantity
Data Acquired	93.5 Mbps	15.6 Mbps	1.3×10^{12} Bits
Transmitted Real Time	22 Mbps	13.3 Mbps	2.5×10^{11} Bits
Recorded/Dumped	32 Mbps		8×10^{11} Bits

Data Lost

- **Recorder Capacity Exceeded** — 1.6×10^{11} Bits
- **Recorder Input Rate Exceeded** — 9×10^{10} Bits

Figure 3-7. A8 Data System Performance

A review of the nature of the lost data indicated that it almost totally consisted of SOT payload data. SOT has a primary objective; the collection of data during solar flares. The SOT data output was modeled at 50 Kbps continuous output, a 5 Mbps output for 15 minutes before and 15 minutes after a solar flare, and a 50 Mbps output for 15 minutes during the flare event (see Figure 3-8). The simulation was set up to generate simulated solar flares at random times at an average rate of three every 24 hours. During the A8 simulation, three simulated flares occurred, none of which coincided with a TDRSS schedule block. Since the on-board storage system was not sized to handle this data, the data was lost.

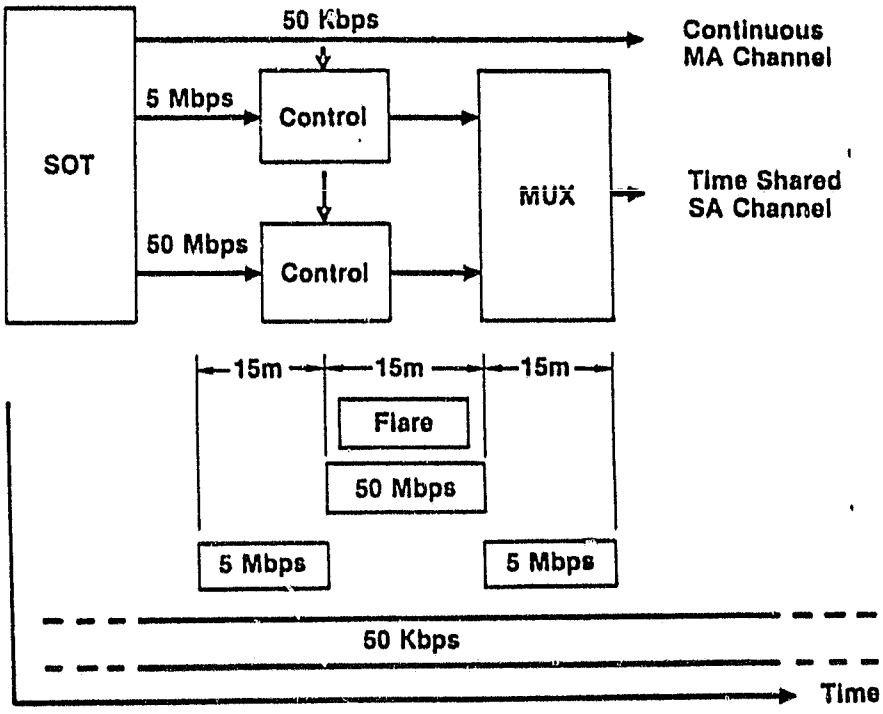


Figure 3-8. SOT Solar Flare Data Handling

Figure 3-9 summarizes the assessed data system performance for the A8 payload. The peak data rates were well within the SASP data and communication capabilities and are also well under the TDRSS KSA channel capacity. Data loss for the A8 payload group could be eliminated by either (1) TDRSS scheduling that assures TDRSS availability during peak data acquisition periods, or (2) providing a modest improvement in on-board storage rate and capacity.

- **Peak Real-Time Data Rates Are Within SASP Data System Capability**
- **Data Loss Can Be Eliminated By**
  - **Improved Scheduling of TDRSS Access, Or**
  - **Modest Improvement in Recorder Capability**
- **Solar Flare Data Requires Special Consideration**
  - **Real Time Monitoring and Fast Response TDRSS Scheduling, Or**
  - **Onboard Data Evaluation and Capture**

Figure 3-9. A8 Assessment

The A8 simulation emphasized the need for an on-board capability to capture random event driven data. In the SOT case, one operational concept is that the 50 Kbps continuous data is monitored at the control center. When this data indicates that a solar flare is imminent, the on-board system is commanded to begin acquiring data at the 5 Mbps rate, then the 50 Mbps rate. However, the TDRSS concept and predicted loading make it extremely unlikely that a command channel can be dedicated to a particular spacecraft and make it difficult to reschedule a command channel on short notice to respond to random events.

An on-board system concept might include a "continuous-loop" recorder that always contains the sensor output data for the last X minutes. An on-board processor would evaluate the data and would cause the recorder to "freeze" the data for the appropriate time period when an interesting event is detected. This stored data would then be dumped at the next scheduled TDRSS access time.

In summary, the A8 analysis showed that the SASP data system, configured with currently available technology, is capable of capturing the combined data output of the A8 payload group with a reasonable amount of TDRSS time. Event-driven high rate data requires special consideration in the on-board data system design.

B. F5 Payload Group

The F5 payload group was selected to represent a data-stressing payload group for a second-order SASP in the late 1980s time period. F5, like A8, was defined early in the SASP Payload Accommodations Study. As shown in Figure 3-10, F5 was a payload group candidate for an applications platform to be launched in 1989 into a 90°, 705 km orbit. The payloads in the group include RO-1, Soil Moisture Radiometer-Phase Array (SMR-PA), Laser Fluorescence Spectrometer (LFS), Multi-Spectral Mid-IR Imager (MMIRI), Upper Atmospheric Research Satellite (UARS), and Ocean Synthetic Aperture Radar (OSAR). RO-1 is, like RO-2 in the A8 payload group, a pallet of resource observation instruments suggested by the SASP Payload Accommodations Study. RO-1 includes a Thematic Mapper from Landsat, a Stereoscopic Imaging System, a Multispectral Resource Sampler, and a Fraunhofer Line Discriminator. Each of the instruments on the RO-1 pallet was considered to be a separate payload with its own data output channel.

- **Second Order Platform**
- **98°, 705 km Orbit**
- **1989 Flight**
- **Applications Platform**
- **Payload Group Includes**
  - **RO-1**
  - **SMR-PA**
  - **LFS**
  - **MMIRI**
  - **UARS**
  - **OSAR**

Figure 3-10. F5 Configuration

The F5 analysis approach, summarized in Figure 3-11, was similar to that previously described for A8. However, for F5 additional simulation runs were made with variations in key input parameters to allow some assessment of the effectiveness of competing approaches to achieving effective data capture. The simulation parameters that were varied are summarized in Figure 3-12.

- **Establish Experiment Data Rates**
- **Establish Experiment Data Timeline Constraints**
- **Assign Experiment Outputs to MUX Channels**
- **Establish Simulation Ground Rules**
- **Run/Evaluate Simulation**
- **Define Trade Parameters**
- **Run Trade Study Cases**
- **Evaluate Results**

Figure 3-11. F5 Analysis Approach

- **Record/Dump Rate**
- **TDRSS Availability (Dump Time)**
- **Onboard Processing/Data Compression**
- **Dedicated Communication/Data Processing Capabilities**

Figure 3-12. F5 Simulation Trade Studies

F5 payload data timeline constraints and operating rules were established and are shown in Figure 2-4. The payload data outputs were assigned to the SASP high rate multiplexer input as shown in Figures 3-13 and 3-14. Figure 3-13 also shows the peak data rate produced by each payload. The processor (PROC) block was added to represent the data rate increase that may result due to source packetization of the data. It was assumed that the rate increase would be approximately 10%.

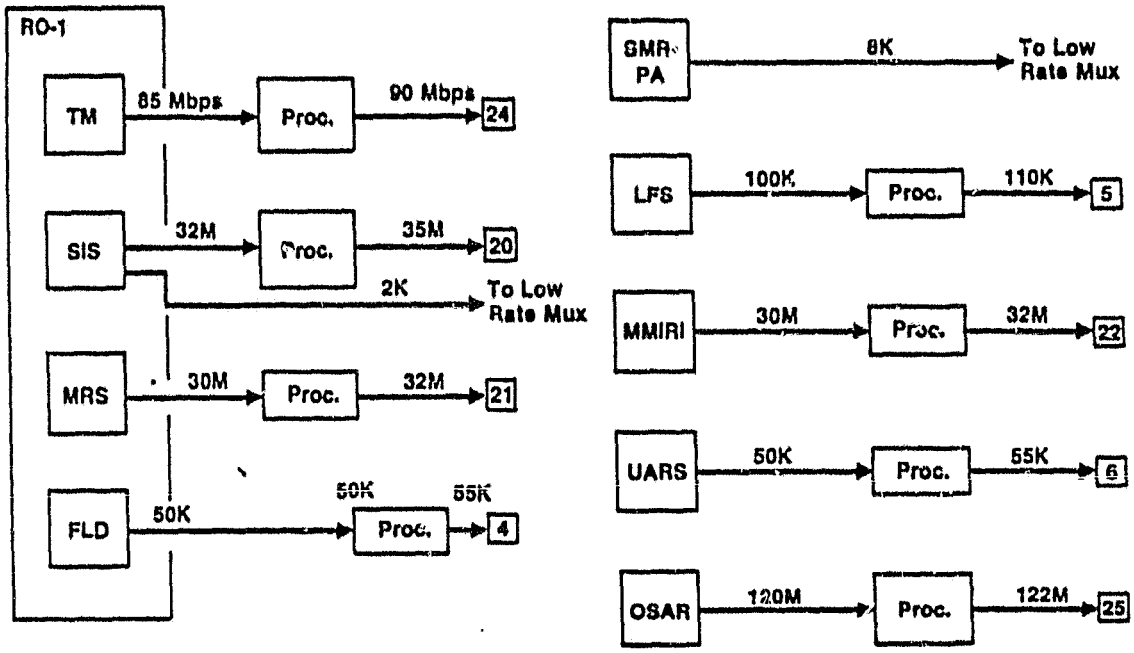


Figure 3-13. F5 Configuration Maximum Data Rates

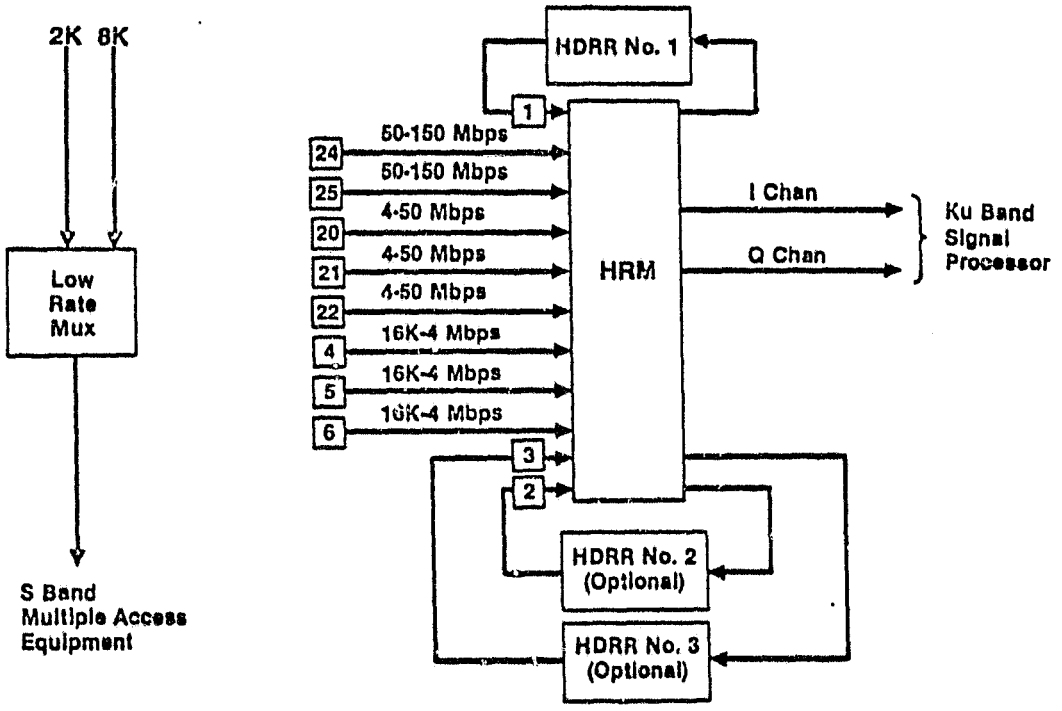


Figure 3-14. MUX Configuration for F5 Payload Group

Figure 3-15 defines the parameters used in each of five simulations for the F5 payload group. The on-board storage record and dump rate and storage capacity and the TDRSS timeline availability were varied as shown. In configuration C, the OSAR payload was deleted on the basis that such an applications-oriented, high data rate, high data quantity payload may be more effective with its own dedicated data and communications system, thereby bypassing and off-loading the SASP data/communications system and the TDRSS. Configuration D simulated the effect of reducing the OSAR and Thematic Mapper peak rates by a factor of 4 by the use of on-board data compression/ reduction techniques.

Config-uration	Record/ Dump Rate	Record Capacity	Data Compression	TDRSS Available	P/L Configuration
Baseline	32 Mbps	3.8×10^{10}	—	20 Min	Full F5
A	64 Mbps	3.8×10^{10}	—	10 Min	Full F5
B	100 Mbps	3.8×10^{10}	—	7 Min	Full F5
C	100 Mbps	3×10^{11}	—	15 Min	Delete OSAR
D	100 Mbps	3×10^{11}	Reduce Pk Rates TM = 22.5×10^{6} OSAR = 30.5×10^{6}	15 Min	Full F5

Figure 3-15. F5 Trade Studies

Figures 3-16 through 3-20 show the results of the F5 simulations in a format similar to that used in the A8 description. The first three simulations, where various combinations of recorder capability and TDRSS timeline were assumed, resulted in large amounts of data being lost - up to 78% in the worst case. This happens because the amount of data being produced by the combined F5 payloads (approximately 109 Mbps average or nearly 10^{13} bits in 24 hours) is so great that it cannot be captured with reasonable on-board storage capabilities and TDRSS timelines. The C and D configuration, Figures 3-18 and 3-20, show that when the OSAR payload is off-loaded or when the OSAR and TM rates are reduced by a factor of 4, the data can be captured, although a 100 Mbps recorder was required as well as two 15 minute TDRSS dumps per orbit.

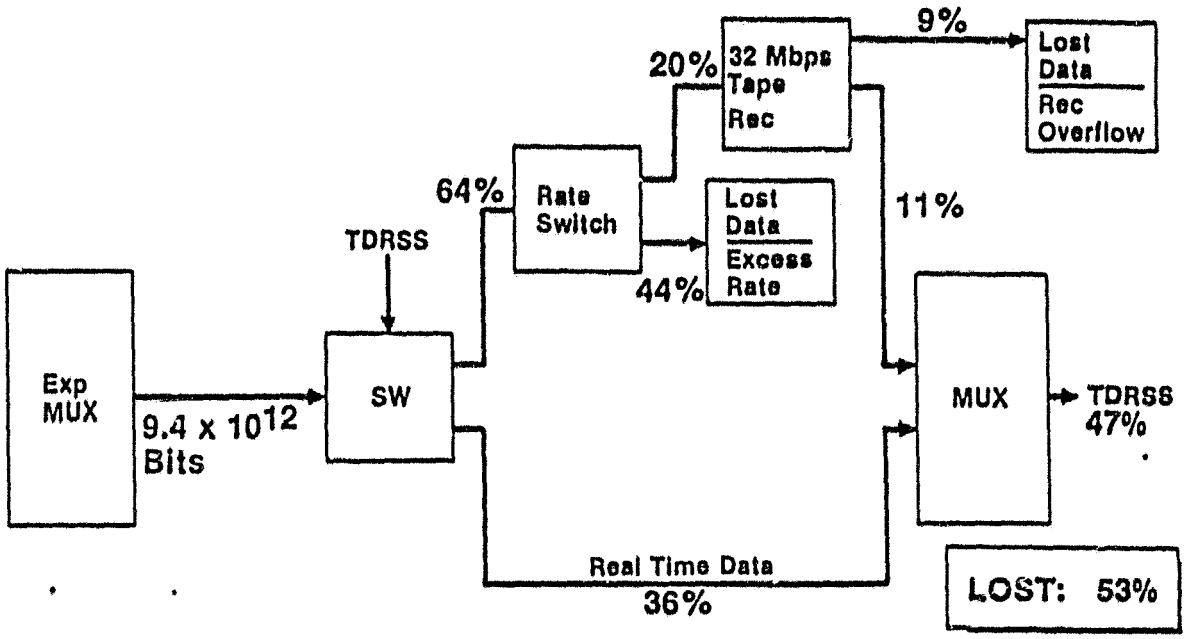


Figure 3-16. F5 Baseline (20 Min TDRSS Time)

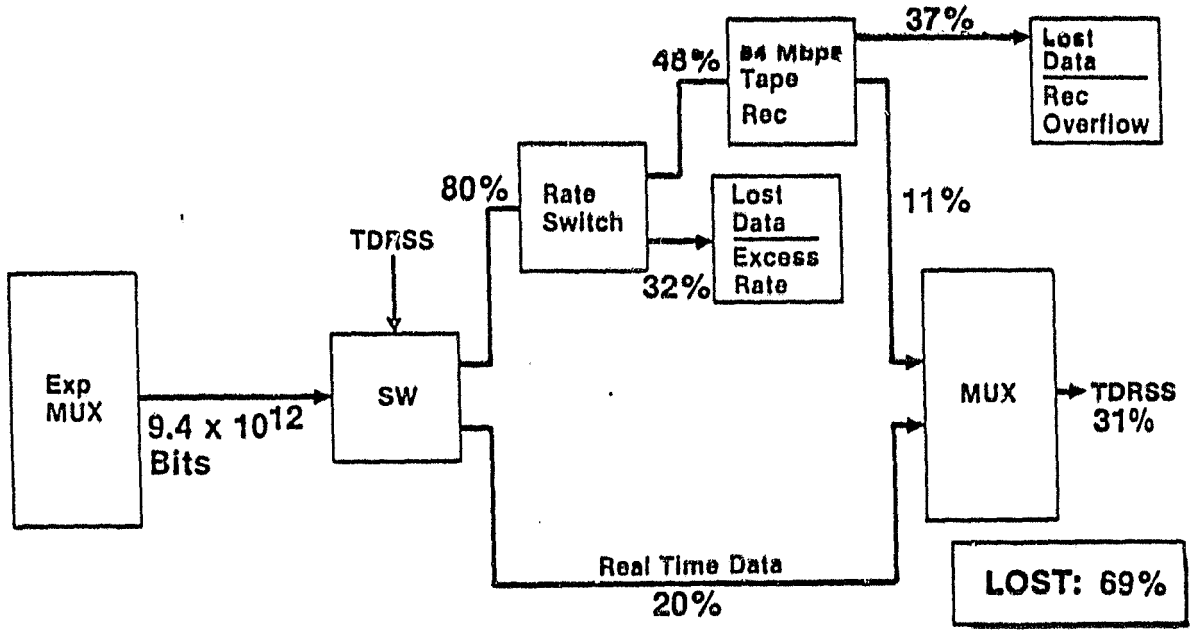


Figure 3-17. F5 - A (10 Min TDRSS Time)

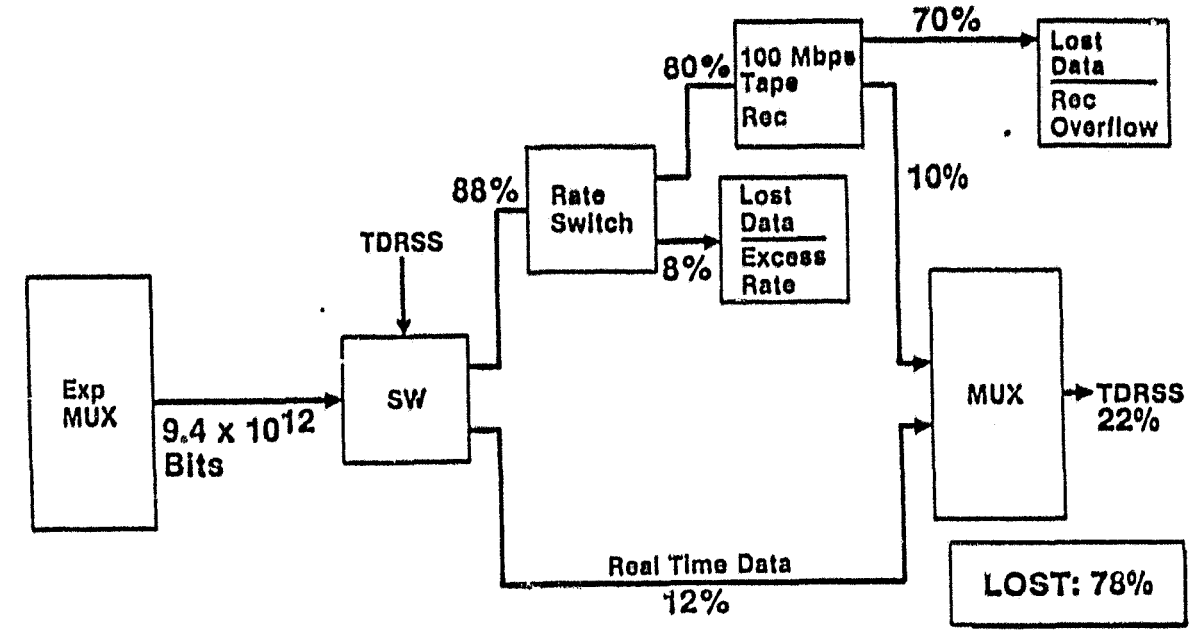


Figure 3-18. F5 - B (7 Min TDRSS Time)

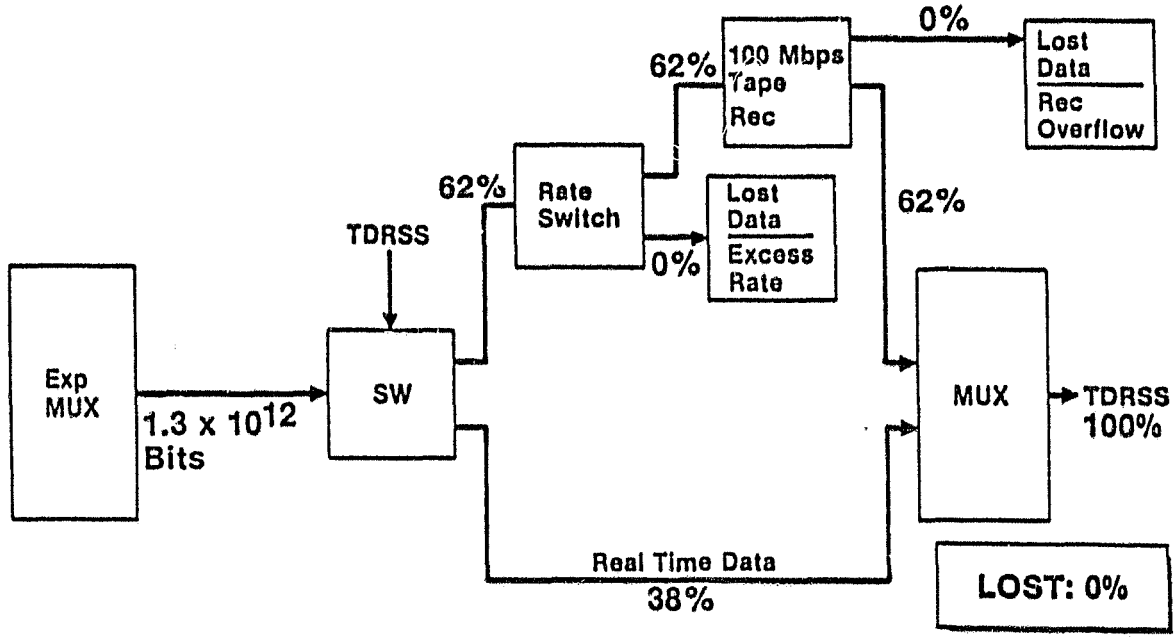


Figure 3-19. F5 - C (15 Min TDRSS Time) (No OSAR Payload)

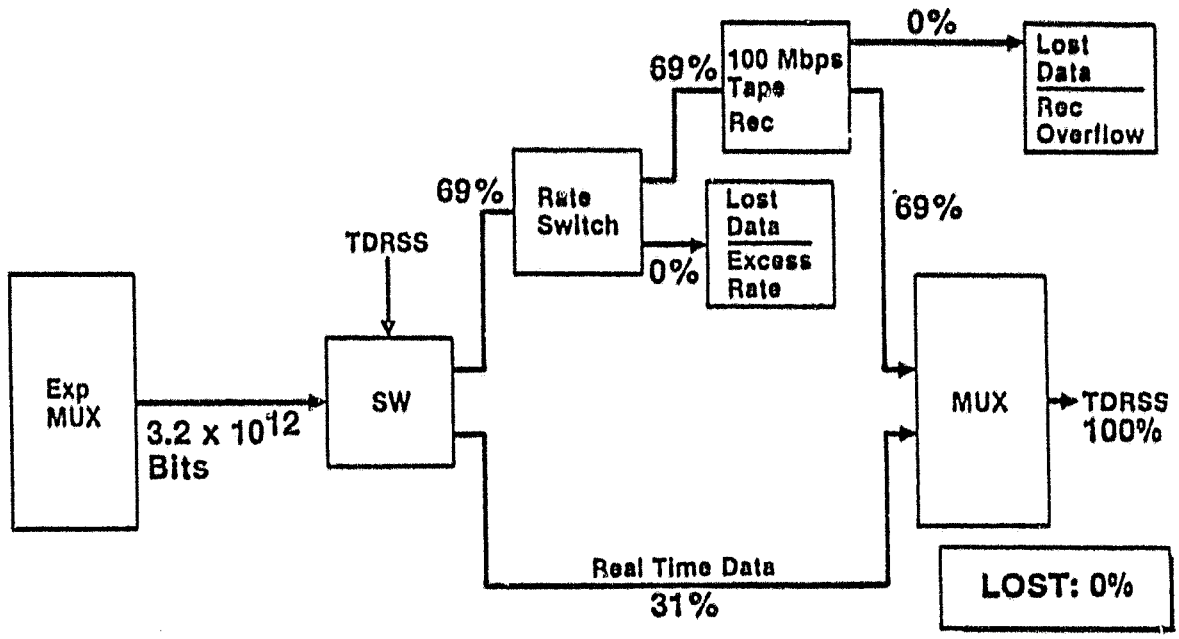


Figure 3-20. F5 - D (15 Min TDRSS Time)
(Use Data Compression for OSAR and TM)

Figure 3-21 summarizes the statistics for the five (5) F5 simulations. Figure 3-22 shows the key conclusions from the F5 analysis. As in the A8 case, peak data rates are within the SASP data system and the TDRSS capability. The total data quantity produced by F5 however, proved to be stressing to the data system. Because of the total expected to be placed on the TDRSS resource, it will be necessary for users to minimize their requirements for TDRSS time. This will require on-board data storage that can be dumped to TDRSS in a short time period, i.e., at a high data rate. For payloads like the OSAR and the Thematic Mapper in the F5 group, on-board data processing and reduction/compression techniques will be needed to prevent the large amounts of data from swamping the SASP data system, the TDRSS, and the ground data networks.

The F5 analysis results were extended to show how the data loss from an F5 payload group would vary as key parameters are changed. Figure 3-23 shows the data loss variation for F5, with a 64 Mbps on-board recorder, as the TDRSS timeline allocation per orbit is changed. This curve indicates that reasonable TDRSS timeline allocations will not allow a large percentage of

the data to be captured, given a 64 Mbps on-board recorder. Figure 3-24 shows the F5 data loss as a function of recorder read/write rate for an assumed 20 minutes per orbit of TDRSS timeline. This curve again shows the difficulty in trying to capture the F5 payload data with state-of-the-art spacecraft recorders and a less than full-time TDRSS channel.

Figure 3-25 shows the data loss for F5 as a function of reduction in the total data quantity (by on-board data reduction/compression) for a 64 Mbps recorder and 15 minutes of TDRSS timeline per orbit. This chart and the two previous ones reinforce the conclusion that on-board data processing is necessary to avoid significant data loss for payload groups like F5.

	Total Data Acquired (24 Hr)	% Transmitted In Real Time	% Recorded And Dumped	% Data Lost
Baseline F5	9.4×10^{12} Bits	36%	11%	53%
A	9.4×10^{12} Bits	20%	11%	69%
B	9.4×10^{12} Bits	12%	10%	78%
C	1.3×10^{12} Bits	38%	62%	0%
D	3.2×10^{12} Bits	31%	69%	0%

Figure 3-21. F5 Simulation Results

- F5 Peak Rates Are Within SASP Data System Capability For Real-Time Transmission
- F5 Data Quantity Stresses Data Subsystem
- Data Storage Capability Is A Critical Issue
- TDRSS Timeline Allocation Will Be A Critical Mission Operations Factor
- On-Board Data Processing/Reduction Techniques Are Necessary to Make High Data Rate Payloads Feasible

Figure 3-22. F5 Assessment

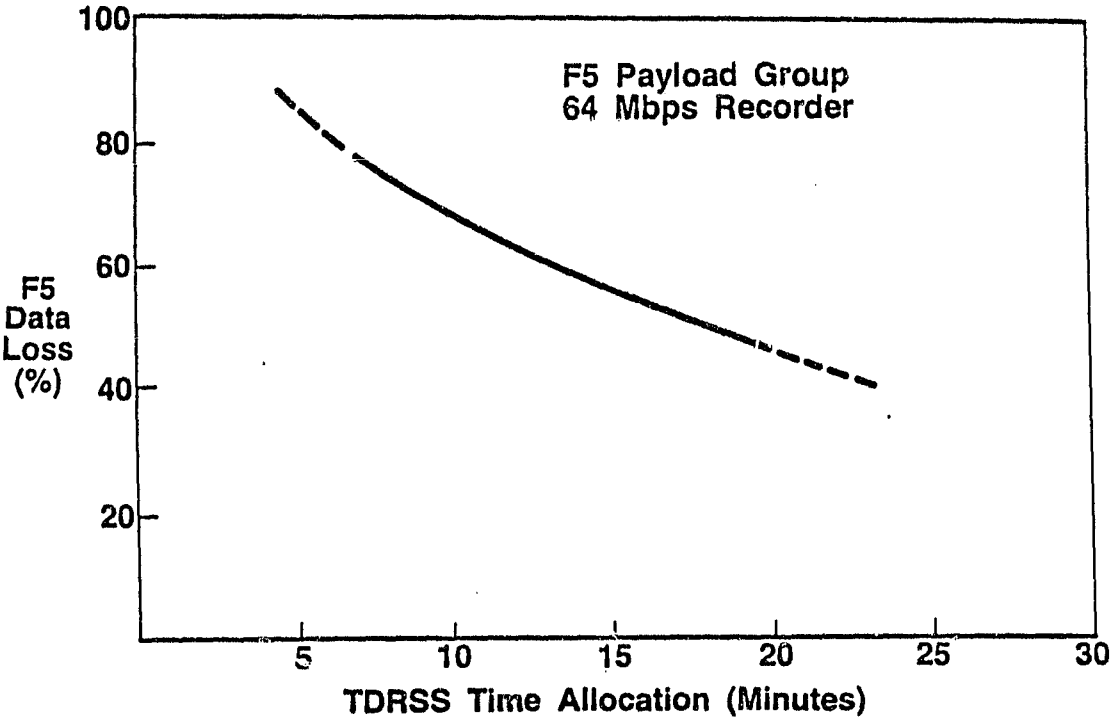


Figure 3-23. F5 Data Loss Versus TDRSS Time Allocation

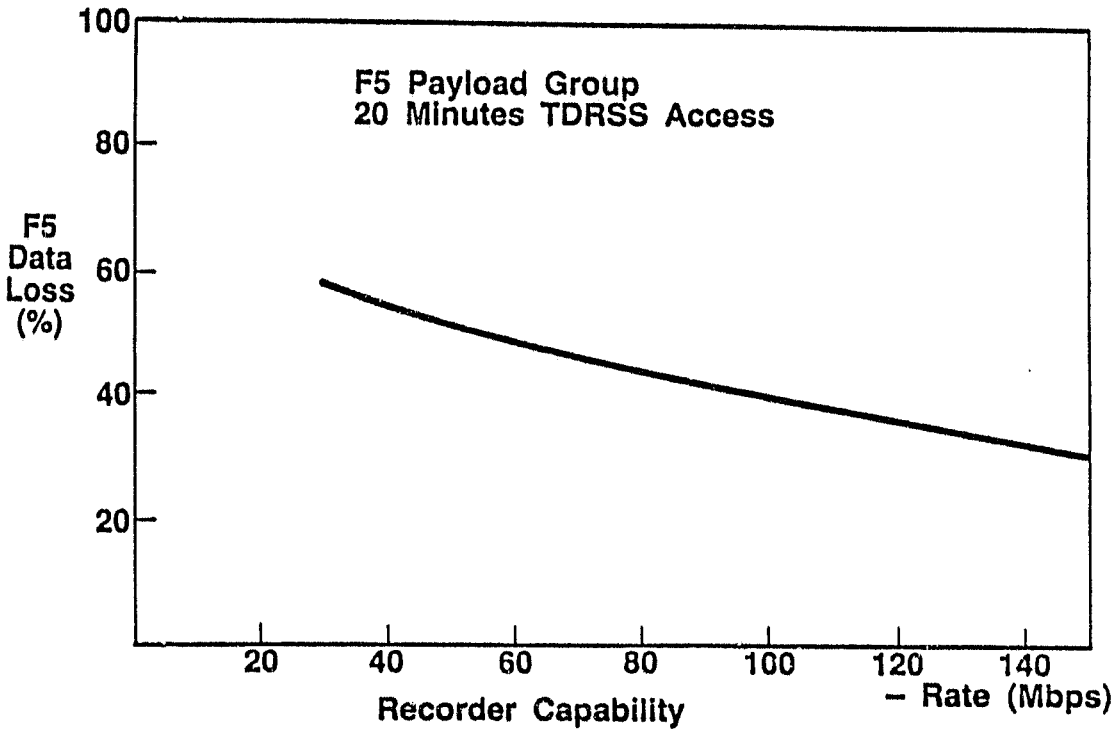


Figure 3-24. F5 Data Loss Versus Data Storage Capability

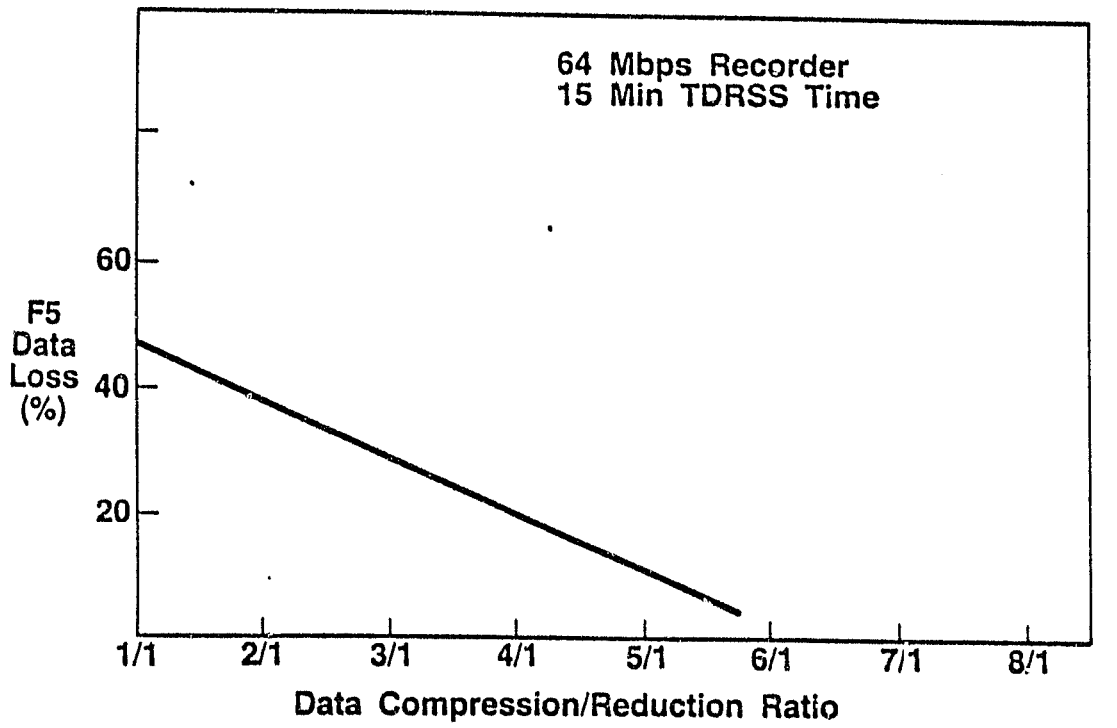


Figure 3-25. F5 Data Loss Versus Data Compression/Reduction Ratio

Section 4
TECHNOLOGY SURVEY

INTRODUCTION

During the DSDS runs done by both MSFC and us, certain data system components onboard the SASP were identified as areas that would potentially require capability improvements through technology growth in the 80s. Those technology areas identified were Onboard Data Storage, Multiplexers and Onboard Processors. To assess the technology in these areas and try to project the growth through the 80s we performed the following:

1. Early in the study we initiated a literature search through our library which gained us access not only to all MDC component library but also NASA and DoD documents. Our search identified over 2000 documents of which all or parts of over 300 were reviewed in support of our projections.

2. Another source of technology data that was utilized is Technical Conferences. Members of the study team attended applicable sessions at five conferences (International Telemetry Conference, WESCON, Space Systems & Technology in the 80s, International Instrumentation Symposium, and Space Shuttle/Spacelab Optical Experiments Conference). Over 70 sessions were attended which were relevant to the SASP technology issues.

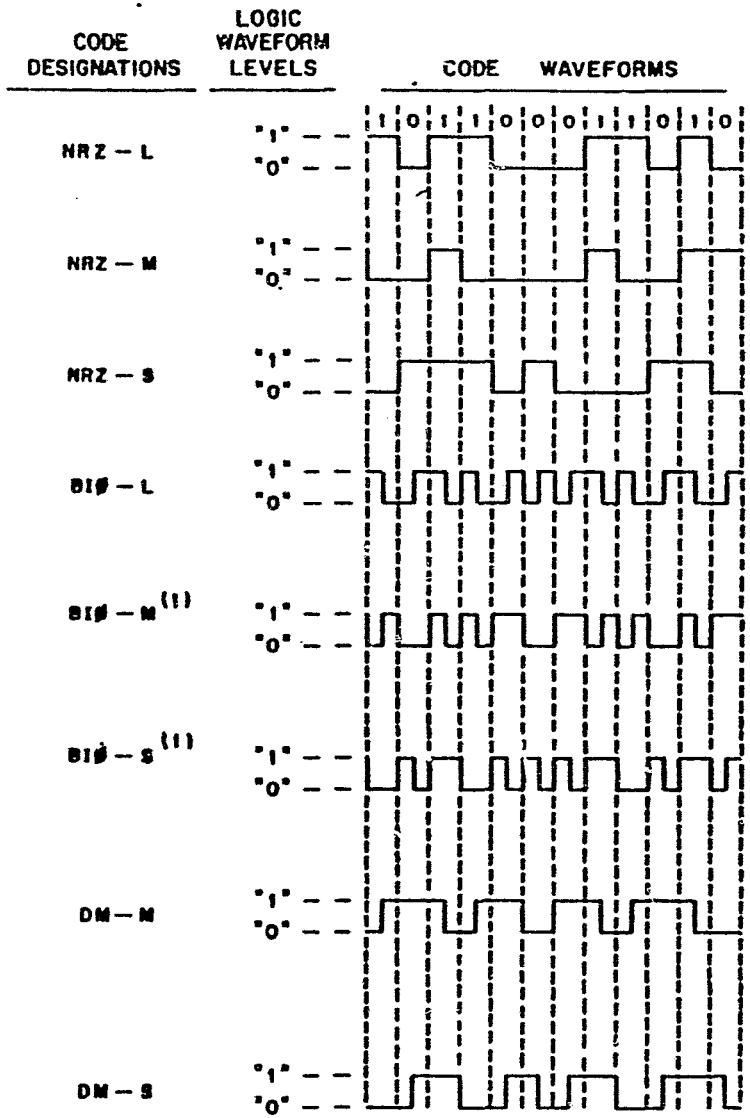
3. Personal and telephone interviews were conducted with technical experts in the subject fields to gather the most current and capable projections of the applicable technology in the 80s. Over 200 people were contacted who contributed significantly to the results of our projections; these were made up of people in NASA, Dod, industry, and academic.

4. Finally, the results of our technology survey and projections were reviewed by a group of senior technical specialists at MDAC-HB and reviewed at MSFC, NASA Headquarters, and GSFC.

A. On-Board Storage

1. Tape Recorders - The most prominent means of storing data on board spacecraft presently is magnetic tape via analog recording techniques. Currently the state-of-the-art is the Spacelab recorder (Odetics) with a maximum recorder rate of 32 Mbps with a total storage capacity of 3.8×10^{10} bits. Other examples of existing spacecraft recorders are the two NASA standards - RCA's 4.5×10^{8}, and Odetics 4×10^{9}. All these recorders are longitudinal devices utilizing conservative bit packing densities. Currently, in ground based longitudinal recorders, several advancements are currently employed to increase record rates and storage capacity. The first of these is new coding techniques[2,3,4,5] to increase bit packing density; examples of these are the Miller Codes (Delayed Modulation), Enhanced NRZ, Randomized NRZ, and Modifications of the Reed Solomon Code (Figure 4-1). Through the additions of encoding and decoding electronics to accommodate these codes bit packing densities are in the order of 33,000 bits/inch/track with a bit error rate of $\leq 1 \times 10^{-7}$. Another technique has been to increase the number of head tracks per inch and increasing the width of the magnetic tape to 2 inches. Examples of these are the Bell and Howell System 600 which utilizes 84 tracks (2" tape) and enhanced NRZ encoded/decoding via serial to parallel conversion to record at rates up to 600 Mbps. Another example is the RCA High Density Multi-Track (HDMR) which utilizes 160 tracks (2" tape) to record up to 240 Mbps. Other companies involved in similar ground applications (longitudinal) are Sangamo, Honeywell, Ampex, and EMI.

The other approach in magnetic recording techniques being advanced for ground applications is the Helical Scan Rotary tape machines. The most interesting recorder surveyed was the Ampex Super High Bit Rate Recorder.[6,7] Utilizing two sets of 27 track heads (2" tape) with bit packing densities of 10 Kb/inch offers recording rates of up to 1000 Mbps with a total storage capacity of 1.3×10^{12} bits (Figures 4-2, 4-3). Presently a lab model is operating at 750 Mbps.



CODE DEFINITIONS

NON-RETURN-TO-ZERO-LEVEL

"One" is represented by one level.
"Zero" is represented by the other level.

NON-RETURN-TO-ZERO-MARK

"One" is represented by a change in level.
"Zero" is represented by no change in level.

NON-RETURN-TO-ZERO-SPACE

"One" is represented by no change in level.
"Zero" is represented by a change in level.

BI-PHASE LEVEL (SPLIT PHASE)

Level change occurs at center of every bit period.
"One" is represented by a "one" level with the transition to the "zero" level.
"Zero" is represented by a "zero" level with the transition to the "one" level.

BI-PHASE-MARK

Level change occurs at the beginning of every bit period.
"One" is represented by a midbit level change.
"Zero" is represented by no midbit level change.

BI-PHASE-SPACE

Level change occurs at the beginning of every bit period.
"One" is represented by no midbit level change.
"Zero" is represented by a midbit level change.

DELAY MODULATION-MARK (MILLER CODE)

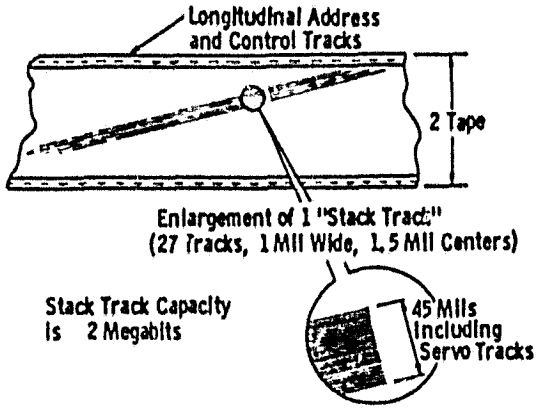
"One" is represented by a level change midbit time.
"Zero" followed by a "zero" is represented by a level change at the end of the first "Zero" bit. No level change occurs when a "zero" is preceded by a "one".

DELAY MODULATION-SPACE (MILLER CODE)

"Zero" is represented by a level change at midbit time.
"One" followed by a "one" is represented by a transition at the end of the first "one" bit. No level change occurs when a "one" is preceded by a "zero".

(1) These definitions for BIØ-M and BIØ-S represent the accepted standard as previously defined in RCC documents 106-66 and 106-73 (Revised NOV 1975). These codes were erroneously defined in RCC documents 106-69, 106-71 and 106-73.

Figure 4-1. PCM Code Definition



A) Tape Format

(5 MB/SQ/IN. USER PACKING DENSITY)				
Bit Rate MB/s	Record Time Min	Tape Length Feet	Reel Dia Inches	Total Storage Bits
1000	21.6	10800	15	1.30×10^{12}
750	28.8	10800	15	1.30×10^{12}
600	36.0	10800	15	1.30×10^{12}
300	72.0	10800	15	1.30×10^{12}
200	108.0	10800	15	1.30×10^{12}
100	216.0	10800	15	1.30×10^{12}
20	1080.0	10800	15	1.30×10^{12}

B) Storage Capacity

Figure 4-2. SHBR Tape Utilization

Technical Details

- Helical Scan Rotary Tape Transport
  - 180° Helical Wrap With 5" Dia Scanner
  - Uses 2" Tape With Present Oxide Characteristics
  - 2 Sets of 27 Track Heads, Each Writing Up to 30 MB/Sec. At 10 KB/In. Packing Density per Track
  - Heads With 1 Mil Tracks on 1.5 Mil Centers
  - 15 Microinch Air Separation Between Tape and Head
  - Continuous Automatic Scan Tracking (AST)*
- Record/Reproduce Electronics
  - Fully Digital Design
  - Speed Changing Via Digital Buffer, Giving Continuously Variable Input/Output Speeds
  - Fixed Equalization as In Today's Computer Disc Recorders
  - "Instantaneous" Start/Stop Capability

*Trademark - Ampex Corporation

Figure 4-3. The Ampex SHBR High Technology Digital Tape Recorder/Reproducer

For space applications several developments were surveyed. RCA is pursuing the application of increased head track densities and the use of high density codes for longitudinal recorders to address the need for higher recording rates and increased storage. Odetics is under contract to modify the Spacelab recorder via the addition of modified Reed Solomon encoding/decoding electronics to increase that machine to 50 Mbps with a total storage of $7.5 \times 10^{10.8}$. The most promising work going on is the teaming of Ampex and Odetics in which Odetics would adapt for space applications the Ampex super high bit rate technology. Over and above the technology growth for increased recording rates and storage is the work that has been done on increasing the reliability of the spaceborne recorder. Much work has been done on the mechanical design and the head tape interface to solve the well known reliability problems of yesterday.

Tape recorder projected growth through 1990 is shown in Figure 4-4. Taking advantage of new high density coding techniques and new head technology (both rotary and longitudinal) indicates that the tape recorder technology could supply a reliable recorder with record rates approaching 1 Gbps and total storage capacity in the order of 10^{12}. Figure 4-5 shows hardware examples that use some of the candidate technology that is applicable to this projected growth.

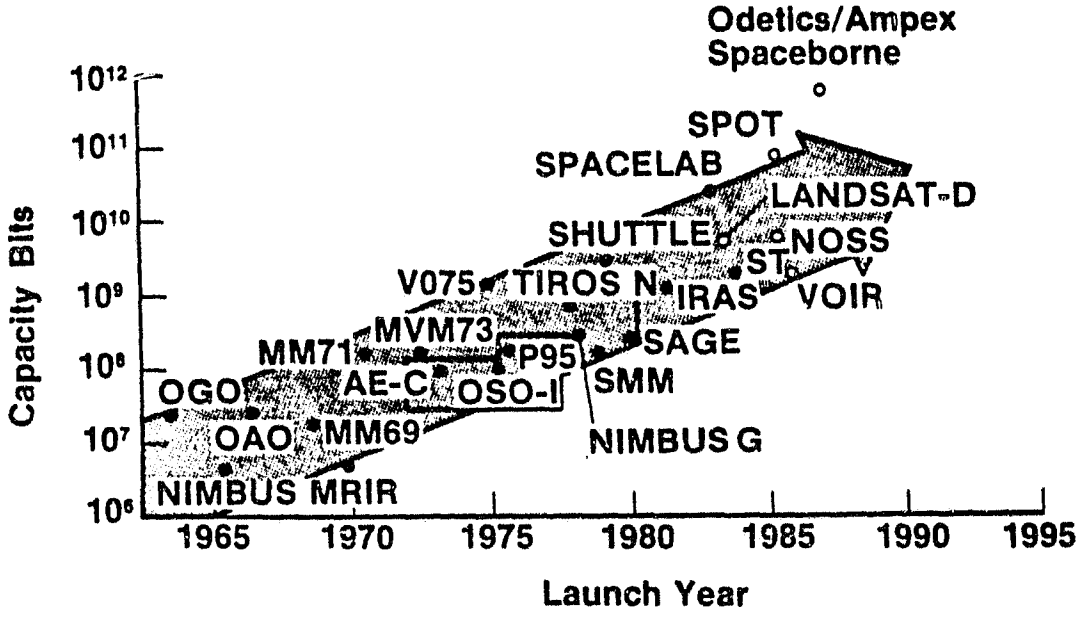
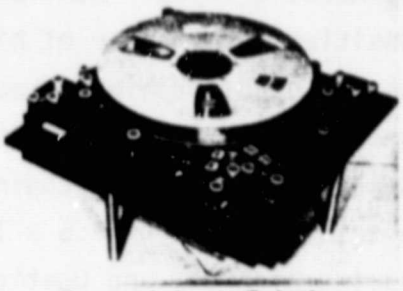
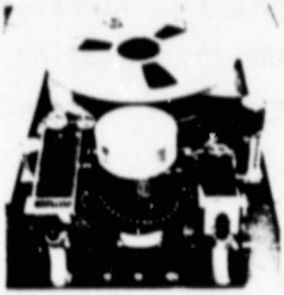


Figure 4-4. Tape Recorder Growth

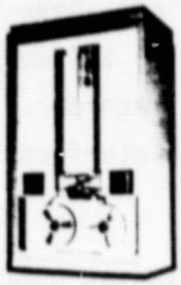


Spacelab – Odetics
32 MBPS

HDMR-Head – RCA
240 MBPS – 160 Tracks



NSS-100 – Ampex
1 GBPS



System 600 –B&H
600 MBPS

Figure 4-5. Tape Recorders

2. Bubble Memory - An alternate to analog magnetic tape for data storage is the magnetic bubble. The solid state recorder utilizing bubble memories has evolved as the prime candidate for replacing magnetic tape recorders in spacecraft. Utilizing digital techniques logic states are determined by the presence or absence of a magnetic domain. A logic "1" is indicated by the presence of a bubble, a "0" by its absence. Acting like a shift register bubbles are moved around in major and minor loops. Access to a set of data is achieved by loading the major loop with bubbles on the appropriate minor loop and then shifting them past a magneto resistive sensing device.

At first, bubbles were large in size; however, with knowledge gained from other technologies, smaller substrate features were readily attained and the size of bubbles easily shrank. A new planar processing technique used by Texas Instruments now foresees 1 μm bubble diameters giving 6 Mbits/cm^2. 1.8 μm bubbles are now commercially available. One hundred Mbit bubble chips are expected by the mid 1980s if progress continues as expected and chips of 256 Mbits are believed to be possible in the far term. Contiguous disk (CD) technology may be a major factor in this size reduction. With CDs the gap is

eliminated; therefore, bubble size is not bounded by gap size. Two additional advantages of the contiguous disks over other techniques are that drive power requirements do not go up with decreasing bubble diameters and the photolithography process can be less exacting in tolerance. Wall encoded bubbles also will play a large part in the battle for small sizes. Here, ones and zeros are made distinguishable by dissimilarities in the structures of the bubble domain wall. Bubbles will be able to be packed closer together without the problem of bubble repulsion.

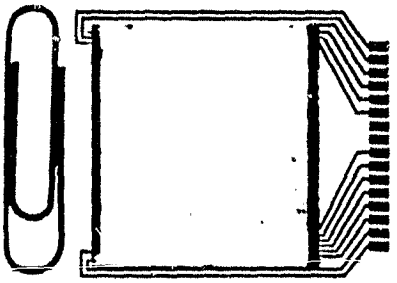
Speed and access times will continue to increase; at first one large major loop was implemented to circulate bubbles on the chip. A new architectural format of major loop/minor loop allows for greater access to a specific data block. Typical speeds now are 750 Kbits/sec. with 3ms access times. A frequency of 100 KHz is used. Current sheet devices look promising for future development. For these the drive coils are replaced by layers of current carrying materials. These will make speeds of 1 to 20 MHz possible.

Applications of bubble memories as tape recorder replacements for Space Applications have been proposed for sometime. The primary emphasis has been on achieving the increased reliability inherent with a solid state device. Both the USAF and NASA have done development work in this regard. The Air Force has done development work (Air Force Avionics Lab, Wright-Patterson AFB) with Texas Instruments to develop a brassboard system using present technology to demonstrate bubble memory system concepts. Based on 5μm bubbles with a 128K bit major minor devise a 16 Mb unit with data rates up to 2 MHz will be fabricated. Estimated weight and volume are 56 pounds and 1555 in^3. The USAF also contracted with Rockwell International to perform a conceptual design for a 10^{12} bit bubble memory system with data rates up to 50 MHz (USAF Contract F33615-76-C-1198).[9] The basic storage element contains 10^8 bits in a 5cm x 5cm area. The elements were then organized into a hybrid-decoder form with the data being organized in 10^7 bit blocks accessed through retarding type decoder networks; operating frequency was 780 KHz. The system goal of 50 MHz was achieved by multiplexing 64 channels in parallel.

The NASA effort managed by Langley Research Center has been supported by Rockwell International.[10,11] They have designed, fabricated, and tested a partially populated 10^8 bit prototype spacecraft recorder. Based on a 4μm

bubble technology and a 100K bit serial memory element it is capable of multiple configurations and data rates up to 1.2 Mbps. NASA recently has been considering development of a flight-qualified version based on the experience gained from the 10^8 prototype. Shown in Figure 4-6 are the specifications for the RI 10^8 and 10^{12} Solid State Data Recorders including a picture of the prototype 10^8 delivered to NASA/Langley. Also shown is a photograph of the Bell Laboratories experimental 11.5 Mbps bubble on a 1.3 in^2 chip. Based on contiguous disk technology their drive power does not increase with decreasing bubble size.

Langley/RI 10^8 Bit Recorder



Bell Labs – 11.5 Mb/Chip

10^8 Bit RCD Specs

SSDR Characteristics Summary

Storage Capacity	1.04 x 10^8 Bits
Size	760 in^3
Weight	43 Pounds
Configuration	
Serial-Programmable	1, 2, or 4 Channels
Parallel-8 Bit	1 Channel
Max Data Rate	
Each Channel	1.2m Bit/Sec
Total	2.4m Bits/Sec
Power (1 Channel, 10k Bits/Sec)	13.7 Watts
Operating Temperature	-10°C to +60°C
Nonoperating Temperature	
No Loss of Data	-40°C to +85°C
With Loss of Data	-50°C to +125°C
Predicted MTBF	41,000 Hours

10^{12} Bit RCD Specs

Year Operational	1985 (Est)
Volume	3,456 in^3
Weight	120 Lb
Storage Capacity	10^12 Bits
Power (Maximum)	200W
Data Rate (Maximum)	50 MHz

Figure 4-6. Bubble Memory

Magnetic Bubble Solid State Recorder projected growth through 1990 is shown in Figure 4-7. Assuming that the predictions quoted in the references do occur means that these types of mass storage devices will be viable competitors for magnetic recorders in space by 1990.

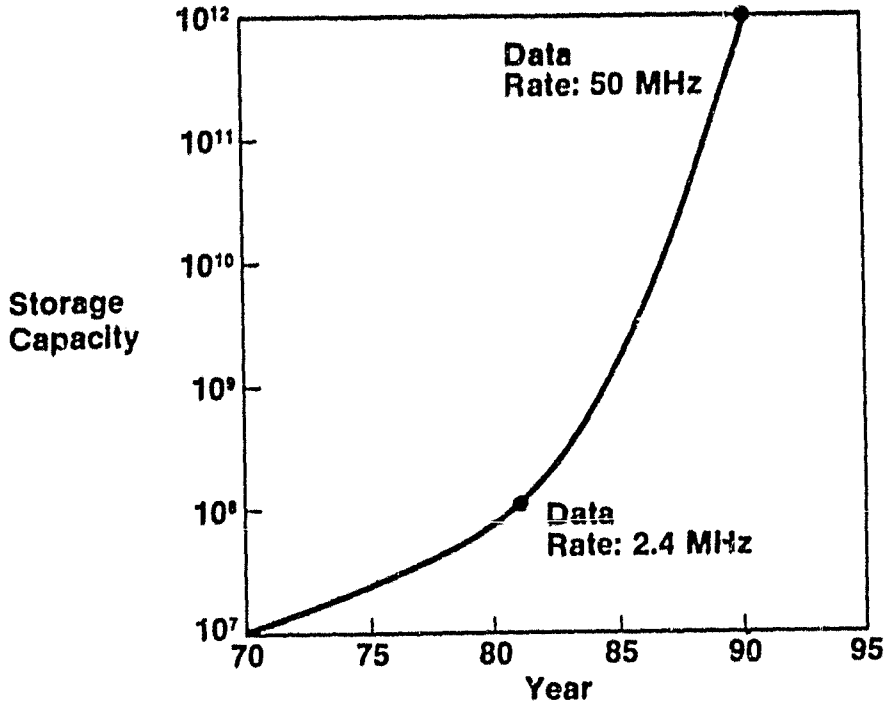


Figure 4-7. Bubble Memory Storage Growth

3. Metal-Nitride-Oxide-Semiconductor (MNOS) Memory - Another alternative to analog magnetic tape for data storage is the MNOS memory devices. The MNOS transistor is unique among solid-state electronic devices in that it permits stored data alterability simultaneously with stored data nonvolatility. It also provides a small-area structure and fabrication compatibility with high density, integrated circuit technologies.

The MNOS transistor is a close relative of the conventional metal-oxide-semiconductor (MOS) transistor in that the usual layer of gate oxide is replaced by a 500 A layer of silicon nitride over a less than 20 A thick layer of silicon dioxide. The application of a moderately-high voltage (approximately 25 volts) to the gate electrode of this transistor causes the thin silicon dioxide layer to become conductive (or to permit charge carriers to tunnel

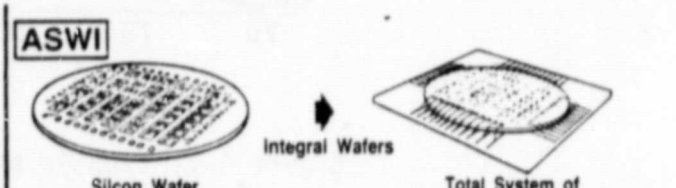
through it). Charge carriers may then pass between the silicon and charge-carrier traps located near the silicon-nitride, silicon-dioxide interface. The presence of trapped charge carriers at this interface modifies the gate voltage which controls passage of charge carriers from source to drain in the conventional operation of the transistor. The MNOS transistor is then said to have an "off" and an "on" states which depend on the concentration and the polarity of the trapped charge carriers.

Westinghouse and McDonnell Douglas Astronautics Co. (MDAC) both have been working for some time to apply the MNOS memory technology to space solid state data recorder applications. The Westinghouse work has centered on using their MNOS Boram Chip shown in Figure 4-8; this is actually a hybrid 1 x 2 inches containing 16 chips. The specification derived by Westinghouse for a Spaceborne 10^8 Bit Recorder is also shown in Figure 4-8 with projected specifications based on various density MNOS chips.[12] MDAC's work has centered around existing work they have been doing utilizing MNOS technology noted with Adaptive Wafer Scale Integration techniques as shown in Figure 4-8.[13,14]

Westinghouse

Characteristics	Design Target	MNOS 32k Bit Chip	MNOS 6 5k Bit Chip	MNOS 131k Bit Chip	MNOS 262k Bit Chip	Units
Bit Capacity	10^8	10^8	10^8	10^8	10^8	Bits
Record Rate	10^5	10^5	10^5	10^5	10^5	Bits Sec
Playback Rate	10^6	10^6	10^6	10^6	10^6	Bits Sec
Power	20	5.4	5.4	5.4	5.4	Watts
Weight	10	19	12	9	7	Pounds
Volume	800	456	290	206	165	Inches^3

10^8 Bit Recorder



- Up to Several Million Circuit Elements
- Reconnectable on a Semiconductor Wafer
- Comapred With 1,024,000 Bit Memories
- Constructed From 16,334 Bit Devices, AWSI
- Saves More Than 2000 Lead Bonds Plus
- 64-Device Hybrid or PC Interconnect Boards

MDAC-HB

Storage Capacity	
System Level	10^9 Bits Usable for Data
Wafer Level	5 MBit Average (4 Inch Wafer)
Reliability	Self-Maintaining With Built-In Spaces
	Block Accessed Serial
	Power Switching
Size	0.6 Cubic Foot
Weight	26 Lbs
Speed	Up to 2.7 Mb Sec
Power	15W Average 25W Peak
Radiation Hardness Option	10^5 to 10^6 Rad (Si) Total Dose

10^9 Bit Recorder

Figure 4-8. MNOS Memory

Adaptive Wafer Scale Integration (AWSI)[15] is a concept which employs electrically alterable, nonvolatile interconnect controller circuits processed into a semiconductor wafer to connect "arrays" of interconnected, operable circuits (also processed into the wafer) to a bus structure deposited on the wafer between the arrays. With this approach, AWSI can have important advantages relative to other high density electronic circuit approaches. Such advantages potentially include: repeated electronic reconfigurability of interconnected circuits, compatibility with a wide variety of semiconductor processes, ability to select for yield, improved reliability, self-healing and fault tolerance, all plus reduction in size, weight, and cost.

Figure 4-9 graphically illustrates the AWSI concept. In AWSI, the die array are all connected via system bus (Figure 4-9). The address of these arrays that pass the probe test are stored in nonvolatile memory. Operable arrays which are initially used in system mechanization are accessible either via indirect addressing or via associative decoder addressing. The remainder of the operable arrays are reserved as spares to be connected into the bus structure as replacements for operating arrays which subsequently may be shown by built-in tests to have become defective. Alternatively, the spares can be later used for system reconfiguration, dependent on application requirements.

With AWSI interconnect:

a. Any array may be connected to, or disconnected from, the structure at any time; connections include both signals and power.

b. Neither nonoperable nor nonoperating arrays draw power.

c. Neither special contact masks, metalization masks nor fusible links are required to connect arrays to bus lines. Conditional interconnect is accomplished electronically instead of via non-alterable mechanical means.

d. Spare operable arrays are stored on the wafer and connected to the bus structure whenever built-in tests reveal that one of the active arrays has failed and must be replaced.

e. Reconfiguration may be achieved within limits established via the system architecture by reconnecting arrays to the bus.

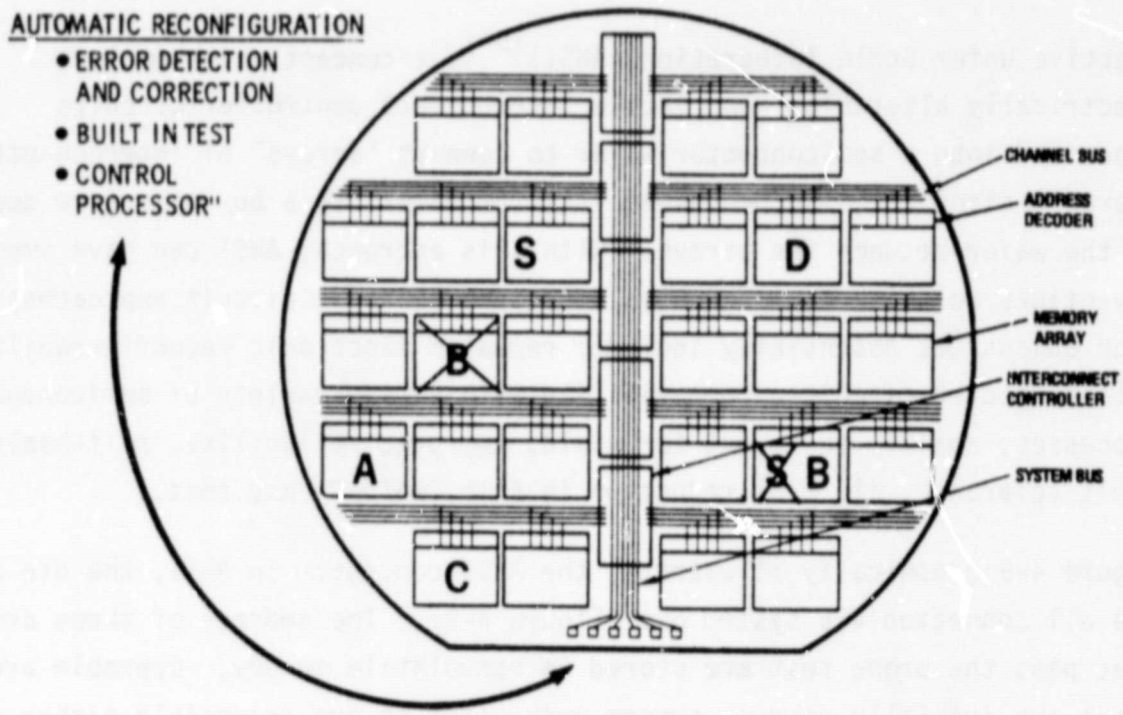


Figure 4-9. Adaptive Reconfiguration is Transparent to the User

Shown in Figure 4-8 are the specifications for a 10^9 Bit Recorder based on the MDAC ASWI approach. Shown in Figure 4-10 is the implementation of a memory wafer based on ASWI.

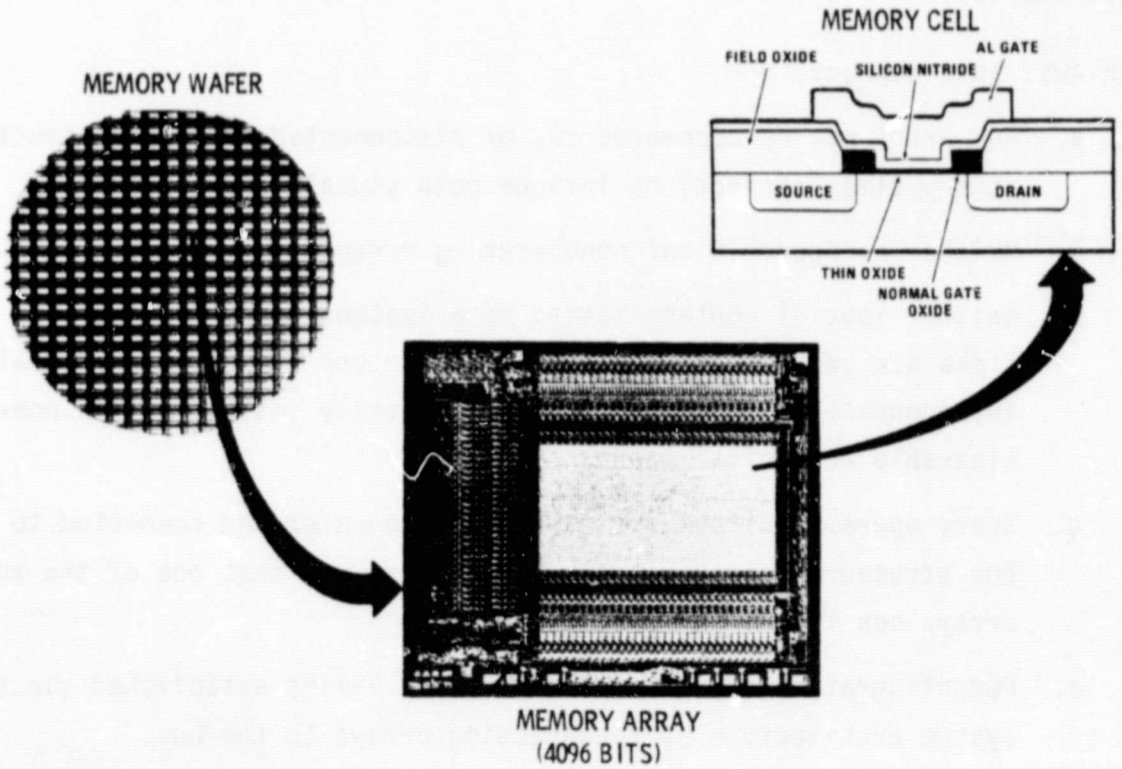


Figure 4-10. Adaptive Wafer Scale Integration Applied to Sequential Access Memory

MNOS memory growth is shown in Figure 4-11; based on the development work done by Westinghouse and MDAC a viable spaceborne solid state data recorder could be a reality by the end of the 1980s with storage capacities as high as 10^{12} bits and data rates as high as 300 Mbps.

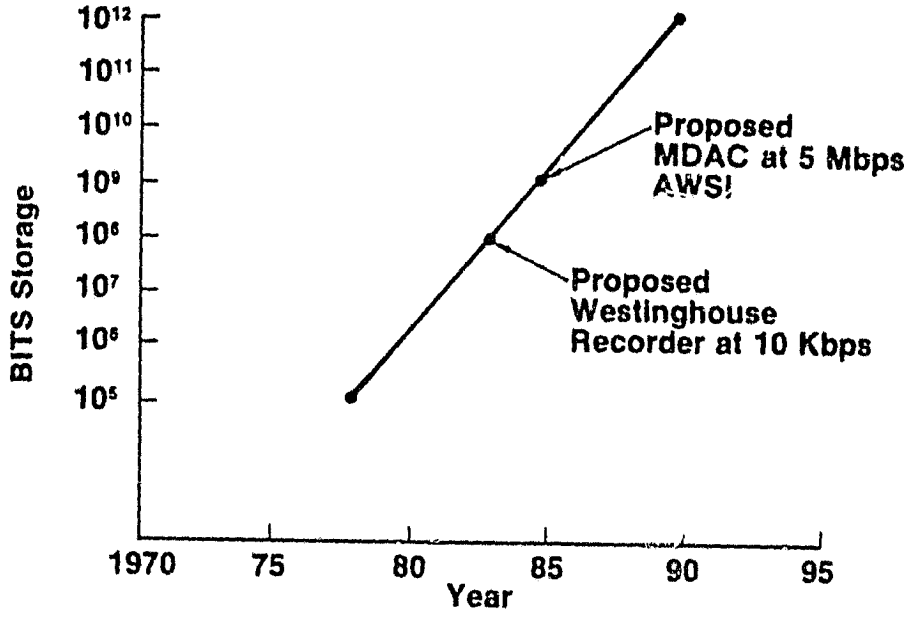


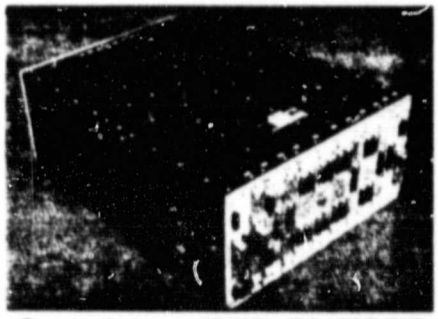
Figure 4-11. MNOS Memory Growth

4. Conclusions - As identified in the data system analyses the SASP will need more on-board storage with higher record/reproduce rates to be effective in a shared community of TDRSS users. Because of limited access to the single access channels of the TDRS the SASP will be required to store onboard scientific data which cannot be handled by the TDRSS Multiple Access Service. In conjunction with the limited TDRSS access time the data stored on board will then need to be played back at the highest rate ($\leq$ 300 MHz) possible to minimize the channel time required through the TDRS. Based on the technology surveys, several candidate technologies could be developed to perform this task. The most promising of these is magnetic tape; the technology exists now for ground-based machines. Current ground-based machines currently have 10^{12} bits of storage and record/reproduce rates in excess of 300 Mbps. With some development, solid state machines based on bubble memory could be realized with storage of 10^{12} bit limited and a maximum record/reproduce rate of 5 MHz. With a concentrated development of MNOS for solid state data recorders, it is felt that a 10^{12} bit storage machine with up to 300 Mbps could be realized by 1990.

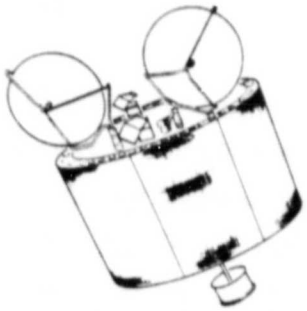
B. Multiplexers

1. Systems - Investigation of the major NASA programs provided us with no existing hardware which could be adapted for the SASP application; however, the Spacelab and Landsat D designs were candidate technology that would be applicable to the SASP. Demonstration of 300 Mbps was nearly achieved by the GSFC "Multimegabit Operation Multiplexer System" which was developed by the Harris Corporation in 1973.[16] The system consisted of two 140 Mbps subsystems with multiple inputs that were interleaved to produce a combined data rate of 280 Mbps. Although only a breadboard design, the capability of the technology was clearly demonstrated.

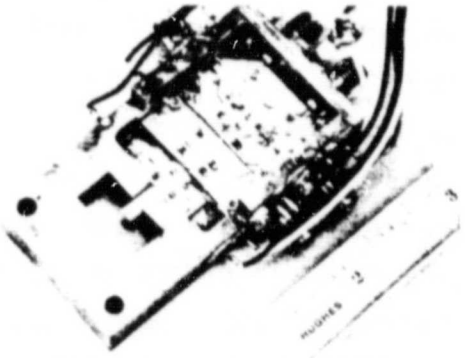
Due to lack of published data on the subject of high speed multiplexers on military programs a series of meetings were conducted with Motorola, Harris, and TRW. The subject was to address specifically the SASP Multiplexer and the application of work they have performed on other programs that would demonstrate the capability of the technology needed for the SASP. In all cases it was made clear that the technology exists and has been demonstrated for DoD spacecraft at $\geq$ 300 Mbps and work was underway to fly multiplexers at rates $\geq$ 1 Gbps.[18-22] Figure 4-12 illustrates some of the applicable hardware identified in our survey.



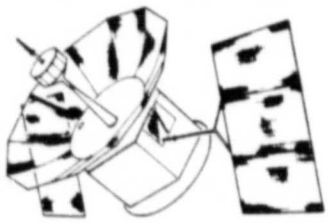
Spacelab – MBB 50 MBPS



MDAC/Motorola
1 GBPS



Hughes – G_aA_s 1 GBPS



DoD/Motorola
300 MBPS

Figure 4-12. Multiplexers

2. Technology -

High Speed Microcircuit Development

The speed of a circuit is measured in terms of the number of operations per second performed by the circuit. This speed can be increased by reducing the transistor size on the circuit or by selecting materials which have inherently faster characteristics.

Sometime in the 1980s, technologists anticipate we will begin to experience the upper limit of silicon IC speed performance, i.e., the ability of silicon integrated circuits to provide improved high-speed signal capability. Silicon-On-Sapphire (SOS) and Gallium Arsenide (GaAS) ICs offer very attractive advantages. Figure 4-13 qualitatively illustrates the speed progression experienced in the microelectronics industry.[17]

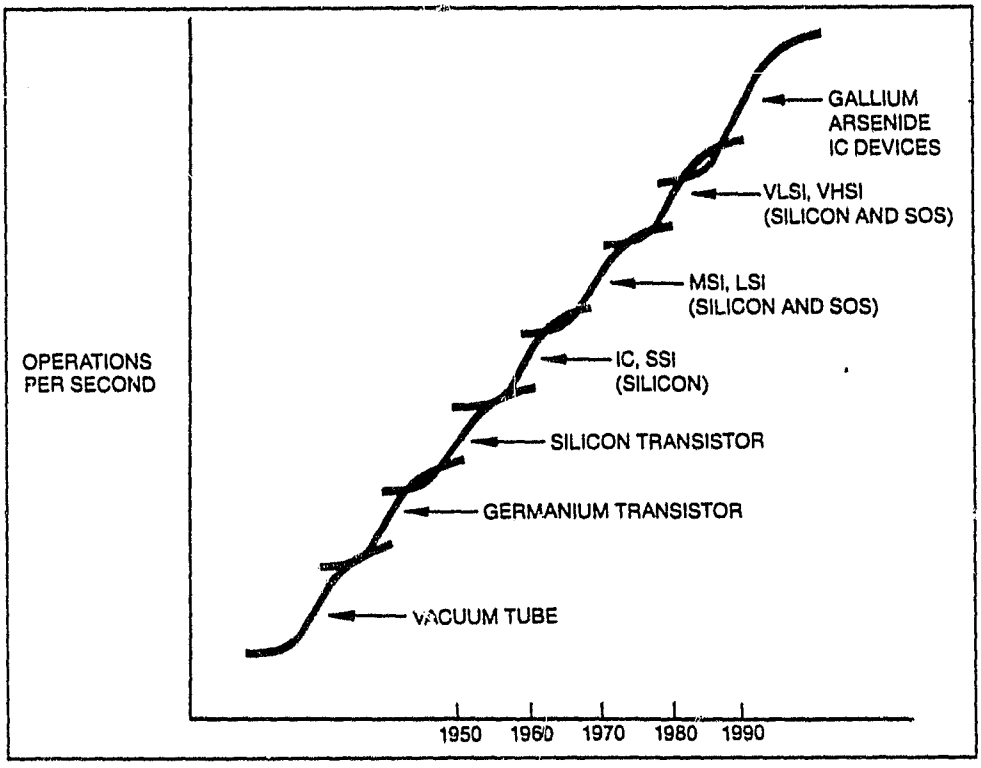


Figure 4-13. Progress in High-Speed Microcircuits - Includes extending the capabilities of silicon semiconductors through the use of Silicon-On-Sapphire (SOS) microcircuits and Gallium Arsenide GaAS) microcircuits.

Silicon-On-Sapphire (SOS) Integrated Circuits

SOS technology implies high-reliability, high-packaging densities, improved resistance to radiation, high-speed operation, and low-power dissipation. SOS gate delays of less than one nanosecond and power dissipation in microwatts/gate have been demonstrated. Most importantly, the SOS approach is potentially cost-competitive with bulk-silicon CMOS (complementary MOS).

Recent SOS product developments have been in the direction of increased density and the achievement of specific large-scale-integrated devices. Several companies are currently developing SOS/LSI devices in the form of microprocessors, semiconductor memories, and logic arrays. SOS microcircuits are being developed for use in future high-speed, low-power government electronic systems.

Gallium Arsenide (GaAs) Integrated Circuits

Gallium arsenide integrated circuits, with propagation delays ranging down to 100 picoseconds, are being developed to improve the speed performance over silicon and SOS integrated circuits. This work is proceeding rapidly - approximately 100 international research laboratories and government organizations are currently active in R&D programs to develop gallium arsenide integrated circuits and discrete semiconductors for commercial and government applications. GaAs ICs are achieved using a different device structure and manufacturing technology than those used for silicon ICs. Almost all GaAs devices are fabricated on a semi-insulating very high resistivity substrate (10^7 to 10^9 ohm-centimeters), essentially a dielectric. If the dielectric is used as a host substrate for interconnection metallization, the stray capacitance is much lower, meaning smaller Resistor-Capacitor (RC) time constants and therefore an improvement in speed performance.

Device construction is characterized by two types of metal systems for the gate, drain, and source electrodes. The gate region has a metallization system that ensures a good Schottky contact - the gate region of a Metal Semiconductor Field Effect Transistor (MESFET) is typically a Schottky barrier metal-semiconductor diode. The source and drain electrodes form ohmic contacts to the semiconductor.

The gate lengths of GaAs transistors range from one-half to two microns. In the 1980s the technology will be characterized by smaller devices with gate lengths less than one micron. Advancements are being made in every facet of GaAs device technology, but the most dramatic developments continue in the areas of GaAs transistors and high-speed GaAs IC logic. GaAs FETs are not only significant in that they provide functional capability not heretofore possible at higher frequencies; they also offer superior performance as low noise devices at lower microwave frequencies, thereby threatening well entrenched silicon bipolar devices.

Levels of integration range from a few transistors per chip up to 64 gates on a monolithic integrated circuit. IC development is being extended through the design, fabrication, and testing of analog high-speed circuits such as voltage comparators, and digital logic functions such as "Not OR" (NOR) gates, "Not AND" (NAND) gates, and flip-flop devices operating at system clock frequencies from one to three GHz.[23]

Future Microelectronics Development

In terms of speed projections, for digital integrated circuits we expect to see GaAs devices running at system clock rates on the order of two to ten GHz. In the 1985 time frame, we also expect silicon technology will be operated at system clock rates of up to one GHz.

Multiplexer growth is evolving with the advent of new high speed semiconductor technology; coupling this with improvements in microprocessor technology provides the base for flexible programmable multiplexers with combined data rates approaching 1 Gbps by the late 1980s. Figure 4-14 shows graphically the projected growth for spacecraft multiplexers through the 80s.

3. Conclusions - Based on the need to maximize the data capability for multiple and changing payloads a new multiplexer was identified for the SASP CDMS. This was defined as a multiple input device (programmable) that could handle data inputs as maximum rates of 150 Mbps and as little as 2 Mbps. In addition to the digital inputs, an analog channel for video data was provided which digitized the information and multiplexed it with the other digital inputs.[24] Maximum output was 300 Mbps which was the maximum data rate compatible with the TDRSS.

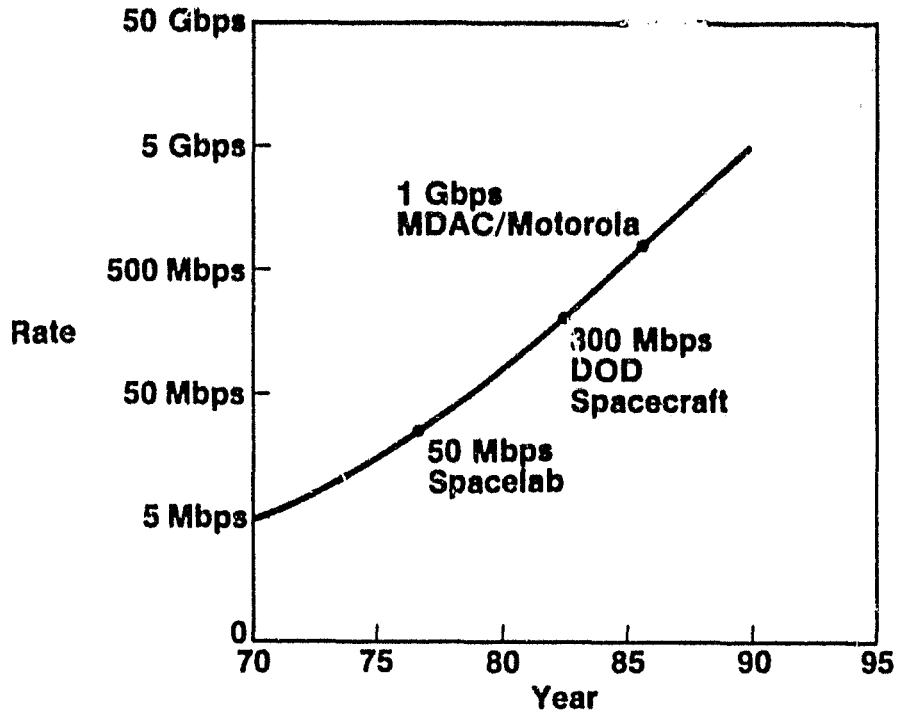


Figure 4-14. Multiplexer Growth

Several electronic companies are presently developing the technology and multiplexer systems that are applicable to the SASP multiplexer. In our discussions with these companies it was felt that much of the DoD spacecraft work on multiplexers that they are doing could be applied to our design requirements. A qualified unit could be provided based on existing state-of-the-art technology by 1985.

C. On-Board Signal Processors

Signal processing is a very broad subject. Spectrum analysis, sensor data comparisons, image enhancement, coding and decoding, error detection, and bandwidth compression are just a few of the examples of signal processing. Everyday newer more stringent requirements are placed upon signal processing. One example of this is the Ballistic Missile Defense Forward Acquisition System (FAS) need defined here at MDAC.[25] The FAS is a probe vehicle that is used to detect, discriminate, and track objects outside the atmosphere using infrared sensors (Figure 4-15).

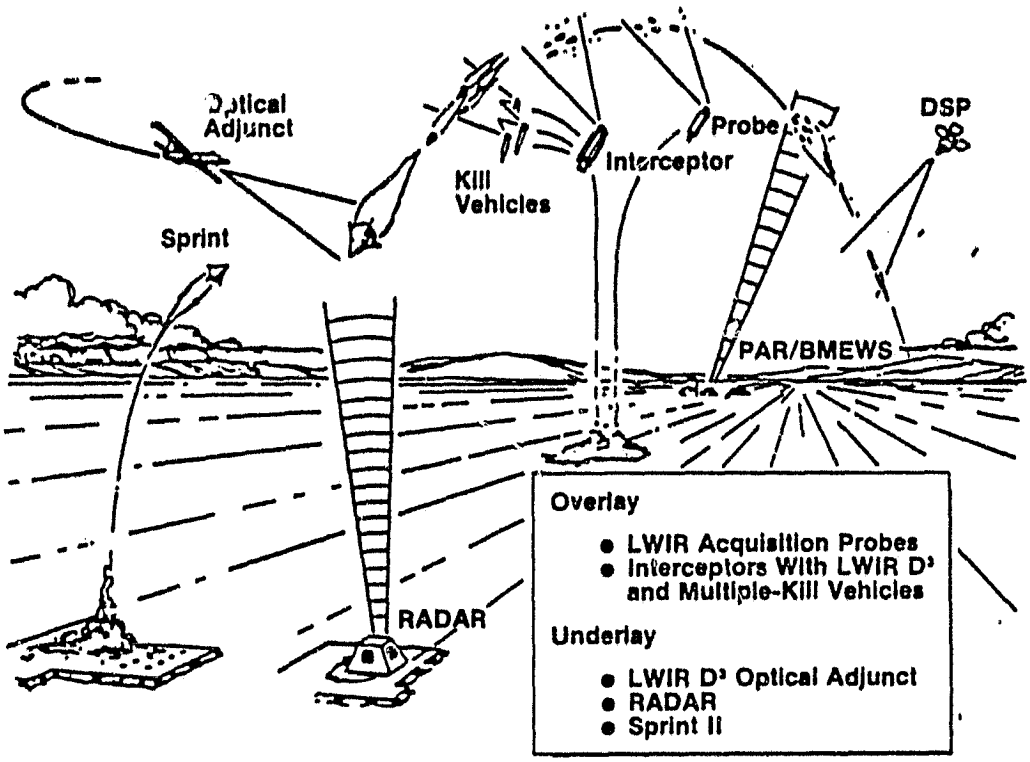


Figure 4-15. BMD Layered Defense System Concept

The FAS sensor scans its assigned sector of the sky. The IR detector outputs are multiplexed and converted to digital signals on the sensor gimbal. The data rate out of the sensor is equal to or greater than 200 Mbps. The signal processor, which may be hard-wired or programmable, performs mostly repetitive, data-content-insensitive functions, such as matched filter processing and closely-spaced object correlation. Resulting object data is passed to the data processor, which performs detector correlation, coordinate transformation, scan-to-scan correlation, state estimation, and discrimination. The state vector of objects that remain are then communicated to the ground (Figure 4-16).

The signal processing functions are mostly repetitive and are not complex but must be performed at extremely high rates. These requirements indicate a hardwired, special purpose processor, although some consideration has been given an array of RCA CMOS/SOS microprocessors. The design approach for the data processing function uses a special purpose network of distributed microprocessors. For the most part, general purpose components (processors, memory, and buses) are used in this network. Bit-slice architecture with bipolar semiconductor technology is a candidate implementation (Figure 4-17).

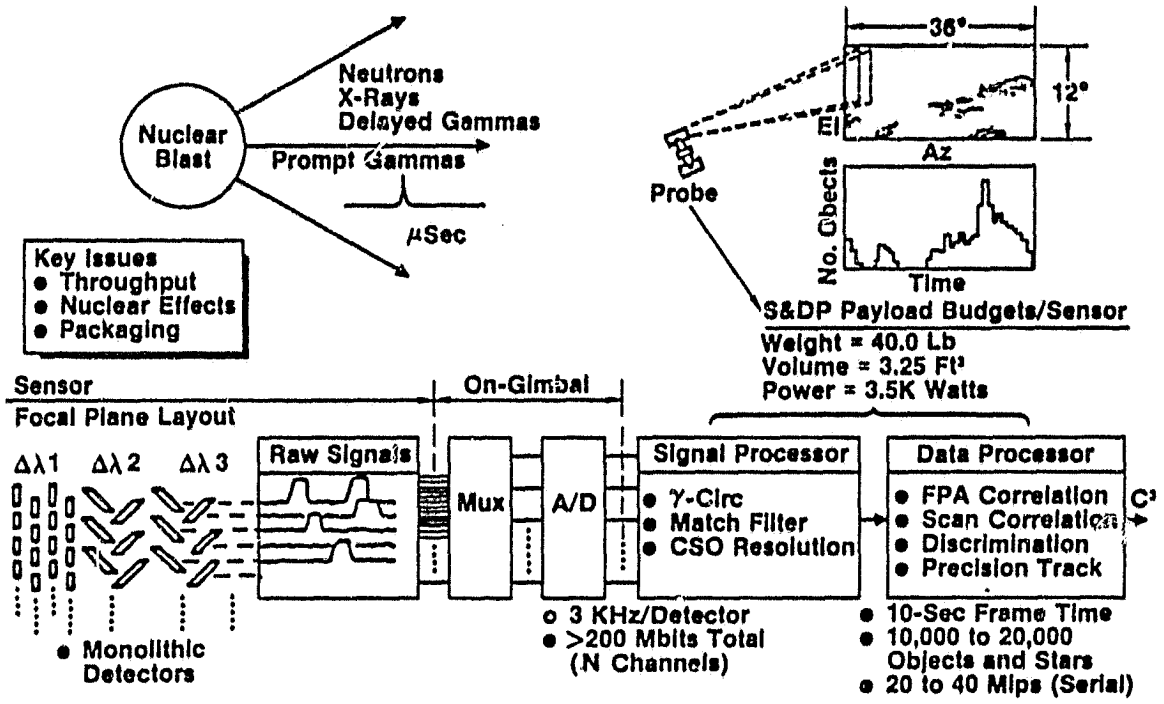


Figure 4-16. BMD FAS Signal and Data Processing Requirements

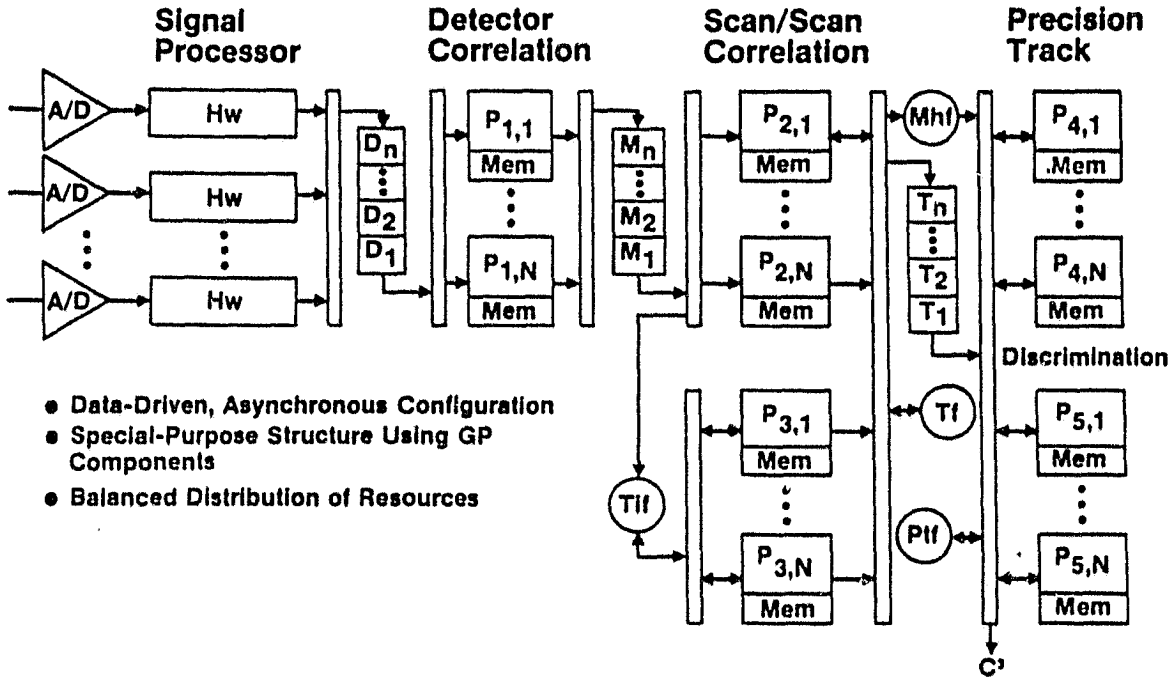


Figure 4-17. S&DP Conceptual Design

MDAC has implemented a prototype distributed programmable signal processor based on existing bit slice architecture. The system was tested using sensor data showing that near real time images could be processed at execution rates of 16 million operations per second. This same design was evaluated using GaAs E-JFET (1 μm Channel) with projected performance of over 60 million operations per second.[26]

Another thrust to develop extremely fast, highly powerful, highly dense processing facilities is the Very Large Scale Integration (VLSI) work going on.[27] A Department of Defense project is looking into VLSI as a solution for the dilemma. The project, dubbed Very High Speed Integrated Circuits (VHSIC), will develop a processor capable of several billions of operations every second. Production is slated for 1986 and the product will contain more than 250,000 gates which will be clocked to 25 MHz minimum. Applications should include radar signal processors, guidance for the global position satellite and various missiles, signal modulation and classification analysis, sonar acoustic data analysis and electro-optical data processing. Problems do exist and need to be overcome before VHSICs can be borne. Five μm geometries will be necessary to provide for higher throughput rates and less power consumption. Several layers will need to be built onto one chip while architectures need to be developed to allow these chips to be as standard as possible. Use of computer aided design will have to be developed for layouts of structures and to test logic. Though an old technique, CAD was not economical for use in designing anything less than VLSI. The use of Gallium Arsenide for high speeds should be developed. However, DoD does not foresee VHSIC GaAs chips immediately. VLSI GaAs will be available by 1985,[28] but the silicon technology is still much more mature. E-beam direct writing will have to be developed for accuracies to 0.1 μm in alignment and exposure.

Trends in processing speeds and computational power continue to rise and relatively high requirements in the future will have to be met. Currently, for example, SAR real time data processing requires about 3 million instructions per second (MIPS) while future requirements are 100-500 MIPS. Similar capabilities will soon have to be provided in areas of tactical signal intelligence, over-the-horizon fire control, global search and rescue systems, and gigabit per second data links. Much work has been done in the past year in processing SAR raw data in real time.[29-31] Due to its nature, SAR produces

a very high data rate (approximately 120 Mbps) which is extremely difficult to process in real time. Currently there exists ground based and aircraft processors which can do a fair job of outputting images from SAR in near real time.[32] Real time here is not necessarily true real time in that the data to be processed might be delayed in seeing the input interface of the processing system.

In SAR processing there are billions of complex mathematical operations which must be performed. Corrections for eccentricities of flight path, antenna pointing inaccuracies, four-look presumming, target curvature and migration of targets by earth rotation must be taken into account also. With the many operations that are associated with these functions, digital time domain processing becomes a large task. For instance, SEASAT data was taken for about 3000 minutes of which only 2100 minutes had been processed by mid-September 1980. Fast Fourier Transform (FFT) analysis using Charge Coupled Device (CCD) technology is one alternative tool. FFT techniques can reduce millions of operations to tens of thousands of operations. The transforms and filtering correlation may be performed in the range direction by "signal-by-weighing" multiplications in a CCD shift register while azimuth correlation is done similarly in many parallel CCD filters. FFTs and CCD filtering will both require the advantages of LSI/VLSI technologies to perform the transverse filtering functions at such high data rates.

To produce a digital SAR data processor, many millions of dollars will have to be spent and more concise data product requirements are going to have to be defined. Predictions now say that only after 1990 will there be any reliable form of processor for processing all the SAR data digitally in real time on-board.

Another processing facility being developed is the NEEDS defined massively parallel processor (MPP).[35] Design plans for the MPP demand six billion adds and one billion multiplies of eight bit binary numbers per second. The processor's original intent was to process image signals in the range of 10^{10} to 10^{12} bits per second in real to near real time. Todays computers are seriously hampered for image processing by maximum operations/second rates of only 10^{8} to 10^{9}.

Figure 4-18 shows an overview of the Information Adaptive System. The Information Adaptive System is a set of hardware and software designed to interface directly with the data source (sensor) onboard the spacecraft and provide direct preprocessing and editing to the maximum extent feasible.[36] Included in this NEEDS effort are data editors, calibration and preprocessing algorithms, selectors for identifying desired data sets and buffer data storage. The entire system is directed by an adaptive controller which can respond to ground controls and reconfigure the onboard data system as needed. The major thrusts of these technology activities are to provide real-time data processing and minimize the amount of data which must be sent from the spacecraft to the ground.

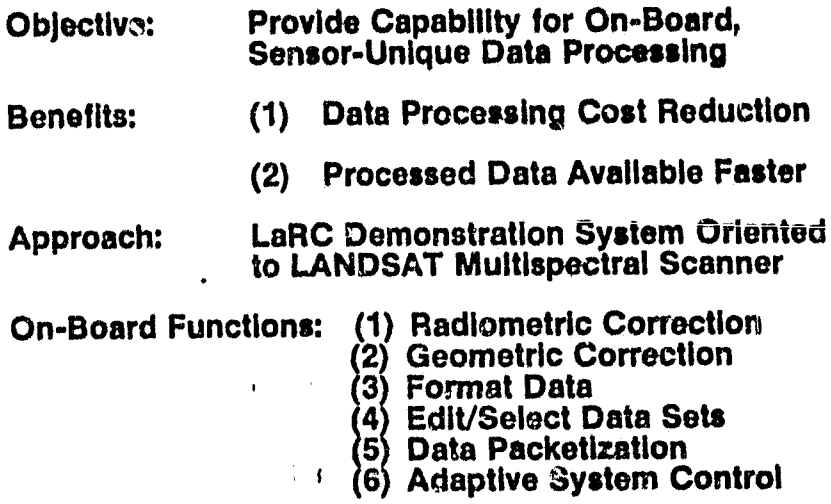


Figure 4-18. Information Adaptive System (IAS)

An ongoing long term technology activity related to the information adaptive system is underway to exploit advanced processor technology to allow real-time onboard information extraction. Information extraction from space-acquired data enables global assessments of environmental status and resources. One form of information extraction, feature classification, is a difficult task requiring the comparison of space-acquired data with several theoretical models constructed by a computer from information about a potential target's electromagnetic radiation intensity, reflectivity, and other distinguishing characteristics. In previous NASA experimental programs, for example the Large-Area Crop Inventory Experiment (LACIE), classification of space-acquired

data required a large ground-based computer facility supported by a staff of photointerpreters to manually classify crops in training and test fields.

As the acquisition and dissemination of space-acquired data moves into an operational environment, real-time onboard information extraction will be required. Presently a new analog-binary charge-coupled device (CCD) integrated circuit has been designed and fabricated to perform high-speed (15 Mbps) feature classification, based on the maximum likelihood, Gaussian probability classification algorithm. The thrust of this effort is to provide the technology base for onboard information extraction.

Although technology will allow increasingly more on-board data processing, and many advantages accrue from on-board data processing; its use for scientific sensors may be limited by the inability or reluctance to define a limited set of data products so that on-board processing can be implemented. A natural tendency among scientists is to want to retain all the raw sensor data that is acquired. A process of education and mutual understanding between scientists and data processing system designers is necessary before on-board data processing for scientific sensors is practical.

Figure 4-19 shows the trend of spacecraft computer performance and some potential future processor performance regimes. Included are the Massively Parallel Processor, SAR Processor, and the Information Adaptive System as onboard systems. Typical functions performed by spacecraft computers are shown at the right, coded to indicate typical functions of current and future spacecraft computers. As indicated earlier, processor performance necessary to achieve on-board SAR data processing is not an easy task and will require performance improvement in excess of normal projections.

CONCLUSION

Identified in the F5 data system analysis is the problem of handling the Ocean Synthetic Aperture Radar (OSAR) within the constraints of the TDRSS. Even by increasing the amount of on-board storage and maximizing the downlink data rate most of the data is lost (ref. Figure 3-16/17/18). The only solutions identified were: (a) utilize more TDRS Single Access Time, (b) not use the TDRSS but have a dedicated RF link, or (c) provide on-board processing to achieve data compression compatible with the TDRSS constraints.

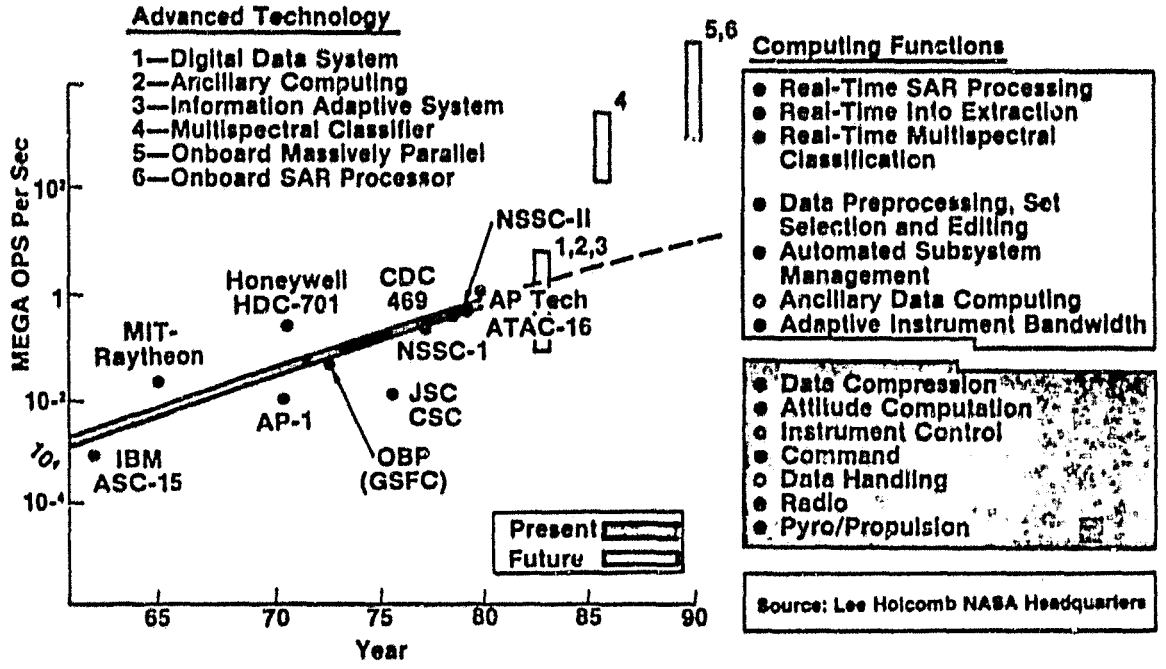


Figure 4-19. Spacecraft Computer Performance Trends

Based on the research done, the technology is available so that onboard signal processors are achievable in the future. For NASA programs much development work needs to be done to provide onboard versions of hardware being developed for ground applications. The technology work that the DoD is doing in CMOS and GaAs and distributed processors is applicable. In addition to solving the communication bottleneck problem, the onboard processor, by greatly reducing the amount of data coming down, also greatly reduces the cost of ground data processing and provides more timely information to the users.

Section 5
CONCLUSIONS

As can be seen from the results of the simulation on F5, new technology required are multiplexers, onboard storage and/or onboard signal processing. The A8, though less stressing, also identified the need for increased onboard storage and larger multiplexing capability and to a less degree onboard signal processing would have helped. The primary driver behind this was the limited access to the TDRSS for single access channels which means that there will be long periods of time when it will not be possible to downlink data > 50 Kbps. The reason behind the limited access is obvious in that the few number of channels must be shared with all the low earth orbit spacecraft plus the Shuttle. In this regard the SASP helps to alleviate the problem if the technology were available to support the desired configuration. Data compression (onboard signal processing) allows the useful/processed data to be stored for long periods of time and then when the TDRS is accessable a high storage reproduce rate will take maximum advantage of the TDRS bandwidth. This is illustrated for both F5 and A8 in Figures 5-1 and 5-2. By combining the candidate multiple payloads into a optimum data stream less TDRS access time is required than if this were individual free-flyer payloads; this was considered to be one of the most significant advantages of the SASP.

For the technology items identified, our surveys show that the hardware will or could be available in the time frame addressed to support the SASP type of groupings; this will depend however, on the resources applied to the development of these items for onboard applications. The onboard storage devices currently being developed could be adapted for the A8 usage with minimal cost and risk; to support the F5 type of data rates would require a new onboard storage device requiring significantly more development. The high rate multiplexer onboard is considered well within the state-of-the-art for onboard implementation and should require minimal development to adapt existing DoD technology to the SASP requirements. Onboard signal processing

	Free Fyers (No Storage)	Free Flyers (With Storage)	SASP (32 Mbps (Storage)	SASP (100 Mbps Storage)
Data Transfer Time (Min/Day)	2295	682	594	329
Acquisition Time (Min/Day)	134	102	70	38
Total SA Time Req'd (Min/Day)	2429	784	664	367

Figure 5-1. SA Channel Utilization
A8 SASP vs. Free-Flyers

	Free Flyers (No Storage)	Free Flyers (With Storage)	SASP (64 Mbps Storage)	SASP (100 Mbps Storage)
Data Transfer Time (Min/Day)	1699	1259	480	308
Acquisition Time (Min/Day)	192	162	64	64
Total SA Time Required (Min/Day)	1791	1421	544	372

Figure 5-2. SA Channel Utilization
F5 SASP (w/o OSAR) vs Free Flyers

is considered payload unique in its application; but for many of the candidate sensors the technology is being developed that could support data compression/editing onboard the SASP.

In addition to the advantages identified for the SASP, onboard signal processing solves another part of the end-to-end data system problem in the form of eliminating large signal processing tasks at the ground stations and providing a more timely access to the data.

Many areas affecting the total SASP End-to-End Data System have not been addressed in depth by the results of our study. Some of those which have surfaced as meriting more attention are listed here and should be considered as candidate subjects of future studies. Certainly as better definition of applicable payloads becomes available realistic studies can be performed to address these issues as they apply to SASP. Some of the areas of concern are:

- Multiple access return link realtime support is limited to 1 MA channel per user presently and forward link must be time-shared between users.
- Ancillary data on-board is important to the overall SASP End-to-End Data System to provide spacecraft autonomy, complete experiment data (packetizing) and both cost effective data and operations.
- With the quantities of data being discussed onboard the SASP, ground processing may become a bottleneck if not properly planned.
- Along with ground processing, distribution of data in an efficient and timely manned must also be addressed.
- In some cases dedicated ground stations and communications links may be more effective than trying to downlink all data through the TDRS.
- Last but certainly not least is the need for standardization at the experimentor interface. Standard interfaces are needed to simplify the integration into the SASP; standard formats will further simplify the integration task and provide a much easier task of data reduction on the ground. Software development for experiment Command & Data Management Systems/Dedicated Experiment Processors has provided some of the biggest cost problems to data on both Spacelab and Space

Telescope experiments. Standard interfaces and a unified, systematic approach to experiment software development is needed to minimize these difficulties for SASP.

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