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Progress Briefs

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W. Murray Bullis, Editor

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SEMICONDUCTOR TECHNOLOGY PROGRAM

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ABSTRACT - This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: optical linewidth and thermal resistance measurements, device modeling, dopant density profiles, resonance ionization spectroscopy, and deep-level measurements. Brief descriptions of selected on-going projects are included, and recent publications and publications in press are listed. Standardized oxide charge terminology developed by a joint IEEE-ECS committee is also described. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

KEY WORDS - Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report covers results of work during the forty-eighth quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 4. The Defense Nuclear Agency; 5. The C. S. Draper Laboratory; 6. The Naval Air Systems Command; 7. The Air Force Wright Aeronautical Laboratories; 8. The Army Electronics Technology and Devices Laboratory; 9. The Naval Weapons Support Center; 10. The Solar Energy Research Institute; 11. The Naval Avionics Center; 12. The Lewis Research Center, National Aeronautics and Space Administration; 13. The Office of Naval Research; and 14. The Naval Ocean Systems Center.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported here are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.



Semiconductor Technology Program

Progress Briefs



Optical Linewidth Measurements

Analysis of the interlaboratory experiment to evaluate the optical linewidth measurement procedures developed in this program was completed. This study has provided considerable information on the usefulness of the NBS linewidth measurement artifact and the associated procedures for measuring linewidths on photo-masks in transmitted light.

The measurements of the participants exhibited systematic differences among themselves and from those of NBS. Although a line-spacing calibration improved some of the largest systematic errors, this type of calibration was not sufficient to bring the participants into agreement with NBS. In a few cases the initial adjustment of the system in accordance with an NBS-furnished line-to-space ratio and a line-spacing value was sufficient for calibration over the dimensional range of 0.5 to 12 μm . More generally, a linewidth calibration curve was necessary. A constant offset was adequate in some cases; a linear linewidth calibration curve was satisfactory for most measurement systems used in the study. The results show that a separate calibration curve or constant offset is required for measuring lines of different polarity (opaque and clear). Many of the measurement systems appeared to have flare, or scattered light, which affected the magnitude of the systematic error for opaque lines as compared with the systematic errors for clear lines.

The data from this study clarify the need for measurement-control procedures in many of the measurement systems. Outliers were prevalent in the data and must be considered as part of the normal operating characteristics of such systems. Single outliers in the data were

frequent; in the case of several systems, an entire set of measurements (taken during a single day by a single operator) was out of statistical control. The standard deviation of the measurement process was close to or greater than $\pm 0.1 \mu\text{m}$ for about half of the measurement systems. For some of the systems, there were also significant day-to-day differences and operator differences. In these cases, the calibration curve may be applicable only to an average of measurements made over several days, and calibration curves based on one operator may be restricted to measurements by the same operator.

The results of the study show that the NBS artifact and the associated measurement procedures are basically adequate for calibrating an optical-microscope linewidth measurement system in the 0.5- to 12- μm region provided that the system is in a state of statistical control. Based on the results of this study, the pattern on the artifact was changed slightly and the procedures were rewritten to improve their usefulness. The improved version of the artifact is being made available as SRM 474 (Optical Microscope Linewidth Measurement Standard).[†] [Sponsor: 2]

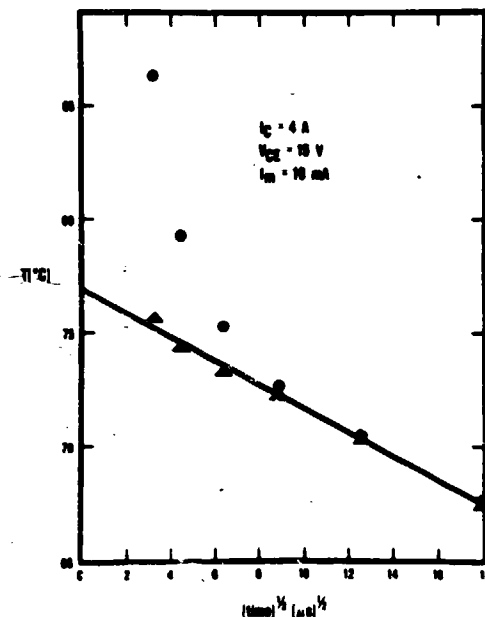
(J. M. Jerke, x3621, and C. Croarkin* and R. Varner,* x2806)

Thermal Resistance Measurements

In qualifying the equipment built to measure the thermal resistance of power transistors being certified as standard reference materials for thermal resis-

*NBS Statistical Engineering Division.

[†]SRM 474 may be purchased from the Office of Standard Reference Materials, Room 3111, Chemistry Building, National Bureau of Standards, Washington, DC 20234, at a price of \$3600.



Cooling curve for a bipolar transistor mounted on a TO-3 header. Points are shown for 10, 20, 40, 80, and 160 μs after switching from the collector current I_C to the measuring current I_B . Un-corrected data are shown as O; data corrected for the effect of the transistor leads are shown as Δ . The solid line shows the expected square root of time dependence of the junction temperature.

tance measurements, it was discovered that the kovar leads used in the hermetic packages can cause a substantial amount of error in making the measurement.

The test for thermal resistance involves switching the collector current of the transistor from a high value to a low value; the temperature-sensitive parameter, which is the base-emitter voltage in this instance, is measured as soon after the switching as possible so that the device has not had time to cool significantly. Ideally, the voltage waveform observed across the base-emitter junction is a large step decrease on which is superimposed a small time-dependent increase. This increase re-

sults from the change in junction temperature which is expected to decrease as the square root of the time after the device is switched. In practice, the voltage is measured at the external leads of the transistor package rather than at the body of the transistor. Typically, the apparent temperature is found to decrease much more rapidly than expected at early times as illustrated by the uncorrected data in the accompanying figure.

The kovar leads introduce substantial distortion in the measured base-emitter voltage waveform. The effect of this distortion lasts for over 100 μs and is in a direction which would cause the observed deviation of the cooling curve from the expected form. The distortion was observed directly as an overshoot when the chip was disconnected from the leads on a TO-3 header and replaced by a copper shorting bar soldered across the base and emitter leads, and the large heating current and small measuring current were alternately driven through the device by the thermal resistance circuit. No distortion was observed in the waveform generated for a U-shaped piece of copper wire inserted into the socket in place of the TO-3 header, or in the waveform generated for a 3-cm long piece of solder (which had the same resistance as the kovar leads) inserted into the socket in a similar manner. However, a steel paper clip inserted into the socket also produced distortion in the waveform. It is surmised that the magnetic material present in the kovar leads is responsible for this effect. There appears to be some contribution by the TO-3 header itself if it is magnetic, as the distortion is slightly less for non-magnetic headers.

The cooling curve can be corrected by subtracting one-half the value of overshoot for any given time from the measured voltage (one-half because in practice the heating current is passing through the emitter lead only). An example of a corrected curve is shown in the accompanying figure.

This observed deviation from the ideal cooling curve has in the past always been referred to as being caused by non-thermal switching transients. The effect is more pronounced at higher currents and was often thought to be the result of not being able to quickly and completely switch the transistor from one state to another. It is not observed in measurements made on plastic power transistors with nonmagnetic leads. [Sponsor: 2]

(D. W. Berning, x3621)

Dopant Density Profiles

Dopant density profile data were obtained on several uniformly doped silicon wafers from 1-MHz capacitance-voltage (C-V) measurements on p-n junctions and Schottky barrier diodes and from dc measurements on four-terminal MOSFETs. The experiments were carried out to compare these nondestructive electrical techniques and to identify limitations and influences which impact the results. It was found that the analysis techniques currently being used did not always yield dopant density values which are constant with depth into the wafer.

The C-V measurements on the p-n junction yield the correct dopant density, compared to bulk resistivity determinations, at shallow depths but indicate increasing values of dopant density at depths greater than a few micrometers. This increase is attributed to a small amount of parasitic MOS capacitance that becomes a significant fraction of the total capacitance as the bias voltage is increased. Hence, as the bias voltage increases, the measured capacitance decreases less rapidly than expected for uniformly doped material. The analysis program now being used corrects for peripheral capacitance effects and for the nonabrupt junction, but does not provide for inclusion of parasitic capacitances. Therefore, it interprets the slower capacitance decrease as an increasing dop-

ant density. This increase is greater for smaller devices, consistent with the parasitic capacitance explanation. A similar effect has been observed in the C-V measurements on Schottky diodes.

Profile measurements on four-terminal MOSFETs with channel lengths up to 36 μm yield gradually decreasing dopant density values with increasing depth in specimens with a low value of dopant density ($3 \times 10^{14} \text{ cm}^{-3}$). This result is attributed to short-channel effects in the MOSFET; as yet the analysis program does not include these effects. Although the results obtained with these three techniques agree to within about 25 percent, it will be necessary to develop analysis programs which correct for the effects which are responsible for these divergent trends before these techniques can be optimized for application to the specialized requirements of VLSI technologies. [Sponsor: 2]

(G. P. Carver, x3541)

Device Modeling

An improved computer code for analysis of surface channel MOSFETs was developed. In this code, the charge-sheet model originally proposed by Brews was modified and extended to short-channel (0.5- μm) surface channel MOSFETs. Two-dimensional electrostatics and an improved formulation of the surface channel electron density are combined with an adaptive multigrid finite element technique. Current-voltage characteristics of MOSFETs can be calculated with two- and four-fold memory space reductions and speed increases of four- to ten-fold over conventional finite element and finite difference approaches. These results are achieved by 1) elimination of one of the equations usually used in short-channel models and 2) improvements in numerical methods which allow detailed simulations of MOSFETs to be performed with high accuracy on large minicomputers. The effects of channel implants and field dependence of mobil-

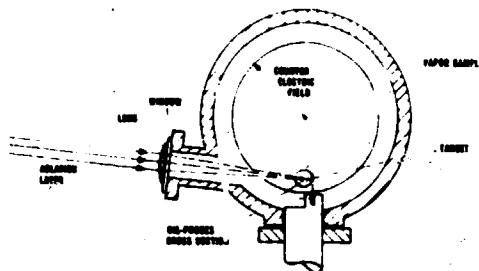
ity are easily included in the model. In the long-channel, constant-mobility case, the model is identical to the model deduced from long-channel theory. In the short-channel case, the effects of channel doping, oxide thickness, and source-and-drain profile shape are fully included. This code will be made publicly available after further testing and publication of the underlying theory. [Sponsor: 2]

(C. L. Wilson, x3625, and J. L. Blue*)

Resonance Ionization Spectroscopy

Sodium has been detected qualitatively in three semiconductor specimens by means of a new analytical technique based on laser ablation and resonance ionization spectroscopy (LARIS). The test specimens were a high-resistivity (500- to 1200- $\Omega\cdot\text{cm}$) *p*-type float-zoned silicon slice with {111} faces, a dislocation-free (50- to 100- $\Omega\cdot\text{cm}$) *n*-type float-zoned silicon slice with {511} faces, and a silicon-doped (0.0036- $\Omega\cdot\text{cm}$) gallium arsenide slice with {100} faces. The experimental apparatus consists of a cylindrical proportional counter provided with ports to admit the test specimen, an ablation probe, and two analytical probes; a cross section of the counter is shown in the accompanying figure.

A small volume from the test specimen ($\sim 10^{-9} \text{ cm}^3$) is vaporized inside the proportional counter by a dye laser pulse with irradiance in the 10^7 W/cm^2 range. Equilibrium of the evaporated material in the counter atmosphere is reached in a few microseconds after the ablation pulse, which is focused to a diameter of about 0.1 mm. By irradiation of this equilibrated material with two laser beams of appropriate frequencies, photoionization of a particular atomic species contained in the vapor can be achieved as previously discussed for the case of sodium in a gaseous sample. The released electron is subsequently multiplied and detected as an



Cross section of LARIS counting chamber. The target is the specimen surface; the two laser beams (RIS probes) used for photoionization are 3 mm in diameter; they are directed coaxially in opposite directions parallel to the counter axis and displaced about 3 mm away from the specimen surface.

electrical signal associated with the photoionized atom.

Several effects associated with the ablation process influence the vapor sample composition and consequently may impose severe limitations on obtaining quantitative data with the LARIS technique. The ablation laser first generates a plasma in the atmosphere in front of the specimen surface. For the laser irradiances used, a laser-supported absorption wave (LSAW) is generated in front of the target. It expands both axially up the laser probe and radially over the target surface with velocities in the 10^4 cm/s range. Heat is injected into the specimen surface through uv-radiation transport and thermal conduction mechanisms. While the ablation pulse is on, the surface temperature at the focal point rapidly rises until the plasma density is high enough to cause probe decoupling by the expanding LSAW front. In particular, the specimen crystallographic orientation influences the crater characteristics. On {111} silicon surfaces, cone-shaped craters with abundant material redeposition are developed. The ejected material is compressed back by the front of the laser-supported absorption wave generated by the ablation pulse, and a melted material rim is developed around the

*NBS Scientific Computing Division.

crater. The rim protrudes above the surface forming a wall that stops material flying close to the surface. On the other hand, on {511} silicon surfaces, shallow bowl-shaped craters with no significant material redeposition are developed. Differences were also observed between craters produced on lapped and polished surfaces. These various differences illustrate a strong influence of the surface properties on the ablation mechanism.

To obtain quantitative data from the LARIS technique, it will be necessary to establish a correlation between the density of the detected species in the vapor sample and its number density in the specimen. This requires further characterization of the specimen and its influence on the ablation process, the dynamics of the LSAM, and the equilibrium conditions in the chamber atmosphere following the ablation pulse. [Sponsors: 2,14] (S. Mayo, x3625; and G. G. Luther,* x2061)

Deep-Level Measurements

Optical absorption studies of sulfur-doped silicon have shown closely spaced absorption lines that do not appear to come from a single species, but do appear to be related to the presence of sulfur. A model that attributes these closely spaced lines to a group of sulfur-impurity or sulfur-defect complexes has been proposed. Details of this work were presented at the March 1980 meeting of the American Physical Society and will appear in *Applied Physics Letters*.

Multiple levels with closely spaced energies cannot be resolved by electrical deep-level techniques with a precision equivalent to that of the optical measurements. Recent deep-level transient spectroscopy (DLTS) measurements on junction diodes have shown that, at any given fixed temperature, the thermal emission rate (the measured quantity from which activation energy is derived)

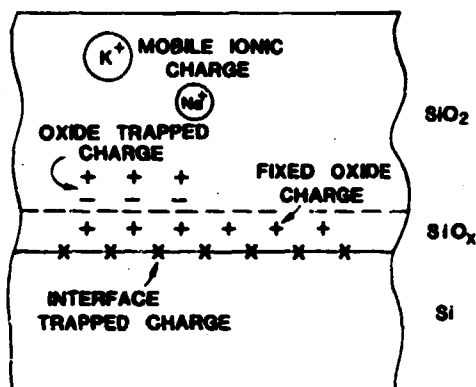
is not a unique characterization parameter for the levels observed in sulfur-doped silicon. Specifically, it has been found that the thermal emission rate is a function both of depth below the P-N junction and of the previous thermal history (i.e., processing) of the test device. Differences in the temperature of the measured DLTS peak position for a given emission window (i.e., given double-boxcar sampling time settings) were observed in two specimens which had been prepared for optical absorption measurements by diffusion of sulfur into silicon at 1350°C in evacuated, sealed quartz tubes. One specimen had been diffused for 22 h and the other for 200 h.

The variations of the electrical results obtained to date are consistent with the variability expected if sulfur gives rise to a manifold of closely spaced states in silicon. Measurements are in progress to determine whether this situation is peculiar to sulfur or is also a characteristic of elements such as gold or platinum which are commonly used for lifetime control in silicon. If sulfur is not exceptional in this regard, it may seriously impact the significance, understanding, and value of deep-level measurements for many applications. [Sponsors: 2,3] (W. E. Phillips, W. R. Thurber, and R. A. Forman, x3625)

Oxide Charge Terminology

A committee[†] established by the Electronics Division of the Electrochemical Society and the IEEE-sponsored Semiconductor Interface Specialists Conference has proposed standardized terminology for oxide charges associated with thermally oxidized silicon. The recommended names for the four types of charges

[†]NBS Center for Absolute Physical Quantities. The committee was chaired by S. E. Deal, Fairchild. Other members were: W. M. Bullis, NBS; S. R. Butler, Lehigh; E. H. Nicollian, Bell Labs; and D. R. Young, IBM. A. Reisman, IBM, was the IEEE Electronics Division representative and A. Tasch, TI, was the IEEE SISC representative. P. Balk, Aachen, and T. Sugano, Tokyo, were the European and Japanese representatives, respectively.



Names and location of charges in thermally oxidized silicon. © 1980 IEEE.*

present in this system are given in the accompanying figure which also illustrates their locations. The symbols Q and N , suitably subscripted, are proposed for the net effective charge per unit area and the net effective number of charges per unit area, respectively, at the silicon-silicon dioxide interface. Therefore, $N = |Q/q|$, where q is the electronic charge. The recommended unit for Q is coulomb per square centimeter and for N , number per square centimeter. The sign of Q is either positive or negative depending on whether the majority of charge is positive or negative. By definition, however, N is always positive. Also, it should be kept in mind that Q and N are defined as effective net charge at the silicon-silicon dioxide interface, even though the actual charge density may be considerably larger if the charge is located some distance from that interface. Uncharged trapping centers are not covered by this proposed terminology. The recommended symbols are:

Fixed Oxide Charge	Q_f, N_f
Mobile Ionic Charge	Q_m, N_m
Interface Trapped Charge	Q_{it}, N_{it}
Oxide Trapped Charge	Q_{ot}, N_{ot}

In the case of interface trapped charge, it is common to express its density in terms of unit area and energy in the

silicon bandgap. Therefore, a special symbol is recommended:

Interface Trap Density D_{it}

The recommended unit for D is number per square centimeter and electron volt. A more complete discussion of the rationale and procedures used in the selection of the terminology may be found in articles by the committee chairman in the April 1980 issue of the *Journal of the Electrochemical Society* and the March 1980 issue of the *IEEE Transactions on Electron Devices*.

Work in Progress . . .

Linewidth Uniformity Measurements - The applicability of multiple cross-bridge resistor (CBR) arrays for measuring linewidth uniformity on patterns with 1.25- μ m feature size is determined by both the precision of the measurement system and the line-edge characteristics. The ratio of the sample standard deviation to the mean for repeated measurements on the same CBR is between 0.5 and 1 percent. For a 6- μ m design linewidth, this corresponds to a measurement precision of 0.03 to 0.06 μ m. The ultimate limitation of the resolution of the CBR arrays will be determined by the control of the line-edge characteristics. Preliminary SEM examination of aluminum CBRs fabricated by conventional chemical etching techniques show that the edge profile is approximately parabolic and has a roughness of the order of the aluminum grain size. [Sponsors: 7,8,9] (D. Yen, x3541)

Band Structure Calculations - Changes in the conduction energy levels and the Fermi energy as functions of temperature and dopant densities are needed in the calculations of diffusion coefficients for process models of devices greater than one micrometer and in calculations of ballistic transport and velocity. Reprinted, with permission, from Standardized Terminology for Oxide Charges Associated With Thermally Oxidized Silicon, by Bruce E. Deal, which appeared in *IEEE Trans. Electron Devices* ED-27, 606-608 (March 1980).

overshoot in submicrometer devices. Using a formalism which approximates the screened coulomb potential by a Bargmann potential, the changes in the Fermi energy and in the first conduction state of silicon were calculated for temperatures from 300 to 1300 K and for donor densities from 10^{19} cm^{-3} to 10^{21} cm^{-3} . The results agree to within experimental error with the bandgap narrowing interpretation of data from silicon devices. They also agree with optical data. Such data for comparison are available at 300 K and for dopant densities of 10^{18} cm^{-3} to 10^{20} cm^{-3} . [Sponsor: 2] (H. S. Bennett, x3625)

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11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here) This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Results of both in-house and contract research are covered. Highlighted activities include: optical linewidth and thermal resistance measurements, device modeling, dopant density profiles, resonance ionization spectroscopy, and deep-level measurements. Brief descriptions of selected on-going projects are included, and recent publications and publications in press are listed. Standardized oxide charge terminology developed by a joint IEEE-ECS committee is also described. The report is not meant to be exhaustive; contacts for obtaining further information are listed.			
12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons) Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.			
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