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THE SMART MIL-STD-1553 BUS ADAPTER HARDWARE MANUAL

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Prepared By

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For

AVIONICS SYSTEMS DIVISION

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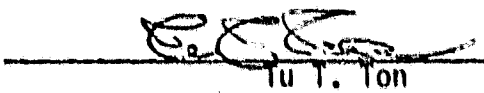
Job Order 34-109

PREPARED BY



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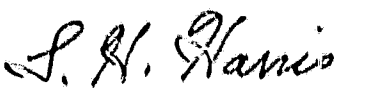

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16. Abstract

The SMART Multiplexer Interface Adapter (SMIA) is a complete system interface for the message structure of the MIL-STD-1553. It was designed to handle all the necessary handshaking to interface between a parallel 8-bit data bus and a MIL-STD-1553 serial bit stream.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
MIL-STD-1553 Bus Controller Remote Terminal Adapter	

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CONTENTS

Section Page

FIGURES

1. DESCRIPTION

The SMART 1553 bus adapter board is a double buffered serial/parallel and parallel/serial converter. It provides all necessary buffering and storage for transmitted and received data. It also provides necessary handshaking, control flags, interrupts to a processor or hard wired logic systems, and the protocol handling for both an MIL-STD-1553 bus controller and remote terminal.

The bus adapter can be configured as either a bus controller or a remote terminal interface. It may be coupled directly to the multiplex bus, or stub coupled through an additional isolation transformer located at the connection point. Fault isolation resistors (direct coupled) provide short circuit protection.

2. FEATURES

- Operates as a (1) Remote Terminal Responding
  (2) Bus Controller Initiating
- Performs parallel to serial conversion when transmitting
- Performs serial to parallel conversion when receiving
- All inputs and outputs are LSTTL compatible
- Supports MIL-STD-1553
- Two complete bus adapters on a single Augat logic board

3. SPECIFICATIONS

Receiver Section:

Input Voltage Level (differential)	40V, P-P (max)
Input Impedance.	>4K ohm differential
Threshold Level.	75OmV P-P nominal

Logic Inputs and Outputs	All logic interface lines operate with low power Schottky TTL loads.

Transmitter Section:

Output Voltage Level (differential)

Transformer Coupled	7.5V P-P differential

Note: When coupled to the data bus with a 1:1 transformer, isolated on the data bus with two 52.5 ohms fault isolation resistors, and loaded by two 70 ohm terminators plus additional receivers.

Stub Coupled.	30V P-P differential (140Ω loads)

3.1 POWER SUPPLY CHARACTERISTICS

(+12V to +15V) ± 2%.	50 MA max (standby) 150 MA (Transmitting)
(-12V to -15V) ± 2%.	35 MA max (standby) 135 MA (Transmitting)
+5V ± 5%	1A

4. INPUT/OUTPUT FUNCTIONS

4.1 FLAGS

4.1.1 "0" MESSAGE FLAG (OMF)

The ZERO MESSAGE FLAG output is set when the 7th through 11th bits of the NRZ serial input data in a command envelope are zero.

4.1.2 "0" WORD FLAG (OWF)

The ZERO WORD FLAG output is set when the 12th through 16th bits of the NRZ serial input data in a command envelope are zero.

4.1.3 INVALID WORD FLAG (IVWF)

The INVALID WORD FLAG output is set when the word just received has an invalid parity bit or invalid format.

4.1.4 POLL COMMAND (POLL CMD)

POLL CMD is set low if the bus adapter receives a valid command transmit word with 0 Message Flag and 0 Word Flag. IA resets POLL CMD.

4.1.5 MESSAGE COMPLETE (MSG CMPLT)

In the receive mode the MESSAGE COMPLETE output is set low when the appropriate number of data words have been received. In the transmit mode, MSG CMPLT indicates that the appropriate number of command, status, or data words have been transmitted. When the COM 1553A is a bus controller, MSG CMPLT will be asserted low when the commanded data words have been transmitted or received.

4.1.6 BROADCAST (BDCST)

BDCST is set low when a "broadcast" command word (the address bits all set to "one") is being received. BDCST is reset by IA.

4.1.7 COMMAND SYNC (CMD SYNC)

Output of a low from this pin occurs during output of data which was preceded by a Command (or Status) synchronizing character.

4.1.8 DATA SYNC (DTA SYNC)

Output of a low from this pin occurs during output of data which was preceded by a Data Synchronizing character.

4.2 HANDSHAKES

4.2.1 DATA REQUEST (DTA RQST)

DATA REQUEST is set high when the transmitter holding register is ready to accept more data.

4.2.2 DATA AVAILABLE (DTA AVL)

DATA AVAILABLE is set when a word received is ready to be read. When the COM 1553A is the bus controller, DTA AVL occurs on command, status, or data words. When the COM 1553A is a remote terminal, DTA AVL is set only on data words.

4.2.3 COMMAND AVAILABLE (CMD AVL)

CMD AVL is set high when a command word received is ready to be read: A high to low transition of $\overline{\text{TX INT}}$ or $\overline{\text{RCV INT}}$ sets it, and it is reset by an RDE pulse or data sync.

4.2.4 $\overline{\text{RECEIVE INTERRUPT}}$ ($\overline{\text{RCV INT}}$)

$\overline{\text{RECEIVE INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a zero and the first 5 bits match AD1-AD5. $\overline{\text{RCV INT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$, or if the line is not active for 32 receive clocks.

4.2.5 $\overline{\text{TRANSMIT INTERRUPT}}$ ($\overline{\text{TX INT}}$)

$\overline{\text{TRANSMIT INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a zero and the first 5 bits match AD1-AD5. $\overline{\text{TX INT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$.

4.2.6 $\overline{\text{READ DATA ENABLE}}$ ($\overline{\text{RDE}}$)

$\overline{\text{RDE}}$ is an input from the system instructing the COM 1553A to place the received data onto D0-D7. Two $\overline{\text{RDE}}$ pulses are required per 16 bit data word - one for each 8 bits.

4.2.7 $\overline{\text{TAKE DATA ENABLE}}$ ($\overline{\text{TDE}}$)

$\overline{\text{TDE}}$ is an input from the system initiating a transmission. Two $\overline{\text{TDE}}$ pulses are required for each 16 bit data word - one for each 8 data bits placed on D0-D7.

4.2.8 $\overline{\text{STATUS WORD ENABLE}}$ ($\overline{\text{SWE}}$)

$\overline{\text{SWE}}$ is the output enable from the subsystem for the following SMIA outputs:

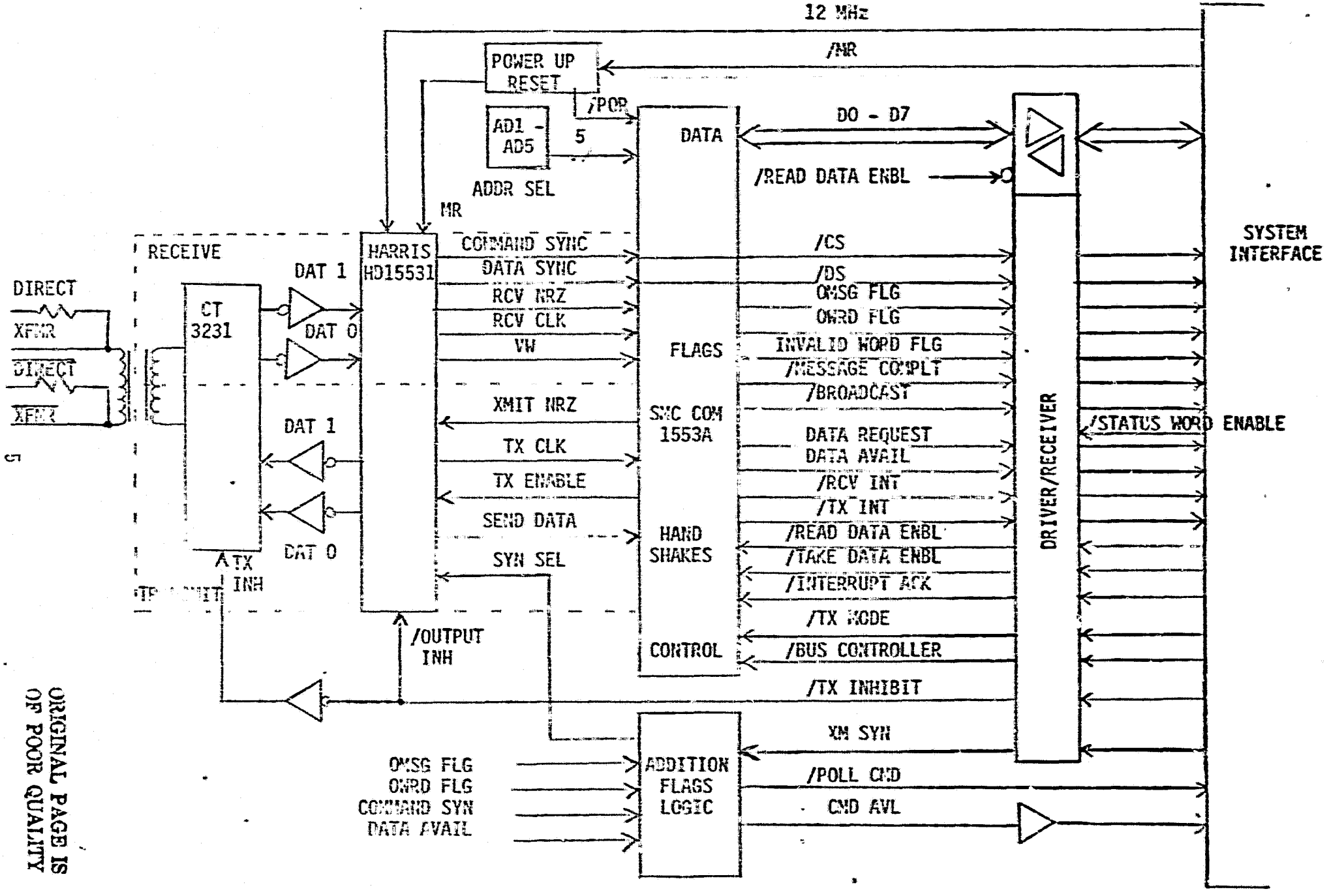


Figure 1 - MIL-STD 1553 Bus Interface Module Block Diagram

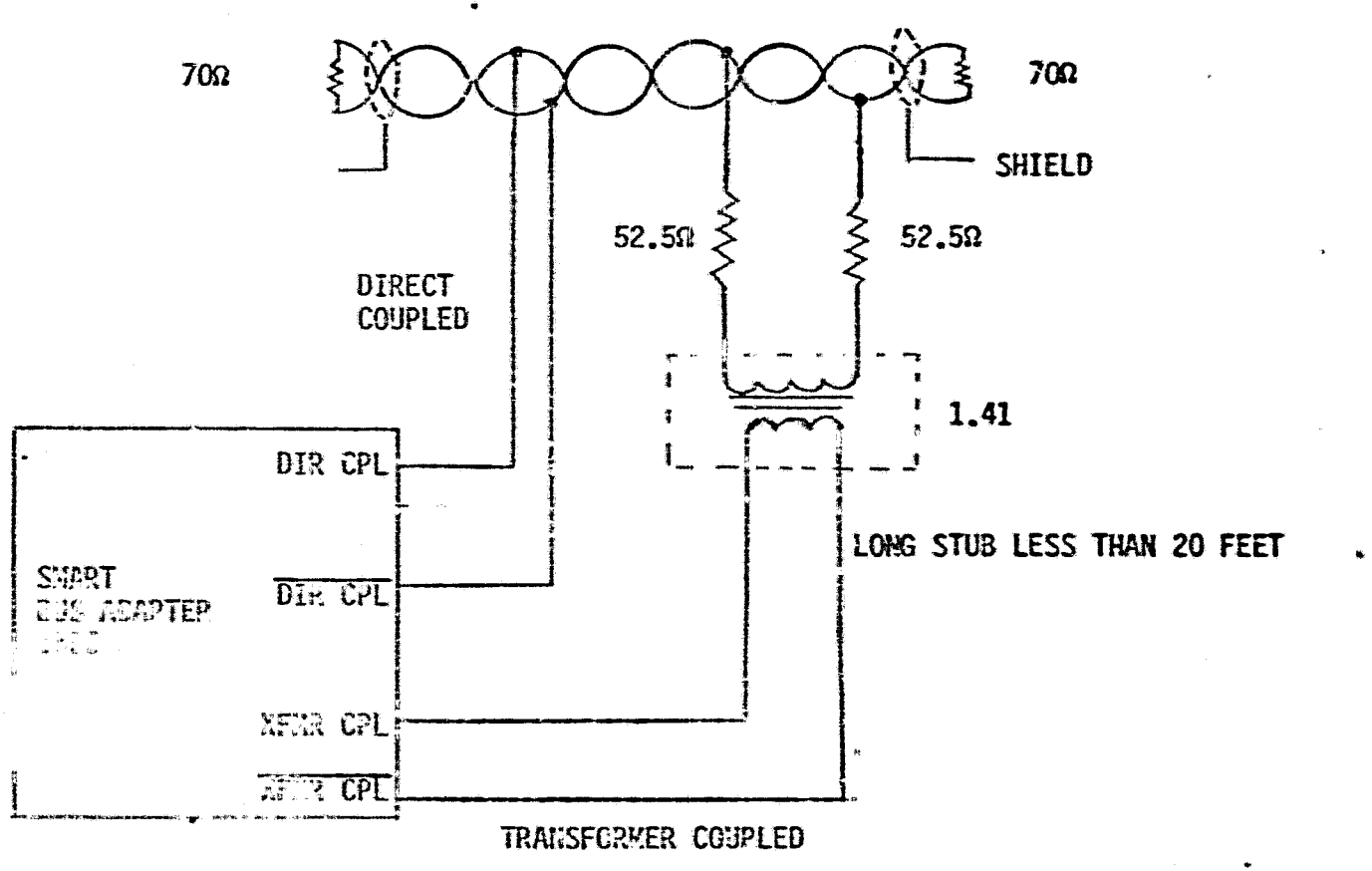


Figure 2 - Typical transformer connections

OMF
OWF
IVWF
DTA AVL
DTA RQ
$\overline{\text{MSG CMPLT}}$

4.2.9 $\overline{\text{INTERRUPT ACKNOWLEDGE}}$ ($\overline{\text{IA}}$)

$\overline{\text{IA}}$ resets $\overline{\text{TX INT}}$, $\overline{\text{REC INT}}$, OMF and $\overline{\text{BDCST}}$. $\overline{\text{IA}}$ may occur between the trailing edges of receive clocks 6 and 10, between the leading edge of receive clock 12 and the falling edge of receive clock 15, or after the falling edge of clock 17.

4.3 CONTROL

4.3.1 TRANSMIT SYNC (XM SYNC)

TRANSMIT SYNC is an input from the interface system to provide the appropriate sync field corresponding to the transmitted word. It generates a command sync for a high input and a data sync for a low input.

4.3.2 $\overline{\text{TRANSMIT MODE}}$ ($\overline{\text{TX MODE}}$)

$\overline{\text{TX MODE}}$ is a system input pulse used to turn the transmitter on or off.

4.3.3 $\overline{\text{BUS CONTROLLER}}$ ($\overline{\text{BC}}$)

$\overline{\text{BC}}$ determines whether the COM 1553A is acting as bus controller ($\overline{\text{BC}}$=0) or as a remote terminal ($\overline{\text{BC}}$=1).

4.3.4 $\overline{\text{MASTER RESET}}$ ($\overline{\text{MR}}$)

A low on this input signal generates a clear signal for the COM 1553A and the Harris HD 15531.

4.3.5 TRANSMITTER INHIBIT (TX INH)

A high true on this input signal inhibits the transmitter (CT 3231) and forces

the encoder outputs to a high inactive state.

4.4 DATA BUS (D0-D7)

This is a bidirectional eight bit data bus to the system. D0 is the LSB. True or complement data output (eight bit bus) is selected by simply using two 74LS245's for true data or two 74LS640's for complementary data.

5. PIN ASSIGNMENTS

AUGAT BOARD CONNECTOR PIN #		FUNCTIONS	INPUT/OUTPUT
CHANNEL 1	CHANNEL 2	(SYMBOL)	
1, 2	62, 63	GND	
60, 61	121, 122	VCC	
8	52	+12VDC	
69	113	-12VDC	
11	50	$\overline{\text{CMD SYNC}}$	Output
12	49	OMF	Output
13	48	OWF	Output
14	47	IVWF	Output
15	46	$\overline{\text{MSG CMPLT}}$	Output
16	45	$\overline{\text{BDCST}}$	Output
17	44	$\overline{\text{POLL CMD}}$	Output
19	42	DTA RQST	Output
20	41	DTA AVL	Output
21	40	$\overline{\text{RCV INT}}$	Output
22	39	$\overline{\text{TX INT}}$	Output
23	38	CMD AVL	Output
24	37	XM SYNC	Input
26→29	35→32	D7-D4	Both
87→90	96→93	D3-D0	Both
72	111	DTA SYNC	Output
73	110	12MHz	Input
75	108	$\overline{\text{RDE}}$	Input

AUGAT BOARD CONNECTOR PIN #		FUNCTIONS	INPUT/OUTPUT
CHANNEL 1	CHANNEL 2	(SYMBOL)	
76	107	$\overline{TDR}$	Input
77	106	$\overline{SWE}$	Input
78	105	$\overline{TA}$	Input
79	104	$\overline{TX\ MODE}$	Input
80	103	$\overline{BC}$	Input
82	101	TX INH	Input
83	100	$\overline{MR}$	Input
4	56	Data Bus H Stub Coupled	
5	55	Shield	
6	54	Data Bus L Stub Coupled	
65	117	Data Bus H Transformer Coupled	
66	116	Shield	
67	115	Data Bus L Transformer Coupled	

6. OPERATION

6.1 RECEIVER OPERATION

The receiver section of the bus adapter is constantly monitoring activity on the MIL-STD-1553 data bus for a valid sync character and two valid Manchester data bits to start an input cycle.

In bus controller mode, the bus adapter monitors all terminal addresses.

In remote terminal mode, only a selected address will be monitored (address switches on the bus adapter matches the first five bits in command word received).

If the address bits compare, the sixth bit is examined. A receive interrupt is generated for a logic zero in bit six; a transmit interrupt is generated if the sixth bit is a one. A zero message flag is generated if bits 7-11 are

all zero. All zeroes in bit field 12-16 denote a zero word flag.

Sixteen bit words, when received, are loaded into the receive buffer and organized into two 8 bit bytes. The most significant byte will be enabled on the I/O data bus with the first RDE pulse. The least significant byte will be enabled with the second RDE pulse.

In the bus controller mode, a data available is generated for command, status, and data words. In remote terminal mode, data available is generated for a data word and command available is generated for a command and/or status word. A message complete is generated when the commanded number of data words has been received.

If a new command sync or data sync has not yet been received within 16 clocks (1MHz) of the fall of the previous sync signal, an idle line condition exists. The idle line condition resets the following signals: $\overline{\text{REC INT}}$, $\overline{\text{TX INT}}$, $\overline{\text{BDCST}}$, "0" MSG FLG, "0" WORD FLAG.

6.2 TRANSMITTER OPERATION

The bus adapter transmits two 8-bit bytes from the subsystem onto the MIL-STD-1553B data bus as one 16-bit word plus sync and parity.

In the bus controller mode, a transmit mode ($\overline{\text{TX MODE}}$) input pulse initiates a transmit cycle, a second $\overline{\text{TX MODE}}$ stops the transmission.

In the remote terminal mode, a transmit cycle is initiated by a system input $\overline{\text{TX MODE}}$ pulse in response to a transmit command received.

The bus adapter sets DATA REQUEST to logic one when it needs more data.

Transmit data is loaded into the transmit buffer by TDE pulses - eight most significant bits by the first TDE pulse, eight least significant bits by the second TDE pulse.

Transmission of the status word from a remote terminal is done automatically. The bus adapter will jam the most significant six bits into the transmit register. The remaining ten bits will be all zero when transmitted. To send additional status information, the ten bits in the status word will be loaded with two TDE pulses. The most significant six bits are non-changeable externally.

The Jam Message Error function (bit six in the status word is a one) occurs when a data word is received and is not followed by a valid word signal.

The Jam function is inhibited when the transmit command word contains "0" message or "0" word, or in the bus controller mode.

A message complete is generated when all data words have been transmitted as commanded.

7. REFERENCES

1. Data Sheet, MIL-STD-1553A "SMART" COM 1553A, Standard Microsystems Corporation
2. Data Sheet, CMOS Manchester Encoder-Decoder, HD-15531, Harris Semiconductor Products Division, July 1978
3. Data Sheet, Low Power Driver/Receiver, CT3231, Circuit Technology Incorporated, October 1979
4. Military Standard 1553B (MIL-STD-1553B), 21 September 1978

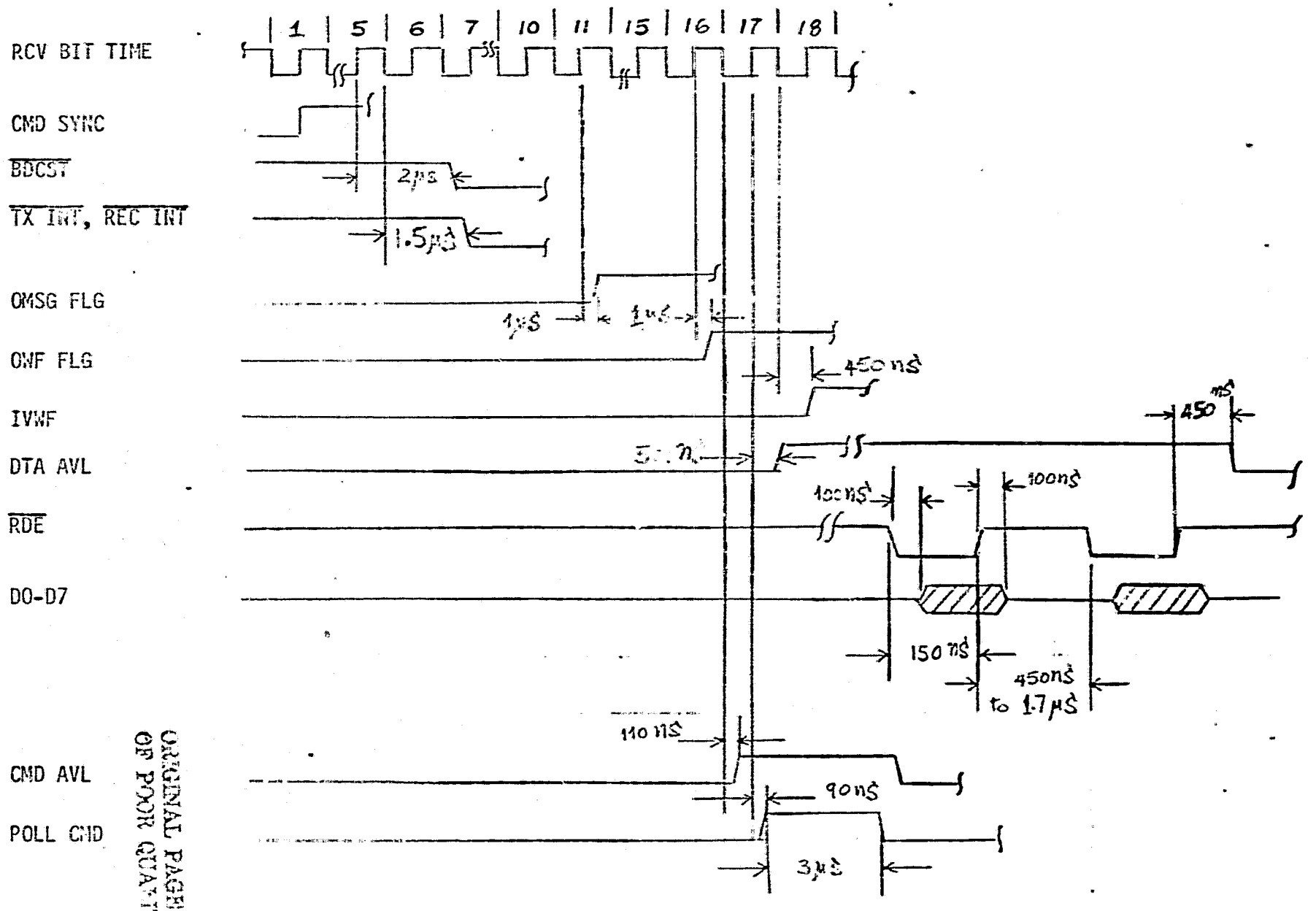
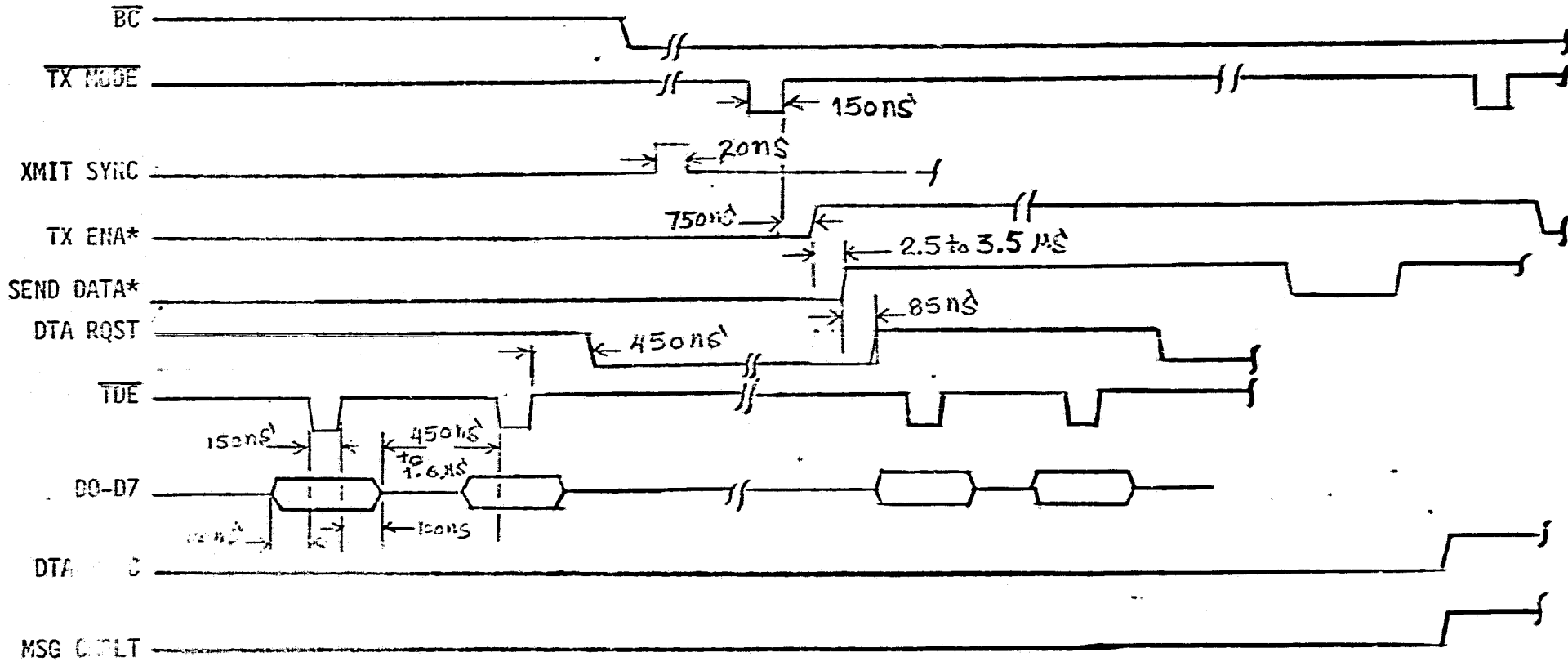


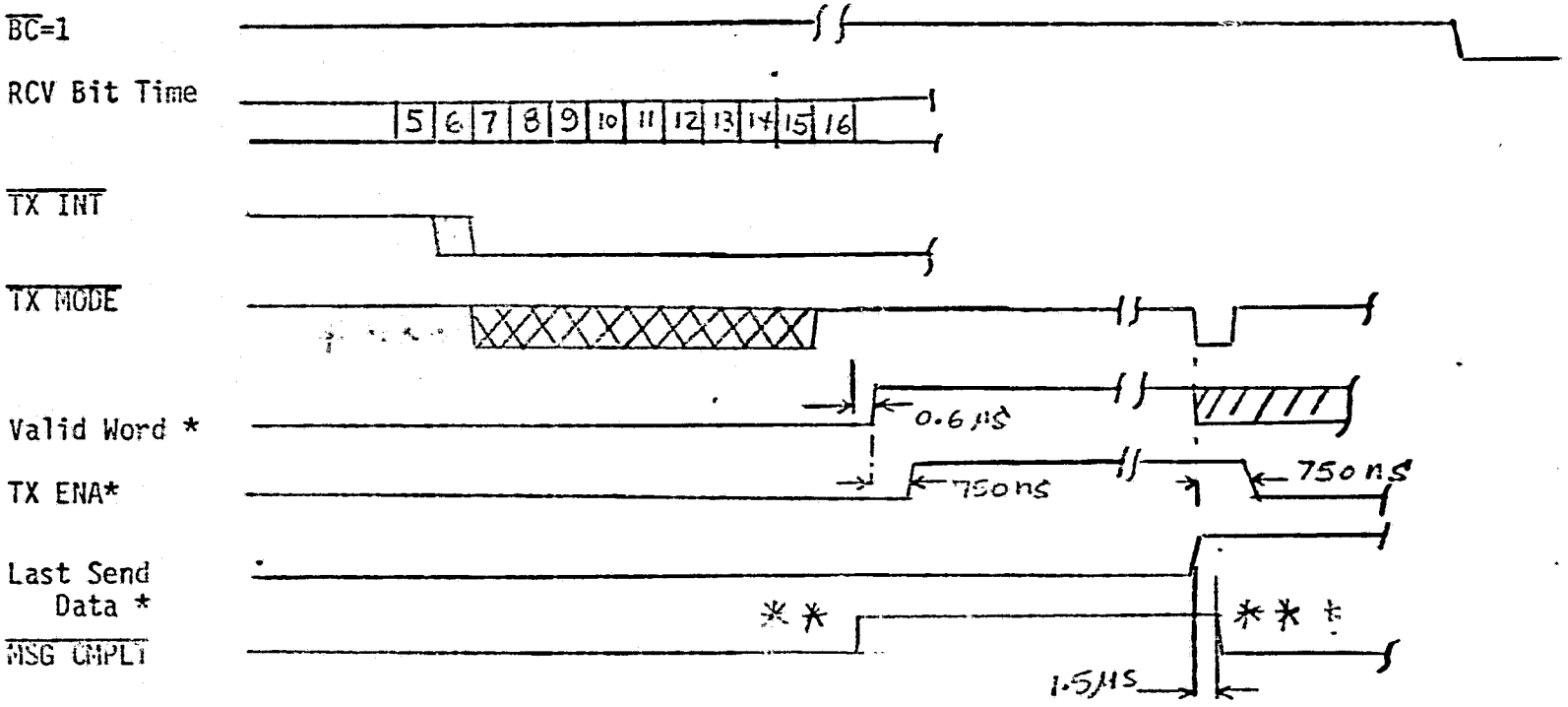
Figure 3 - Receive Timing



*Internal signal - not available to user.

Figure 4 - Subsystem to SMIA Transmit Timing (Bus Controller Mode)

Ex: Bus Controller transmit one command
and one data word.



* Internal signal - not available to user.

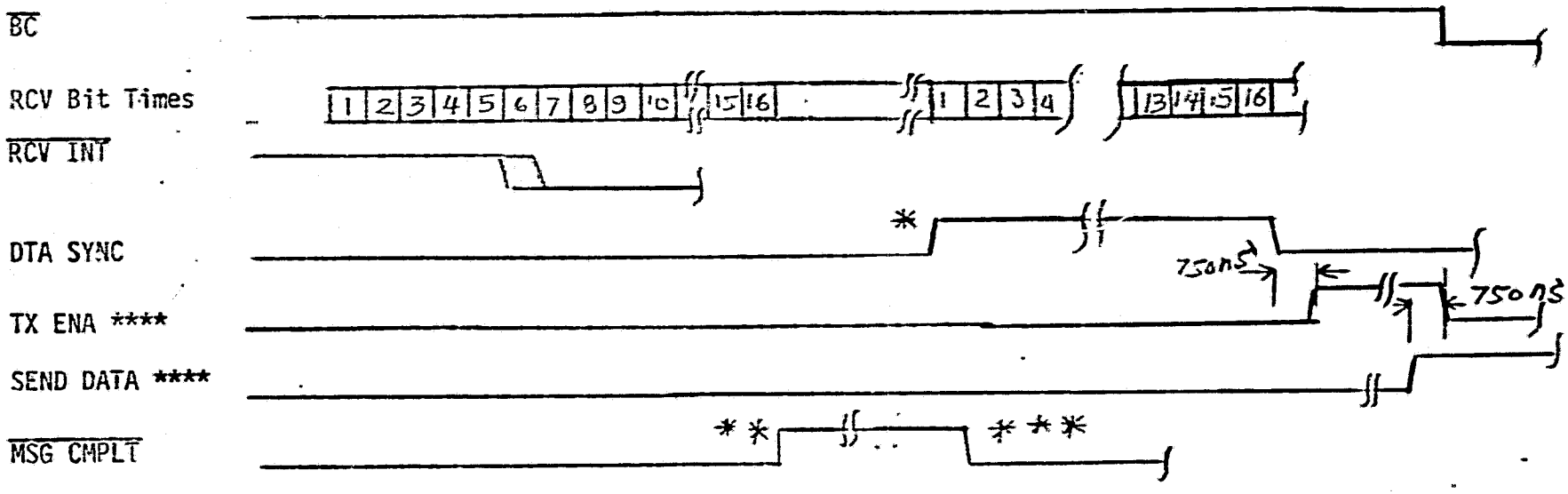
** Word Counter preset to transmit command word field plus one. This allows for the status word.

*** $\overline{\text{MSG CMPLT}}$ generated by the last send data of the transmit message group.

**** $\overline{\text{TX MODE}}$ negative transition will occur in cross hatched area.

Figure 5 - Subsystem to SMIA Transmit Timing (Remote Terminal Mode)

Ex: Remote Terminal receives a transmit command.



* This is the last data word received associated with a previously received command word. During this message sequence, TX ENA is set by MSG CMPLT function and reset by receipt of send data.

** Word Counter preset to count in command word.

*** $\overline{\text{MSG CMPLT}}$ generated by last data sync of the message group.

**** Not available to user.

Figure 6 - Remote terminal timing-Receives a receive command and transmits status word to bus controller.

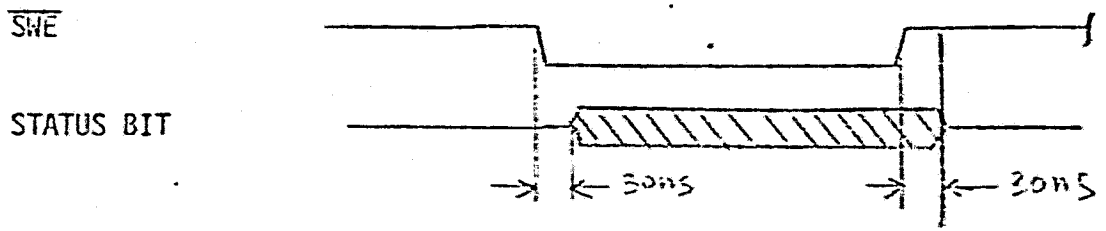
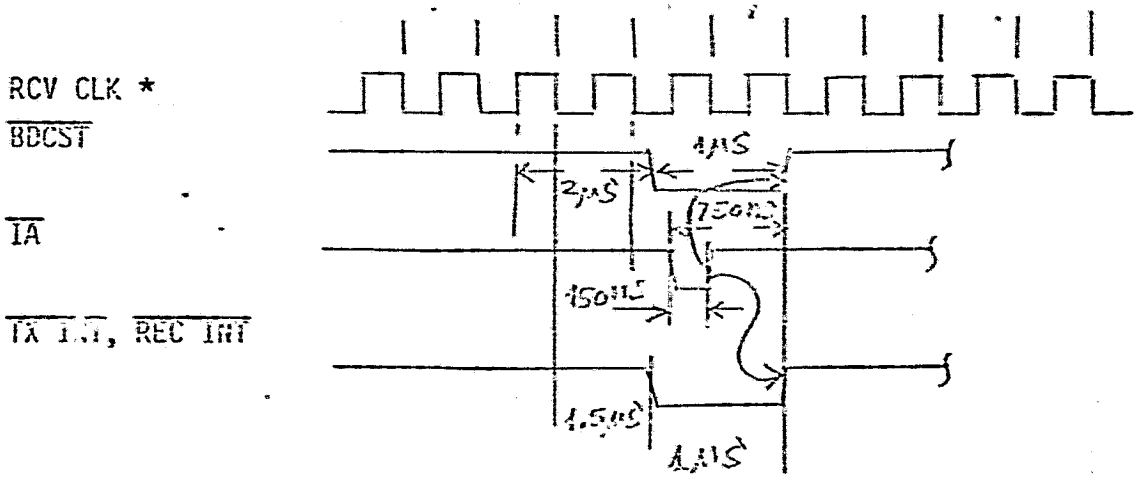


Figure 7 - Status enable timing



* Not available to user.

Figure 8 - BDCST, TX INT, RCV INT reset timing