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Department of Electrical Engineering
Texas A&M University

FINAL REPORT

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X-RAY TOPOGRAPHY STUDY OF COMPLEX SILICON MICROCIRCUITS

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ABSTRACT

This report is a correlation study on the yield of complex silicon microcircuit wafers versus defects observed in x-ray topographs produced by a high speed curved wafer x-ray topographic camera. Most of the topographs were made after final wafer probe. Also included in this report is a description of the new larger version of the camera required to accommodate the larger wafer sizes in current production. Our conclusions are that most high volume silicon wafer processing in todays industry does not need x-ray topography as a routine process control. However in changing any existing process or developing a new process the technique can be of significant benefit. Further the technique may be useful in developing any technology which requires low defect density single crystal material.

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INTRODUCTION

X-ray topography is a method for imaging and identifying defects in nearly perfect crystals. The technique has been used in semiconductor device processing control to some degree for over twenty years. The chief advantage of the method is that it is nondestructive and may be used repeatedly on the same wafer after each of several high temperature processing steps to identify which step is the source of process induced defects which are known to be detrimental to yield and reliability of the products. The chief disadvantage of the method is the expensive equipment and highly trained personnel required combined witn the very low wafer throughput with conventional topographic cameras.

The curved wafer x-ray topographic camera was developed under NASA contract NAS8-26379 to overcome the very low wafer throughput problem. The invention reduces the exposure time required about two orders of magnitude with no sacrifice in image quality. NASA obtained US Patent Number 4,078,175 on the invention in March of 1978. The apparatus was further improved under NASA contract NAS8-32527 including the addition of a live television capability. The primary objective of this contract was to estimate the value of the technique in production process control by correlating crystal defects which may be identified by the method with device yield at final wafer probe.

The Large Wafer X-ray Topographic Camera

The rapid expansion of the wafer sizes used by the semiconductor industry required the construction of a new larger version of the curved wafer x-ray topographic camera. The details of the camera are shown in the first three figures. Although the camera in its present configuration is limited to wafers up to 125 mm it may be extended to 150 mm with a simple modification.

The He filled scatter tube rests on top of the x-ray generator on three leveling screw feet. The vertical slit adjustment is controlled by a single micrometer head. This control limits the vertical divergence of the x-ray beam and is only changed when the wafer size is changed. The television monitor is mounted on a rotating base which allows viewing from this position during the adjustment. The camera itself sits on a separate stand and is loosely coupled to the scatter tube through a rubber boot which decouples the vibration from the rotating anode generator. Each end of the scatter tube is covered by a thin mylar window to seal in the He gas flush. The He gas flush was an improvement added to the smaller camera to minimize air absorption of the copper target characteristic x-ray radiation. This produces higher contrast images in a shorter exposure time. This feature is essential to the operation of the large wafer camera due to the greater length of travel of the x-ray beam. The horizontal divergence of the beam is controlled by an adjustable slit on each side of the scatter tube on the camera stand. The horizontal divergence must be changed each time the wafer size is changed or the particular Bragg diffraction condition is changed. The beam divergence control is necessary to avoid unnecessary air and chuck

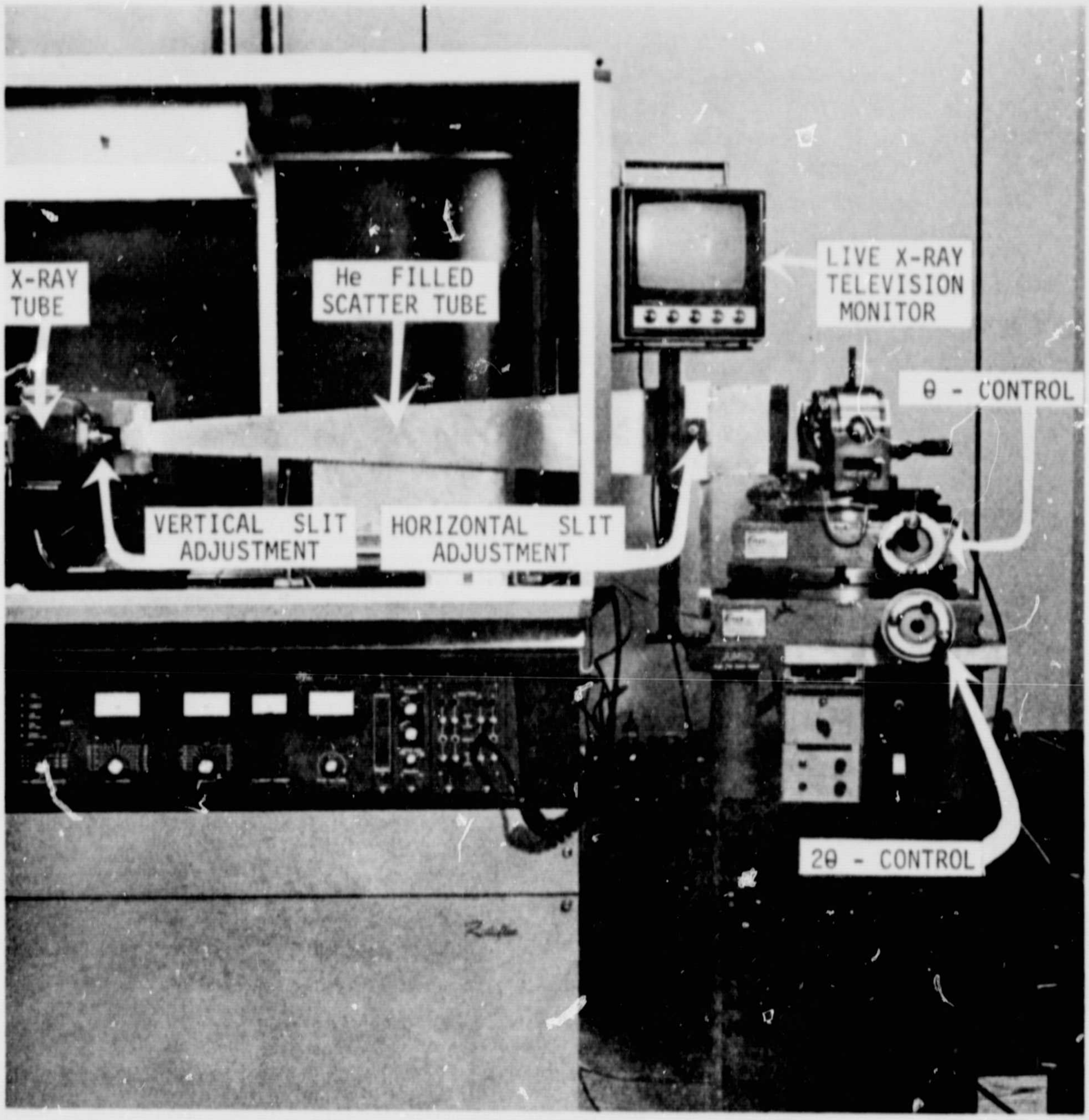

Fig. 1 4 inch wafer x-ray topography system with realtime TV monitoring

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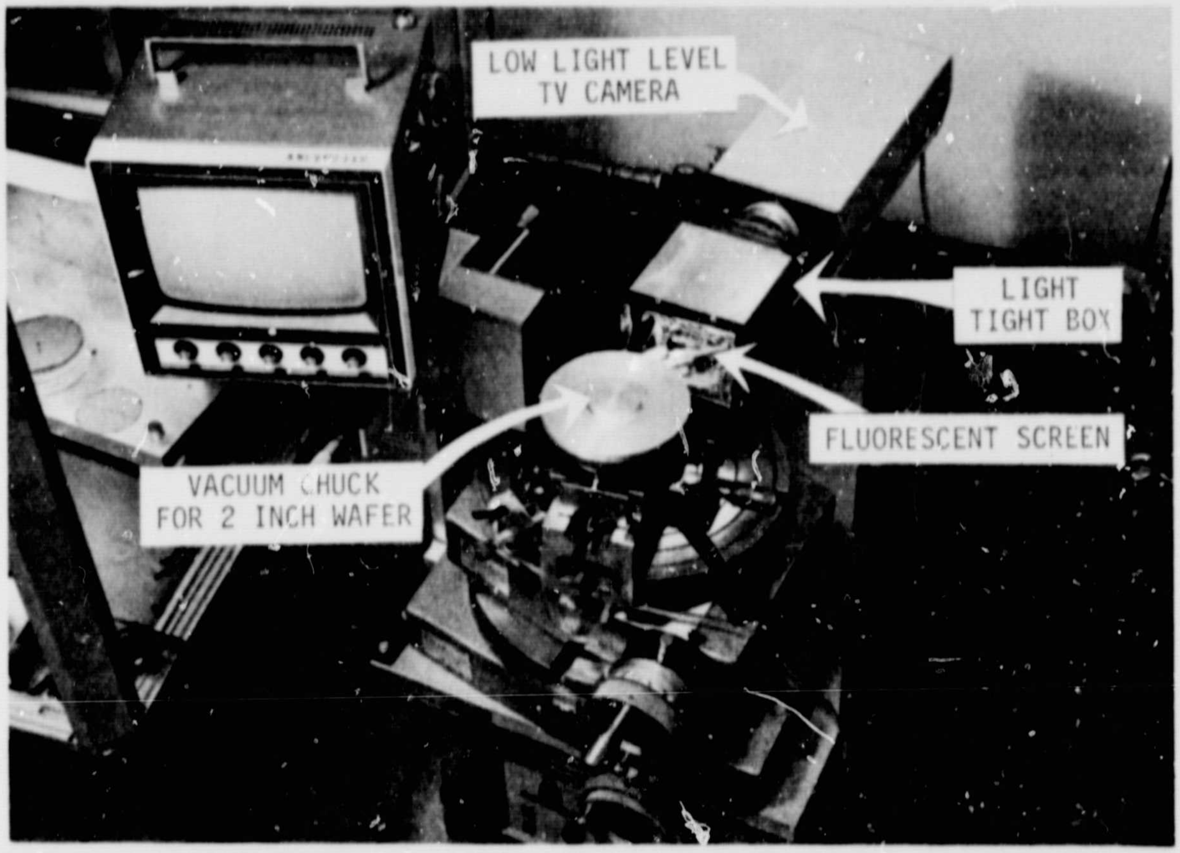

Fig. 2 x-ray topographic camera with 2 inch curved chuck attached. The chuck rotation assembly is tilted to the wafer load position. The θ and 2θ positions are typical of those used in reflection x-ray topography.

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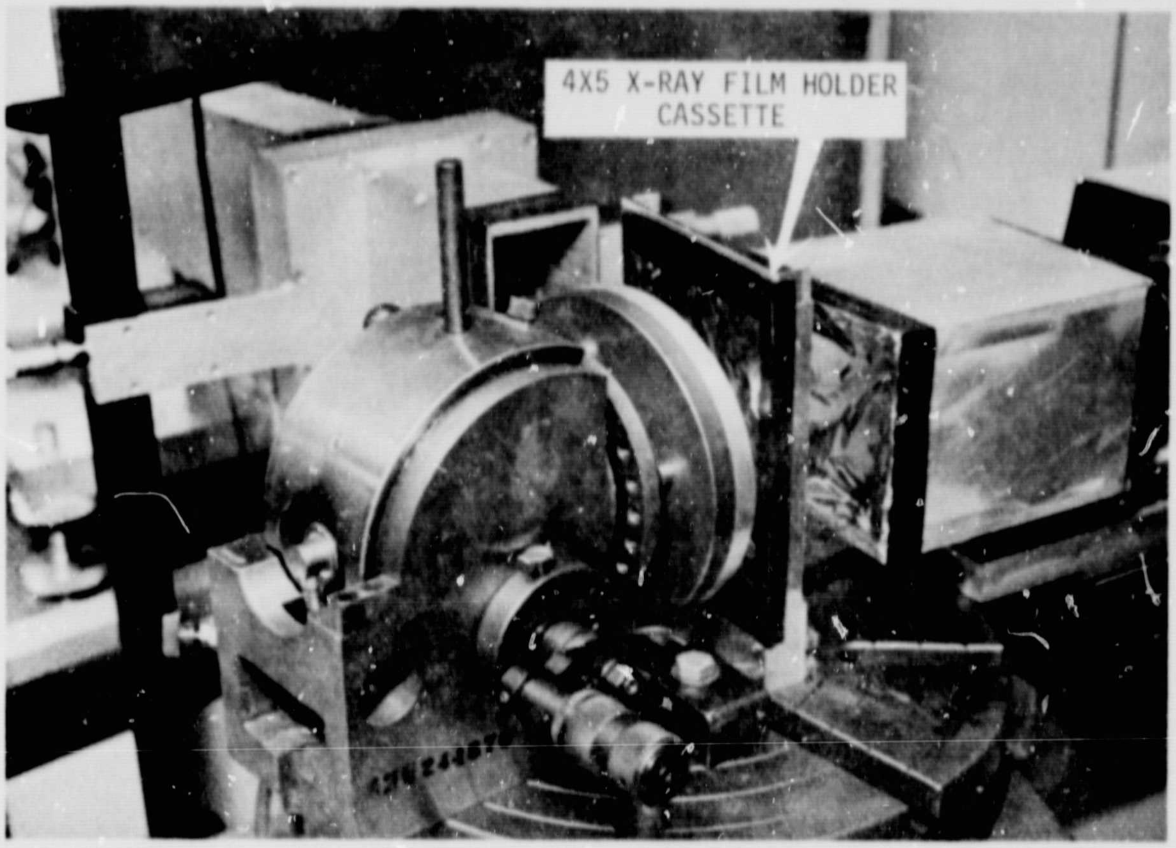

Fig. 3 Close up of the x-ray camera with the chuck rotation assembly tilted to the operating position. The film holder cassette (without a film holder installed) is shown in its normal position for an exposure. The cassette may be placed anywhere on the rotary table and is held firmly by permanent magnets. The rod extending straight up from the assembly is a handle used for tilting the assembly between the load and operate detent positions.

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scattering for safety and image quality reasons. The entire scatter tube is lined with lead and a lead shield (not shown) covers the camera during operation.

All of the critical moving parts of the camera were adapted from standard machine tool equipment. These include a 15" rotary table, a 12" rotary table and a dividing head. These parts are very accurate, rugged, and inexpensive when compared to commercial x-ray equipment. The dividing head can accommodate a variety of interchangeable chucks of different sizes and curvatures. Indeed the dividing head was used to machine the chucks in a milling machine! The dividing head was modified to adapt a vacuum slip ring assembly and spring loaded detents at the horizontal (wafer load) and vertical (operate) positions.

The arm which supports the TV camera contains a motor driven platform which allows the fluorescent screen to be quickly brought in close to the wafer during the initial adjustments and then back out of the way during the film exposure. Placing the screen in exactly the same position that the film will be in during the exposure allows the operator to avoid multiple overlapping images.

The actual exposure is accomplished by placing a light tight aluminum foil covered cassette on the rotary table surface. Standard 4 x 5" film holders are loaded with x-ray film. With two films per holder several consecutive wafers may be topographed followed by batch film processing in the dark room. The film we are now using is Kodak single coated type R. This film offers an excellent compromise between exposure time and resolution and seems to be the only reasonalbe compromise for large wafer topography. Exposure times for this film with the camera in its present configuration vary from 30 minutes to one hour depending on the particular x-ray reflection being used.

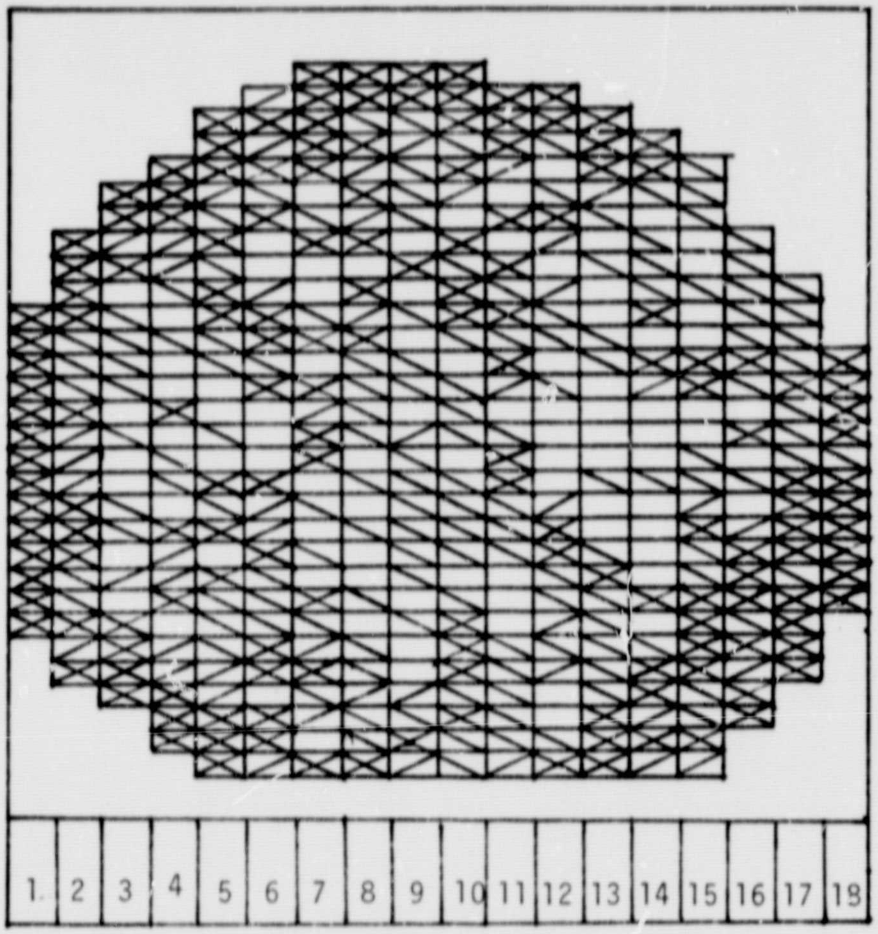
This new version of this camera has proved to be simple and convenient to use and very versatile. The chucks may be quickly interchanged for wafer size or wafer cut [(111) or (100) silicon] or special fixtures may be used for small irregular pieces. In addition to silicon the camera has been used to topograph gallium phosphide, gallium arsenide, lithium gadolinium molybdate, lithium niobate, and other single crystals. The live television capability has greatly simplified the routine operation of the camera. It seems that the only area for improvement in the system would be in attempting to develop a high resolution TV image for true realtime direct wafer inspection.

Defect vs Wafer Probe Correlation

A variety of probed wafers were obtained from three different vendors. These will be denoted by vendor A, vendor B, and vendor C. The yields at final wafer probe could be computed directly for each of the furnished wafers. However the overall batch yields and processing yields are considered proprietary by each vendor and were unavailable. Further the specific processing steps used were unavailable for the same reasons. Most of the circuitry was large scale memories and microprocessor chips using some form of MOS technology.

The wafers supplied by vendor A were all 16K dynamic rams. The starting material is 4 inch p-type silicon and all active devices are n-channel enhancement mode MOSFETs. Poly I is used as one plate of the storage capacitors and gates for some of the FETs. Poly II is used as one of the address lines and for gates for other transistors. Typical yields on these wafers were very high (95% of the probed die were good in one case). X-ray topographs of these wafers were very free of process induced defects. One of the wafers supplied by vendor A, however, has a yield of only about 30% and this is the only wafer they supplied which showed any significant amount of processing damage. We chose this wafer as one of the wafers on which to do a die-to-die correlation. The results are summarized in Table I. Since there are a number of factors which may contribute to a probe test failure other than crystal defects one may be justified in not using the 129 die on this wafer which failed the probe test and did not have visible crystal defects. Using the remaining 297 die for the correlation gives a more realistic value of 85% correlation. In summary the wafer-to-wafer and die-to-die correlation for the wafers from vendor A were excellent.

Table I



Device failed probe test

Defects shown in X-ray topograph

Yield 30.7%

% Correlation 59.2%

defect free circuits which passed probe test 86 (20.2%)

defect free circuits which failed probe test 129 (30.3%)

circuits with defects which passed probe test 45 (10.5%)

circuits with defects which failed probe test 166 (39%)

All of the wafers supplied by vendor B were 3 inch (100) silicon and contained mostly microprocessor circuits. Yields on these wafers were zero or very poor (2 or 3 good die per wafer). The only significant defects seen in the topographs were a few arc like scratches which were probably produced by one of the scrub cleaning steps. The scratches were visible with a light microscope. The very low yield on these wafers is almost certainly due to improper processing or perhaps mask alignment and unrelated to crystal defects. The obvious thing that can be concluded from these results is that their process does not produce any of the familiar process induce slip damage even on the wafer edges. The thermal processing steps for these 3 inch wafers had evolved and been refined to the point that massive process induced dislocations had been eliminated. Further the sampling was biased by the choice of very low yield wafers. In summary one could conclude that x-ray topograph would not be useful in monitoring this particular very mature process.

Vendor C supplied a variety of 2 inch wafers from an older established process and a few 4 inch wafers from the first lot after conversion to the larger wafers. The circuits and process used on both sizes were very similar. Very few process induced defects were noted on the 2 inch wafers and the yields were good. The four inch wafers all had zero yield except one which was chosen for another die-to-die correlation. The topographs of the four inch wafers all showed substantial amounts of process induced defects. Example photographs are included as figures 4 through 8.

The one 4 inch wafer from vendor C with any yield at all is shown in figures 4 and 5. Only 195 die on this wafer had been probed. Several of the rows were skipped during probe to speed up the process but the wafer coverage was good. The results of the die-to-die correlation on this

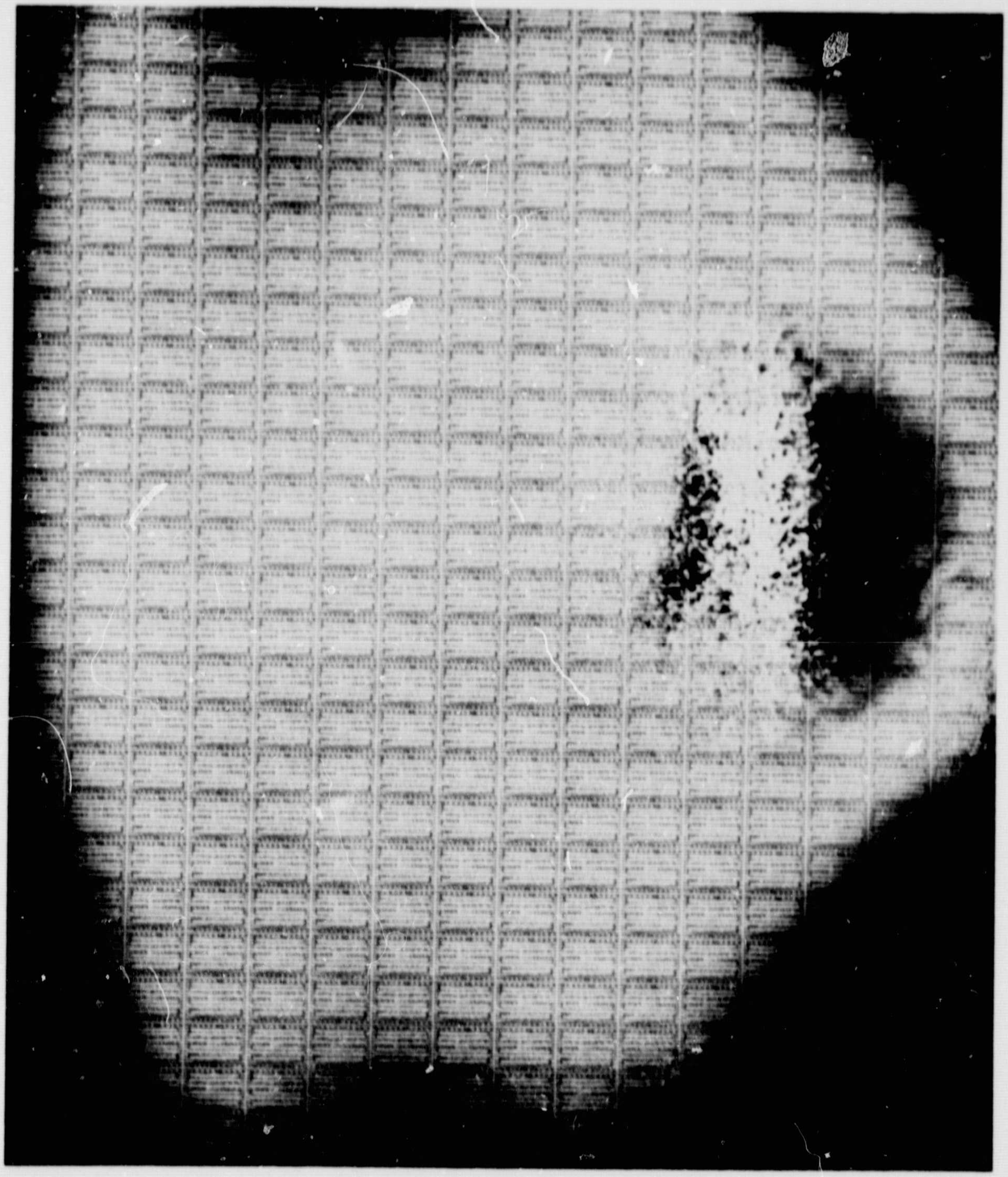


Fig. 4 This is an extreme example of the amount of process induced damage which may be encountered in developing a new process.

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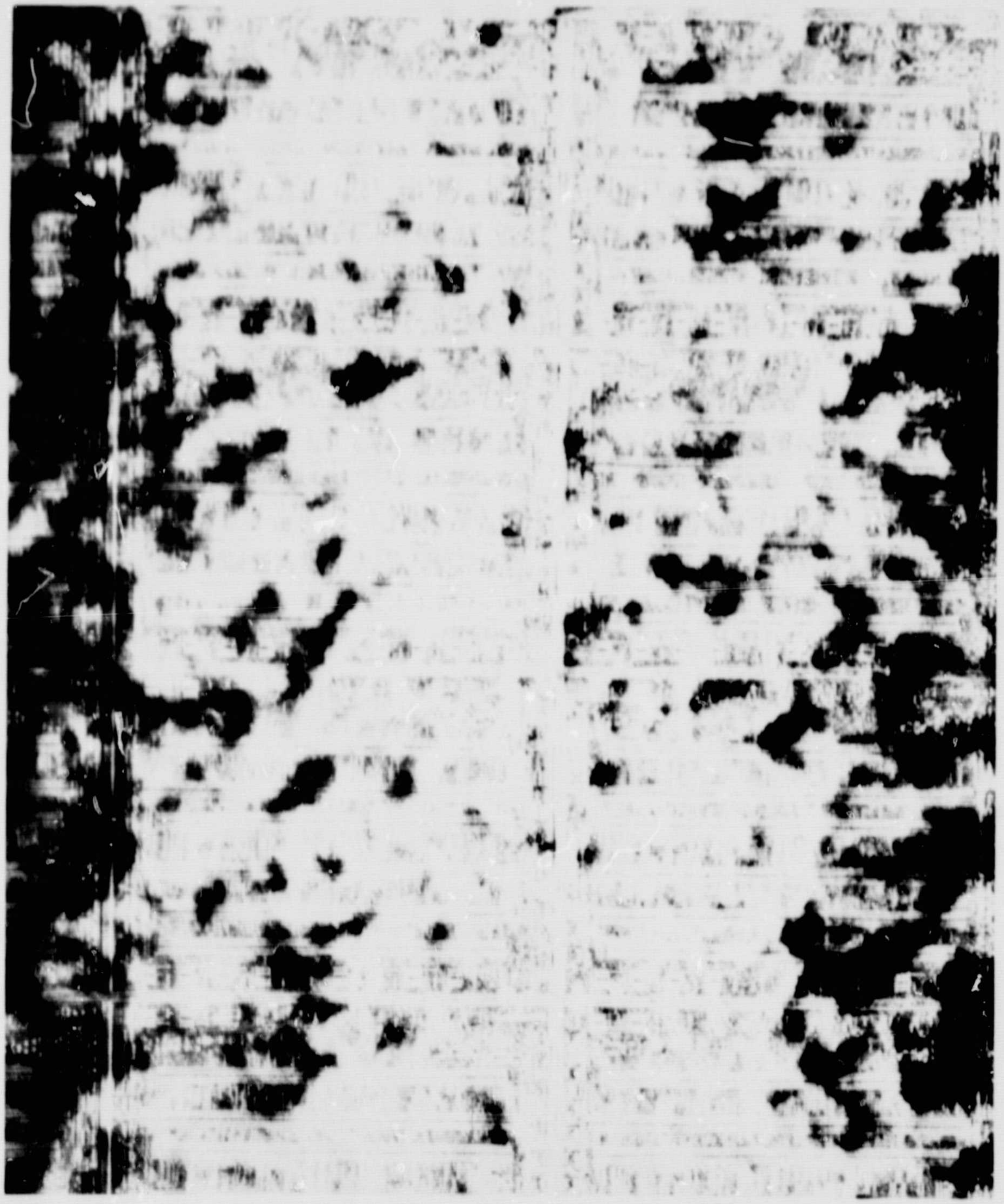

Fig. 5 Microscope photograph of the damage shown in figure 4. This extremely heavy damage is not visable by microscopic inspection of the wafer itself.

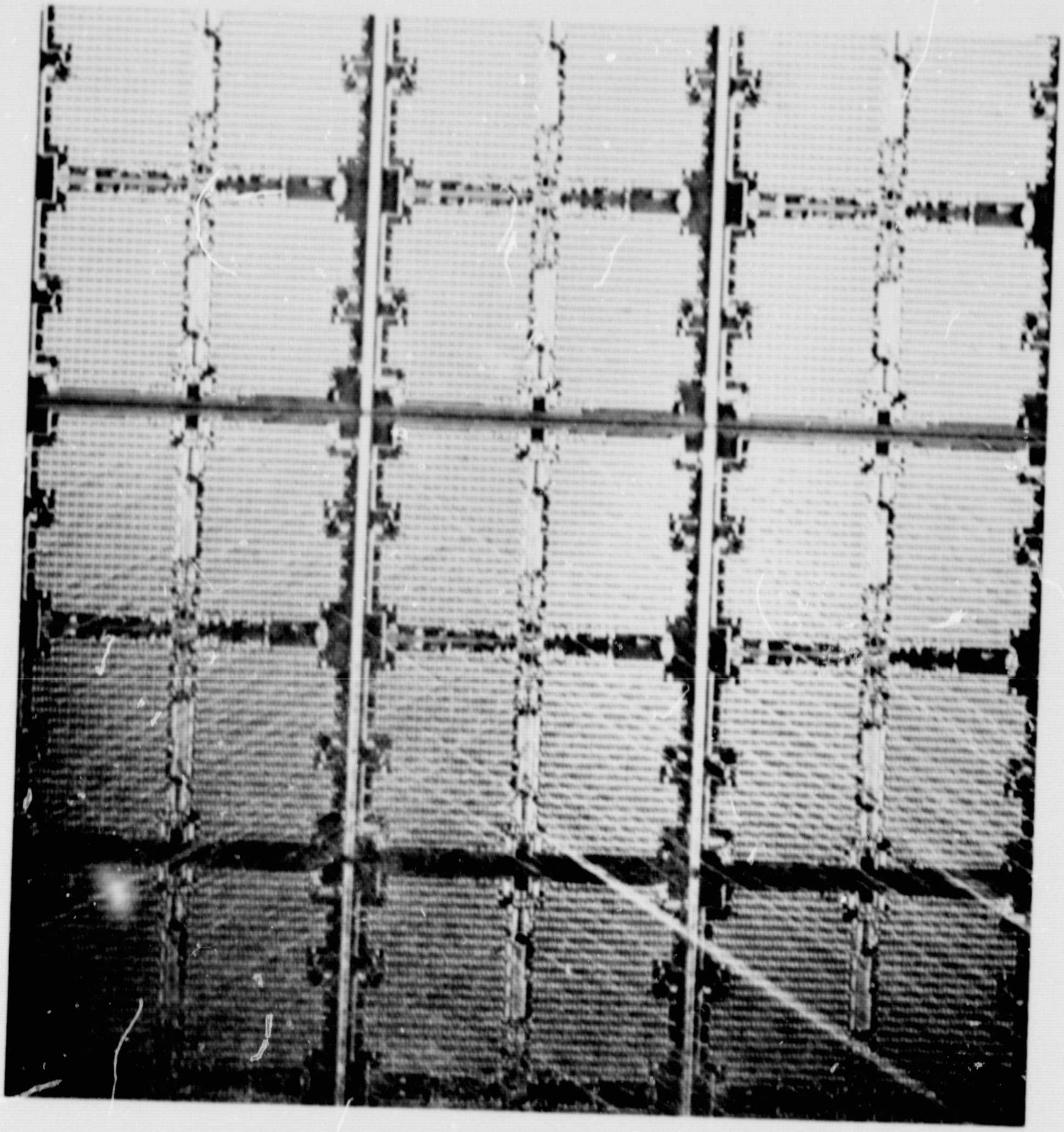

Fig. 6 This is an example of slip damage produced during processing. This damage extends over about 30% of the wafer.

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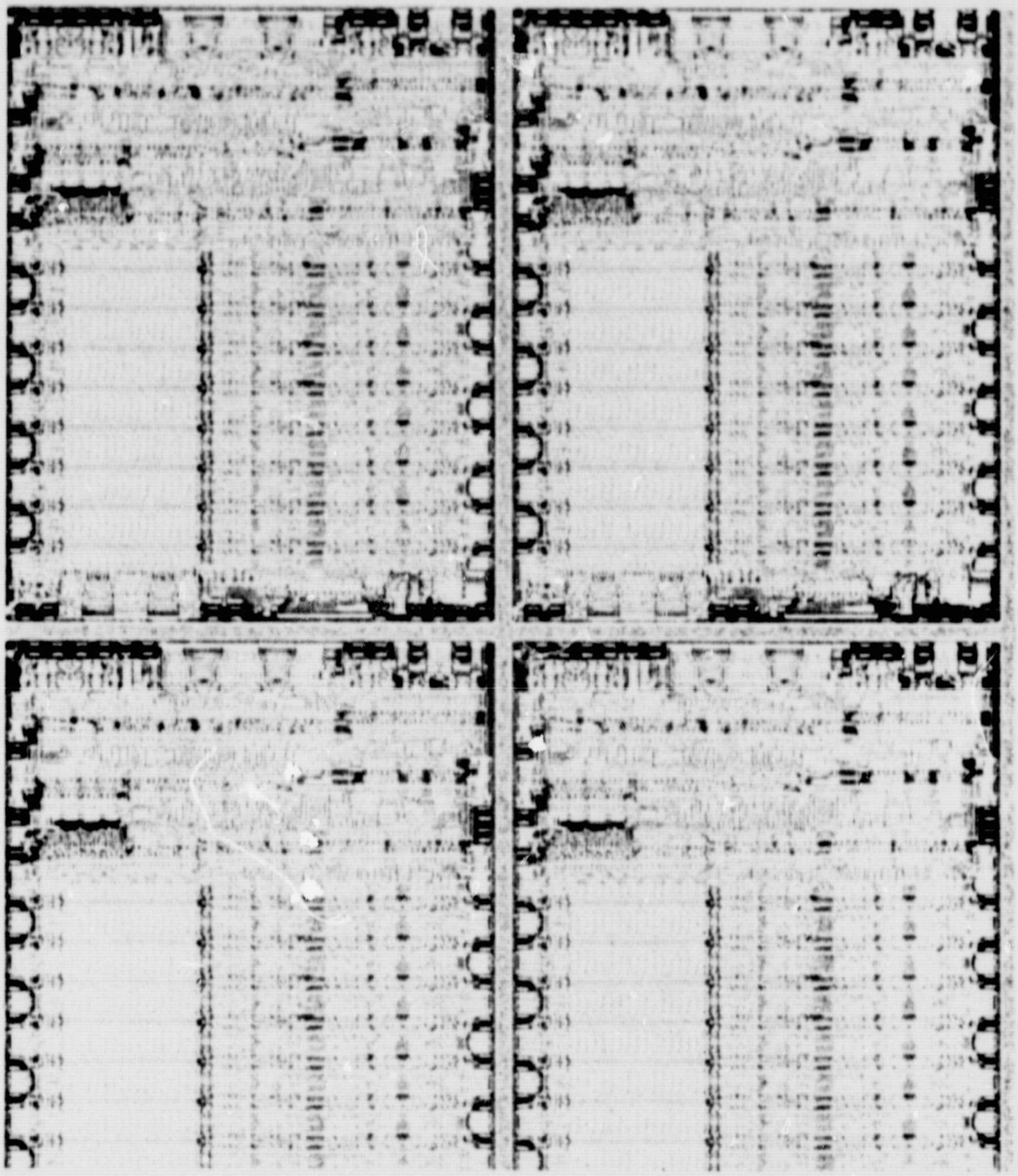

Fig. 7 This is another example of process induced defects. Notice the texture within the scribe lines. This is a zero yield wafer and the damage is present over 100% of the wafer surface.

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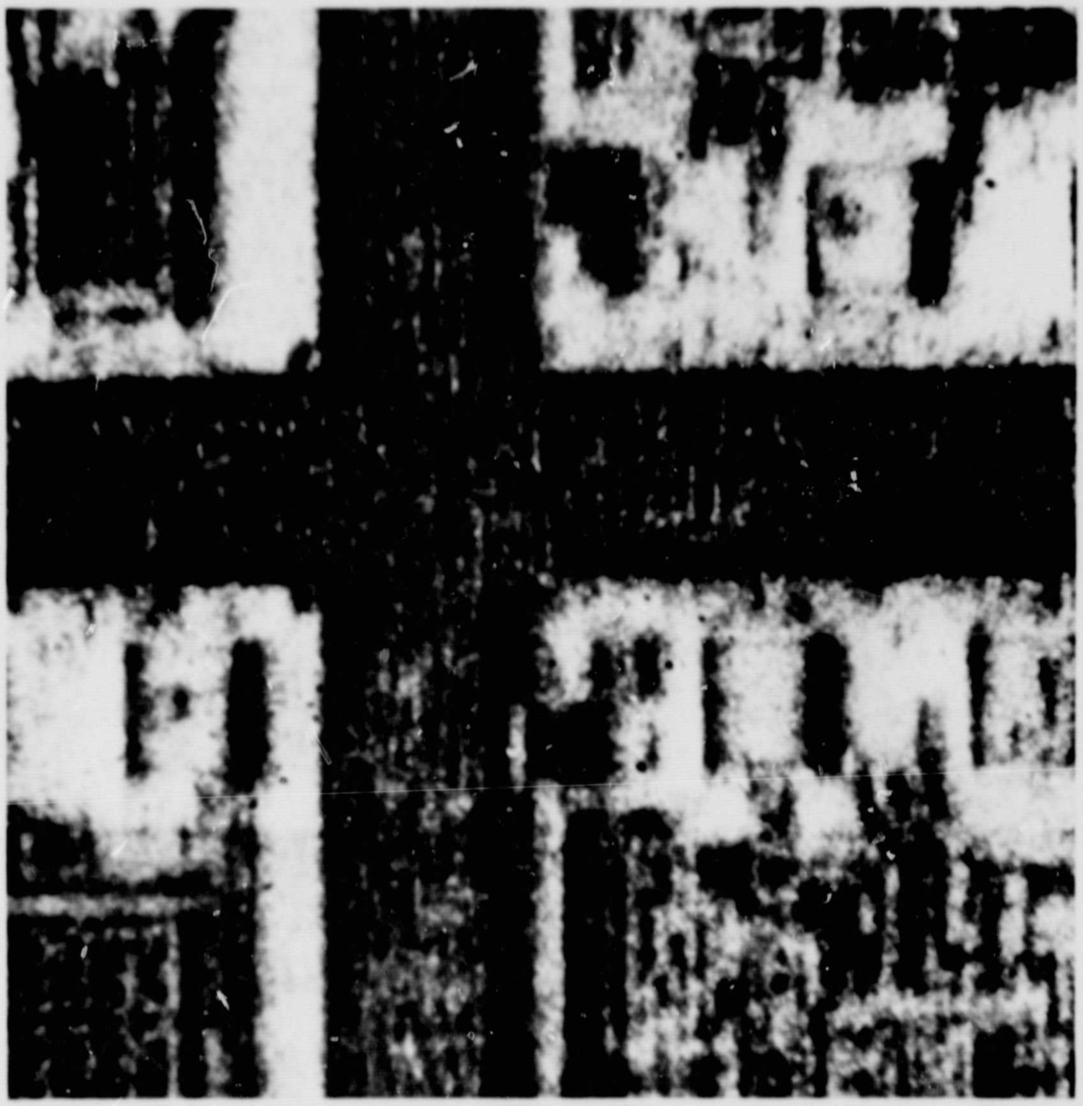

Fig. 8 Microscope photograph of the damage shown in figure 7. The short straight lines are probably stacking faults and extend under the field oxide. This damage is not visible on the wafer itself.

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wafer are given in Table II. The correlation is about 75% on this wafer. One surprising result is that two of the die in the most heavily damaged regions of this wafer passed the probe test.

The die-to-die and wafer-to-wafer correlation of final wafer probe test with defects seen in x-ray topographs of wafers from vendor C must be considered excellent. Further these results indicate the area of silicon processing for which x-ray topography can make a significant contribution: ie. an old process with new equipment and a new wafer size.

Table II

defect free circuits which passed probe test 31 (15.9%)

defect free circuits which failed probe test 17 (9%)

circuits with defects which passed probe test 32 (16.4%)

circuits with defects which failed probe test 115 (59%)

Yield <u>32.3%</u>

Correlation <u>75%</u>

CONCLUSIONS

Even with the development of the high speed curved wafer x-ray topographic camera the method is still relatively slow and expensive compared to all processing steps. Further without some automated pattern recognition equipment the interpretation of the topographs is also slow and expensive. Silicon process control has developed to a state where frequent large amounts of process induced crystal defects are rare. This is particularly true in the large high volume companies. For these reasons it is concluded that routine x-ray inspection of existing successful high yield processes is not cost effective. However, the method may be very useful in monitoring silicon processing in the following cases:

1.) development of a new process or device

2.) a sudden unexplained drop in yields

3.) application of an old process to a larger wafer size

and 4.) prescreening of chips for high reliability application particularly in large scale hybrid circuitry.

Although silicon processing is highly developed today there are many new technologies which are beginning to have substantial commercial and military impact. Among these are:

1.) SAW filter devices

2.) III-V compound semiconductor IC's

3.) bubble memories

4.) thin film transistor circuitry

and 5.) a large variety of electro optic materials.

It is very probable that curved wafer x-ray topography can be of significant aid in bringing these technologies to the same level of maturity as silicon.