RECENT PROGRESS
IN THE
NASA-GODDARD SPACE FLIGHT CENTER
ATOMIC HYDROGEN STANDARDS PROGRAM

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ABSTRACT

At NASA-Goddard Space Flight Center, and through associated contractors, a broad spectrum of work is being carried out to develop improved hydrogen maser frequency standards for field use, improved experimental hydrogen maser frequency standards, and improved frequency and time distribution and measurement systems for hydrogen maser use. The Applied Physics Laboratory of Johns Hopkins University under the technical direction of NASA-Goddard Space Flight Center, has been developing a new generation of field operational hydrogen maser frequency standard called the NASA Research or NR hydrogen maser. Recent data has shown the NR maser to have a frequency stability floor of 1×10^{-15}, a magnetic sensitivity of less than 3×10^{-14} per gauss, a pressure sensitivity of 5×10^{-15} per inch of mercury, and a temperature sensitivity of 4.5×10^{-14} per degree celsius with about a one day time constant. At Goddard Space Flight Center, a new low cost, high performance field operable hydrogen maser is being designed. The new design is presented. Novel and unique features are stressed. At Goddard Space Flight Center, extensive theoretical and experimental work has been performed on the use of digital phase locked loops to average the phases of several atomic standards. More recently, this work is being continued at the Applied Physics Laboratory. A brief presentation of the principles of these loops and recent experimental results on the performance of these loops is given.

INTRODUCTION

At NASA-Goddard Space Flight Center and through associated contractors, a broad spectrum of work is being carried out to develop improved hydrogen maser frequency standards for field use, improved experimental hydrogen maser frequency standards, and improved frequency and time distribution and measurement systems for hydrogen maser use. This paper will report on recent progress in these areas. The paper is broken into three more or less independent sections: recent results on the NR masers being built by the Applied Physics Laboratory (APL) of Johns Hopkins University, the development of a new low cost hydrogen maser at Goddard Space Flight Center (GSFC), and work on a low noise phase comparison system and digitally phase locked crystal oscillator called the Distribution and Measurement System.

NR MASERS

The Applied Physics Laboratory of Johns Hopkins University under the technical direction of NASA-Goddard Space Flight Center, has been developing a new generation of field operational hydrogen maser frequency standards called the NASA Research or NR hydrogen maser. The NR maser is shown in Figure 1. The maser is a completely self-contained field instrument, capable of running off 120 VAC or 28 VDC, and containing its own emergency battery supply capable of running the maser for about 12 hours. The maser also contains a microprocessor based diagnostic and control system which gives diagnostic information on more than 64 monitoring points in the maser and allows maser operation to be controlled remotely. Communication with the maser is via any one of three RS-232 I/O ports. A typical diagnostic output on one of these ports is shown in Figure 2.

The NR maser is designed to be easily field serviceable. It is shown opened for servicing in Figure 3. One servicing feature unique to this design is field serviceable vacuum pumps. There are two 60 l/s Vacion pumps in the unit which can be valved off so they can be replaced without letting the maser up to air. The whole replacement process takes about 2 hours.

The performance parameters of the NR masers measured to date are as follows:

Magnetic Sensitivity

1×10^{-14} to 3×10^{-14}

Pressure Sensitivity

5×10^{-15} per inch of mercury

Temperature Sensitivity

4.5×10^{-14} per degree celsius with about a one day time constant.

Stability

The fractional frequency stability of NR-1 versus NX-2 is shown in Figure 4. The stability statistic is the Allan deviate divided by the square root of 2 to normalize the data to a one maser error. The data shows the stability with and without the NR autotuner on. Notice that, in the NR masers, there is essentially no degradation in short term stability with autotuning.

Figure 5 shows the Allan deviate of NR-1 versus the Jet Propulsion Laboratory's (JPL) DSN-2. The data was taken by JPL. In this plot, the NR-1 vs DSN-2 data is not divided by the square root of two, but the DSN-2 stability is removed with the three corner hat method by using DSN-1 vs DSN-2 data taken simultaneously with the NR-1 vs DSN-2 data.

NEW MASER DEVELOPMENT

At Goddard Space Flight Center, a new low cost, high performance field operable hydrogen maser is being designed. A block diagram of what it will look like is shown in Figure 6. Our goal is to reduce the cost of producing

a hydrogen maser by $100,000.00. We are attempting to achieve this cost reduction by using commercial electronics and packaging in the maser wherever possible.

The maser, hopefully, will also have improved long term stability over previous designs. We hope to achieve this by using the cavity and storage bulb design shown in Figure 7. The basis of the improved long term stability will be the improved mechanical stability achieved by fusing a quartz microwave cavity and quartz storage bulb into one piece. After fusing, the storage bulb will be coated with teflon and the outside of the cavity will be coated with silver or aluminum. The cavity will be coarse tuned by grinding it successively after measuring its frequency in vacuum.

DISTRIBUTION AND MEASUREMENT SYSTEM

At Goddard Space Flight Center, a low noise phase comparison system and frequency distribution system called the Distribution and Measurement System (DMS) is being developed. The purposes of this system are: to inter-compare the phases of 5 MHz supplied by several atomic frequency standards, to digitally phase lock a 5 MHz crystal oscillator to the average phase of these standards, and to distribute this phase locked 5 MHz in a low noise manner.

Figure 8 shows a simplified block diagram of the DMS. A digitally controlled crystal oscillator (DXCO) is used to provide the 5 MHz output of the DMS under normal conditions. A phase comparison system is used to monitor the difference in phase between the 5 MHz output of the DXCO with a resolution of 0.4 ps. This information is used by an LSI-11 microprocessor to phase lock the DXCO to the average phase of the atomic standards. In this phase lock mode, the frequency of the DXCO can be arbitrarily offset with respect to the average frequency of the atomic standards with a range of $\pm 1 \times 10^{-7}$ (fractional frequency). This effectively turns the DXCO into a low noise synthesizer.

In practice, the frequency resolution of this synthesizer is virtually infinite. The processor controls the DXCO frequency with a resolution of 8×10^{-13} per bit. But the phase lock loop allows the processor to change the frequency of the DXCO ten times a second so that the loop can adjust the phase of the DXCO in 0.08 ps steps. The 0.4 ps phase comparison system resolution is larger than this by a factor of 5, and so is the real limiting factor in the phase tracking loop. The system, thus, has a frequency tracking resolution of:

$$\frac{\delta f}{f} = \frac{0.4 \text{ ps}}{t}$$

where t is the averaging time in seconds.

The frequency offsetability of the phase lock loop is used to keep the DXCO output on time with UTC (Universal Coordinated Time) regardless of the frequencies of the input standards. An event clock monitors the difference in time between the local timing system 1pps output driven by the DMS and UTC information provided via LORAN-C or some other time source. The proper frequency offset to keep this time difference zero is maintained either manually or in a secondary loop.

The DMS also performs error detection and monitoring functions. The health of the input standards, the DXCO, and other system elements are constantly monitored. If a standard fails, it is thrown out of the phase lock loop. Errors that will cause loop failure, including processor failure, cause the 5 MHZ output to be switched from the DXCO to the first standard. A teletype and digitally controlled multichannel strip chart recorder constantly provides hard copy documentation of system operation. This information can also be sent to remote locations via several RS-232 interfaces in the DMS.

Control of the DMS is accomplished locally through the teletype and can be accomplished from remote locations via the RS-232 interfaces.

HARDWARE DESCRIPTION

A more detailed block diagram of the FCS is shown in Figure 9. The system contains the following hardware which performs the functions listed:

A. Offset Crystal Oscillator (LO): Provides 4.999990 MHz to the Buffer/Mixer Section.

B. Buffer/Mixers (B/M): Uses the 4.999990 MHz from the LO to down convert the 5 MHz inputs to 10 Hz beats. In the buffer/mixers, zero crossing detectors turn the low level signals from the mixers into TTL square waves.

C. Multichannel Event Clock (CL): Records the epoch of the 10 Hz beats and 1 pps inputs to 200 ns. Because the B/M conserves phase angles in down converting the 5 MHz inputs to 10 Hz, the CL effectively measures the phases of the 5 MHz inputs relative to the LO with 0.4 ps resolution. When the processor takes the difference in epoch between any two 10 Hz channels, the phase of the LO is subtracted out.

D. Interpolator (INT): Used in conjunction with CL to measure the epoch of the 1 pps inputs to 10 ns. Used to keep the timing system 1 pps on time with respect to UTC.

E. Digitally Controlled Crystal Oscillator (DXCO): Provides the main 5 MHz output in normal operation. The output frequency is controlled by the processor with better than part in ten to the twelfth resolution.

F. RF Switch (SW): Switches the main output to the 5 MHz input designated CS1 when the processor fails to send a check pulse once every 120 ms or when the DXCO output fails.

G. RF Filter (FL): Removes glitches when SW switches the main output.

H. Strip Chart Recorder (REC): A 16-channel, digitally controlled strip chart recorder which is used to provide a visual record of the phase and 1 pps data.

I. RS232 Interfaces (RS232): 4 RS232 interfaces are provided to interface to the teletype and remote devices.

J. Teletype (TTY): Controls and communicates with the microprocessor and provides an alphanumeric record of phase and 1 pps data.

K. Microprocessor (UP): An LSI-11 microprocessor is used to perform system control functions.

L. Buffer Amplifiers and X2 Multiplier: Provides 6-5 MHz and 2-10 MHz outputs for the main output.

M. Multichannel A/D Converter (A/D): Monitors voltages in the atomic standards for error detection.

N. TOC Output (TOC): Provides a pulse output and a 1 second TTL gate controlled by UP for providing a TOC pulse for setting up the timing system.

O. CAMAC: CAMAC is an IEEE digital instrumentation standard used to house the digital portion of the DMS (CAMAC Crate), provide a data bus for communication between the UP and most digital subsystems (CAMAC data-way), and the module structure for digital subsystems (CAMAC modules).

Phase Comparison System

Before describing the theory of the phase comparison system, it is helpful to review some pertinent frequency standard theory. The output of a frequency standard can be described by:

$$V = A \sin [2\pi f_0 + \phi(t)] \tag{1}$$

where f is its nominal or ideal frequency and $\phi(t)$ describes all the phase deviations from ideal behavior. One can show that if this signal source is used to drive a counter used as a clock, that at any instant, the error in this clock's reading is given by:

$$x(t) = \frac{\phi(t)}{2\pi f_0} \tag{2}$$

x is called the normalized phase error or clock reading error. For simplicity, in this document, x will be called the phase or phase error.

By taking the time derivative of ϕ, one obtains the instantaneous angular frequency offset from $2\pi f_0$:

$$\frac{d\phi}{dt} \equiv \dot{\phi} = 2\pi \delta f(t).$$

Dividing this by $2\pi f_0$ yields the instantaneous fractional frequency error:

$$y = \frac{\delta f}{f_0} = \frac{\dot{\phi}}{2\pi f_0} = \frac{dx}{dt} = \dot{x}. \tag{3}$$

That is, the instantaneous fractional frequency offset, y, is the time derivative of the clock error, x. Averaging y over some time τ :

$$\bar{y}(t + \tau, t) = \frac{1}{\tau} \int_t^{t+\tau} y(t')dt', \tag{4}$$

yields the important relation:

$$\bar{y}\ (t + \tau,\ t) = \frac{x(t+\tau) - x(t)}{\tau}\ . \tag{5}$$

Now, within this framework, the phase comparison system can be described.

The phase comparison system is a generalization of the dual mixer phase comparison technique.[1] To understand the detailed operation of the phase comparison system, consider an input on channel i of the form:

$$V_i = A_i \sin (2\pi f_0 t + \phi_i(t)),$$

and a signal from the local oscillator of the form:

$$V_L = A_L \sin (2 f_0 t + \phi_L(t)),$$

where f_0 = 5 MHz. Notice that all the phase deviations in these signals from that of an ideal 5 MHz oscillator have been put into ϕ_i and ϕ_L respectively (included in ϕ_L is the 10 Hz offset from 5 MHz). The mixer for channel i outputs the beat frequency between the local oscillator and the channel i input. Since the local oscillator is lower in frequency than all the channel i inputs, the ith mixer output is of the form:

$$V_M = A_M \; g(\phi_L (t) - \phi_i (t)),$$

where g is some sine-like function whose only important properties for this discussion are that:

$$g (m\pi) = 0,$$

and that the slope of g is positive for:

$$\phi_L - \phi_i = 2m\pi .$$

Zero crossing detectors in the buffer/mixers turn the function, g, into a square wave whose positive edge occurs at:

$$\phi_L (t_{ni}) - \phi_i (t_{ni}) = 2n\pi,$$

where the phases ϕ_L and ϕ_t have been defined to make $\phi_L - \phi_i$ zero at the time (epoch) of the first positive edge under consideration, t_{0i}. Using (2), this becomes:

$$x_L\,(t_{ni}) - x_i\,(t_{ni}) = \frac{n}{f_0}$$

Taking the difference between two channels, gives:

$$x_i\,(t_{ni}) - x_j\,(t_{mj}) = x_L\,(t_{ni}) - x_L\,(t_{mj}) - \frac{n-m}{f_0}$$

Using (5), for $\bar{y}_L$ and $\bar{y}_j$, the fractional frequency offset of the LO and

CSj respectively, this becomes:

$$x_i\,(t_{ni}) - x_j\,(t_{ni}) + \frac{n-m}{f_0} = \tag{6}$$

$$[\bar{y}_L\,(t_{ni}, t_{mj}) - \bar{y}_j\,(t_{ni}, t_{mj})]\,(t_{ni} - t_{mj}).$$

This is the equation we are after since it relates the phase difference between two inputs to the t_{ni} which are measured by the multichannel event clock.

To use (6), $\bar{y}_L$ and $\bar{y}_j$ must be known. In practice, some estimates of $\bar{y}_L$ and $\bar{y}_j$ are used. The error this will introduce is:

$$\delta x = \delta \bar{y}\,(t_{ni} - t_{mj}).$$

Typically $t_{ni} - t_{mj} \leq 100$ ms. If $\bar{y}$ is measured to 10^{-12}, δx will be less than 10^{-13} s. So, in practice, since the LO is a low noise crystal oscillator whose stability from 1 s to 100 s is 1×10^{-12}, one can use any input whose accuracy is 10^{-12} to estimate $\bar{y}$ and one can take up to 100 s or so to make the measurement and have an accuracy of 10^{-13} s for differential phase measurements. Since the noise floor of the LO is 10^{-12}, this also means that the system noise is 10^{-13} s or better if limited by the LO.

If the multichannel event clock has a resolution, R, the smallest phase change that can be measured is:

$$\delta x \simeq \bar{y}_L \, R$$

For $\bar{y}_L = 2 \times 10^{-6}$ (10 Hz offset), and $R = 2 \times 10^{-7}$s, $\delta x = 0.4$ ps.

Digital Phase Lock Loop

Consider first, locking the DXCO to a single reference input. Let y be the fractional frequency output of the DXCO. If the digital control has a sensitivity of S ($\delta f/f$ per bit) and the control register value is Y:

$$y = S \, Y + y_f,$$

where y_f describes the free running behavior of the DXCO. Let x_{ni} be the phase difference between the DXCO and the reference oscillator:

$$x_{ni} = x_0 \, (t_{n0}) - x_i \, (t_{ni}).$$

Using (6):

$$x_{ni} = R \, (T_{n0} - T_{ni})(\bar{y}_L - \bar{y}_i),$$

where channel 0 is the DXCO channel, R is the resolution of the event clock, and T_{ni} is the time of the n^{th} beat zero crossing for channel i in bits. Since we are locking on only one reference, we can assume it is on frequency, that is, $\bar{y}_i = 0$.

A first order phase lock loop is given by the equation:

$$Y_n = - \, (B/S) \, x_{ni},$$

which for times long compared with the best period, τ_0, is equivalent to:

$$\frac{dx}{dt} = - Bx + y_f.$$

This has the solution:

$$x = x_0 e^{-Bt} + y_f/B,$$

where B^{-1} is the time constant of the phase lock loop.

Because the DXCO is less noisy than a cesium frequency standard up to about a 100 s averaging time, B^{-1} should be about 100 s for use with cesium standards. This causes problems, however, due to y_f. The DXCO has a rated frequency drift of less than 10^{-10} per day or:

$$\frac{dy_f}{dt} \simeq 10^{-15}\ s^{-1}$$

Since this is a slow drift:

$$\frac{dx}{dt} \simeq B^{-1}\frac{dy_f}{dt}$$

$$\frac{dx}{dt} \simeq 10^{-13}$$

Thus, this drift rate in the free running DXCO would cause a frequency offset of 10^{-13} in the phase locked DXCO, an unacceptable error.

To overcome this problem, a second order loop is used. The DXCO register is incremented at each beat period, τ_0, by:

$$\Delta Y_n = - (B/S)\Delta x_{ni} - (C\tau_0/S)\ x_{ni},$$

where Δa_n is defined as:

$$\Delta a_n \equiv a_n - a_{n-1}.$$

This is equivalent to:

$$\frac{\Delta Y_n}{\tau_0} = -(B/S)\ \frac{\Delta x_{ni}}{\tau_0} - (C/S)\ x_{ni},$$

or for times long compared to τ_0:

$$\frac{d^2x}{dt^2} = -B\frac{dx}{dt} - Cx + D,$$

where D is the drift rate of the DXCO. This equation, in general, has the solution

$$x(t) = \frac{1}{\sqrt{B^2-4C}}\left[(\dot{x}(0) + r_1x(0))e^{-r_1t} + \dot{x}(0)+r_2x(0))e^{-r_2t}\right] + \frac{D}{C}, \qquad (7a)$$

where

$$r_1 = B/2 + \frac{1}{2}\sqrt{B^2 - 4C},$$

$$r_2 = B/2 - \frac{1}{2}\sqrt{B^2 - 4C},$$

and $x(0)$ and $\dot{x}(0)$ are the phase and frequency at $t = 0$, respectively. For the phase lock loop to be stable.

$$B^2 \geq 4C.$$

At $B^2 = 4C$, we have critical damping, in which case the solution is:

$$x(t) = t\ (\dot{x}(0) + r_c x(0))e^{-r_c t} + x(0)e^{-r_c t} + \frac{D}{C} \qquad (7b)$$

where

$$r_c = B/2 \text{ and } C = \frac{B^2}{4}.$$

In this case, a frequency drift will only produce a phase offset:

$$x = D/C$$

For critical damping, $r_c^{-1} = 100$ s, and $D = 10^{-10}$/day, $x = 10$ ps. This is below the phase jitter of the average phase of even 10 cesium standards, and so, should not cause problems even if there are daily changes in the drift rate of the DXCO when used with cesium standards.

Consider, now a second order phase lock loop tracking the DXCO to the average phase of several atomic standards (CS_i) offset by an adjustable fractional frequency offset, y_0. Again, the phase difference between the DXCO and CS_i is:

$$x_{ni} = R(T_{n0} - T_{ni})(\bar{y}_L - \bar{y}_i)$$

where again R is the resolution of the clock, and T_{ni} is the i^{th} channel beat zero crossing epoch. But in a practical phase lock loop, a problem in computing x_{ni} occurs. Since the frequency of the DXCO is not the same as that of CS_i, even if $y_0 = 0$, $T_{n0} - T_{ni}$ will diverge in time.

This means that an infinite memory would be required to store all the values of T_{ni} required to compute $T_{n0} - T_{ni}$ at any given instant. To avoid this problem, using (6) again, we can rewrite x_{ni} as:

$$x_{ni} = R\,(T_{n0} - T_{mi})(\bar{y}_L - \bar{y}_i) - \frac{n - m}{f_0}. \qquad (8)$$

This allows us to use the closest T_{mi} to T_{n0} and not have to store past values. From (8), we can obtain the difference between the DXCO phase and the average phase of N cesiums.

$$x_n = \frac{1}{N} \sum_{i=1}^{N} \left[R(T_{no} - T_{mi})(\bar{y}_L - \bar{y}_i) - \frac{n - m(i)}{f_0}\right] \qquad (9)$$

where the fact that m is a function of i is explicitly indicated.

To lock the DXCO to the average phase of the cesiums with a fractional frequency offset y_0, we can define a variable:

$$X_n = y_0 (T_{n0} - T_{00}) - \frac{x_n}{R}$$

where the units of X_n are in bits. Using (9) and the fact that the event clock is driven by 5 MHz from the DXCO, so that when the DXCO is locked:

$$R = \frac{1}{f_0},$$

we obtain:

$$X_n = \frac{1}{N} \sum_{i=1}^{N} [(T_{mi} - T_{n0})(\bar{y}_L - \bar{y}_i) + J_{ni}] \qquad (10)$$

$$+ y_0 (T_{n0} - T_{00}),$$

where

$$J_{ni} = n - m(i).$$

With this variable, a second order loop is defined by:

$$\Delta Y_n = \left(\frac{B}{Sf_0}\right) \Delta X_n + \left(\frac{C\tau_0}{Sf_0}\right) X_n, \qquad (11)$$

where, again, ΔY_n is the amount the DXCO control register is incremented. In practice, ΔY_n should be limited to:

$$-L \leq \Delta Y_n \leq L,$$

in order to keep the Y register from being changed drastically by a bad data point.

Because the CS_i have different frequencies, the J_{ni} and $y_0 (T_{n0} - T_{00})$ will be unbounded as n goes to infinity. This will cause computational problems. But the other terms in X_n are bounded and X_n itself is bounded because of the phase lock loop. Therefore:

$$K_n = \frac{1}{N} \sum_{i=1}^{N} J_{ni} + y_0 (T_{n0} - T_{00}),$$

is bounded as n goes to infinity. So to avoid computational problems, (10) can be rewritten as:

$$X_n = \frac{1}{N} \sum_{i=1}^{N} (T_{mi} - T_{n0})(\bar{y}_L - \bar{y}_i) + K_n, \qquad (10a)$$

where K_n is computed incrementally by computing:

$$\Delta K_n = \frac{1}{N} \sum_{i=1}^{N} \Delta J_{ni} + y_0 \ \Delta T_{n0}. \qquad (12)$$

The ΔJ_{ni} can be computed by two methods. The simplest method is to use the definition of the J_{ni} and increment ΔJ_{ni} for each DXCO zero crossing and decrement ΔJ_{ni} for each CS_i zero crossing. The disadvantages of this is that should a noise pulse cause a false T_{ni} or should a zero crossing be skipped, the DXCO will shift in phase by 200 ns/N.

To avoid such permanent phase shifts in the DXCO, another method for calculating the ΔJ_{ni} can be used. With the convention that T_{mi} is the first channel i event after T_{n0} occurs:

$$D\ T_{ni} = T_{mi} - T_{n0}$$

will range between zero and approximately τ_0. If the $\bar{y}_i$ and y_0 are not too large, DT_{ni} will change slowly with n until 0 or τ_0 is reached. Then, the value of DT_{ni} will suddenly change. Thus, to compute ΔJ_{ni}, one can use the algorithm:

If: $\quad D\ T_{ni} - D\ T_{n-1,i} > \frac{\tau_0}{2R}$

then: $\quad \Delta J_{ni} = -1.$

If: $D T_{ni} - D T_{n-1}, i < -\frac{\tau_0}{2R}$,

then: $\Delta J_{ni} = +1$.

Otherwise: $\Delta J_{ni} = 0$.

The advantage of this method is that if there is a bad J_{ni} or a skipped zero crossing, ΔJ_{ni} will switch between +1 and -1 or vice versa on successive calculations leaving no permanent phase shift.

$\bar{y}_L$ and the $\bar{y}_i$ can be calculated from the event clock data. Once the DXCO is locked, it defines local time, and by definition is at frequency f_0. Therefore, $\bar{y}_L$ and the $\bar{y}_i$ can be estimated by:

$$\bar{y}_{nL} = \frac{\bar{f}_{nL} - f_0}{f_0} = \frac{m}{T_{n+m,\,0} - T_{n\,0}}, \tag{13}$$

and

$$\bar{y}_{nL} - \bar{y}_{ni} = \frac{\bar{f}_{nL} - \bar{f}_{ni}}{f_0} = \frac{m}{T_{n+m,i} - T_{ni}}. \tag{14}$$

Because the LO is a free running crystal oscillator, $\bar{y}_L$ must be constantly updated to correct for crystal drift. Since only $\bar{y}_L - \bar{y}_i$ must be known, to calculate X_n, (14) is all that is needed for loop operation. To make the estimate error on the order of 10^{-12} or less, but often enough to correct for LO changes, m should be about 1000 (100 second averages). (13) is used to determine $\bar{y}_i$ from (14) for diagnostic purposes.

DMS Performance

The performance of the phase comparison system and the 5 MHz distribution amplifiers used in the DMS have been presented elsewhere[2] so this data will not be presented here. Figures 10, 11, and 12 show the critically damped second order phase lock loop performance for 1 s, 10 s, 100 s time

constants respectively using two Hewlett Packard high performance cesium frequency standards as input standards. Besides showing the parameters discussed in the previous sections, the figures also show the 1 pps from one of the cesiums monitored by the clock. This shows whether the loop jumps cycles of 5 MHz. In the figures, X_e is X_n and VXCO is Y_n from the theory section. In the boxes are listed the top of scale (TOF) and bottom of scale (BOF) values for each variable. Notice that in the 10 s loop there is brunching of the VXCO (Y variable) noise distribution and that in the 100 s loop there is a sudden jump in X_e accompanied by a jump in VXCO representing about a 4×10^{-12} jump in the DXCO crystal. (Notice also that in the 100 s loop the 1 pps did not jump. This shows that the loop does not jump cycles even under a severe disturbance.) We think both of these phenomena are due to vibration of the AT cut crystals used in the DXCO (FTS-1000) by fans in the rack holding the DMS. Currently we are trying to cure this problem by vibrationally isolating the DXCO.

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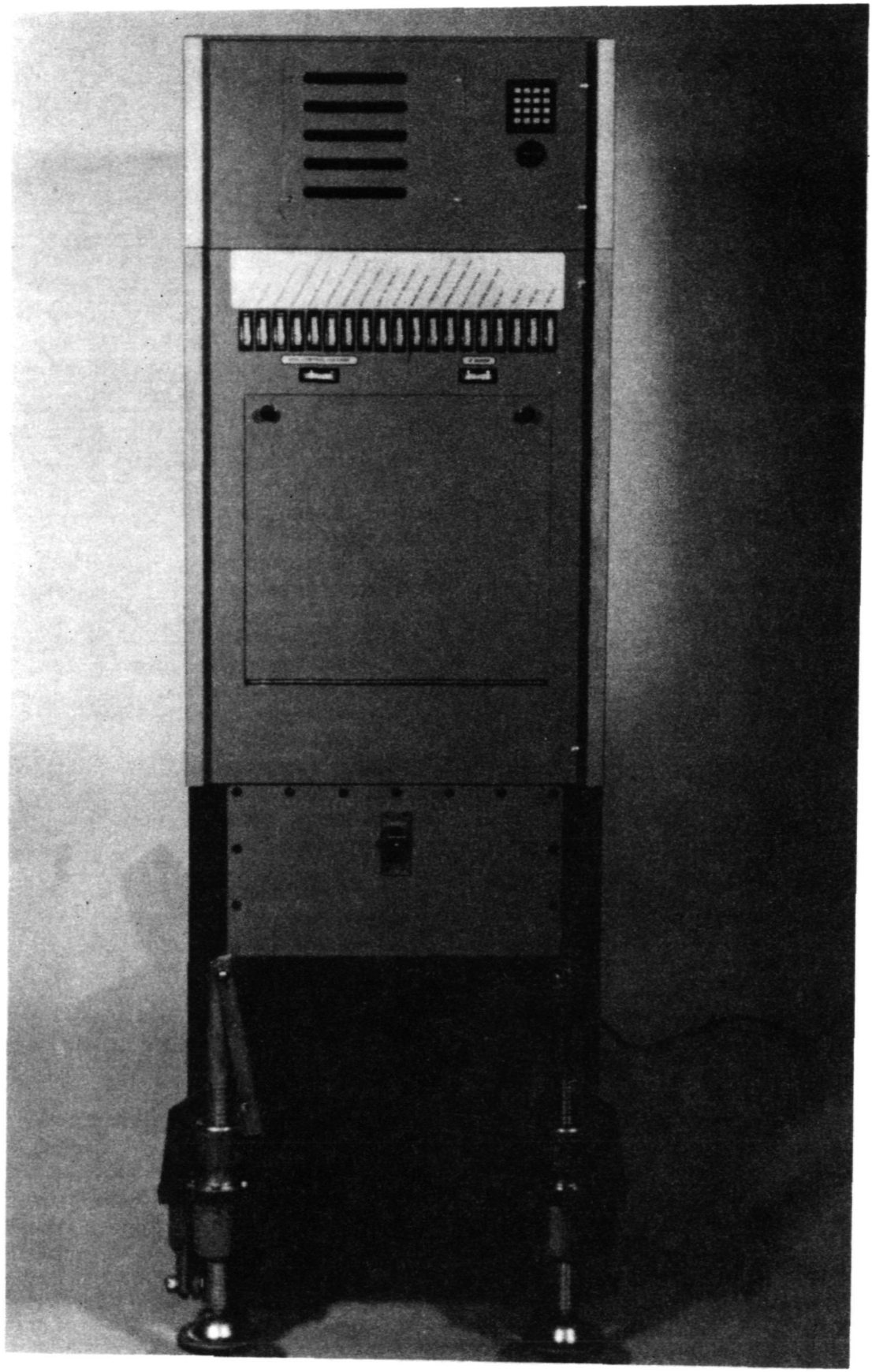

Figure 1. NR Maser

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MASER 04 80 239 19 41 33 FH   M-001600L025065  11 14 113740 SYN M 0588 1224 858
015  0050 DGSW 100111101011 DACWDS 50 08 65 12  010204 020110 031105

1 VOLTAGES V   28.029  17.329  05.044  17.344   03.640  14.010  20.665  01.941
2 BUFFERS  V   00.161  00.166  00.083  00.148   00.569  00.528  00.577  00.215
3 MULT SEN V   00.019  00.427  00.344  00.119   00.440  00.225  00.143  09.627
4 CURRENTS A   05.843  00.210  00.042  00.021   00.477  00.004  00.007  00.007
5 HEATERS  A   00.552  00.878  00.351  00.066   00.083  00.062  00.217  00.220
6 CONTROL MA   00.038  00.004  00.019  00.000   00.000  00.000  00.225  00.005
7 MISC         02.583  02.307 115.248  00.222   00.217  00.489  03.187  07.507
8 THERM.   C   47.438  35.500  46.563  29.062   29.688  34.000  72.313  71.939
```

Figure 2. Microprocessor Output

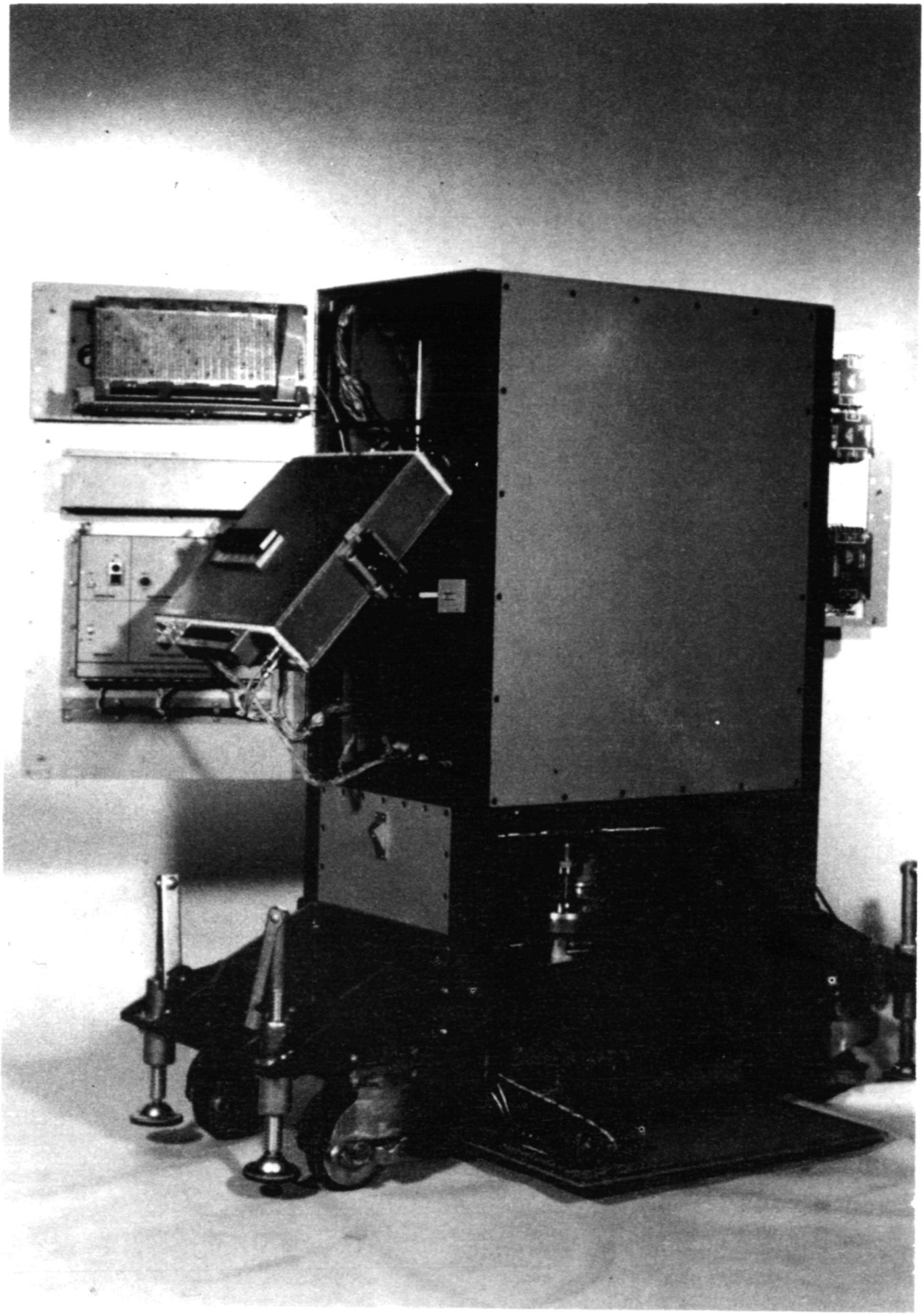


Figure 3. NR Maser Opened For Servicing

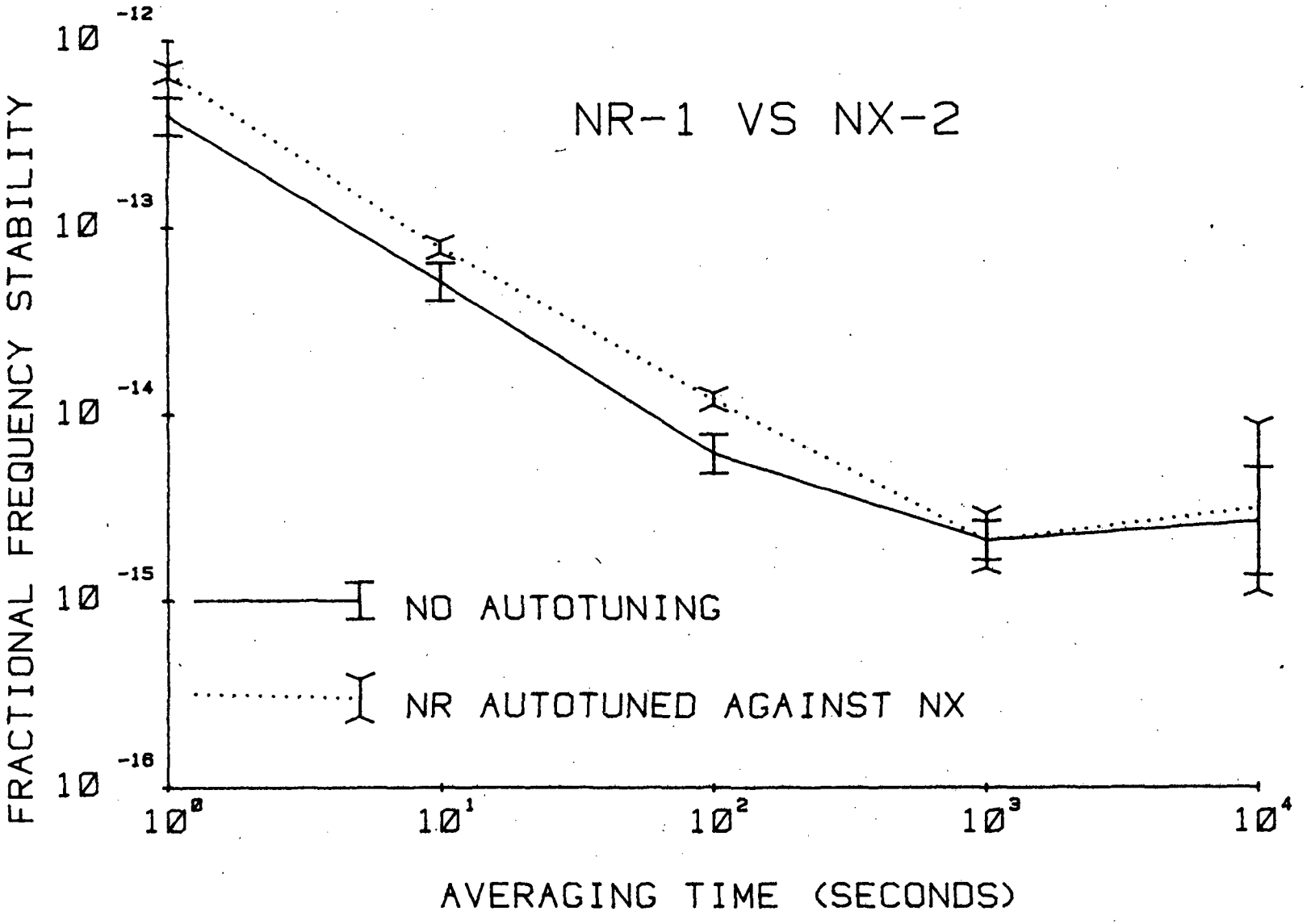


Figure 4. Stability of NR-1 vs NX-2

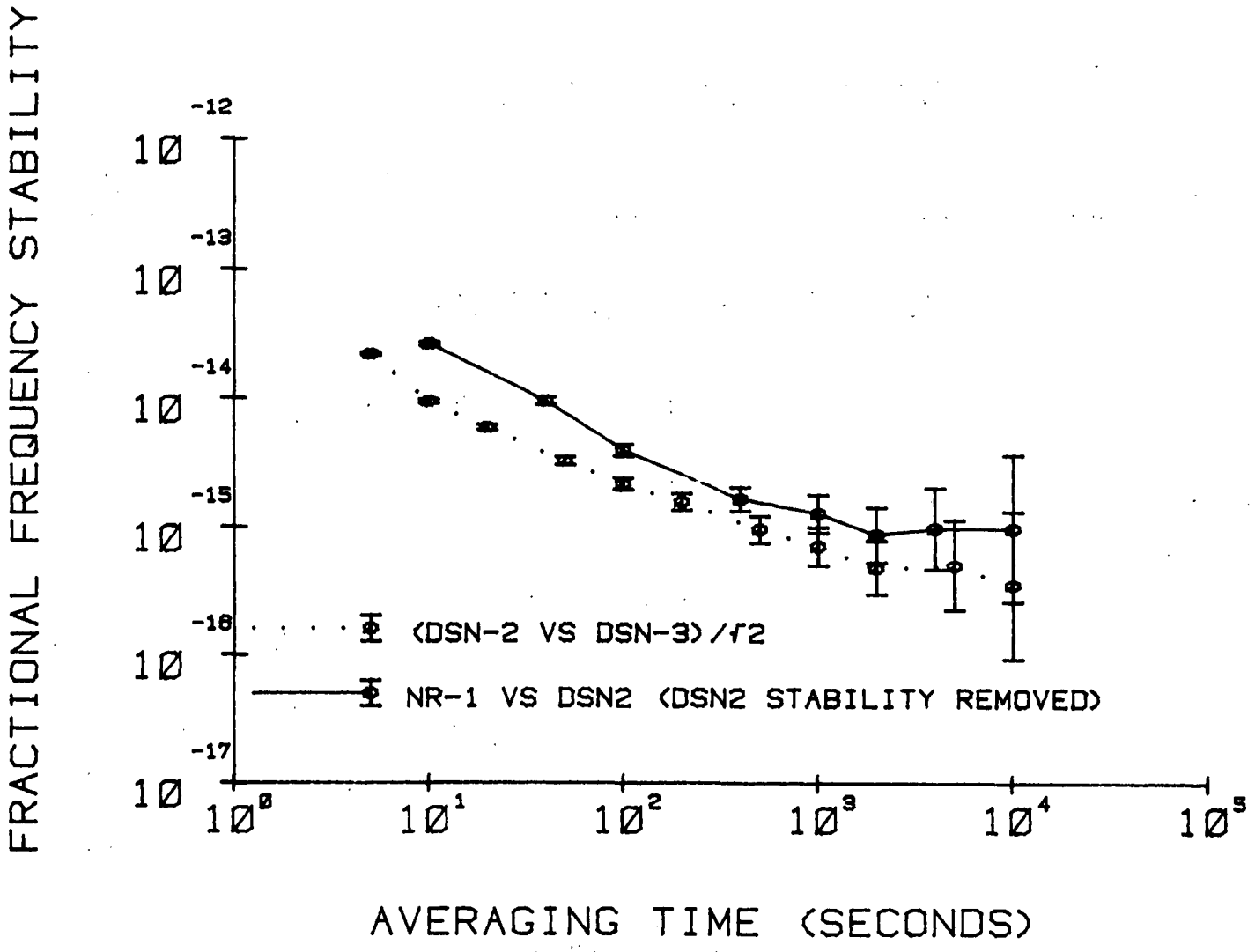


Figure 5. Stability of NR-1 vs DSN-2

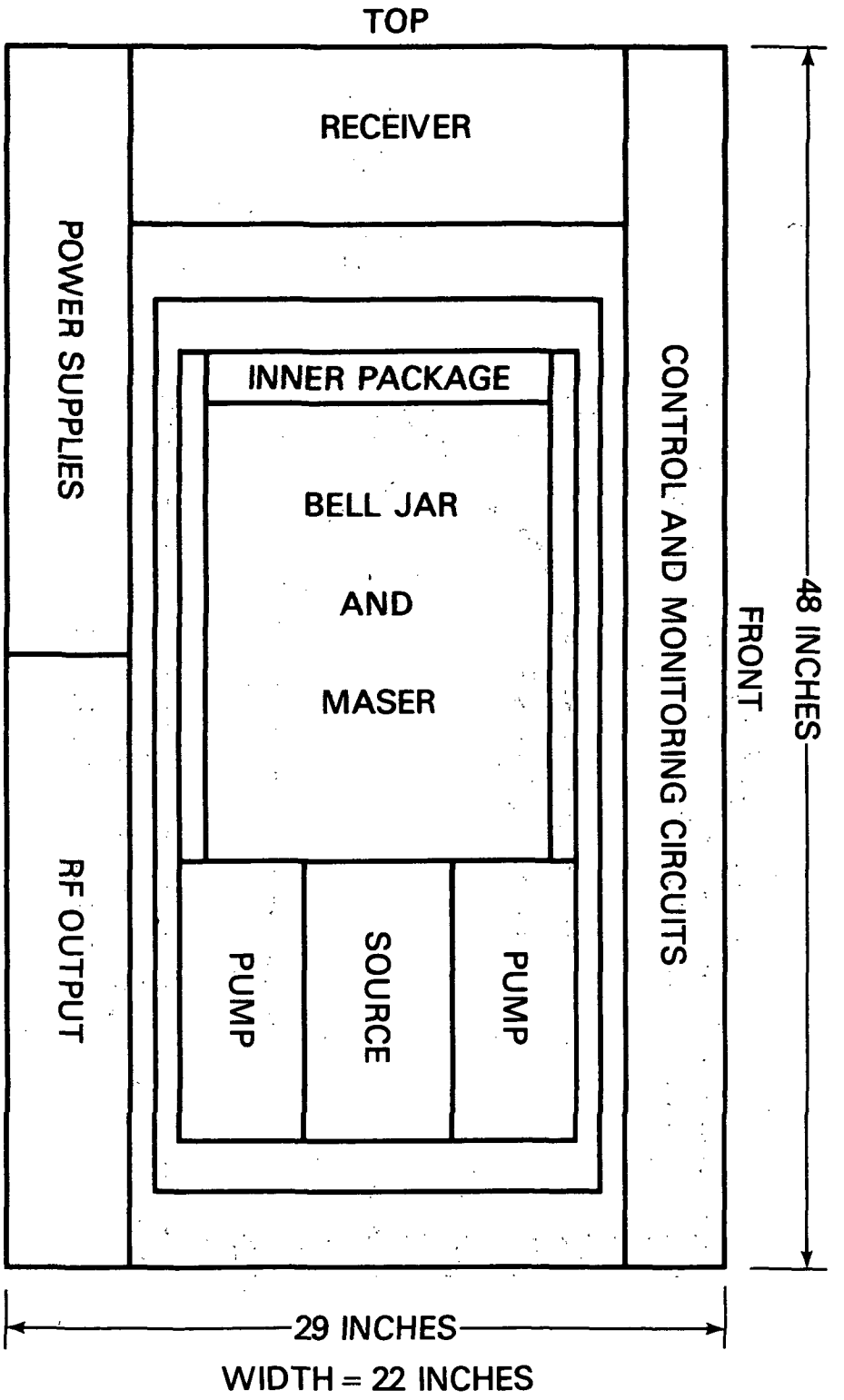


Figure 6. Low Cost Hydrogen Maser

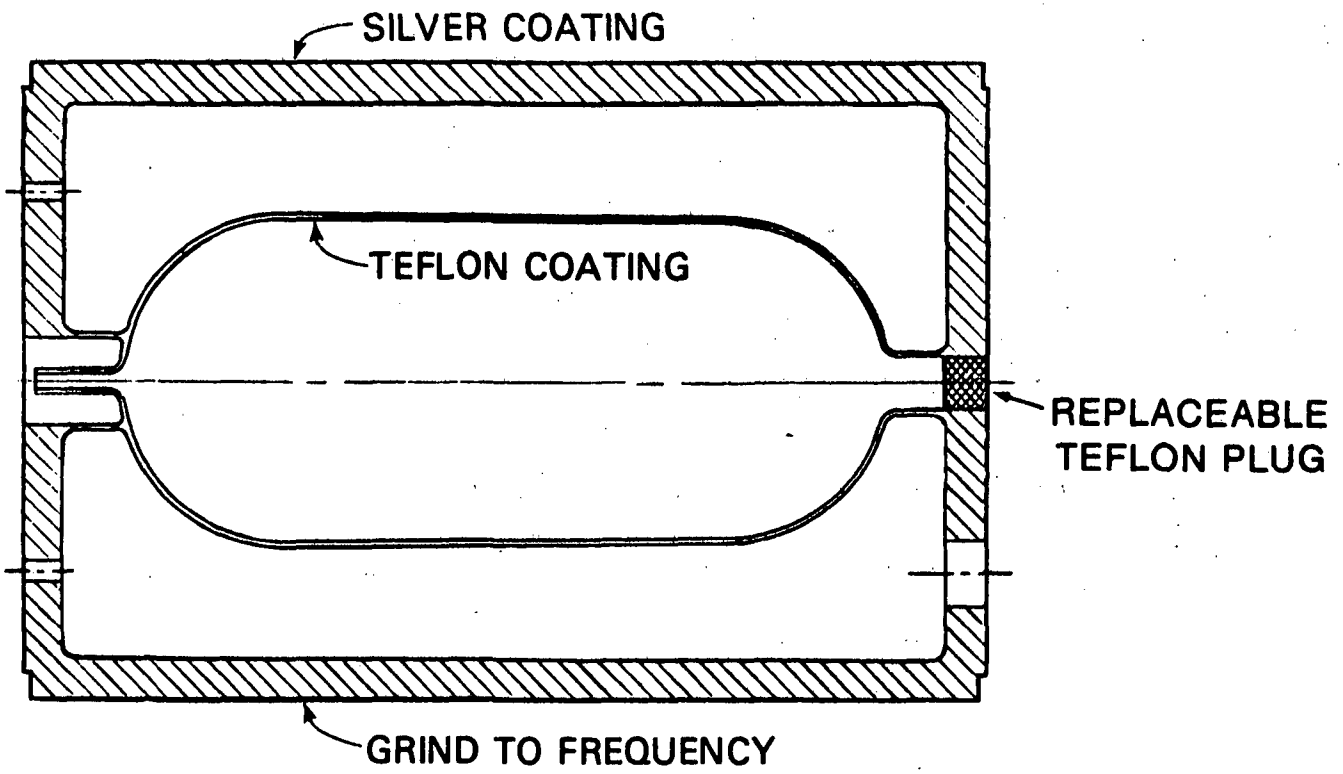


Figure 7. Integral Cavity and Storage Bulb

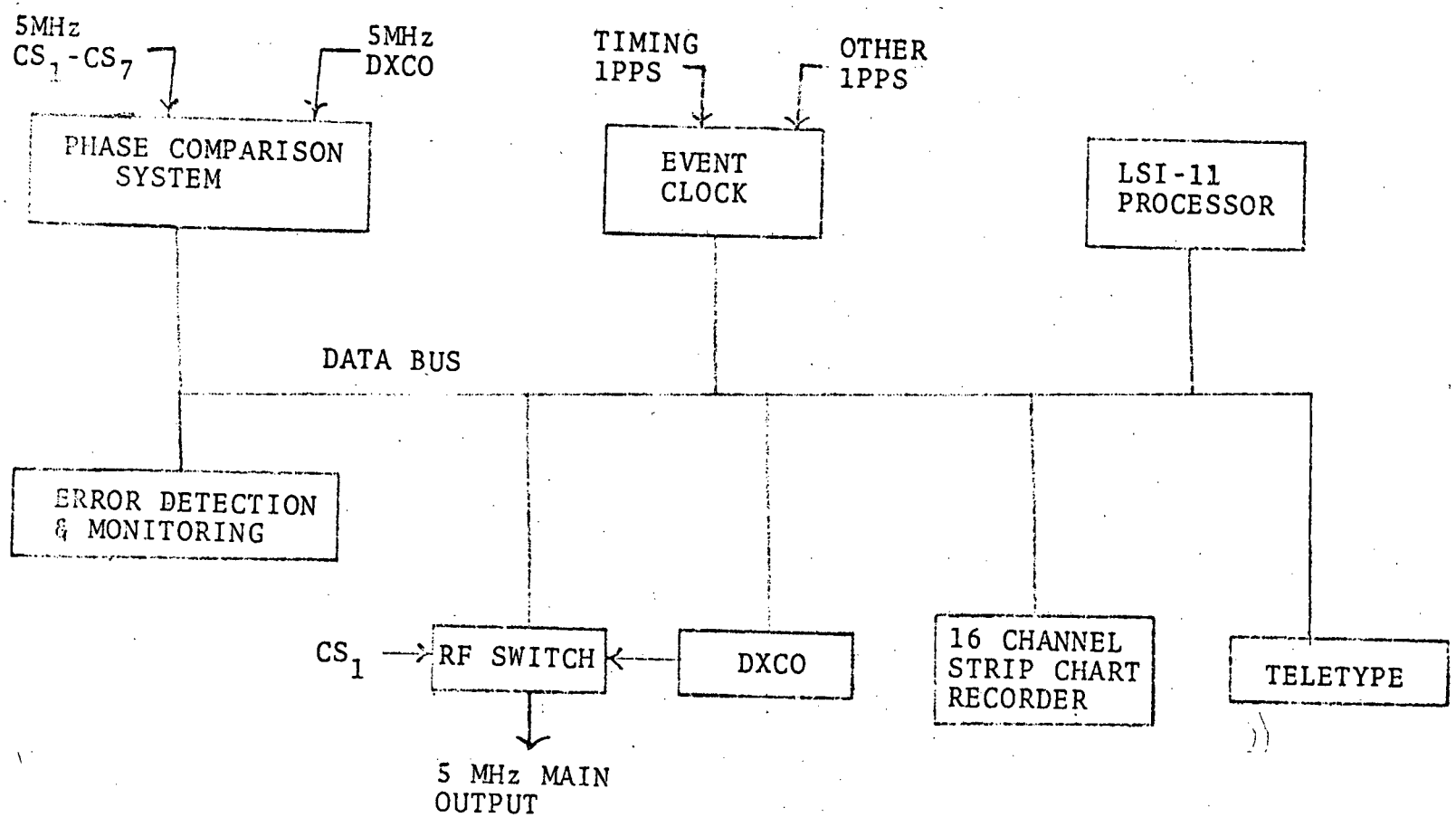


Figure 8. Simplified Block Diagram of the Distribution and Measurement System

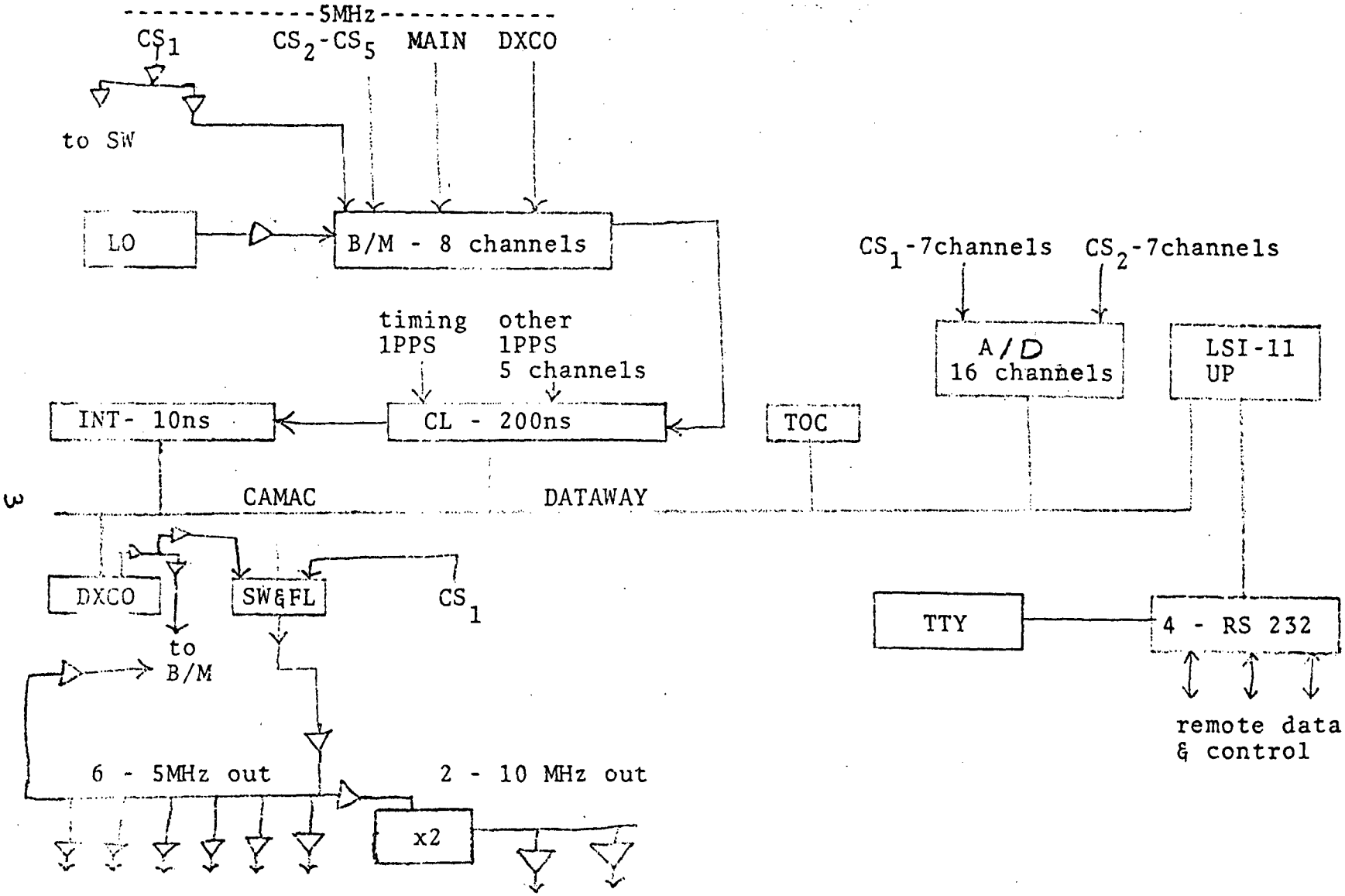


Figure 9. Detailed Block Diagram of the Distribution and Measurement System

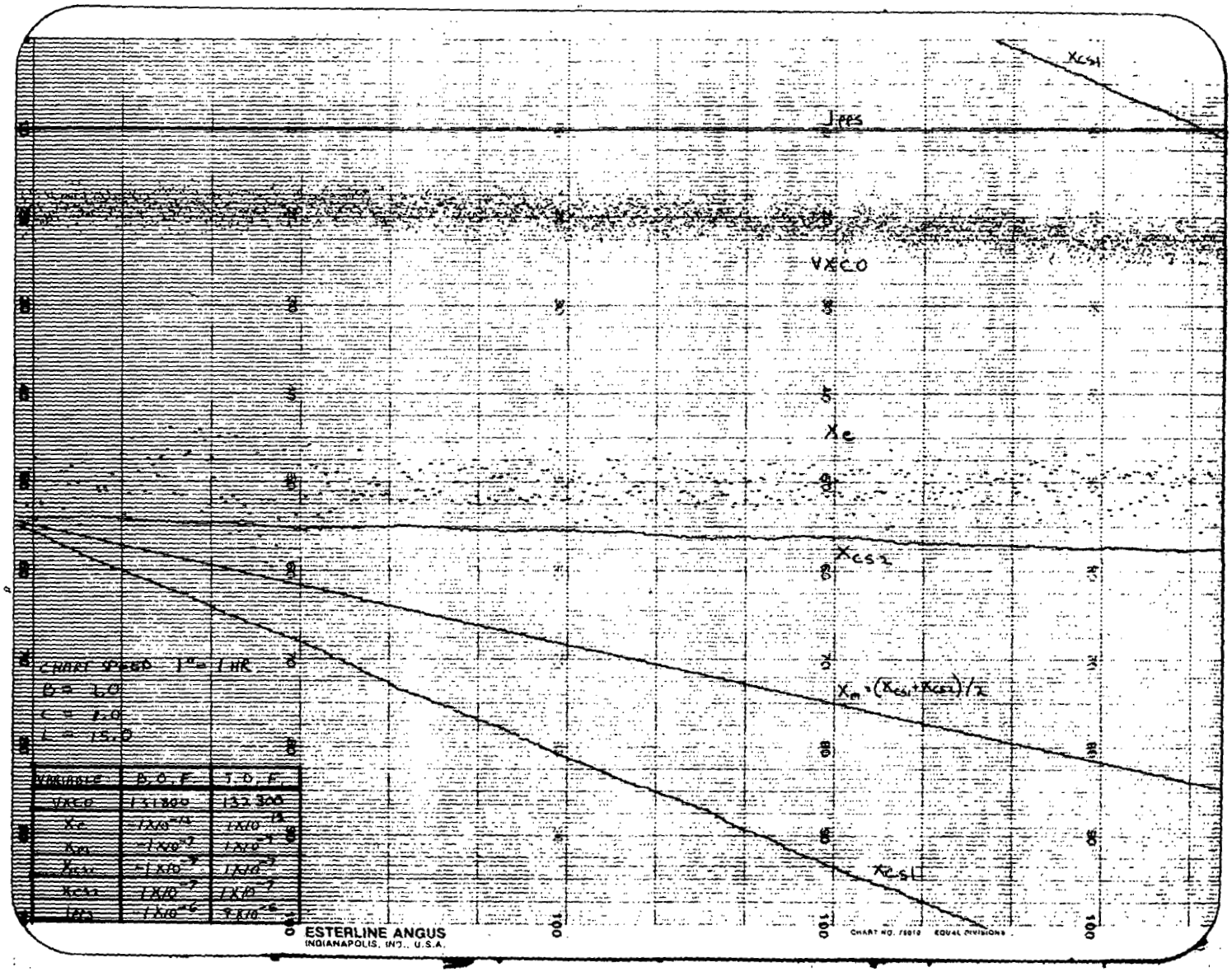


Figure 10. DMS Phase Lock Loop for 1-Second Time Constant

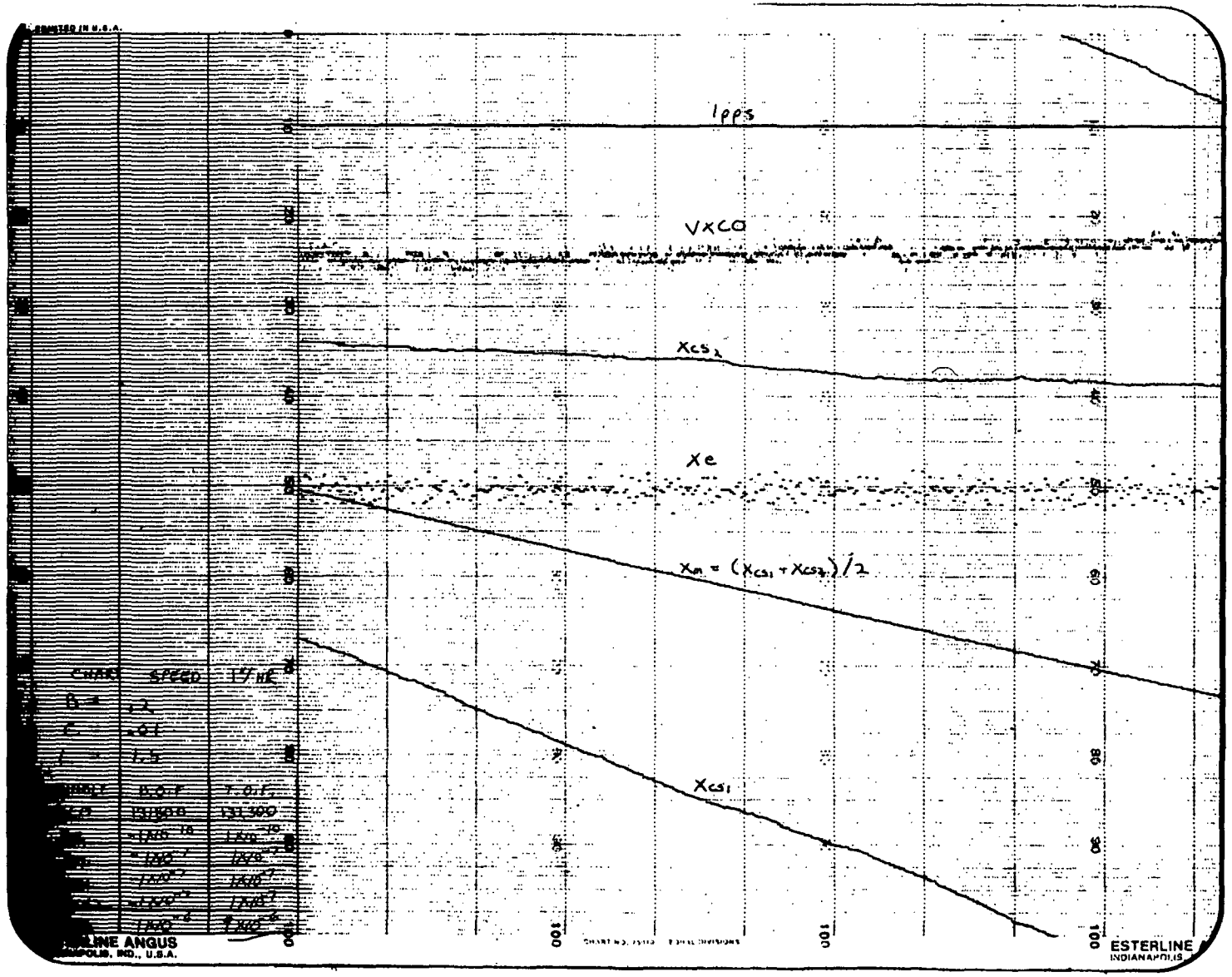
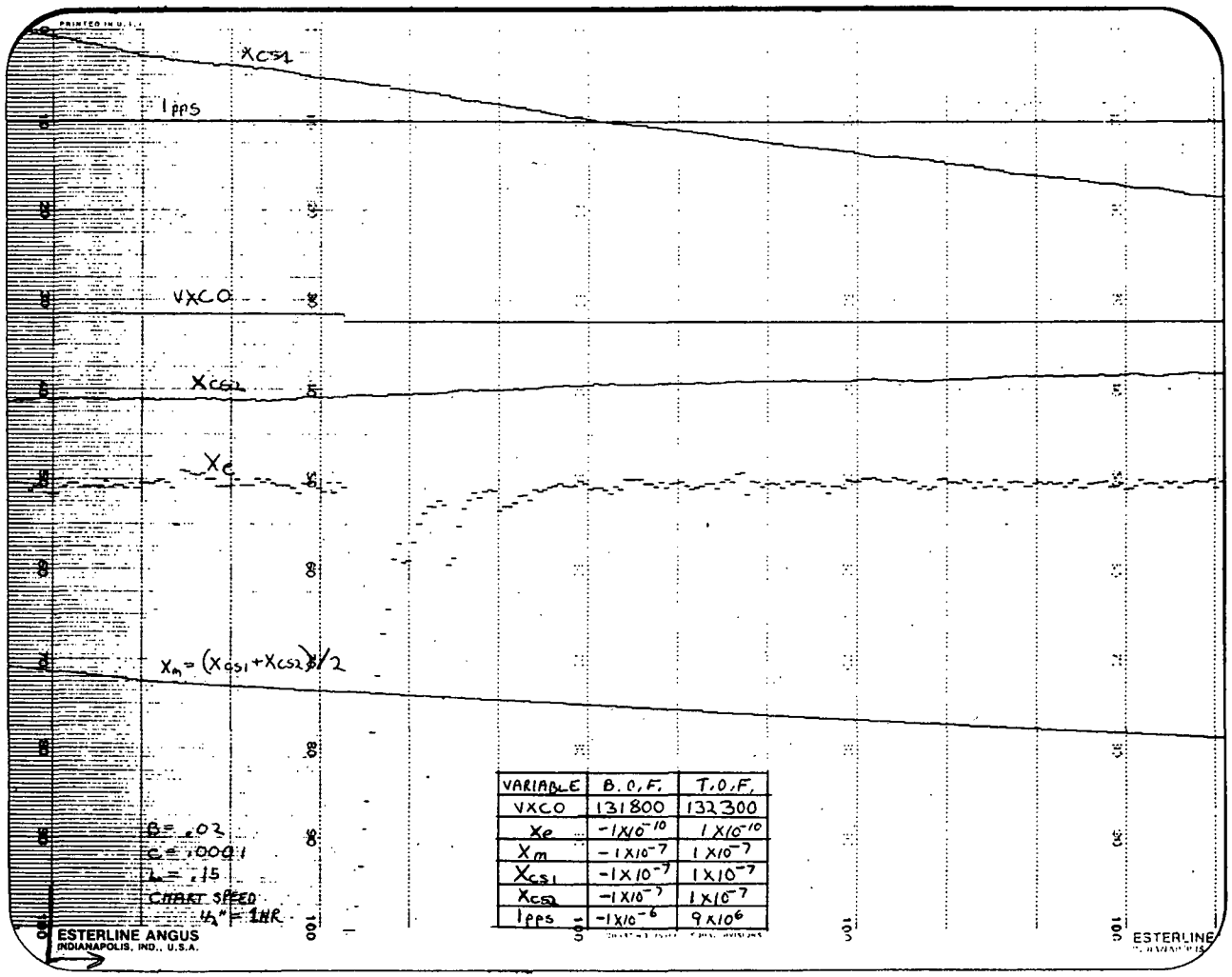


Figure 11. DMS Phase Lock Loop For 10-Second Time Constant



VARIABLE	B.O.F.	T.O.F.
VXCO	131800	132300
X_e	$-1X10^{-10}$	$1X10^{-10}$
X_m	$-1X10^{-7}$	$1X10^{-7}$
X_{CS1}	$-1X10^{-7}$	$1X10^{-7}$
X_{CS2}	$-1X10^{-7}$	$1X10^{-7}$
1pps	$-1X10^{-6}$	$9X10^{6}$

Figure 12. DMS Phase Lock Loop For 100 Seconds Time Constant