NASA CR-165372
DYD-10892-CE

HIGH-CURRENT, FAST-SWITCHING TRANSISTOR DEVELOPMENT

by P. L. Hower

WESTINGHOUSE R&D CENTER

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA Lewis Research Center
Contract NAS3-21380

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF TABLES

1. SUMMARY

The overall objective of this program is the development of device design and process techniques for the fabrication of high-current, fast-switching transistors with sustaining voltages, $V_{ceo}(sus)$, in the 400 to 600V range.

This report describes work that shows how the results obtained under a previous contract (NAS3-18916) have been applied to a larger-diameter (33-mm) transistor. An improved base contact for equalizing the base-emitter voltage at high currents has been developed along with an improved emitter-contact preform which increases the silicon area available for current conduction. The electrical performance achieved is consistent with the proposed optimum design.

Various sections of this report describe the device design, wafer-processing techniques, and various measurements which include forward SOA, dc characteristics, and switching times.

2. INTRODUCTION

Although challenged by the emergence of power MOSFETs and GTOs, the bipolar transistor is still one of the major switching components used for power electronics applications. For those cases where controlled turn-off is required, it is probably the dominant component.

For a given area of silicon, the MOSFET appears to be a more efficient switch at high frequencies, for example $f \gtrsim 20$ kHz, while the GTO excels below a few kHz. In addition, there are possible circuit simplifications with the MOSFET, while the GTO will probably require a gate drive arrangement that is at least as complex and expensive as a bipolar. Consideration of high-temperature operation tends to favor the bipolar over the MOSFET and GTO.

A conclusion supported by work within and outside of the present contract is that all three devices, together with the thyristor, appear to have a place within the power electronics spectrum. The bipolars can be expected to continue to dominate those applications where the frequency lies within a range of approximately 3 to 20 kHz.

This final report describes work that shows how the results obtained under a previous contract (NAS3-18916) have been applied to a large-diameter (33-mm) transistor. Rather than simply scaling up the previous mask dimensions, a number of new ideas and modifications of the previous design have been made. These changes are:

1) An improved base-contact system for equalizing the base-emitter voltage at high currents;

2) an improved emitter-contact preform which increases the silicon area available for current conduction;

3) an increase in the amount of interdigitation of emitter and base, permitting one to achieve an h_{FE} vs I_C performance that more closely approximates the ideal case.

Various sections of this report describe the design, processing, and measured electrical results of these new transistors. Appendix 1 lists the target specifications for the high-current, fast-switching transistors. The report concludes with various projections of future possibilities.

3. DEVICE DESIGN

3.1 Background

As is true in many situations, the design of a transistor requires a compromise. The desire to achieve a large blocking voltage conflicts with the need to control a large collector current at a given current gain h_{FE}. By using appropriate models for transistor behavior, it is possible to state this conflict quantitatively and at the same time develop an "optimized" design.[1] For example, if $V_{CEO}(sus)$ and h_{FE} (at some V_{CE}) are given, then it is possible to determine an impurity profile that will maximize the collector current density, thereby giving a minimum area design (for a given I_C) or a maximum current (for a given emitter area A_E).

The physical reasons for this result can be traced to basic electrical properties of silicon, e.g., carrier mobilities, impact ionization coefficients, and heavy doping effects. Therefore, once $V_{CEO}(sus)$ and h_{FE} (V_{CE}) are chosen, there will be a corresponding current density that cannot be exceeded and the only way to obtain the desired I_C is to make A_E large enough.

There are also other criteria which influence the transistor design. Switching times, forward and reverse safe-operating areas, and junction-leakage currents should be given consideration when designing a transistor. In most designs, however, the dominant terms are $V_{CEO}(sus)$ together with some specification describing the on-state, such as h_{FE} at some I_C and V_{CE}.

3.2 Design Procedure

For a given emitter area, A_E, there are five variables that determine the $V_{CEO}(sus)$, h_{FE} (I_C, V_{CE}) combination. These variables are indicated in Figure 1 and are defined as:

N_c (cm^{-3} impurity concentration in the lightly doped collector

W_c (cm) metallurgical width of the collector

Q_B (cm^{-2}) total acceptors per cm^2 in the metallurgical base

T (s) collector high-level recombination lifetime

G_E ($cm^{-4}s$) emitter "Gummel number"

These five variables must be controlled during processing if the transistor is to meet the desired gain and $V_{CEO}(sus)$.

One of the discoveries made during this contract was the appearance of a relationship between G_E and T. G_E accounts for the hole current "back-injected" from the base into the emitter, while T accounts for recombination in the collector. The physical make-up of G_E is a much discussed topic with recombination, band-gap narrowing, and various other heavy doping effects all being mentioned.

Normally, one would like G_E to be as large as possible since at high currents the gain-current product G approaches a constant given by

$$G = h_{FE} I_c \approx \frac{4q A_E G_E D_c^2}{W_c^2} \qquad (1)$$

Thus, any increase in G_E will increase G, which can be regarded as a figure of merit.

Figure 2 shows the results that have been obtained to date. The data points apply to a wide variety of transistors and include both 33- and 23-mm devices. Open-circuit decay lifetime was measured with a Solid-State-Measurements test unit using the base collector junction as the p-n junction as described in Reference 2.

Although it is worthwhile to speculate why an apparent link exists between G_E and T, these speculations will not be described here.

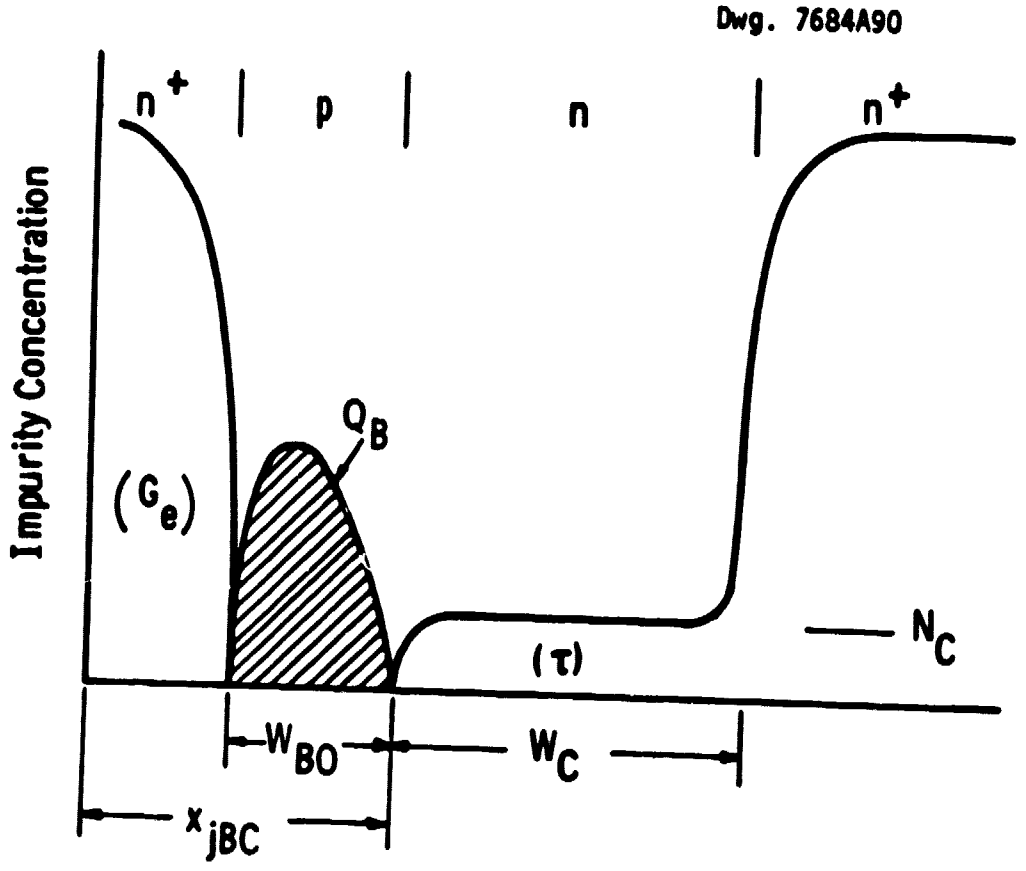


Figure 1 - General shape of the triple-diffused impurity profile

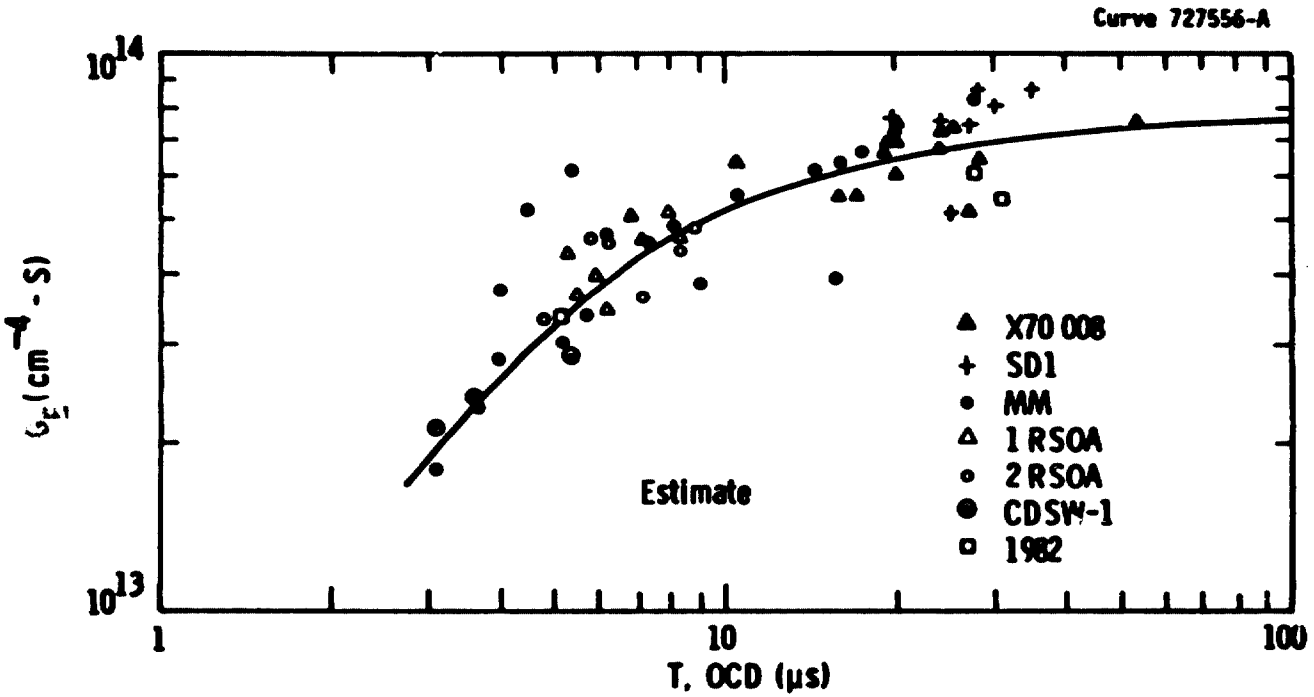


Figure 2 - Measured emitter Gummel number vs. open-circuit decay lifetime for various transistors

We simply treat the G_E vs. T curve of Figure 2 as "given," thereby reducing the number of independent variables from five to four.

In addition, we assume that lifetime is not independent but is fixed by the process. Thus, for a given lifetime one can use the technique of Reference 1 to select Q_B, N_c, and W_c with h_{FE} corrected to account for collector recombination as described in Reference 2.

A computer program has been developed to carry out the optimization, and an example of the printout is shown in Figure 3. For this example the minimum A_E is 2.18 cm^2. The plot of Figure 3 is a running account of the minization process. In this case the peak gain h_{FEO} is treated as one of the independent variables where

$$h_{FEO} = \frac{G_E}{G_B} = \frac{G_E}{Q_B/D_B} \qquad (2)$$

with G_B being the base Gummel number and D_B the effective electron diffusion coefficient in the metallurgical base.

Figure 4 shows the required emitter area as a function of lifetime for two different designs corresponding to the contract goals of G = 1700 A for V_{CEO}(sus) = 400V and G = 1200A for V_{CEO}(sus) = 600V. The curves of this figure have been obtained using the data of Figure 2 and the optimum design program.

3.3 Mask Design

A 33-mm mask set has been prepared which incorporates a number of features that improve the overall performance of the transistor when compared with the geometry of the present 23-mm D6C design. These features are:

1) A decrease in emitter stripe width from 30 to 20 mils resulting in approximately 50 percent more perimeter;

2) providing a path for base current to reach the outer portions of the emitter;

3) an emitter contact preform that is compatible with feature (2);

4) a new base contact that improves the distribution of base current.

```
                New Input Data

VCE=   2.5 V              IC = 170.0 A
VCEO(sus)=   400.0 V      HFE=   10.0
TJ=    25.0 DEG.C         τ=   10.0 μs
DC= 23.0 cm^2/s           ΔE=  .050 eV

At ref.temp. the program uses:
μCO( 25.0 C)= 1300.0 cm^2/V-s
Ge= 5.30E+013 cm^-4-s

At TJ these values apply:
μCO( 25.0 C)= 1300.0 cm^2/V-s
Ge= 5.30E+013 cm^-4-s
_
                Optimum Design

AE= 2.18E+000 cm^2     hFEO=   22.7

NC=1.78E+014 cm^-3          m=   .700

WC=   44 0 μm          BVCBO=   796 V
Rho,C=    27.1 ohm-cm   τ=   10.0μs
```

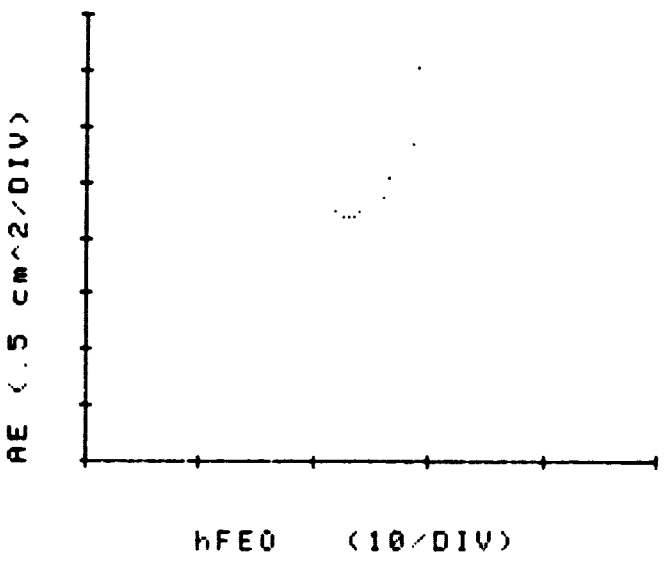


Figure 3 - Computer printout for transistor optimization program

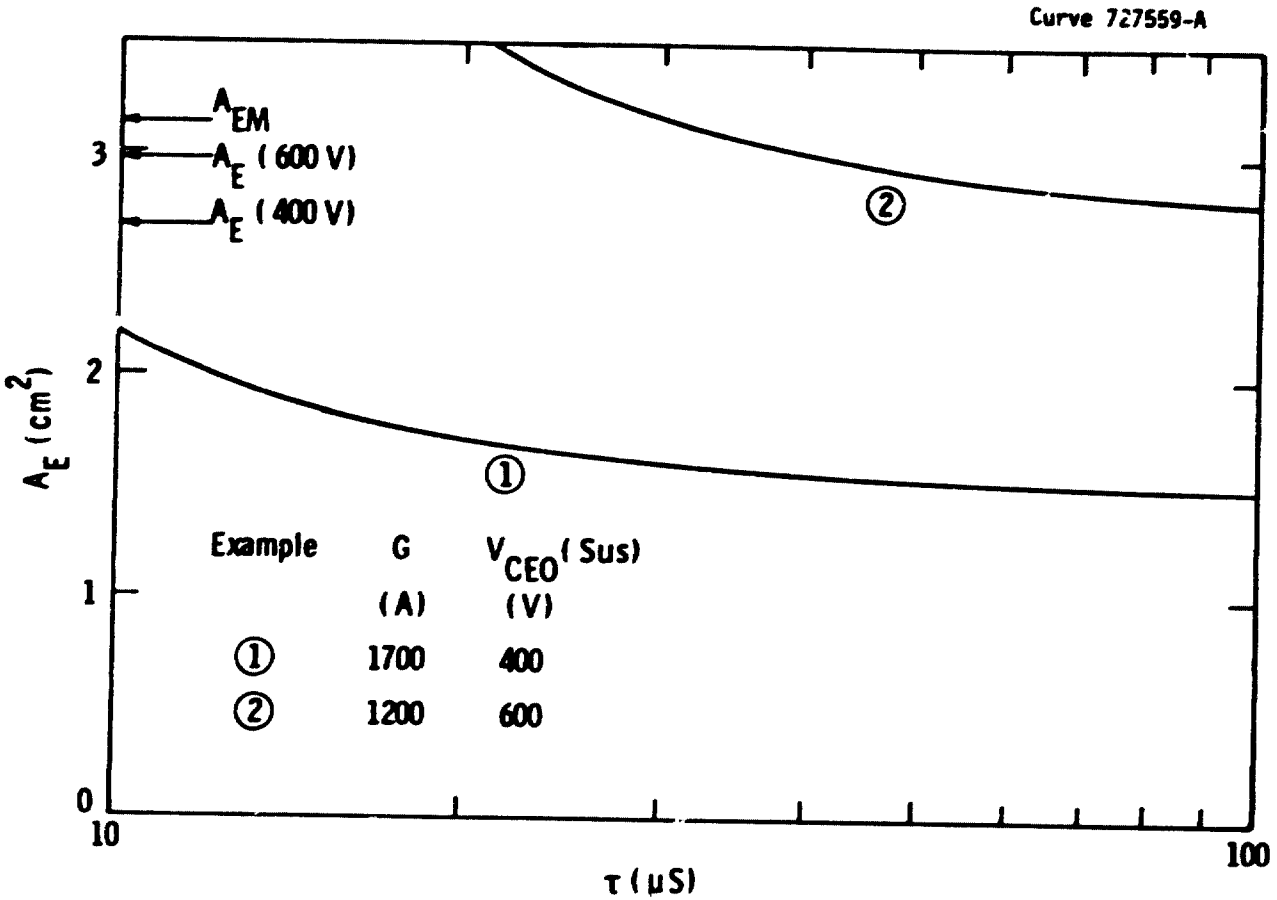


Figure 4 - Minimum emitter area vs. collector lifetime for two design examples

Figure 5 shows the pattern used for the metal mask of which various characteristics are summarized in Table 1. The metallurgical and effective emitter areas are indicated in Figure 4.

For the A_E values of Figure 5, a lifetime of 30 μs was assumed. The 400V design goals are easily met with this value of lifetime, although it appears to be marginal for the 600V goals. For this design a $\tau \gtrsim 50$ μs is required. Lifetime values of this magnitude have been achieved with careful processing, the results of which are described in Section 4.

Figure 6 shows a plot of calculated h_{FE} vs. I_C for the two designs. These calculations are based on the model of Reference 2 and the G_E vs. τ curve of Figure 2.

3.4 Influence of Base Metallization on Gain Performance

It was noted in the final report of Contract NAS3-18916 that the potential drop introduced by the sheet resistance of the base contact metallization can influence the collector current distribution. This effect is normally not important for the 23-mm device and shows up only at large values of collector current.

Figures 7, 8, and 9 show the results for the 23-mm transistor of a current distribution analysis[3] which takes into account the effects of base-sheet metallization, emitter-contact resistance, and transistor behavior. The method of analysis is similar to that of Reference 4 and assumes that the transistor is in quasi-saturation.

Figure 9 shows how the effective area is reduced as current is increased. This effect is treated here as being independent of emitter current-crowding, but in an actual transistor both effects would have to be taken into account.

Figure 7 shows that it is the voltage drop along the "base trunk" which contributes most of the V_{Be} variation. Thus, if one could build up the metallurgical cross-section of the base trunk, the curves of Figure 7 would move closer together and the high-current performance would be improved.

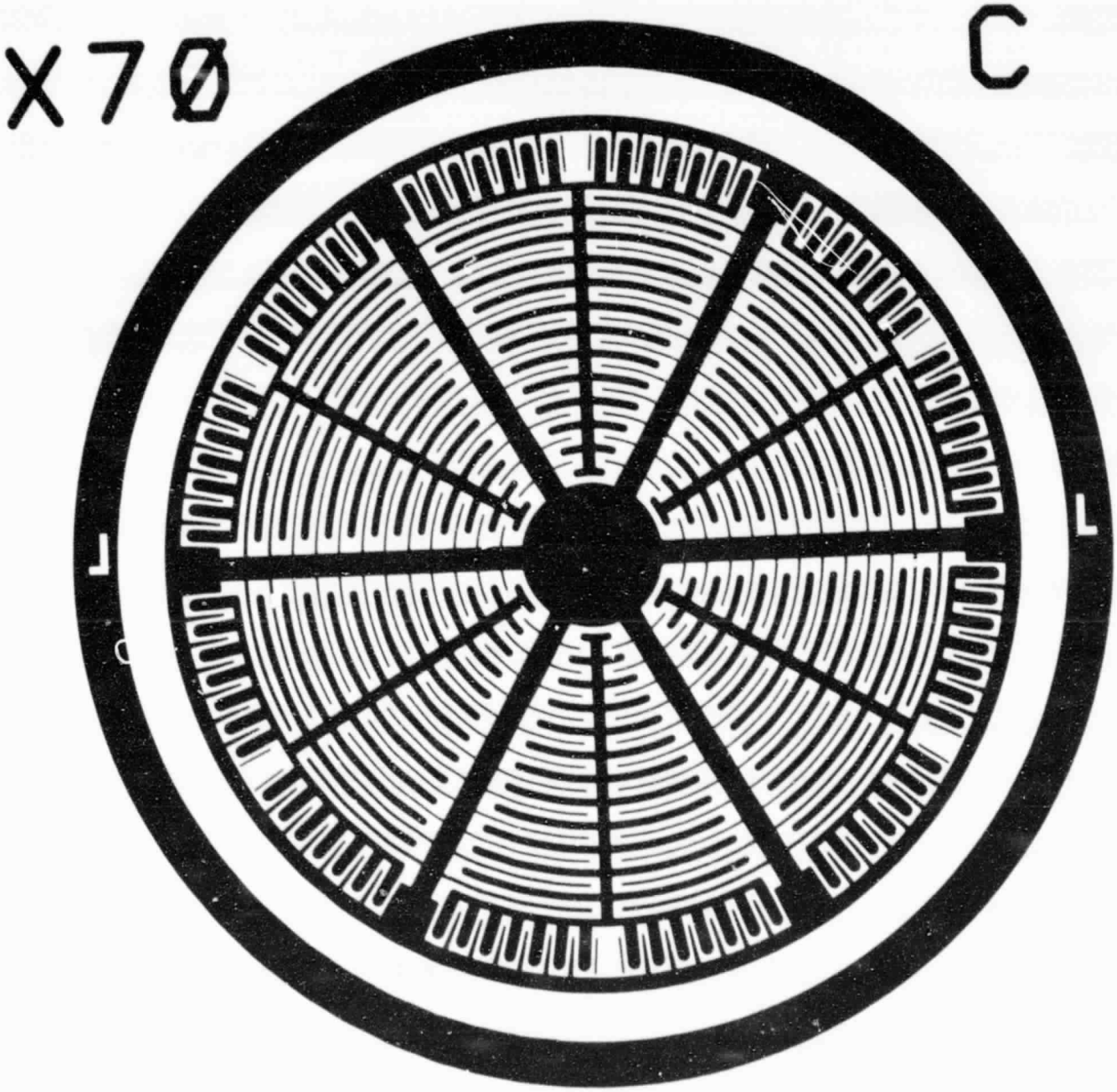


Figure 5 - Mask design for the 33-mm transistor

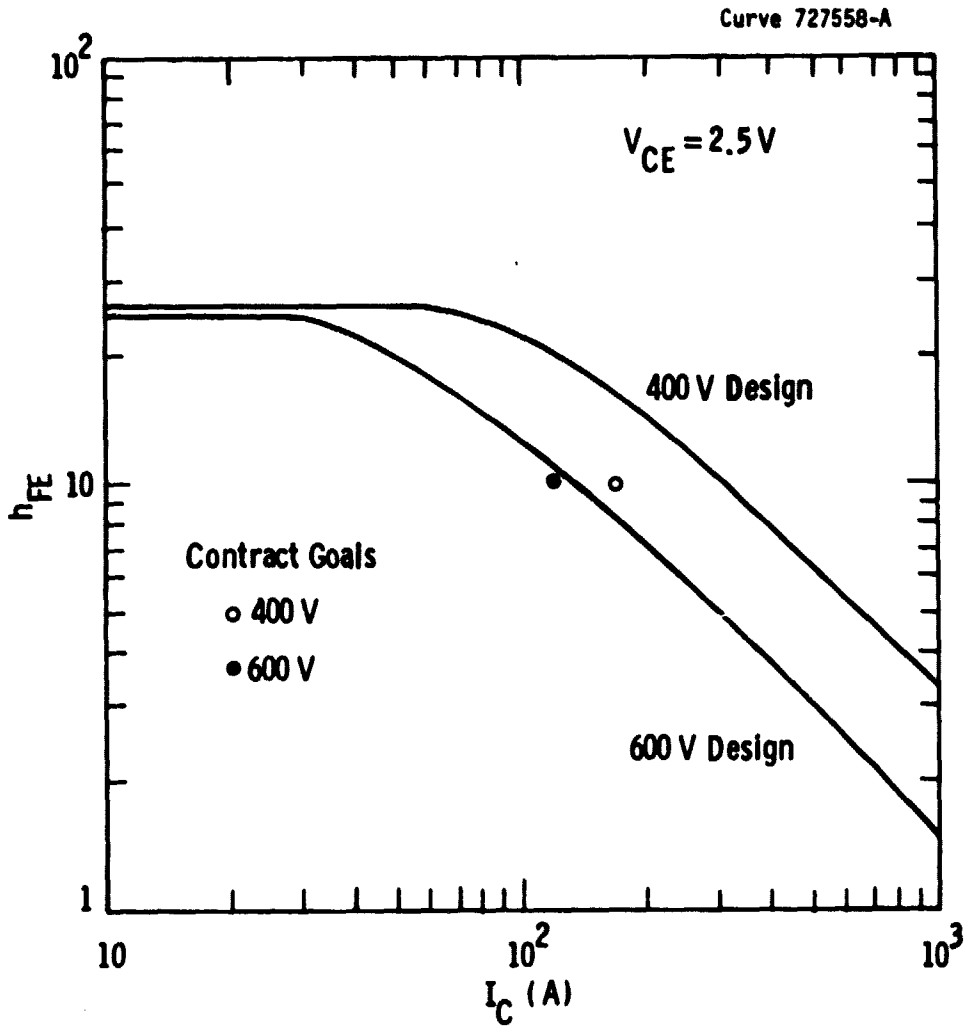


Figure 6 - Calculated current gain vs. collector current

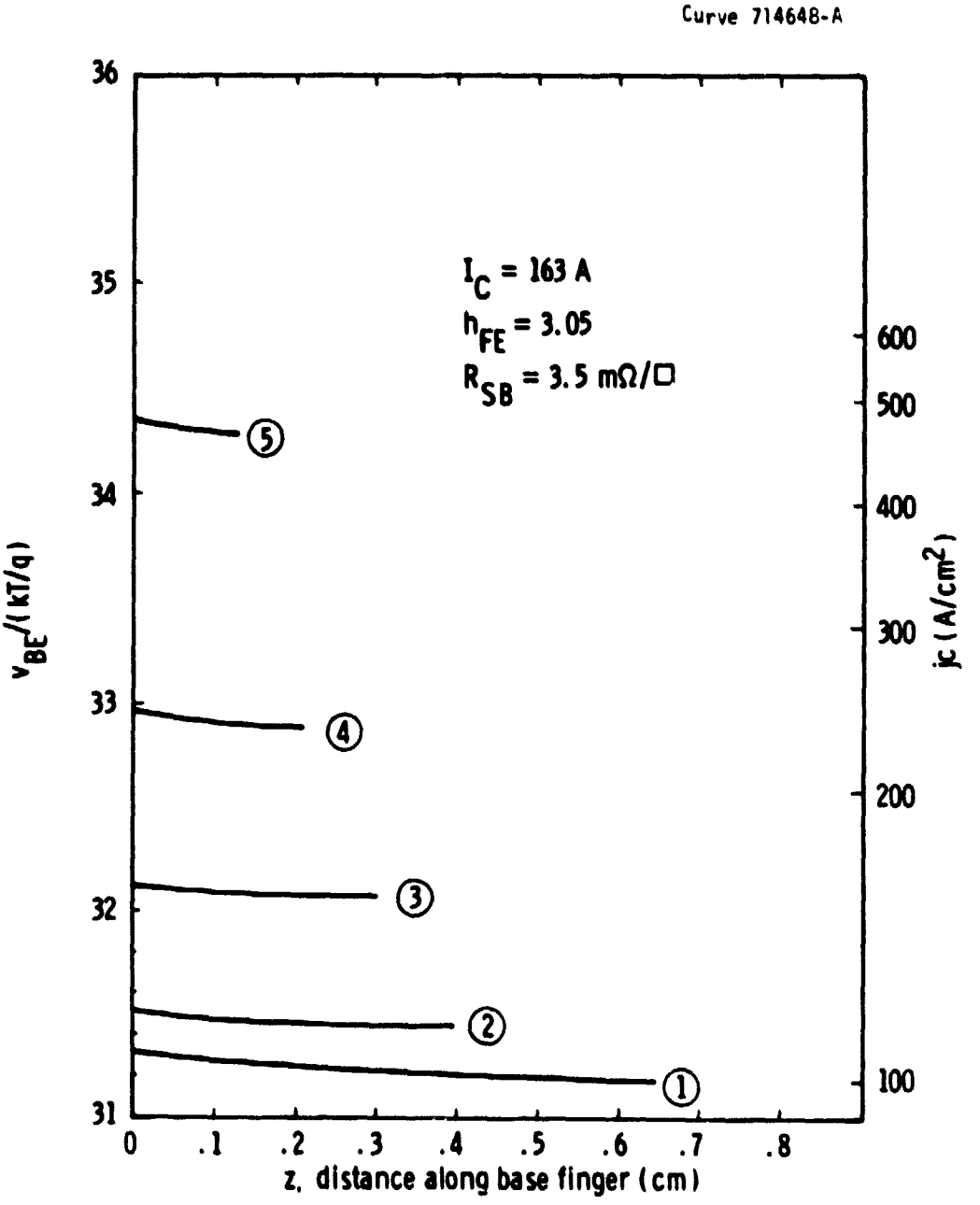


Figure 7 - Base-emitter voltage (normalized to kT/q = .0256V) and current density for the typical sector shown in Figure 8

Figure 8 - Metallization pattern showing base fingers and radial distance from base-trunk centerline

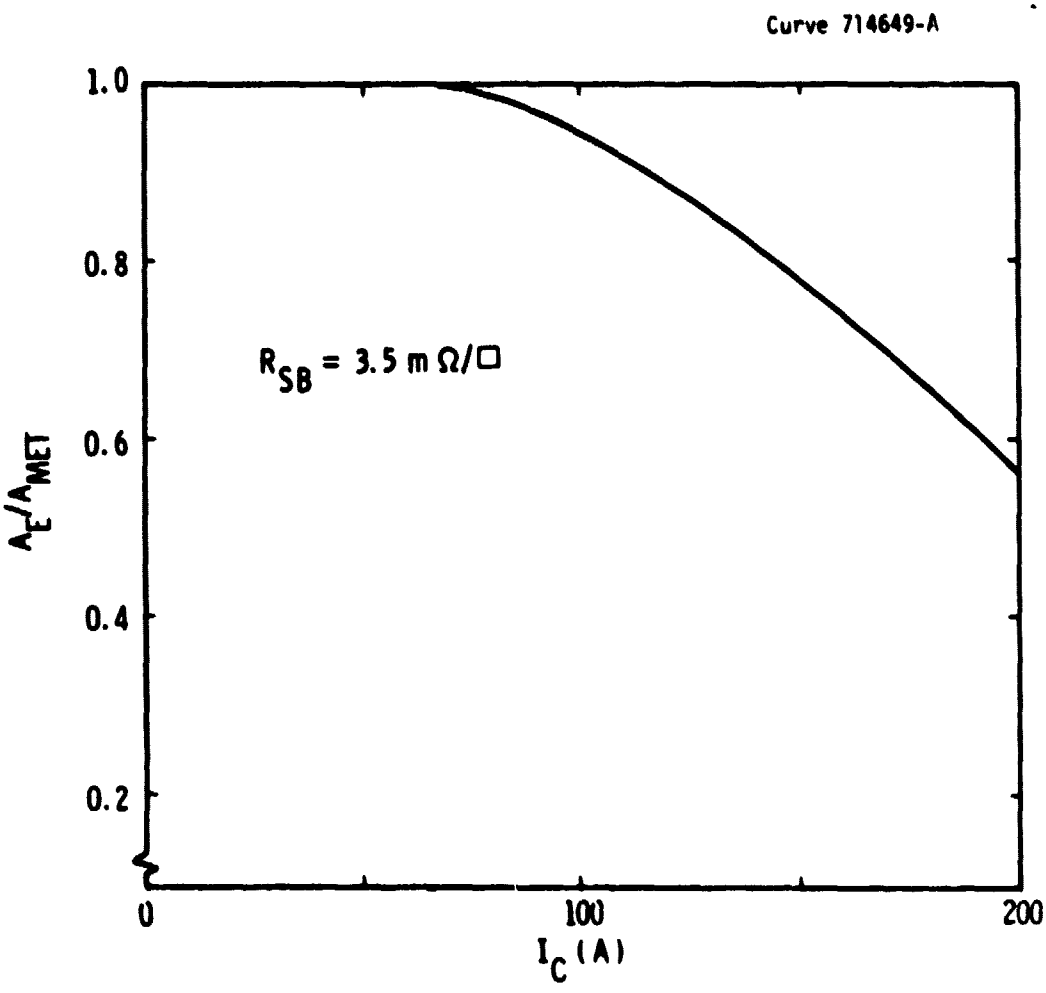


Figure 9 - Fractional reduction in emitter area vs. collector current due to base-metallization sheet resistance for the pattern of Figure 8

Table 1 - X70 Mask Design

metallurgical emitter area	= A_{EM} = 3.3 cm^2
perimeter	= Z = 121 cm
one-half stripe width	= L_E = 0.0254 cm
effective emitter area (400V design)	= A_E = 2.67 cm^2
effective emitter area (600V design)	= A_E = 2.96 cm^2

Under the present contract such a method was devised and is the subject of a patent disclosure. This new contact method should be particularly useful for low voltage, 33-mm designs and for increased diameters in the 400 to 600V range.

For the design of Figure 5 the standard metallization scheme appears to be adequate, although some improvements can be achieved. This conclusion is based on the base-distribution analysis and also on experimental measurements made using transistors which incorporated the improved base-contacting scheme.

Figure 10 shows the reduction in ausi-current product G that occurs as I_C is increased for the conventional and improved base-contacting methods. The new contact has value for G $\gtrsim$ 1900A where $h_{FE} \gtrsim 10$.

For a lower voltage design (225 V) with the conventional contact, G is significantly reduced from the ideal value at h_{FE} = 10. The appropriate curves are shown in Figure 11. In this case, I_C values of approximately 800A should be possible with a 33-mm fusion using the new base contact.

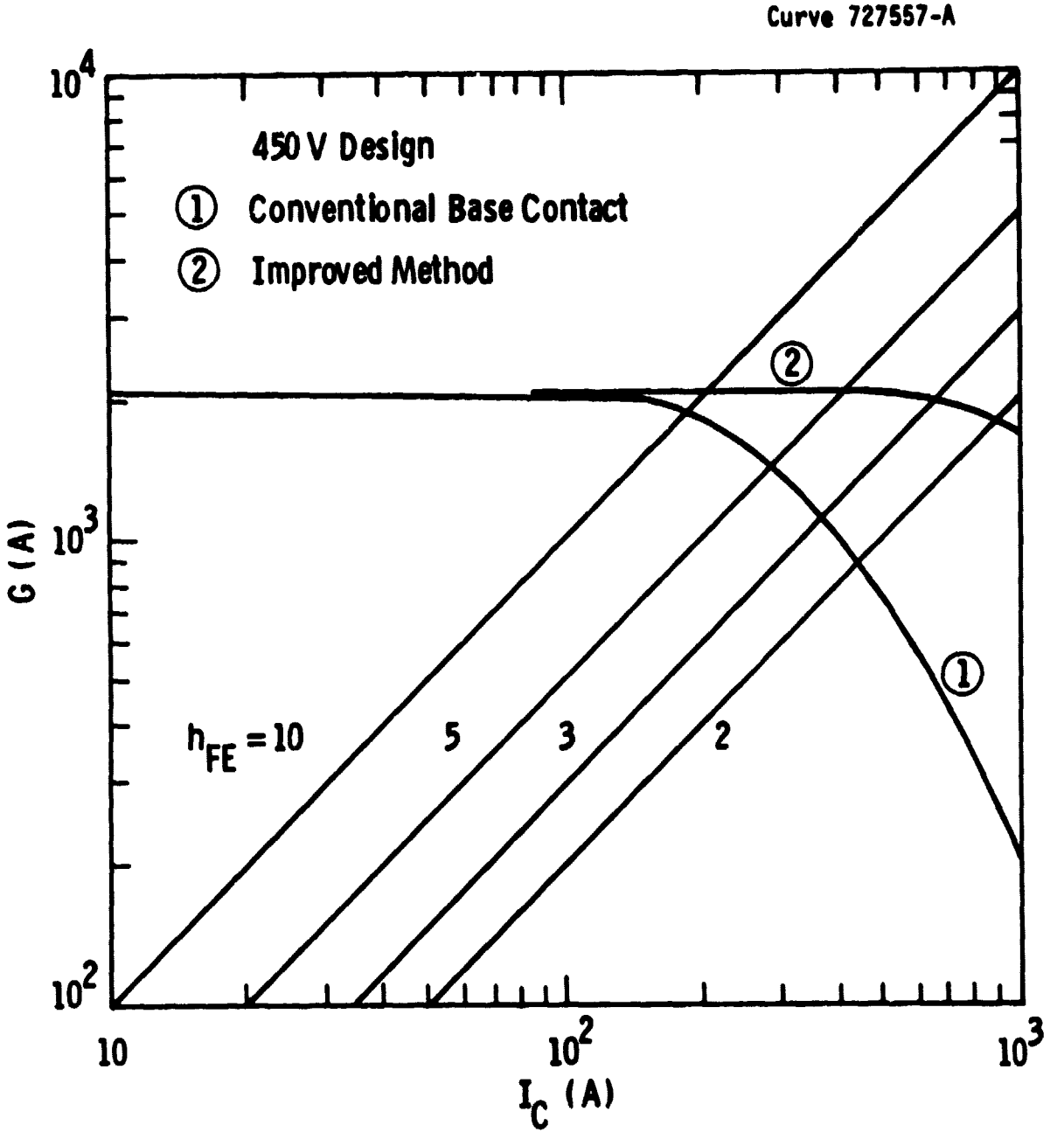


Figure 10 - Gain-current product vs. collector current for two different base contacts (450V design)

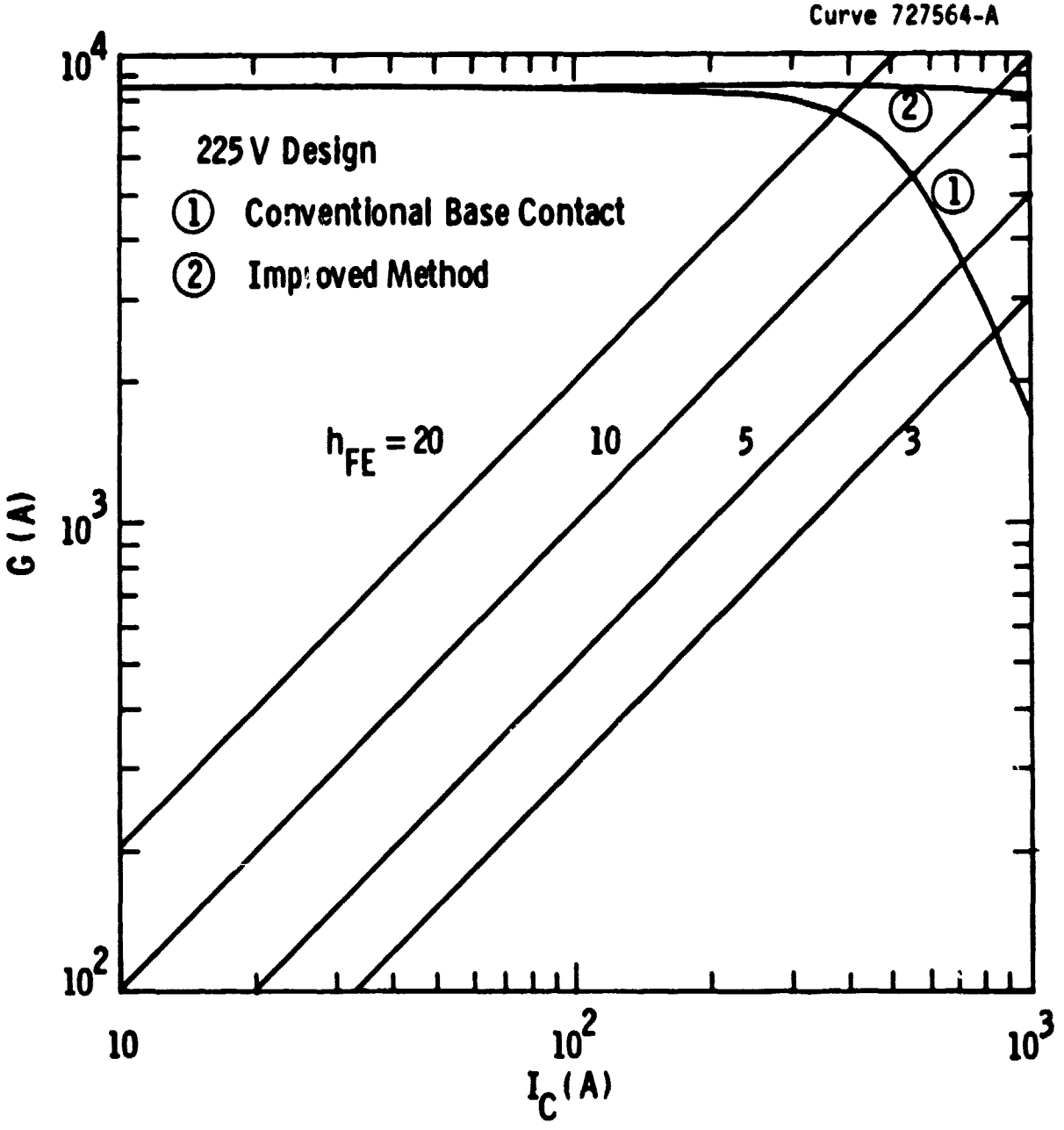


Figure 11 - Similar to Figure 10, but for a 225V design

4. RESULTS

4.1 Fabrication Method

With the exception of a few minor modifications, the transistors were processed using the scheme developed under Contract NAS3-18916. A processing flow diagram indicating the various steps and the appropriate device cross-sections is shown in Figure 1[illegible]. Most of the steps involve conventional silicon-processing procedures with the exceptions being alloying, bevel grind, spin etch, and emitter preform attachment. These steps are near the end of the process and are peculiar to high-power device fabrication.

A completed transistor element or "fusion" is shown in Figure 13. For purposes of electrical testing, the emitter preform is held in place using a ring of RTV silicon elastomer. When the device is encapsulated and under pressure, the emitter and collector contact is maintained by a comprehensive force, as is typical in high-power device technology.

Packaged transistors are shown in Figure 14. The stud package is useful for experimental evaluation and breadboard construction; however, this package generally requires more mounting space and is more expensive than the disc package.

The disc package shown in Figure 14 was developed under a Westinghouse program and is intended for pilot production of the 33-mm high-current transistor which has been designated D70. To facilitate circuit and device evaluation, all the devices submitted in connection with this contract have the stud package.

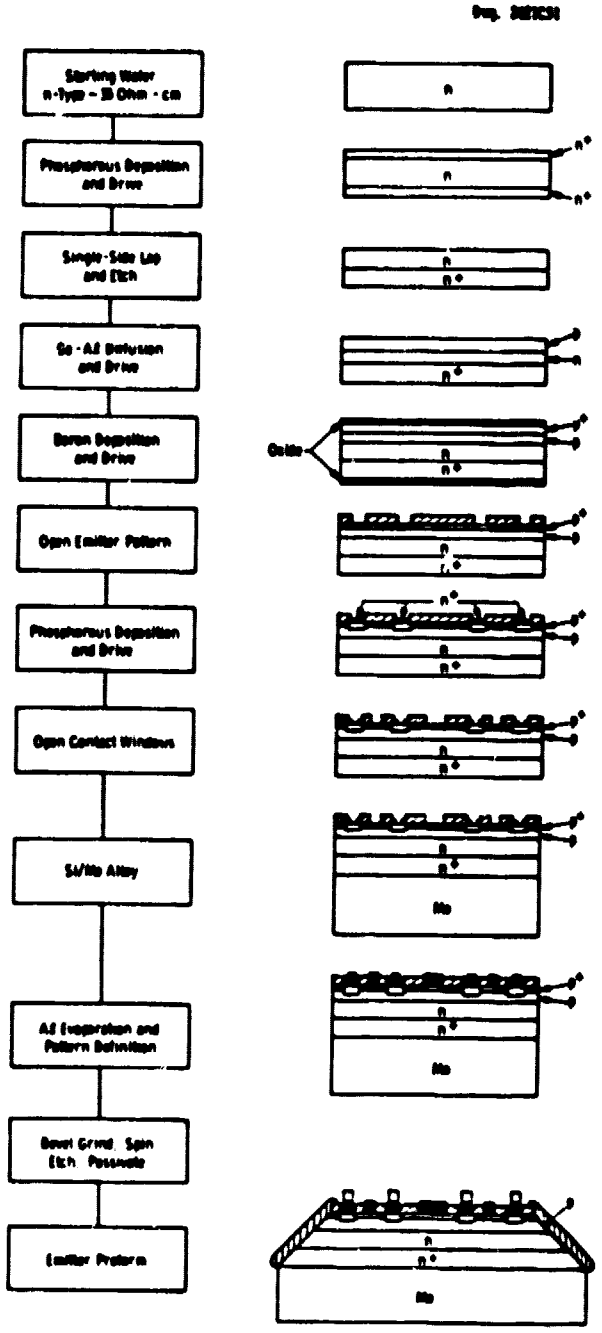


Figure 12 - Processing flow sheet with device cross-sections

Figure 13 - 33-mm transistor fusion

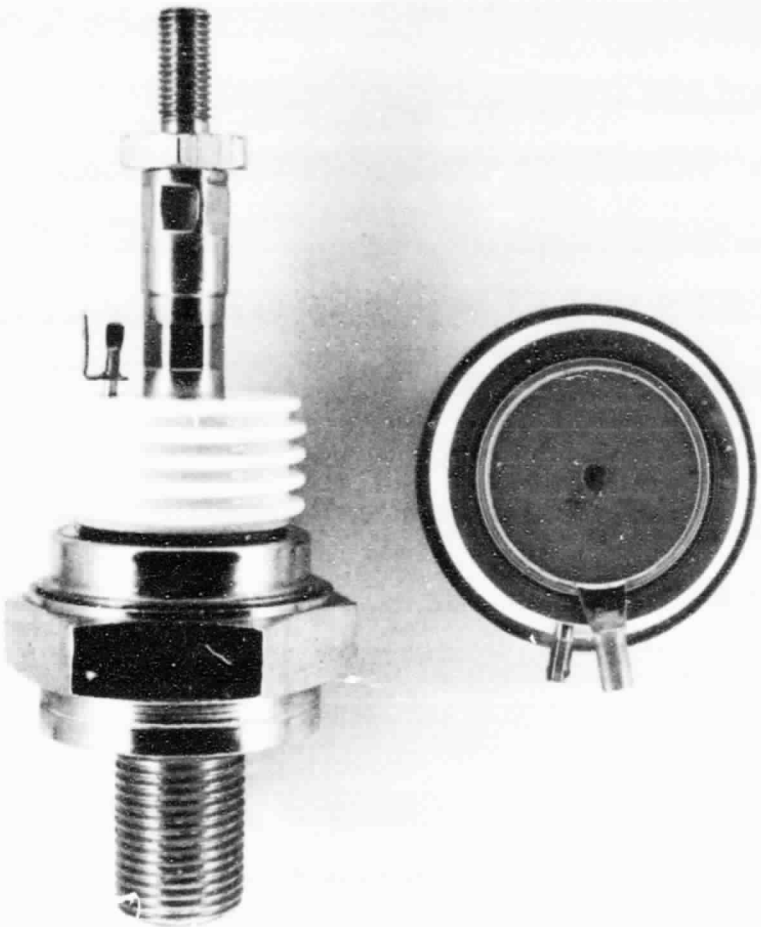


Figure 14 - Left to right, stud and disc packages used for the transistor

4.2 Electrical Performance

4.2.1 Gain Data

Figure 15 shows three collector characteristics for a transistor having a $V_{CEO}(sus)$ = 428V. The upper two photos were obtained using a specially constructed curve traced with I_C and I_B capability to 1000A and 200A respectively.

Measured h_{FE} vs. I_C data is shown in Figure 16, where the $G = (H_{FE}\ I_C)$ asymptate has a value of 2270A. This value is in excess of the contract goal of 1700A and compares favorably with the G = 3000A for the 400V design predicted in Figure 6. That is, if we scale the measured G by the usual 2.3 power of the open base-sustaining voltage, then a 400V version of the measured transistor would have $G \simeq 2700A$, which is within 10 percent of the optimum design.

A similar plot for a higher-voltage transistor with $V_{CEO}(sus)$ = 577V is shown in Figure 17. For this transistor the measured G is 1450A. Scaling this value to a $V_{CEO}(sus)$ = 600V gives G = 1325A, which exceeds the contract goal and is also in close agreement with the theoretical prediction of Figure 6.

Since most user interest appears to be with devices in the 400 to 500V range, work has been concentrated on these devices during the contract period.

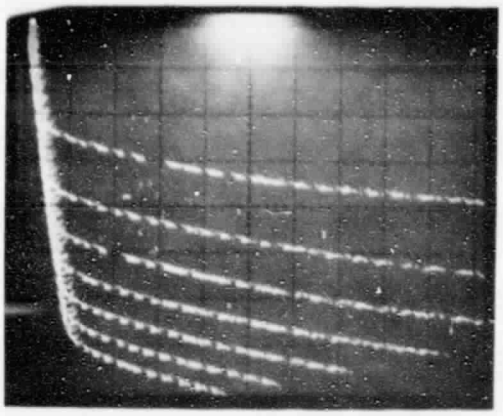
Various data summaries are given in Appendix 2 for transistors supplied as part of this contract. These devices have $V_{CEO}(sus)$ which cover the range of 400 to 600V.

4.2.2 Forward Safe-Operating Area

Figure 18 shows the predicted forward SOA for different pulse times assuming a single pulse of duration t_p. These curves were calculated by using measured transient thermal-impedance data together with the criterion that the transistor becomes thermally unstable at a particular junction-to-case temperature. This temperature will be a function of I_C and R_E. Since the transistor must be in the thermally

Ⓦ TRANSISTOR DATA

DATE 2-24-81



I_C

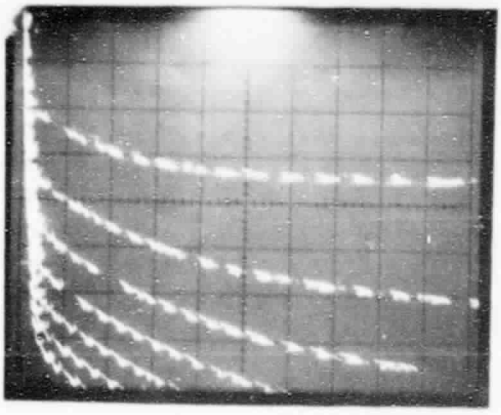
DEVICE 17-32

I_C 50 A/D

V_{CE} 1 V/D

I_B 10 A/s

7 steps



I_C

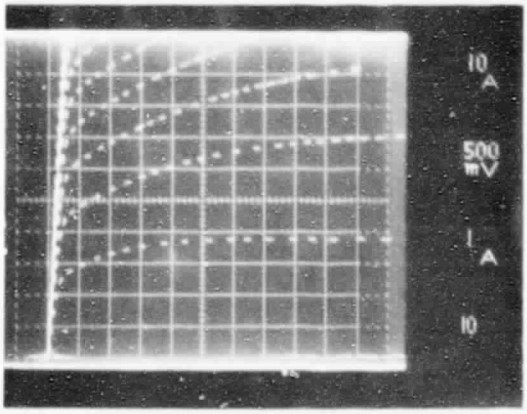
DEVICE 17-32

I_C 20 A/D

V_{CE} 1 V/D

I_B 2 A/s

7 steps



I_C

DEVICE 17-32

I_C 10 A/D

V_{CE} 0.5 V/D

I_B 1 A/s

V_{CE}

Figure 15 - Curve-tracer data for transistor 17-32
$V_{CEO}(sus)$ = 428V

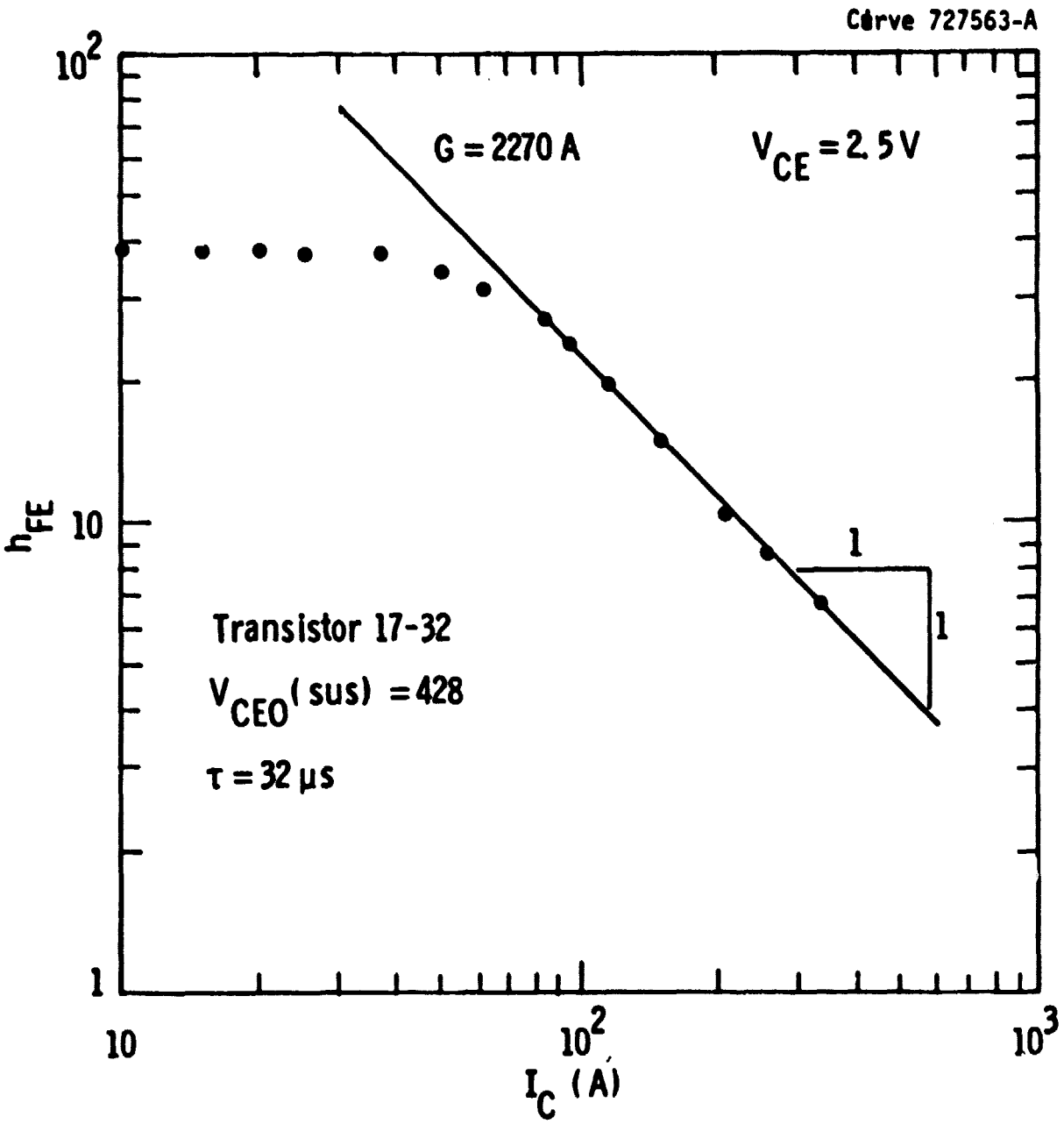


Figure 16 - Current gain vs. collector current for the transistor of Figure 15

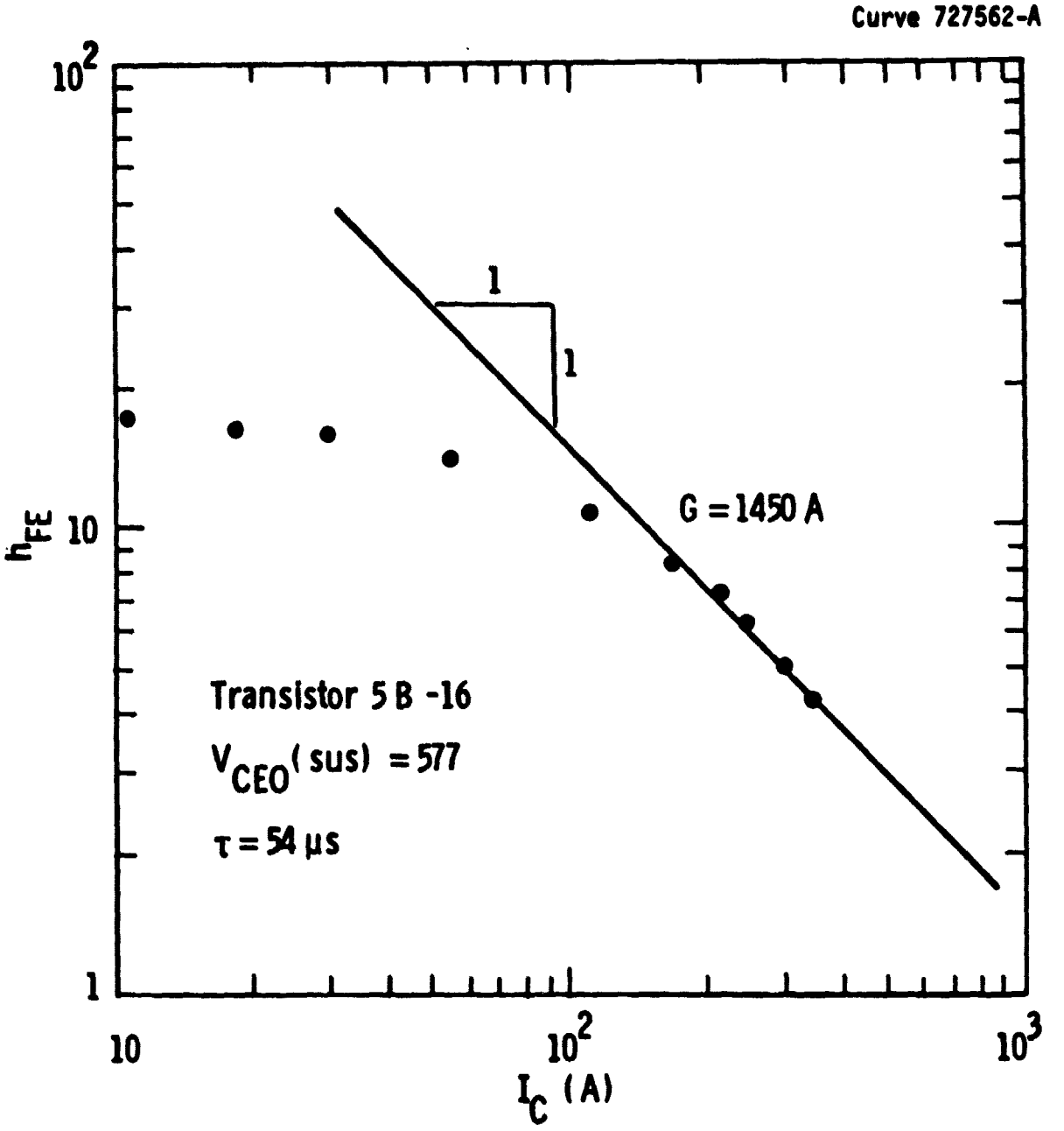


Figure 17 - Current gain vs. collector current for a V_{CEO}(sus) = 577V transistor

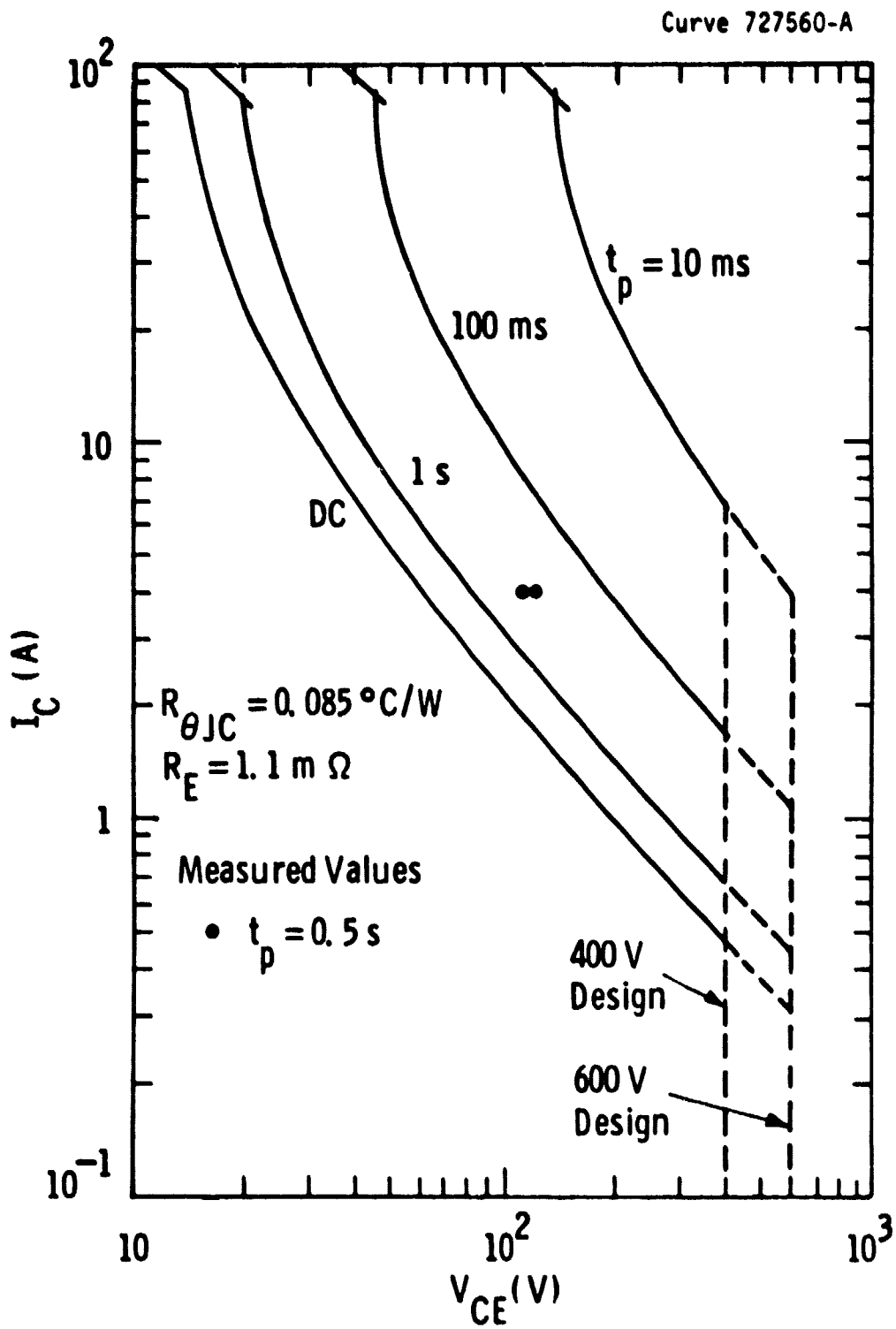


Figure 18 -- Forward safe-operating area for the 33-mm high-current transistor (Designated Model D70)

unstable mode for some time before it reaches second breakdown, these predictions will be conservative for short pulse times, e.g., $t_p \gtrsim 1$ ms.

Also shown in Fiugre 18 are measurements of the onset of thermal instability for two transistors. Second breakdown was observed to follow thermal instability in both cases, i.e., no stable hot spots formed. Measurements for both devices agree well with theory.

4.2.3 Switching Measurements

Most switching measurements were confined to the turn-off interval under clamped inductive-load conditions. The test circuit used is shown in Figure 19. The base drive consists of widely spaced pulse trains which permit steady-state conditions to be reached in the inductor but with low average power. In this way both turn-on and turn-off losses can be measured with only negligible device heating.[5]

Figure 20 shows a typical set of waveforms for the turn-off interval. The analog integration technique shown in Figure 21 is used[5] to obtain E_{OFF}, which is the area under the instantaneous power curve shown in the middle photograph of Figure 20. A similar procedure can be used to measure the turn-on energy loss E_{ON}.

E_{OFF} data are shown in Figure 22 for two different peak voltages, v_{CE}. The integration time t_g is 1 μs and has only a relatively weak influence on the data for $t_g \gtrsim 1$ μs. The influence of reverse base drive is shown in Figure 23. Using the method of Reference 5, this data can be used to predict maximum switching volt-amperes vs. switching frequency.

Dwg. 6439A26

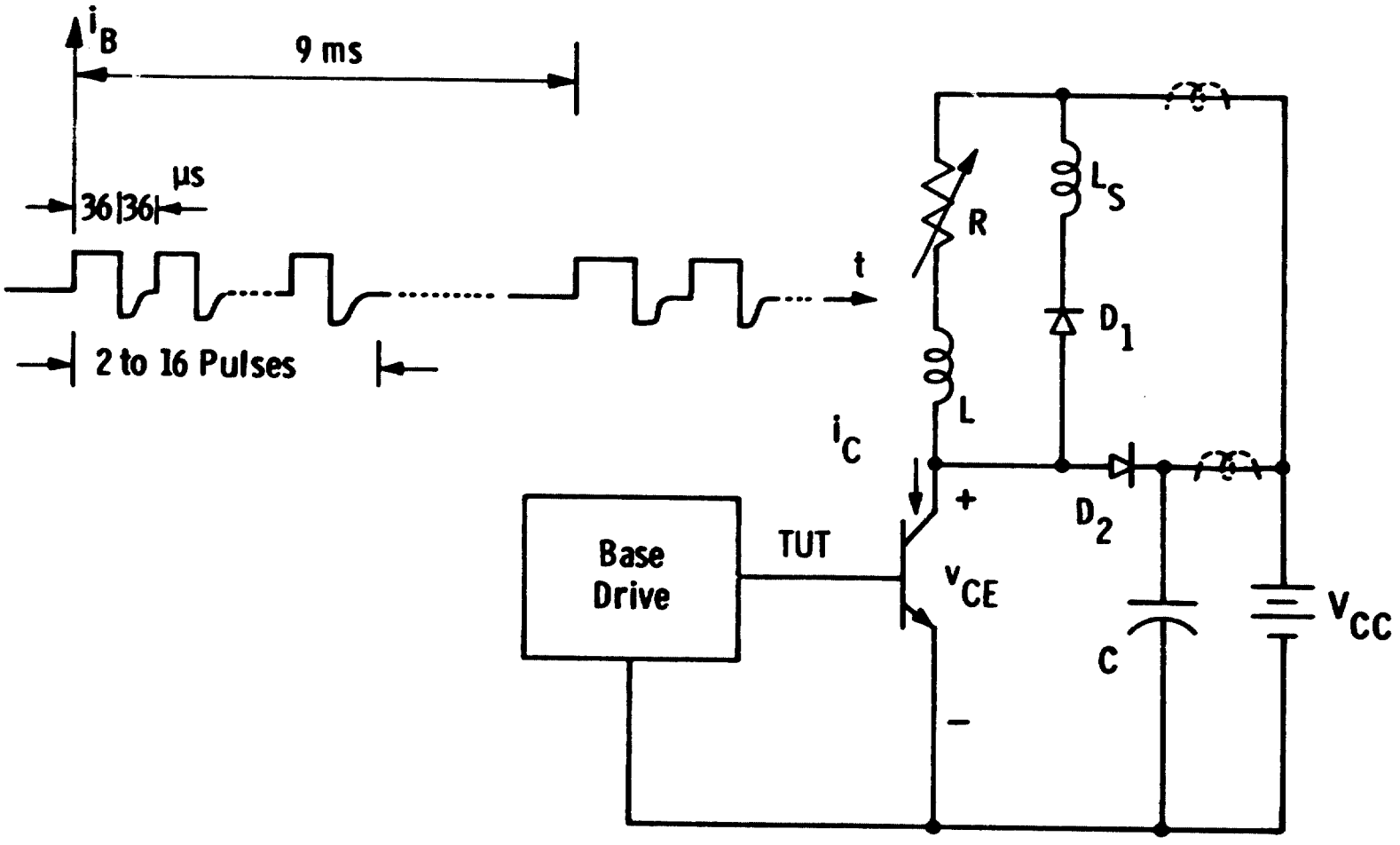
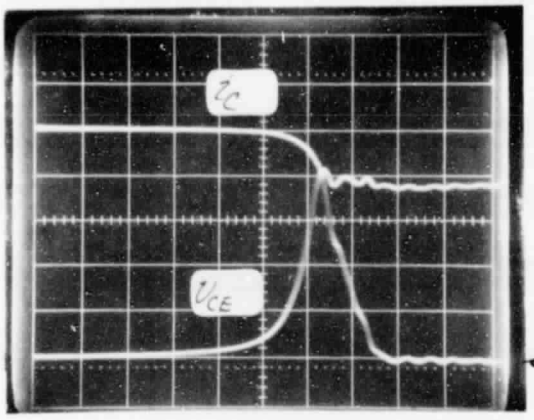


Figure 19 - Test circuit used for switching-performance evaluation

Ⓥ Transistor - Test Data - Inductive Switching

Date 5·6·80

Device 58-3



v_{CE} = 0 →

← i_C = 0

v_{CE} 100 V/d

i_C 20 A/d

p — kW/d

t 0.2 µs/d

T_C = 26.5 °C

V_{CC} = 350 V

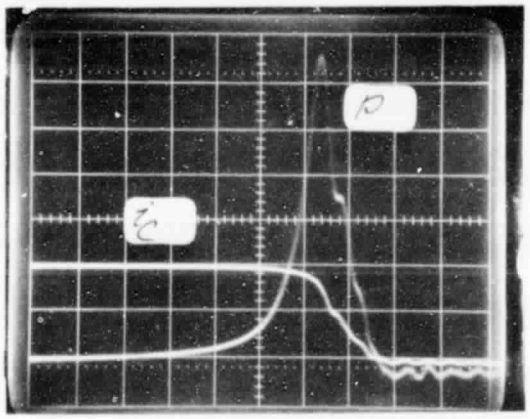
I_C = 100 A

I_{BF} = 20 A

I_{BR} = 10 A

L = 280 µH

L_s = 1.5 µH



i_C = 0
&
p = 0 →

v_{CE} 100 V/d

i_C 50 A/d

p 5 kW/d

t 0.2 µs/d

i_B ____ A/d

v_{BE} ____ V/d

V_{int} ____ V

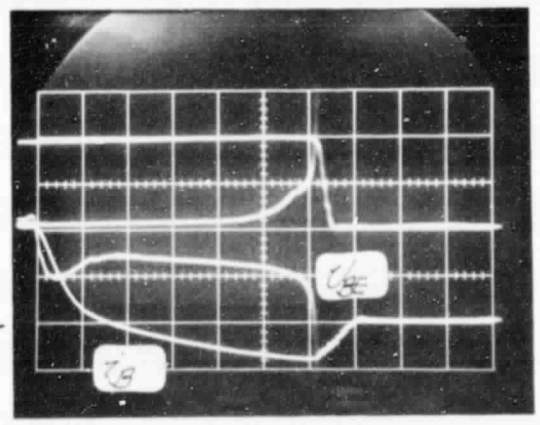
SF ____ kW/D

t_g ____ µs

E_{OFF} ____ mJ*

E_{ON} ____ mJ*

t_s ____ µs



v_{BE} = 0 →

i_B = 0 ←

v_{CE} 5 V/d

i_C 50 A/d

p ____ kW/d

t 1 µs/d

i_B 10 A/d

v_{BE} 1 V/d

*E = $\frac{V_{int} \cdot SF \cdot t_g}{10}$

Figure 20 - Turn-off waveform data

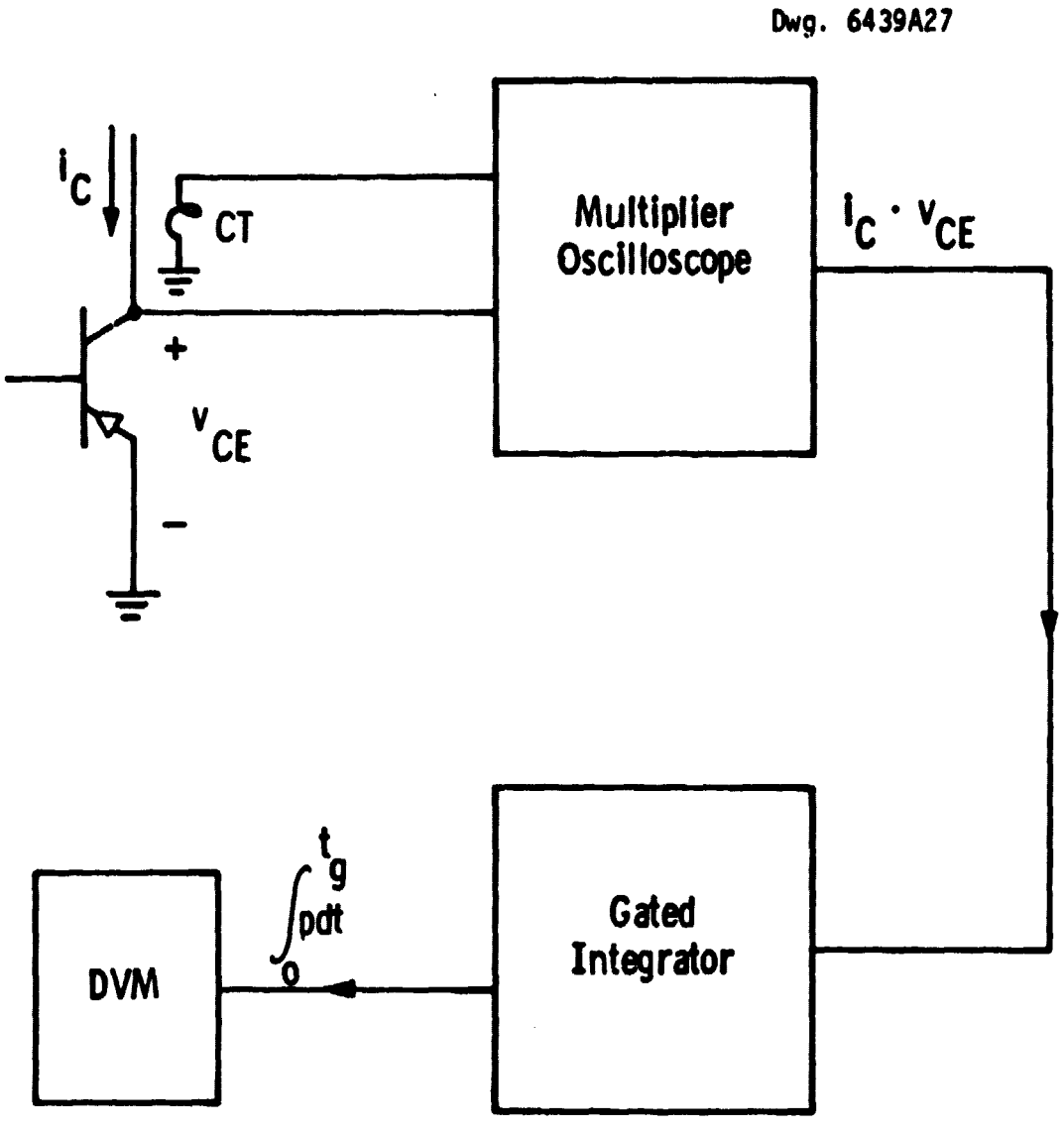


Figure 21 - Block diagram for energy loss measu: ent

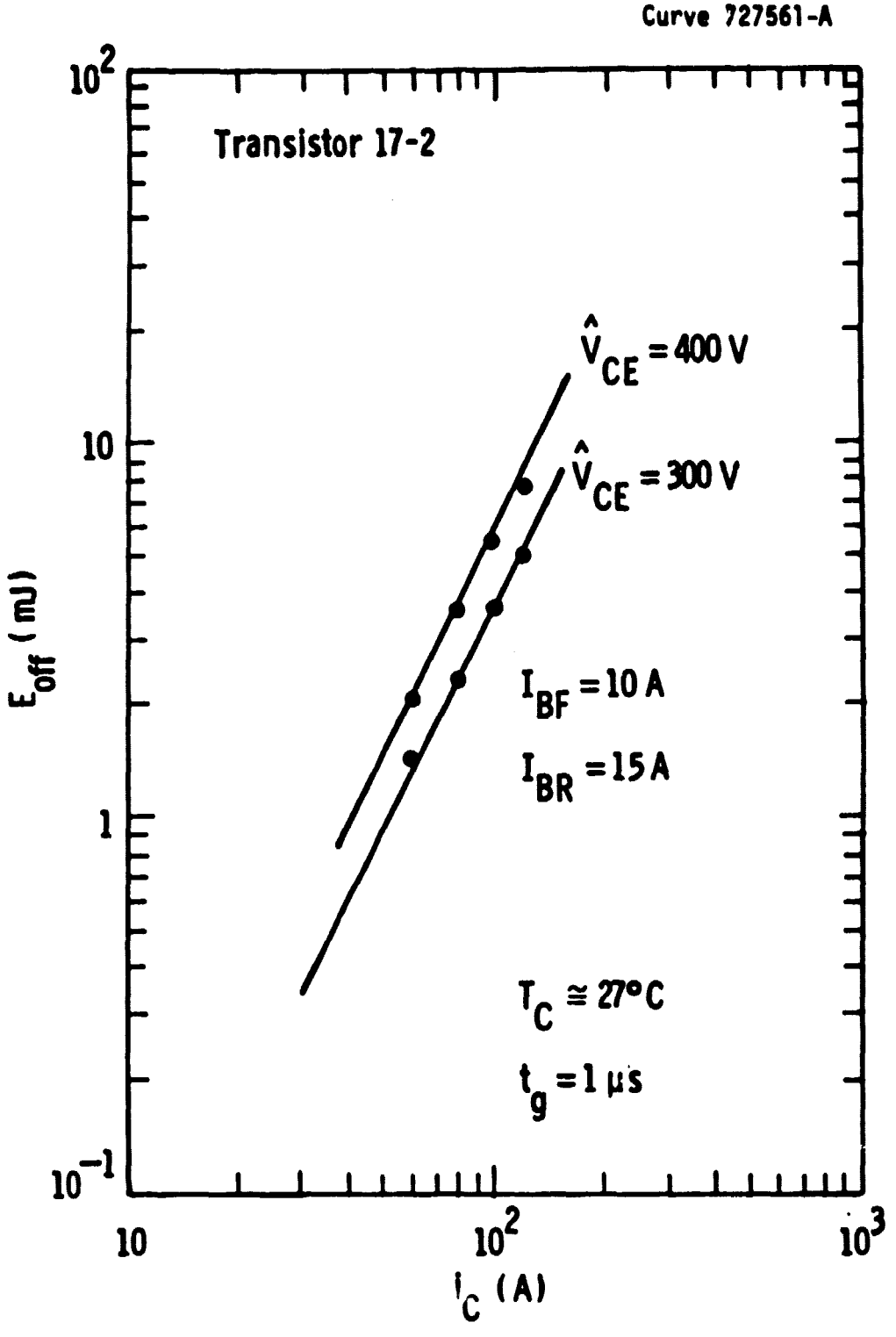


Figure 22 - Turn-off energy vs. peak-collector current for two values of peak-collector emitter voltage

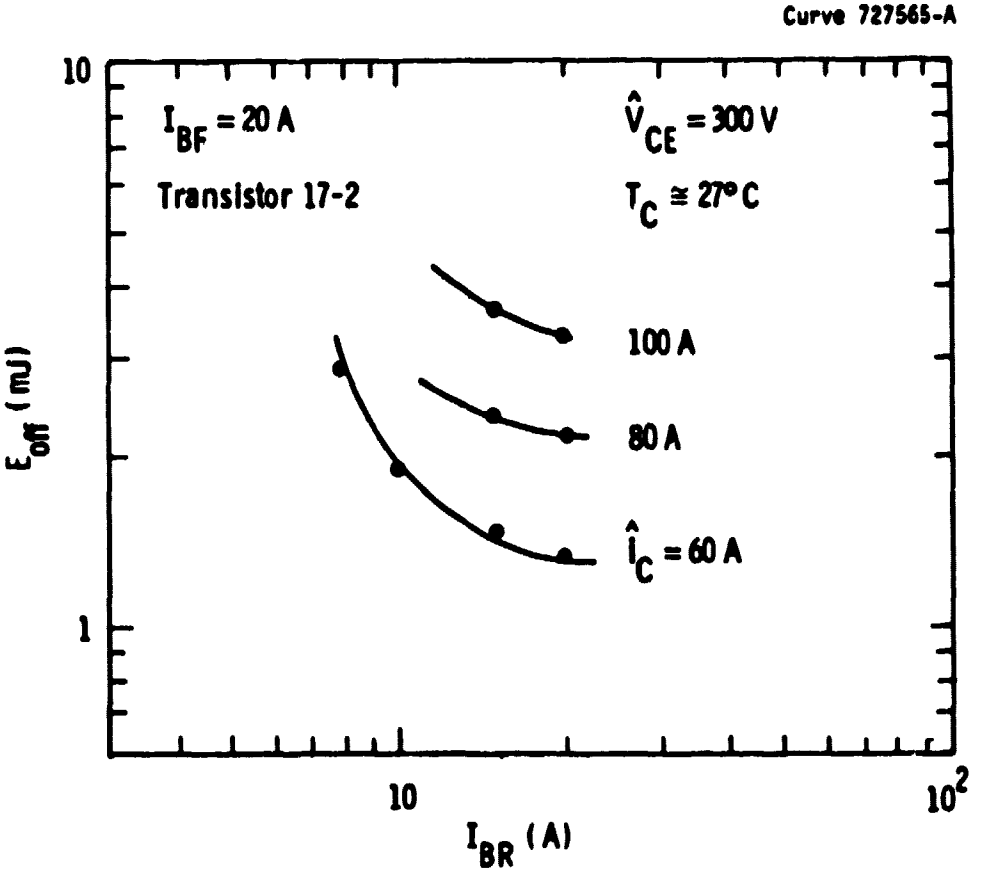


Figure 23 - Turn-off energy vs. reverse-base current for three different peak-collector currents

5.0 DESIGN FORECAST FOR 50-MM AND TARGET TRANSISTORS

While there are many engineering problems to be solved in realizing transistors of increased current and voltage, the performance that can be predicted for a transistor of 50-mm size is given below.

Design specifications have been determined to allow for an effective emitter area of approximately 6.0 cm^2 and a sustaining voltage in the 400V to 600V range. The optimum design values for the 600V device are shown in Figure 24 with an overall fusion diameter of 50 mm (allowance is made for current crowding). Using the output results of this analysis, the h_{FE} vs I_C curves for both sustaining voltages are shown in Figure 25. It can be seen that the h_{FE} I_C asymtote has a value > 6000A for the 400V device and a value > 2000 for the 600V unit. This device can be mounted into an existing 50-mm package which has been developed under a Westinghouse program for use on thyristors.

```
                New Input Data

VCE=   2.5 V              IC = 250.0 A
VCEO(sus)=   600.0 V      HFE=  10.0
TJ=    25.0 DEG C         τ=  50.0 μs
DC= 23.0 cm^2/s           ΔE=  .050 eV

At ref temp the program uses
μCO( 25.0 C)= 1300.0 cm^2/V-s
Ge= 7.48E+013 cm^-4-s

At TJ these values apply
μCO( 25.0 C)= 1300.0 cm^2/V-s
Ge= 7.48E+013 cm^-4-
-
                Optimum Design

AE= 6.08E+000 cm^2        hFEO=  26.0

NC=8.86E+013 cm^-3          m=   .600

WC=  69.0 μm          BVCBO= 1228 V
Rho.C=   54.3 ohm-cm   τ=  50.0μs
```

Figure 24 - Input and output parameters for 600 V design

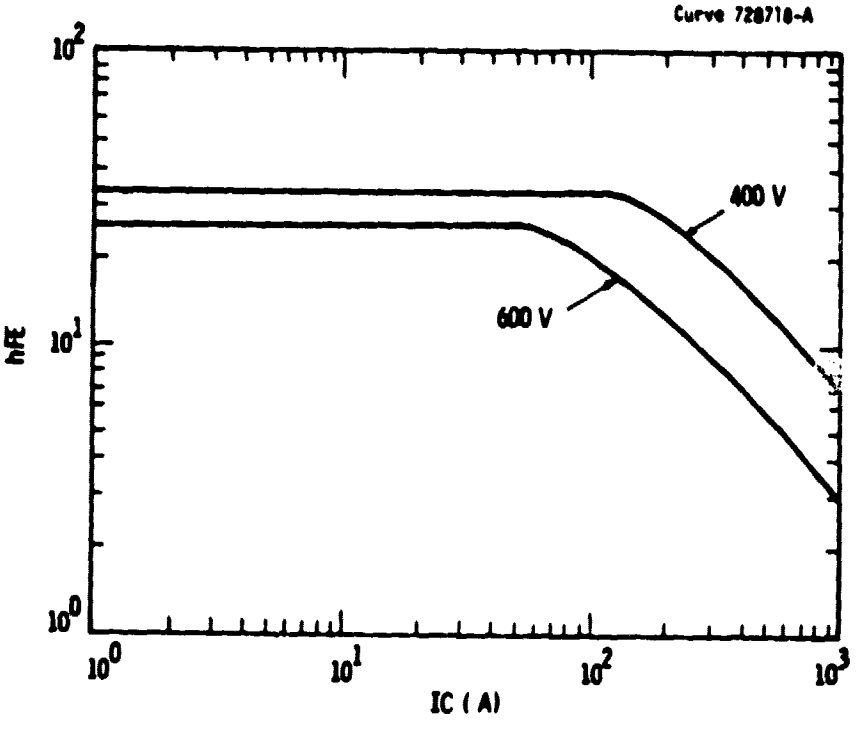


Figure 25 - Gain vs collector current

6. CONCLUSION

A viable design has been made of a high-current, large-area transistor able to operate at a $V_{CEO}(sus)$ in the range of 400V to 600V and an I_c of 170 amperes at an h_{FE} of 10. In carrying out this work a number of problems have been solved which deal with the operation of the transistor at very high base currents. The analysis takes into account the influence of the base-contact metallization as it affects the collector-current distribution in the emitter. The base-emitter voltage drop at high currents along the base contact has been defined, modeled, and a viable solution demonstrated. Since most of the drop is along the trunk of the base contact, a base insert has been used to equalize the base-emitter voltage at high currents. This makes it possible to scale-up to large wafer sizes with power-handling capability of several hundred KVA. An improved emitter-contact preform which effectively increases the silicon area will also allow for lower conduction losses in these larger sizes.

The results of these improvements can be extended to future device possibilities such as the 50-mm size unit described in Section 5. This unit would allow gain-current products of 4500A for a $V_{CEO}(sus)$ voltage of 400V and slightly lower for the 600V range. A reliable, fast-switching bipolar transistor of increased current should make it possible to meet the requirements for new space-power conversion applications, for motor control applications in the traction and vehicle industry for fast, high-current solar array switching, and for variable-speed, constant-frequency conductors for aircraft electrical systems.

The work has been very successful. The transistors that have been made represent the highest switching product with fall times in the submicrosecond range. Fifty devices have been delivered which meet the goals for the proposed device and can be used for various new applications.

7. REFERENCES

1. P. L. Hower, "Optimum Design of Power Transistor Switches," IEEE Trans. on Electron Dev., ED-20, pp. 426-435, April 1973.

2. P. L. Hower, "Influence of Collector Recombination Lifetime on the Current Gain and Storage Time of High Voltage Power Transistors," Lifetime Factors in Silicon, pp. 29-46, American Society for Testing and Materials, 1980.

3. P. L. Hower and C. K. Chu, "Development and Fabrication of Improved Power Transistor Switches," Report No. CR-159524, NASA Lewis Research Center, Contract NAS3-18916.

4. P. L. Hower and W. G. Einthoven, "Emitter Current Crowding in High-Voltage Transistors, IEEE Trans. on Electron Dev., ED-25, pp. 465-471, April 1978.

5. P. L. Hower, J. B. Brewster, and M. Morozowich, "A New Method of Characterizing the Switching Performance of Power Transistors," IEEE Ind. App. Soc. Conf. Record, pp. 1044-1049, 1978.

APPENDIX 1

Target Specifications for High-Current, Fast-Switching Power Transistors

Table 2 — Electrical Characteristics

Symbol	Characteristics with Test Conditions	RFP Value	Proposed Value	Units
$V_{CEO}(sus)$	Collector-emitter Sustaining Voltage at I_C = 200 mA, I_B = 0, 300μs pulse	400 600	400 min 600 max	V V
V_{CBO}	Collector-base Voltage at I_C = 200 m	$\geq V_{CEO}(sus)$	$\geq V_{CEO}(sus)$	V
$h_{FE}I_C$	Max Gain-collector Current Product at V_{CE} = 2.5 V			
	• $V_{CEO}(sus)$ = 400 V	1700	1700	A
	• $V_{CEO}(sus)$ = 600 V	1200	1200	A
I_B	Max Base Current			
	• Pulsed (<2% duty cycle)	100	150	A
	• Continuous dc	50	75	A
$I_C(peak)$	Max Collector Current, pulsed at V_{CE} = 2.5 V			
	• $V_{CEO}(sus)$ = 400 V	500	500	A
	• $V_{CEO}(sus)$ = 600 V	350	350	A
$I_C(continuous)$	Max Collector Current, continuous at V_{CE} = 2.5 V			
	• $V_{CEO}(sus)$ = 400 V	340	340	A
	• $V_{CEO}(sus)$ = 600 V	250	250	A
h_{FE}	Direct current gain for $V_{CEO}(sus)$=400V			
	• I_C = 100 A, V_{CE}=2.5V	17	17	
	• I_C = 250 A, V_{CE}=2.5V	6	6	
h_{FE}	Direct current gain for $V_{CEO}(sus)$=600V			
	• I_C= 100 A, V_{CE} =2.5V	12	12	
	• I_C= 250 A, V_{CE} =2.5V	5	5	
$V_{CE}(sat)$	Collector-emitter Saturation Voltage at I_C = 100 A, I_B = 10A	1.0	1.0	V
$V_{BE}(sat)$	Base-emitter Saturation Voltage at I_C = 100 A, I_B = 10A	1.3	1.3	V
RθJC	Thermal Resistance Junction to Case	0.1	0.1	°C/W
P_T	Power Dissipation at Case Temp, T_C=75°C	1250	1250	W
T_J	Operating and Storage Junction Temp. Range	-40 to 200	-40 to 200	°C
t_D*	Turn-on Delay	0.1	0.1	μs
t_r*	Rise Time (10 to 90% I_C)	0.5	0.4	μs
t_s*	Storage Time	2.5	2.5	μs
t_f*	Fall Time (90 to 10% I_C)	0.5	0.3	μs

*All switching times measured with resistive load, supply voltage, V_{CC}=200V, I_C=100A, I_{B1}= $-I_{B2}$=10A using 100 μs pulses with duty cycle <2%.

APPENDIX 2

Data Summary for Devices Shipped Under this Contract

All measurements are at approximately 25°C. $V_{CEO}(sus)$ is measured at 200 mA using an inductive turn-off circuit with L=25 mH. G is based on h_{FE} vs. I_C data at V_{CE} = 2.5 V Lifetime values are open-circuit-decay measurements of the base-collector junction.

Data Summary

Device	V_{CEO}(sus) (v)	G (A)	V_{CBO}/I_C (v/mA)	V_{EBO}/I_E (v/mA)	h_{FEO} -	T (μs)	$G_E/10^{13}$ (cm^{-4}-s)
5B-3	580	1050	701/.5	G	17	18	
5	576	1300	700/.5	5/30	20	50	
11	562	1400	590/.5	G	20	24	
12	557	1600	700/.5	G	19	62	
13	546	1500	720/.5	G	20	33	
15	556	1350	750/.5	5/30	20	14	
17	495	1620	375/.5	G	21	41	
18	576	1500	680/.5	G	20	60	
19	576	1680	700/.5	G	16	60	
21	558	1620	703/.5	5/30	24	43	
36	604	1740	760/.5	3/30	21	49	
37	604	1570	730/.5	4/30	22	43	
38	583	1680	730/.15	2/30	19	50	
39	607	1350	700/.5	3/30	20	25	
40	551	2450	710/.5	3/30	28	44	
41	561	1460	700/1	4/30	26	34	
42	689	1460	720/.5	2/30	18	46	
43	589	1510	600/1.5	3/30	23	39	
44	543	1510	500/1.5	3/30	22	30	
5B-45	540	1510	700/1.5	2/30	22	46	
8-3	529	1080	640/5	9/30	19	24	
9	582	1050	790/1	3/30	21	19	
11	575	881	820/1	8/30	15	18	
12	553	990	830/1	8/30	17	10	
14	534	1352	800/1	8.5/30	20	28	6.41
15	561	1060	820/.5	8.5/30	16	24	6.76
18	553	950	840/.5	9.5/30	20	19	6.80
19	565	1250	825/.5	9/30	16	24	7.29
8-22	562	1080	790/.5	9/30	16	27	6.18

Notes: (1) G denotes $I_E \geq 30$ mA @ 7V

Data Summary

Device	V_{CEO}(sus) (v)	G (A)	B_{CBO}/I_C (v/mA)	V_{EBO}/I_E (v/mA)	h_{FEO} -	T (μs)	$G_E/10^{13}$ (cm^{-4}-s)
8-23	587	1050	750/.5	9/30	18	28	
8-24	545	1260	750/.5	8/30	17	25	7.35
7-5	473	1600	700/1	10/1	39	40	
7-9	466	1300	700/1	7/1	26	13	
7-13B	479	1400	680/1	7/20	39	33	
U1	429	2050	720/1	7/30	44	28	
17-2	429	2230	500/2.5	G	37	44	
6	454	2300	645/1	G	42	32	
8	454	1900	670/1	6/30	38	32	
9	460	1730	640/2.5	G	36	20	
12	463	1920	680/2.5	G	39	38	
14	499	1570	680/1	G	35	30	
17	465	1780	620/2.5	G	35	44	
18	450	1930	645/1	G	35	50	
22	444	2600	680/1	G	40	38	
32	428	2250	435/5	G	40	32	
35	438	2010	430/5	6/30			
37	410	1570	640/1	G	34	31	
40	445	1460	450/5	5/30	28	31	
41	415	2500	580/2.5	G	44	36	
43	459	1650	620/5	G	32	27	