RAD HARD PROM
DESIGN STUDY

Third Interim Report

July 1981

MEC-81-076-R

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1. INTRODUCTION

This report presents the results of a preliminary study on the design of a rad hard fusible link PROM. The study began by surveying the various fuse technologies and the effects of radiation on MOS integrated circuits. Based on that information, a set of design rules was defined which will allow the fabrication of a rad hard PROM using a Si-gate CMOS process. A preliminary cell layout was completed and the programming concept defined. A block diagram is used to describe the circuit components required for a 4K design. Finally a design goal data sheet was generated giving target values for the AC, DC, and radiation parameters of the circuit.

II. SURVEY OF FUSE TECHNOLOGIES AND DESIGN APPROACHES USED IN PROGRAMMABLE ROM'S

Fuse Technologies

Fusible link PROM's are typically fabricated with either NiCr, TiW or polysilicon fuses. Each material has advantages and is used by one or more manufacturers in currently available parts.

The earliest bipolar PROM's used a NiCr fuse technology and, as a result, this fuse material has been studied extensively. Much of this research has been directed toward understanding a failure mode which causes programmed fuses to relink. This phenomena, known as "growback," is the result of a field induced mechanism where metal dendrite formation occurs in the gap region of the blown fuse. It has been shown (1) that fuses which are blown by relatively slow risetime, low level programming pulses have some residual NiCr in the gap and exhibit a higher probability of relinking under high stress conditions. This same study concludes that "growback" is not a significant long term reliability problem provided that, after programming, the devices receive a dynamic burn-in at maximum temperature and V_{CC}, followed by a functional test. Fairchild, Signetics, Harris and Motorola continue to use NiCr fuses for their bipolar PROM's.

Due to the potential reliability problem associated with NiCr, several PROM manufacturers have switched to a TiW technology for their newer designs. TiW doesn't exhibit the "growback" phenomena and it provides several additional advantages with little process modification. Since the fuse resistance is lower, typically 40Ω versus 300Ω for a NiCr fuse, the TiW parts are faster and programming voltages can be reduced. The Schottky process used to fabricate most bipolar PROM's incorporates a TiW layer as a diffusion barrier between the Al metallization and the Platinum Silicide Schottky, therefore the use of TiW fuses requires only minor process changes. Monolithic Memories, National Semiconductor, and Texas Instruments replace the NiCr link with a TiW fuse.

Polysilicon is another fuse technology which has proven to be highly reliable and free of any growback effects (2). N-doped poly is typically used and is deposited with standard Si-gate MOS processing techniques. This technology is well defined and allows very close control over the critical fuse dimensions. Another advantage of this technology is the ability to vary the fuse resistance by doping the polysilicon. This allows the designer a degree of freedom not easily obtainable with metal fuses. Even though polysilicon is not normally available in a bipolar process, some manufacturers such as Intel and AMD have felt that it's benefits justify the increased processing complexity that it's use requires. The Harris 6611 and 6641 are the only MOS fusible link PROM's currently available and they both incorporate poly fuses.

Polysilicon Fuse Design

After studying the various fuse technologies, polysilicon appears to be the best fuse material for the fabrication of a rad-hard CMOS PROM. Several Rad-hard Si-gate processes exist which could accommodate poly fuses without process modification. One is the 4μ Si-gate CMOS process developed by Sandia National Labs.

When designing a fusible link PROM, the most challenging task is the design of a fuse which can be easily blown by the programming circuitry, yet withstand worst case read current levels. This job is simplified if the programming current level and the read current level are made significantly different. Typically, this ratio is at least 10:1. After a programming current is defined, it is necessary to size the fuse so that it will open consistently at a current slightly below this level. A theoretical analysis indicates that the current necessary to blow the fuse is proportional to the square root of the fuse width, therefore tight control over the fuse width is necessary to insure acceptable programming yield and reliable operation.

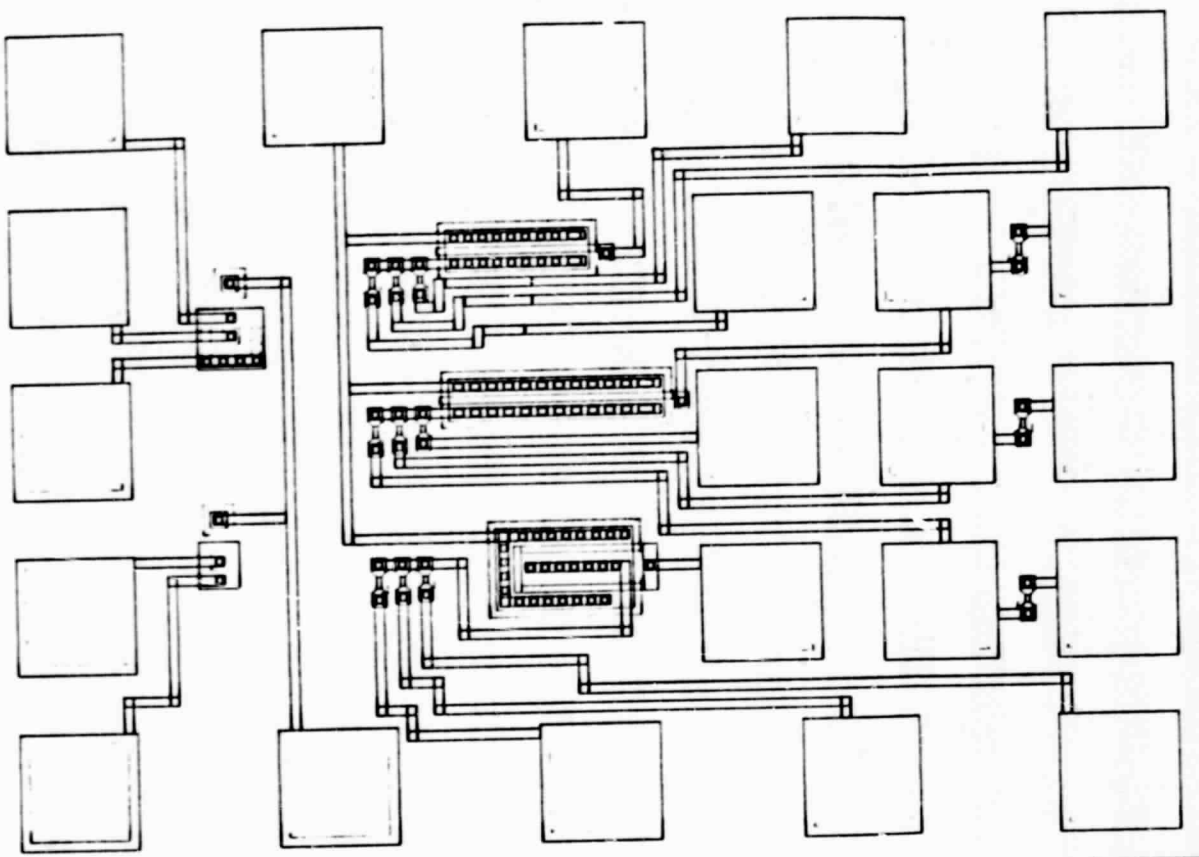
Another consideration in the fuse design is the choice of fuse resistance. In this case, an engineering tradeoff must be made in order to achieve optimum circuit operation. Since the fuse resistance contributes to the bit line RC time constant, it is desirable to keep this resistance as low as possible insuring fast operation. However, a low fuse resistance will increase the size of the memory cell and programming circuit due to the requirement that the impedance of the programming circuit match that of the fuse. This insures maximum power transfer during programming.

In the preparation of this report, both Intel and Harris poly fuse PROM's were studied. The data on Intel fuses was obtained from published papers (2, 3) while the Harris data came from measurements of actual parts. Intel fuses are fabricated from an N-type polysilicon layer, 3400 Å thick, which is doped to match the programming circuit impedance. The width of the fuse notch is targeted at 2.2μ and is designed to blow within 1μs with a 30 mA programming pulse. The sense current for these fuses is 2 mA nominally. Intel reports (2) that the actual fuse widths follow a Gaussian distribution with 99.99% of the fuses greater than 1μ in width. Fuses greater than .3μ wide were proven to be stable at the 2 mA sense current. Harris Semiconductor has two CMOS PROM's on the market, the 256x4 6611 and the 512x8 6641. The polysilicon fuses used for these devices were measured to be 1.6x7μ for the 6611 and 2x7μ for the 6641. Programming current data was not available but these values will be measured at a later time.

In studying the Intel and Harris PROM's, it was discovered that both manufacturers remove the passivation glass from the fuse area. Empirically, it was determined (2) that a more complete and easier burnout could be accomplished by the presence of O_2. In addition, removal of the P-glass allows the fuse to change shape as it opens. This lack of passivation poses no reliability problems since all junctions remain covered with only the unprogrammed fuses exposed.

MEC Fuse Test Circuit

To supplement the information gained from studying Intel and Harris PROM's, a fuse test circuit was included on a test chip being processed by Sandia Labs. This circuit, laid out using Sandia's 4μ RAD hard CMOS process, will provide empirical data on the relationship between fuse size and programming current. Three fuse sizes and three access transistor sizes were included along with two bipolar devices. A plot of this test circuit is included on the following page.



NOTES:

1. LEVEL 1 (P-WELL) IS COLORED BROWN.
2. LEVEL 3 (THIN OXIDE) IS COLORED RED.
3. LEVEL 4 (POLYSILICON) IS COLORED BLUE.
4. LEVEL 5 (N+ [illegible]) IS COLORED [illegible].
5. LEVEL 6 (P+ IMPLANT) IS COLORED BLUE VIOLET.
6. LEVEL 7 (CONTACTS) ARE COLORED BROWN.
7. LEVEL 8 (METAL) IS COLORED BLACK.
8. [illegible]

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SCALE: 500/1

DRAWN BY: EWC

REVISED:

TITLE: FUSE PROGRAMMABILITY TEST CIRCUIT

DATE: 07-09-81

APPROVED BY:

SIZE: B

DRAWING NUMBER:

III. RADIATION EFFECTS STUDY

Radiation Hardened Device Design

The process modifications used to produce radiation tolerant CMOS circuits typcally concentrate on minimizing threshold voltage shifts and preventing latchup. Relatively minor process changes can yield an order of magnitude improvement in the radiation hardness of standard circuits, however for operation at 10^6 rad levels, special circuit techniques must be employed as well.

When an MOS device is exposed to ionizing radiation some electrons in the gate oxide gain enough energy to break away from their atoms and be swept away by the applied gate potential. This causes a net positive charge to accumulate in the oxide and a shift in the n and p channel thresholds toward more negative voltages. In a standard CMOS process, V_{tn} can become negative and $|V_{tp}|$ can exceed the power supply voltage after high radiation doses. Rad hard processes control charge build up in the oxide to prevent these large threshold shifts and the resultant circuit failure.

Studies have shown the factors having the greatest impact on positive charge build up are the oxide thickness and its method of growth (4). The oxide thickness relationship is particularly significant since the threshold shift is a cubic function of thickness. For this reason, rad hard processes use a gate oxide thickness of approximately 500 Å rather than the 750 Å typically used in a standard process. The oxide growth method used in most rad hard processes is a dry oxidation at 1000°C. Empirically this has been determined to yield the hardest oxides (4).

In addition to the process changes just discussed, two commonly used techniques have been found to degrade radiation hardened oxides and are therefore avoided. These are high temperature (>925°C) anneals and E-beam aluminum depositions. Lower temperature anneals and thermally evaporated aluminum are used instead.

While threshold voltage shifts increase gradually with total radiation dose, a more serious problem can occur under high dose rate conditions. Radiation induced photocurrents can cause the parasitic PNPN device, inherent in bulk CMOS structures, to latch up allowing large currents to flow between the supplies. This can be prevented by reducing the maximum parasitic transistor gain product, $\beta_{pnp}\beta_{npn}$, to less than unity. Generally rad hard processes accomplish this by limiting minority carrier lifetimes with gold doping.

Layout changes can also improve the radiation hardness of CMOS devices. One common change is the addition of p^+ guard rings around the n-channel transistors. This insures that the channel of the n-type device stops within the p-well and doesn't short to the n-type substrate. Layouts with no guard bands require the p-well concentration to be higher with an increase in V_{tn} as a result. Another layout rule which improves rad hardness is the requirement for frequent V_{ss} tie downs of the p-well and guard band. This prevents voltage drops across the p-well under high photocurrent conditions. These voltage drops are a necessary condition for latchup to occur.

B. Design Concepts for Radiation Hardened CMOS Circuits

Process and layout changes can reduce the effect of radiation on CMOS devices but circuits designed to operate at high dose levels must still allow for significant parameter variations. For example, p-channel threshold shifts are approximately -4V at 10^6 RADS, even for a rad hard process. In general, rad hard circuits should be designed to track parameter variations rather than depending on the absolute value of those parameters. One example is the use of differential sense circuits rather than simple inverter sense amps.

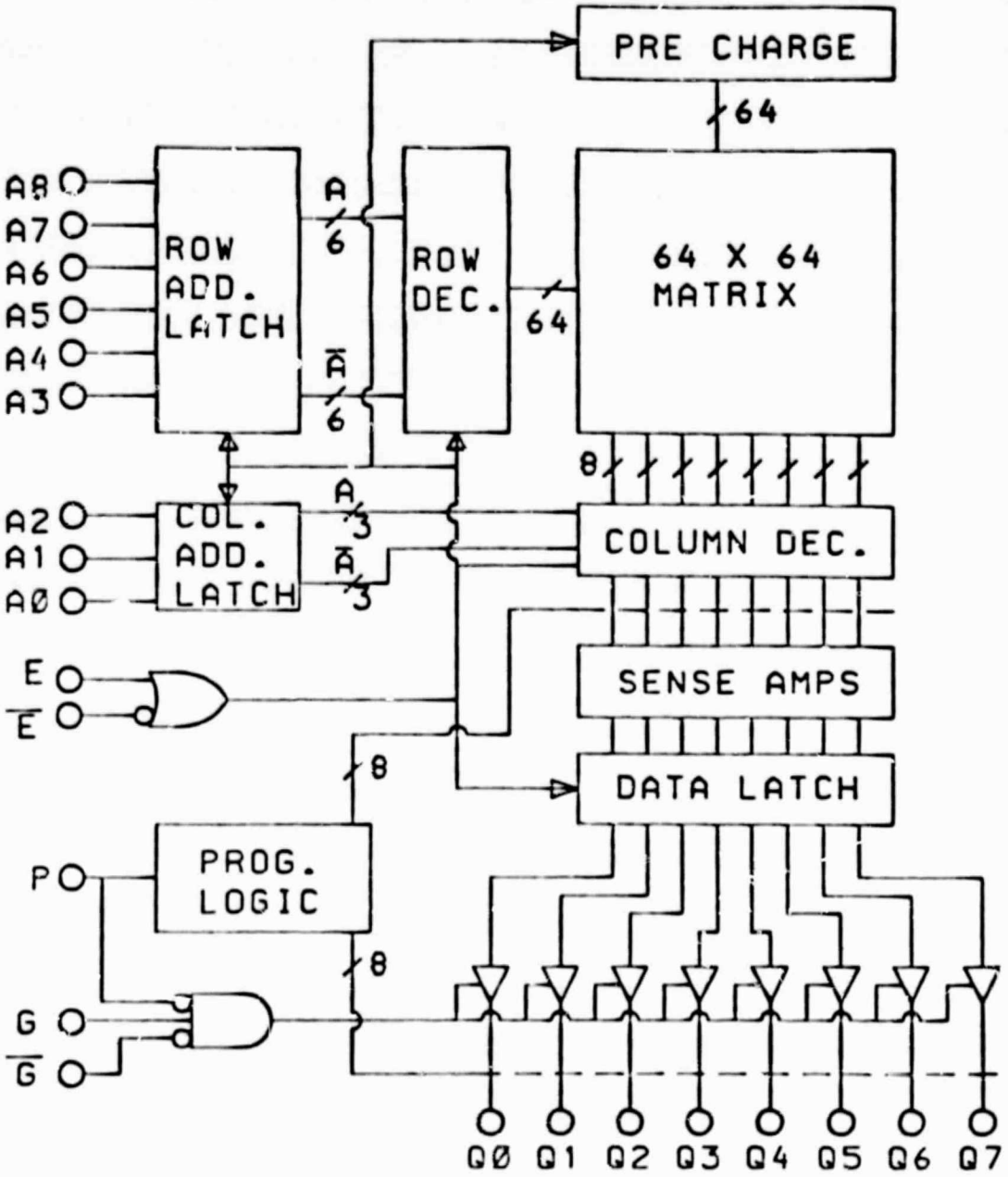
Another consideration is the relative performance of individual devices. Devices which perform poorly after radiation should be enlarged or compensated in some manner. Since the p-channel device loses a great deal

of drive due to its large threshold shift, it will not be very effective after irradiation at pulling a node to the plus supply. For this reason, circuits which precharge lines high will experience less speed degradation after irradiation.

One aspect that is particularly important in the design of a rad hard memory is signal timing. If care isn't taken, signal transistions may occur out of sequence after irradition. To prevent this from occurring, circuit operation should be carefully simulated with both pre- and post-irradiation device parameters.

IV. PROPOSED FUNCTIONAL BLOCK DIAGRAM

A block diagram for the proposed radiation hardened PROM is included on the following page. This diagram indicates the circuits necessary for the construction of a 4K PROM organized 512x8 with latched data and address lines and three state output buffers.



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		SCALE: NONE	DRAWN BY: EWC REVISED:
TITLE: FUNCTIONAL BLOCK DIAGRAM			
DATE: 07-09-81	APPROVED BY:	SIZE: A	DRAWING NUMBER:

V. DESIGN RULE DEFINITION

In defining the layout design rules for this PROM, the decision was made to use a guard banded process similar to Sandia Labs' 4μ Si-gate CMOS. This is a 9-level, ion implanted process incorporating all of the radiation hardening techniques described in Section III of this report. The basic design rules are shown below with the full set of rules included in the remainder of this section.

Design Rule Basic Values in Microns

	4μ M Rules
Alignment--Mask run out Feature size Misalignment	
TOTAL	2.5
Additional Alignment tolerance for indirectly aligned levels, per level of remoteness	0.5
Sideways diffusion	80% x_j
Maximum depletion region	
in substrate	4.0 (12V)
in p-well	1.5
Minimum feature size	
metal	4 x 4
polysilicon pitch in interconnect	4
contact	3 x 3
polysilicon width	3
p-well depth	6 - 7

SANDIA SILICON GATE CMOS DESIGN RULES IN MICRONS

	4μ M Rules
Minimum metal lines	4
Minimum metal space	4
Minimum polysilicon interconnect[1]	
(a) line	3
(b) space	4
(c) Gate length	3
Minimum polysilicon to oxide step[2]	2
Minimum N^+ width	4
Minimum spacing N^+ inside well; N^+ defined by:	
(a) polysilicon	4
(b) N^+ mask	4
Minimum N^+ to p^+ guard band; N^+ defined by:	
(a) thick oxide	7
(b) polysilicon	7.5
(c) N^+ mask	8
Minimum p^+ implant width	4
Minimum contact	3 x 3
Minimum contact opening to polysilicon edge:	
(a) over thin oxide	2.5
(b) over thick oxide	1.5
Minimum contact opening to non-poly defined diffusion edge inside diffused area	2
Minimum contact opening (metal to poly or diffusion) from oxide step	2
Minimum contact overlap for shorting diffusion	4
Minimum overlap to short diffused regions together	2
Minimum metal contact overlap on all sides	0.5
Minimum thick oxide width	4
Minimum thick oxide space	4
Minimum p^+ guard band width	4
Minimum p^+ drain to p^+ guard band space;	
(a) thick oxide	13
(b) polysilicon	13.5
(c) p^+ mask	14

[1]For runs of aluminum lines parallel to polysilicon lines > 120μ M, aluminum must be interdigitated line to line with polysilicon lines.

[2]Polysilicon can "dogleg" along an oxide step, straddling it for no more than 24μ M if the polysilicon is 5μ M wide.

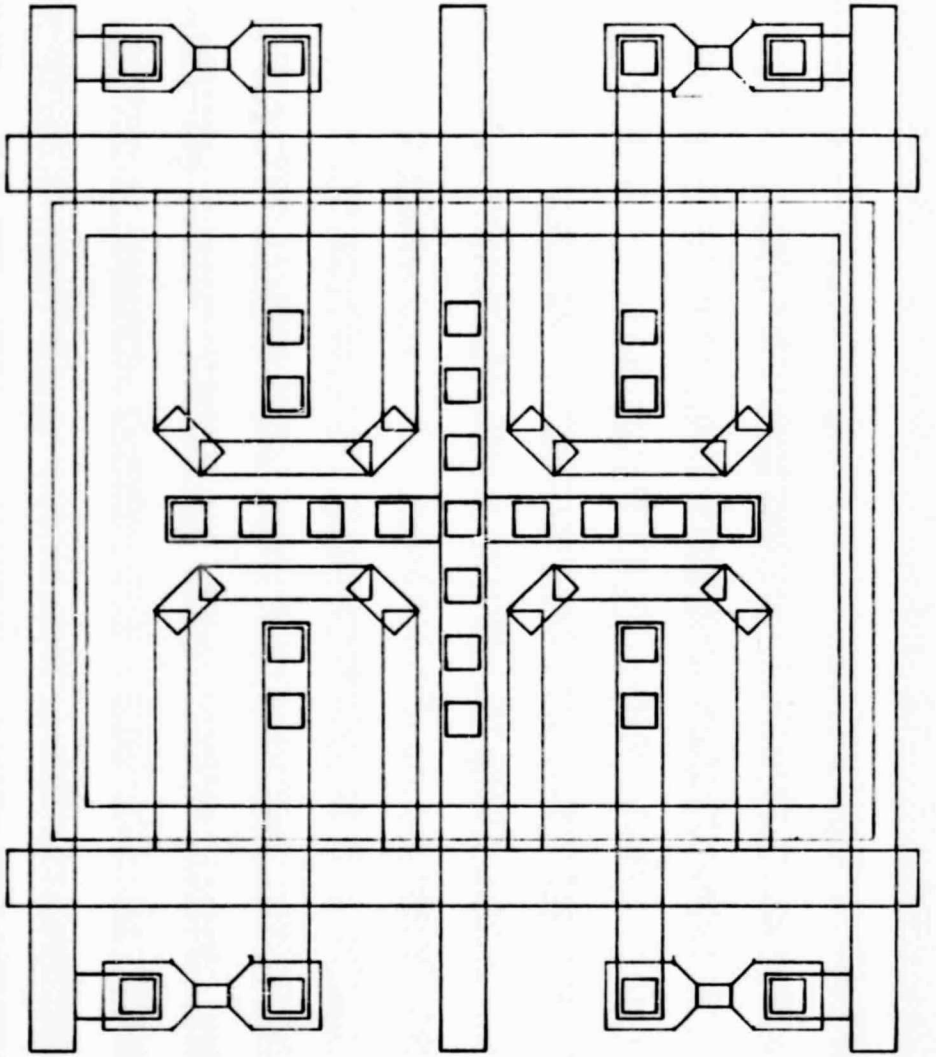
	Au M Rules
Minimum p^+ source at V_{dd} to guard band; p^+ defined by:	
(a) thick oxide	9
(b) polysilicon	9.5
(c) p^+ mask	10
Inside edge of guard band to outside p-well distance	1
Minimum thick oxide to p^+ guard band inside edge	4
Minimum polysilicon overlap outside thick oxide	4
Minimum polysilicon overlap of p^+ guard band	4
Minimum distance of edge of p^+ mask to edge of thick oxide where thick oxide defines p^+ edge	3
Minimum p-well to p^+ drain when p^+ drain defined by:	
(a) thick oxide	16
(b) polysilicon	16.5
(c) p^+ mask	17
Minimum p-well to p^+ source at V^{dd}; p^+ source defined by:	
(a) thick oxide	12
(b) polysilicon	12.5
(c) p^+ mask	13.0
Minimum contact to p^+ guard band edge	3
Minimum p-well to p-well (isolated)	19
Minimum p^+ to p^+ both sides active defined by:	
(a) same mask, non-poly	10
(b) polysilicon	4
(c) thick oxide	10
Minimum gate length of "both-sides-active" p-chan transistor	4
Minimum bonding pad to p^+	40
Minimum bonding pad to metal	40
Minimum scribe channel border to p^+ or metal	50
Minimum input pad to pad space	220
Minimum output pad to pad space, unbuffered	220
Minimum buffered output pad to pad space	320
Minimum pad size	100 x 100
Minimum protective oxide overlap of contact pad	4
Minimum V_{dd} and V_{ss} bus width	16

Mask Alignment Sequence

1 - p-well
2 - p^+ guard band (align to p-well)
3 - thick oxide opening (align to p-well)
4 - polysilicon (align to thick oxide)
5 - N^+ implant (align to polysilicon)
6 - P^+ implant (align to polysilicon)
7 - contact opening (align to polysilicon)
8 - metal (align to contact opening)
9 - protective oxide (align to metal bonding pads)

VI. PRELIMINARY MEMORY CELL DESIGN

Based on information obtained in the fuse technology study, a preliminary cell design has been completed. This cell uses a p-channel access transistor with a 20/1 aspect ratio and a poly fuse 2μ wide and 3μ long. With the supply set at 15 volts, the programming current would be approximately 15 mA. After results are obtained from the MEC fuse test circuit, a precise value for the programming current will be known and the device sizes can be finalized. This preliminary topology has been generated using the design rules specified in the previous section and occupies chip area of 40 by 47μ. This is expected to be reduced during the design phase. A checkplot of this layout is included on the following page.



NOTES:
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3. LEVEL 6 (P+ IMPLANT) IS COLORED BLUE VIOLET.
4. LEVEL 7 (CONTACTS) ARE COLORED GREEN.
5. LEVEL 8 (METAL) IS COLORED BLACK.
6. LEVEL 9 (PASSIVATION GLASS) IS COLORED RED VIOLET.

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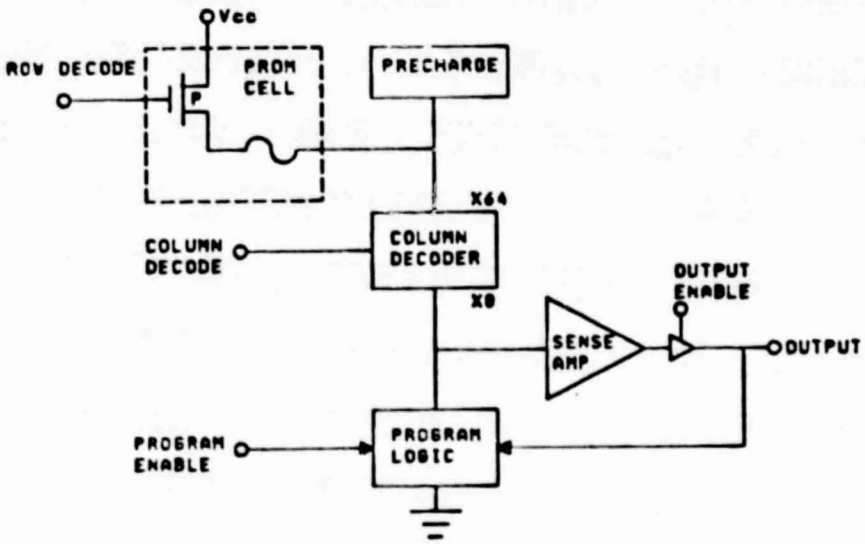
VII. PROGRAMMING TECHNIQUES AND CIRCUIT DESIGN CONCEPT

Programming Circuit Concept

A diagram depicting the programming circuitry is shown below and will be used to explain the programming concept. In a normal read operation, the accessed memory cell is connected to the sense amplifier by a transmission gate in the selected column decoder. Since the sense amp has a high input impedance, only a very small current will flow in this mode. During programming, a low impedance path to ground is provided allowing a current to flow which is large enough to blow the fuse. The programming logic provides this path only when the program enable pin is high and the appropriate output pin is low. During this time, the output buffers are tri-stated allowing the output pins to be used as data inputs.



Programming Procedure

As fabricated, all memory cells are in the logic zero state and can be selectively changed to the logic one state by the controlled application of programming potentials and pulses. During programming, a given word is addressed and the bits within that word are programmed one at a time. After an entire word has been programmed, the next word is addressed. The complete programming sequence consists of the following steps:

1. The address of the first word to be programmed is applied to the PROM and latched by the rising edge of the chip enable input.
2. The outputs are placed in the high impedance state by the falling edge of output enable (G).
3. V_{CC} is raised to the programming level of 15 volts.
4. The data output pin of the bit to be programmed is pulled low and all other outputs are pulled up to V_{CC}.
5. A 500 μs pulse is applied to the program enable pin.
6. The data output pins are allowed to float and the V_{CC} pin is returned to 10.0 volts.
7. Chip enable (E) is returned to ground.
8. A normal read cycle is performed to verify that the bit has been programmed successfully.
9. If step 8 indicates the bit has programmed normally, return to step one and program the next bit of the addressed word. If step 8 is unsuccessful, program the same bit again.
10. After all bits of the first word have been programmed, repeat 1-9 for the remaining 511 words.

VIII. CHIP SIZE ESTIMATES

Using the dimensions of the preliminary cell layout, a 4K PROM would require an area of 101x118 mils for its 64x64 cell array. Assuming typical dimensions for the remaining circuitry, the total chip size would be approximately 140x200 mils. For an 8K PROM, a different cell layout would probably be used. A longer and narrower cell, approximately 32x59 microns, would allow two 64x64 arrays to be placed side by side in an area 161 mils wide and 149 mils tall. The total chip size would now be about 200 mils square.

IX. DESIGN GOAL DATA SHEET

- The following pages contain a design goal data sheet which provides target values for supply voltages, radiation hardness levels and the typical AC and DC parameters. The IEEE/JEDEC approved specification nomenclature has been used throughout.

MICROELECTRONICS ENGINEERING CORPORATION

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

APRIL 1981

MEC-6642R

512x8 RAD HARD CMOS PROM
DESIGN GOAL DATA SHEET

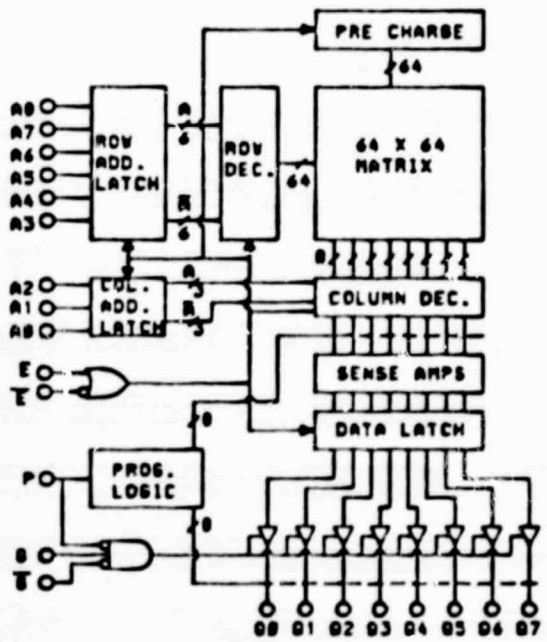
GENERAL DESCRIPTION

The MEC-6642R is a 512 x 8 radiation hardened CMOS PROM in the popular 24 pin, byte wide pinout. Polysilicon fuse links provide reliable programming and are easily implemented in the rad-hard Si-gate process. This process, in conjunction with radiation tolerant circuit techniques, allows the device to maintain its low power consumption and fast access time with a total radiation dose of up to 10^6 RADS Si. Address and data latches are provided on chip allowing simple interfacing with microprocessors which use multiplexed address and data bus structures.

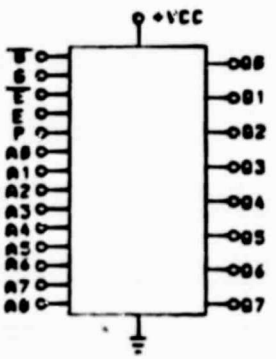
FEATURES

- FIELD PROGRAMMABLE
- RAD HARD TO 10^6 RADs SI
- POLY SI FUSE LINKS
- LOW POWER — 500 μ W MAX
- FAST ACCESS TIME — 150ns MAX PRERAD, 200ns MAX POSTRAD
- OPERATES WITH 5 TO 10 V SUPPLY
- TTL COMPATIBLE WITH 5 V SUPPLY
- PINOUT SIMILAR TO HARRIS 6641
- THREE STATE OUTPUTS
- ADDRESS AND DATA LATCHES ON CHIP
- WIDE TEMPERATURE RANGE

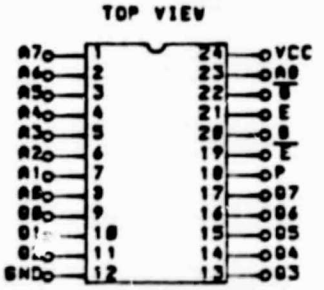
BLOCK DIAGRAM



LOGIC SYMBOL



PIN OUT



A: ADDRESS INPUT
O: DATA OUTPUT
E: CHIP SELECT
G: OUTPUT ENABLE
P: PROGRAM ENABLE

ABSOLUTE MAXIMUM RATINGS OPERATING CONDITIONS

SUPPLY VOLTAGE	+10.5V	SUPPLY VOLTAGE	5.0V to 10.0V
INPUT VOLTAGE	(GND -0.4V) to (Vcc +0.4)	AMBIENT TEMPERATURE	-55C to +125C
STORAGE TEMPERATURE	-65C to +150C		

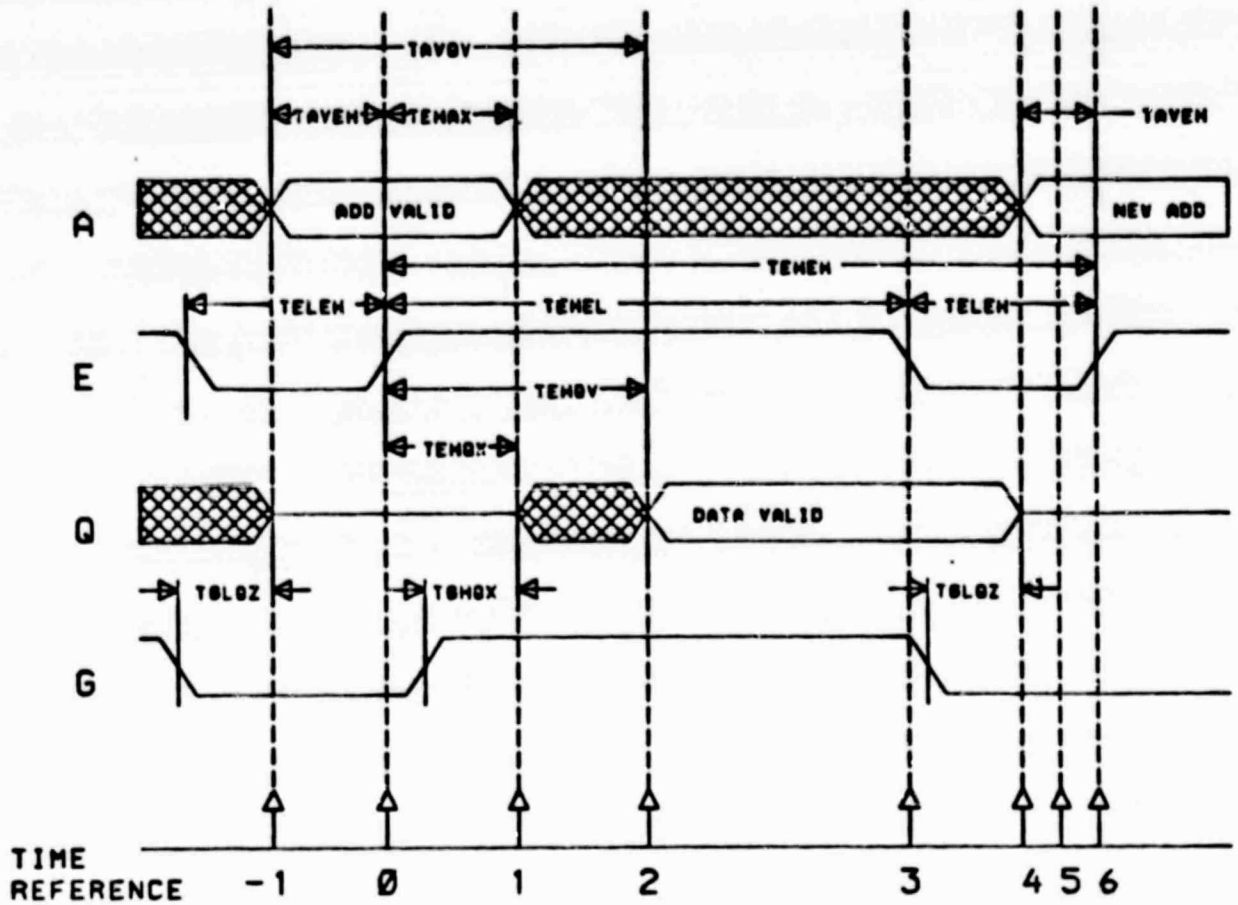
DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	STANDBY SUPPLY CURRENT		50	μA	Vcc-10.0V
ICC	OPERATING SUPPLY CURRENT		10	MA	Vcc-10.0V f-1MHZ

AC CHARACTERISTICS (Vcc-10.0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TEHQV	CHIP ENABLE ACCESS TIME		200	NS
TAVQV	ADDRESS ACCESS TIME		220	NS
TAVEH	ADDRESS SET UP TIME	20		NS
TEHAX	ADDRESS HOLD TIME	60		NS
TELEH	CHIP ENABLE NEGATIVE PULSE WIDTH	150		NS
TEHEL	CHIP ENABLE POSITIVE PULSE WIDTH	200		NS
TEHEH	READ CYCLE TIME	350		NS
TEHQX	CHIP ENABLE TO OUTPUT ENABLE	20	100	NS
TGHQX	OUTPUT ENABLE TO OUTPUT ENABLE	20	100	NS
TGLQZ	OUTPUT ENABLE TO OUTPUT DISABLE	20	100	NS

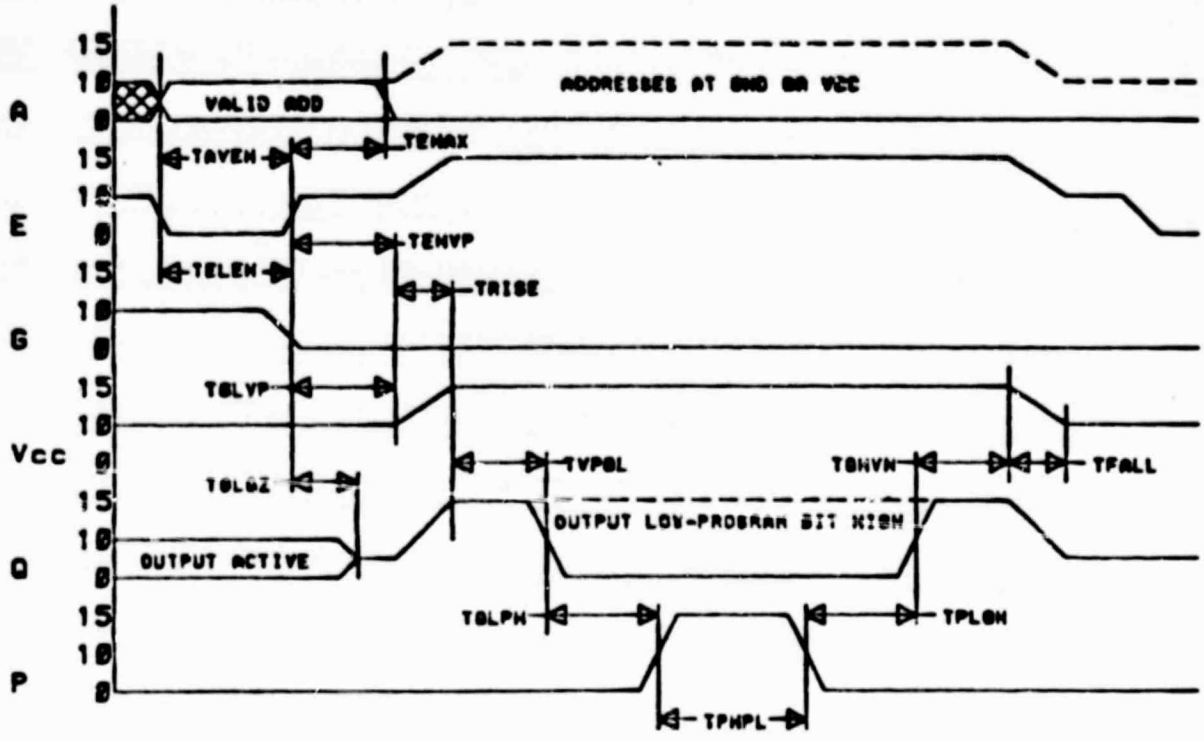
READ CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	POINT IN READ CYCLE
	A	E	G	Q	
-1	X	L	L	Z	MEMORY DISABLED
0	V	↓	L	Z	CYCLE BEGINS; ADD. ARE LATCHED
1	X	H	H	X	OUTPUT ENABLED
2	X	H	H	V	OUTPUT VALID
3	X	↓	H	V	OUTPUT LATCHED
4	V	L	L	Z	READ ACCOMPLISHED & OUTPUT DISABLED
5	V	L	L	Z	MEMORY DISABLED (SAME AS -1)
6	V	↓	L	Z	CYCLE ENDS, NEW CYCLE BEGINS

PROGRAMMING CYCLE



PROGRAMMING SYSTEM TIMING

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TAVEH	ADDRESS SET UP TIME	500		NS
TEHAX	ADDRESS HOLD TIME	500		NS
TELEH	CHIP ENABLE LOW TIME	500		NS
TEHVP	CHIP ENABLE HIGH TO VCC RISING DELAY	500		NS
TGLVP	OUTPUT ENABLE LOW TO VCC RISING DELAY	500		NS
TGLQZ	OUTPUT ENABLE LOW TO OUTPUT HIGH Z		100	NS
TRISE	VCC RISE TO PROGRAMMING LEVEL	1.0		µS
TVPGL	VCC HIGH TO OUTPUT LOW DELAY	500		NS
TGLPH	DATA SETUP TIME	500		NS
TPHPL	PROGRAMMING PULSE WIDTH	300	400	µS
TPLGH	DATA HOLD TIME	500		NS
TGHVN	OUTPUT HIGH TO VCC NORMAL DELAY	500		NS
TFALL	VCC HIGH TO VCC NORMAL FALL TIME	1.0		µS

REFERENCES

[1] E. R. Hnatek, "Bipolar PROM Reliability," Microelectronic Reliability, Volume 18, pp. 325-332, 1978.

[2] R. C. Smith, S. J. Rosenberg, C. R. Barret, "Reliability Studies of Polysilicon Fusible Link PROMs," IEEE Reliability Physics Symposium, 1976, pp. 193-197.

[3] G. H. Parker, J. C. Cornet, W. S. Pinter, "Reliability Considerations in the Design and Fabrication of Polysilicon Fusible Link PROMs," IEEE Reliability Physics Symposium, 1977, pp. 88-89.

[4] W. R. Dawes, G. F. Derbenwick, B. L. Gregory, "Process Technology for Radiation Hardened CMOS Integrated Circuits," Journal of Solid State Circuits, Vol. SC-11, No. 4, August 1976.