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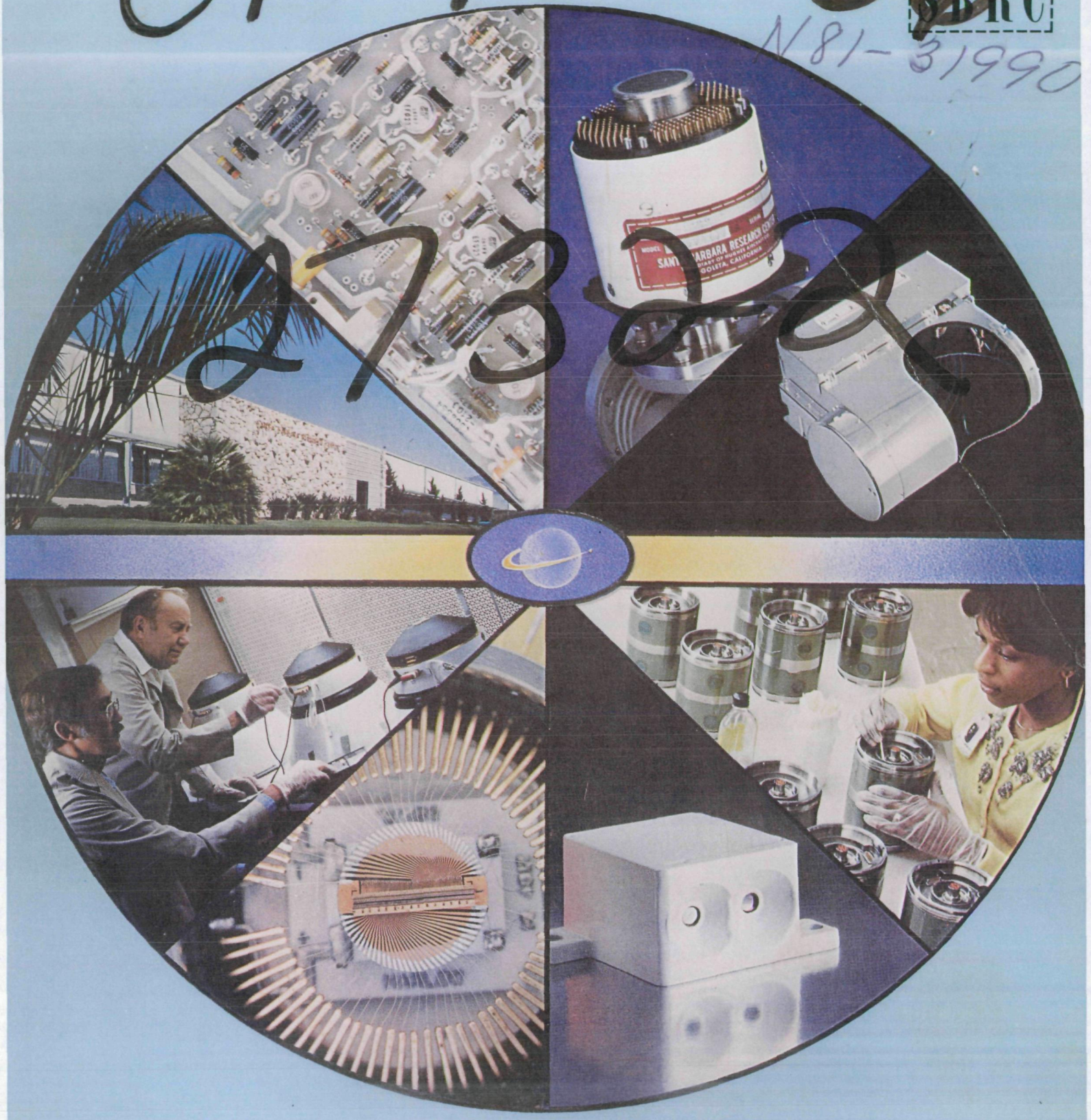

SANTA BARBARA RESEARCH CENTER

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NASA Contractor Report 165766

Advanced InSb Monolithic Charge Coupled Infrared Imaging Devices (CCIRID)

T.L.KOCH, R.D.THOM, and W.D. PARRISH

SANTA BARBARA RESEARCH CENTER
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CONTRACT NAS1-15551
SEPTEMBER 1981

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TABLES

SYMBOLS

E	=	dielectric strength (v/cm)
ϵ	=	inefficiency per transfer of CCD
ϵ_{SS}	=	inefficiency due to surface states
λ	=	wavelength, μm
η	=	quantum efficiency
$\tau_{(\lambda)}$	=	transmission of spectral filter at wavelength λ
Ω	=	field-of-view (FOV), degrees
σ_p	=	Gaussian implant width parameter, μm
A_D	=	detector area, cm^2
A_v	=	voltage gain
C	=	speed of light, 3.00×10^8 meters/second
C_o	=	CCD output capacitance, farads
CTE	=	charge transfer efficiency (efficiency per transfer)
D^*	=	detectivity, cm $Hz^{\frac{1}{2}}$/watt
$D^*_{\lambda p}$	=	peak detectivity, cm $Hz^{\frac{1}{2}}$/watt
f_c	=	CCD clock frequency, Hz
f_{ch}	=	chopped clock frequency, Hz
f_s	=	detector sampling frequency, Hz
h	=	Planck's Constant, 6.63×10^{-34} joule-second
H_{sig}	=	signal irradiance at plane of array, watts/cm^2
k	=	Boltzmann's Constant, 1.38×10^{-23} joule/K or 8.62×10^{-5} eV/K 1 eV = 1.6×10^{-19} J
N	=	number of detectors in TDI
N_B	=	number of CCD bits
N_D	=	substrate net impurity concentration, cm^{-3}
N_{fc}	=	number of oxide charges per unit area = Q_{fc}/q, cm^{-2}
N_{max}	=	number of carriers in CCD
N_n	=	number of noise carriers
N_{SS}	=	surface state density, #/cm^2-eV

q	=	electron charge, 1.6×10^{-19} coulombs
Q_B	=	background photon flux at plane of array, phot/sec-cm^2
Q_s	=	signal charge, coulombs
R_λ	=	responsivity at wavelength λ, volts/watt
R_p	=	Gaussian distribution peak, μm
T	=	temperature, degrees Kelvin
T_C	=	CCD clock period, seconds
T_{INT}	=	detector integration time, seconds
T_s	=	sample period, seconds
T_S	=	storage time, seconds
V_{FB}	=	flatband voltage, volts
V_G	=	gate voltage, volts
V_n	=	noise voltage, volts
V_o	=	$V_s + V_{FZ}$, total output voltage, volts
V_s	=	output voltage due to signal charge, volts

Section 1

INTRODUCTION

The development of integrated detector-charge-coupled device (CCD) arrays will allow considerable improvements in future infrared sensors. The use of CCDs will create reductions in weight, volume, and power requirements of the detector array and associated electronics. Monolithic integration of detectors together with CCDs in an intrinsic IR semiconductor is an attractive approach for such arrays. The monolithic intrinsic concept, as it has come to be known, offers higher operating temperature and quantum efficiency compared to its monolithic extrinsic (Si:X) counterpart having the same cutoff wavelength. High quantum efficiencies may be realized with suitable device design because the intrinsic or fundamental absorption is utilized, and optical crosstalk effects, particularly important in dense arrays will be small. The monlithic infrared CCD imaging devices may be configured in either linear or area (two-dimensional) arrays, and may be designed to accomplish functions such as time-delay-and-integration (TDI) for signal/noise ratio enhancement in scanning IR sensors.

The long-range objective of this work is to develop a new concept in infrared imaging sensors utilizing charge transfer techniques. The near-term objective is to fabricate prototype devices that can be used to establish applications and operational characteristics of the IR imaging sensors.

The material being used for these studies is indium antimonide (InSb), which provides detection capabilities in the 1-to 5.4-μm spectral region. InSb is a favorable material for monlithic infrared CCD arrays because it can be grown with relatively high purity, low dislocation density, and in large size ingots. InSb wafers with diameters in the 2.5- to 4.0-cm range are suitable for convenient handling and photolithographic processing.

BACKGROUND

The feasibility of InSb CCD's was demonstrated and reported[1, 2] with development efforts conducted during the mid-1970's. An improved InSb CCIRID chip, designated the SBRC 8585 (Figure 1 (a)), was designed and photomasks for its fabrication procured under NASA contract NAS1-14395[3].

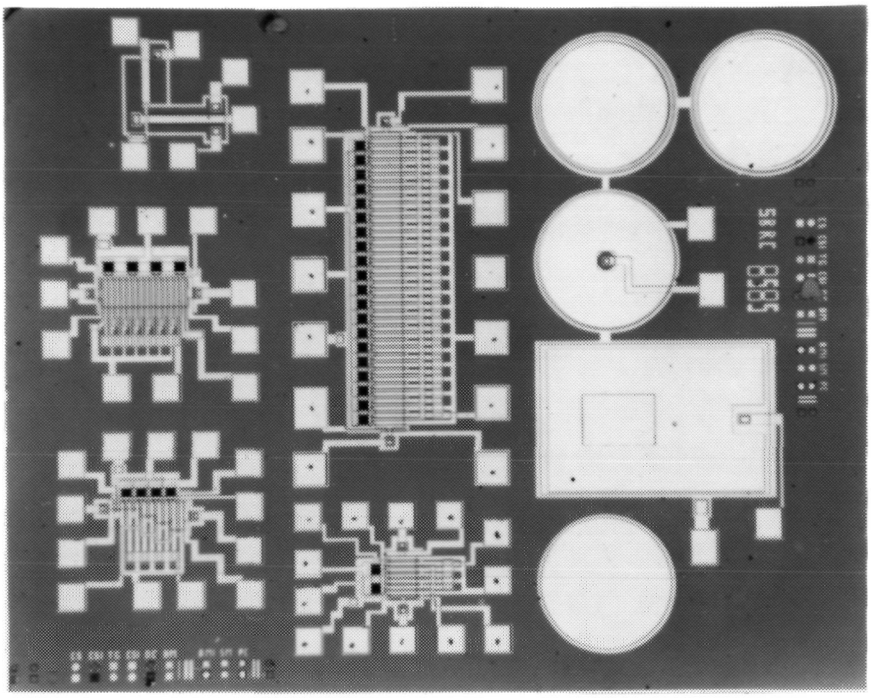
During contract NAS1-14922[4], two 20-element InSb CCIRID's (Figure 1 (b)) - the major device on the SBRC 8585 chip - were fabricated, characterized, and delivered to the NASA Langley Research Center. The operational characteristics of these devices (IS 498-17-A3 and IS 498-17-F4) have been reported by Thom, et. al., [5, 6, 7, 8].

The initial delivered devices were characterized by: a charge transfer efficiency (CTE) of 0.995; and a quantum efficiency, (η) of $\simeq$ 50%. These characteristics are not considered to be fundamental in nature and are amenable to improvement through furthur process development.

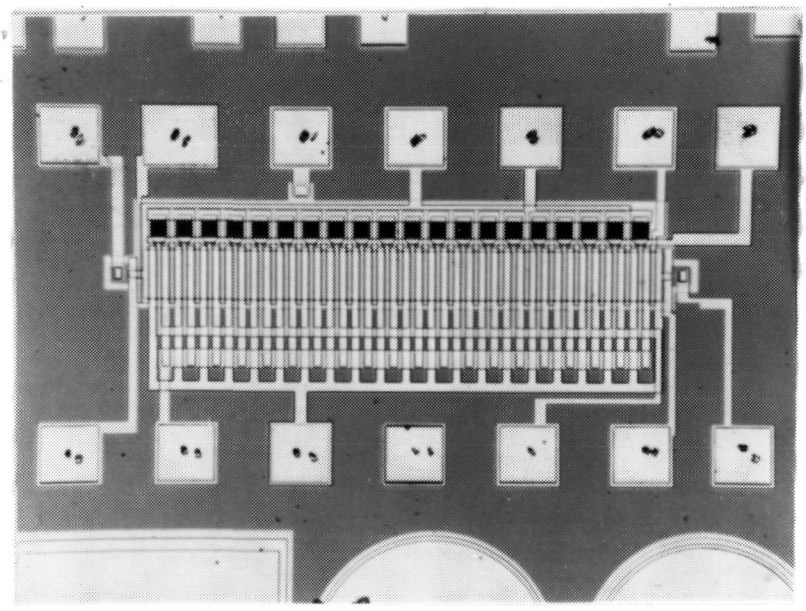
Several factors were addressed during this program which were intended to improve the previous device characteristics.

The monlithic InSb CCD fabrication process, based on a 4ϕ, overlaping aluminum gate approach with SiO_2 dielectric layers, is amenable to further reduction in line width and extension to large area arrays. A major task during this contract was to design and procure photomasks for a next-generation chip which extends the monolithic InSb technology state of the art from linear to area arrays. This new chip, designated the SBRC 8587, incorporates a 20 x 16 TDI imaging array, a 100-element linear array, and several other test devices.

Further extension of the InSb CCD state of the art is possible through the addition of planar ion implanted n^+-n channel stops. Development of a feasible process was performed on Internal Research and Development (IR&D) - funded programs during 1977, and 1978. Adaptation of the implanted channel stop process for use in CCD fabrication was pursued during this contract.



a) SBRC 8585 InSb CCIRID Chip



b) 20-Element InSb CCIRID

Figure 1. Monolithic InSb CCIRID

This report describes the process improvements pursued during the program in an attempt to improve the overall operational characteristics and yield of 20-element linear arrays. It also includes new improved electrical and optical characteristics obtained from a device previously delivered to NASA Langley Research Center. A complete description of the parameters used in designing the next-generation CCIRID chip is given plus a discussion of the development of a planar channel stop. The report is organized as follows:

1. Section 2 describes in detail the InSb material characteristics, fabrication and structural sequence, and process modifications incorporated for improving the device operational CTE and yield characteristics of 20-element linear imagers.

2. Section 3 discusses newly obtained radiometic operational characteristics, from device IS 498-17-F4 (S/N-002) previously delivered on contract NAS1-14922.

3. Section 4 discusses the design, layout, mask procurement and process description of the next-generation CCIRID chip.

4. Section 5 describes the developed parameters and process description for incorporation of planar channel stops.

5. Section 6 describes the optical parameters and process development of a transparant photogate layer which should ultimately improve the quantum efficiency of these CCIRIDs. In addition, a discussion is included regarding the evaluation of an alternate device insulating structure utilizing chemical vapor deposited silicon dioxide.

6. Section 7 gives a final summarization of the results obtained on the contract.

Identification of commercial products in this report is to adequately describe the materials and does not constitute official endorsement, expressed or implied, of such products or manufacturers by the National Aeronautics and Space Administration.

ACKNOWLEDGEMENT

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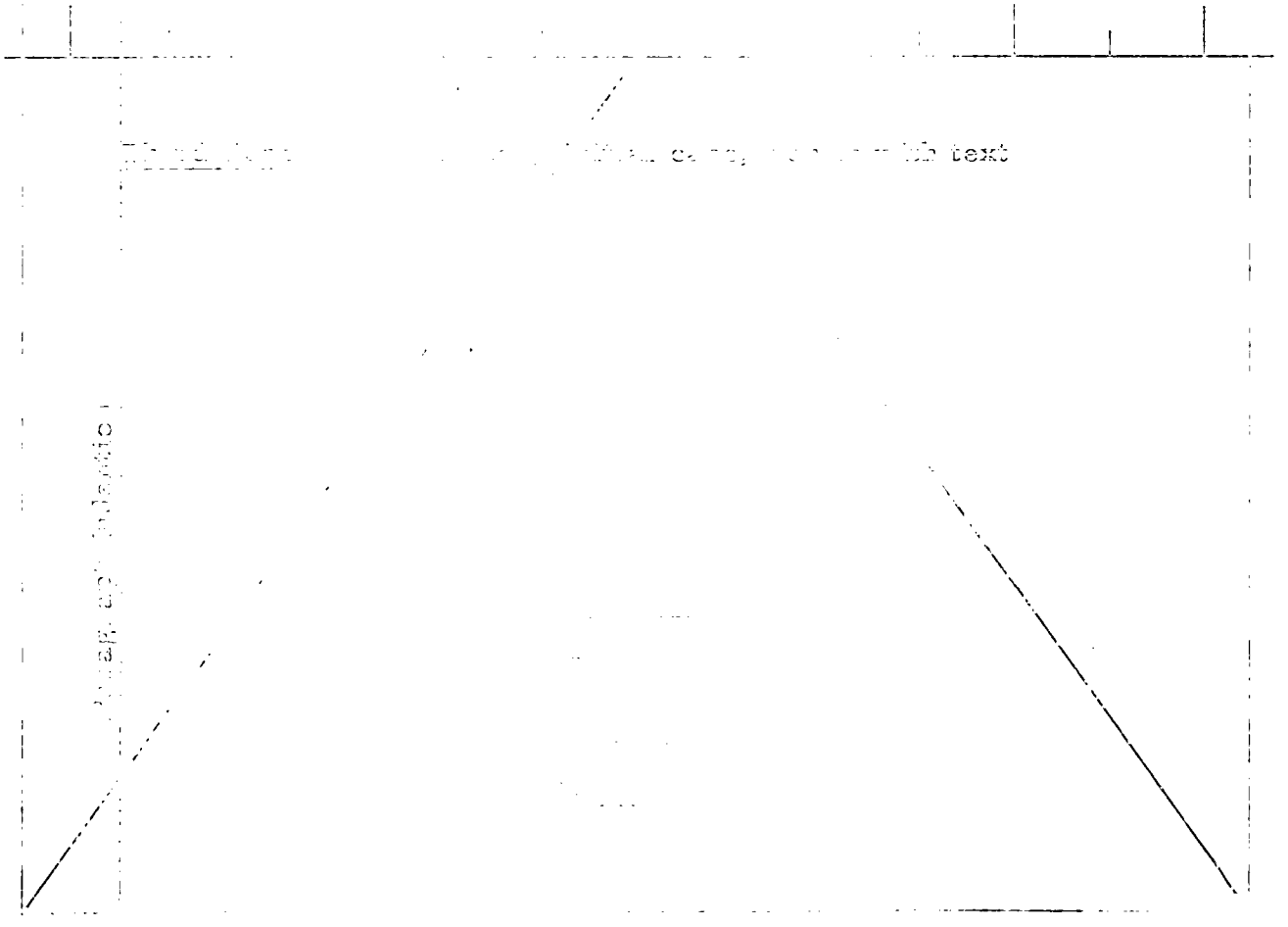


Section 2

SBRC 8585 20-ELEMENT LINEAR IMAGER DEVICE FABRICATION

InSb WAFER CHARACTERISTICS

The bulk InSb wafers used for device fabrication during this contract period were undoped n-type InSb purchased from Metal Specialties, Incorporated, in Fairfield, Connecticut (distributors for M.C.P. Electronics Limited in Windsor, Bershire, England), and Cominco American, Incorparated, of Spokane, Washington.

Each wafer was oriented to within 0.5° of the <111> axis as sliced from an ingot grown on the <211> axis by Czochralski withdrawal techniques. The slices were shaped into uniform 3.2 cm diameters by cutting with a diamond hole saw placed in such a manner that a natural flat remained for mask orientation during photolithographic processing. The slices were subsequently lapped and chemically polished into wafers 635 μm thick with a surface finish on the antimony (Sb)-rich, (111)B face of less than 0.1 μm. Etch pit density measurements performed on both the A (In-rich) and B(Sb-rich) faces indicated EPD ranges from 5 to < 100 cm^{-2} were achieved with the polishing processes.

The net carrier concentration (N_D) for these wafers ranged from $6.1 \times 10^{13} cm^{-3}$ to $2.5 \times 10^{14} cm^{-3}$ as measured by Hall techniques at 77 K. The wafer electron mobility ranged from 4.5 to $6.5 \times 10^{5} cm^{2} \cdot V^{-1} \cdot sec^{-1}$ and the resistivity ranged from 0.03 to 0.54 ohm · cm. Analysis of the wafers, using Berg Barrett X-Ray topography techniques, indicated that no crystal damage remained following the final B-face surface polish.

DEVICE FABRICATION

The devices delivered on contract NAS1-14922 utilized a low-temperature chemical vapor deposited (LT CVD) SiO_2 gate oxide which has been reported to yield MIS structures with very low surface state densities

($N_{SS} \leq 10^{10}$ $cm^{-2} - eV^{-1}$).[9,10,11] CCDs with such insulators should have been capable of operating with CTE values approaching 0.9995 or better. It was hypothesized that the CTE was limited by lateral nonuniformities in surface potential arising from microscopic granularity in the LT CVD SiO_2.[4,7,8] Therefore, throughout this contract period, the structural process parameters were varied in attempting to reduce the oxide granularity and increase the CTE.

A listing of the SBRC 8585 process scheme is given in Table 1. In addition, a process flow chart with corresponding cross-sectional views across and along the CCD channel as the structure is fabricated is shown in Figure 2. Several of the operations in the table and flow chart have been marked with an asterisk to identify processes which were subjected to variation during this period. Operations 4XX and 7XX will be discussed in this section. The entire transparent gate development effort (Operation 11XX) will be discussed in Section 6.

GATE INSULATOR PROCESS (OPERATION 4XX)

The gate insulator deposition process (Operation 4XX) is the most critical operation of the entire process sequence. It is at this point the InSb surface is cleaned and passivated. Over the course of this and the preceding contract,[4] two LT CVD SiO_2 systems have been utilized for depositing the surface passivation layer. These include a vertical-flow type AMS-1000 system and a horizontal-flow type AMS-2600 system. Both use pyrolytic decomposition of silane (SiH_4) in the presence of oxygen to form SiO_2:

$$SiH_4 + O_2 \xrightarrow{\text{Heat}} SiO_2 + 2H_2\uparrow \qquad (2\text{-}1)$$

The basic process using InSb was first developed and reported by Lincoln Laboratories[12] and later improved and reported by Kim[13] and Langan.[9]

Differing results have been achieved with the two reactors. The

should be page 2-5 ✓

Table 1. 8585 CCIRID Fabrication Process

Operation	Process Title	Layer/Mask Designation	Process Description
0XX	Initial wafer preparation	---	Initial wafer clean-up (removal of shipping materials)
1XX	Alignment pattern	AP	Deep polish etch AP pattern
2XX	Implant p^+ source/drain	SD	Apply SD implant pattern: ion implant $p^+(Be^+)$
3XX	Anneal SD implant	---	Prepare surface and anneal implant
*4XX	Gate insulator	GI	Perform surface etch: deposit SiO_2 (1500 Å) layer: anneal
5XX	Channel stop metal	CS	Deposit Al (500 Å) layer: etch CS pattern; perform surface C-V tests
6XX	Diode contacts (first)	DC1	Etch initial diode contact windows
*7XX	Channel stop insulator	CSI	Deposit SiO_2 (1000 Å - 2000 Å); etch CSI pattern (1000 Å - no etch option)
8XX	Channel stop contact	CSC	Etch contact windows to CS
9XX	Diode contact (final)	DC2	Etch final reduced diode contact window: optional Pd plate

Table 1. 8585 CCIRID Fabrication Process (continued)

Operation	Process Title	Layer/Mask Designation	Process Description
10XX	Buried metal	BM	Deposit Al (1500 Å) etch BM pattern
*11XX	Transparent gate	TG	Deposit Ti(75Å); lift-off TG pattern Deposit Al(500Å); lift-off BMI pattern (stop etch layer)
12XX	Buried metal insulator	BMI	Deposit SiO_2(2000 Å) etch BMI pattern
13XX	Surface metal	SM	Deposit Al (1500 Å) etch SM pattern
14XX	Buried contacts	BC	Deposit SiO_2 (2000 Å) etch BC pattern
15XX	Surface contacts	SC	Etch SC pattern
16XX	Pad metal	PM	Deposit Al (3000 Å) etch PM pattern
17XX	Final evaluation	---	DC short tests C-V tests CCIRID tests

*Denotes critical process.

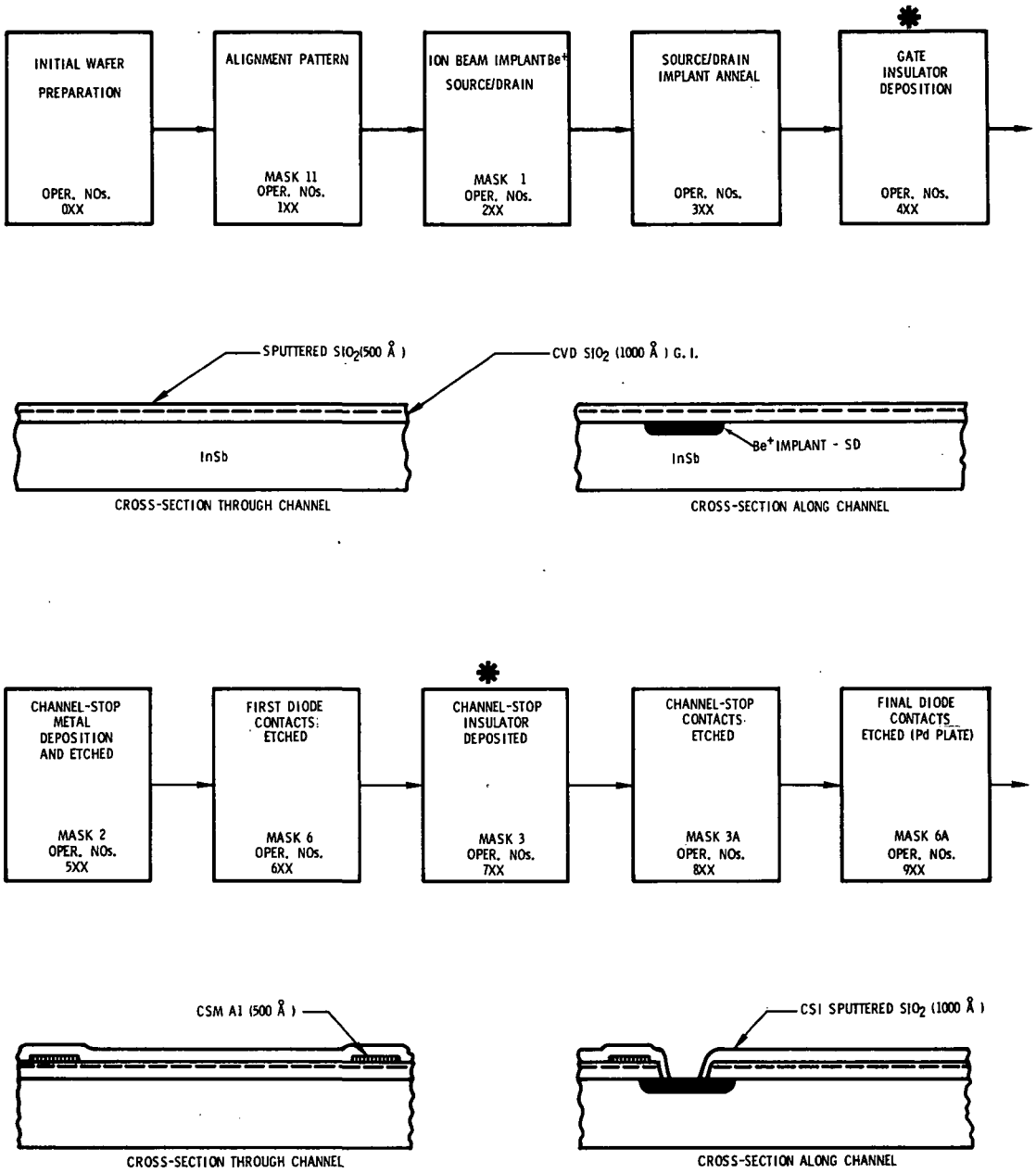


Figure 2. Present SBRC 8585 CCIRID Process Flow

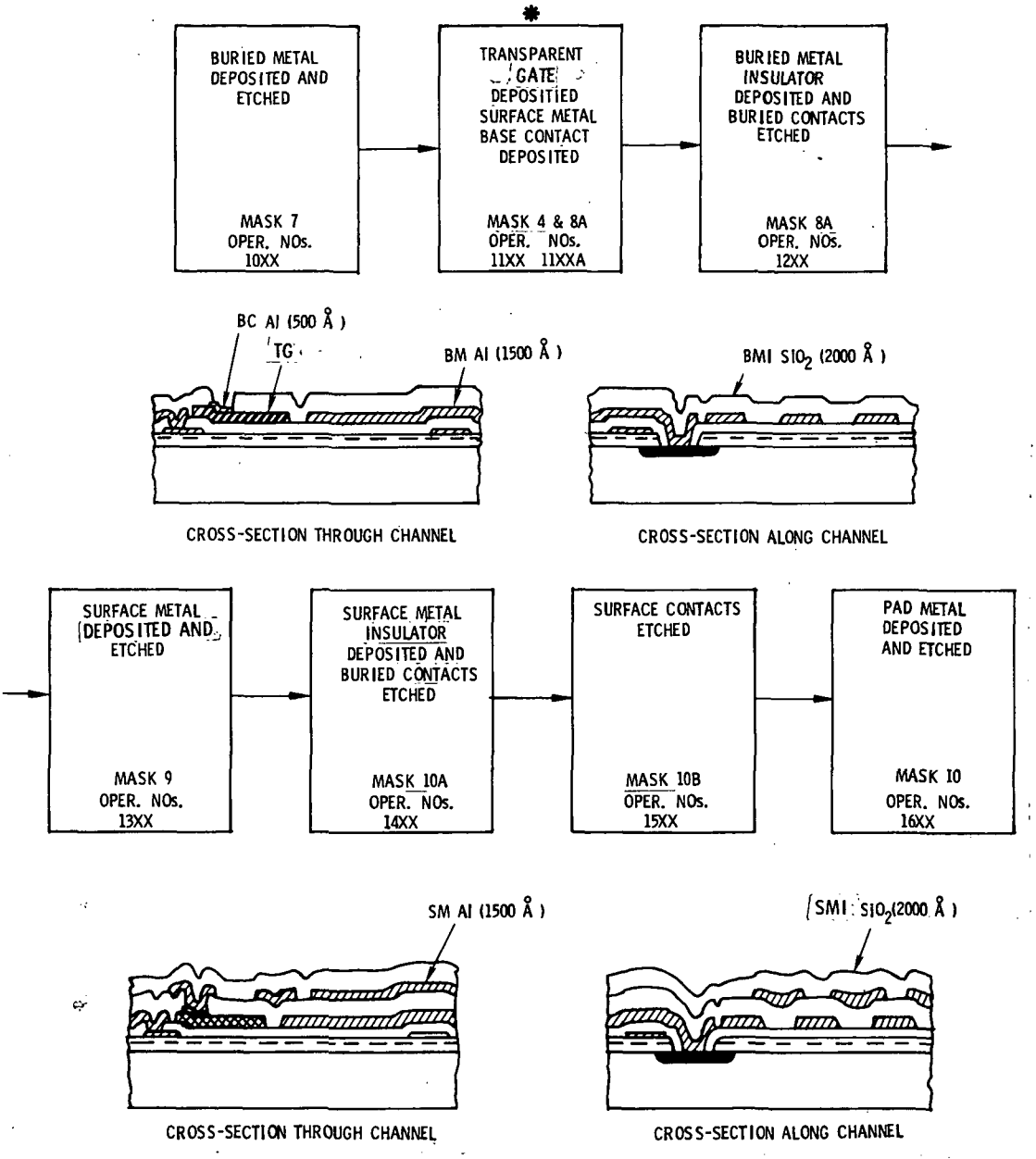


Figure 2. Present 8585 CCIRID Process Flow (continued)

AMS-2600 has produced excellent MIS characteristics, but its oxide is considered to be more granular and have less desirable mechanical properties than the AMS-1000. The AMS-1000 tends to produce slightly less granularity, but its electrical characteristics are inferior to the AMS-2600.

Auger depth profiles of the oxides have shown a thin native oxide of InSb (several monolayers) exists at the InSb/LT CVD SiO_2 interface. This thin oxide accomplishes the actual electrical passivation. The LT CVD SiO_2 serves as a benign insulator for preservation of the thin oxide during processing and as an electrical isolation layer which the thin oxide does not supply. Auger depth profiles of oxide samples from the the two reactors show a lower oxidation state of Sb exists in the native oxide following an AMS-1000 deposition than exists in the native oxide following a deposition with the AMS-2600. This has been hypothesized to be related to reduction of the native oxide by free silicon resulting from a heterogeneous reaction in the vertical reactor. The horizontal reactor mixes the oxygen and silane well away from the sample surface such that the SiO_2 forms homogeneously; thus, the tendency to more granularity.[4, 9]

In addition to granularity, the LT CVD SiO_2 layer is porous. This is exemplified by its etch rate, which is as much as three times faster than thermally-grown SiO_2. Thus, reproducible etching is difficult to control, and the LT CVD oxides, by themselves, tend to absorb water molecules (as deduced by performing bakeout studies on LT CVD SiO_2 MIS samples using capacitance-voltage (CV) analysis before and after baking in a dewar). For these reasons, the multilayered oxide structure shown in Figure 2 is used as the gate insulator.

A 500 Å thick RF-sputtered SiO_2 layer is deposited over a 1000 Å - thick LT CVD SiO_2 layer. This RF-sputtered SiO_2 layer is very similar to thermally-grown SiO_2 in both dielectric constant and etch rate. Thus, it serves as a water barrier for the LT CVD oxide and a base layer for all subsequent processing.

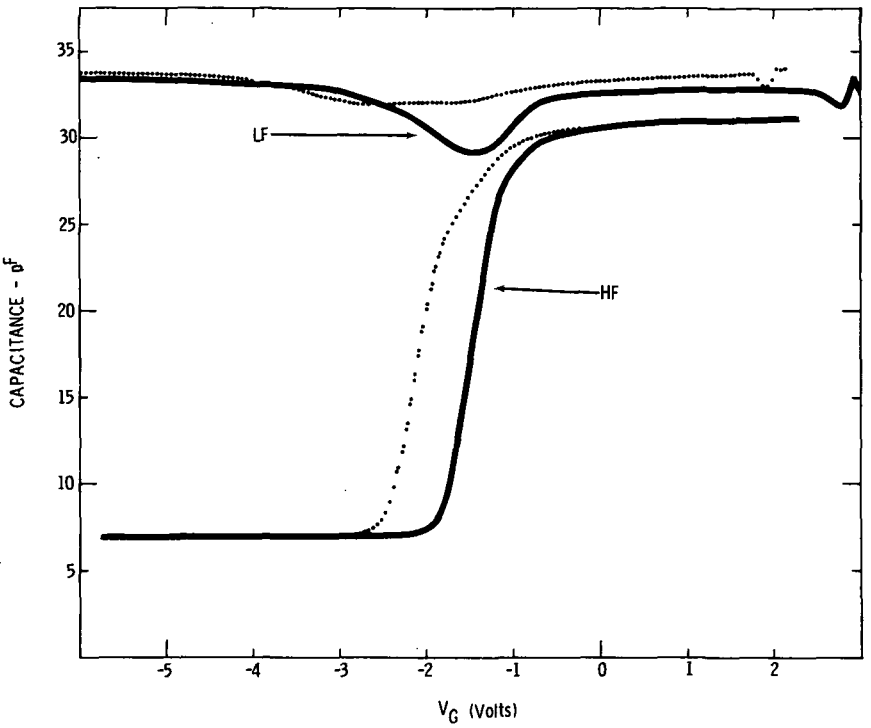
Following the deposition of the RF-sputtered SiO_2 layer, the wafers are annealed and subsequently overcoated with a dc-sputtered aluminum layer which serves as the channel stop of CCD wafers. A witness wafer of InSb accompanies the CCD lot through this process.

Figure 3 (a) shows the high-frequency (HF) and low-frequency (LF) C-V curves obtained from the witness sample for lot 8585-21. This lot received a gate insulator deposited in the AMS-1000 CVD reactor. Figure 3 (b) shows the HF and LF C-V curves obtained from the witness sample of lot 8585-22 using a gate insulator from the AMS-2600 CVD reactor. Obviously, the characteristics in (b) are much superior to those in (a) (i.e., the curves in (b) have less hysteresis, near-zero flatband voltage, and much deeper LF minima). The dip in LF of sample (a) correlates to a N_{SS} value of $\sim 6 \times 10^{11}$ $cm^{-2} \cdot eV^{-1}$. The LF dip in (b) correlates to a N_{SS} value approaching 10^{11} cm^{-2} -eV^{-1}.

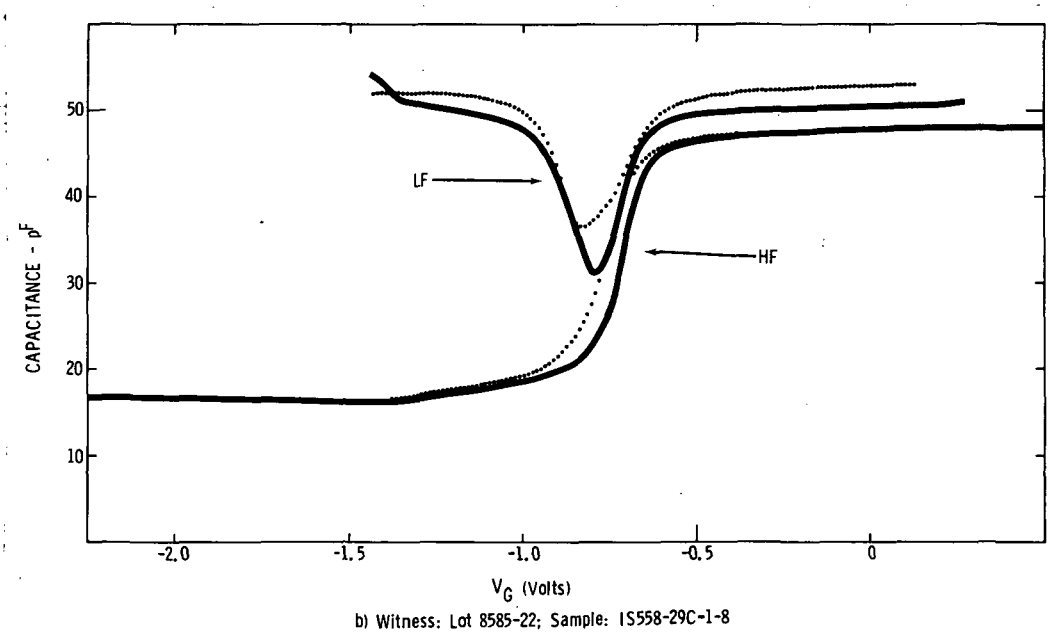
Calculation of the predicted transfer inefficiencies (ϵ_{SS}) due to parallel-edge surface state losses for 20-element CCD's from the above lots indicated that Lot 8585-21 would yield a CTE less than 0.999, while Lot 8585-22 would yield a CTE greater than 0.999. Similar results were predicted but not achieved on the previous contract. At that time, the CTE was hypothesized to be limited by granularity-induced charge trapping. Means were not yet available to reduce the basic LT CVD SiO_2 granularity as deposited (See Appendix). However, a process change was implemented to minimize the charge trapping effect by not enhancing the granular nature of the oxide during later processing. The major point in contention was to eliminate etching the CCD channel at Operation 7XX.

CHANNEL STOP INSULATOR ETCH (PROCESS 7XX)

During the previous contract, a 2000 Å -thick channel stop insulator (CSI) of RF-sputtered SiO_2 was deposited on the wafers following etching and testing of the channel stop metal (CSM). This layer was used to build up a



a) Witness: Lot 8585-21; Sample: W4166E-3a-1-8



b) Witness: Lot 8585-22; Sample: IS558-29C-1-8

Figure 3. HF and LF C-V Characteristics for a) AMS-1000 Reactor and b) AMS-2600 Reactor

thick field oxide for added strength during wirebonding and add isolation between the CSM and the subsequent buried gate metal (BM).

Following the CSI deposition, the CCD channel (delineated by the etched CSM pattern) was dry-plasma etched to form an insulator thickness below the BM CCD gates of ~ 2250 Å. This etch process was believed to enhance the granularity effect and increase the density of pinholes. The enhanced granularity was believed to create additional charge trapping which decreased the array CTE. In addition, the pinholes would directly relate to increased BM gate-to-substrate shorts and reduce the yield. With these items in mind, the CSI SiO_2 was reduced to a thickness ≥ 1000 Å, and the channel etch operation was eliminated.

Possible problems resulting from the thinner oxide were shorting between the CSM and BM levels and an increase in shorting from the BM bond pads to the substrate following wire bonding. Witness wafers have thinner oxides (1500 Å) under the capacitor when they are wire bonded and shorting is usually not a problem. Also, the CCD bond pads receive an additional 3000 + Å deposition of aluminum to form a more resiliant base for wire-bonding. Thus, the thinner oxide under the bond pad was not expected to be a problem.

With respect to intergate shorting between the CSM and BM levels, bias tests between the gates were conducted following BM delineation (Operation 10XX) of early lot wafers. No breakdown was observed at or above ± 20 V, corresponding to a dielectric strength of $E > 2 \times 10^6$ V - cm^{-1}. Thus, the oxide thickness was considered satisfactory for use.

Actual CTE verification of this process was not achieved as all lots using it were subsequently shorted beyond use by microarcing during sputtered depositions.

20-ELEMENT CCIRID PROCESSING

Over the course of the program, seven lots were introduced into the process sequence. Of these, lots 10, 15, 21, and 24 were completed and subjected to device short testing. The remaining lots were halted in process following discovery of microarc-induced shorting.

Lots 8585-10 and 8585-15 were processed in order to evaluate the use of the LT CVD SiO_2 as an upper layer insulator. The results of this evaluation will be discussed in Section 6.

Lot 8585-21 was the first to be completed utilizing all of the process improvements instituted during this program. It incorporated: non-etched CCD channels; ITO transparent gates; and use of a mobile ion-free developer that was found to reduce previous problems of multilayer structure delamination.

All of the above improvements resulted in wafers with a high yield ($>80\%$) of visually acceptable devices.

During dc short testing, all of the 20-element linear arrays were found to have multiple gate-to-gate and gate-to-substrate shorts.

Samples from the wafers were analyzed by scanning electron microscopy (SEM) techniques and found to exhibit small arc spots in all metal levels. These had been noted as possible dirt particles during visual inspection. A dc short test was conducted on portions of wafers which had broken earlier in the process sequence. Results of this test indicated the arc spots were not present prior to final pad metal deposition. Several precautions against personnel-induced electrostatic discharge arcing had been instituted, such as the use of ground straps and grounding of hot plate surfaces. It was concluded the shorting had occurred from arcing of the aluminum cathode in the planar magnetron sputtering system.

To alleviate this problem, the system was dismantled and cleaned, and a new aluminum cathode was installed and subjected to break-in deposition tests. Test structures of Al and SiO_2 were deposited and evaluated

with no problems being realized. Thus, the system was accepted and lot processing resumed.

Lot 8585-22 was then processed through the buried metal level and subjected to in-process testing of the capacitors and diode junctions. During these tests, arc spots were again observed in the channel stop and buried metal levels. We had been aware of the problem and had not seen any arcing prior to BM Al deposition. At the same time, a group of wafers being processed on an IR&D project exhibited a similar shorting mechanism. All lot processing was, therefore, halted and an intensive study initiated to determine the arcing mechanism, correct the problem, and perform tests using CCD test patterns to confirm whether the problem had been solved.

SPUTTERING SYSTEM ANALYSIS

When using the planar magnetron sputtering system for RF-sputtering of SiO_2 insulators, the plasma occasionally induces an excess amount of charge into the capacitive CCD metal layers and an arc-down occurs producing large craters in the wafers. This problem is relieved by ensuring that the wafers are electrically floating during the deposition cycle. A more serious problem was discovered when short testing lot 8585-21 revealed gross shorting of all arrays. While some percentage of gate shorts is normally observed due to pinholes and other localized defects, total shorting indicated a process or equipment problem not heretofore observed. This problem was traced to high-voltage microarcing during RF and dc sputter depositions of upper level SiO_2 and Al films. This problem only occurs as levels are fabricated beyond channel stop metal delineation. The arc spots generally resemble dirt particles when viewed with an optical microscope. High magnification SEM analysis shows them to be electrostatically induced arc craters ranging in size from 0.5 to 5 μm in diameter. Consultations with the system vendor (Airco Temescal), Peter Clark of Sputtered Films, Incorporated, in Santa Barbara, CA., and other experienced personnel in the field, plus experimental depositions conducted at SBRC, indicate the problem is related to wafer grounding, accumulative build-up of SiO_2 on the

fixturing, system deposition pressure, magnetic field strength, and cathode voltage. Experiments conducted to determine the necessary corrective action indicate the arcing can be suppressed by dismantling the sputter system at scheduled intervals for cleaning the internal fixturing, keeping the deposition parameters at levels which maintain the high-voltage at low limits, ensuring the system is fully earth-grounded, and insulating the wafers during depositions. These practices were implemented for all depositions. In addition, the magnets were recharged to ensure they were all at full strength. Other items were also considered, such as connecting the CCD gates to earth ground to allow the induced charge to drain away. This was found to be unfeasible, as it would require extensive redesign of the mask set and extra processing to separate the gates for testing. A system redesign was also considered and rejected for economic reasons.

Adhering to the above practices allowed occasional CCD structures to complete the process sequence, but the problem was not totally relieved as arcing still occurred without any indication or warning. Because of this repetitive problem, all subsequent InSb CCD lots were also lost due to this shorting mechanism.

Continued efforts to eliminate the microarcing problem have thus far been unsuccessful. Therefore, use of the system for depositing upper layer films has been halted and alternate deposition methods are being pursued.

20-ELEMENT CCIRID DELIVERY

The arcing problems discussed resulted in no new 20-element CCIRID's being obtained for delivery under this contract. Therefore, two devices which had been fabricated on contract NAS1-14922 were retested, packaged, and delivered.

These devices are noted as serial numbers 003 and 004 (SBRC Part Numbers IS 498-17-B2 and IS 498-17-B5). They have operational characteristics similar to those described in the previous contract final report[4] and as further discussed in Section 3.

Section 3

CHARACTERIZATION OF 20-ELEMENT LINEAR IMAGERS

INTRODUCTION

During this contract, new data were obtained for several 20-element monolithic InSb arrays. One array in particular, number 498-17-F4, was characterized in detail, resulting in much new radiometric data. This array, (Serial No. 2 delivered under the previous contract) was returned to SBRC for this more complete evaluation. Considerably higher D* in the multiplexing mode than previously measured was achieved through use of a clamped sample-and-hold (CSH) output circuit, which will be described. In addition, D* measurements were made in the TDI mode for the first time.

TEST CONFIGURATION, CLOCK WAVEFORMS, AND TIMING DIAGRAM

The test configuration used in the radiometric evaluation is illustrated in block diagram form in Figure 4. The helitran dewar configuration was identical to that described in the Final Technical Report for Contract NAS1-14922. The 2.65-μm spike filter was used with a 55° FOV, giving a background photon flux of $Q_B = 10^{12}$ phot-sec^{-1}-cm^{-2}. The blackbody temperature was 800K and the radiation was chopped at frequency f_{ch} with a square-wave chopper. The chip voltage output V_o (the output of the 3N163 MOSFET source-follower in the array flatpack) was fed to a wideband, unity-gain buffer located on an intermediate-temperature stage in the dewar. The first measurements were made using a fast sample-and-hold (FSH) circuit. With the FSH, the buffer output was amplified by an external post-amplifier with 500 kHz bandwidth and voltage gain (A_{v2}) of 10 prior to sample-and-hold (SH) as shown in Figure 4. For the later measurements using the CSH circuit, the 10X post-amplifier was not used; the CSH circuit contained its own gain stages and adjustable low-pass filter.

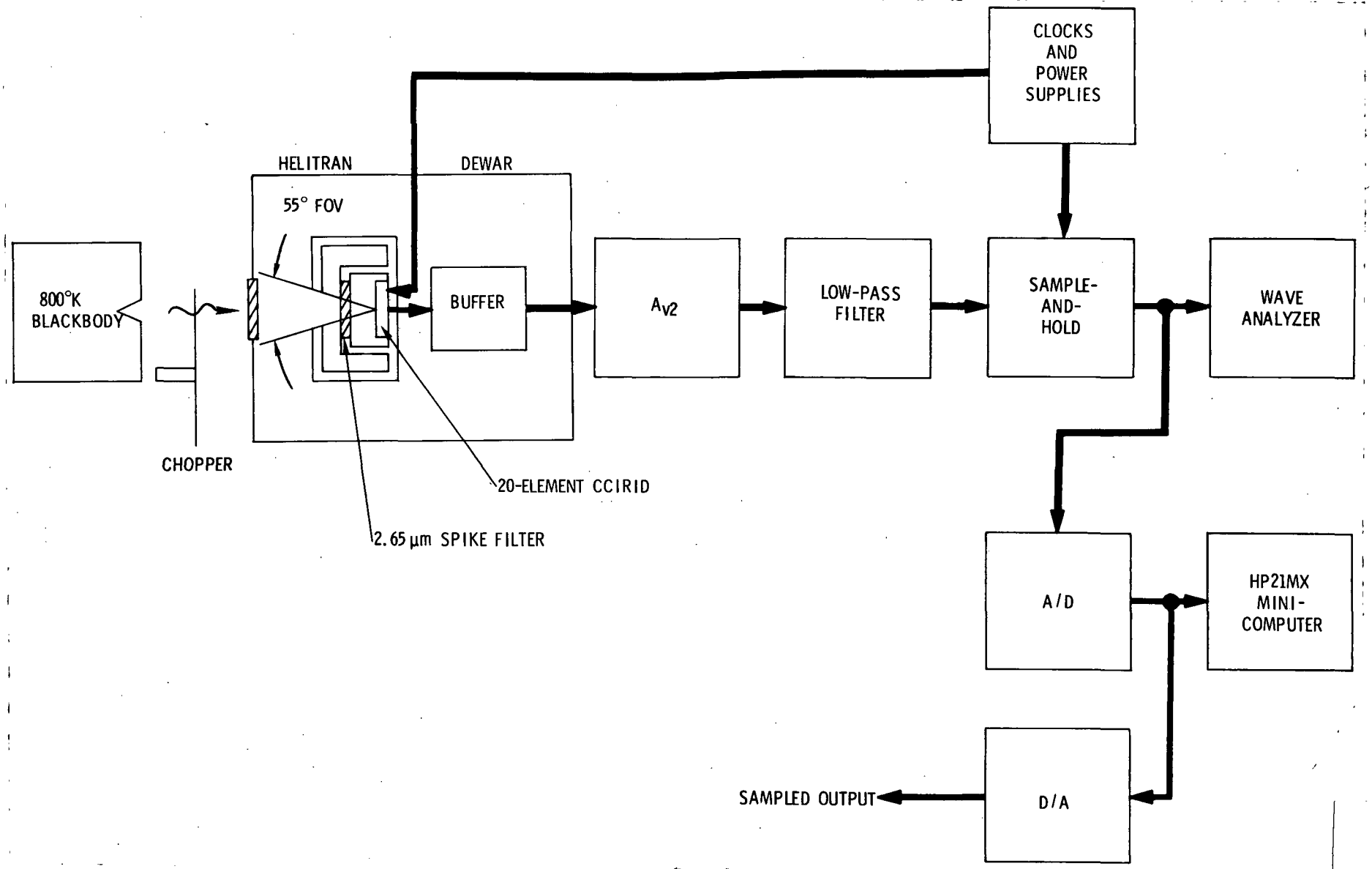


Figure 4. General Test Configuration

The clock waveforms for the array multiplexing mode (Figure 5) were used with $T_{int} \geq N_B T_C$. The timing diagram for sample-and-hold of the array outputs is shown in Figure 6. This figure shows the relationship among T_C, T_{int}, the sample period T_s, and the chopping frequency of the signal radiation. The SH circuit can acquire any one of the signals in the output pulse train using a thumbwheel selector on the master time mark generator. Figure 3-3 illustrates sampling of detector output number 18. The element selected is repetitively sampled each T_s seconds; in this case $T_s = T_{int}$, that is, the element is sampled once per integration time. The voltage level on the sampled output is held on a capacitor in the SH circuit for T_s seconds until the next sample is taken. The resulting output of the SH circuit is shown schematically in the bottom waveform of Figure 3-3. The SH output is the (amplified) response of the selected detector sampling the signal radiation at rate $f_s = T_s^{-1}$. For $f_s >> f_{ch}$, the square-wave input irradiation will be accurately reproduced. As f_s approaches f_{ch}, the RMS value of the SH output will decrease as $\sin(\pi f_{ch} T_s) / (\pi f_{ch} T_s)$ in accordance with sampling theory.

Figure 7 shows array 498-17-F4 operating in the multiplexing mode and sample-and-hold of individual outputs. The oscilloscope photograph on the left in Figure 7 shows the output pulse train (bottom waveform) of the 20-element array with clock and other test conditions given in the figure. The top waveform in the same photograph is the sampling pulse which, in this sample, is timed to sample the output of element 20. The center waveform is the SH voltage on element 20. The output swing of this element is 40 mV, as seen in the bottom waveform (i.e., the difference in output voltage level for the element viewing the blackbody aperture and viewing the chopper blade). In this series of photographs, there was no post-amplifier in the circuit ($A_{v2} = 1$) so that the output of the SH (center waveform) is also 40 mV peak-to-peak.

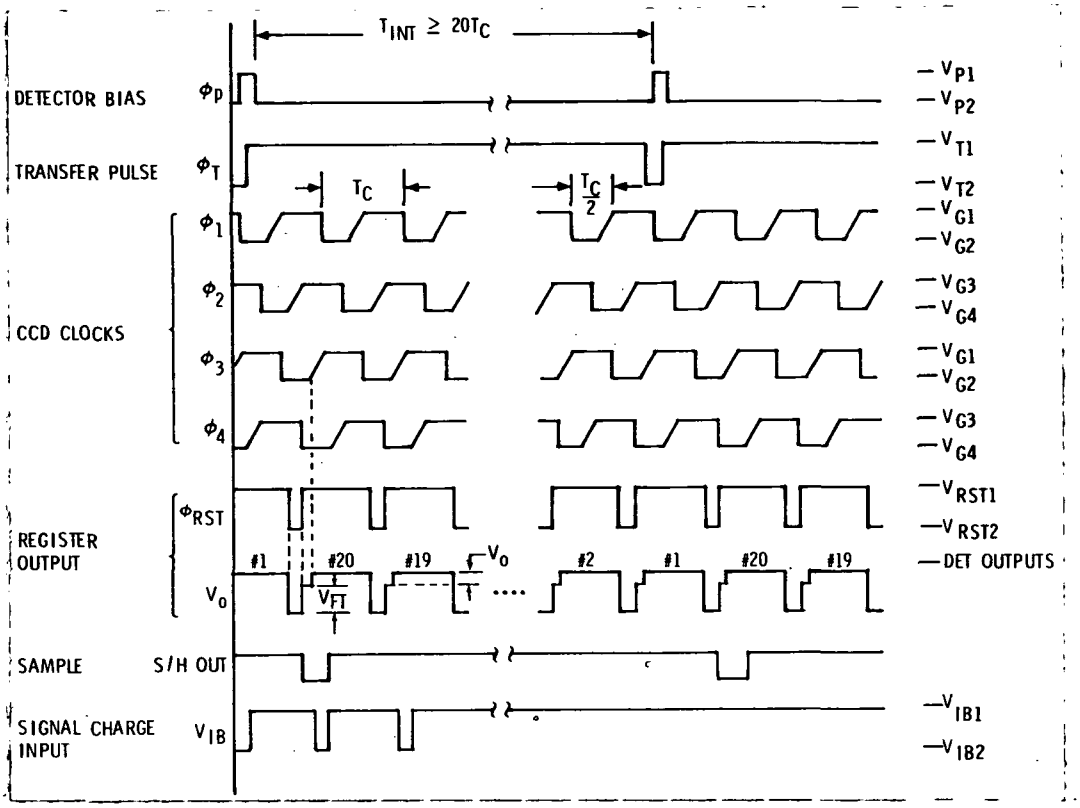


Figure 5. 20 Element InSb CCIRID Timing Diagram For Multiplexing Mode $T_{int} \geq N_B T_C$

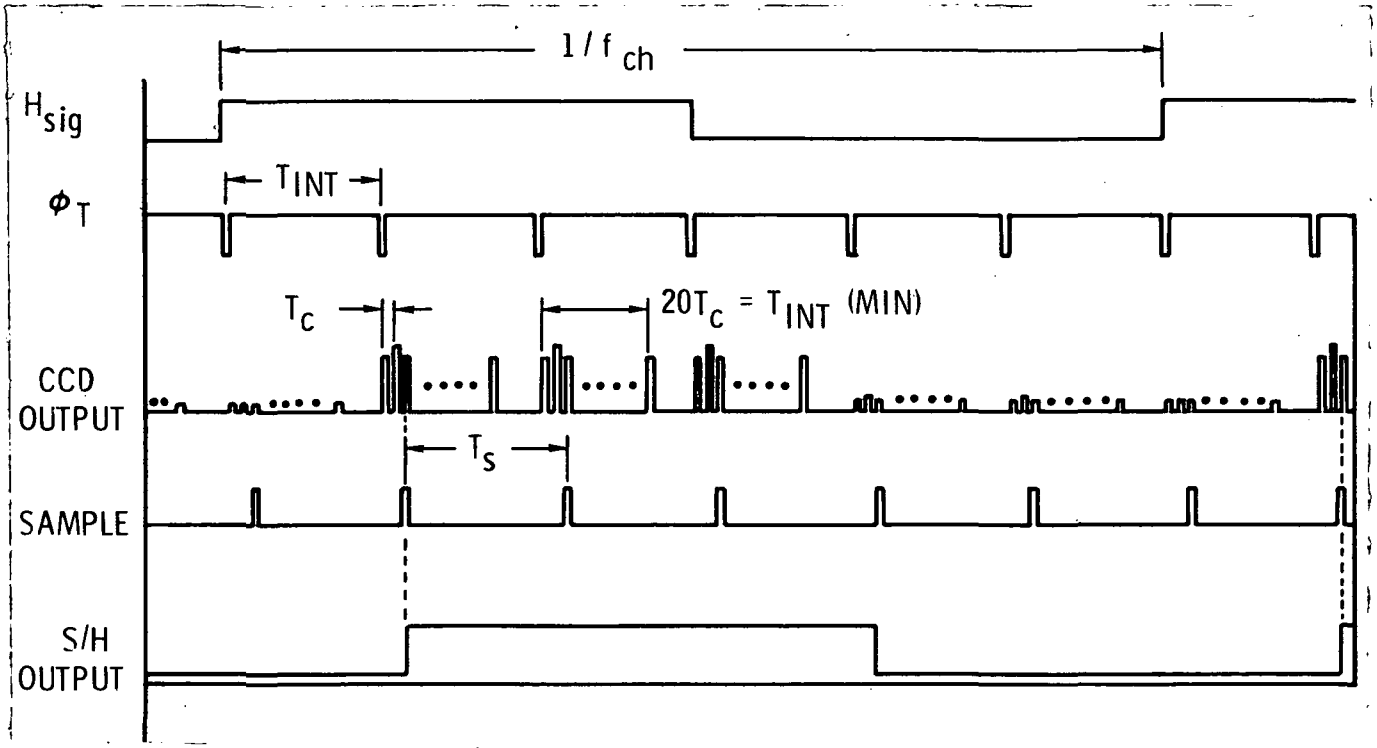


Figure 6. Timing Diagram For Sample-And-Hold 20 Element InSb CCD Array (Multiplexing Mode)

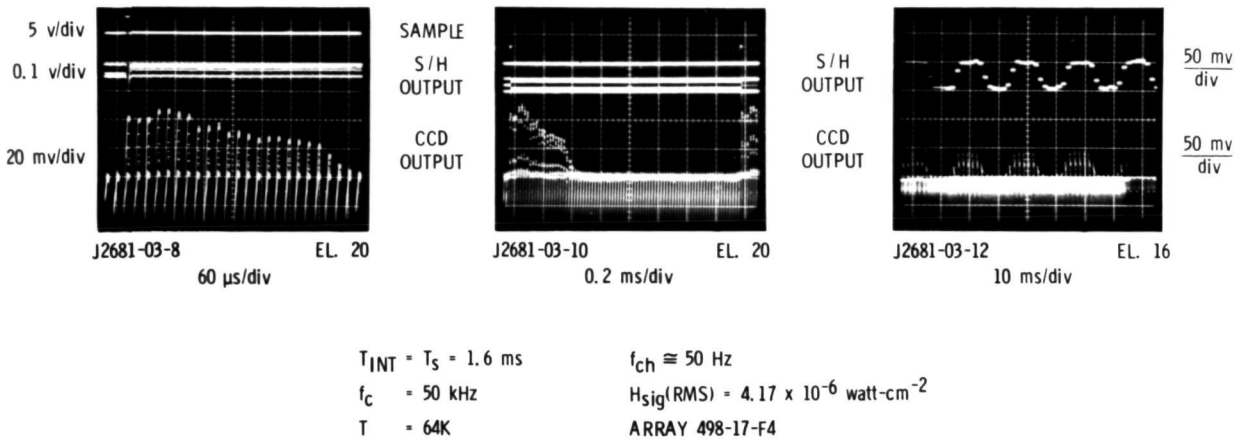


Figure 7. Sample-And-Hold of 20-Element InSb CCD Array Output

The center photograph in Figure 7 is identical to the lefthand photograph except that the time/division has been increased to show the full sample period (= T_{int}), which in this case is 1.6 msec. At the far left of the photograph is the first sample of element 20, and at the far right is the next sample.

The righthand photograph in Figure 7 shows the CCD output (lower trace) and SH output (upper trace) with the time/division increased by a further factor of 50. Each "pulse" in the lower waveform is in fact a burst of 20 output pulses (unresolved in the photograph). The chopped radiation input with $f_{ch} \cong 50$ Hz is evident in the output waveform. The upper trace is the output of a single sampled element (number 16) responding to the chopped radiation

RESPONSIVITY AND QUANTUM EFFICIENCY

The output signal voltage of the device, neglecting transfer loss, is given by

$$V_s = \frac{\eta q \lambda A_D T_{int} H_{sig} A_{v1} A_{v2}}{hcC_o} \quad \frac{\sin(\pi f_{ch} T_{int})}{(\pi f_{ch} T_{int})} \qquad (3-1)$$

where

η = quantum efficiency (carriers/photons)

q = electronic charge (coul)

λ = wavelength of (monochromatic) signal radiation (cm)

A_D = individual photogate area (cm^2)

H_{sig} = signal irradiance (w/cm^2)

A_{v1} = gain of output source-follower

A_{v2} = post-amplifier gain

h = Planck's constant

c = speed of light

C_o = total CCD output capacitance (farad)

The responsivity is simply obtained from (1) using

$$R_\lambda = \frac{V_s(\lambda)}{A_D H_{sig}} \text{ (volts/watt)} \qquad (3-2)$$

The output signal is proportional to η and inversely related to C_o; these parameters are amenable to optimization through device design and process technology, whereas the other quantities in Equation (3-1) are usually fixed by the system application.

Individual array outputs were measured with a wave analyzer tuned to the chopping frequency. First, using the FSH circuit and post-amplifier with $A_{v2} = 10$, the rms output voltage versus rms signal irradiance H_{sig} was measured with integration time held constant. Figure 8 shows that the output signal is linear with incident irradiance in accordance with Equation (3-1). The saturation level, for the test conditions listed in the figure, was 165 mv, and the measured noise was 250 $\mu v/Hz^{\frac{1}{2}}$ with the FSH, both referred to the output of the post-amplifier.

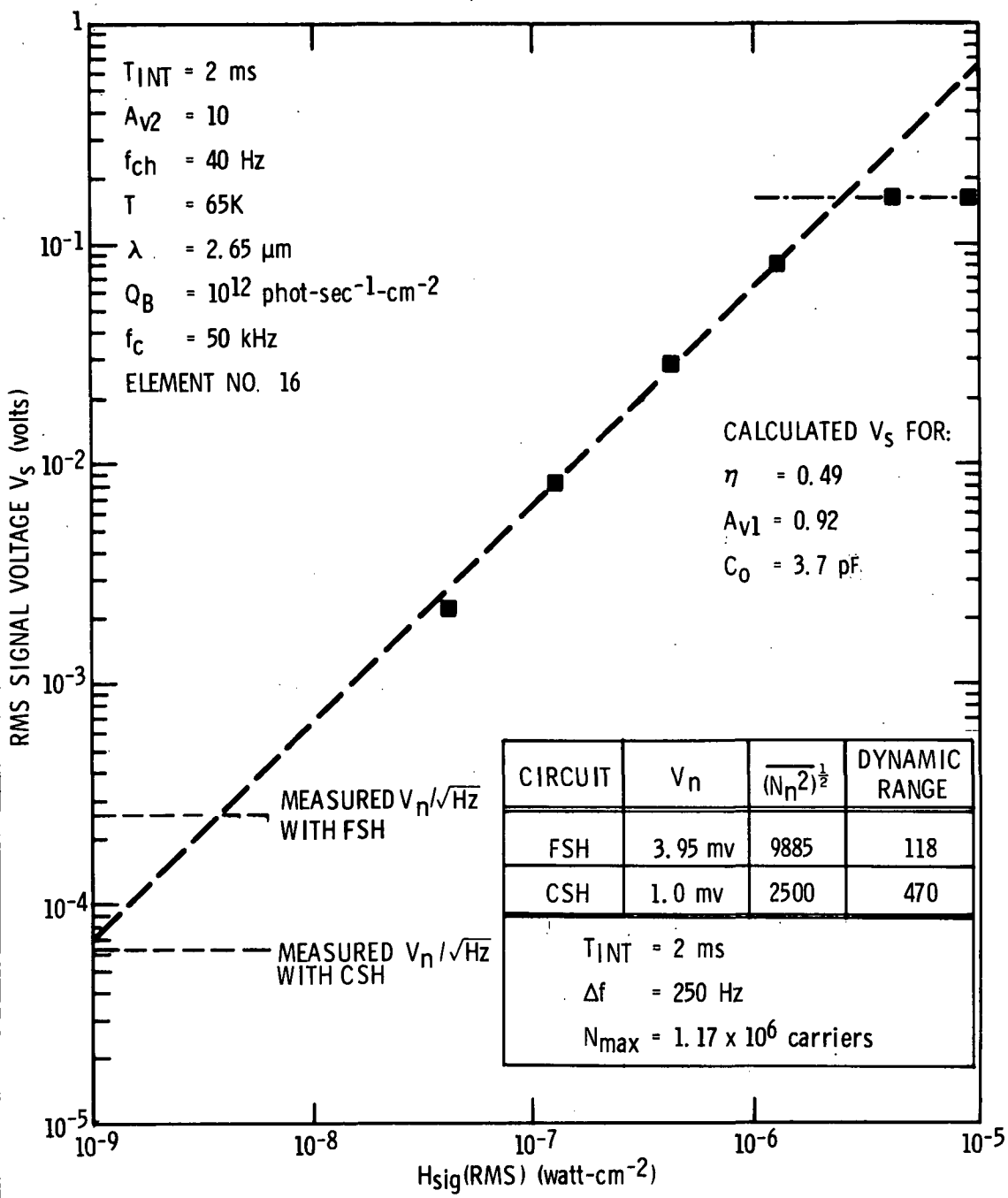


Figure 8. RMS Signal Voltage Versus Irradiance For One-Element of Array 498-17-F4

All of the quantities in Equation (3-1) are either known or measurable allowing η to be calculated from the measured signal levels. The capacitance on the output node was calculated to be 3.9 pF* from the known areas of the output junction, the output diode bonding pad and lead, gate overlaps, and the parameters of the 3N163 MOSFETs. The calculation was checked by direct measurement of C_o of a 20-element array at 77 K using a C-V plotter, with the MOSFETs biased to obtain the correct active input capacitance, yielding 3.7 pF for C_o. The gain of the output 3N163 (A_{v1}) is 0.92 for the source resistor and drain current used. Solving for η using the signal voltages in Figure 8 yields $\eta = 0.49$. For several other widely varying combinations of T_{int} and H_{sig}, calculated values of η have ranged from 0.43 to 0.50. This value of η is consistent with independent measurement of the transmission of the semitransparent gate structure (the Ti and associated SiO_2 layers). These layers were deposited on germanium substrates and their transmission and reflection measured versus wavelength; improved computer analysis of the data yielded an effective transmission of about 0.5 for the Ti photogate structure, greater than the value of 0.38 which has been estimated earlier based on a simpler calculation approach.

The responsivity of the present devices, although high, is still lower than ultimately possible because of the interim use of silicon MOSFETs in the output circuit rather than on-chip transistors. The largest contribution to the 3.7-pF output capacitance is 2.2 pF associated with the output diode bonding pad and lead, which will be eliminated with on-chip MOSFETs. The photogate structure can also be improved further, as discussed elsewhere in this report.

* The value of C_o assumed previously, 6pF, is incorrect; the source-follower and stray contributions were in error.

D* AND DYNAMIC RANGE WITH FSH

From the data in Figure 8, the detectivity may be calculated for the device operating with the FSH circuit:

$$D^*_{\lambda p} = 2\,(A_D)^{-\frac{1}{2}} \frac{V_S}{H_{sig} V_n/Hz^{\frac{1}{2}}} = 1.5 \times 10^{11} \text{cm-Hz}^{\frac{1}{2}}\text{-watt}^{-1} \qquad (3\text{-}3)$$

The prefactor of 2 in Equation (3-3) is to convert $D^*_{\lambda_1}$ at the measurement wavelength of 2.65 μm to $D^*_{\lambda p}$ at 5.3 μm. Integrating the measured narrow-band noise over frequency for T_{int} = 2 ms gives a total wideband noise at the 3N163 output of V_n = 395 μv. In terms of noise electrons this corresponds to

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} = \frac{V_n C_o}{.92q} = 9885\ e^- \qquad (3\text{-}4)$$

at the CCD output. From the saturation level of signal output voltage, the maximum charge capacity of the array is $N_{max} = 1.17 \times 10^6$ carriers. The dynamic range under the operating conditions of Figure 3-5 and with the FSH circuit is therefore

$$\text{Dynamic Range} = \frac{N_{max}}{\left(\overline{N_n^2}\right)^{\frac{1}{2}}} = 1.18 \times 10^2 \qquad (3\text{-}5)$$

CLAMPED SAMPLE-AND-HOLD AMPLIFIER

Following the measurements with the FSH, a CSH amplifier was designed, assembled, and checked out for 20-element array testing. A block diagram of the CSH circuit is shown in Figure 9 along with its measured gain and noise. The CSH amplifier, first introduced by White[14], implements the correlated double sampling (CDS) concept which is illustrated schematically in Figure 10. The dual advantages of output kTC and 1/f noise rejection were anticipated to improve the signal-to-noise ratios of the 20-element array.

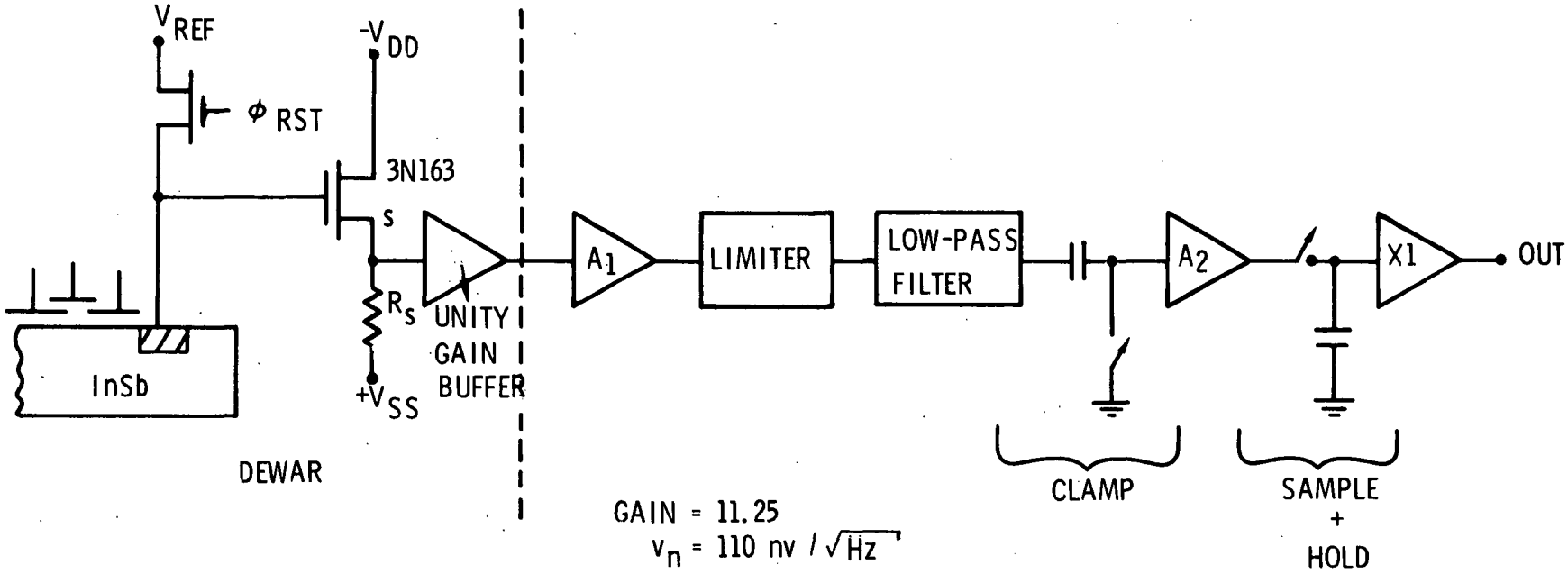


Figure 9. Clamped Sample-And-Hold Amplifier

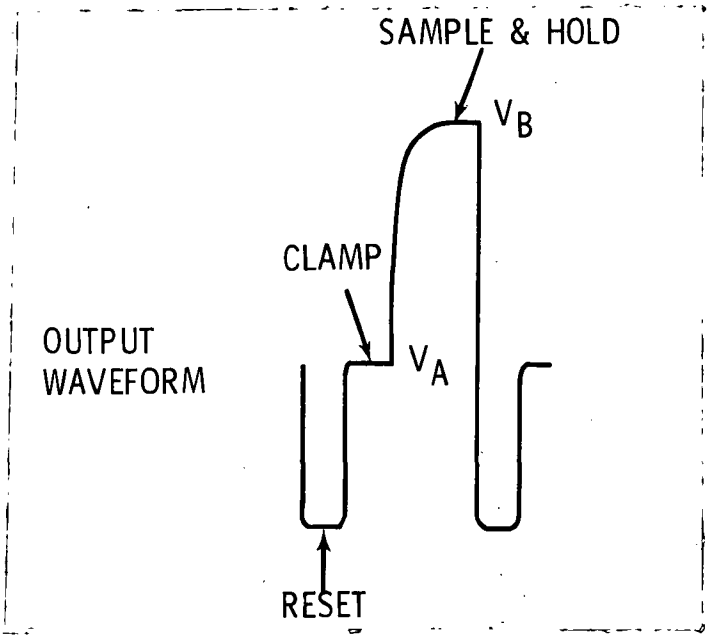


Figure 10. Correlated Double Sampling Concept. The Output of the Clamped Sample-And-Hold is (V_B-V_A) Times the Gain.

The method of correlated double sampling is an effective means to accurately detect signal charge present at the output of a CCD multiplexer. CDS involves setting a capacitor to some reference level, isolating the capacitor, and then transferring signal charge from the output diode to the capacitor. The voltage across the capacitor becomes representative of the signal charge present on the collection diode of the multiplexer. This is then sampled and held for readout. The foregoing is accomplished by means of a CSH circuit.

There are three advantages to this method:

1. Clock feedthrough is eliminated. The clamping and sampling occur at instants when clock pulses are not changing.
2. Most kTC noise of switching is removed. Supply noise and switching noise are present on the reference node during the clamp phase, but when this node is later sampled after charge transfer from the output diode to the capacitor, the noise is subtracted away leaving only the signal and noise associated with transfer from the output diode, which is quite small.

3. The transfer function of a SH circuit is such that it suppresses low frequency noise components (1/f noise). The transfer function of a SH circuit is $1-e^{-sT}$, where T is the switching time between the clamp and the sample. This translates into a sin(x) filter which gives little response near zero frequency. The low-pass and bandpass sections are multiplied with this SH transfer function to give the over CSH transfer function.

Figure 11 is a schematic diagram of the CSH amplifier with component values selected for operation of the circuit at clock frequencies on the order of 500 Hz. For other clock frequencies, the passbands of the individual filter stages should be readjusted in order to pass all of the fundamental at the anticipated clock frequency. If the passband is too narrow or mislocated with respect to the clock frequency, the signal will be distorted. If the passband is too large then wideband noise will be folded into the signal, defeating the function of the circuit.

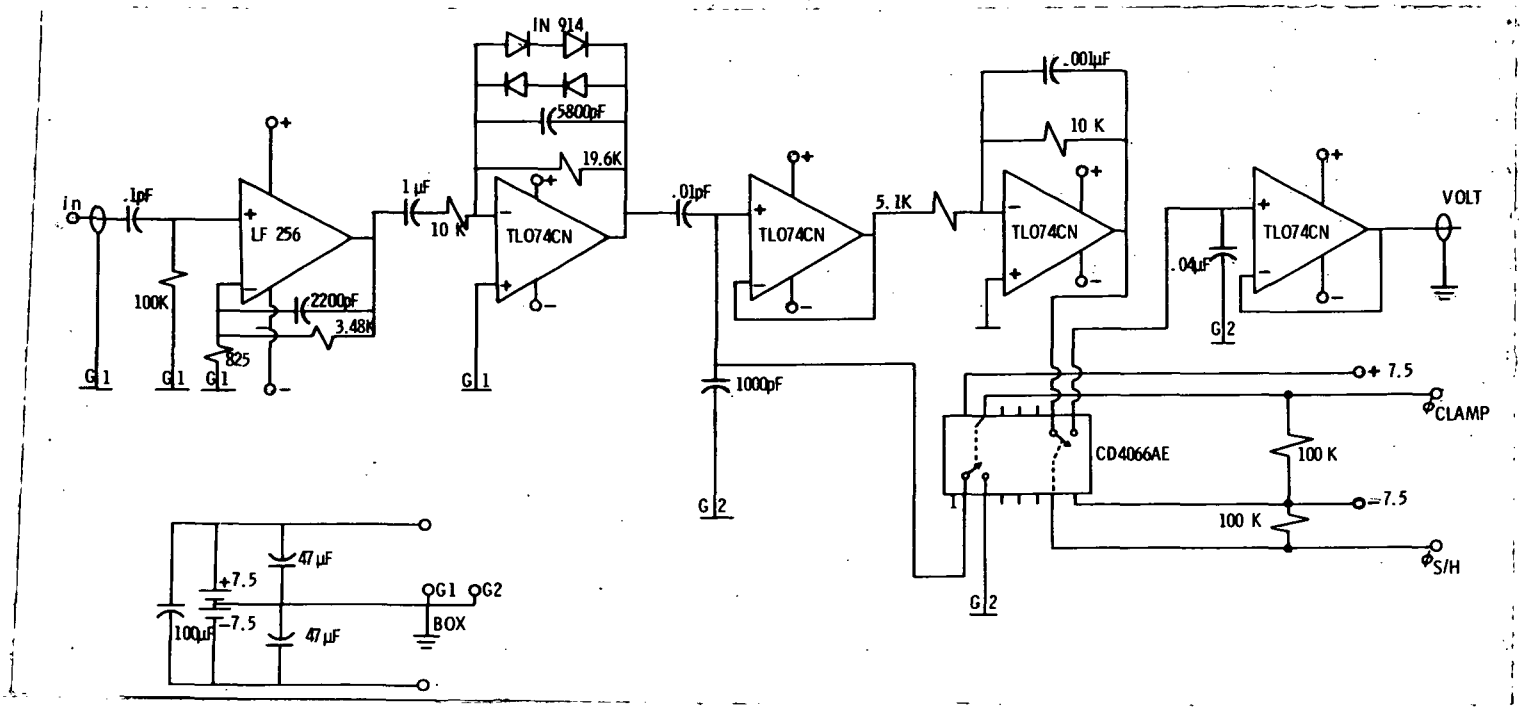


Figure 11. Clamped Sample-And-Hold Schematic

Timing relationships are shown in Figure 12; the clock voltage on the last clock gate preceding the output diode is ϕ_3. Just before ϕ_3 is turned off, releasing charge into the transfer gate, the capacitor is switched to V_{ref} with ϕ_{RESET} and the capacitor is clamped to this potential. Charge is then dumped on to the capacitor with ϕ_T and later sampled with ϕ_{SH}.

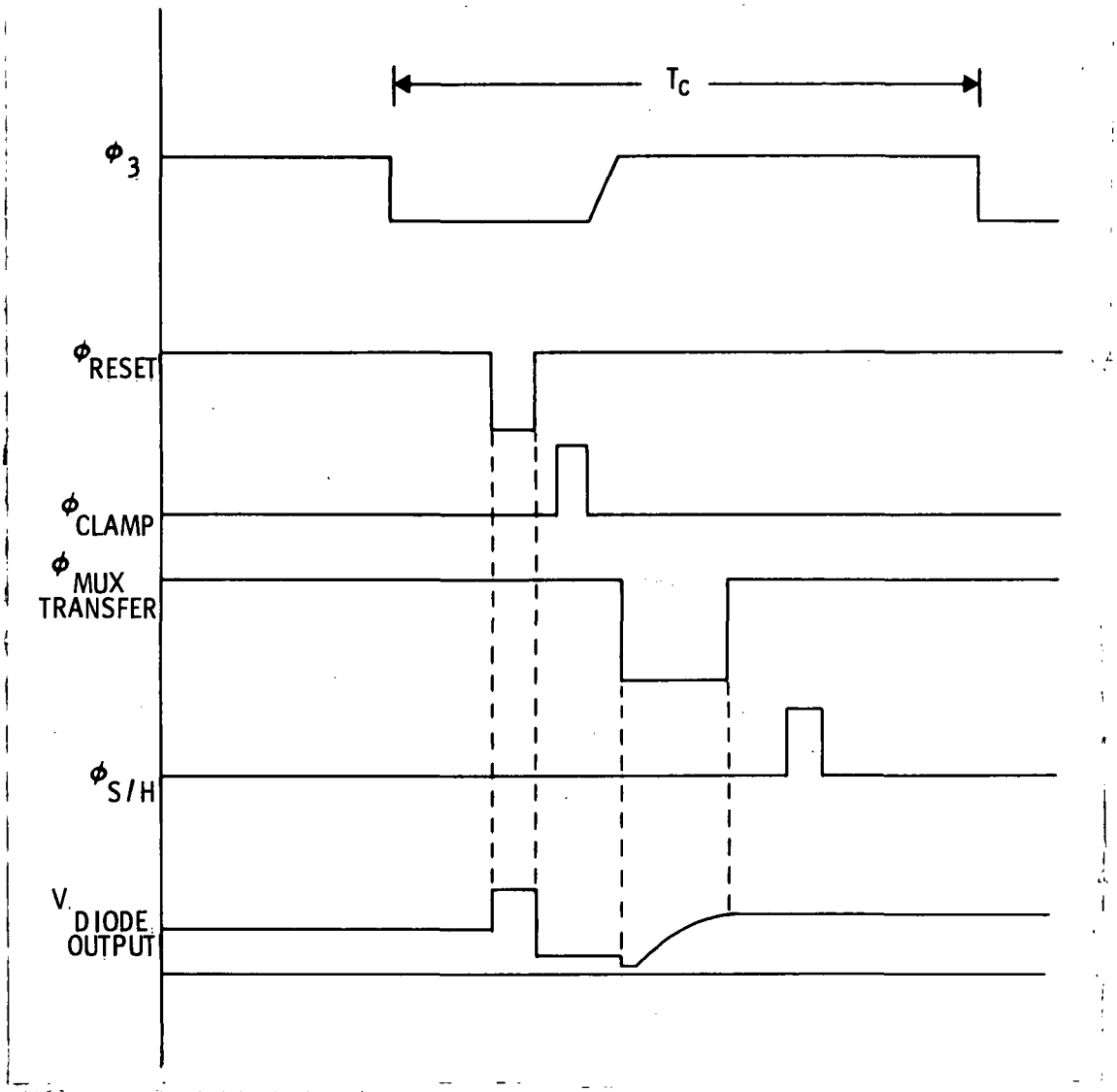


Figure 12. Clock Diagram For CSH Amplifier

D* AND DYNAMIC RANGE WITH CSH

Using the CSH, D* was measured for each element in array 498-17-F4 in the multiplexing mode at T = 65 K, f_c = 5 kHz, and T_{int} = 5 msec, with the results shown in Figure 13. The signal flux was chopped at 15 Hz so that the measurements were not affected by the sin $(\pi f T_{int})/(\pi f T_{int})$ roll off. Noise was measured using a narrow bandwidth Δf = 3 Hz centered at 15 Hz, with the blackbody aperture blanked off. The D* at the peak wavelength λ_p = 5.3 μm was calculated from Equation (3-3). The average $D^*_{\lambda p}$ for the array is 6.4×10^{11} cm-Hz$^{\frac{1}{2}}$/watt, showing a significant improvement over the D* measured with the FSH amplifier.

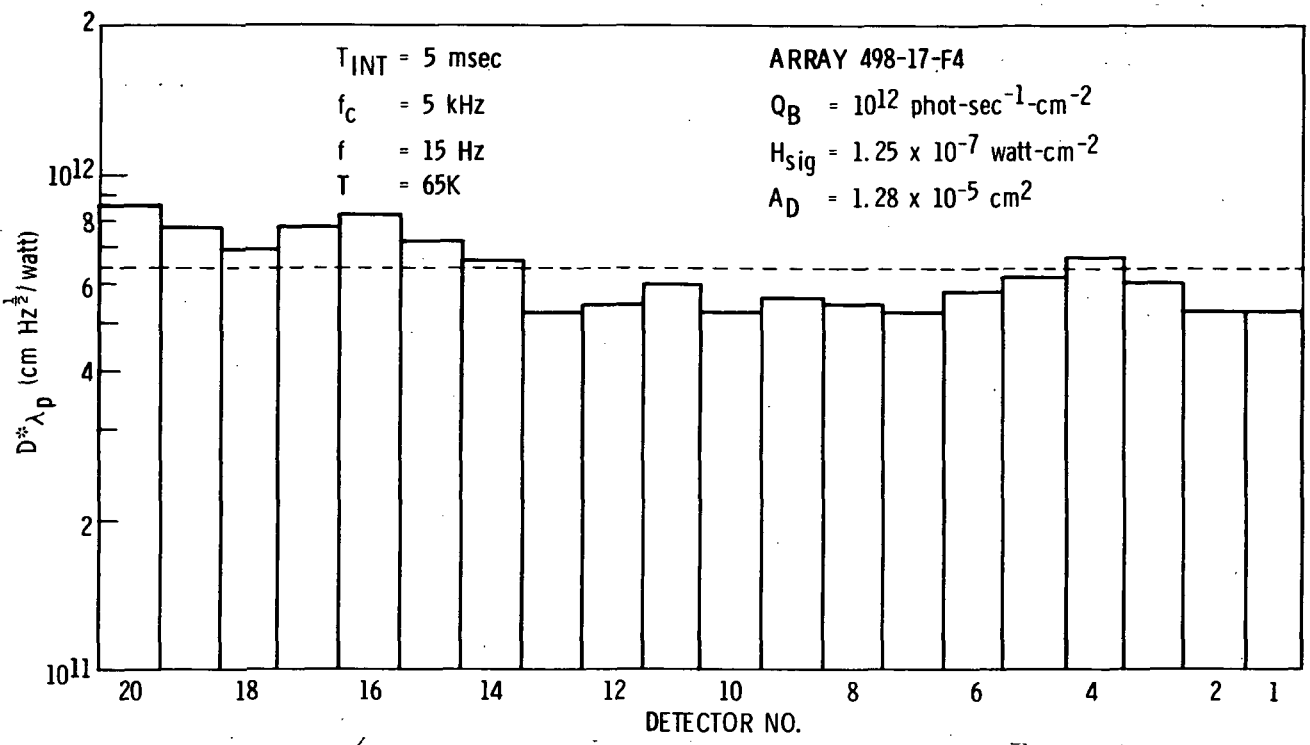


Figure 13. Measured D* of Array 498-17-F4 in Multiplexing Mode

The elements with the highest D* are nearer the output end of the array. For element 16, for example, with $H_{sig} = 1.25 \times 10^{-7}$ watt-cm^{-2}, the measured signal and noise levels at the CSH output were

$$V_s = 20.5 \text{ mv}$$
$$V_n = 194 \ \mu\text{v in } \Delta f = 3 \text{ Hz}$$

giving

$$D^*_{\lambda p} = 2\left(\frac{3}{1.28 \times 10^{-5}}\right)^{\frac{1}{2}} \left(\frac{20.5}{(0.194)(1.25 \times 10^{-7})}\right) \tag{3-6}$$
$$= 8.2 \times 10^{11} \text{ cm-Hz}^{\frac{1}{2}}\text{/watt}$$

The wideband noise referred to the 3N163 output is 100 μv. Reflecting this back to the CCD in terms of noise electrons gives

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} = \frac{V_n C_o}{0.92q} = 2500 \text{ e}^- \tag{3-7}$$

giving an improved dynamic range with the CSH of

$$\text{D.R.} = \frac{1.17 \times 10^6}{2.5 \times 10^3} = 470. \tag{3-8}$$

The measured noise of 2500 electrons is higher by about a factor of two than the sum of all calculated CCD noise variances, where the contributions of photon, detector thermal, detector 1/f, surface state, kTC, output thermal, and output 1/f noise were included. Because of the low-background flux ($Q_B = 10^{12}$ phot-sec^{-1}-cm^{-2}) utilized in the tests, the photon noise is small,

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} = (\eta Q_B A_D T_{int})^{\frac{1}{2}} = 113 \text{ carriers.} \tag{3-9}$$

Likewise the noise due to fast surface states,

$$\left(\overline{N_n^2}\right)^{\frac{1}{2}} = (kTA_{CCD}N_{SS}\ell n2/q)^{\frac{1}{2}} = 654 \text{ carriers,} \tag{3-10}$$

is not believed to be the dominant source of the noise. Here A_{CCD} is the total CCD channel area (1.1×10^{-3} cm^2) and a conservative value of N_{SS}, 10^{11} cm^{-2}-eV^{-1}, was used. The excess noise is believed to originate from noise on the various clock drivers.

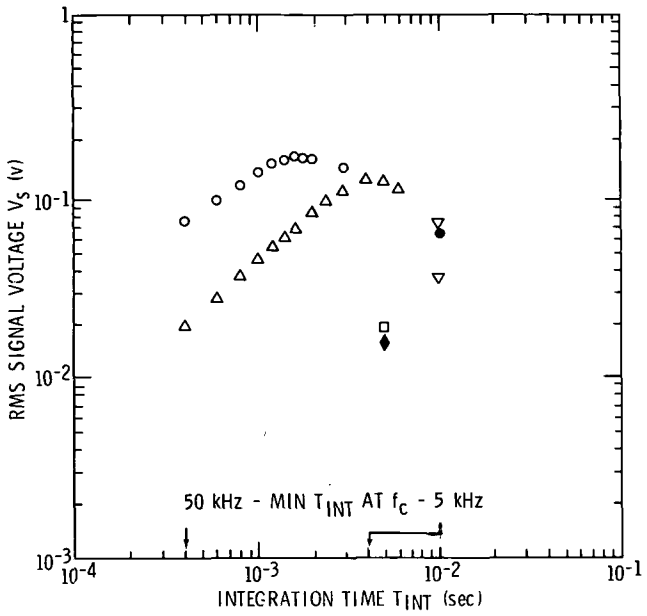
Noise on one pulse generator, the output reset (ϕ_{RST}) clock, is particularly critical, as it will capacitatively couple to the output node through the relatively large gate-to-source capacitance (0.6 pF) of the 3N163 MOSFET. Measurement of the noise on the voltages of several commercially-available clock drivers has shown that this source can account for several hundred to thousands of noise electrons, depending on the effective bandwidth at the CCD output. More study is needed, but present evidence suggests that such system noise sources, coupled with output circuit characteristics, are at least partially responsible for the excess noise. The achieved noise levels, however, result in promising D* and dynamic range.

TDI

D* was also measured for the 20-element array clocked in TDI at f_c = 500 Hz, with a signal irradiance $H_{sig}(RMS) = 1.24 \times 10^{-8}$ watt-cm^{-2}, and T = 59K. Narrow-band noise was again measured with the wave analyzer as a function of frequency. At f = 200 Hz, the TDI signal voltage at the sample-and-hold output was 6.0 mv rms and the noise voltage was 34 $\mu v/Hz^{\frac{1}{2}}$. Substituting in Equation (3-3) yields a peak detectivity $D^*_{\lambda p}(TDI) = 8 \times 10^{12}$ cm-Hz$^{\frac{1}{2}}$/watt.

SIGNAL DEPENDENCE ON INTEGRATION TIME

From Equation (3-1), the signal voltage of the device should increase linearly with the integration time for a constant input irradiance. Measurements were made on array 498-17-F4 to verify this dependence. Figure 14 plots measured rms signal voltage versus integration time for four different levels of input irradiance as called out in the table. The array was clocked at two different frequencies, 50 kHz and 5 kHz. The minimum integration times for these two values of f_c, from the relationship T_{int} (min) = 20 T_c, are shown by arrows on the T_{int} scale. A linear variation of V_s with T_{int} is evident in Figure 14, as is a saturation level of about 150 mv.



$\lambda = 2.65\ \mu m$

$Q_B = 10^{12}$ phot-sec^{-1}-cm^{-2}

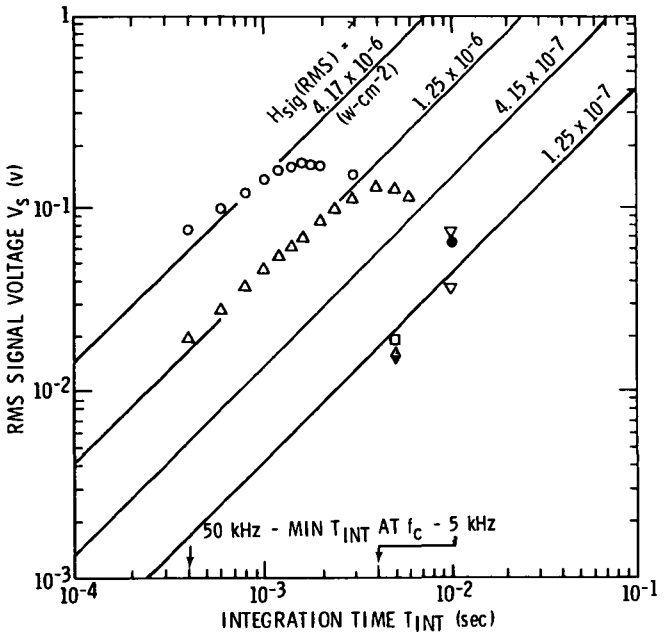
$A_{V2} = 10$

SYM	EL	TEMP (°K)	f_c (kHz)	f_{ch} (Hz)	H_{sig}(RMS) (w-cm^{-2})	OUTPUT CIRCUIT
o	16	65	50	40	4.17×10^{-6}	FSH
△	16	65	50	40	1.25×10^{-6}	FSH
●	17	64	5	15	4.15×10^{-7}	CSH
▽	17	64	5	15	4.15×10^{-7} / 1.25×10^{-7}	NONE
♦	16	64	5	15	1.25×10^{-7}	FSH
□	16	64	5	15	1.25×10^{-7}	CSH

Figure 14. RMS Signal Voltage Versus Integration Time (Multiplexing Mode) 20-Element Array 498-17-F4

Figure 15 shows the same data but calculated signal curves from Equation (3-1) have been added for the four rms input irradiance levels. Again, good agreeement with the data is obtained using $\eta \cong 0.5$ and $C_o = 3.7$ pf along with the other known quantities.

The saturation effect observed in the data of Figure 15 is due to detector dark current and behaves as expected, as shown in Figure 3-13. First, for a constant f_{ch}, as T_{int} is increased the $\sin(\pi f_{ch} T_{int})/(\pi f_{ch} T_{int})$ term in Equation (3-1) will roll off the signal as T_{int} approaches T_{ch}. This factor is shown for the 1.25×10^{-6} watt/cm^2 curve and $f_{ch} = 40$ Hz by the broken curve in Figure 16. This clearly shows that the saturation effect in the data is due to a mechanism other than the sin x/x term. The solid curve labelled V_s(max) in Figure 16, obtained from the equation given in the figure, shows that the mechanism is in fact dark current generation in the detector. The equation expresses the fact that the maximum signal charge Q_s (max) that can be accommodated is the difference between the total charge capacity Q_T(max) and the charge generated by the sum of background and dark current, which increases linearly with T_{int}.

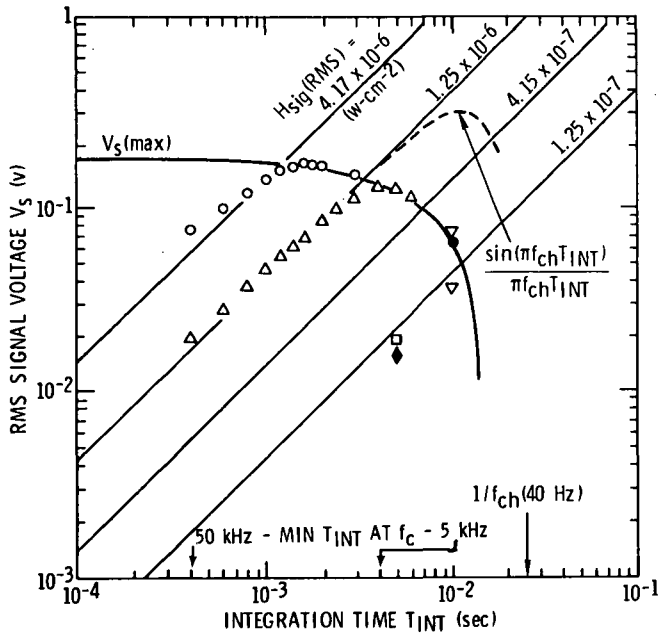


Calculated Curves:

$$V_s = \frac{\eta q \lambda A_D T_{int} H_{sig} A_{V1} A_{V2}}{hcC_o}$$

η = 0.5
λ = 2.65 μm
A_D = 1.28 × 10^{-5} cm^2
A_{V1} = 0.92
A_{V2} = 10
C_o = 3.7 pF

Figure 15. RMS Signal Voltage Versus Integration Time (Multiplexing Mode) 20-Element Array 498-17-F4



V_s (max) Calculated From:

$$Q_s (max) = Q_T (max) - A_D T_{int} x$$

where $x = \left[q\eta Q_B + \left(\frac{A_{gen}}{A_D}\right) J_D \right]$

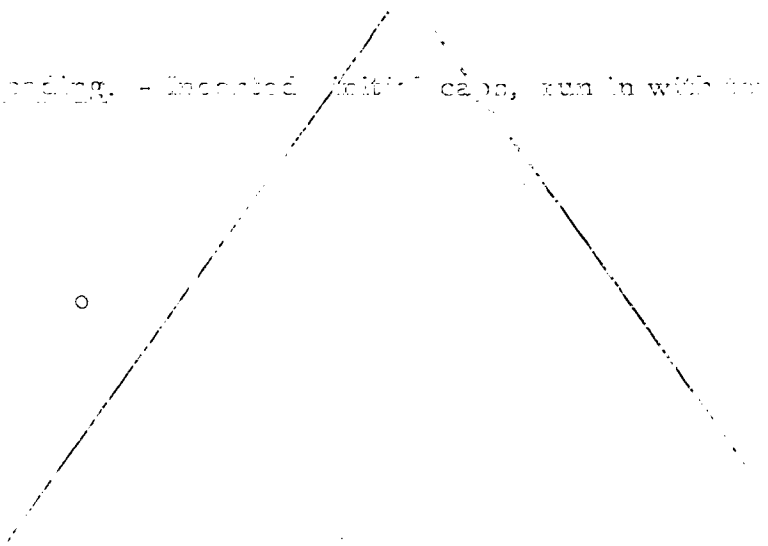
Q_T (max) = 2 × 10^{-13} coul

J_D (65K) = 6.9 × 10^{-7} a-cm^{-2}

A_{gen}/A_D = 1.43

Figure 16. RMS Signal Voltage Versus Integration Time (Multiplexing Mode) 20-Element Array 498-17-F4

The A_{gen}/A_D factor accounts for the fact that the dark current generation area is larger than the photogate area due to the area of the (opaque) bus line. The storage time at 65K for the device lot in question is approximately 100 msec, which corresponds to a dark current density of 0.7 $\mu a/cm^2$. This is seen to give an excellent fit to the measured saturation characteristic.



Section 4

NEXT GENERATION MONOLITHIC CCIRID CHIP (SBRC 8587) DESIGN AND PROCESS DEVELOPMENT

A major portion of this contract effort addressed circuit design, mask procurement, and process development of a next-generation area and linear array chip. This new chip was designated the SBRC 8587. Detailed circuit layout of the chip was performed by the Hughes Carlsbad Research Center in Carlsbad, CA. Circuit digitizing, plotting, pattern generation, and mask fabrication were performed by Microfab of Palo Alto, CA.

SBRC 8587 CHIP LAYOUT

An overall layout of the new chip is shown in Figure 17. A corresponding photograph from the mask vendor's digitized layout is shown in Figure 18. The overall chip size is 3912 μm (154 mils) by 4953 μm (195 mils) and includes the following devices:

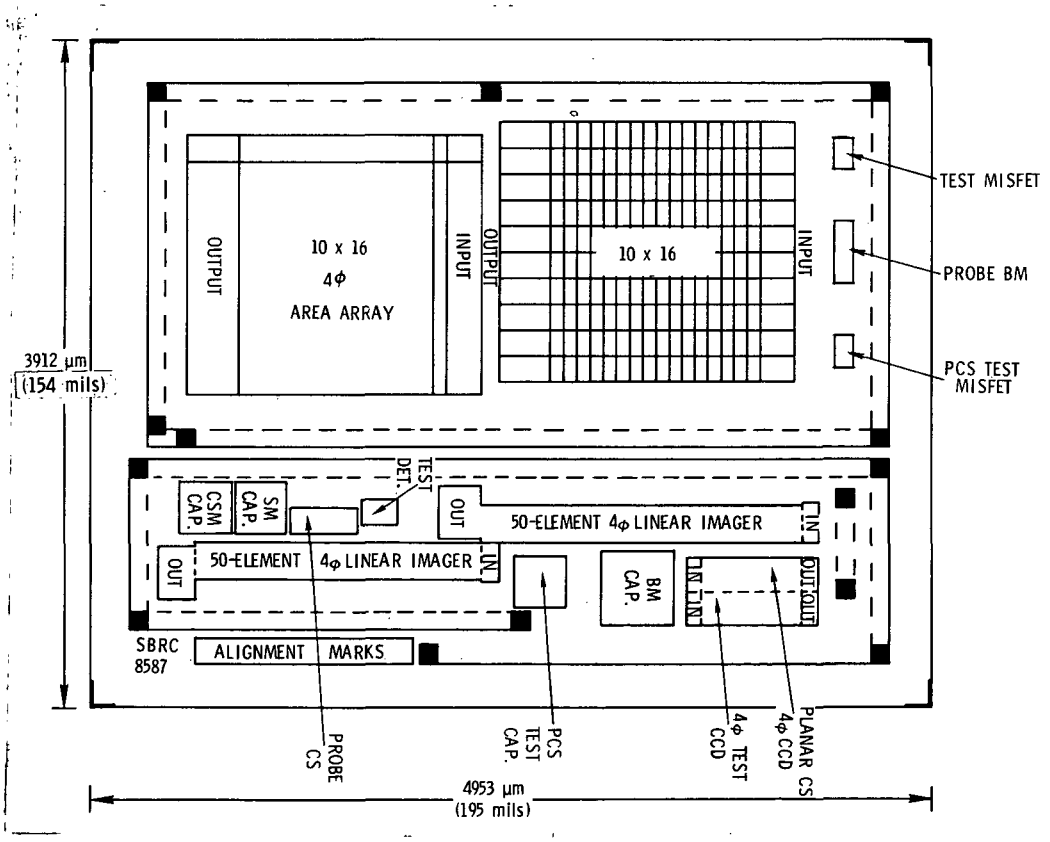


Figure 17. Next Generation (SBRC 8587) Monolithic Area Array Chip

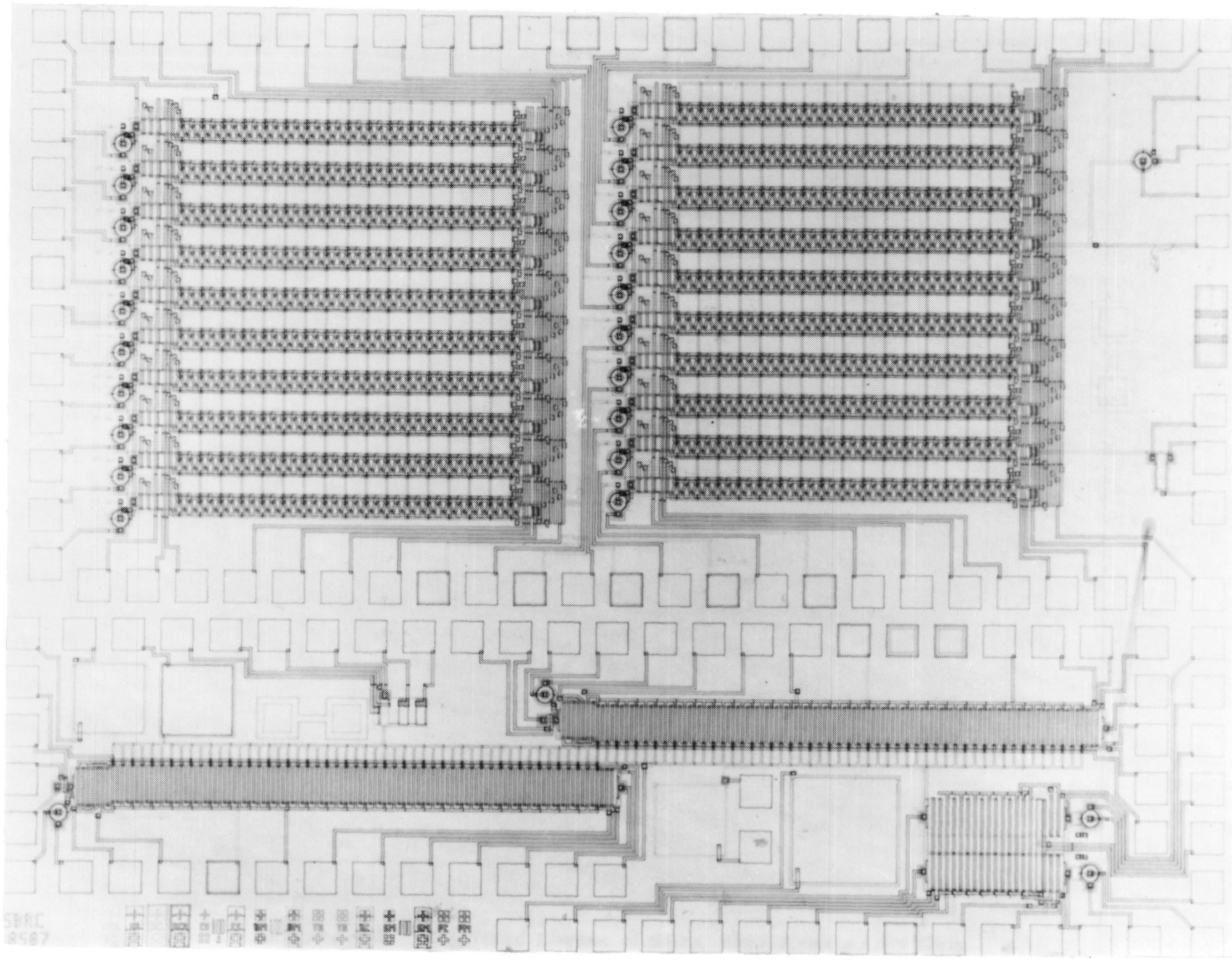


Figure 18. Digitized Layout of SBRC 8587 Area Array Chip

1. a 20-row by 16-detector time-delay-and-integration (20 x 16 TDI) area array;
2. a 100-element linear CCD imager;
3. an 8-bit surface-channel CCD shift register in parallel with a similar CCD with a planar n^+ -n' channel stop; and
4. a single-bit CCD test detector for quantum efficiency measurement.

Several test devices are also included for in-process oxide analysis, etch depth determination and MISFET characterization, including:

1. guarded capacitors for C-V characterization of each oxide layer;
2. a dumbbell-geometry resistor for probe testing to determine oxide etch completion at the channel stop and buried metal levels;
3. a test MISFET with an identical structure to the array output device MISFET; and
4. a test MISFET in a bar configuration to determine the channel stop characteristics of an n^+ -n planar channel stop.

The major devices of interest for future applications are the 20 x 16 TDI area array and the 100-element linear imager.

20 X 16 TDI AREA ARRAY

The majority of the 8587 chip area is devoted to a 20-line by 16-element TDI imaging array. The array consists of two 10 x 16 arrays which have been aligned with respect to each other in the direction of TDI except staggered one-half unit cell spacing (one detector spacing) to yield a fill factor of approximately 100% when used as a scanning imager.

The basic problem presented to the designer when expanding a linear monolithic CCD array design to a two-dimensional monolithic array is where to locate the clock lines for each row. This is particularly challenging for monolithic intrinsic infared arrays for which 4-phase clocking is optimal. On the 8585-design 20-element array, for example, the four clock lines are brought out on either side of the active region of the device which, if extended to an area array, would result in too low an area efficiency.

With this problem in mind, the 20 x 16 TDI area array was designed with a 4ϕ meander[15] (or zig-zag) CCD configuration. In the meander layout,

the gates run parallel to the long axis of the CCD channel rather than perpendicular to it, and in effect serve as their own clock bus lines. That is, the clock lines are located in the CCD channel areas and no additional chip area is needed for clock line routing. An additional advantage of this type of CCD and detector input structure is that it can be laid out without contact windows in the unit cell. This type of CCD geometry has been successfully used on several Hughes Aircraft Company silicon CCD area arrays.

The overall 20 x 16 TDI array unit cell is shown in Figure 19. The unit cell covers an area 152.4 μm (6 mils) wide by 76.2 μm (3 mils) in length. It consists of a single transparent photogate detector element, a transfer gate, and two bits of a zig-zag CCD bordered by a field plate channel stop. The detector is 68.6 μm (2.7 mils) wide by 71.1 μm (2.8 mils) in length covering approximately 42% of the unit cell area. Minimum geometry used throughout for lines and spaces is 5 μm (0.2 mil).

20 X 16 TDI AREA ARRAY OPERATION ANALYSIS

Operation of the detector input and readout structure is similar to

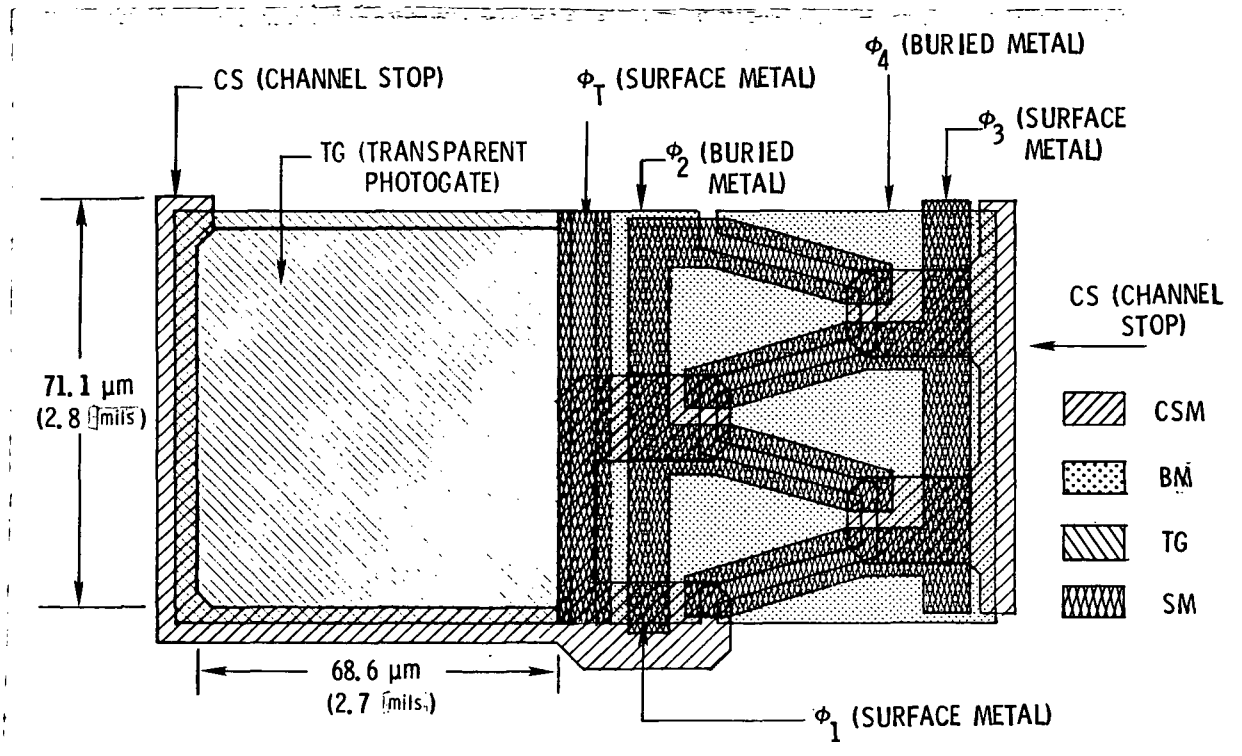


Figure 19. Unit Cell of 20 x 16 Area Array Next Generation Monolithic Intrinsic Chip

that of the SBRC 8585 20-element linear imager. The transparent photogate regions are biased into deep depletion. As infrared radiation is absorbed in the substrate, electron-hole pairs are created, and the holes (minority carriers) are collected and stored under the depleted photogates for the case of a p-channel device (i.e., InSb).

The successful operation of the photogate detector on the SBRC 8585 20-element imager has supported use of the photogate as both the detector and charge integrator, as opposed to using a separate store well as originally proposed. The advantages are that space is saved, imager efficiency is increased, and noise and dark current resulting from the channel thermal and depletion regions of a separate store well are decreased. A small nonlinearity of quantum efficiency versus background and integration time is experienced with the photogate detector-integrator, but will not severely affect performance.

At the end of an integration period, the charge under the photogates is transferred into the CCD wells by pulsing the transfer gate. While the next integration is taking place, the charge is transferred along the CCD by clocking the CCD gates in a two-phase sequence. The four CCD gates per bit are not electrically connected allowing two phase clocking with different absolute potentials on each of the two gates per phase, thereby maximizing flexibility and usable range of threshold potentials.

The zig-zag CCD configuration operates in a standard two-phase manner with the charge moving from side to side instead of straight down the channel as in a standard CCD layout. This layout allows the gate electrodes for each phase to be a single piece of conductor instead of having to make contacts at each gate as in the two dimensional array format. As an additional benefit, the back edge of the zig-zag CCD makes an excellent port for transferring charge from the detectors into the CCD.

An increase in the required transfer time for the zig-zag CCD reduces

the maximum frequency of operation. However, using a pessimistic evaluation of transfer time by ignoring the helpful effects of fringing fields and self-induced drift, while considering only thermal diffusion, the transfer time is predicted to be well within that required for typical scan applications. Thermal diffusion mechanisms yield a charge versus time relationship as follows:

$$\text{Charge Transfer Inefficiency} = \epsilon = \frac{N(t)}{N(o)} \cong \frac{8}{\pi^2} \exp\left(\frac{-\pi^2 Dt}{4L^2}\right) \qquad (4\text{-}1)$$

where D is the diffusivity of holes and L is the charge transfer length (25.4 μm). For a charge transfer efficiency of 0.999 (ϵ = 0.001), the transfer time required is 13.3 μsec for a hole mobility of 200 cm^2/v-sec at 77 K. This corresponds to a clock frequency of 75.4 kHz. Past experience with silicon CCDs has shown actual performance many times greater than predicted using thermal diffusion calculations alone. Therefore, it is believed that the zig-zag CCD should have more than sufficient speed for most imaging applications.

The signal-to-noise performance and the maximum background versus clock rate for this imager were also analyzed. Figure 20 is a graph of the calculated output noise voltage versus background for a clock rate adjusted to give a 25% full bucket of charge at the output. As can be seen, the signal-to-noise performance should be near the background limited performance, if the clock rate and bandwidth are properly adjusted. The output 1/f noise may be reduced by the use of correlated double sampling. The calculated maximum background versus clock frequency is shown in Figure 21. Moderately high backgrounds, as would be found for a typical 3- to 5- μm 300 K scanning system, can be accommodated by the imager at clock frequencies within the CCD's capabilities.

20 X 16 TDI AREA ARRAY CHARGE SPLITTING OPTION

A second channel stop mask was also designed and procured. This mask adds an additional channel stop segment in the photogate region which splits the detector in half and uses one bit per detector to split the signal,

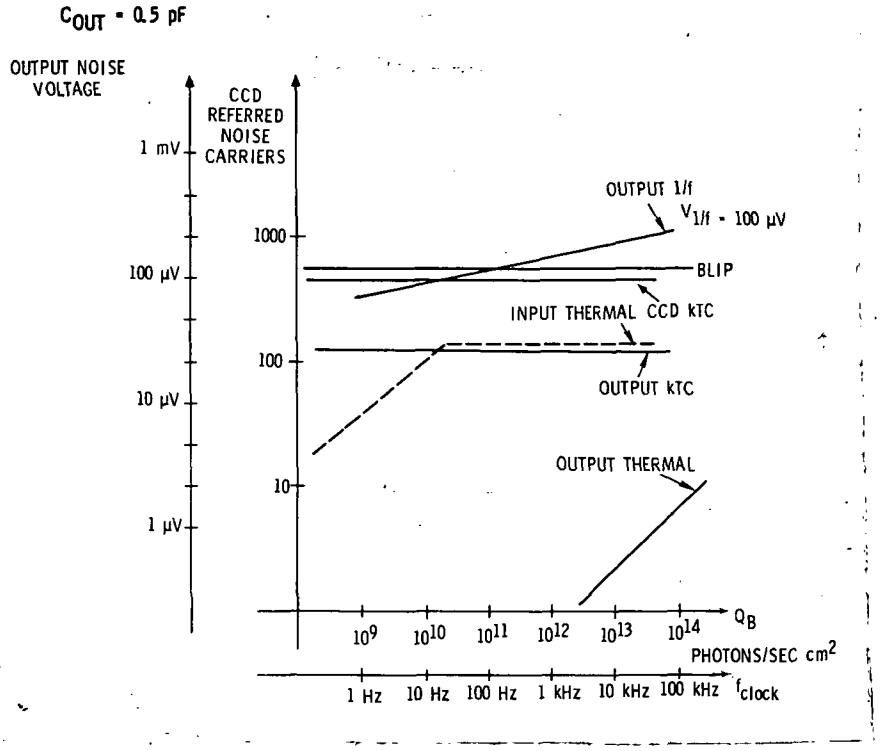


Figure 20. Calculated Noise Performance for 20 x 16 TDI Imager

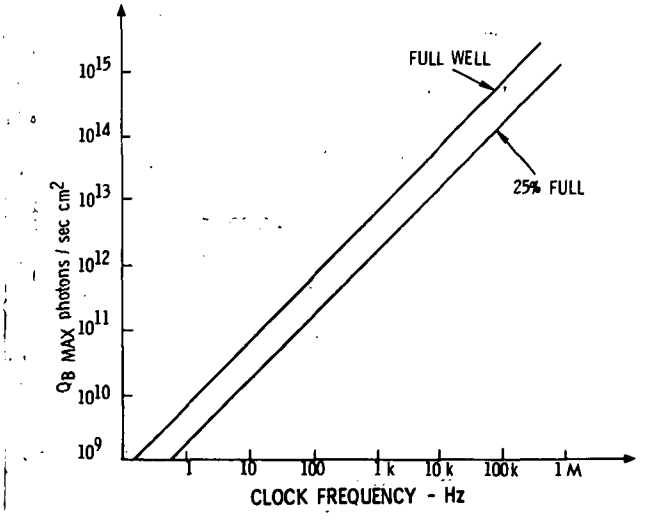


Figure 21. Calculated Maximum Background Versus Clock Frequency for the 20 x 16 TDI Imager

4 7

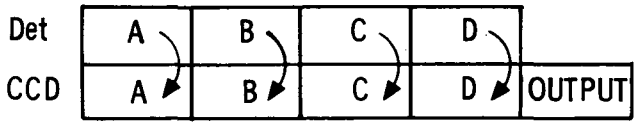
charge into two equal parts prior to inputting into the CCD register. When operating in the charge splitting mode, one detector images and integrates charge which is transferred and read at the output as signal, while the other collects a nearly equal charge to be used to effectively boost the charge transfer efficiency. The effect of this additional charge on the effective CCD performance has been analyzed as shown in Figure 22.

Consider a two-element imager being read out with a four-bit CCD. If each element consists of two detectors, which are much smaller than the optical blur diameter, then the charge integrated under them will be approximately equal. When the charge is transferred from the detectors into the CCD, the resultant charge pattern shown in Figure 22(a) is formed in the CCD; A is the desired charge from the first detector; A is equal to B, the precursor to A: C is the second detector whose charge is read at the output with D as its precursor. Figure 22 (b) shows a tabulation of the charge distribution for various stages in the transfer to the output. As the dominant charge packet from detector A reaches the output (after 4 transfers), the packet contains charge from detectors A, B, C, and D. Since A is approximately equal to B the net charge from detector A and B is $\eta^4 A + 4\epsilon\eta^3 A$ where η is the charge transfer efficiency and $\epsilon = 1 - \eta$. This is the signal charge term. The crosstalk terms are $6\epsilon^2\eta^2 C + 4\epsilon^3\eta D$ which, as η approaches unity, is equal to $\approx 6\epsilon^2 C$. In general, the degradation factor for n transfers can be written as

$$\text{degradation} = 1 - \eta^{n-1}(1 + (n-1)\epsilon) \qquad (4\text{-}2)$$

$$\text{and crosstalk} \cong \binom{n}{n-2}\epsilon^2\eta^{n-2} \qquad (4\text{-}3)$$

where n is the number of bits between the detector input and the output. For the 32-bit CCD (16 detectors), the net degradation of the last detector would be but 1.1% for $\eta = 0.995$. The crosstalk would be approximately 1%. If the two detector unit cell were not used, but still using two CCD bits per detector, the degradation and cross talk would be 14.8% and 1%, respectively.



a) Two Cell Imager with 2 detectors per unit cell

	A	B	C	D	Output	
After first transfer	ϵA	ηA ϵB	ηB ϵC	ηC ϵD	ηD	
After second transfer	$\epsilon^2 A$	$2\epsilon\eta A$ $\epsilon^2 B$	$\eta^2 A$ $2\epsilon\eta B$ $\epsilon^2 C$	$\eta^2 B$ $2\epsilon\eta C$ $\epsilon^2 D$	$\eta^2 C$ $2\epsilon\eta C$	Output from second unit cell
After third transfer	$\epsilon^3 A$	$3\epsilon^2\eta A$ $\epsilon^3 B$	$3\epsilon\eta^2 A$ $3\epsilon\eta^2 B$ $\epsilon^3 C$	$\eta^3 A$ $3\epsilon^2\eta B$ $3\epsilon^2\eta C$ $\epsilon^3 D$	$\eta^3 B$ $3\epsilon\eta^2 C$ $3\epsilon^2\eta D$	
After fourth transfer	$\epsilon^4 A$	$4\epsilon^3\eta A$ $\epsilon^4 B$	$6\epsilon^2\eta^2 A$ $4\epsilon^3\eta B$ $\epsilon^4 C$	$4\epsilon\eta^3 A$ $6\epsilon^2\eta B$ $4\epsilon^3\eta B$ $\epsilon^4 D$	$\eta^4 A$ $4\epsilon\eta^3 B$ $6\epsilon^2\eta^2 C$ $4\epsilon^3\eta D$	Output from first unit cell

b) Charge distribution in each bucket and at output after each transfer

Figure 22. Effect of Charge on CCD Performance

If only one bit per detector were used, the degradation and crosstalk would be 7.7% and 7.4%, respectively. Thus, it is concluded that the best readout performance would be obtained by using two detectors per unit cell.

The effect of using such a scheme for present devices which have limited CTE (0.995) would be that the first bit would precharge the surface states in the depletion well to near the exact level of the second bit. Then, the charge lost by the first bit is picked up by the second bit. Since this charge is equal to the charge the second bit would lose, the second bit would not be degraded. The net effect would be that the effective CTE would be approximately equal to the square root of the true CTE.

20 X 16 TDI AREA ARRAY INPUT AND OUTPUT CIRCUITS

The 20 x 16 TDI array input circuit consists of a standard three-gate pulsed diffusion fill-and-spill configuration. The input will be primarily used for testing the CCD register while also being available to inject a small fat zero charge to optimize charge transfer efficiency. The output structure of the area array has been configured in a manner which allows charge extraction with either true floating gate (TGF) or reset floating diffusion (RFD) signal amplification.

A drawing of the output section of an individual array is shown in Figure 23. In a manner similar to the 20-element imager on the SBRC 8585 chip, the output structure of the SBRC 8587 array incorporates a floating gate (FG) and a junction (OD) at the end of the register for purposes of charge extraction. A major difference is that the 20 x 16 array also includes an on-chip MOSFET structure (not shown in Figure 23) for direct signal amplification and a gate (V_{BIAS}) overlapping FG which is used to establish a potential on the floating gate.

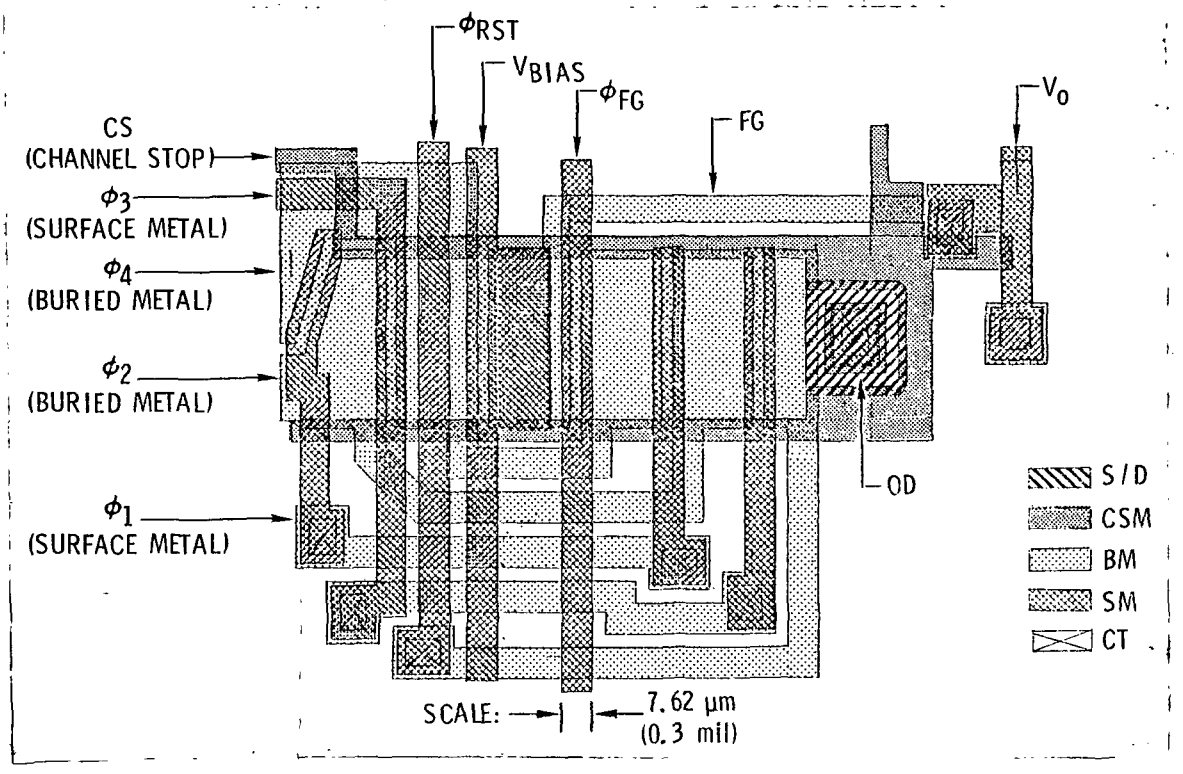


Figure 23. Output Circuit of 20 x 16 TDI Area Array Next-Generation Monolithic Intrinsic Chip

Optional masks in the SBRC 8587 set are used to select which output circuit will be produced. In the baseline TFG structure, the floating gate will connect directly to the gate of the on-chip MOSFET, without intervening bonding pads or long lead routings which would increase the output node capacitance. The OD junctions in the baseline output serve as sinks for the charge packets after they have been sensed by the FG. In the alternate output scheme, which may be selected as an option, the FG connection to the MOSFET is broken and both FG and OD are connected to bonding pads. This enables either OD to be used in a RFD circuit with off-chip transistors (as done currently with the SBRC 8585 chip), or FG to be used for charge detection with an off-chip TFG circuit. The use of optional masks of this type will allow the SBRC 8587 design to be used for both InSb and HgCdTe CCD arrays. In the case of HgCdTe, this allows use of the design for both n-channel devices for which the operational characteristics of junctions and MOSFETs have been reported[16] and p-channel devices in which junctions have not yet been realized.

The true floating gate output amplifier was chosen for direct incorporation as the on-chip device from among three alternatives, as shown in Figure 24. The TFG circuit (Figure 24(a)) was chosen for use on the 20 x 16 TDI array because of its high tolerance to large threshold voltages and low diode breakdown voltages. Consider the other two alternatives for on-chip output amplifiers as shown in Figures 24(b) and (c). Each must be able to have breakdown voltages for the diffusion to substrate of at least the threshold voltage plus output voltage swing. The true floating gate output does not have this constraint. Its breakdown voltage need be only the signal swing as no diffusion is connected to the MOSFET gate.

100-ELEMENT LINEAR IMAGING ARRAY

The second major array on the SBRC 8587 chip is a 100-element linear imaging array. As can be seen in Figure 18, the array design incorporates two separate 50-bit CCD multiplexers with a continuous row of 100 detector photogates. The overall 100-element array covers an area 508 μm (20 mils)

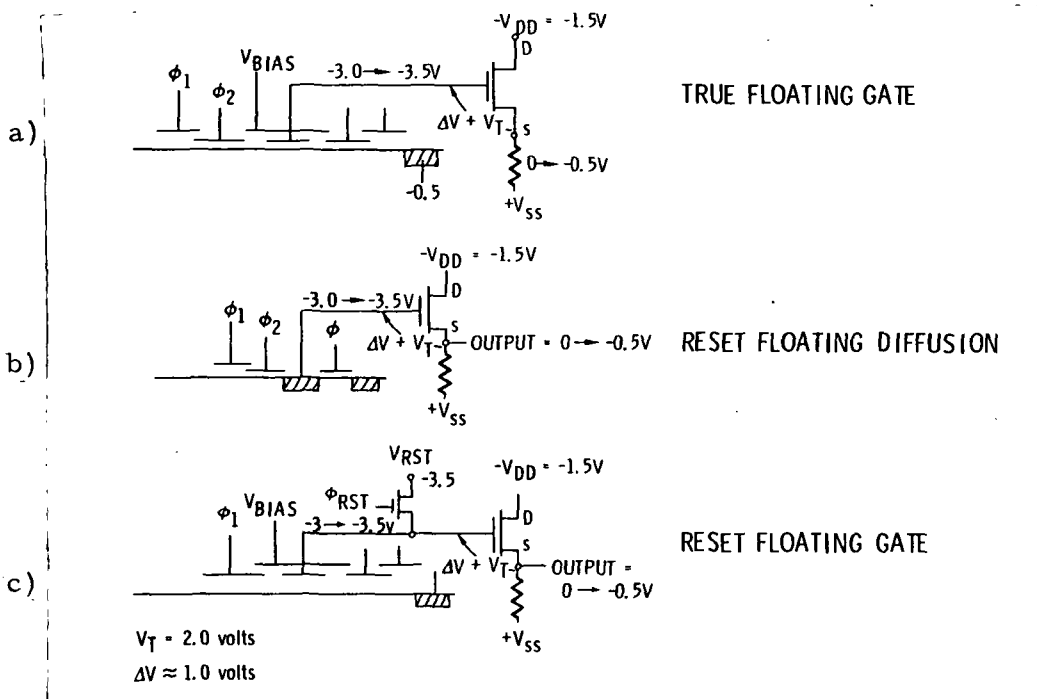


Figure 24. Output Circuit Options.

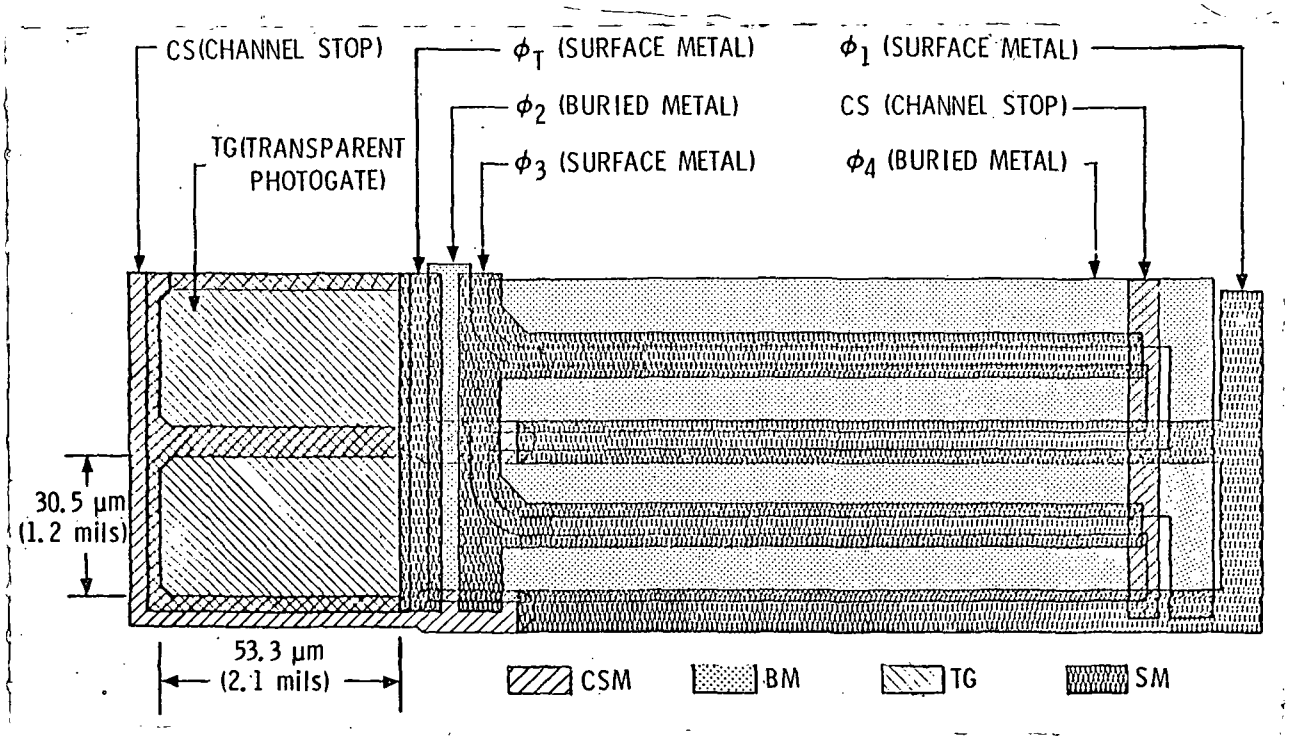


Figure 25. Unit Cell of 100-Element Linear Imager Next-Generation Monolithic Intrinsic Chip

wide by 4242 μm (167 mils) long and has an active area 254 μm (10 mils) wide by 3861 μm (152 mils) long. A layout of the 100-element array unit cell is shown in Figure 25. The unit cell covers an area 38.1 μm (1.5 mils) wide by 246.4 μm (9.7 mils) long with a transparent photogate detector element which is 30.5 μm (1.2 mils) wide by 53.3 μm (2.1 mils) long. As in the 20 x 16 TDI array, the minimum dimension for line widths and spaces is 5.0 μm (0.2 mils).

The 100-element imager has a single transparent photogate detector inputting into a single bit of a conventional type (rather than zig-zag) 4ϕ CCD structure which, however, is of novel design. This design uses a transfer gate (ϕ_T) which transfers the charge into an "L" shaped buried gate (ϕ_2). The use of the "L" shaped gate structure enables the CCD to be laid out without the usual requirement of running clock lines outside the basic CCD active area. This method greatly reduces the non-active area required for a linear CCD and also eliminates the one or two contact windows per bit which are normally required.

The CCD will operate in a "pseudo-two-phase" manner in that the device uses 12.5 μm (0.5 mil) wide buried gates (ϕ_2 and ϕ_4) for charge storage and 5.0 μm (0.2 mil) wide surface metal gates (ϕ_1 and ϕ_3) for transferring the charge from ϕ_2 to ϕ_4. The device uses a three-gate pulsed diffusion fill-and-spill input circuit for fat zero input and CCD testing as does the 20 x 16 TDI array.

Unlike the 20 x 16 TDI array, the 100-element array uses a reset floating diffusion, similar to that shown in Figure 24 (b), as its baseline output circuit. It also has optional masks for interconnection of the output diffusions (OD) to either an on-chip source-follower MOSFET amplifier or wirebond pad for off-chip output signal amplification.

PLANAR n^+ -n CHANNEL STOP TEST ARRAY

A third device on the SBRC 8587 chip is a CCD test array for determining the effects of utilizing planar channel stops (PCS). This device

consists of two eight-bit, 4ϕ shift registers which operate in parallel using common CCD gates. (See Figures 17 and 18.)

One CCD channel is bordered with an ion-implanted n^+-n channel stop, while the other has a conventional field plate of channel stop metal as has been used on all other monolithic intrinsic CCD structures to date.

The PCS test array uses the same input structure as those described earlier. It also uses optional mask interconnections to on-chip TFG output MOSFETs or bond pads for output to off-chip amplifiers. The CCD operates similar to the 100-element linear array and uses 21.59 μm (0.85 mil) wide storage gates and 8.89 μm (0.35 mil) wide transfer gates.

SBRC 8587 TEST DETECTOR STRUCTURE

As discussed in Section 6, it is difficult to obtain an actual quantum efficiency measurement value for CCD's using the transparent photogate detector configuration. This had been attempted through the use of test structures fabricated on germanium and computer iteration of the transmission and reflectance results, but the resultant data is only approximate. Therefore, a test device was incorporated in the SBRC 8587 chip design which will allow actual quantum efficiency measurements to be made.

A drawing of the test detector is shown in Figure 26. It incorporates three detectors for performing the quantum efficiency measurement. The first detector utilizes a single bit CCD connected to a transparent photogate detector which has the identical structure used in the 20 x 16 TDI and 100-element arrays. The second detector has an ion implanted region under a transparent photogate forming a PV diode from which signal to noise (S/N) response can be measured. The third detector is formed by a PV detector without the transparent photogate. Thus, the S/N of one can be balanced against the other two. This will allow determination of how much signal is lost from absorption in the photogate, and how much is lost from the depletion well. The area covered by each detector is 31.75 μm (1.25 mils) wide by 66.25 μm (2.6 mils) long giving an active detector area of $2.1 \times 10^{-5} cm^2$.

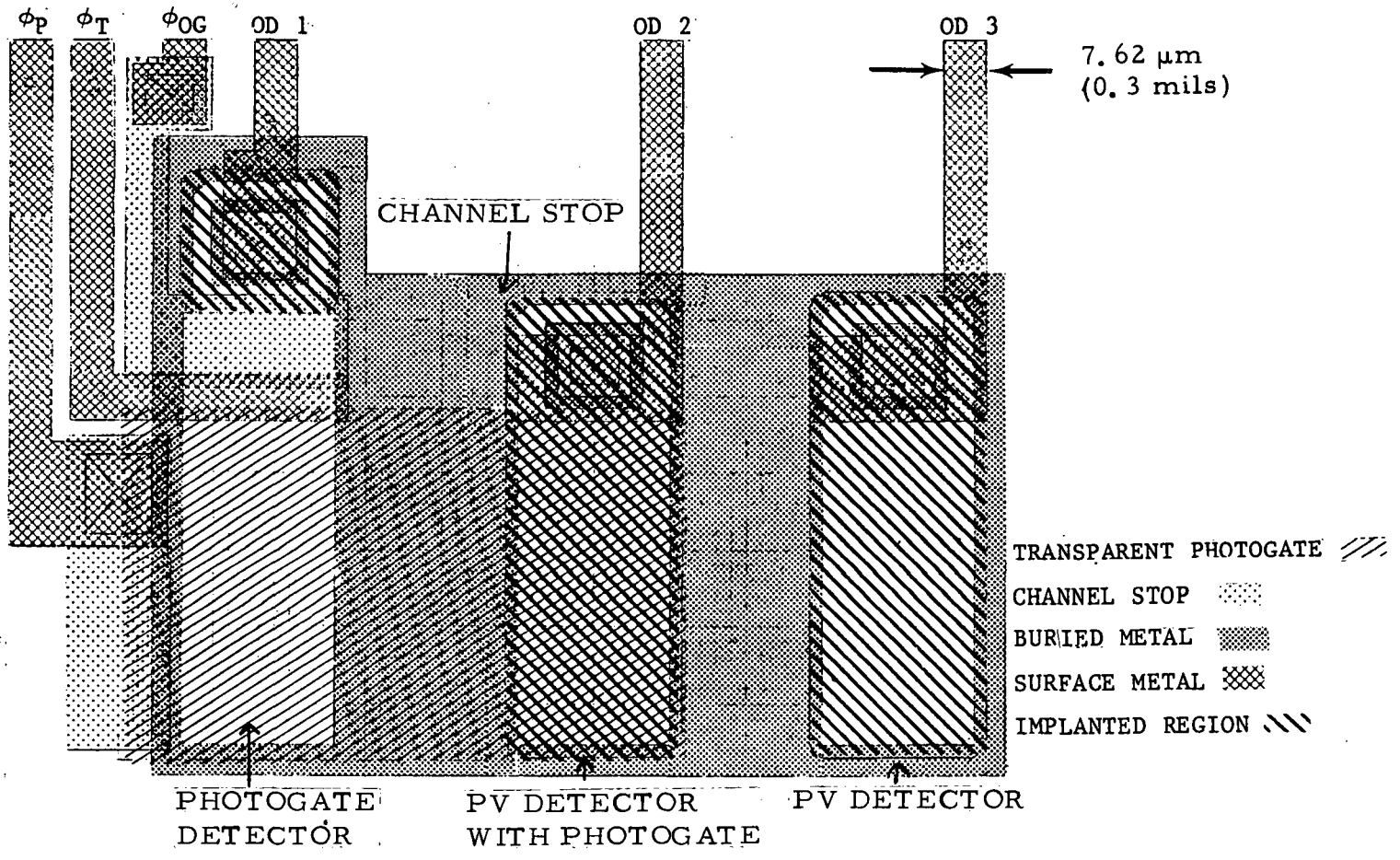


Figure 26. SBRC 8587 Photodetector Test Array

SBRC 8587 MOSFETS

Figure 27 shows a layout of the MOSFET structure used for on-chip signal output amplification on all arrays of the SBRC 8587 chip. The MOSFET has a circular channel region to reduce high field effects, which can occur at square corners of junctions, for example. The source is gated with a channel stop on the outside edge to eliminate substrate effects from outside the channel region. The channel width-to-length aspect ratio (Z/L) is 11.22 for all devices on the chip, with an overlapping gate on the buried metal level. Interconnection from the source and drain to bond pads is formed with conductors on the surface metal level. For devices which use the optional mask to connect the CCD output to bond pads for off chip signal amplification, a surface metal field plate will cover the MOSFETs to eliminate illumination noise feedback into the CCD channel.

The PCS test MOSFET shown in Figures 17 and 18 has a rectangular bar structure with matching source and drain implant regions. It also has an overlapping buried metal gate with an overlapping channel stop field plate around the outside edges. The Z/L ratio for this device is 4.17.

In order to determine if the ion-implanted n^+-n channel stop is functioning properly, two separate structures would be fabricated. One device would have a 5.0 μm (0.2 mil) wide n^+-n ion-implanted channel stop bar running the entire 127.0 μm (5.0 mils) width of the MOSFET channel. The second device would be fabricated without an implanted channel stop. If, when tested, the MOSFET with a planar channel stop does not operate while the device without a planar channel stop does operate, the channel will have been successfully pinched off and the planar channel stop has functioned properly.

SBRC 8587 IN-PROCESS TEST DEVICES

The remaining devices on the chip consist of four guarded capacitors for in-process and post-process C-V characterization of the individual gate levels, and rectangular resistor bars for probe testing to determine etch completion of contacts to underlying metal layers.

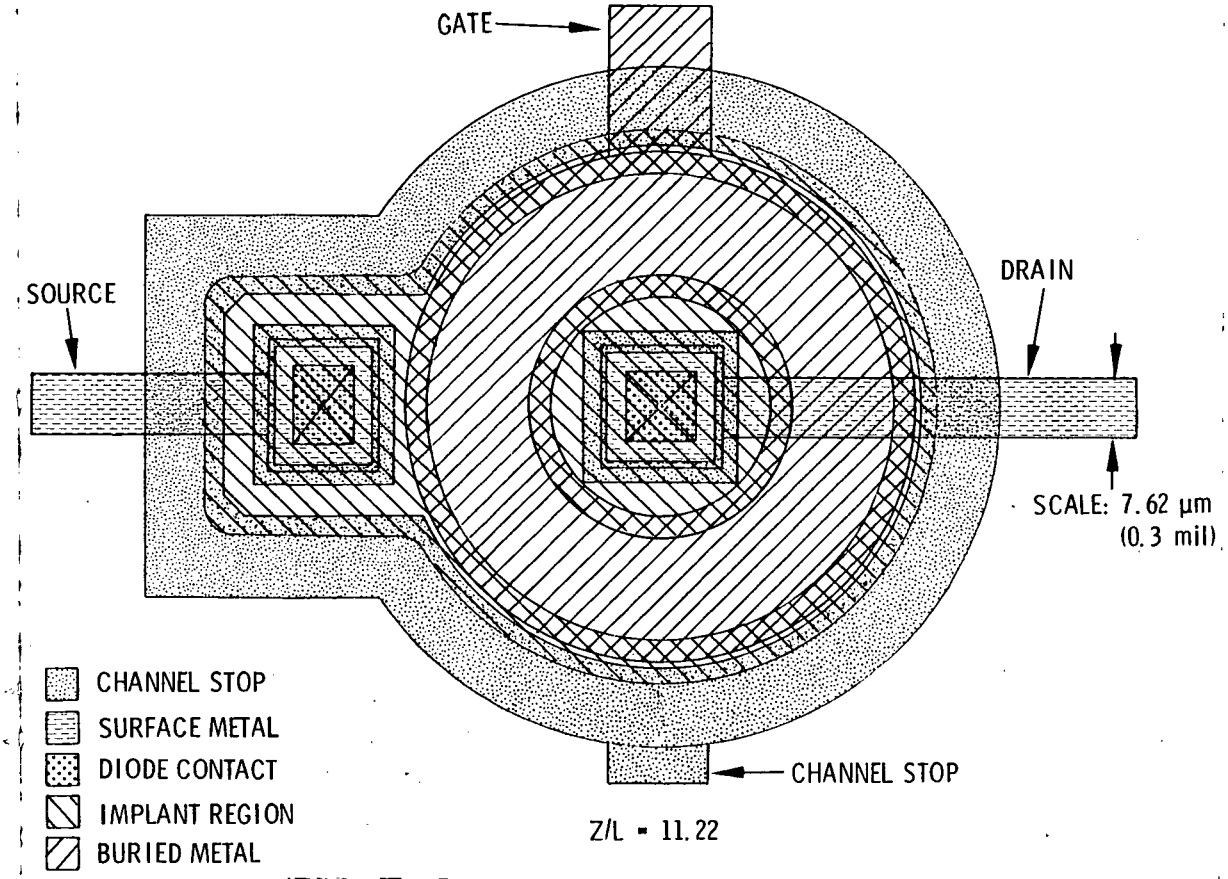


Figure 27. SBRC 8587 Output MOSFET Structure

Originally, it was planned to include all of the test devices including the photodetector test array and test MOSFETs on one chip and use a drop-in technique to only repeat the chip four to six times across a wafer. This would have allowed a greater number of die/wafer of the lower yield imaging arrays. Because of the large number of masks needed to fabricate the arrays (twelve) this proved to be not economically feasible.

SBRC 8587 MASK SET

Following completion of the design and layout of the basic units of the SBRC 8587 chip at Hughes Industrial Products Division in Carlsbad, CA., the design prints were sent to Microfab in Palo Alto, CA. for digitizing, final plotting, pattern generation, and mask fabrication. A list is shown in Table 2 which describes the identification and type of all masks procured. As noted earlier, the mask set was designed for processing both InSb and HgCdTe monolithic arrays. Therefore, there are a few masks levels (all metal gate patterns) for which both clearfield and darkfield masks were procured. This will allow for both direct metal etching or reverse photolithographic processing as required for fabricating CCDs on the two different materials.

SBRC 8587 PROCESS DEVELOPMENT

The fundamental goal during the design phase of the SBRC 8587 chip was to utilize the experience gained from fabricating SBRC 8585 devices and develop improved processing techniques for fabricating SBRC 8587 arrays. With this in mind, the preliminary SBRC 8587 design effort concentrated on methods for simplifying the processing sequence, increasing the overall yield, and improving the operational characteristics. Descriptions of the process sequence developed from this effort are listed in Table 3. Flow charts of the respective processes and their corresponding cross-sectional views are shown in Figure 28.

SBRC 8587 PROCESS IMPROVEMENTS

As noted in Table 3, several of the processes are improvements over the SBRC 8585 process scheme.

Table 2. SBRC 8587 Mask List

Mask #	I.D.	Description	Clearfield	Darkfield
8587-1	AK	Alignment Key	--	X
-2	PCS	Planar Channel Stop	--	X
-3	SD	Source/Drain	--	X
-4	DC1	First Diode Contact	--	X
-5A	CS	Channel Stop (with charge splitting)	X	--
-5A	CS	Channel Stop (with charge splitting)	--	X
-5B	CS	Channel Stop-Option 1 (without charge splitting)	X	--
-5B	CS	Channel Stop-Option 1 (without charge splitting)	--	X
-6	BM	Buried Metal	X	--
-6	BM	Buried Metal	--	X
-7	TG	Transparent Photogate	--	X
-8	BC	Buried Contacts	--	X
-9	DC2	Second Diode Contact	--	X
-10A	SM	Surface Metal (with MOSFET outputs)	X	--
-10A	SM	Surface Metal (with MOSFET outputs)	--	X
-10B	SM	Surface Metal-Option 1 (without MOSFET outputs)	X	--
-10B	SM	Surface Metal-Option 1 (without MOSFET outputs)	--	X
-11	PC	Pad Contacts	--	X
-12	PM	Pad Metal	X	--

Table 3. SBRC 8587 CCD Process Description

Operation	Process Title	Layer/Mask Designation	Process Description
0XX	Initial wafer preparation	---	Initial wafer clean-up (Removal of shipping material)
1XX	Alignment Key	AK	Deep polish etch etch AK pattern
**2XX	Implant n^+ planar channel stops	PCS	Apply PCS pattern ion implant $n^+(S^+)$ lift-off pattern
**3XX	Anneal PCS implant	---	Prepare surface anneal n^+ implant
4XX	Implant p^+ source/drain	SD	Apply SD implant pattern ion implant $p^+(Be^+)$ lift-off pattern
5XX	Anneal SD implant	---	Prepare surface anneal p^+ implant
6XX	Gate insulator	GI	Prepare surface: deposit SiO_2 (1500Å) Anneal
*7XX	Diode contacts (initial)	DC1	Deposit Al (500Å) etch Al DC1 pattern etch SiO_2 DC1 pattern
8XX	Channel Stop metal	CS	Etch CS pattern
*9XX	Channel stop insulator	---	Deposit SiO_2 (1000Å) - no etch - deposit Al (1000Å)

Table 3. SBRC 8587 CCD Process Description (continued)

Operation	Process Title	Layer/Mask Designation	Process Description
10XX	Buried metal	BM	Etch BM pattern
*11XX	Transparent gate	TG	Apply TG pattern deposit lift-off pattern
*12XX	Buried contacts	BC	Deposit SiO_2 (2000Å) etch BC pattern
*13XX	Diode contacts (final)	DC2	Etch DC2 pattern Pd plate
14XX	Surface metal	SM	Deposit Al (3000Å)(1000Å - option) etch SM pattern
**15XX	Surface contacts	SC	Deposit SiO_2 (2000Å) etch SC pattern
**16XX	Pad metal	PM	Deposit Al (3000Å) etch PM pattern
17XX	Final evaluation	---	DC short tests C-V tests CCIRID tests

* Denotes process improvement.
** Denotes optional processes.

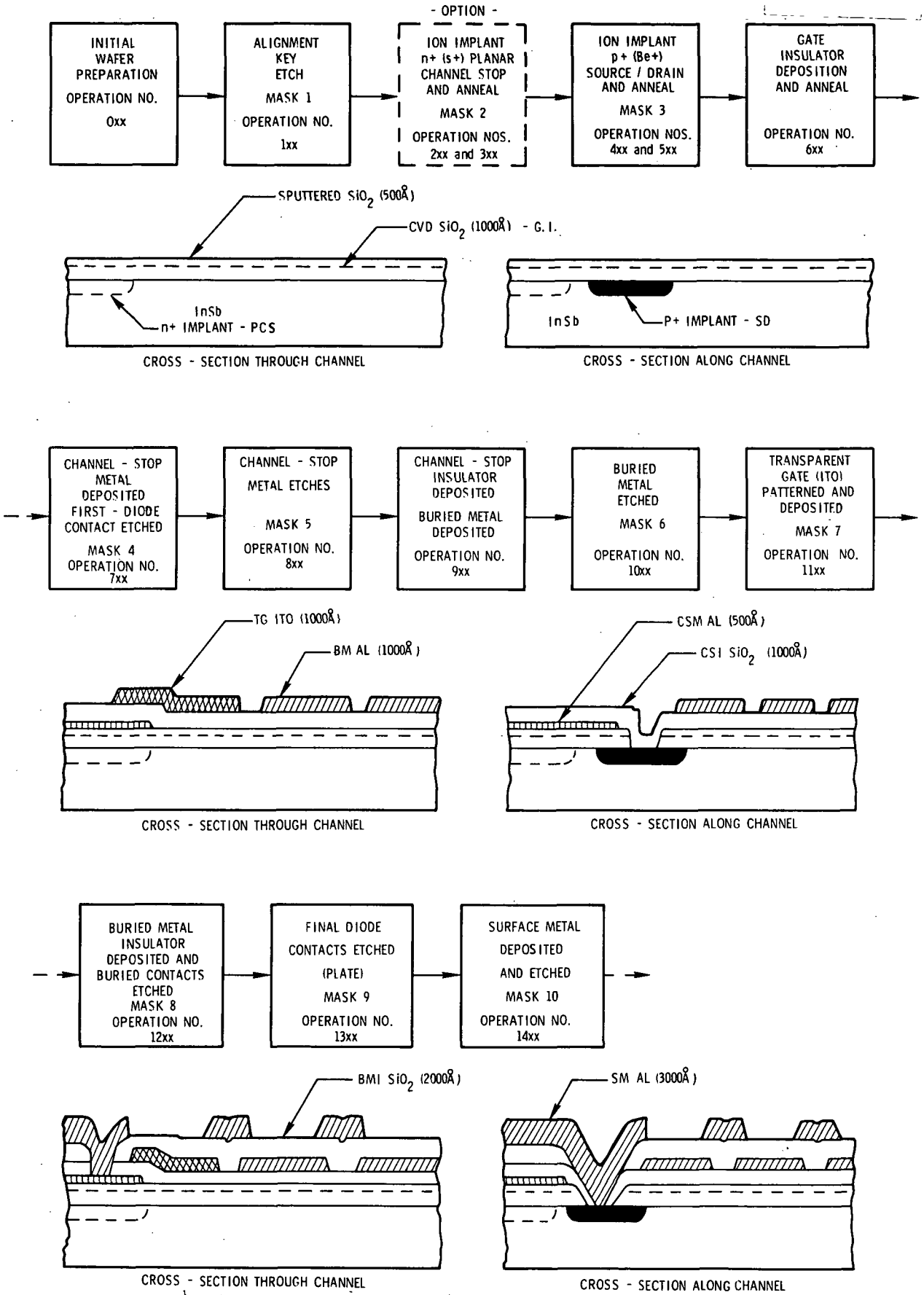


Figure 28. Block Diagram and Cross-Section Views of SBRC 8587 CCD Chip Fabrication Sequence.

The first consideration involves the need to minimize positive ions available for migration and entrapment in the basic gate insulator. Photoresist chemicals are known to contain a small percentage of free sodium ions. Therefore, elimination of photoresist processing on the gate insulator will reduce the quantity of positive ions available.

The SBRC 8585 process sequence requires four photoresist operations to be performed on the gate and/or channel stop insulator, prior to depositing and delineating the buried metal gate pattern. Each of these subjects the insulator to possible mobile ion contamination. Therefore, the SBRC 8587 process sequence has been changed, as follows, to eliminate or delay these operations:

1. The initial diode etch sequence is performed prior to etch delineation of the channel stop (Operation 7XX).
2. Similar to the SBRC 8585 process, etch-back of the channel stop insulator has been eliminated (Operation 9XX).
3. Etching contact windows to the channel stop metal is deferred until operation 12XX, when all buried contacts will be etched simultaneously.
4. Final diode contact formation is deferred until Operation 13XX.

The remaining process improvement involves forming contacts to the transparent photogate. An item of concern when processing SBRC 8585 arrays is that each individual transparent photogate must have a contact window etched prior to interconnection with the surface metal layer. Although this process has been addressed and improved (refer to Section 6), in the past this operation has created numerous shorts to the substrate from pinholes forming in the underlying oxides. In addition, the transparent photogate material must have a high transmission to yield optimum quantum efficiency. Coatings such as these may not be capable of withstanding any type of etching. Therefore, the SBRC 8587 design eliminates the need for etching contacts by depositing a solid strip of photogate material and forming a single direct contact to a buried metal conductor.

OPTIONAL PROCESSES

As indicated in Table 3, operations 2XX, 3XX, 15XX, and 16XX are considered optional for the SBRC 8587 mask design. Operations 2XX and 3XX are specifically for performing n^+-n ion implantation and annealing of the planar channel stop. Planar channel stops are not yet being applied to the area array or linear imager of the SBRC 8587 mask set. As noted in the discussion of the Planar n^+-n Channel Stop Test Array, there will be a small pair of CCDs on the chip for evaluating the effect of planar channel stops on charge transfer. If the test array proves that planar channel stops are feasible, the mask set can be modified to accommodate this technique on the area array and linear imager at a later date. Therefore, it is not considered as an essential operation in fabricating the present SBRC 8587 mask set.

Operations 15XX and 16XX are specifically for applying a surface passivation or antireflection coating to the CCD structure. They are not required for device operation and will not be utilized during the early period of device development.

Section 5
PLANAR CHANNEL STOP DEVELOPMENT

The channel stop is a basic component of any CCD array necessary to provide lateral confinement of signal charge within the CCD channels, delineate detectors from one another, etc. There are three advantages of a planar approach: (1) the channel stop metal field plate presently used, and its corresponding insulator, are eliminated, simplifying the structure and increasing yield; (2) much tighter geometries, as will be required in future chip designs such as redesign of the SBRC 8587 20 x 16 TDI area array to incorporate backside-illuminated detectors for 100% fill factor staring purposes, are achieveable; and (3) the channel stop need not be laid out in a continuous, unbroken pattern. This latter limitation to the present channel stop metal approach was realized during preliminary layout of the 20 x 16 area array.

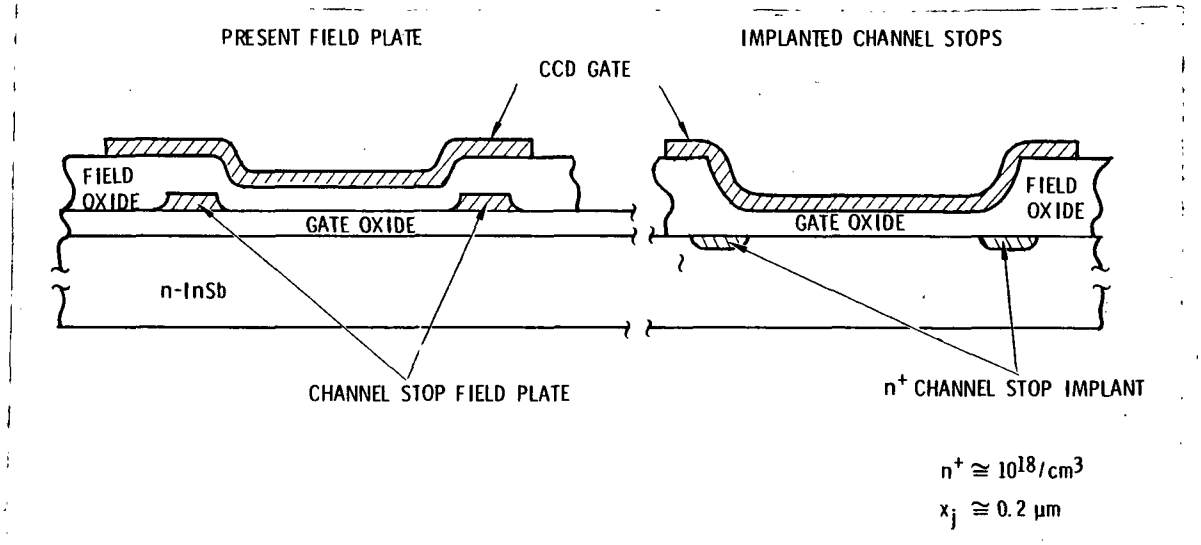


Figure 29. Planar Channel Stop Approach

If isolated channel stop segments are necessary in layout -- for example, to divide a single charge packet into two charge packets -- no difficulty is created with an implanted or diffused majority-carrier channel stop, as it need not be externally biased. With the channel stop metal approach, however, each isolated segment of channel stop would have to be contacted through a contact cut, and tied by bus bar to a bonding pad so that appropriate dc bias can be applied to each segment. The many contact cuts required would reduce yield and the busing requirement complicates the layout of area arrays, which are already sufficiently difficult. An illustration comparing cross-sectional views of the present channel stop metal versus a planar ion-implanted channel stop is shown in Figure 29.

P-channel InSb CCDs (n-type substrates) require an n^+-n channel stop. The n^+ region must be heavily doped (at least 10^{18} cm^{-3}) and must extend at least 0.1 to 0.2 μm below the surface. After implantation the wafers must be annealed to reduce implantation damage and to electrically activate the implanted species.

With this in mind, a program was initiated with IR&D funding in 1977 to determine the optimum dopant ion, implantation energy and dose, and anneal time and temperature. This work was carried out at SBRC with ion implantation being performed at NASA Langley Research Center. Through these efforts, a basic approach was achieved which utilized sulphur as the ion-implanted specie with an implanted profile well-approximated by a Gaussian distribution, with a peak at depth (R_p) and a width of Gaussian parameter (σ_p).

Sulphur was selected as the ion because it provides a greater range, at the same energy, than other n-type dopants and a larger projected width (σ_p). This combination allows the implant peak to be placed near the nominal depth of 0.1 μm while maintaining sufficient ion concentration near the surface. Sulfur also causes less damage per ion than the other dopants because of its lower mass.

Calculations led to selection of an ion energy of 140 keV, corresponding to $R_p = 0.119\ \mu m$ and $\sigma_p = 0.063\ \mu m$[17]. Doping at the surface (before etchback) is predicted as 17% of the peak value. Also $4\sigma_p > 0.2\ \mu m$, so that the implant spreads over the desired depth. Although the optimum dose (ϕ) has not yet been firmly established, a range from 1.6×10^{13} to $8 \times 10^{13}\ cm^{-2}$ was selected. A dose of $1.6 \times 10^{13}\ cm^{-2}$ gives a nominal peak sulfur density of $10^{18}\ cm^{-3}$.

Damage sites created by implantation in InSb act as donors. In unannealed samples, carrier concentration due to damage is more than ten times higher than the density of the implanted species, but damage doping itself is not necessarily harmful because it is of the same type as the impurity doping in our case. The damaged region, however, must contain a high density of generation-recombination centers, which produce minority carriers that can diffuse into the CCD channel. For this reason it is necessary to anneal out most of the damage.

Various anneals were conducted varying doping level vs time vs temperature for sulphur implants compared to argon (a nonactive specie) implants. For implanted doping levels of $\sim 10^{20}\ cm^{-3}$ for both implanted types, the doping was found to decrease with annealing time and temperature until leveling off at a doping level of $\sim 10^{16}\ cm^{-3}$. Since argon implants created only damage sites, it was concluded the annealed sulphur implants resulted in an electron concentration which is due to implantation damage with no electrically active sulphur species present.

Most damage anneals out below 360°C for this dose, although a second type of damage site exists at a concentration of about $10^{16}\ cm^{-3}$ which does not anneal out up to 380°C. Even though doping is due to damage, one can still produce the electron concentration necessary for a planar channel stop by implanting with sulfur at 140 keV with a dose of more than $10^{13}\ cm^{-2}$ and annealing near 350°C.

RESOLUTION OF S^+ IMPLANTS

To measure the resolution attainable with ion implantation in conjunction with current processing, and to measure lateral diffusion of the sulfur during annealing, a set of implant spreading experiments was performed using a test pattern with varying gaps between implanted regions. The implanted areas were defined by anodic staining to allow accurate measurement. Three cases were studied: unannealed, and annealed at 320°C and 350°C in N_2 for 0.5 hour. In each case the gap between implanted regions was found to be not significantly different from the photoresist width before implantation.

The conclusions were: (1) after implantation and annealing, the tolerance is 0.5 μm, which is sufficient for a planar channel stop; and (2) the lateral diffusion of sulfur is less than 0.5 μm in 0.5 hour at 350°C.

SBRC 8587 PLANAR CHANNEL STOP APPLICATIONS

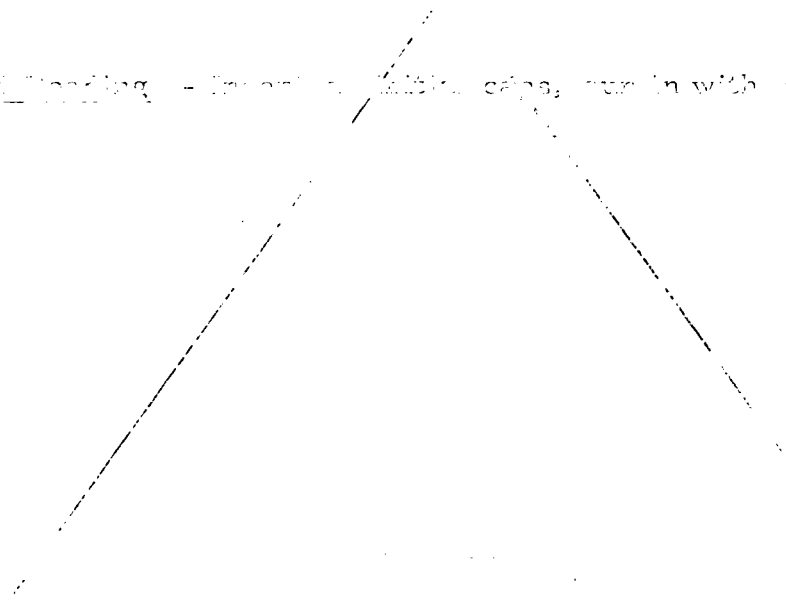
A planned study is to fabricate a test structure consisting of a capacitor with a ring-shaped channel stop implant around the perimeter of the capacitor. Such a structure allows measurement of minority carrier generation rate under the gate and comparison with the rate under a gate without an implant. This test structure is incorporated on the SBRC 8587 chip with the capacitor on the buried metal level. In addition and as noted in Section 4, two-eight-bit CCD shift registers are included on the SBRC 8587 chip for direct comparison between CCD outputs from a register with a field plate channel stop and a register with a planar channel stop.

Finally a process sequence has been developed for incorporation into SBRC 8587 chip fabrication as follows (see Figure 28 and Table 3):

1. An alignment key will be etched into the substrate for aligning patterns following ion implantation.
2. A 7 ± 2 μm positive photoresist pattern defining the planar channel stop implant regions will be applied, and the wafers implanted with S^+.

3. The photoresist will be stripped off, and the surface etched to remove any stray sulphur. Then the water will be annealed in N_2 at 350°C for 0.5 hour.

4. The wafer will then be prepared for normal Be^+ ion implantation and carried through the CCD process. It is necessary to anneal the sulphur implant prior to annealing the Be^+ as the higher temperature (350°C vs 320°C) would create a degraded Be^+ implanted specie.



Section 6

PROCESS TECHNOLOGY DEVELOPMENT

During the first portion of the contract, much of the effort was directed towards improving the process technology to obtain higher quantum efficiency and yields than had been realized in the past. Elimination of etching the CSI layer (discussed in Section 2) was one of the developments considered. Further studies, included developing a new transparent gate material and evaluating the feasibility of LTCVD versus sputtered SiO_2 upper layer insulators.

TRANSPARENT GATE DEVELOPMENT

InSb CCIRID devices fabricated, characterized, and delivered on the previous contract utilized a thin (0.0075 μm) titanium (Ti) film as the conductive transparent gate material. Detectivity measurements performed on fully operational devices indicated that the quantum efficiency realized from that structure was not optimum. Optical measurements were then performed with the photogate structure coatings deposited on germanium substrates. Calculations of the measurements determined that the maximum transmission achieved with the structure did not exceed 50%. A development effort was subsequently carried out using internal IR&D funds to develop an electrically conductive transparent gate material which would yield an improvement in transmission. This development effort resulted in development of a transparent gate coating utilizing an indium tin oxide (ITO) type of material.

Actual measurements of the transmission, absorption, and reflectance of these mutlilayered structures are not possible, since the values needed are the ones entering the absorbing InSb layer. Therefore, computer modeling was performed on this contract in an attempt to gain insight into the optical qualities of the Ti and ITO structures.

The graphs shown in Figures 30 and 31 were derived from the above computer models. One set of curves is from iterating the refractive index (n) and the absorption coefficient (k) (where the complex index is written $\hat{n} = n + ik$) against actual transmission measurements obtained from similar structures fabricated on germanium windows (k = 0).

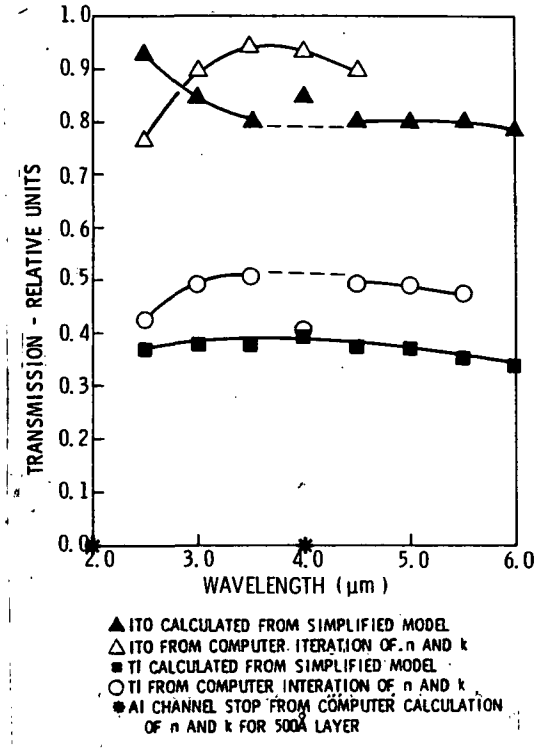


Figure 30. Calculated Transmission Versus Wavelength for Transparent Photogate Structures Using Titanium (75 Å) and ITO (1000 Å) Plus Al Channel Stop.

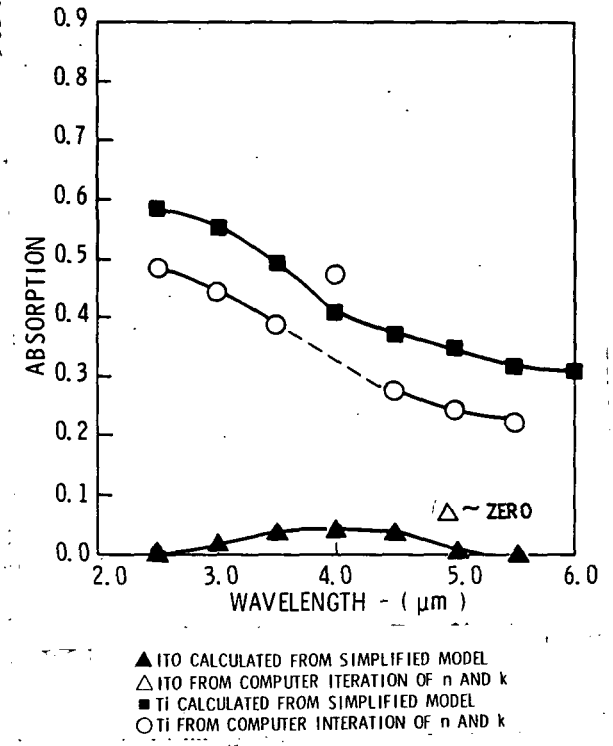


Figure 31. Calculated Absorption Versus Wavelength For Transparent-Photogate Structures Using Ti (75Å) and ITO (1000 Å)

A second set of curves was derived from a simplified model of the structure shown in Figure 32. This structure disregards multiple reflections occuring inside the structure and assumed that ~100% of all absorption occurs upon initial entry. To calculate the transmission intensity (I_T) of the structure the equation is

$$I_{TOTAL} \sim I_{T1} + I_{T2} + \cdots\cdots I_{Tn} \qquad (6\text{-}1)$$

where

$$I_{T1} \sim I_{TS} - I_{TS}R_B \qquad (6\text{-}2)$$

and

$$I_{T2} \sim I_{TS}\, R_B\, R_S\, (1 - R_B) \qquad (6\text{-}3)$$

Assuming reflections beyond the second order are negligable (i.e. $I_{T3} + \cdots I_{Tn} \sim 0$) the equation for total transmission is

$$I_{TOTAL} \sim I_{TS}\, (1 - R_B + R_B R_S - R_B{}^2 R_S) \qquad (6\text{-}4)$$

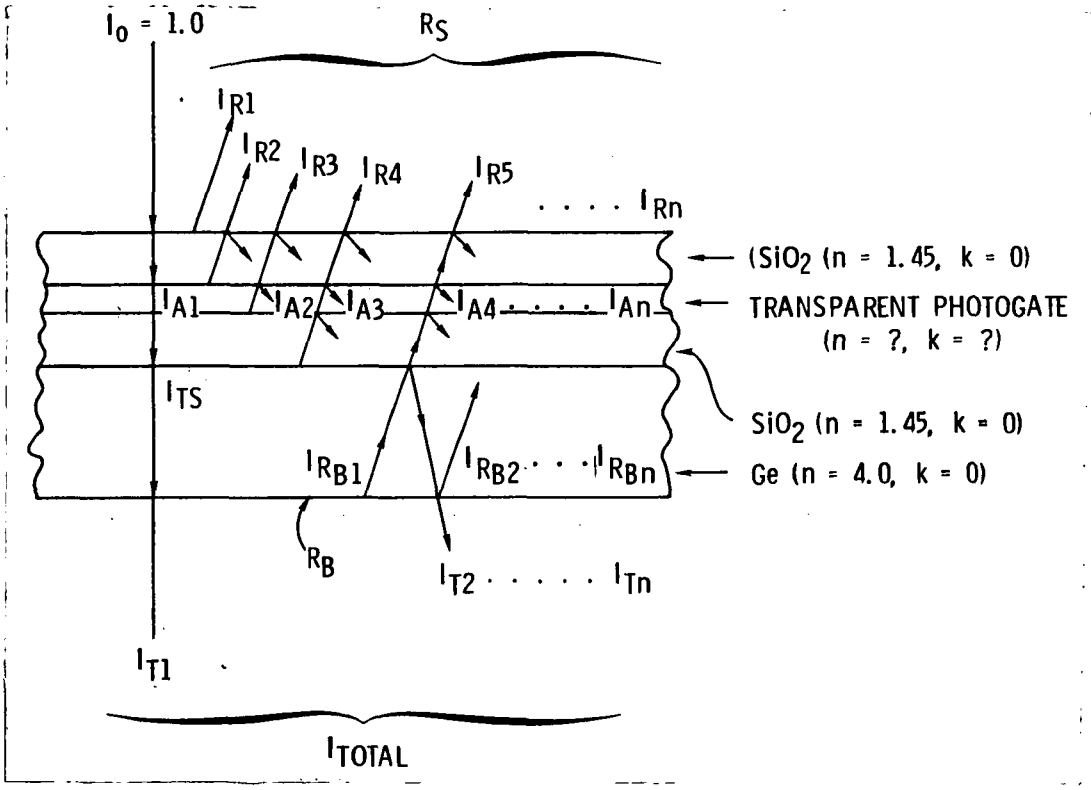


Figure 32. Simplified Optical Model of Transparent Photogate Structure

Converting equation (6-4) to find I_{TS}, we obtain

$$I_{TS} \sim I_{TOTAL} / (1 - R_B + R_B R_S - R_B^2 R_S) \qquad (6\text{-}5)$$

which is the transmission into the substrate. Using I_{TS}, I_o, and the intensity reflected from the surface (R_S), the absorption of the photogate is calculated as

$$I_{A1} \sim I_o - I_o R_S - I_{TS} \qquad (6\text{-}6)$$

The values calculated from equations 6-5 and 6-6 were obtained from actual transmission and reflectance measurements of I_{TOTAL} and R_S respectively and the results are shown in Figures 30 and 31.

As shown, there are some discrepancies in both sets of curves such as an anomalous absorption peak at ~ 4.0 μm in the computer modeled Ti curve, and a rise in transmission for the ITO simplified model. Still, they indicate that a definite improvement should result from use of the ITO coating.

A graph of actual values obtained for the reflection from the ITO and Ti structures is shown in Figure 33. This graph indicates that the major contributor to losses in the structure is from reflection. It is possible that an optimized anti-reflection coating over the structure could reduce this reflectance and again increase the optical transmission. Further development is required to perform computer modeling of the layered structure and improve the existing coating anti-reflection qualities or develop a new coating for this purpose.

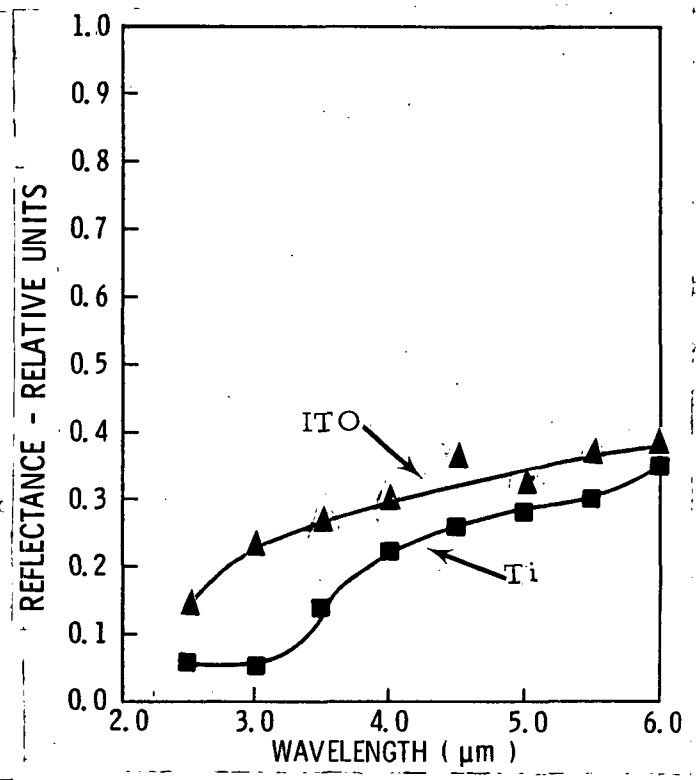


Figure 33. Measured Reflectance of Transparent Photogate Structures Using Ti (75 Å) and ITO (1000 Å)

Although the ITO transparent gate coating offers a substantial improvement in optical quality, it is not inert to the etchants used for SiO_2 and Al coatings. As stated in Section 4, the SBRC 8587 design will incorporate the bias conductor on the same level as the transparent gate. Thus no etching will be performed on that coating. It was necessary to develop a technique to protect the ITO coating during etching of the SBRC 8585 design.

Elimination of an Al etch problem was accomplished by switching sequences. The BM Al is deposited and etched. The TG photoresist pattern is then delineated, the ITO coating deposited, and the pattern lifted off. Previously, the TG pattern was delineated, Ti deposited and the pattern lifted off prior to depositing and etching the buried metal (BM) Al.

In order to protect the ITO coating from being attacked by plasma etching, when the BMI SiO_2 contact windows are etched, a BMI photoresist pattern is delineated directly on the ITO coating. Then a 500 Å layer of Al is deposited and the pattern lifted off. This process forms a small Al pad as a base contact for each contact window. Thus, when the BMI SiO_2 has been deposited, and the contact windows etched, the Al pad acts as an etch-stop and the ITO coating is not etched. This structure was temporarily incorporated into lot processing. Cross-sectional views of the structure are shown in Figure 2. A view of an actual array is shown in Figure 34. This array structure consists of an ITO transparent gate (A), the base contact Al coating (B), and etched contact windows in the BMI layer (C). Although the coating was used, no actual quantum efficiency data was obtained, since no devices were obtained for CCD testing.

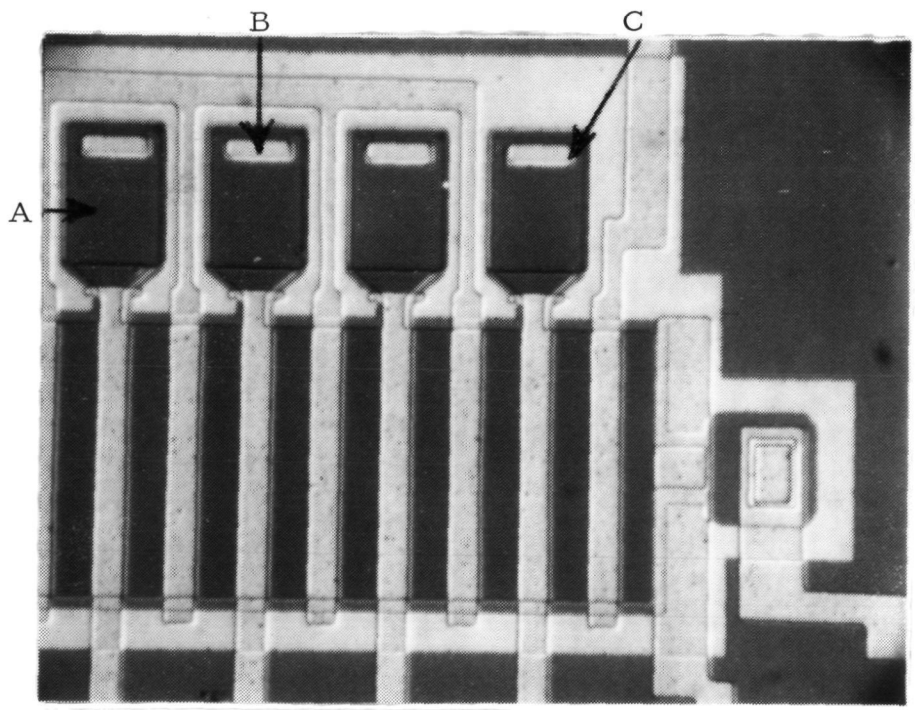


Figure 34. Fabricated Transparent Gate and Base Contacts.

In addition, some problems with poor adherence and lifting of the ITO coating were experienced during the final layer Al and SiO_2 process steps. These were attributed to seepage of chemicals around the Al stop etch pad. Therefore, use of the coating was halted until a new mask for delineating a larger stop etch pad could be designed and procured, and the problems with microarcing could be relieved.

LT CVD VERSUS SPUTTERED SiO_2 UPPER LEVEL INSULATORS

The major contributor to poor yields on the previous contract[4] was delamination of the upper layer structures at the LT CVD SiO_2 InSb interface. This delamination usually occured at the photoresist development stage in delineating upper level Al layers. Various studies were conducted on complimentary programs to investigate this phenomenon. To date no direct cause has been found, although a mismatch in the thermal coefficient of expansion for InSb and SiO_2 is considered the prime candidate. SiO_2 which has been directly sputtered on InSb will delaminate immediately. Since CCD delamination does not occur until several layers are built up, the LT CVD SiO_2 layer is considered to be more closely matched to InSb than sputtered SiO_2.

To test the above theory, an experimental lot (8585-15) was processed which utilized LT CVD SiO_2 for all insulating layers. The lot was completed and achieved both encouraging and discouraging results.

The encouraging result was that no delamination occurred at any time. Discouragingly, preliminary C-V tests at the BM level indicate the flatband voltage had degraded to -17.5 volts (Figure 35). The test data also indicates the surface state density is greater than 10^{12} cm^{-2} eV^{-1}.

The poor quality of the surface of Lot 15 is believed to be caused by diffusion of water through the porous LT CVD SiO_2 layers to the SiO_2/InSb interface. Therefore, a second full structure LT CVD SiO_2 was initiated which had the normal sputtered SiO_2 sealing layer deposited over the initial 1000 Å LT CVD SiO_2 gate insulator.

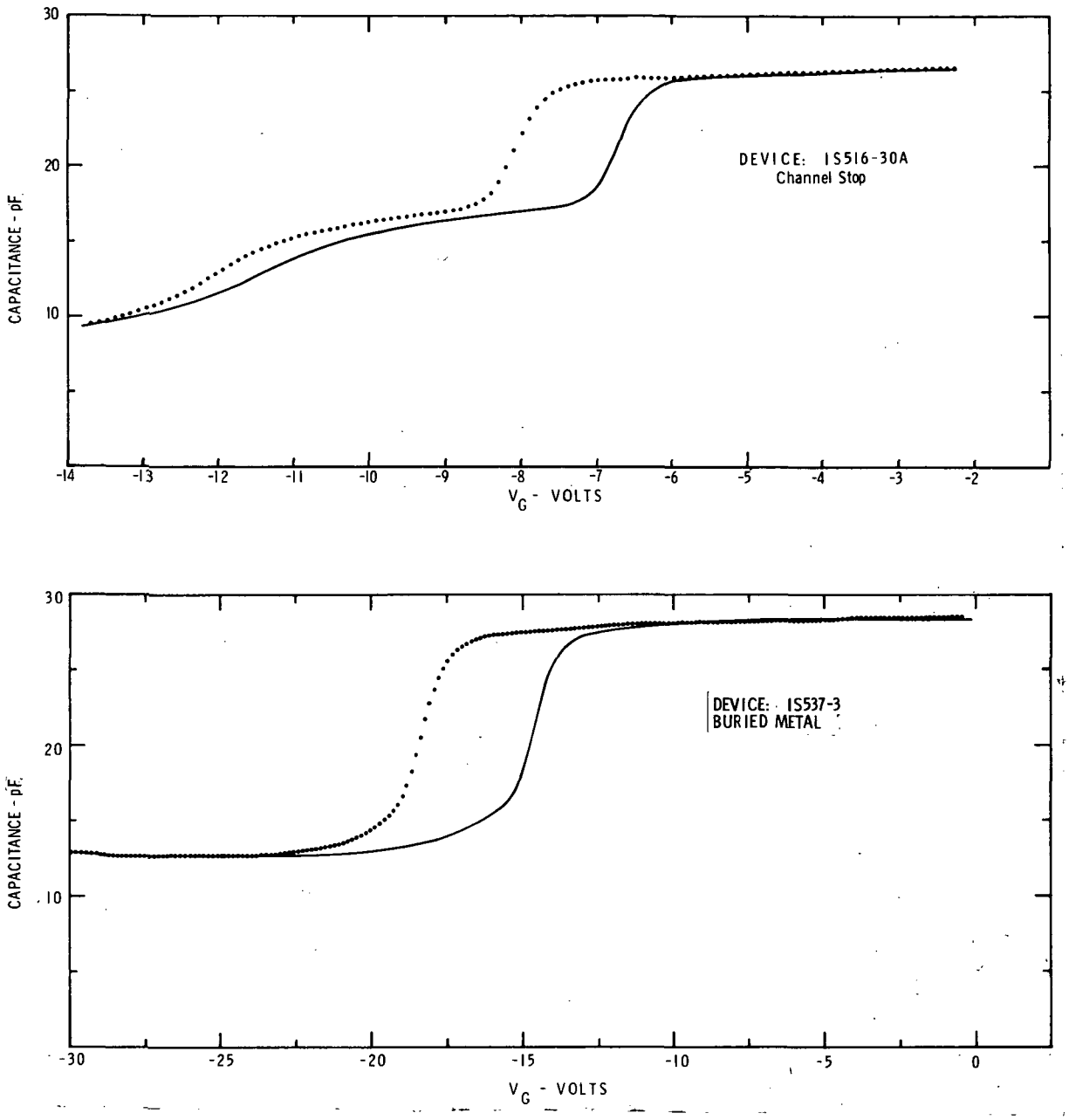


Figure 35. C-V Characteristics for Lot 8585-15 LT CVD SiO_2 Insulator Structure at Channel Stop and Buried Metal Levels. All Layers - AMS-1000.

Preliminary tests at the BM level for this lot (8585-10) showed flatband voltages near -4 volts with ~0.5-volt hysteresis (Figure 36). These C-V tests indicated the N_{SS} was still near mid $10^{11} cm^{-2}\text{-}eV^{-1}$.

Encouragingly, neither of these lots exhibited any of the delamination problems experienced previously. Visual inspection resulted in over 80% of the individual 20-element arrays being categorized as acceptable for dc short-testing. However, in probe testing, all of the arrays exhibited gate-to-substrate and/or gate-to-gate shorts, yielding no arrays of acceptable electrical quality for CCD testing.

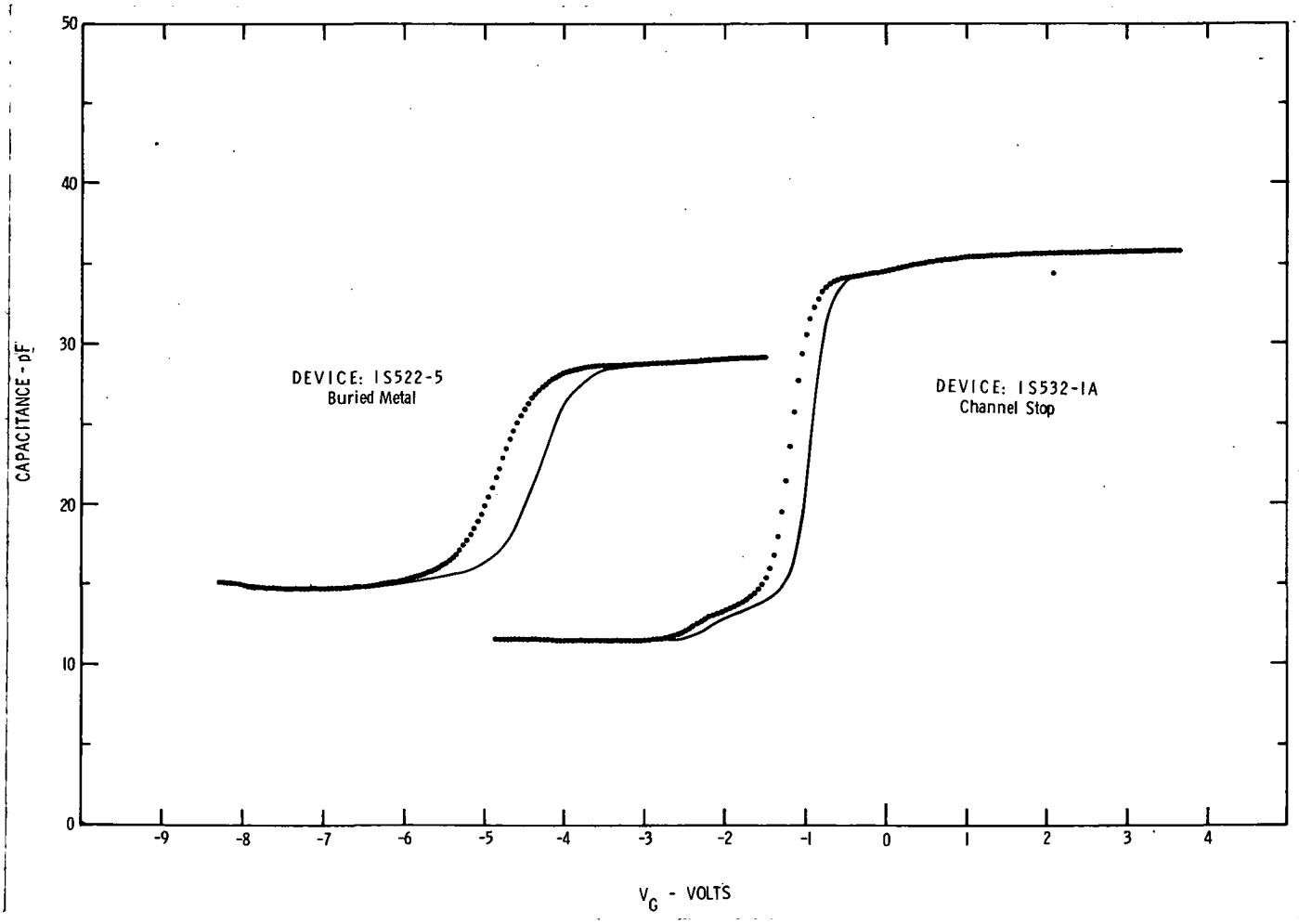


Figure 36. C-V Characteristics for Lot 8585-10 LT CVD SiO_2 Insulator Structure at Channel Stop and Buried Metal Levels.
Gate Insulator - AMS-2600
Upper Levels - AMS-1000

SEM examination of the wafers showed that the LT CVD oxide, which shows evidence of a 1500 Å diameter granularity when used as the gate insulator, displayed an increased granularity to ~ 4000 Å diameter in the thicker upper layers (Figure 37). This increased granularity and associated pinholes were believed to be the cause of the shorting in this group of wafers. It is also possible that microarcing had also occurred, but that problem had not been identified at the time.

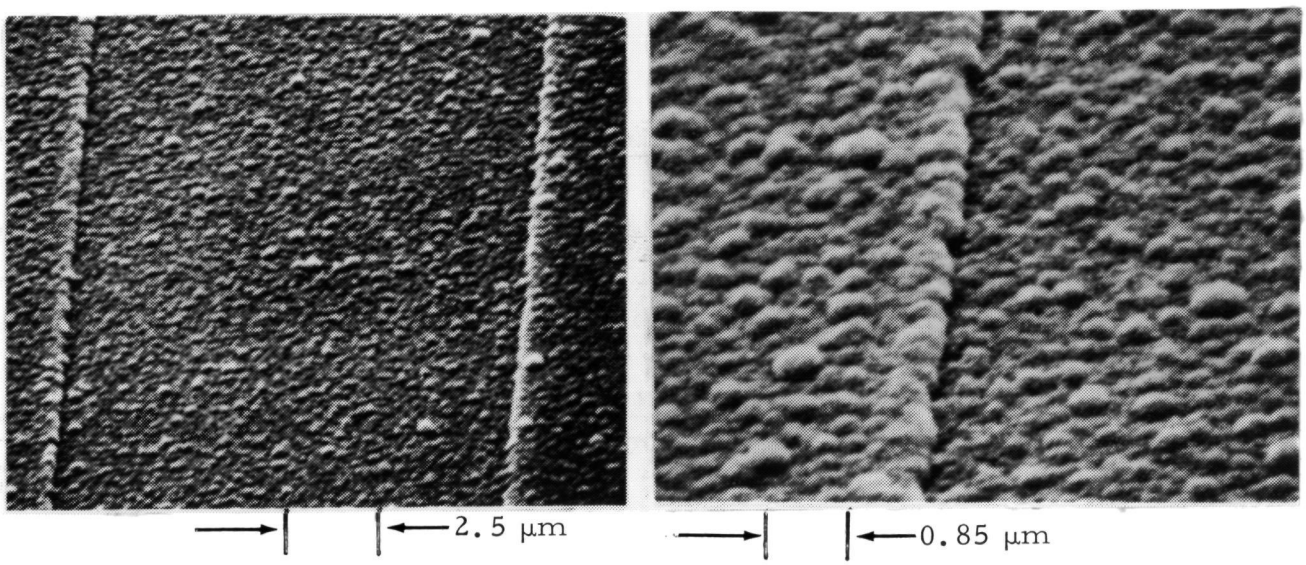


Figure 37. Granularity of LT CVD SiO_2 Following Use As Upper Level Insulator

Section 7
SUMMARY

This report has discussed the further development of advanced InSb monolithic charge coupled infrared imaging devices (CCIRIDs). This technology utilizes low-temperature chemical vapor deposited (LT CVD) SiO_2 as an InSb surface passivation which forms the basic MOS structure of the surface channel 4ϕ CCD, the principal component of the imager. The devices use transparent MOS photogates for charge integration to form the basic infrared detectors. During this contract period, 20-element linear imaging CCDs were fabricated and tested using an existing mask design designated the SBRC 8585. In addition, a next-generation CCIRID chip was designed which will extend the CCIRID technology into long "push-broom" type linear scanning arrays as well as area scanning arrays which will operate in the time-delay-and-integration (TDI) mode, thereby enhancing the signal/noise ratio of the IR sensors.

20-element linear imaging CCIRIDs fabricated, characterized and delivered on a previous contract are characterized by a CTE of $\sim$ 0.995 and a quantum efficiency of $\sim$ 50%. Corresponding MIS analysis of the LT CVD SiO_2 insulator indicates the CTE should approach 0.9995 or better. This difference is hypothesized to be attributed to lateral nonuniformities in surface potential arising from microscopic granularity in the LT CVD SiO_2. This is further not considered to be a fundamental limiting factor and alternate forms for depositing non-granular LT CVD SiO_2 have been pursued on Independent Research and Development programs. During this contract, efforts were directed toward alternate methods to relieve the granularity issue by eliminating process steps which would effectively enhance the LT CVD SiO_2 granularity. Realization of CTE improvement was not, however, accomplished due to a repetitive shorting problem related to electrostatic discharge arcing during RF and dc sputter depositions of SiO_2 and Al. Test devices with a newly developed transparent photogate material of indium tin

oxide were produced and analyzed which yield a transmission intensity of $\geq 70\%$ across the 2.5-5.4 μm spectral region and offer considerable promise for future improvement in the quantum efficiency of CCIRIDs. Additional characterization of a previously delivered 20-element linear imaging CCIRID operating in the multiplexing mode, and using clamped sample-and-hold (CSH) signal processing techniques resulted in an average $D^*\lambda_p$ value of 6.4×10^{11} cm-Hz$^{\frac{1}{2}}$-watt^{-1} for the full 20-elements at a $\lambda_p = 5.3$ μm. A maximum $D^*\lambda_p$ of 8.2×10^{11} cm-Hz$^{\frac{1}{2}}$-watt^{-1} was obtained for elements near the output end of the CCD register. Use of the CSH circuit resulted in dynamic range improvement from 118 to 470. The device was also evaluated in the TDI mode of operation with a resulting $D^*\lambda_p$ (TDI) = 8×10^{12} cm-Hz$^{\frac{1}{2}}$-watt^{-1}.

A next-generation CCIRID chip was designed, laid-out and masks procured. The chip is designated the SBRC 8587 and incorporates a 20 X 16 TDI area array, a 100-element linear imaging array, twin eight-bit shift registers for comparing charge transfer with a surface channel stop and a developmental planar channel stop, plus several test devices. All of the arrays have optional interconnections for charge extraction and amplification through on-chip MOSFETS and are intended for use on both InSb and HgCdTe.

Finally, two 20-element InSb CCIRIDs with characteristics similar to previously-delivered devices were tested and delivered to NASA Langley Research Center. These devices are identified as serial numbers 03 and 04 (Is 498-17-B2 and Is 498-17-B5).

APPENDIX

During this contract period, investigations into the use of plasma enhanced CVD (PECVD) SiO_2 to decrease the granularity, while maintaining the natural oxide, were initiated on a 1979 Independent Research and Development program. These initial investigations, using a reactor at Hughes Research Laboratory in Malibu, California, indicated the granularity could be reduced and a similar type system was capitalized for purchase by SBRC. The results of these investigations offered promise for oxide improvement on subsequent contracts, but the use of PECVD SiO_2 was not available for this contract.

Additional IR&D studies to reduce the granularity from depositions in the AMS-1000 and AMS-2600 reactors were also carried out. These were accomplished by variations in the deposition temperature. Although some improvement in granularity was realized, the surface state density increased. Thus this was not a feasible approach.

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15. Supplementary Notes

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Final Report

16. Abstract

This report discusses the continued development of monolithic InSb charge coupled infrared imaging devices (CCIRIDs). The processing sequence and structural design of 20-element linear arrays are discussed. Also, new results obtained from radiometric testing of the 20-element arrays using a clamped sample-and-hold output circuit are reported. At a background of $Q_B = 10^{12}$ photons-sec^{-1}-cm^{-2} and T = 65K, measured average $D^*_{\lambda p}$ values of 6.4×10^{11} cm-Hz$^{1/2}$-watt^{-1} were obtained for a 20-element array at a λ_p value of 5.3 μm. The design and layout of a next-generation CCIRID chip are discussed. The major devices on this chip are a 20×16 time-delay-and-integration (TDI) area array and a 100-element linear imaging array. The report also describes the development of a process for incorporating an ion-implanted S^+ planar channel stop into the CCIRID structure and the development of a thin-film transparent photogate. The transparent photogates will increase quantum efficiency to greater than 70% across the 2.5- to 5.4-μm spectral region in future front-side illuminated CCIRIDs.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
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