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**THIS NASA INVENTION APPEARS TO HAVE  
EXCELLENT COMMERCIAL POTENTIAL**

NASA CASE NO. **MFS-25,586-1**

PRINT FIG. **1**

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(NASA-Case-MFS-25586-1) MOTOR POWER FACTOR N82-11360  
CONTROLLER WITH A REDUCED VOLTAGE STARTER  
Patent Application (NASA) 17 P  
HC A02/MF A01 CSCL 09A Unclas  
G3/33 13570

# MOTOR POWER FACTOR CONTROLLER WITH A REDUCED VOLTAGE STARTER

## Technical Abstract

This invention relates to devices for reducing current surges occurring when induction motors are first started, and particularly to such devices for employment with three-phase motors where they are most often used.

Structurally, the invention is embodied in the form of an addition to a three-phase type motor power factor controller which is the subject of a pending patent application entitled "Three-Phase Power Factor Controller", bearing Serial No. 199,765, filed October 23, 1980. As will be noted, the application on the present invention is in the form of a continuation-in-part of this prior application.

Basically, the present invention adds to the three-phase system of the pending application means for modifying the operation of the system for a motor start-up interval of 5 to 30 seconds. The modification is that of providing via ramp generator 174 an initial ramp-like signal which replaces a constant power factor signal supplied by potentiometer 70. The ramp-like signal is applied to terminal 40 where it is summed with an operating power factor signal from phase detectors 32, 34, and 36 to thereby obtain a control signal for ultimately controlling SCR devices 12, 14, and 16 to effect a gradual turn-on of motor 10. The significant difference of the present invention over prior art is that the SCR devices are turned on at an advancing rate with time responsive to the combination signal described rather than simply a function of a ramp-like signal alone. The added signal, the operating power factor signal, enables the production of a control signal which effectively eliminates a prior problem with many motor starting circuits, which is that of accompanying motor instabilities.

It is believed also significant that by adding to the applicant's prior power factor control system a coordinate starting control that there is provided in one system an essentially complete motor control which provides both improved efficiencies during running operation and enables the elimination of current surges during start-up without attendant problems of rough starting.

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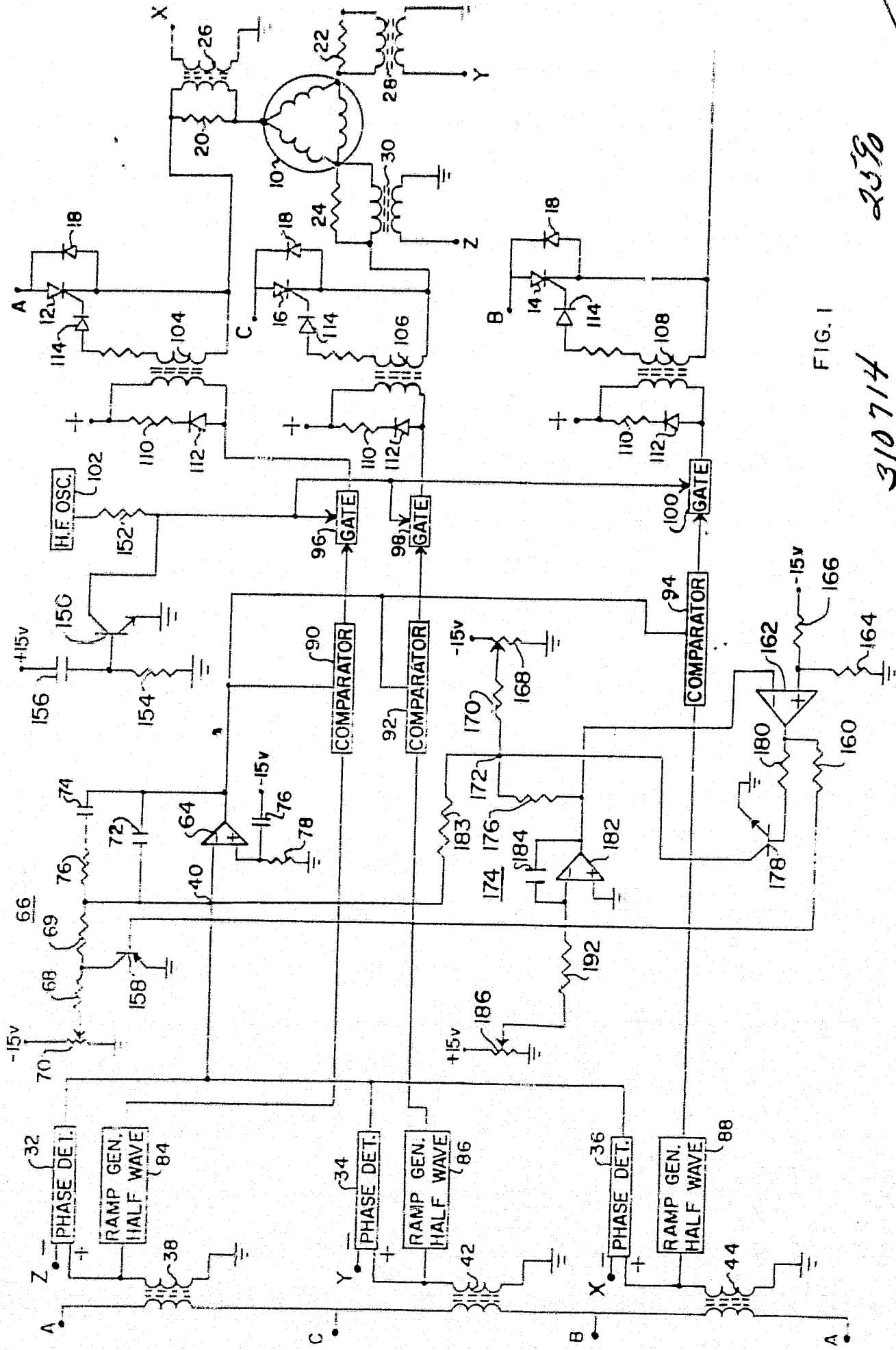


FIG. 1

310714 2390

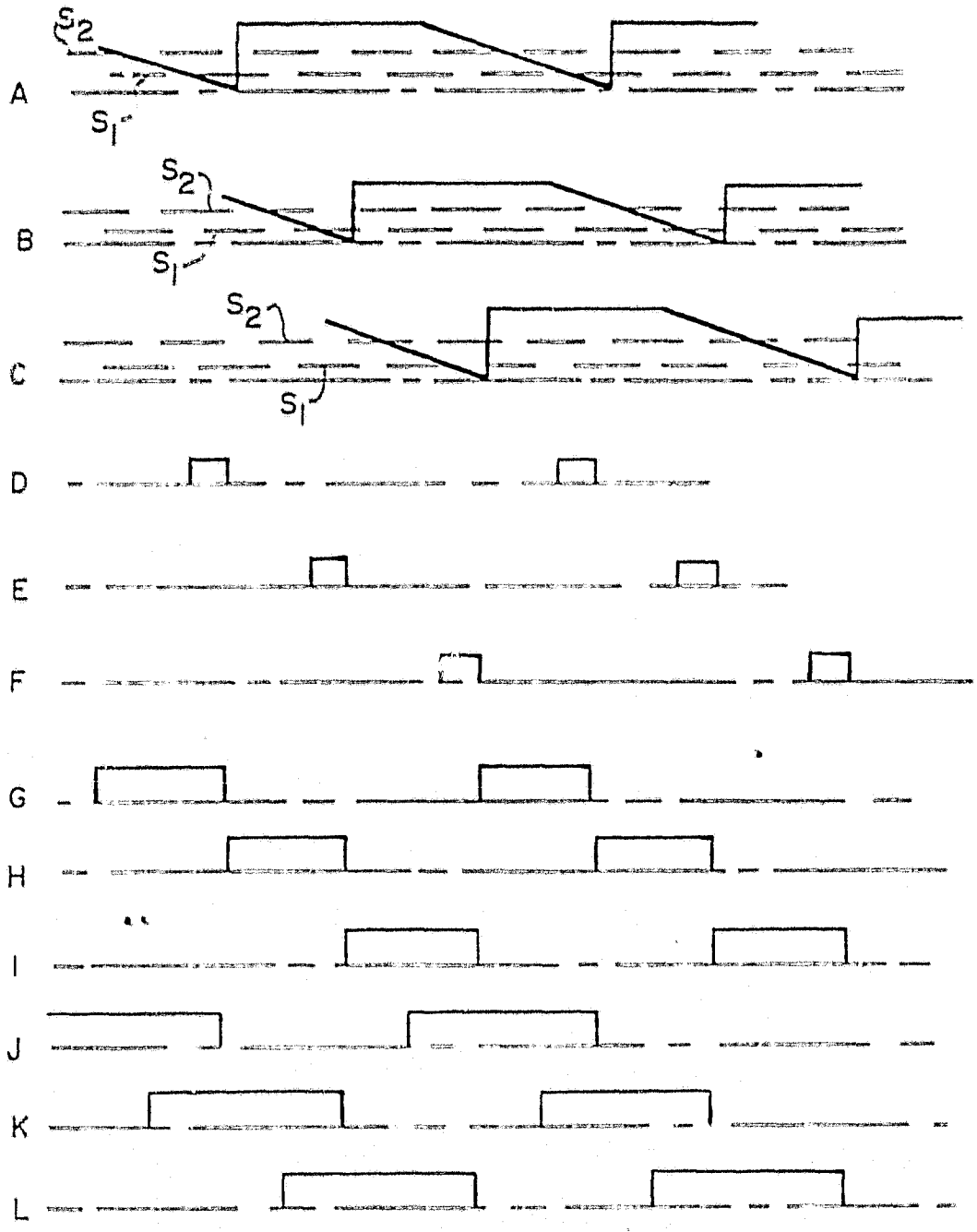


FIG. 4

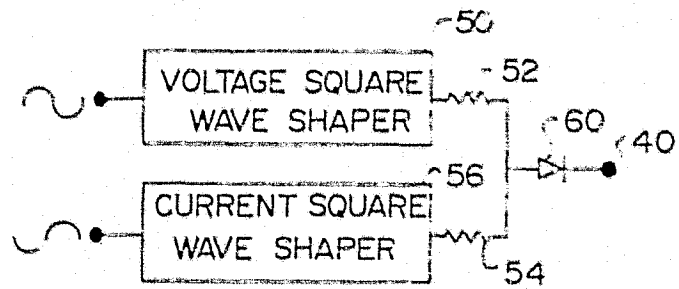


FIG. 2

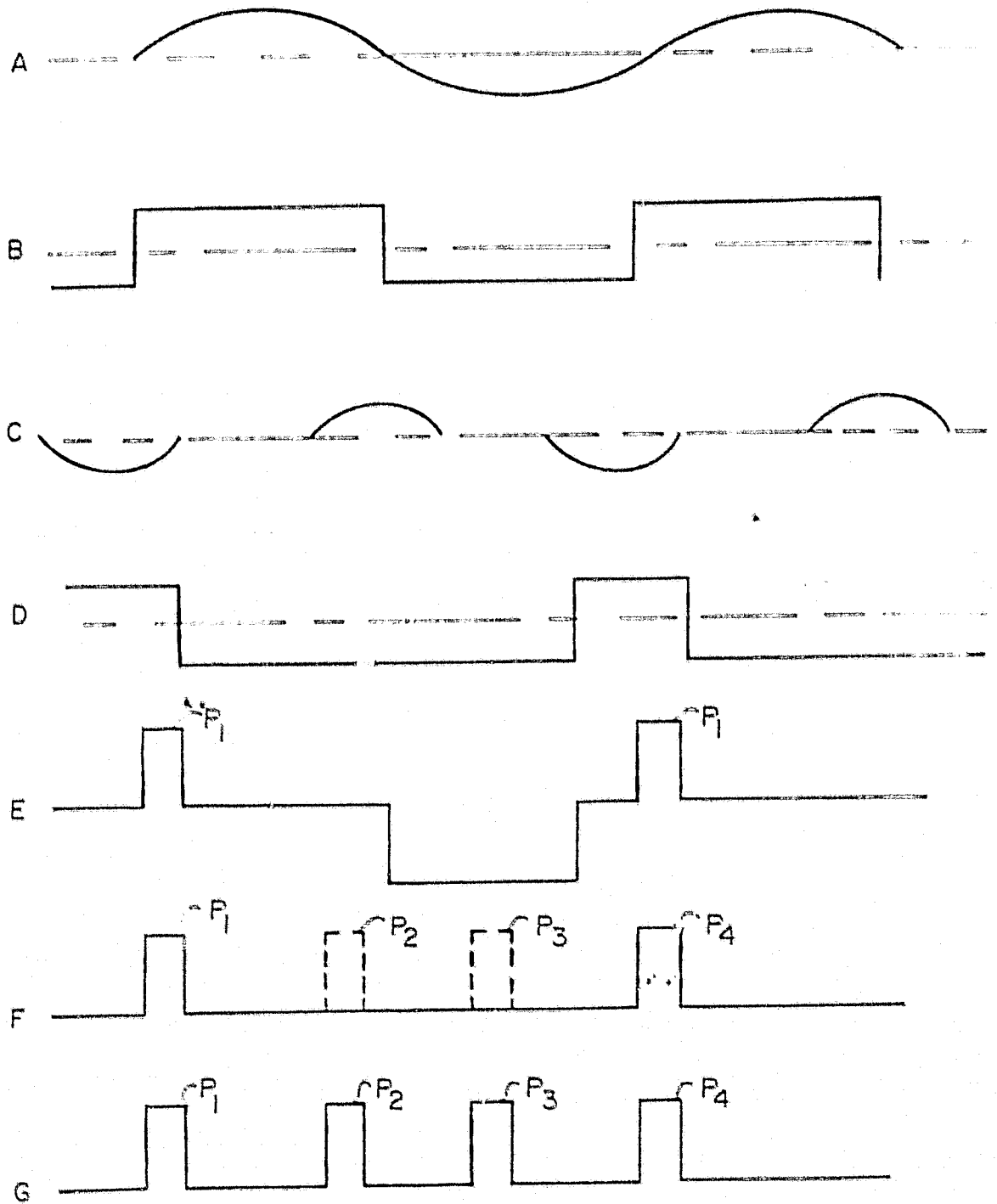


FIG. 3

## MOTOR POWER FACTOR CONTROLLER WITH A REDUCED VOLTAGE STARTER

Origin of the Invention

The invention described herein was made by an employee of the United States Government and may be manufactured and used by or for the government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

Technical Field

This invention relates generally to power input controls for induction motors, and particularly to a power factor type motor controller incorporating a reduced voltage starting capability.

This application is a continuation-in-part of application Serial No. 199,765, filed October 23, 1980, entitled "Three-Phase Power Factor Controller".

Background Art

In the applicant's Patent No. 4,052,648, entitled "Power Factor Control System for A.C. Induction Motors", there is disclosed a power reduction system for induction motors in which the operating power factor of a motor is monitored, and the effective voltage input to the motor is controlled as a function of the difference between a commanded power factor signal and the operating power factor. In the parent application, the applicant disclosed a power factor type control system particularly adapted for three-phase induction motors.

In addition to minimizing motor power consumption during normal running conditions, which was the goal of referenced patent application, a second area of concern is that of current surges which occur when a motor is first turned on. These surges can amount to five to eight times normal operating current and are both wasteful of electrical power and can contribute to excessive load surcharges being borne by electrical users. While discrete starting circuits have been employed which ideally gradually apply a starting volt-

age, it has been found that in some instances, these circuits fail to provide a smooth start-up, and not infrequently there may occur significant motor vibrations during at least a portion of the start-up interval.

5           It is the object of this invention to provide a single control system which both regulates power usage during normal running of a motor and provides for a graduated turn-on of motor voltage without the attendant problem of motor vibration. It is a particular object of the invention to provide a system of this category for a three-phase motor where  
10 graduated voltage starting circuits are most frequently used.

#### Disclosure of the Invention

In accordance with this invention, signal means are provided which initially block the application of the normal  
15 or "run" power factor command signal, and by means of a ramp signal generator, there is provided an increasing, with time, voltage in place of that command signal. This increase in voltage is of an amplitude and rate which will effect a graduated turn-on of the thyristor or thyristors  
20 of the motor circuit, effecting a full turn-on in a selected period of typically 5 to 30 seconds. A comparator examines the ramp voltage, and when the ramp voltage has risen sufficiently to effect a full turn-on of the thyristors and full motor operating speed, the comparator provides a sig-  
25 nal which unblocks the normal power factor command signal, enabling the turn-on of a thyristor or thyristors to thereafter be determined by motor loading in a conventional manner for a power factor type controller.

#### Brief Description of the Drawings

30           Fig. 1 is an electrical schematic diagram of an embodiment of the invention.

          Fig. 2 is an electrical schematic diagram of the phase detectors employed in the embodiment of the invention shown in Fig. 1.

35           Fig. 3 consists of a series of waveforms illustrative



of the operation of the phase detector shown in Fig. 2.

Fig. 4 consists of a series of waveforms illustrating the generation of triggering pulses in accordance with the circuitry shown in Fig. 1.

## 5 Detailed Description of the Drawings

Fig. 1 illustrates a three-phase power factor control system employing the invention. Three-phase motor 10 is powered through SCR (silicon control rectifier) devices 12, 14, and 16 from a three-phase power line, typically providing 220 or 440 volts, 60 cycle, A.C. from terminals A, B, and C. One phase of such a signal is illustrated by voltage wave a of Fig. 3. As the SCR devices provide for conduction only in one direction, a diode 18 is connected across each SCR and poled for opposite direction conduction. Current is sampled by current sampling transformers 26, 28, and 30, shunted by resistors 20, 22, and 24, each of these resistors being connected in series with an input to motor 10. Transformers 26, 28, and 30 are individually connected across one of these resistors (via a primary winding, as shown), and with one secondary terminal grounded, the other secondary terminal provides a discretely phased current signal output (as shown in waveform c of Fig. 3). Terminal X is associated with phase A, terminal Z is associated with phase C, and terminal Y is associated with phase B. A power factor signal, a signal inversely proportional to the current-voltage phase differential of each of the three-phase inputs, is obtained, separately, by phase detectors 32, 34, and 36. Phase detector 32 receives a current responsive signal sample from terminal Z, representative of the C phase current, and a voltage signal from transformer 38, representative of the A-C phase voltage, and provides a first phase detected output on terminal 40. Phase detector 34 receives a sample from terminal Y, representative of the B phase current, and a C-B voltage sample from transformer 42 and provides a second phase detected output on terminal 40. Phase detector 36 receives a phase A current signal sample from terminal X, and a B-A phase

voltage sample from transformer 44 and provides a third phase detection signal on terminal 40. The three signals, designated  $P_1$ ,  $P_2$ , and  $P_3$ , respectively, from the three-phase detectors are shown in waveforms f and g of Fig. 3.

5       The phase detectors are identical, and an embodiment of each is shown in Fig. 2. It includes two conventional squaring circuits. One is voltage square wave shaper 50, which provides through resistor 52 a rectangular wave (waveform b of Fig. 3) responsive to the input voltage  
10 (waveform a of Fig. 3). The second one is current square wave shaper 56, which provides through resistor 54 a rectangular wave (waveform d of Fig. 3), representative of the negative half cycle of input current (waveform c of Fig. 3). This output of phase detection is also noted by the  $\pm$  signs  
15 at the input terminals of the phase detectors (as shown in Fig. 1). The outputs of the two wave shaping circuits are combined through resistors 52 and 54. Diode 60 passes only the positive portion of each output to terminal 40, which is common with the outputs of phase detectors 32, 34, and  
20 36 (as shown in Fig. 1). Waveform e illustrates the combination process showing the waveform of a single phase detector as it would appear without diode 60, which diode eliminates the negative portions of the waveforms. Significantly, in the detection process, each phase detector  
25 produces a pulse (e.g.,  $P_1$  from detector 32,  $P_2$  from detector 34, and  $P_3$  from detector 36) which is, in effect, turned "on" by the leading or rising edge of waveform b and turned "off" by the trailing edge of waveform d. Thus, the width of pulse  $P_1$  (it has a constant amplitude) tends  
30 to increase upon the occurrence of increased phase angle between current and voltage (thus decreased power factor) and decrease in width with decreased phase angle (and thus increased power factor).

Assuming, as indicated, that pulse  $P_1$  represents the  
35 output of phase detector 32, waveforms f and g illustrate the relatively time presence of output pulses  $P_2$  and  $P_3$  from phase detectors 34 and 36, respectively. As the outputs are brought together at terminal 40, waveform g of

Fig. 3 illustrates the combined signals at this point. This composite of these becomes the basic feedback control signal, and as will be noted, this is a signal of pulses of a repetition rate of 180 Hz. This is in contrast to  
5 previous circuit approaches wherein a single phase detected output (from one of the three phases) is employed, which would, of course, have been either at a 60 Hz or 120 Hz rate, depending upon whether a half or full wave detection was employed.

10 The next step in accordance with this invention is to effect a signal conditioning of the control signal wherein the direct current character of the signal must be compatible with the thyristor trigger circuitry and still have a frequency response up to on the order of 20 Hz. The control signal is applied to the inverting input of operational  
15 amplifier 64 of signal condition or integrating circuit 66, together with a power factor command signal supplied through resistors 68 and 69 from potentiometer 70. Potentiometer 70 is biased negatively to provide a difference  
20 or subtraction signal with respect to the positive signal as developed at the outputs of the phase detectors. Signal conditioning is effected by an inverse feedback network consisting of two circuits, one being capacitor 72 connected  
25 between the output and inverting input of operational amplifier 64, and the other consisting of a series combination of capacitor 74 and resistor 76 connected between these two points. The feedback network is basically an integrative or lag one. The combination of resistor 76 (approximately  
30 15,000 ohms) and capacitor 74 (approximately 5 MFD) is initially effective (at zero frequency) to commence providing a lag effect. At about 2 Hz, the lag state commences to diminish as the value of resistor 76 commences to have a dominant effect over capacitor 74. Then, at about 20 Hz, capacitor 72 (approximately .68 MFD) commences to be ef-  
35 fective to again impose a pronounced lag effect. The resulting signal is a relatively smooth signal representing the integral of the composite outputs of the phase detectors less the command signal. The signal, as used, is repre-

5 sented by the sample signal waveforms  $S_1$  and  $S_2$  as shown in Fig. 4. It is important that while the signals have a relatively smooth and constant level, approximating the average signal value present, the signal must be responsive to signal changes incident to changes in motor loading, typically calling for a signal response upward to approximately 20 Hz. This is achieved by the circuitry shown.

10 The circuitry thus far described was designed for the development of a control signal for a regulation of input power to motor 10 once the motor was started. The present invention is particularly directed to developing a signal for controlling the application of power to motor 10 during the period from the instant when power is turned "on" for a discrete selected interval of typically 5 to 30 seconds, 15 during which the motor will have increased to operating speed. The purpose of this invention, as described above, is to prevent abrupt surges in input current which are not necessary for starting the motor and to accomplish this without accompanying instabilities. To accomplish this, 20 circuitry is added which provides a substitute command signal to that provided by potentiometer 70 during the start-up interval.

In order to insure that the substitute signal will be in place before any control signal is utilized, operational 25 amplifier 64, which processes control signals, is initially disabled for approximately 100 milliseconds. As operational control signals are applied to the inverting input of operational amplifier 64, and are negative going to provide turn-on signals for the thyristors, a counter or disabling 30 signal is applied to its non-inverting input. This is accomplished by applying a -15 volts to capacitor 76, which is in series with resistor 78, in turn connected between the non-inverting input of operational amplifier 64 and ground. The time constant of this circuit is adjusted to 35 effect signal blocking for the period described.

As a means of preventing a possible turn-on signal from getting to the thyristors until operational amplifier 64 is disabled, the output of trigger oscillator 102, which

triggers on the thyristors, is initially blocked. This is accomplished by NPN transistor 150, which is connected through output resistor 152 across the output of oscillator 102. Transistor 150 is initially turned "on", shorting  
5 the output of oscillator 102 by a declining ramp signal appearing across resistor 154, which is in series with capacitor 156 and a +15 volts source. Typically, the time constant provided by resistor 154 and capacitor 156 is such that transistor 150 would be essentially discharged in ap-  
10 proximately 10 milliseconds, after which the blocking action would cease and transistor 150 would be turned "off", enabling a normal output from oscillator 102.

In addition to the precautions described above to insure that motor 10 will not turn "on" before the starting  
15 circuitry is operative, means are provided to prevent the application of a normal "run" command signal from potentiometer 70 during the entire starting interval. This is accomplished by connecting PNP transistor 158, collector-  
to-emitter across the output of potentiometer 70, between  
20 resistors 68 and 69. Transistor 158 is turned "on" upon the application of power to the circuitry by a negative voltage applied to its base through resistor 160 from the output of operational amplifier 162. In this manner, the output of potentiometer 70 is effectively shorted out.  
25 The negative output state of operational amplifier 162 is effected by applying a greater negative bias on its non-inverting input than on its inverting input. The bias to the non-inverting input is a fixed bias, being a selected fraction of -15 volts as provided by a voltage divider  
30 comprising resistors 164 and 166 and connected across the -15 volts as shown. Initially, the voltage applied to the inverting input of operational amplifier 162 is zero, the initial output of operational amplifier 182, and thus the potential on the non-inverting input of operational  
35 amplifier 162 prevails.

Potentiometer 168, through resistor 170, provides an initial starting level negative signal to terminal 172 where it is added to a negative going, start-up, ramp

signal supplied from the output of starting ramp generator 174 through resistor 176.

5 NPN transistor 178 is connected emitter-to-collector between terminal 172 and ground and provides means of blocking an interfering effect from a starting signal after the starting sequence. Transistor 178 is controlled by an output through resistor 180 from operational amplifier 162 and is initially held "off" during the starting sequence by the negative output of operational amplifier 162.

10 Starting ramp generator 174 is a conventional integrator comprising operational amplifier 182 and a capacitor 184 connected from its output to its inverting input. A selected positive bias is obtained from potentiometer 186, connected between the +15 volts terminal and ground. 15 This bias is fed through input resistor 192 to the inverting input of operational amplifier 182. The result is that, upon the application of voltages to the circuit, there will initially occur at the output of operational amplifier 182 an essentially zero voltage which ramps down 20 negatively at a selected rate determined by this bias and the time constant of capacitor 184 and input resistor 192 to achieve a desired rate of motor turn "on" signal. The negative going signal at the output of operational amplifier 182 is fed through resistor 176 to terminal 172 and 25 there added to a voltage from potentiometer 168, fed through resistor 170. This signal is then applied through resistor 183 to terminal 40 and there summed with the operating power factor (or current-voltage phase angle) signal and applied to operational amplifier 64 to effect 30 an increasing (negatively) control signal which gradually, over a typical period of 5 to 30 seconds, results in effective motor voltage to be raised to full voltage. The actual operational control effected by the control signal on the thyristors is discussed below.

35 The output of operational amplifier 182 is also applied, in this case, to the inverting input of operational amplifier 162; and when the output rises to a level which exceeds the level applied to the non-inverting input of

operational amplifier 162, the output of the latter switches from a negative state to a positive state. This changed state is fed as a switching potential to transistors 178 and 158 to turn transistor 178 "on" and transistor 158 "off". The result is that transistor 178 prevents any further starting signal from appearing at terminal 172, and transistor 158 unblocks the output of potentiometer 70 to restore normal power factor control for "run" operation of motor 10.

10        It is significant that during the start-up cycle, although the normal power factor command signal from potentiometer 70 is disabled, the effective power factor signal, summed from phase detectors 32, 34, and 36, continues to be an effective control input. This combination overcomes  
15 the tendency of motor instabilities to occur, which is common with certain other types of motor start-up circuitry.

Actual thyristor triggering signals, whether during the start of run modes, are developed by the comparison of the control signal (e.g.,  $S_1$  and  $S_2$  of Fig. 4) output of  
20 operational amplifier 64 and ramp shaped signals  $r$ . A ramp signal for each phase is developed by one of conventional ramp generators 84, 86, and 88, responsive to A-C, C-B, and B-A phase voltages from transformers 38, 42, and 44, respectively. The ramp outputs  $r$  of these generators  
25 are illustrated by solid line in waveforms a, b, and c, respectively, of Fig. 4, and are separately applied to conventional comparators 90, 92, and 94, together with a control signal from operational amplifier 64. In operation, a comparator provides a pulse output when the level  
30 of the control signal, e.g., dashed line  $S_1$  of Fig. 4, intersects the leading edge of a ramp signal. Thus, as shown, for example, with a control signal  $S_1$  applied to the comparators, there is produced output pulses shown in waveforms d, e, and f of Fig. 4. These pulses, which result  
35 in the triggering of the thyristors, as will be described, occur once per cycle, and are thus representative of a half wave mode of operation. The relatively narrow triggering pulses shown as waveforms d, e, and f

of Fig. 4 produce relatively short turn-on times for SCR devices 12, 14, and 16, and thus produce a relatively low RMS input voltage to motor 10. This state of operation will initially have been brought about by phase detectors  
5 detecting a downward shift in power factor (by an upward shift in current-voltage phase angle) occurring when motor loading is shifted to a low state. The resulting output signal of operational amplifier 64 will be such as to produce a motor RMS input voltage which brings about an  
10 equilibrium between the commanded power factors determined by the bias output of potentiometer 70 and integrated output of the phase detectors.

The actual control of the current turn-on periods for the thyristors is effected by gates 96, 98, and 100, which  
15 pass high frequency signals responsive to the outputs of comparators 90, 92, and 94. Gates 96, 98, and 100 are electronic switches and function to effect gating of the high frequency signal (e.g., 10 KHz) from high frequency oscillator 102 through the primary windings of transfor-  
20 mers 104, 106, and 108 to the thyristors. Resistor 110 and diode 112 are connected in series across the primary of each transformer in order to suppress inductive volt-ages to a safe level consistent with semi-conductive cir-  
cuits employed. The secondaries of transformers 104,  
25 106, and 108 are connected (as shown) in series with diode 114 between the gate and cathode of SCR devices 12, 14, and 16. Turn-on periods for the thyristors follow, for example, the period of the pulse outputs of the comparators (as shown in waveforms d-i). The waveforms marked  
30 by waveforms g-i, which are produced by control signal  $S_2$ , are illustrative of the turn-on periods for a moderately to substantially loaded motor in contrast to pulses shown in waveforms d-f, which are indicative of a slightly loaded or a motor having no load.

35 During start-up, there would initially be provided a triggering output as illustrated by the narrow width pulses shown in waveforms d-f, and these would gradually widen until they were of a complete half cycle width as represented



by waveforms j-l as the output of ramp generator 174 increases negatively as described. After the start-up period, and assuming there is a lightly loaded or unloaded motor, the system would adjust to a control as dictated by potentiometer 70 to provide, again, minimum length pulses as shown in waveforms d-f. Alternately, if the motor were moderately loaded, the "after" pulse widths would be as shown by waveforms g-i.

While there is illustrated herein the application of the present invention to a three-phase system, the invention is equally applicable in the manner described to a single-phase system. Further, while Fig. 1 illustrates a three-phase system employing SCR devices as thyristors in a basically half wave control system, it is to be appreciated that the invention is also applicable to full wave three-phase systems employing either triacs or SCR devices connected in anti-parallel.

In summary, it is to be noted that by means of the present invention, the substantial benefits provided by a power factor type controller for a running motor may be extended to cover motor start-up and thus to provide a single and overall control for an induction motor.

MOTOR POWER FACTOR CONTROLLER WITH A  
REDUCED VOLTAGE STARTER

ABSTRACT

5 A power factor type motor controller in which the  
conventional power factor constant voltage command  
signal is replaced during a starting interval with a  
graduated control voltage. The present invention adds  
to the three-phase system of pending application Serial  
No. 199,765, filed October 23, 1980, means for modifying  
10 the operation of the system for a motor start-up interval  
of 5 to 30 seconds. The modification is that of providing  
via ramp generator 174 an initial ramp-like signal which  
replaces a constant power factor signal supplied by  
potentiometer 70. The ramp-like signal is applied to  
15 terminal 40 where it is summed with an operating power  
factor signal from phase detectors 32, 34, and 36 to  
thereby obtain a control signal for ultimately controlling  
SCR devices 12, 14, and 16 to effect a gradual turn-on  
of motor 10. The significant difference of the present  
20 invention over prior art is that the SCR devices are turned  
on at an advancing rate with time responsive to the  
combination signal described rather than simply a function  
of a ramp-like signal alone. The added signal, the  
operating power factor signal, enables the production of  
25 a control signal which effectively eliminates a prior  
problem with many motor starting circuits, which is that  
of accompanying motor instabilities.