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Development Report: Automatic System Test and Calibration (ASTAC) Equipment

Robert J. Thoren
Paragon Pacific, Inc.

July 1981

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Lewis Research Center
Under Contract DEN 3-203

for
U.S. DEPARTMENT OF ENERGY
Conservation and Renewable Energy
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Division of Wind Energy System
Washington, D.C. 20545
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FOREWORD

The work documented in this report was performed under Contract DEN3-203 issued by the NASA Lewis Research Center, Cleveland, Ohio 44135. The contract work was performed by Paragon Pacific, Inc., El Segundo, California 90245, under the technical direction of Mr. David C. Janetzke of the Lewis Research Center.

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SUMMARY

The Automatic System Test and Calibration (ASTAC) Equipment has been developed by Paragon Pacific, Inc. to be used in conjunction with the NASA Lewis Research Center Wind Energy System Time-Domain (WEST) Analyzer. ASTAC is used to monitor the performance of the WEST Analyzer and to identify component malfunctions which may occur from time to time within WEST.

The heart of the ASTAC system is a microcomputer which is used to input prescribed test signals into all WEST subsystems via a hybrid interface unit, and to process WEST output responses to these test signals. Measured responses are compared to theoretical levels calculated off-line using specialized ASTAC software. This report describes the microcomputer, the interface unit and the software packages which in total comprise the ASTAC system.

Examples of ASTAC test results obtained on the WEST Analyzer are presented and described in detail. In addition, a section has been included which briefly describes the methods by which the microcomputer and interface unit can be maintained.

INTRODUCTION

This report describes the Automatic SPHYC* Test and Calibration System (ASTAC) developed by Paragon Pacific, Inc. (PPI) under contract with the NASA Lewis Research Center, Cleveland, Ohio. ASTAC is a microprocessor-based, stand-alone automatic test system developed for use in conjunction with the Wind-Energy System Time-Domain (WEST) Analyzer (see Reference 1). ASTAC will be used to monitor the performance of the WEST analyzer. Figure 1 is a photograph of the complete ASTAC system.

General Description of the ASTAC System

ASTAC utilizes a microprocessor based controller and interface unit to open and close electronic switches within WEST circuits by command from data contained on a "floppy disk" storage device. Test signals are substituted into the open circuits, and resulting subsystem performance is measured. The measured performance is compared to theoretically correct performance indices also contained on a floppy disk. Test results are available for viewing on a cathode ray tube (CRT) or in hard copy from a line printer.

Organization of the Remaining Sections of This Report

The next section discusses the need for ASTAC and the specific functions performed by the system.

The following section presents a brief technical description of the ASTAC system. The major hardware elements incorporated in ASTAC are described as well as the two different types of ASTAC/WEST interface ports.

The various software packages which form a key element of the ASTAC system are explained in the next section.

Following the software section is a description of the measurements obtained from running the ASTAC system. Factors effecting the accuracy of these measurements are also discussed.

A section discussing the procedures by which the ASTAC hardware can be maintained is included.

Conclusions and recommendations for additional ASTAC refinement are presented in the last section.

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*SPHYC is an acronym for Special Purpose Hybrid Computer.

THE NEED FOR ASTAC

All SPHYC's including the WEST analyzer are special purpose hard-wired hybrid computers specifically designed to solve complex linear and nonlinear differential equations.

The equation sets are implemented using Paragon's library of analog, digital, and hybrid computational module printed circuit cards, which utilize both analog and digital integrated circuits (IC's). The types and quantities of these PC cards incorporated into any one SPHYC is a function of the numbers and complexity of the equations implemented.

WEST, incorporating one hundred and thirty-three (133) of these module cards, is fairly average in terms of its hardware count. Table I presents the actual breakdown of the types and quantities of electronic hardware utilized in WEST and is included herein to give the reader an idea of the complexity of a typical SPHYC.

TABLE I

WEST/ANALYZER ELECTRONIC COMPONENT SUMMARY

DESCRIPTION	QUANTITY
High Gain Amplifiers	123
Summer/Inverter Amplifiers	196
Integrators	30
Multipliers	190
Potentiometers	504
Analog Switches	80
Comparators	38
Sample/Hold Amplifiers	48
Analog Multiplexers	308
Voltage Followers	18
Digital Inverters	18
Digital Gates	39
J-K Flip-Flops	10
Sundry Digital	30
Total Number of Operational Amplifiers =	415

Performance verification and system maintenance are two very important issues which need to be addressed when comtemplating dynamic simulations as complex as WEST. Specifically, how can one monitor the performance of WEST and, if improper performance is detected, identify the one or several components (out of thousands) which may be malfunctioning, without using inordinate amounts of skilled, and expensive, engineering labor resources. The ASTAC system was Paragon's solution to this maintenance problem. ASTAC has been designed specifically to perform the following performance verification and maintenance tests on the WEST Analyzer:

- Rapidly verify correct system performance on a routine basis by comparing the calculations made by WEST subsystems with theoretical results derived directly from the implemented equations;
- Quickly detect excessive drift or lack of repeatability in high speed analog sections;
- Diagnose quickly the specific components at fault when incorrect system performance has been detected;
- Detect when WEST limits (e.g., maximum analog voltages) have been exceeded during productive operation of the simulator.

TECHNICAL DESCRIPTION OF THE ASTAC SYSTEM

Figure 2 depicts the overall hardware implementation of the ASTAC system. The heart of the system is a microcomputer, which can be connected by telephone lines to an off-site general purpose digital mainframe and which can function as a remote batch terminal. WEST test procedures, processed off line using the digital mainframe, are received over the telephone lines by the microcomputer and stored on a "floppy disk." The microcomputer is also connected to WEST by an interfacing unit referred to as the ASTAC Interface Unit or AIU. The AIU communicates with the microcomputer through a standard serial digital I/O port. Both the microcomputer and AIU are described in this section.

Microcomputer Hardware

The microcomputer utilized in the ASTAC system is the PDP1103 manufactured by Digital Equipment Corporation (DEC). This system was selected for the ASTAC application because of its industry wide acceptance, relatively low cost, proven maintainability, and its full line of well documented and time tested software. The PDP1103 system utilized in ASTAC incorporates the following components:

PDP1103 Microcomputer - A packaged version of the DEC LS1-11 microcomputer which includes a rack-mountable enclosure containing the LS1-11 16-bit processor, 32K x 16-bit memory, a four channel asynchronous serial line unit for interfacing peripheral devices to the LS1-11 bus, an LS1-11 bus-structured backplane, the power supply, and a switch indicator panel;

RX01 Dual Floppy Disk Drive - 0.2M byte capacity per disk drive;

VT100 DECscope Terminal - Video screen with keyboard;

LA180-PA Line Printer - 132 characters maximum per line. Line rate varies from 50 to 450 lines/minute depending on column width.

ASTAC Interface Unit

The ASTAC Interface Unit serves as the hardware link between the microcomputer and the WEST Analyzer. Controlled by the microcomputer, ASTAC generates test signals (voltages), into the many WEST subsystems via specially provided AIU/WEST interface ports. The AIU also measures WEST responses to these prescribed test voltages.

Figure 3 presents a detailed block diagram of the AIU. The primary components are as follows:

- Interfacing logic which decodes and latches the bit stream coming from the microcomputer, and also recodes data for transmittal back to the microcomputer;

- D to A and A to D converters which interface the microcomputer-produced digital data to analog signals, when required by a test;

- Switches which are normally closed for WEST operation, but which can be opened by command from the microcomputer. When open, the switches cause computational circuits in WEST to be broken, so prescribed signals produced by the microcomputer can be substituted in lieu of signals produced by WEST. In this way, subsystems in WEST can be driven by "known" signals, in order to test the subsystems by measuring calculated signals and comparing them to the theoretical values;

- An addressing system which commands the selector, built into the WEST unit, to select signals for a test. After transmittal back to the microcomputer, these selected signals are compared with theoretical values and printed.

The AIU uses the same modular design as the WEST Analyzer: it consists of a number of Paragon analog, digital, and hybrid function printed circuit cards plugged into a standard card cage with wirewrap interconnects between PC cards. Figure 4 is a photograph of the types of printed circuit cards in the AIU. Figure 5 is a photograph of the AIU card cage.

The front panel of the AIU contains several switches and connecters which are provided for configuring the RS-232 serial digital data interface between the microcomputer and AIU. Variables such as data word length and transmission rate (Baud Rate) are programmed using these controls.

AIU/WEST Interface Ports

Figure 6 presents a representative example of one of the many circuits programmed into the WEST Analyzer. Keeping with traditional hybrid system programming, each different type of symbol in the figure is associated with a particular electronic component or group of components. Paragon has selected the oval symbol to represent AIU/WEST interface ports. The oval symbol, labeled BK, with one input and one output is referred to as a "break port." The break port can be thought of as a switch which is closed during normal WEST operations, but which can be commanded open to have a specified test voltage applied to its output.

These switches reside within the AIU and are connected to the WEST Analyzer by means of an interface cable, as illustrated in Figure 7. DL in Figure 7 is a digital logic signal which controls the state of the electronic switch. When DL is low (0 volts), the switch selects the normal input (the break port is considered closed). When DL is high (+10 volts), the break port is open and the switch output will be equal to V_{test}, the signal present on the sample/hold amplifier output. The state of the switch (open or closed) and the value of V_{test} are specified by the microcomputer.

There are one hundred and forty-four (144) of these electronic switch-sample/hold amplifier pairs wired into the AIU, requiring four interface cables (36 switches per cable). The interface cables are attached to the WEST and AIU at four rear panel connectors on each drawer.

The oval symbol with only one input (labeled IX in Figure 6) is referred to as an "interrogate port." In reality, each interrogate port is a separate input to a 64 channel input x 1 output multiplexer PC card, and each can be monitored by the AIU as commanded by the microcomputer. Figure 8 presents a photograph of the 64 x 1 multiplexer (MUX) card.

There are provisions within the WEST Analyzer for five of these 64 x 1 multiplexer PC cards, constituting a total of 320 separate channels. The MUX cards are inserted into specially provided connectors on the rear panel of the Analyzer. MUX addressing is accomplished via a controller cable between the AIU and WEST Analyzer.

Figure 9 depicts the AIU/WEST installation. The upper cabinet houses the AIU. The break interface cables, MUX controller cable, and multiplexer cards are visible in the photograph.

SUPPORTING SOFTWARE

Paragon Pacific has developed several software packages (all coded in FORTRAN) which form a key element of the ASTAC system. These codes are used for processing the hundreds of variables and constants associated with the math models implemented in WEST, for calculating theoretical system and subsystem level response to prescribed test setups, and for executing the tests utilizing the AIU. Each of these codes is discussed in this section.

Program SYSTEP

The System Test Program (SYSTEP) is the main batch-processing code which prepares WEST test procedures and other supporting data. SYSTEP is actually two independently executable digital computer programs, called SYST1 and SYST2 for convenience.

SYST1 is used for processing the many variables and constants present in the WEST simulations. Alphabetical listings of all variables are produced by SYST1 with scaling values and a brief description of each. Break and interrogate addresses, for those variables incorporating them, are also provided. An alphabetical listing of all constants is prepared too. In addition, all scalar equations implemented in WEST are coded in FORTRAN, and processed by SYST1 for later use by SYST2.

SYST2 reads in: (1) the FORTRAN equations processed by SYST1, (2) the parametric values for all system constants defined in SYST1, and (3) a set of test specifications defining the specific tests to be performed by ASTAC on the WEST Analyzer. SYST2 then solves the FORTRAN equations for each test setup and prepares a listing (by test) presenting the theoretical resultant for each WEST variable effected by each test. SYST2 also generates an output file containing the test setups and theoretical results, formatted for transmission over the telephone to the ASTAC microcomputer. This file is stored on a floppy disk for direct use in the automatic testing of the WEST Analyzer.

Program TESTIT

Program TESTIT is the in-house code that reads and executes the test specification file generated by SYST2. This code is resident in the PDP1103 microcomputer and is keyboard controlled.

In addition to executing the automatic test setups stored on floppy disks, TESTIT can be operated in a manual mode, where test instructions created directly at the keyboard are implemented. It can also be executed in an auto-scan mode. In this mode, all WEST variables possessing interrogate ports are continuously monitored by the AIU. Any system overloads which may occur are then detected by the AIU and displayed either on the terminal or line printer.

ASTAC TEST RESULTS

WEST/ASTAC test results are available for viewing using either the PDP1103 CRT (cathode ray tube) or in hard copy using the line printer. Measured and theoretical voltages are presented for each variable processed during the execution of a test. Figure 10 presents a typical test with the various data items identified. Figure 11 presents a portion of an ASTAC listing for the WEST Analyzer.

The complete test specifications file for WEST consists of one hundred and nineteen (119) separate tests of the type indicated in Figure 11. These tests exercize all electrical hardware associated with each of the many scalar equations hardwired in the WEST Analyzer. Most of the tests are of a static nature where measured outputs do not vary in time; however, certain subsystems within WEST require dynamic tests. One example is a gain check of the wind turbine blade radial integrators. The integrators are first reset to zero volts and then commanded to integrate a prescribed input voltage. Each integrator output is then interrogated after a prescribed time interval and compared to its theoretical output.

Examination of the test results presented in Figure 11 reveals for the most part excellent agreement between measured and theoretical values for the many variables processed. Discrepencies are typically under 100 millivolts which represents a full scale (10 volt signal level) error under one percent.

Experience gained with the AIU seems to indicate that it typically exhibits a full scale error of less than $\frac{1}{4}$ percent. This means that it can set and/or interrogate a full scale signal (±10V) to within ±25 millivolts.

The primary cause of AIU error is associated with the sample/hold amplifiers utilized in the AIU. These devices tend to drift from a prescribed held value. The drift rate can be reduced by increasing the size of the hold capacitor used with each sample/hold amplifier; however, there are trade offs involved. Increasing the size of the hold capacitor increases the time needed to acquire a prescribed voltage, and also increases the problem of dielectric absorption - a phenomenon whereby a sample/hold amplifier tends to return to the voltage it was holding before being set to a new value.

The greatest shortcoming of the ASTAC system is in the areas of dynamic testing. The nature of a dynamic test implies performing interrogates at prescribed time intervals after the beginning of a test. The ASTAC hardware is limited in its ability to precisely control the timing of an interrogate command. The restricting factor is the transmission rate of the PDP1103 microcomputer. The PDP1103 transmits data across the serial I/O port to the AIU at the rate of only 1000 bits per second. This translates into a maximum AIU measure command processing rate of only one every 30 milliseconds. Thus, 0.3 seconds elapses between the first and tenth measurements of a test requiring the simultaneous measurement of ten WEST variables.

Fortunately, this shortcoming in the ASTAC system only slightly diminishes its usefulness. The vast majority of testing required to be performed by ASTAC is static in nature; and critical timing is also not a consideration in the dynamic tests used with WEST.

ASTAC MAINTENANCE

The ASTAC Interface Unit was designed with built-in circuitry which, in conjunction with a software package named ASTX, can execute fully automatic diagnostic checks of key hardware elements within the AIU. Program ASTX resides in the PDP1103 and is keyboard controlled. It issues specific instruction sets to the AIU when the AIU is undergoing self-testing. An error message is displayed on the CRT if the AIU fails any one of the diagnostic tests. The error message indicates the type of failure and the particular subsystems involved.

The WEST Analyzer, developed for the NASA Lewis Research Center incorporates Verification And Calibration Equipment called VACE. VACE is used for testing and calibrating the many printed circuit module cards utilized in WEST. This same unit can be used for testing and calibrating, when necessary, the printed circuit cards in the AIU. This feature provides NASA with the key tools necessary to maintain the AIU; malfunctions within the AIU are identified using program ASTX, and VACE is then used to locate the malfunctioning printed circuit card component(s).

An extensive set of well documented, self-diagnostic procedures for the PDP1103 component of the ASTAC system has been developed by Digital Equipment Corporation for use when troubleshooting this equipment. These diagnostic tests are resident on floppy disk and can be executed by anyone familiar with the PDP1103 system.

CONCLUSIONS AND RECOMMENDATIONS FOR ADDITIONAL ASTAC DEVELOPMENT WORK

The ASTAC system has successfully demonstrated its ability to quickly and accurately assess the performance status of the many subsystems programmed into the WEST Analyzer, and to identify and localize malfunctions when they occur. One hundred and nineteen (119) separate tests are executed by ASTAC and approximately 320 individual WEST signals are monitored. The complete set of diagnostic tests can be executed in little more than twenty minutes, including setup time. Manual tests as thorough as those executed automatically by the ASTAC system would require days, and sometimes weeks to perform.

Complex simulations such as that offered by the WEST Analyzer are only as useful as they are reliable. Daily verification of the many WEST subsystems made possible by the ASTAC system should greatly increase user confidence with WEST. ASTAC is an indispensable element of the WEST Analyzer, and in a very real way makes WEST and other custom hardwired hybrid systems practical reality.

Recommendations for Additional Work

This report has dealt with ASTAC primarily as a maintenance tool; however, it also offers other unique capabilities. The readers attention is directed to Reference 1, wherein the recommendation was first made that ASTAC be used not only as a maintenance tool, but also as a WEST controller and data handler. As a controller, ASTAC would be used to automatically program the Analyzer for a specific case(s) (i.e., nominal windspeed, direction, wind gust power spectra, power network loading spectra). Keyboard instructions would replace the manual adjustment of WEST front panel controls. As a data handler, ASTAC would be used to automatically interrogate selected WEST outputs (e.g., blade loads, blade flapping angles, etc.). Time histories of these variables would be stored on floppy disks and would be available for post processing using the microcomputer within ASTAC. Hard copy plots could be produced if required.

Serious consideration should be given to using the ASTAC system in this expanded role. The hardware and software elements required are almost all available in the WEST/ASTAC systems. A minimal effort is all that should be required to add this capability.

REFERENCES

1. Hoffman, John A.: Development Report: Wind Energy System Time-Domain (WEST) Analyzers Using Hybrid Simulations Techniques. NASA CR-159737, February, October, 1979.

FIGURE 1 - ASTAC SYSTEM HARDWARE

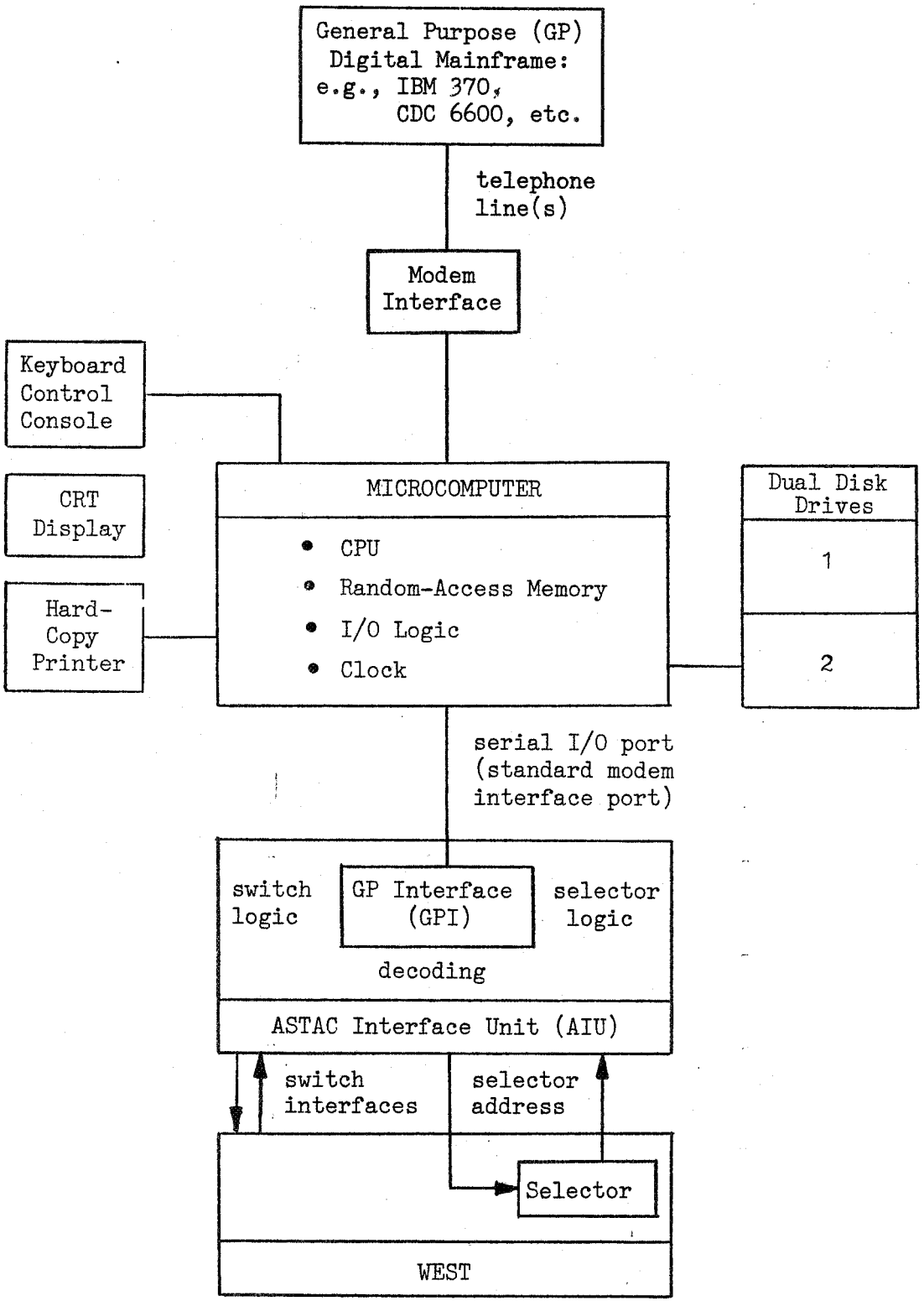

Figure 2 - General ASTAC System Arrangement

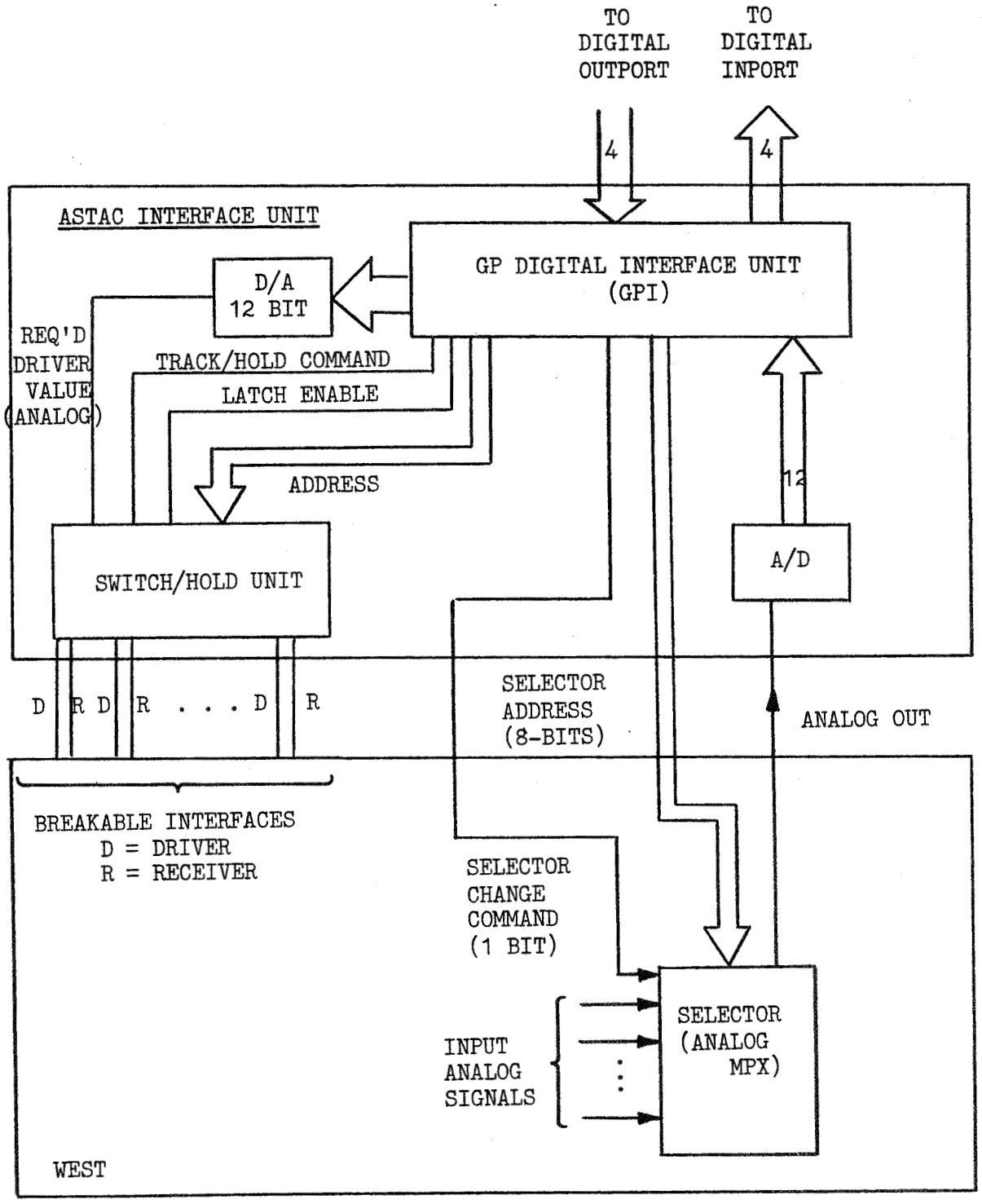

FIGURE 3 - ASTAC Interface Unit and Test Article

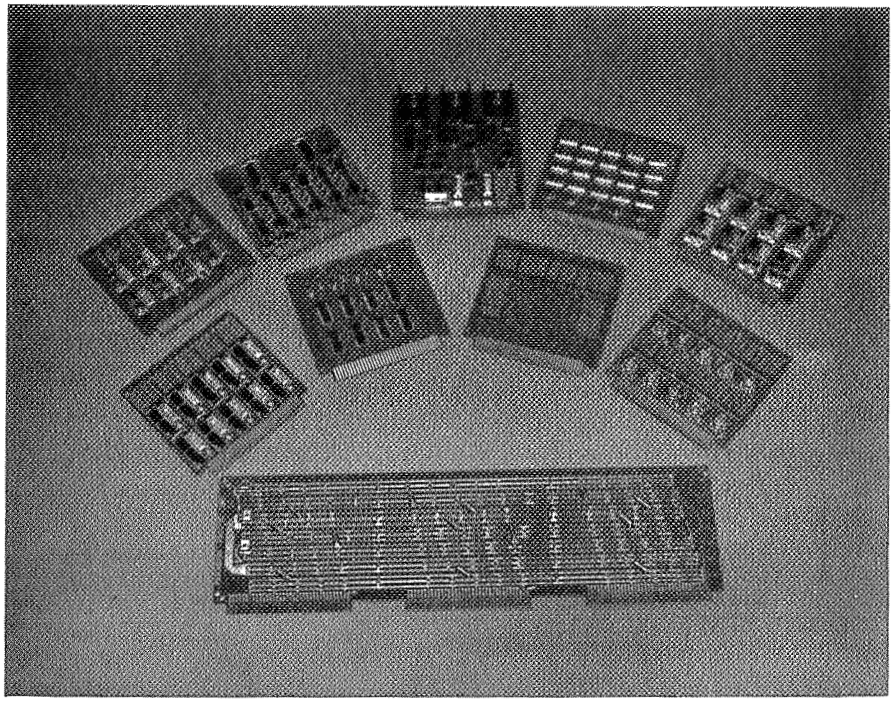

FIGURE 4 - EXAMPLES OF PRINTED CIRCUIT CARDS UTILIZED IN THE AIU

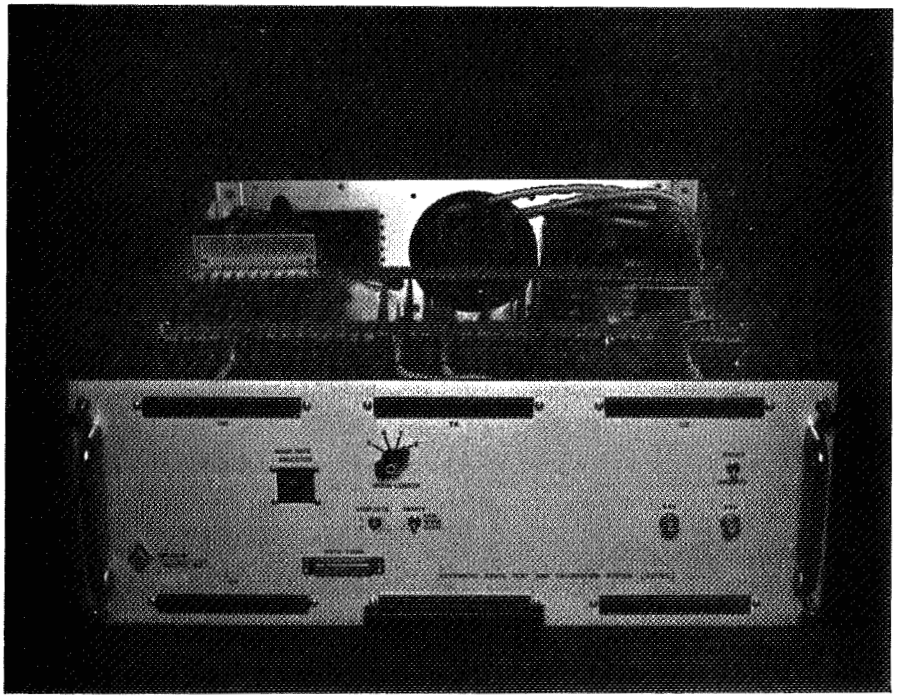

FIGURE 5 - ASTAC INTERFACE UNIT (AIU) CARD CAGE

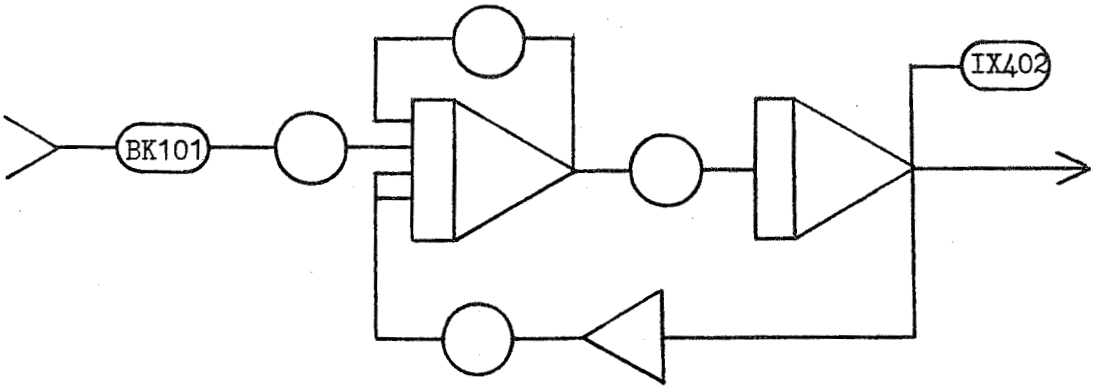

FIGURE 6 - TYPICAL WEST CIRCUIT UTILIZING "BREAK" AND "INTERROGATE" PORTS

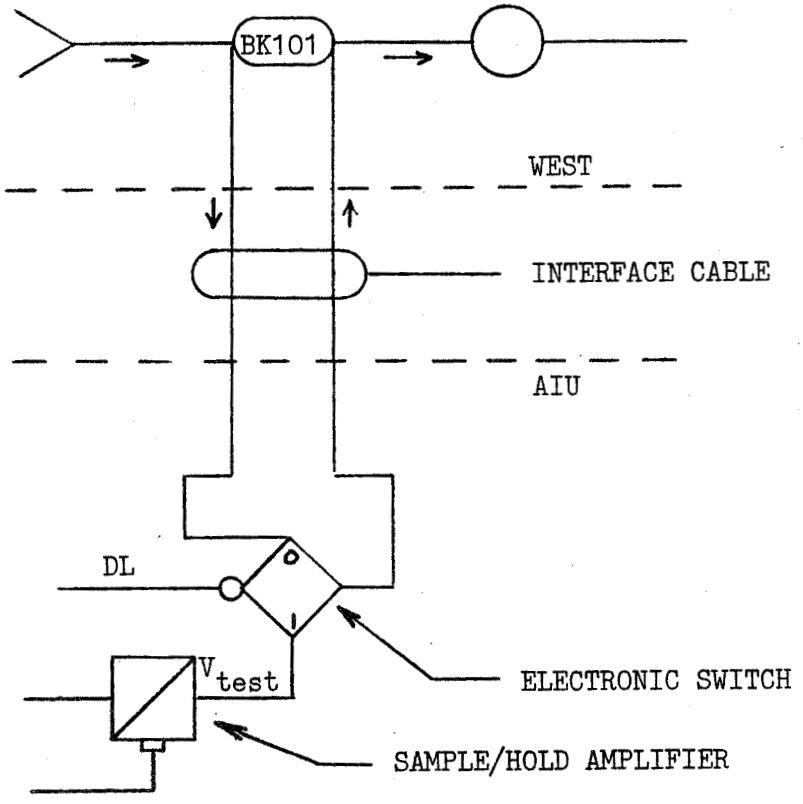

FIGURE 7 - WEST/AIU "BREAK" INTERFACE PORT

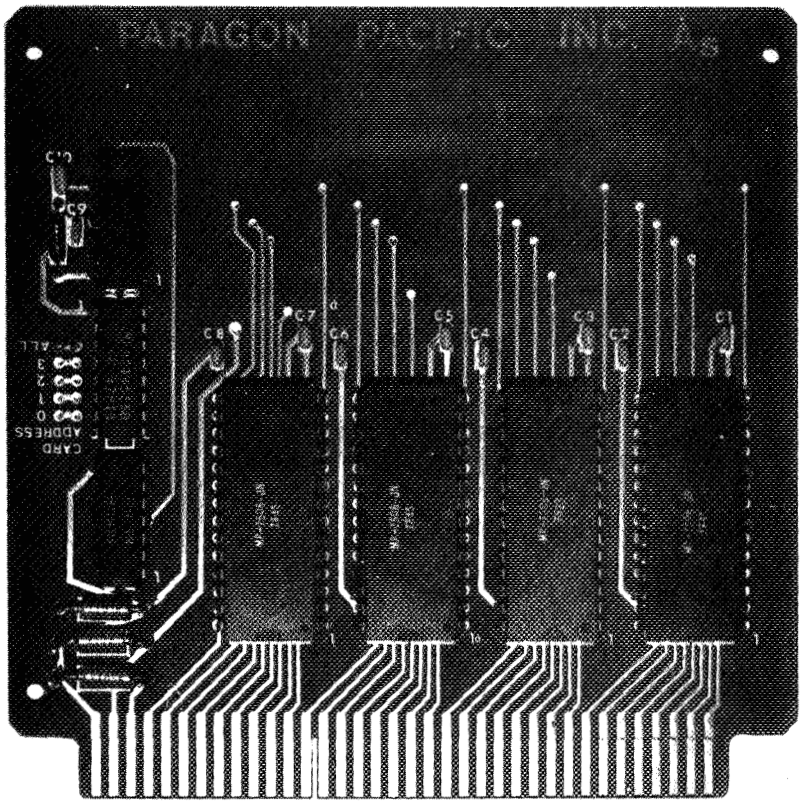

FIGURE 8 - 64 x 1 ANALOG MULTIPLEXER PRINTED CIRCUIT CARD

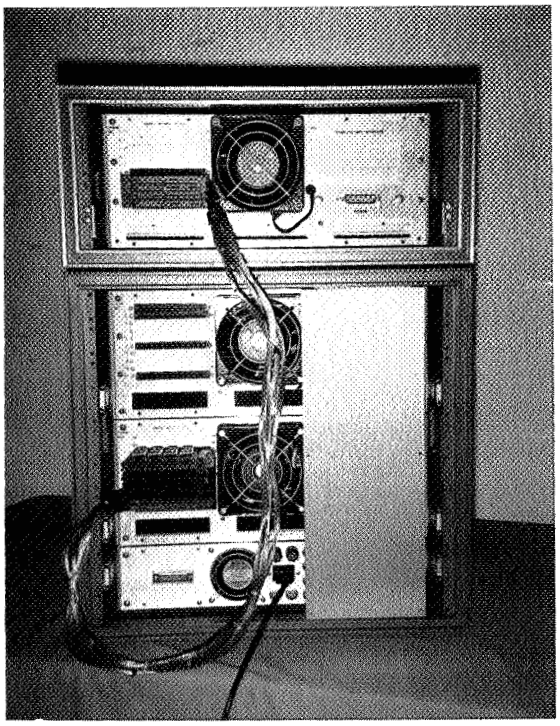

FIGURE 9 - WEST/AIU COMBINATION WITH
INTERFACING CABLES AND MUX CARDS INSTALLED

TEST 0 3003

UN	4062	4050	UC	4541	4619	SNALFA	4052	4015
CSALFA	9072	9158	AVAMOR	-4	87	T33M1	-463	-480

Theoretical Voltage
(Millivolts)

Measured Voltage
(Millivolts)

Signal Name

FIGURE 10 - ASTAC INTERPRETATIONS

TEST	0	3002					
IXMXOD	312	363	IXPS	-1201	-1125	IZE	1176	1181
IXD	209	252	IZD	-307	-257	SNALFA	2807	2765
CSALFA	9536	9610	AVAMOR	1835	1828	IDZPS	-34	29
IDX	-830	-753	T33M1	-415	-431	ALFYD	2124	2154
SNZETA	-2451	-2327	TANTAU	9521	9449	CZTAM1	-327	-274
TAUO	6162	6125	ZETAO	1176	1174	CTAUM1	9091	9010
ZETA	1171	1174	SINTAU	9521	9449	SW05	-6230	-6125
THETA	-1064	-999	SW04	-419	-349	CW04	-10000	-10000
X01	-10000	-9999	X02	7968	7999	X03	5981	5999
X04	3935	3999	X05	1958	1999	X06	-4	0
X07	-1977	-1999	X08	-3964	-3999	X09	-5927	-5999
X10	-7890	-7999	ALFY	-3525	-3443	T13	9521	9449
T11M1	9116	9002	UN	3383	3271	T31	9443	9400
UB	4921	4962	T32	2382	2327	VB	-5947	-5892
WB	-517	-404	UA	-5034	-4999	QA	244	249
RA	-4951	-4899	VA	4941	4999	PA	-429	-374
UC	5644	5683	T21	1464	1425	T23	-2451	-2309

TEST	0	3003					
UN	4062	4050	UC	4541	4619	SNALFA	4052	4015
CSALFA	9072	9158	AVAMOR	-4	87	T33M1	-463	-480
T31	9414	9371	T32	2563	2521	ALFY	-3515	-3443
TAUO	6157	6125	CZTAM1	-380	-323	SNZETA	-2636	-2521
SW05	-6240	-6125	THETA	-1162	-1099	ZETA	1274	1274
X01	-10000	-9999	X02	7958	7999	X03	5976	5999
X04	3925	3999	X05	1953	1999	X06	-9	0
X07	-1982	-1999	X08	-3974	-3999	X09	-5937	-5999
X10	-7900	-7999	ZETAO	1279	1274	SW04	-415	-349
CW04	-10000	-10000	T21	1582	1544	T23	-2626	-2502

TEST	0	3004					
UN	3881	3865	UC	4584	4660	SNALFA	3857	3830
CSALFA	9150	9237	AVAMOR	0	90	T33M1	-415	-431
T31	9443	9400	T32	2368	2327	ALFY	-3515	-3443
TAUO	6152	6125	CZTAM1	-327	-274	SNZETA	-2451	-2327
SW05	-6235	-6125	THETA	-1064	-999	ZETA	1171	1174
X01	-10000	-9999	X02	7968	7999	X03	5981	5999
X04	3935	3999	X05	1958	1999	X06	-9	0
X07	-1982	-1999	X08	-3969	-3999	X09	-5927	-5999
X10	-7900	-7999	ZETAO	1181	1174	SW04	-419	-349
CW04	-10000	-10000	T21	1464	1425	T23	-2441	-2309

FIGURE 11 - WEST ANALYZER ASTAC TEST RESULTS

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15. Supplementary Notes

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16. Abstract

A microcomputer based automatic test system has been developed for the daily performance monitoring of the NASA Lewis Research Center Wind Energy System Time-Domain (WEST) Analyzer. The test system consists of a microprocessor based controller and hybrid interface unit which are used for inputing prescribed test signals (voltages) into all WEST subsystems and for monitoring WEST responses to these signals. Measured performance is compared to theoretically correct performance levels calculated off line on a large general purpose digital computer. Test results are displayed on a cathode ray tube (CRT) or are available in hard copy from a line printer. Excessive drift and/or lack of repeatability of the high speed analog sections within WEST can be easily detected and the malfunctioning hardware identified using this system. In addition, the test system can be used to continuously scan all key signals within WEST and to detect system limiting (e.g., maximum analog voltages have been exceeded) during routine operation of the WEST Analyzer.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
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