NASA-CR-166262

BOEING

XV-15 TILT-ROTOR FLY-BY-WIRE

COLLECTIVE AXIS CONTROL DEMONSTRATOR

DEVELOPMENT SPECIFICATIONS

D210-11819-1

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TABLE OF CONTENTS

LIST OF FIGURES

1.0 INTRODUCTION

This document contains the specifications for an XV-15 Tilt-Rotor Collective Axis Demonstrator. The demonstrator shall be an actual breadboarding of a non-mechanical fly-by-wire Primary Flight Control System (PFCS) for the collective axis. The performance characteristics of the collective axis shall provide typical axis control response data for evaluation. The demonstrator shall be breadboarded as a dual system instead of the triplex system proposed in the Preliminary Development Specification found in Appendix B of document D210-11569-1.

2.0 SYSTEM DEFINITION

The PFCS demonstrator shall provide functional control of the tilt-rotor aircraft collective axis by control of rotor driver actuators and engine N_1 control actuators. The demonstrator shall modify pilot control inputs as a function of nacelle incidence angle and rotor speed. The PFCS shall accept inputs from the SCAS for aircraft stability and maneuverability enhancement. The demonstrator shall contain control and display functions to fully demonstrate performance characteristics. PFCS and SCAS computation functions shall be performed in a single flight control processor.

3.0 DESIGN AND CONSTRUCTION

The design shall be constrained to the collective axis to demonstrate the performance and accuracy of the PFCS. The demonstrator shall be constructed as a dual system from commercially available parts including single board computers, analog-to-digital converters, and power supplies. The demonstrator shall be totally self-contained avoiding external connections and hydraulic supplies except as modified herein.

4.0 PFCS DEMONSTRATOR DESCRIPTION

Pilot inputs shall be via mechanical control levers comprising lateral stick control, engine condition lever, and engine throttle control. Signals proportional to control position shall be conditioned in the Flight Control Processor (FCP) to generate commands for the rotor control driver actuators and engine N_1 control actuators.

4.1 System Functions

Major system functions shall be as shown in Figure 4.1 and described in the following paragraphs.

a. Motion Sensing - The control position transducers shall convert lever motions to equivalent electrical signals for input to the Flight Control Processor.

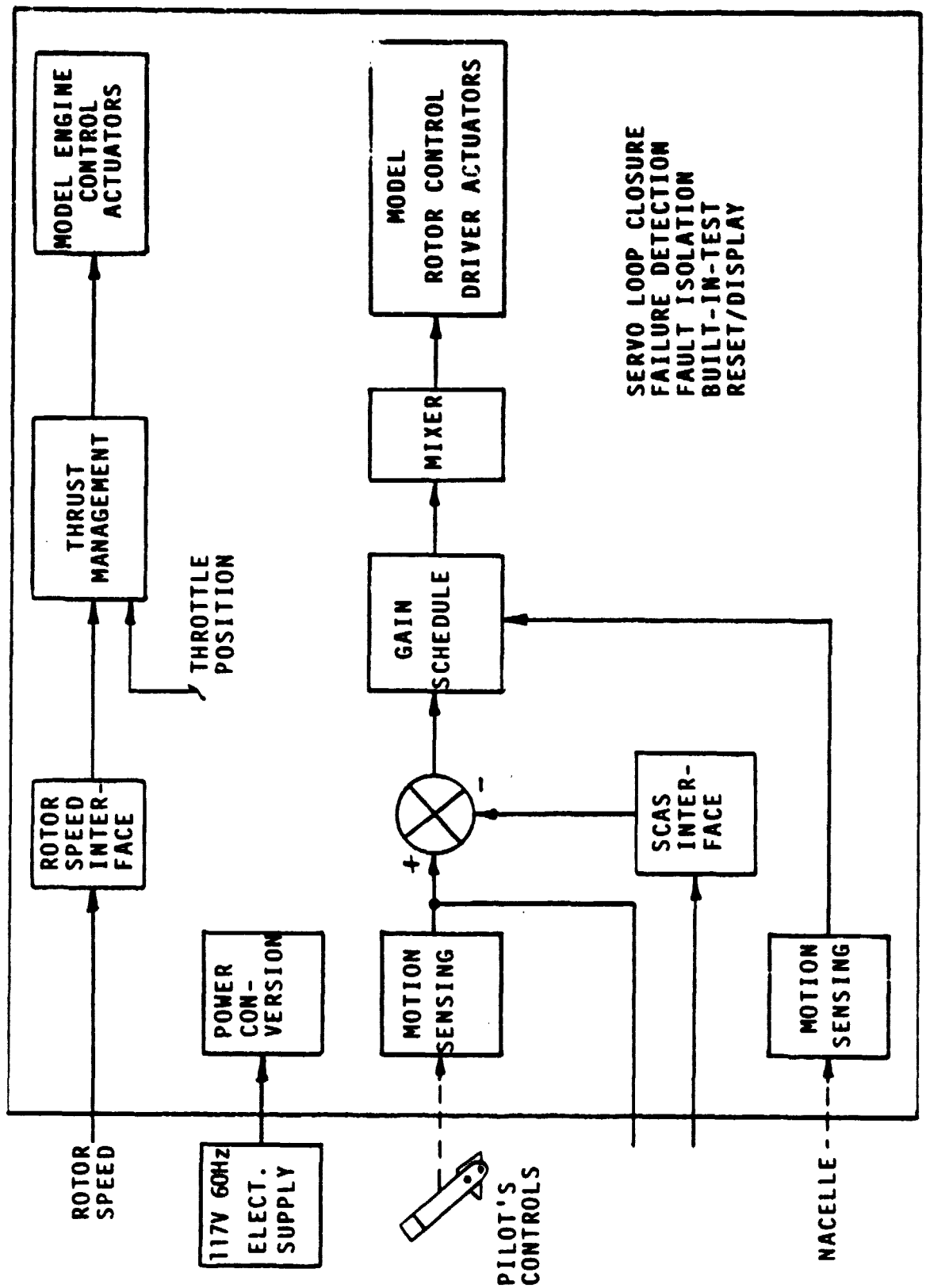


FIGURE 4.1. Primary Flight Control System Functions

b. SCAS Interface - The PFCS shall accept SCAS commands from the SCAS via authority and rate-limit functions. The limited signals shall be summed with the control position signals before mixing.

c. Gain Scheduling - Collective axis command signals (summation of pilot control and SCAS command) shall be scheduled as a function of nacelle angle. In general, pilot inputs to the rotor shall be phased out as nacelle is brought to the horizontal position (zero degrees).

d. Thrust Management - Shall provide for control of rotor collective pitch and engine N_1 controls. The system shall respond to pilot throttle setting and rotor rpm. Direct pilot control of collective pitch shall be phased out at zero degrees nacelle incidence. Manual trim of rotor rpm and differential collective pitch shall be provided on the system control panel.

e. Mixing - The scheduled axis commands and governor outputs shall be mixed using appropriate gains to position the rotor control actuators.

f. Servo Loop Closure - Shall include the electronics to control rotor driver actuators.

g. Power Conversion - Shall convert 117 volt 60 Hz AC supply to AC for sensor excitation and DC supplies as required to operate electronic devices used in the system.

h. Failure Detection - Each flight control processor shall process all failure detection within its channel and, upon detecting a failure, shall shut down the channel inputs to the affected actuators and transmit failure information to the control panel and maintenance unit.

4.2 Major Component Responsibilities

The following is a regrouping of PFCS demonstrator functions by major component.

a. Control Position Transducers

- Motion Sensing

b. Flight Control Processor

- Signal Conditioning and Buffering
- SCAS Computation and Interface
- Gain Scheduling
- Thrust Management

- Mixing
- Servo Loop Closure
- Power Conversion
- Failure Detection

c. Rotor Actuator

- Rotor Control Driver Actuator
- Electronic Model Actuator

d. Control Panel

- Engine Throttle Control
- Lateral CPT
- Engine Condition
- SCAS Mode Select/Display

e. Display Panel

- Fault Reset
- Manual Nacelle Incidence Angle Control
- Manual RPM Control
- Manual Torque Matching (Differential Collective Pitch)
- Fault Isolation Display
- Patchable Digital-to-Analog Conversions

- Built-in-Test Control - Fault Display

4.3 External Interfaces

The PFCS demonstrator shall be designed to operate independent of external equipment. Control functions shall be performed on electronic model actuators to simulate XV-15 Tilt-Rotor collective axis features. The following equipment shall be interfaced at the Boeing Vertol facility for demonstration only.

a) Rotor Driver Actuators - This is an electrical interface with servo valves and linear position transducers.

b) Hydraulic Power Supply - This is a mechanical interface with the rotor driver actuators.

4.4 Redundancy Management

The demonstration system shall be configured with the following levels of redundancy:

1. Sensors (electrical link), PFCS signal processing, and PFCS electro-optical interconnect lines: Single-fail operative.

2. Hydromechanical portions of the actuators and hydraulic lines to actuators: Single-fail operative.

3. Electrical power supply: Single-fail operative.

4. Hydraulic power supply: Dual.

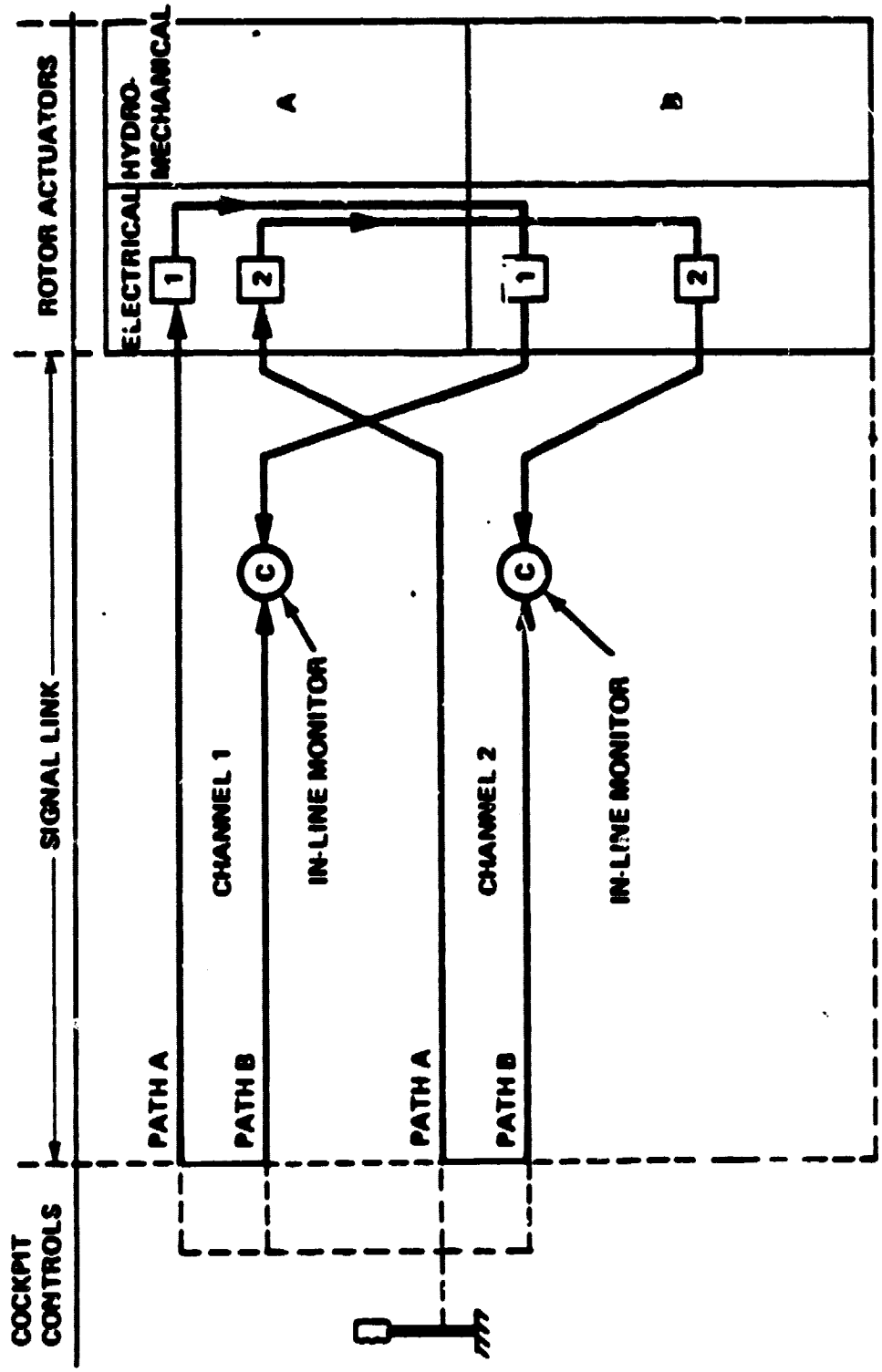
5. Mechanical portions of PFCS sensors: Single-fail operative checked in a background inter-channel comparison.

4.4.1 Overall System

The in-line (self) monitored concept of redundancy management used for the primary system involves the use of two identical signal paths in each channel between the cockpit controls and the actuator input (Figure 4.2). If a discrepancy occurs that is greater than a preestablished tolerance level, that channel is considered to have failed and is shut down. The electro-hydraulic actuators have dual hydraulic sections and dual electrical sections. Each channel of the electrical link is powered by an independent electrical supply. Channel inputs are summed magnetically in the electro-hydraulic valves of the actuator. The following sections discuss detailed methods used in each major portion of the system.

4.4.2 Position Transducers

Pilots input and actuator position feedback are measured by Linear Variable Differential Transducers (LVDT) which are self monitored and applied to each processor sub path.



4.2 REDUNDANCY MANAGEMENT CONCEPT

4.4.3 Signal Path Monitor

Figure 4.3 shows the mechanization of the signal path comparator. This comparison is made in two steps. The outputs of Path A and B digital-to-analog converters are compared to detect failures in the sensors and electronics. After comparison, the signals are averaged in the servo-amplifiers. This removes any accumulated error due to tolerance stackup from the next stage of comparison.

Electrohydraulic valve currents of each actuator section are compared with a third servo amplifier, which drives an EHV torque motor model. This comparison allows detection of failures in the servo amplifier, actuator wiring, or EHV torque motor coil. The model EHV torque motor is used to prevent shutdown of both actuator sections, should one EHV suffer a ballistic hit, by providing an independent third voting reference.

4.4.4 Control Stage Hydromechanical Failures

Failures downstream of the EHV coil are detected by comparison of valve current with the control stage piston position. The unbalanced control stage design eliminates the passive failure modes, which can require a special test excitation to assure detection. An unbalanced pressure must be maintained to hold the piston in equilibrium.

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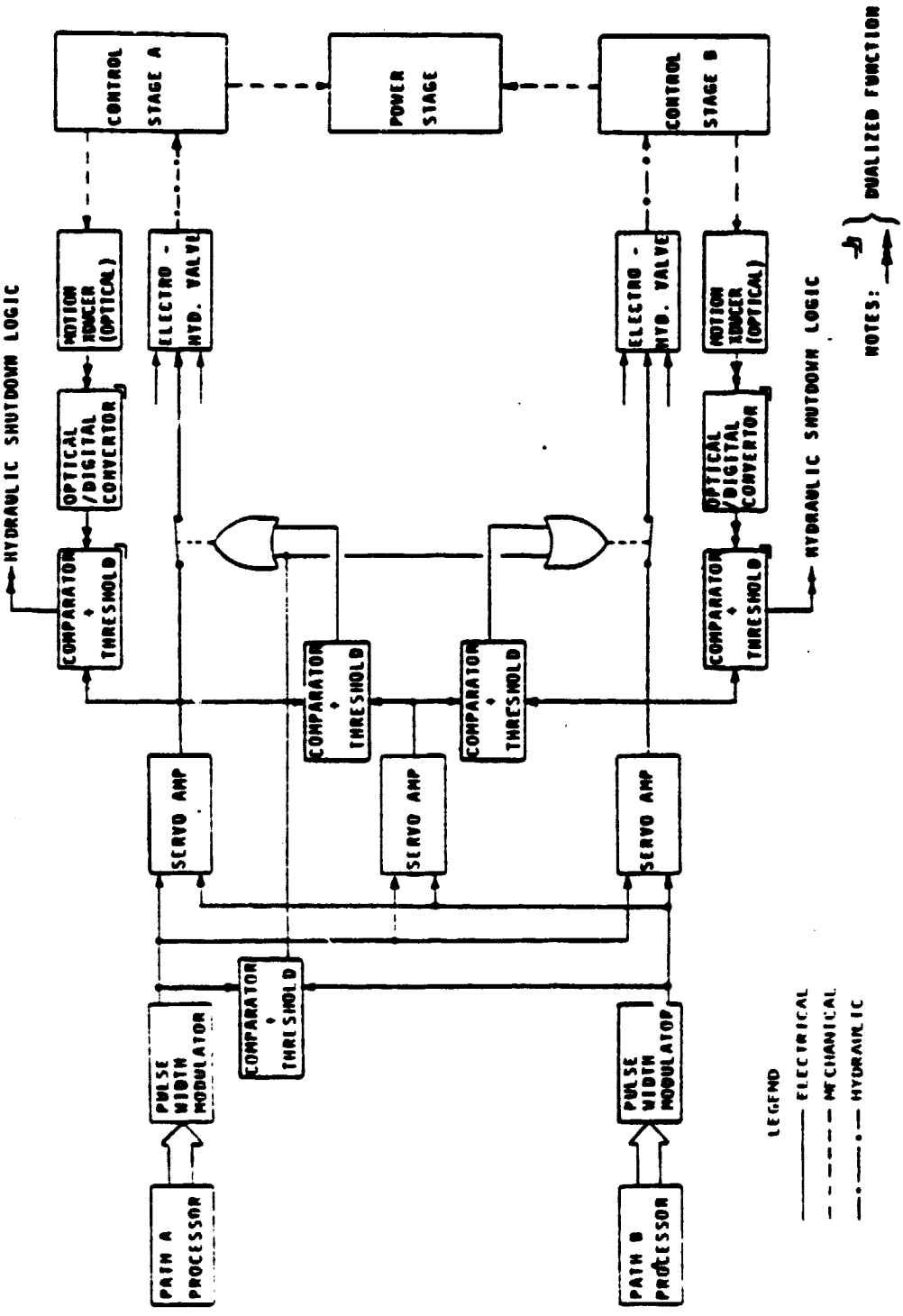
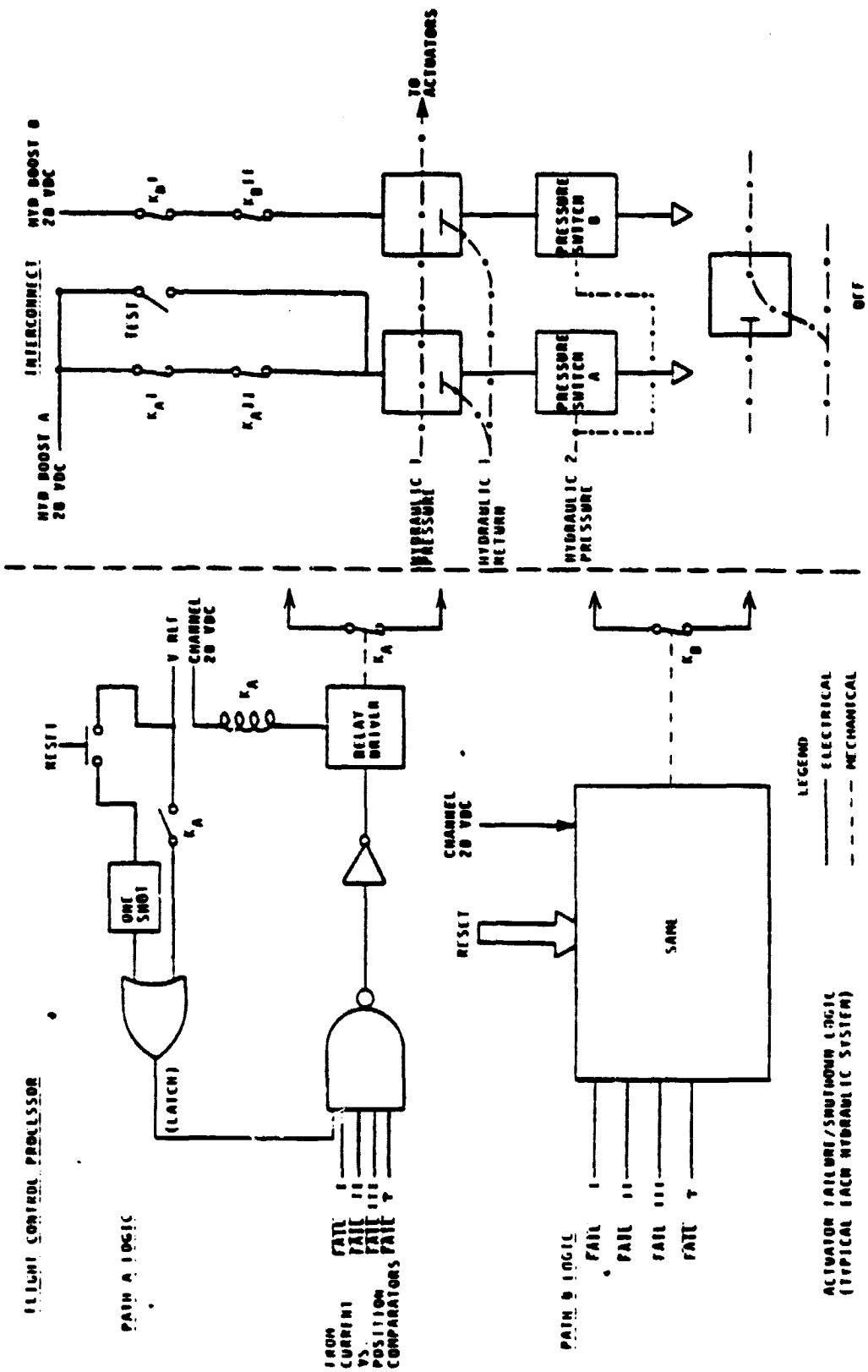


4.3 BASELINE ROTOR ACTUATOR REDUNDANCY MANAGEMENT

Detection of all failures in the control stage is made by comparison of piston position and input current. When a hardover failure occurs, it is opposed by the other channel, resulting in collapse of the anti-jam override spring capsules. Under this condition, control of the power stage is lost until the failed actuator is shut off. With both spring capsules collapsed, there will be a slow rate displacement of the power stage valve because power stage valve offset is limited to that allowed by neutral rigging tolerances.

The current versus displacement comparators (Figure 4.3) for all actuators are "ORED" to control the hydraulic system shutoff valve (Figure 4.4). When the system is reset the contacts of relays K_A and K_B are held open. Both path processors monitor for failures and control individual shutoff valves. When two channels agree on a failure, power is applied to the valves. When either valve is energized and pressure is shut down, control of the actuator is restored. The delay is of the order of 50 milliseconds.

Failures that result in a control stage jam, particularly near center, will present a slightly different detection problem. For this case, the comparator output will be accumulated over a period of time after which hydraulics would be shut down and pilot notified.



4.4 ACTUATOR FAILURE/SHUTDOWN LOGIC (TYPICAL EACH HYDRAULIC SYSTEM)

5.0 SYSTEM CHARACTERISTICS

5.1 System Performance

5.1.1 Gains, Schedules, Transfer Functions - Shall be as defined in Figure 5.1.

5.1.2 Accuracy - The demonstrator shall include the following requirements relating to system accuracy.

a. Static Gain Accuracy - The average gain for all FCP units shall be within 2% of the values specified. The static gain of individual FCP units shall be within 1.5% of the average. For a given control input the accuracy is defined as the percent difference between the desired and actual actuator position.

b. System Null - The total steady state null associated with the PFCS (sensor to driver actuator) shall not exceed 0.4% of actuator full stroke.

c. Resolution - Resolution is defined as the minimum change in control required to obtain actuator motion. The resolution (equated in actuator motion) shall not exceed 0.04% of actuator full stroke.

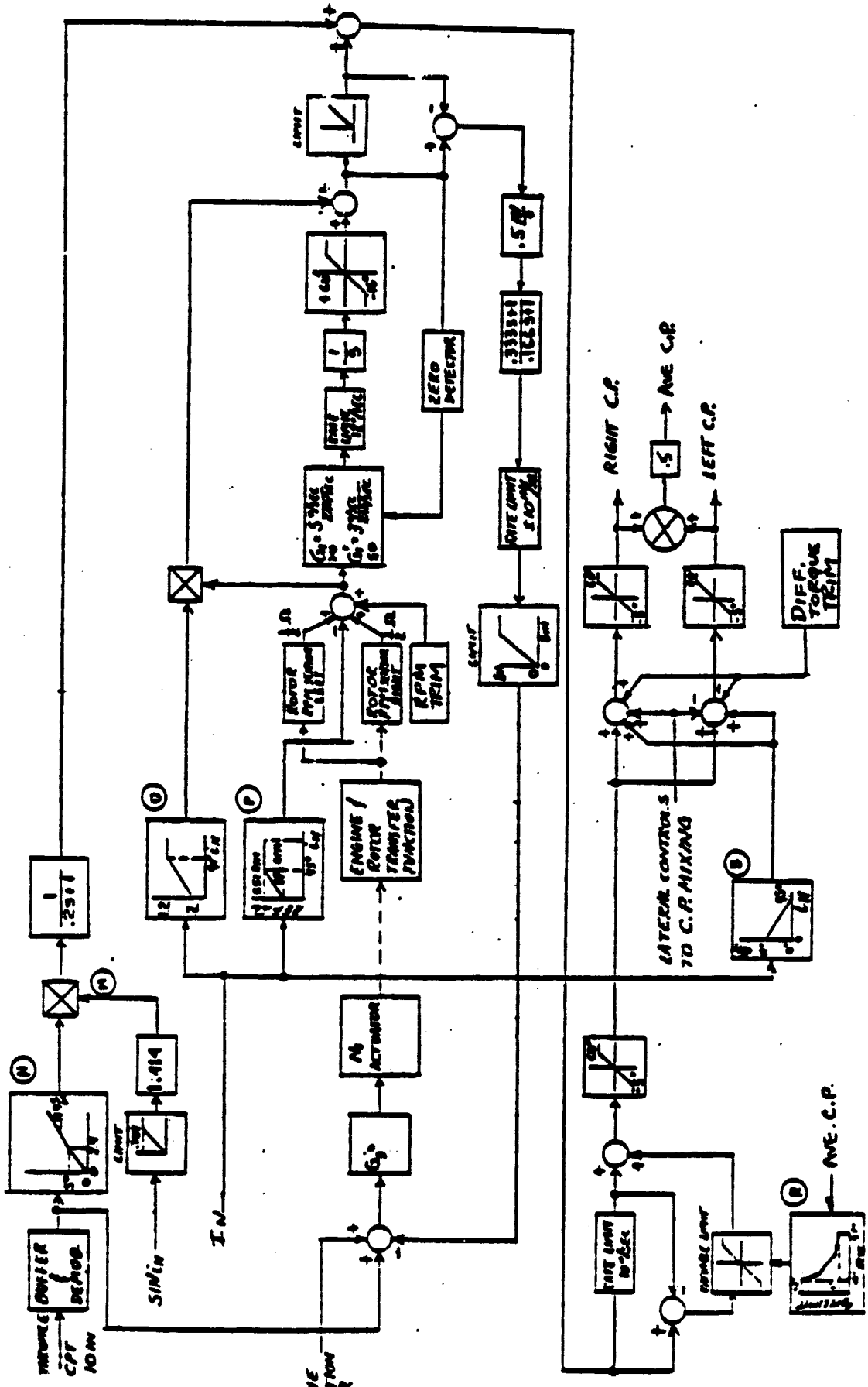


FIGURE 5.1. THRUST MANAGEMENT SYSTEM

d. System Hysteresis - Hysteresis within the PFCS shall not exceed 0.08% of actuator full stroke.

5.1.3 Driver Actuator Frequency Response - The driver actuator shall exhibit a second order response with a natural frequency of 130 rad/sec and damping factor of 0.7. This response shall be achieved while driving a friction load of 50 pounds.

5.1.4 Electronic Model Actuator - The model actuator shall exhibit the same response characteristics as the driver actuator defined in paragraph 5.1.3.

5.1.5 Failure Detection and Effects - The demonstrator PFCS shall include the following requirements relating to system failures and effects.

a. Failure Detection and Isolation - Operation of the redundant channels shall be monitored to detect any failure or malfunction. After the detection of a failure, the failed channel shall be automatically inhibited from affecting the correctly operating channel.

b. Failure Detection Threshold - The failure detection threshold must be set low enough to detect passive failures with normal system disturbances, detect valid failures, and minimize failure transients.

The threshold must be high enough to minimize nuisance trips due to normal channel tolerances and transients.

c. Monitoring Circuitry - The detection, logic, and switching circuitry reliability shall be included in the channel reliability requirements. The failure or malfunction of the logic and switching circuitry shall be interpreted as a channel failure.

5.2 System Physical Characteristics

5.2.1 Control Levers - The demonstrator control input levers shall be constructed from sheet metal and connected through mechanical interfaces to electrical position transducers.

5.2.2 System Packaging - The demonstrator PFCS components shall be packaged in a 19-inch rack assembly as sketched in Figure 5.2 such that each channel is separately contained. System control and display panels are an exception to this requirement.

5.3 Environmental Conditions

The following environment shall be used to establish normal performance characteristics under standard conditions for making laboratory bench tests.

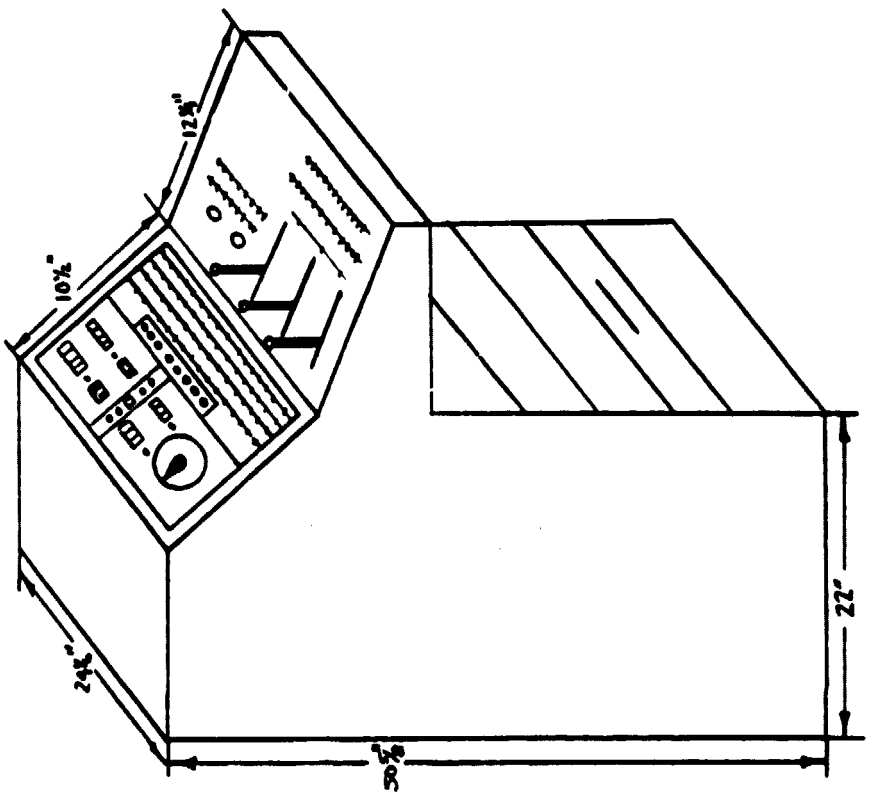


FIGURE 5.2. Demonstrator Packaging

a. Temperature - room ambient 25° ± 5°C (77° ± 9°F)

b. Altitude - normal ground

c. Humidity - room ambient up to 90% relative humidity

6.0 MAJOR COMPONENT CHARACTERISTICS AND REQUIREMENTS

The demonstrator shall be designed to implement all pilot input signals with display and maintenance features required for a dual system configuration.

6.1 Subsystem Description

The PFCS demonstrator shall be comprised of the following units:

Flight Control Processor	2 per demonstrator
Control Panel	1 per demonstrator
Display Panel	1 per demonstrator
Control Position Transducers	3 per channel

6.1.1 Flight Control Processor (FCP) - The FCP shall be configured with miltiple Single Board Computers (SBCs) as shown in Figure 6.1. The architecture shall be such that the Intel 86/12A board configured in Figure 6.2 operates in parallel with the Intel 80/04 board configured in Figure 6.3.

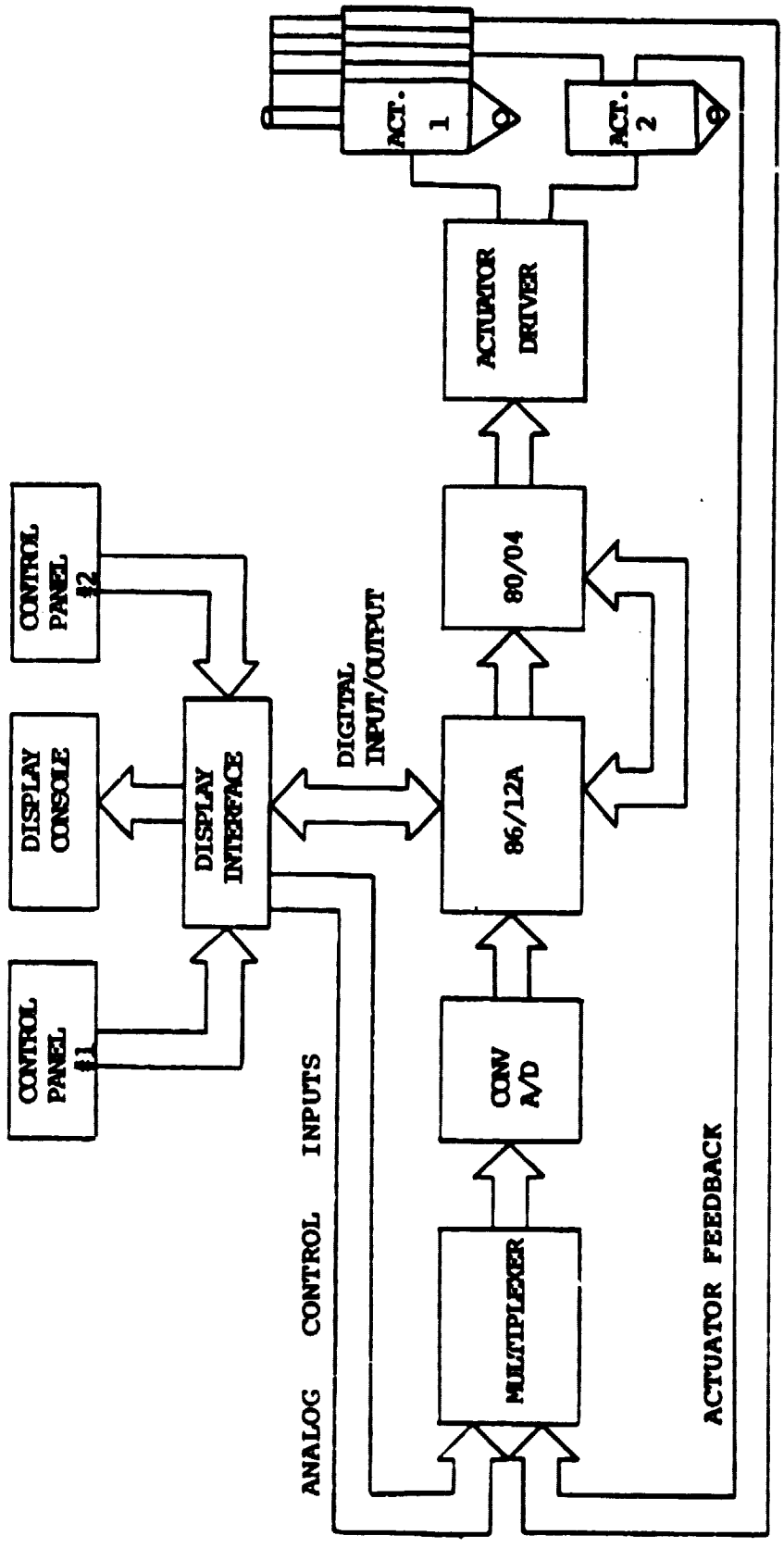


FIGURE 6.1. System Block Diagram

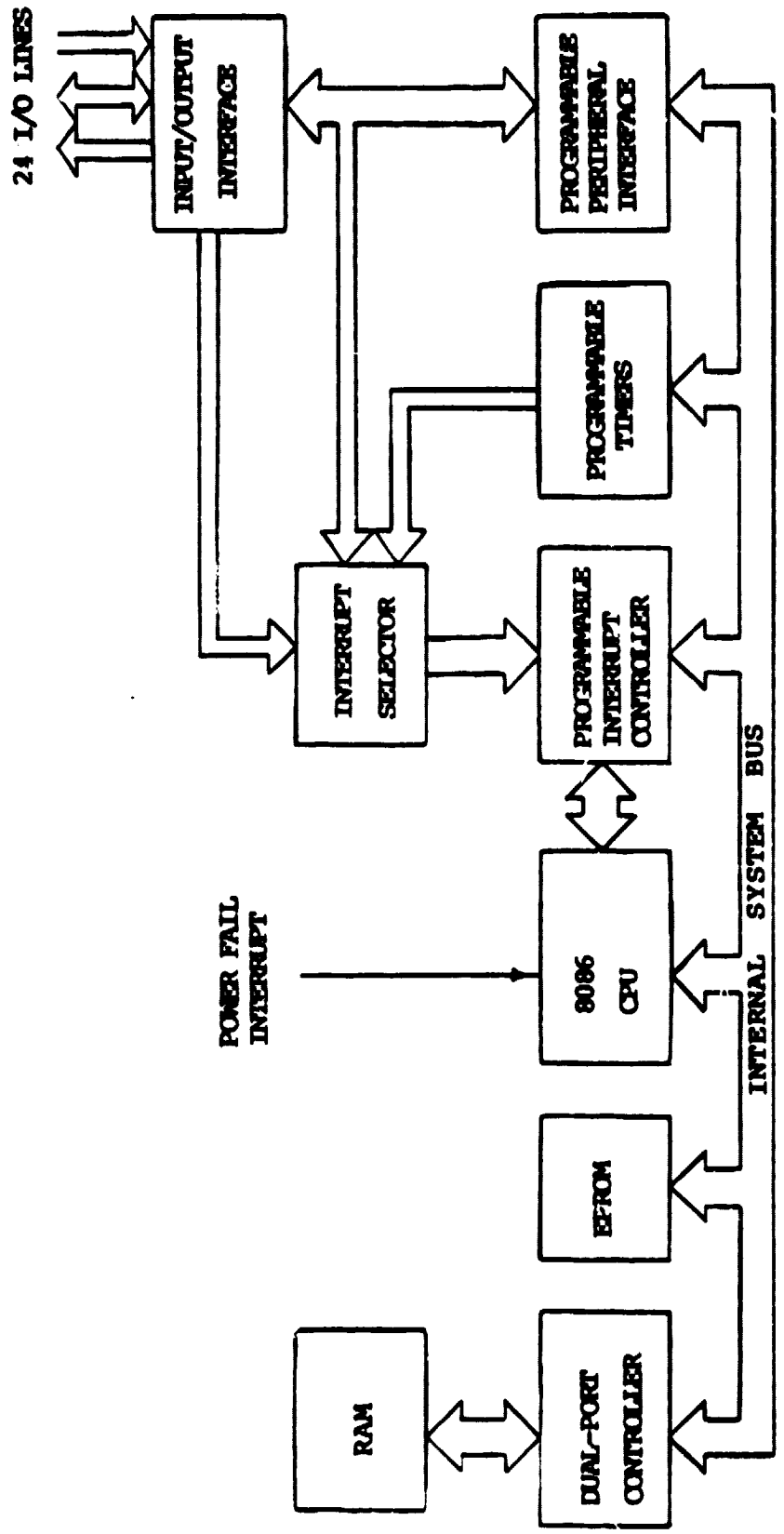


FIGURE 6.2. 8086 Configuration

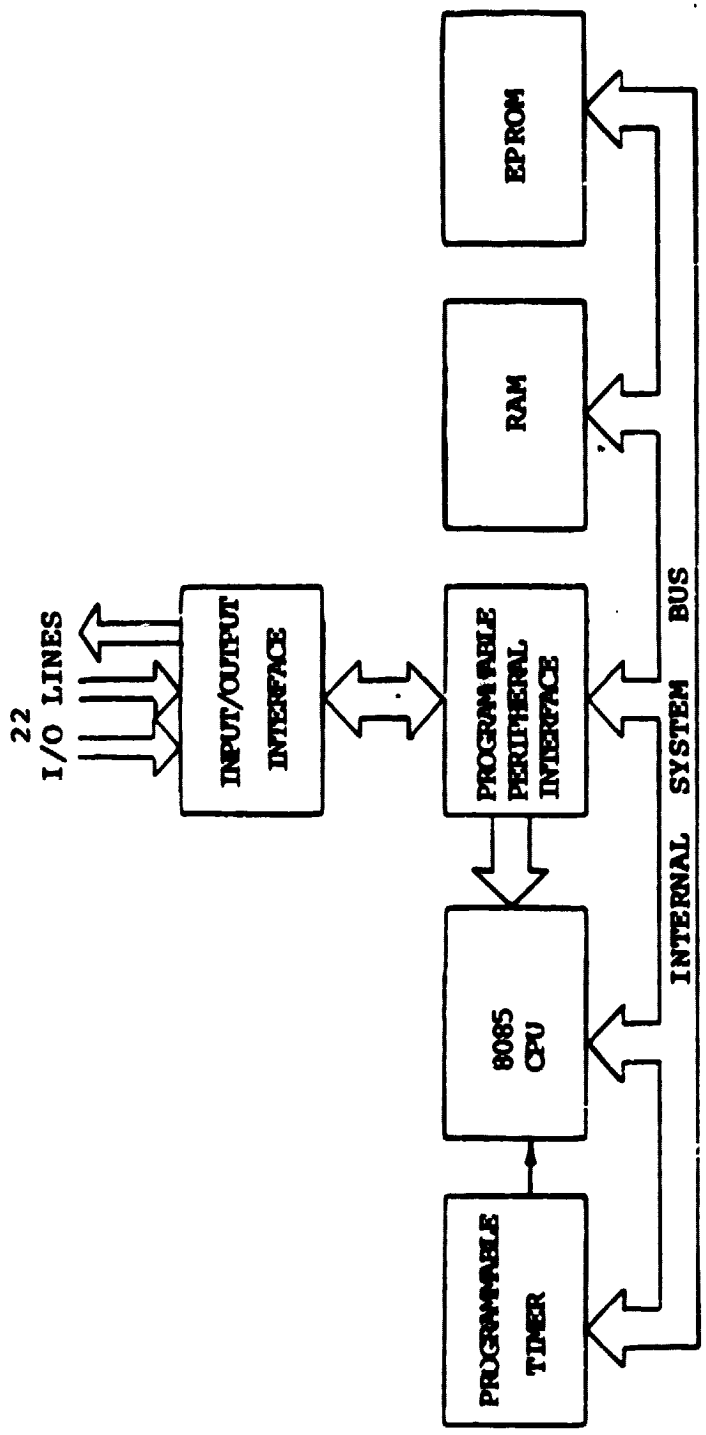


FIGURE 6.3. 8085 Configuration

a. Intel 86/12A Board - The 16-bit single board computer using a 5 MHz 8086 microprocessor shall execute controls to sample and process pilot control inputs. Signals shall be processed through the required flight control laws for collective axis control including mixing and limiting. The computed actuator outputs shall be sent via a 7-bit parallel port to the output processor.

b. Intel 80/04 Board - The 8-bit single board computer using a 3 MHz 8085 microprocessor shall convert each actuator output from the 7-bit parallel format to a serial pulse stream.

c. 8086-8085 Interface - Communication between the control and output processors shall be conducted through parallel Input/Output (I/O) ports. Bus I/O interfaces shall be supplied as required.

6.1.2 Control Panel - The control panel shall provide lateral control position, engine throttle control, engine condition and SCAS inputs.

6.1.3 Display Panel - The display panel as illustrated in Figure 6.4 shall provide nacelle incidence angle, rpm trim, differential torque trim, fault annunciation, patchable Digital-to-Analog Conversion (DAC), Built-In-Test-Equipment (BITE), and reset capa-

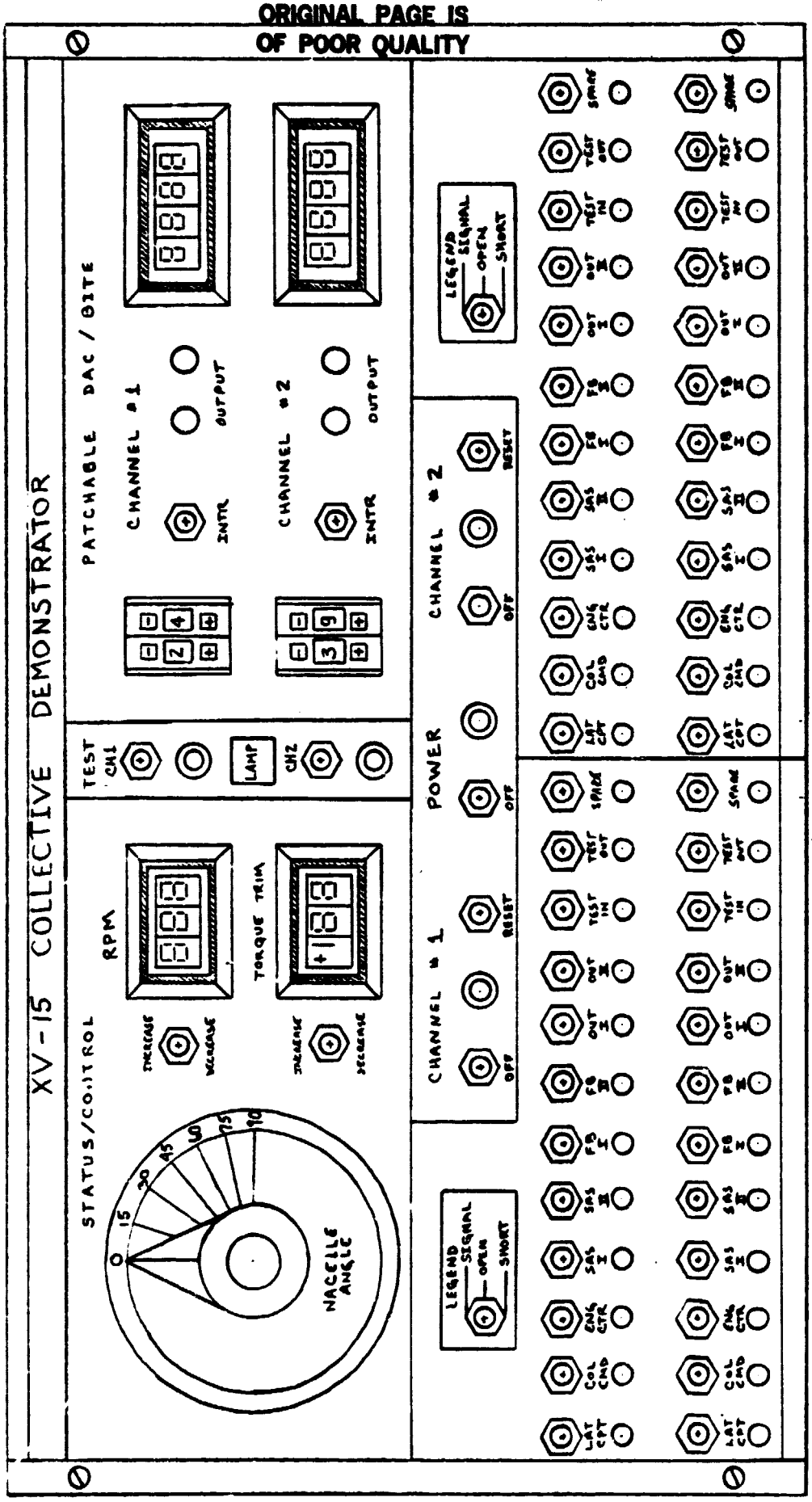


FIGURE 6.4. Display Panel

bility. The following functions shall be provided in conjunction with the patchable DAC and BITE.

- o Determine the operable channel within the system.
- o Provide logic to drive control panel.
- o Conduct GO/NO-GO ground tests on each channel.
- o Provide readouts to indicate location of system failure to assist in isolation of faults to a line replaceable unit.

6.1.4 Control Position Transducers - The control position transducers (CPTs) shall translate pilot control motions into equivalent electrical signals which are in turn transmitted to the processors.

6.1.5 Electrical Interconnecting Cables - The electrical interconnecting cable assemblies shall be fabricated utilizing simple multi-conductor flat ribbon-cable, wire-wrap wires, commercial connectors, and appropriate strain relief. The system configuration shall be designed such as to use point-to-point cables to the extent possible.

6.2 Display Interfaces

6.2.1 Rotor Speed - Rotor speed shall be provided as an 8-bit digital word. The display interface shall be as depicted in

Figure 6.5. A manual trim control shall be used to change rpm at a rate of 20 rpm/sec. Microprocessor control of rpm display shall be accomplished by a single path selected by the channel select logic.

6.2.2 Nacelle Incidence - The nacelle incidence sensor shall be a synchro excited from the control unit internal A/C supply and providing an output proportional to the sine of the nacelle incidence angle.

6.2.3 Differential Torque - As shown in Figure 6.6 manual control of differential collective pitch trim shall be provided as an 8-bit read-only-display and indicate percent of full scale.

6.2.4 Patchable DAC/BITE - The patchable DAC/BITE interface shall be as shown in Figure 6.7. The multi-functional display shall contain a bus structure which allows any processor path to be displayed on either display. Binary Coded Decimal (BCD) switches shall select which function is to be displayed.

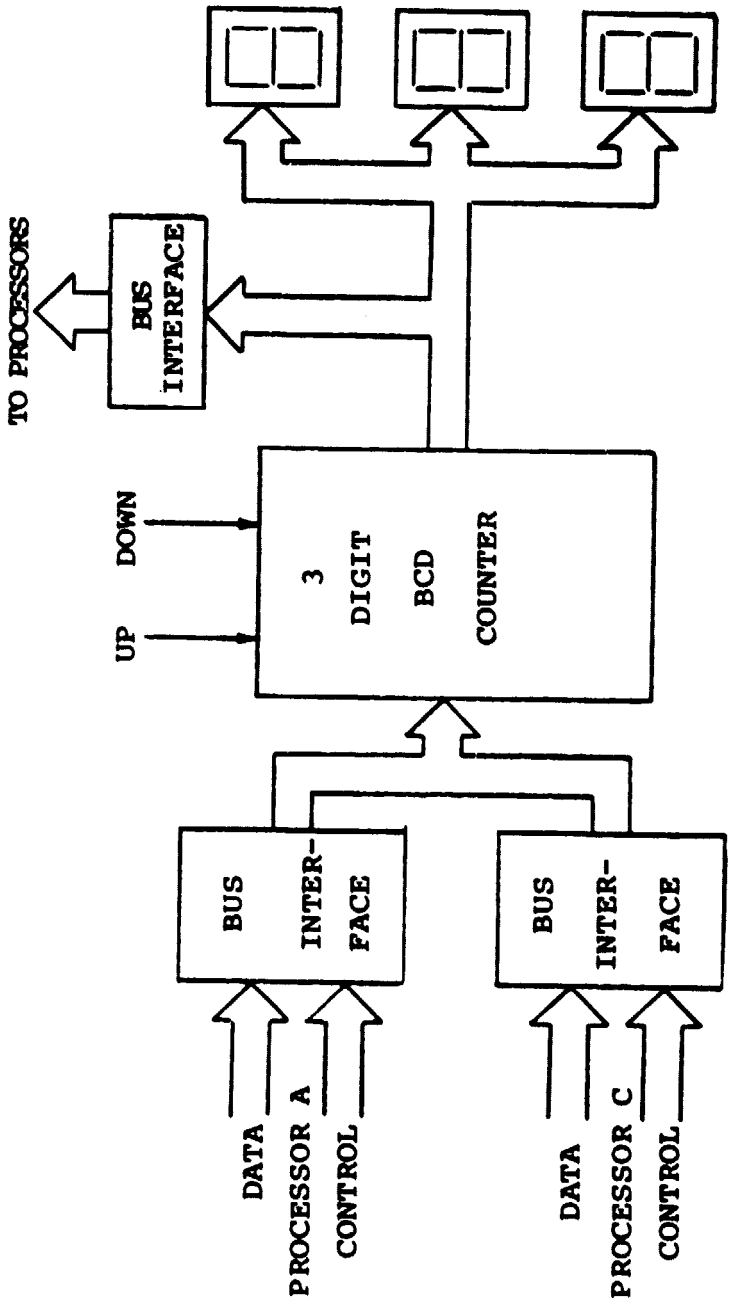


FIGURE 6.5. RPM Display Interface

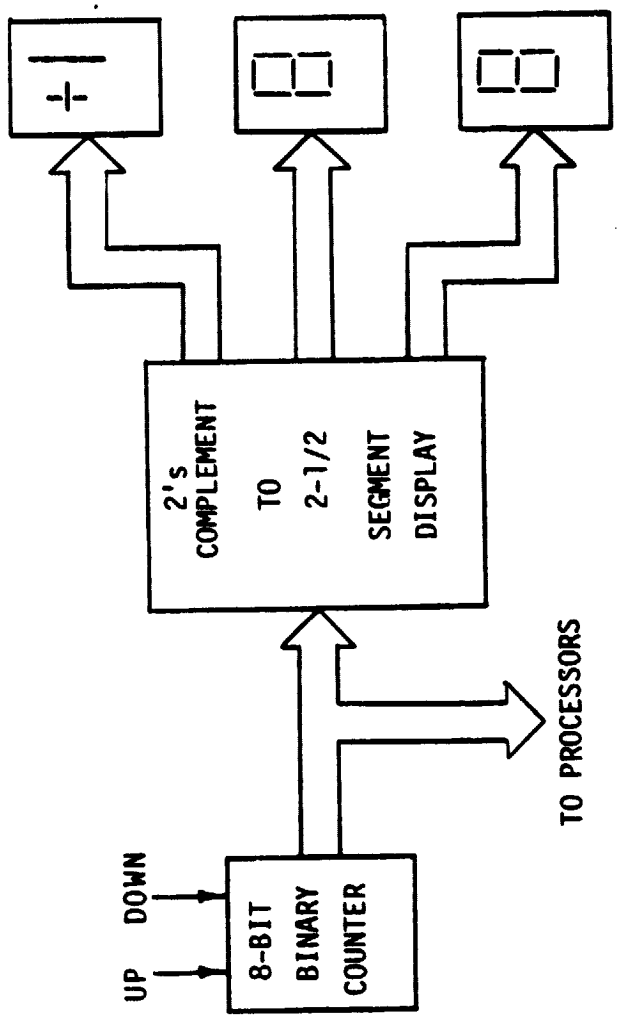


FIGURE 6.6. Differential Torque Interface

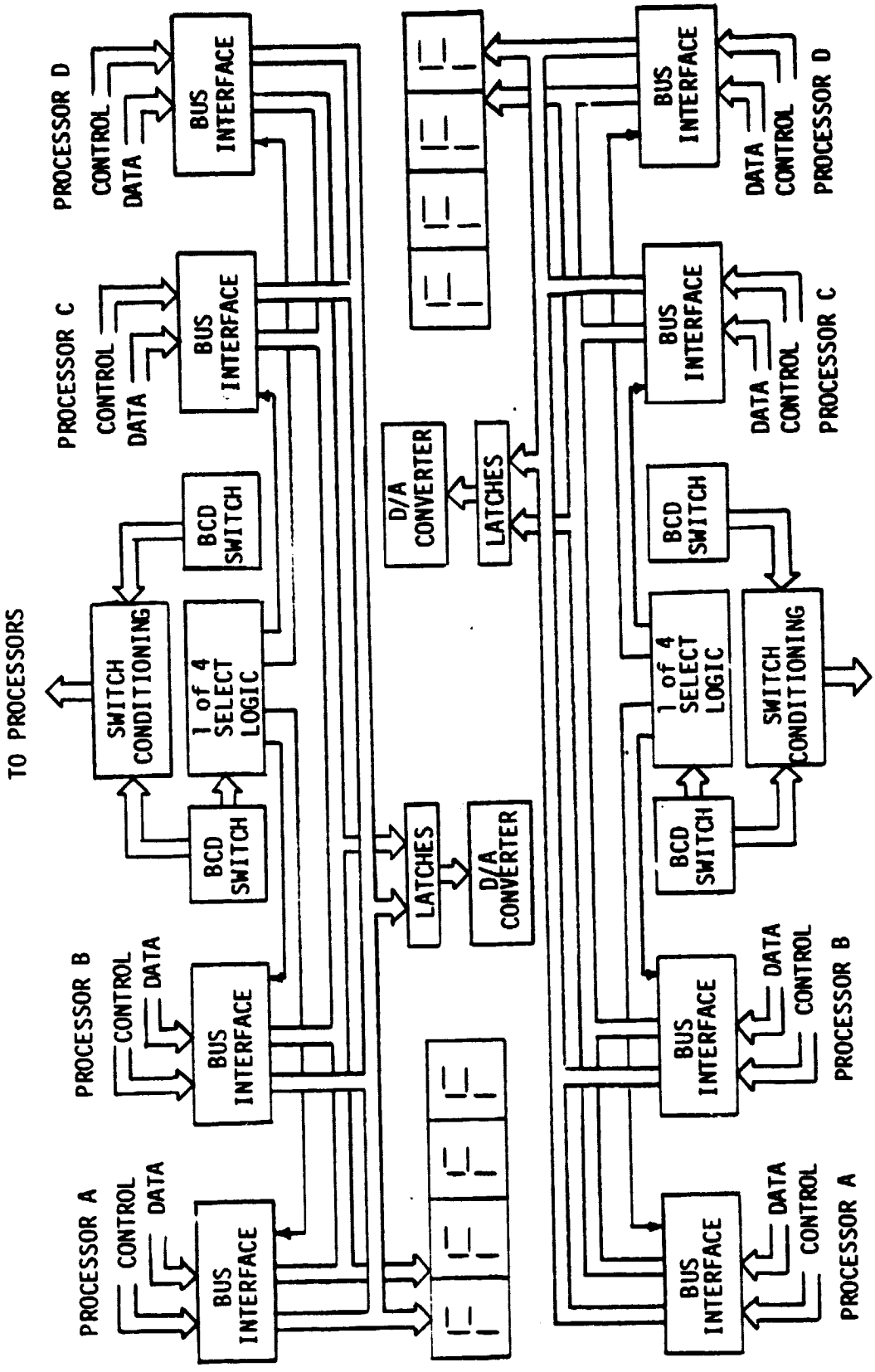


FIGURE 6.7. Patchable DAC/BITE Interface