MONOLITHICALLY INTEGRATED ACTIVE OPTICAL DEVICES*

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SUMMARY

We discuss considerations relevant to the monolithic integration of optical detectors, lasers, and modulators with high-speed amplifiers. Some design considerations for representative subsystems in the GaAs-AlGaAs and GaInAs-InP materials systems are described. Results of a detailed numerical design of an electro-optical birefringent filter for monolithic integration with a laser diode is described, and early experimental results on monolithic integration of broadband MESFET amplifiers with photoconductive detectors are reported.

INTRODUCTION

A number of workers have been involved in the monolithic integration of detectors and lasers with amplifiers for applications in optical communication.[1] The work reported here is specifically aimed at circuits and subsystems suitable for use in very-high data rate applications. The OPFET class of photoconductive detectors in III-V compounds shows picosecond response time coupled with internal gain and low noise. In order to realize the potential of these detectors in a practical system, monolithic integration with high-speed, low-noise preamplifiers is probably a necessity. In addition, there is a need for integration of laser diodes with high-speed amplifiers in order that complete opto-electronic systems can be constructed.

Frequency tunable lasers are useful for FM communication, for frequency multiplexed systems, and offer outstanding potential for very-high data rate transmission.[2] These may be constructed by suitable combinations of gain, birefringent and electro-optical components in the laser cavity.[3,4]

Two materials systems seem especially attractive for monolithic integration of opto-electronic subsystems. They are the GaAs-AlGaAs and GaInAs-InP heterostructure systems. The first system is useful because well-characterized opto-electronic components and amplifiers have been constructed in this system, and much is known about the materials problems which must be overcome to construct successful subsystems. The GaInAs-InP heterostructure system, lattice-matched to InP substrates, is interesting because of its potential application for longer wavelength communications, where optical fibers show minimum dispersion. A further reason for interest in this system is the very high electron saturation

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velocity, which was shown to be the greatest for any of the GaInAsP quaternaries grown lattice-matched to InP. In previous work we showed that the electron saturation velocity in GaInAs is nearly double that of GaAs for comparable carrier densities at room temperature.[5] This enables one to construct photoconductive detectors with higher internal gain, and transistors with higher G_m and speed in the GaInAs system than in the conventional GaAs system. A drawback to the GaInAs-InP system is that unsolved materials problems must be overcome to construct successful monolithic opto-electronic circuits, and the individual devices are much less developed in this materials system, particularly the transistor technology.

SOME DESIGN CONSIDERATIONS FOR MONOLITHIC OPTO-ELECTRONIC SUBSYSTEMS

Monolithic integration of optical and amplifying devices requires semi-insulating substrates if the well-developed MESFET technology is to be utilized for amplifiers. Such substrates are readily available in both GaAs and InP; however, problems immediately arise for MESFET type transistors on InP substrates. From initial considerations, it might seem that a simple GaInAs, InP heterostructure interface would be useful for both optical and electrical confinement, and would be suitable for construction of MESFETs. One of the problems with such interfaces grown by MBE is shown in Fig. 1,[6] where it is seen that in an abrupt GaInAs-InP interface substantial leakage currents can flow which prevent construction of good transistors. In these MBE grown layers the interfacial currents were linked with the growth process for the interface, which may result in an InAsP interfacial layer with poor electrical characteristics. These problems were initially solved by incorporating Al into the system to provide an AlInAs interfacial layer between the GaInAs active region and the InP substrate.

While this approach solved problems with leakage current in transistors, it raises further problems for laser diodes. A schematic diagram of a proposed heterostructure system for monolithically integrated opto-electronic circuits on indium phosphide substrates is shown in Fig. 2. The structure indicated schematically there has the potential for producing good transistors for amplifiers, good optical detectors, and good lasers. The requirements for OPFET type detectors are similar to those of the MESFETs, which are that one be able to construct low-leakage Schottky barrier gates on active layers which are thin enough to be pinched off at a reasonable voltage, and that the structure show no excessive leakage currents through interfaces. The structure shown in Figure 2 meets these requirements. The AlInAs layer under the gate serves to make a good Schottky barrier as was previously demonstrated.[7] Fig. 2 is schematic in the sense that details of the ohmic contacts and Schottky barriers are not shown. Under the contacts, the undoped upper layers must either be removed, doped, or consumed in the contact alloying process. There are various approaches for doing these steps, the details of which are not discussed here. The requirement for pinching off the active FET layer at a reasonable gate voltage means that the thickness of the layer must be 0.2 microns or below for a doping of $10^{17}cm^{-3}$, or that the doping must be reduced for thicker active layers.

The AlInAs layer between the substrate and active layer serves to reduce the leakage currents in the transistor to reasonable values. It also serves to provide excellent carrier and optical mode confinement for the laser structure. One advantage of this material system for the TJS laser structure shown is that the cladding layers can be easily made semi-insulating, providing excellent

current confinement in the TJS laser diode. Another advantage of the structure shown for the TJS laser is that it incorporates two-dimensional index guiding, which should give extremely good mode confinement. The parallel metal stripes on the surface serve as a slot waveguide to confine the lasing mode in the direction parallel to the surface. We have done extensive calculations and modeling on various geometries of these slot waveguides, some of the results of which are included in the following section.

The problem with the AlInAs interlayer is that in cases studied to date, it reduces the quality (in terms of luminescence linewidth and efficiency) of the GaInAs active layer.[8] However other workers have shown that this is not a fatal limitation.[9] Substantial materials work remains to be done to solve this problem.

SLOT WAVEGUIDES FOR MONOLITHIC INTEGRATION

The slot waveguide configuration shown schematically in Fig. 2 appears to be extremely promising for monolithic integration in III-V compounds. The reasons for this are the experimental demonstration of stable guiding with very low threshold injection lasers in the AlGaAs heterostructure system[10], the compatibility with TJS lasers as shown in Fig. 2, and the obvious compatibility with electro-optic devices employing planar surface electrodes.

We have done extensive numerical calculations on the properties of slot waveguides in various geometries, and confirm that excellent low-loss waveguides can be made in various III-V compound heterostructure systems. These waveguides contain as an inherent component the electrode structures necessary for inducing electro-optic effects, or pumping TJS lasers. A further advantage of this waveguide geometry is that it is compatible with optical pumping, which is convenient for fundamental investigations. The basic geometry of the slot waveguide system we analyzed is shown in Fig. 3. The long direction of the slot is oriented along a <110> direction so that electric fields applied by the electrodes are along along <110> directions as required for usable electro-optic devices. The various guide geometries we analyzed are shown in Fig. 4. These waveguides are not only useful to provide a passive guide for a laser structure, but are also suitable for combining an electro-optically active device within a laser cavity, such as a Q-switch or a tunable birefringent filter (which will provide a frequency tunable diode laser).

We previously demonstrated the feasibility for rapid electro-optic frequency tuning of diode lasers,[3] and are now constructing a monolithically integrated version of this system. While the simple slot waveguide geometry shown as Type I can provide good guiding and low enough loss for a laser cavity, additional considerations arise when one considers electro-optic devices. (See Fig. 5 for the results in the simple system). Two additional considerations of importance for electro-optic devices are achievement of phase matching between TE and TM modes so that good conversion efficiency can be obtained on application of an electric field, and the requirement for some electro-optic structures that both TE and TM modes exhibit low loss. These requirements led to the investigation of the other waveguide geometries shown as Types II through VI. The only geometries which meet both of these requirements, of good phase matching and low loss for TE and TM modes, are Types V and VI, with Type VI being the preferred guide. As shown in Figs. 6 and 7, both of these systems can provide good phase matching; however, the Type VI

guide appears to have relaxed fabrication tolerances as compared to Type V. The fabrication tolerances are very sensitive functions of the Aluminum content in the cladding layers. Decreasing Al content relaxes these tolerances. The mode confinement for a representative Type VI guide is shown in Fig. 8 and the electro-optic coupling efficiency for TE to TM modes is shown in Fig. 9. As shown in Fig. 5, the simpler waveguide types I-IV show a great difference between loss for TE and TM modes. Such a structure would be particularly useful for Q-switching a diode laser in a monolithically integrated configuration.

INTEGRATED SUBSYSTEMS

In Figs. 10 and 11 we show the circuit diagram and photograph of a finished circuit of a monolithically integrated OPFET detector and three stage wide bandwidth amplifier. This system has been designed to give a voltage gain of 7, a power gain of 250 (over 23 dB), and a frequency response exceeding 5 GHz. One unique feature of this chip is the inclusion of a new type of interdigitated OPFET detector shown in Fig. 12. The areal response of this detector is shown in Fig. 13 which is the photocurrent due to a HeNe laser spot, raster scanned over the detector. The low frequency gain measured in this experiment was 14, which is most likely a factor of 2 larger than would be measured at high speeds. Such high speed measurements are now in progress. In Figs. 14 and 15 we show the circuit diagram and layout for an integrated laser/driver-transistor circuit being fabricated in the materials structure shown in Fig. 2. The two small FETs connected in series on the gate of the driver transistor provide a convenient, area-and-power-efficient method for setting the bias level on the laser diode.

CONCLUSIONS

In this paper we have identified what we consider to be viable approaches for the monolithic integration of detectors, lasers, amplifiers, and electro-optic components in two material systems which operate in quite different wavelength regions. For the first time, we have carried out extensive numerical calculations on slot waveguide structures in III-V compounds, and have computed parameters which are useful for the design of guides for electro-optic components in the systems. The results of these computations give information on the confinement of various geometry guides, the attenuation and the electro-optic coupling parameters of these guides. Finally, we have fabricated the most complex monolithic integrated opto-electronic circuits so far reported in III-V compounds, and have verified their performance at low frequency. We expect these circuits to give good operation at gigahertz speeds.

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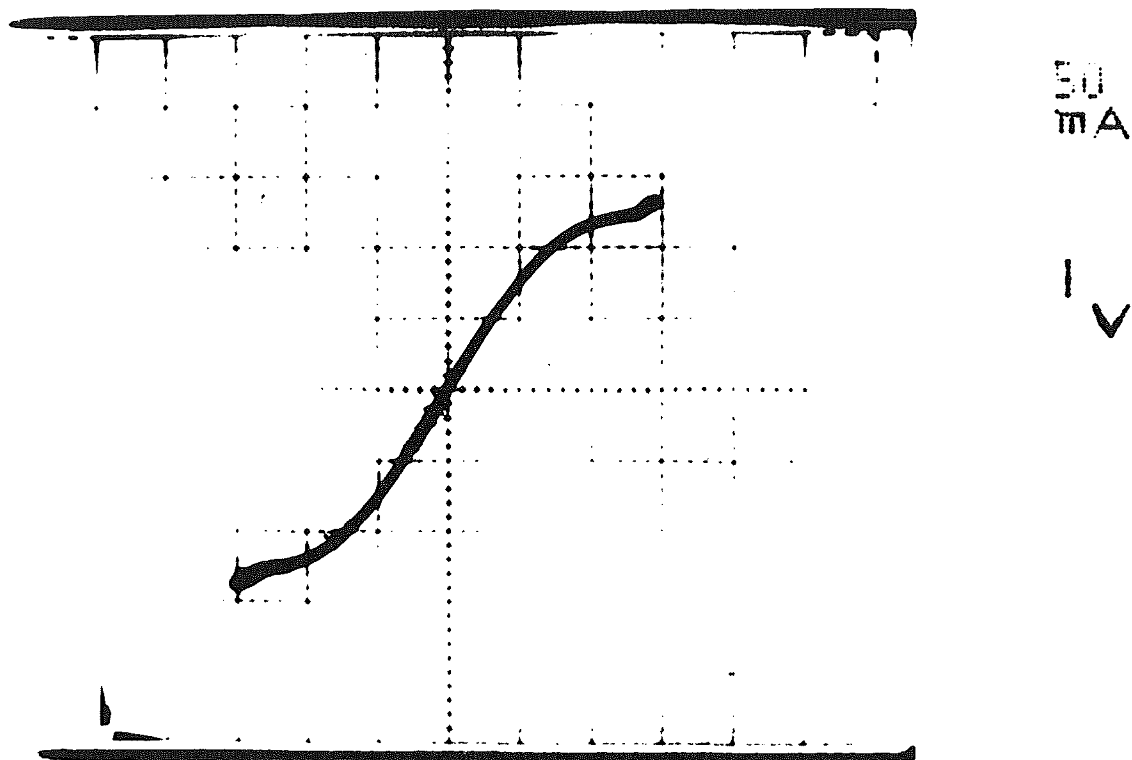


Fig. 1 I(V) curve of a GaInAs OPFET grown on an InP substrate by MBE[6]. Rise in current at end of trace is due to leakage through the substrate-epilayer interface.

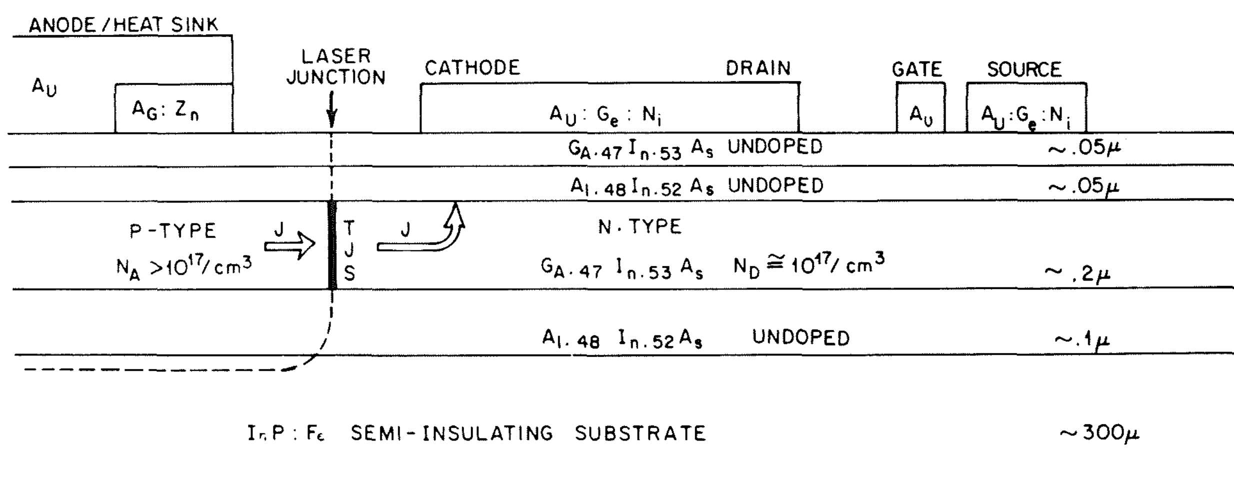
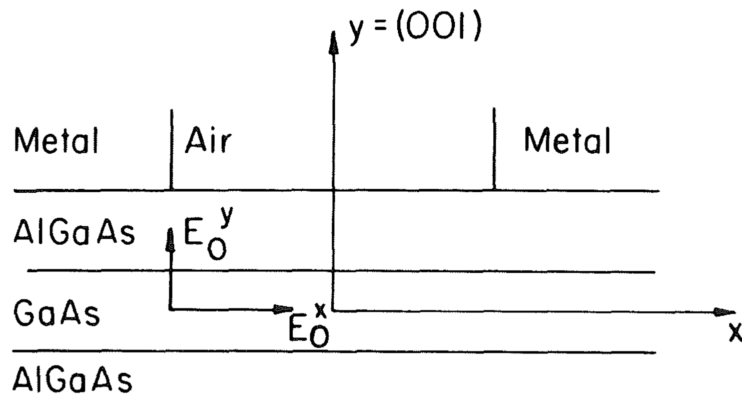
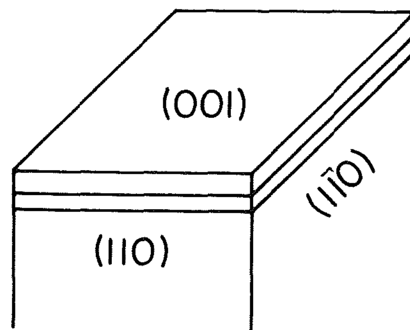


Fig. 2 Schematic diagram of proposed heterostructure system for monolithically integrated opto-electronic circuits on InP substrates.



(a)



(b)

Fig. 3 Basic geometry of a slot-waveguide structure compatible with monolithic electro-optic devices in III-V compounds.

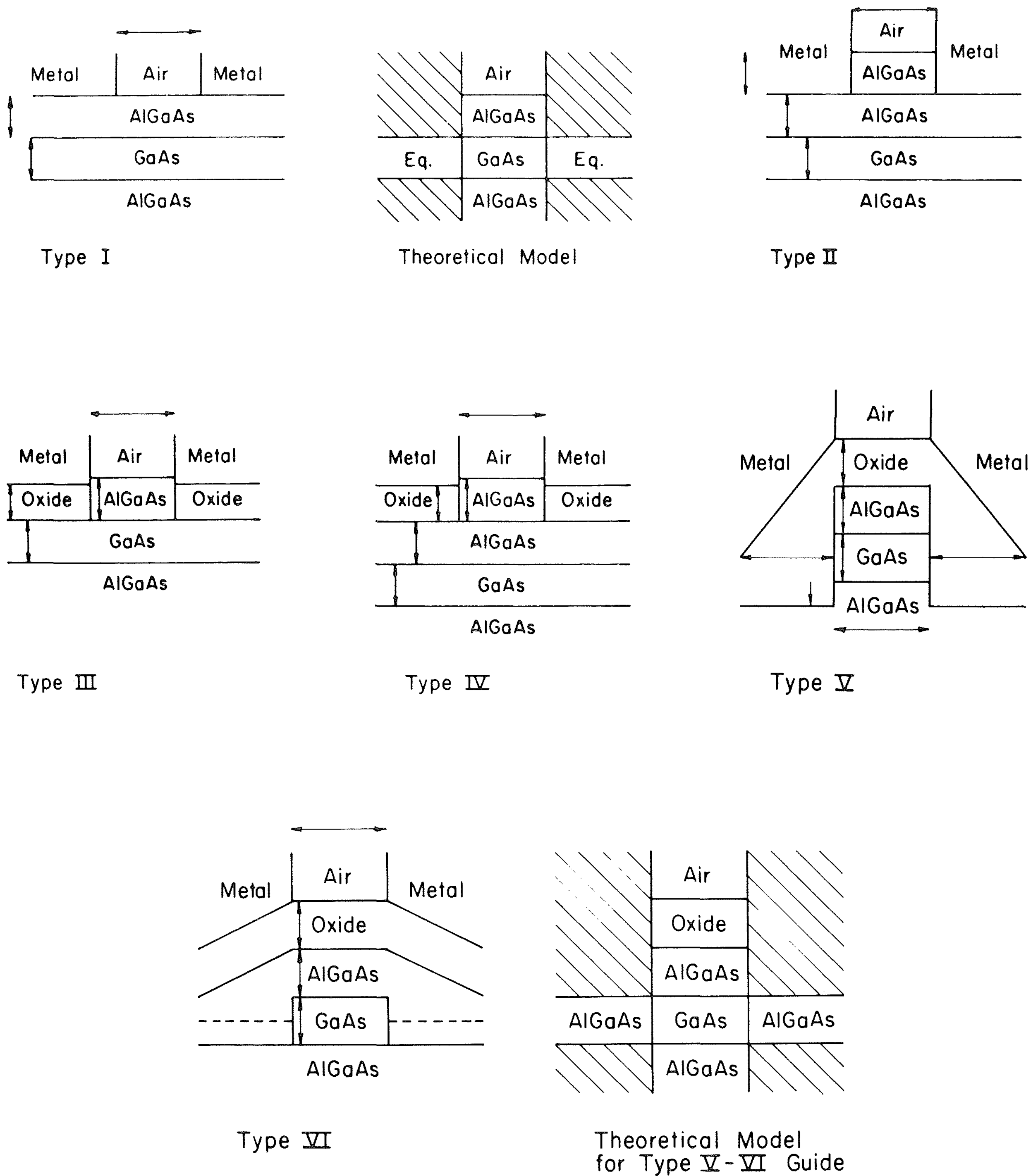
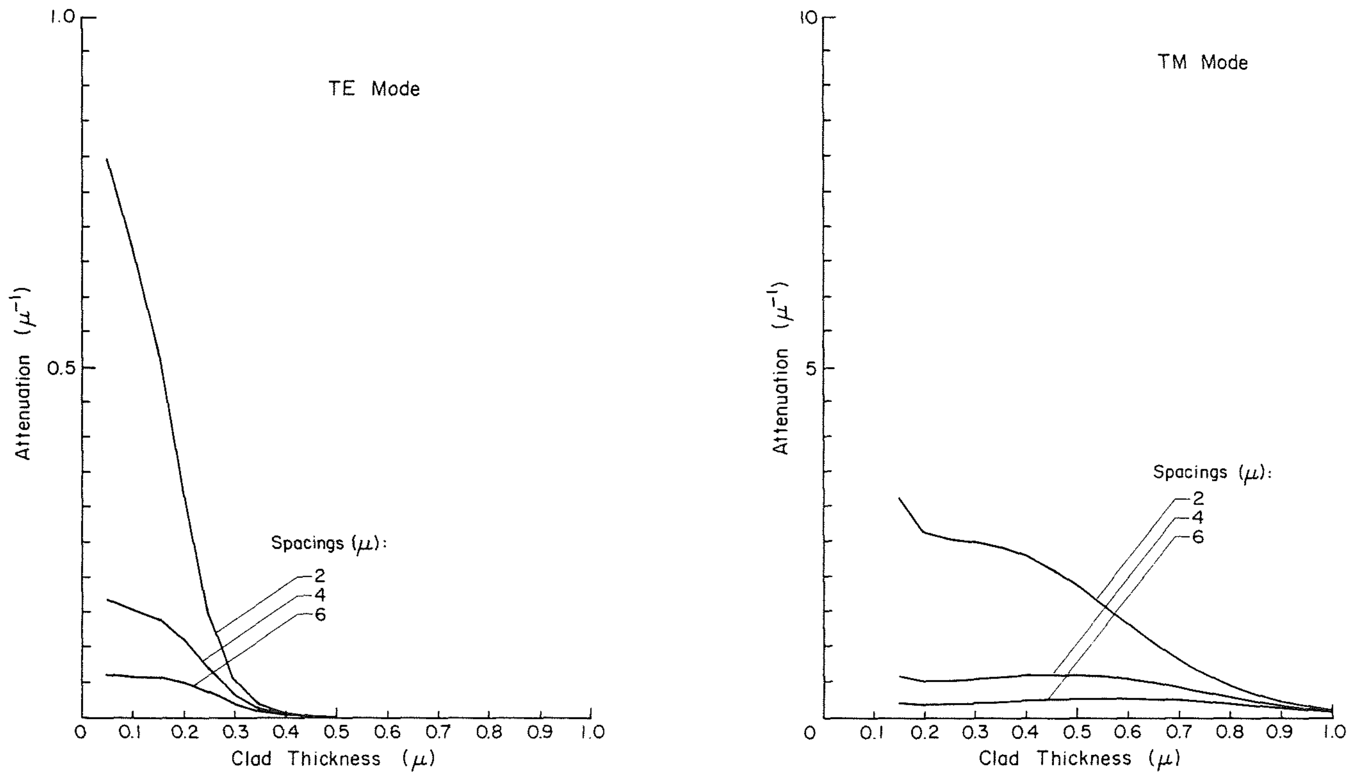
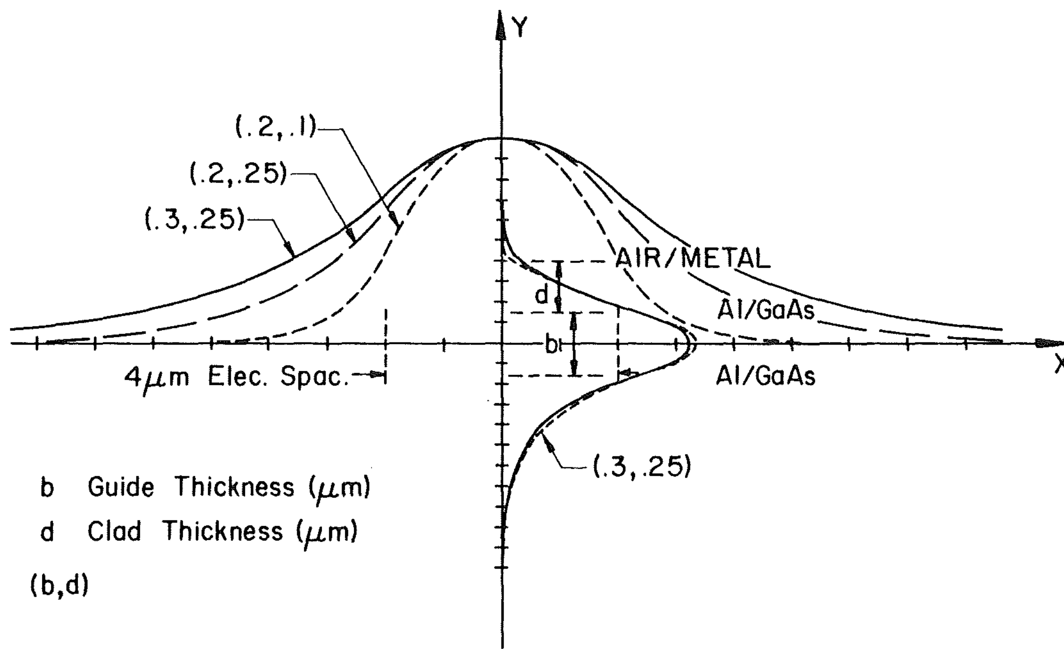


Fig. 4 Slot-waveguide geometries for which analysis was carried out, along with basic models used for two classes of guides.



a) Attenuation vs. clad thickness for several electrode spacings.



b) Mode confinement.

Fig. 5 Results for modes in Type I waveguide.

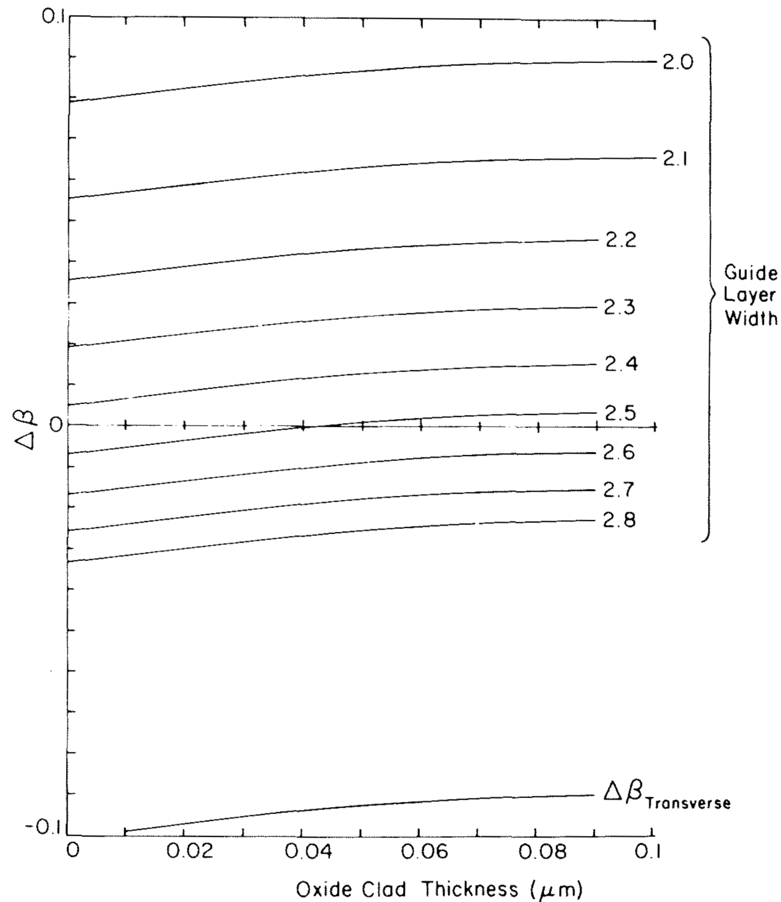


Fig. 6 Phase difference, $\Delta\beta$, between TE and TM modes in Type V waveguide. $\Delta\beta$ is zero for a 2.5 μm wide guide and an oxide clad of 0.04 μm. Note sensitivity to fabrication tolerances.

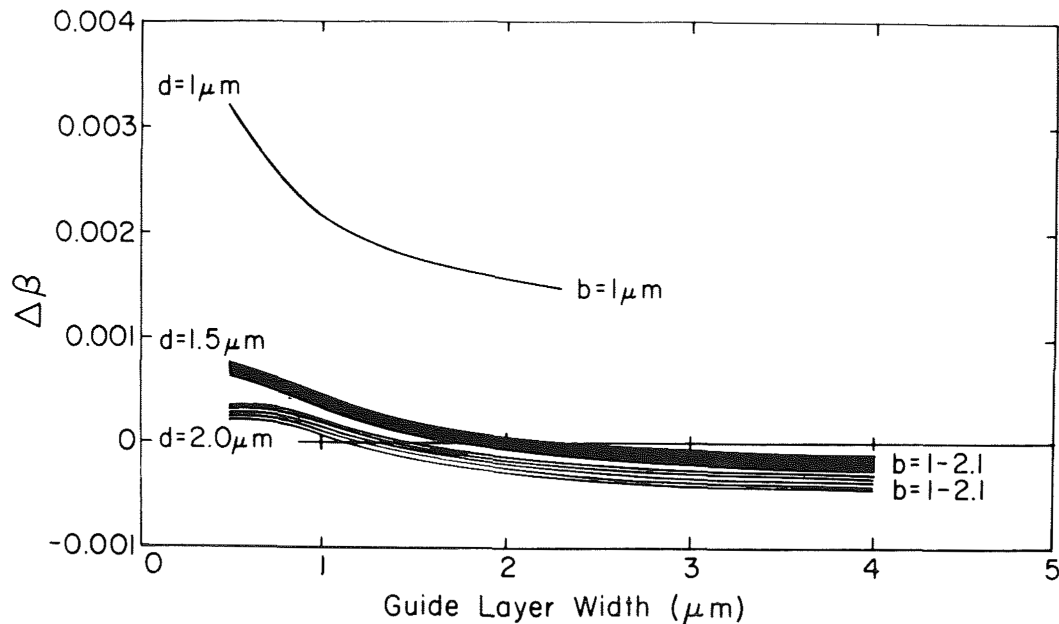


Fig. 7. Phase difference, $\Delta\beta$, between TE and TM modes in Type VI waveguide: Oxide and $Al_xGa_{1-x}As$ thickness are d and b respectively. Case illustrated is for x = .05. Note large tolerances in d, b, and width to allow $\Delta\beta$ to be nearly zero.

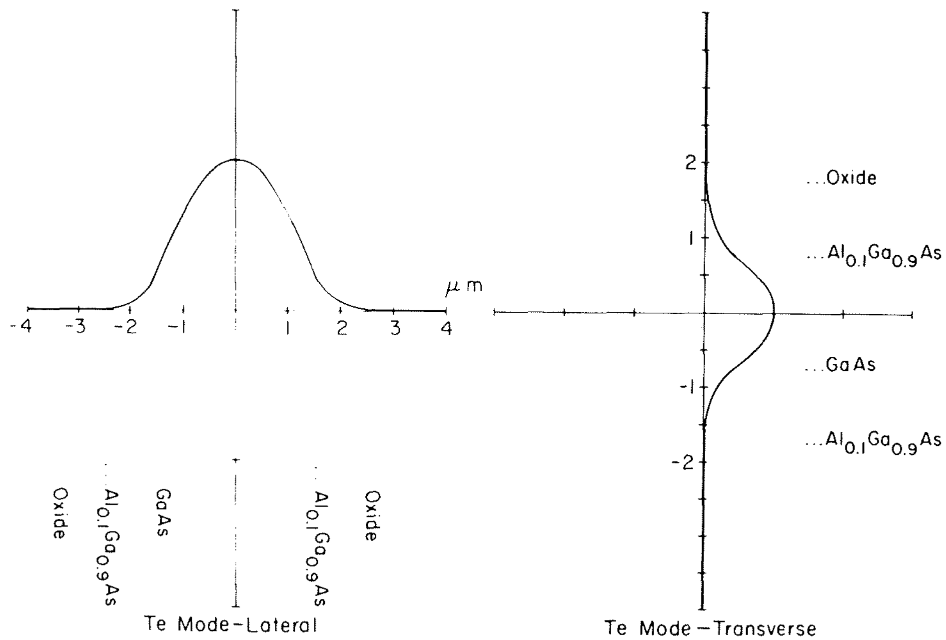


Fig. 8. Mode confinement for a representative Type VI waveguide. Amplitudes are normalized.

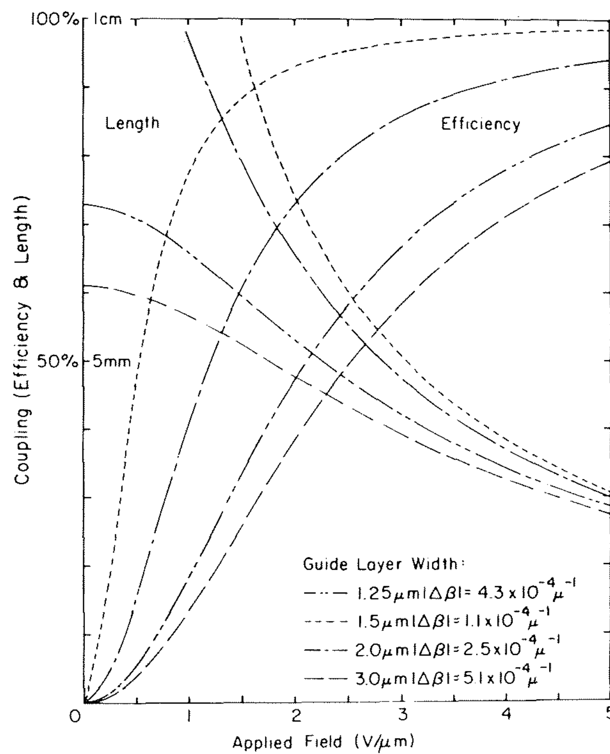


Fig. 9. Efficiency for coupling TE to TM modes in Type VI guides via the electro-optic effect.

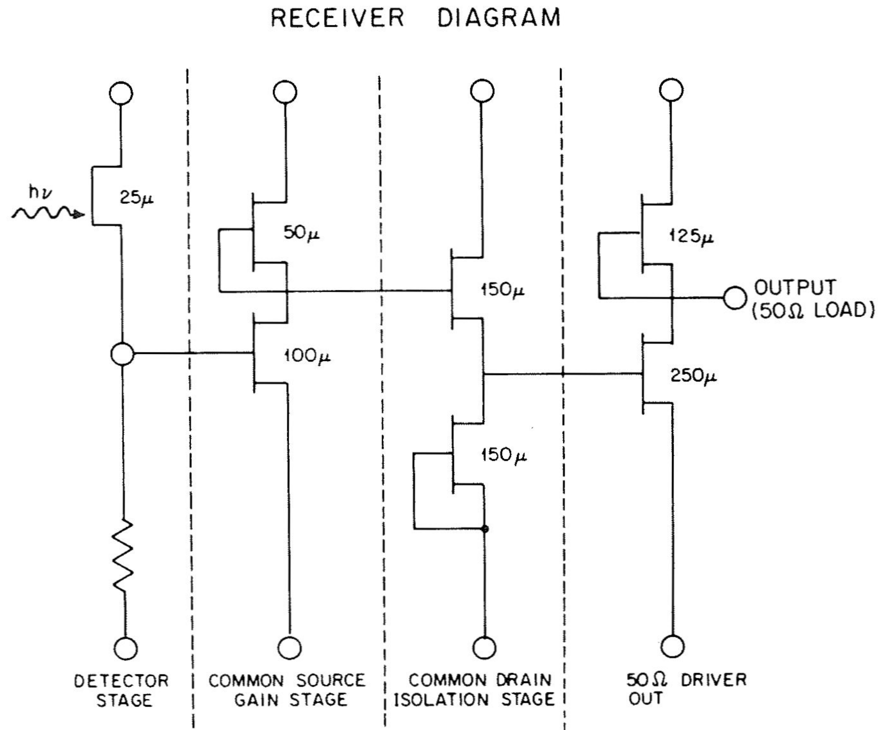


Fig. 10 Circuit diagram of a monolithically integrated receiver combining an OPFET with a 3-stage amplifier.

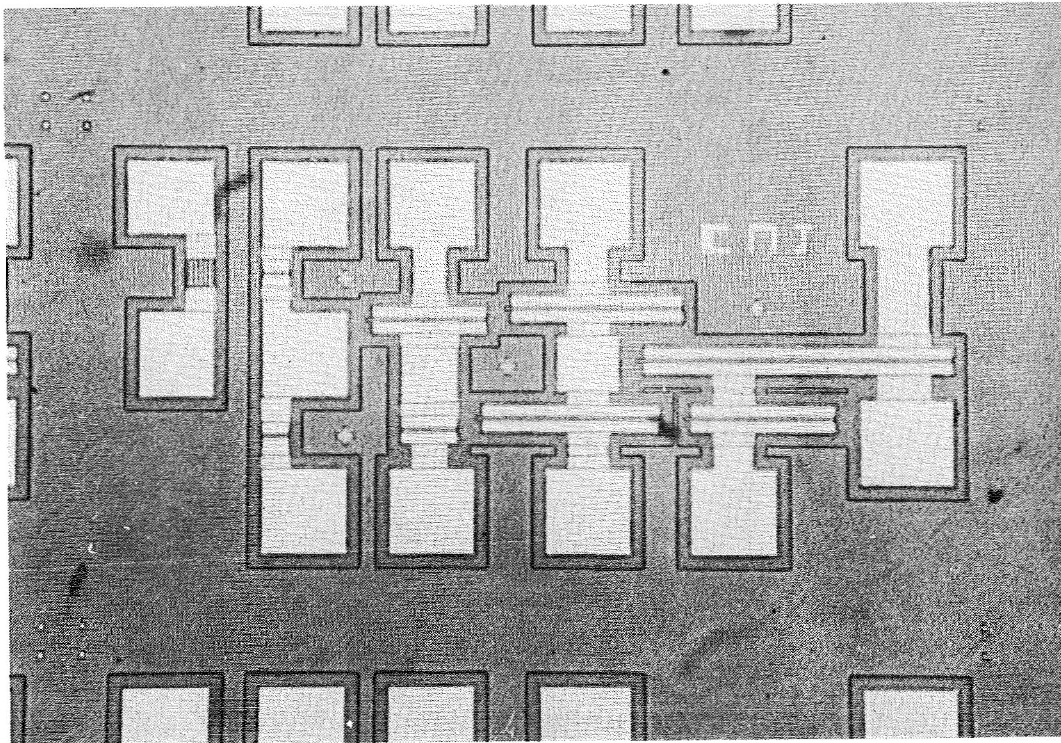
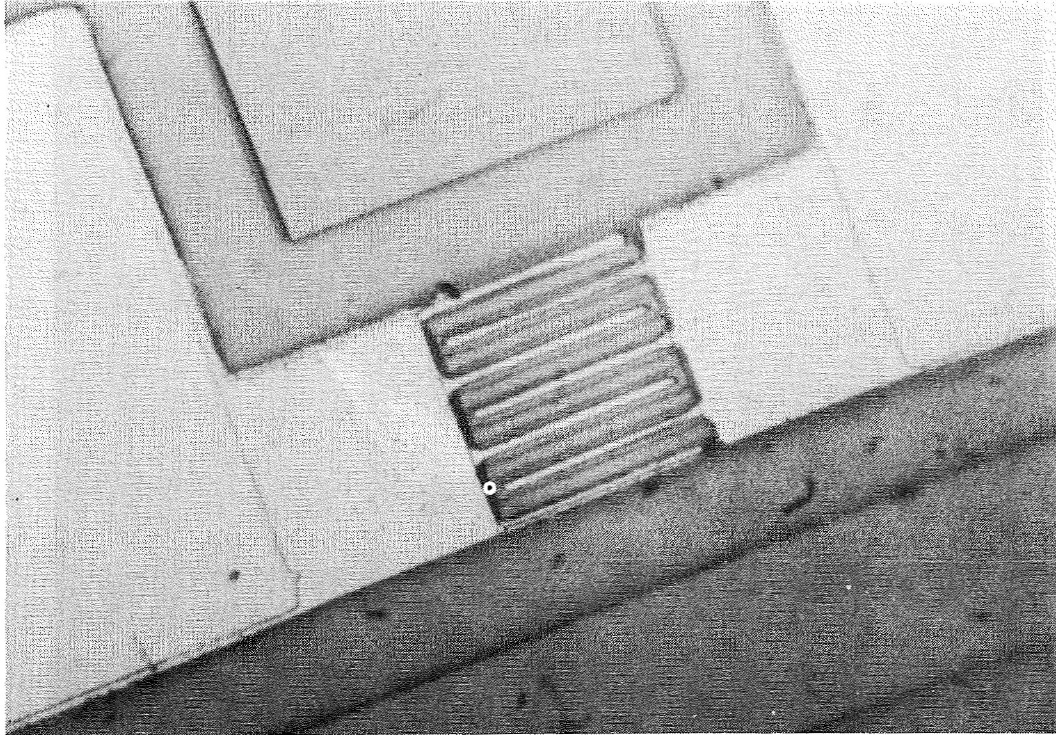
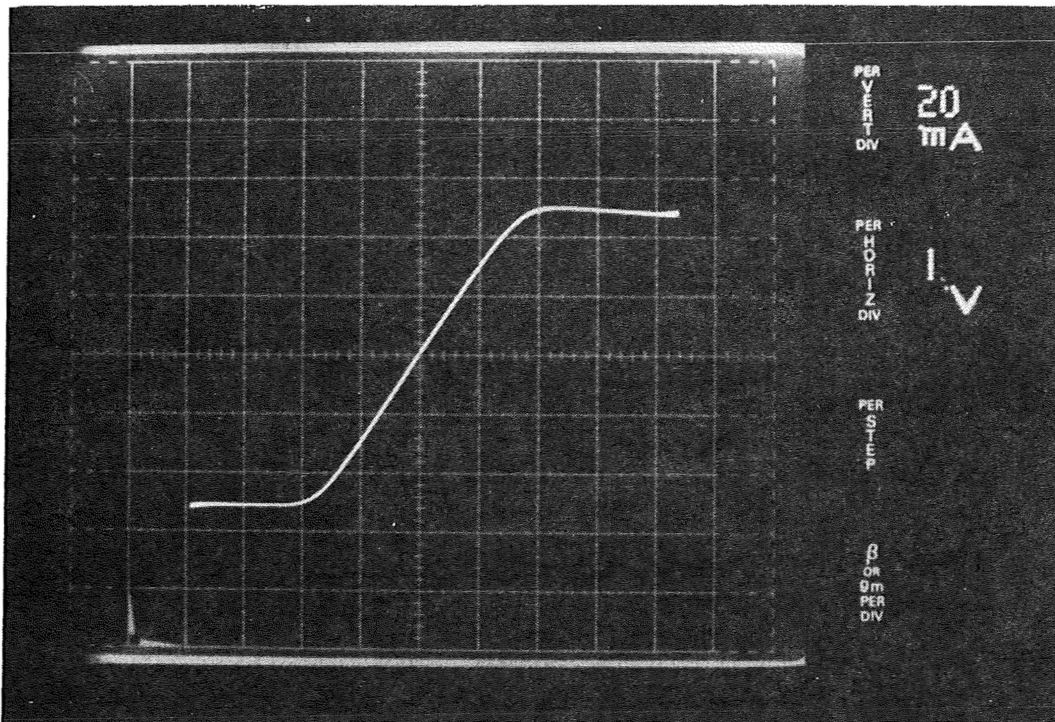


Fig. 11 Photograph of receiver of Fig. 10. Gates are missing in this photograph.



(a)



(b)

Fig. 12 Interdigitated OPFET with grooves between fingers (a), and I(V) curve of detector (b).

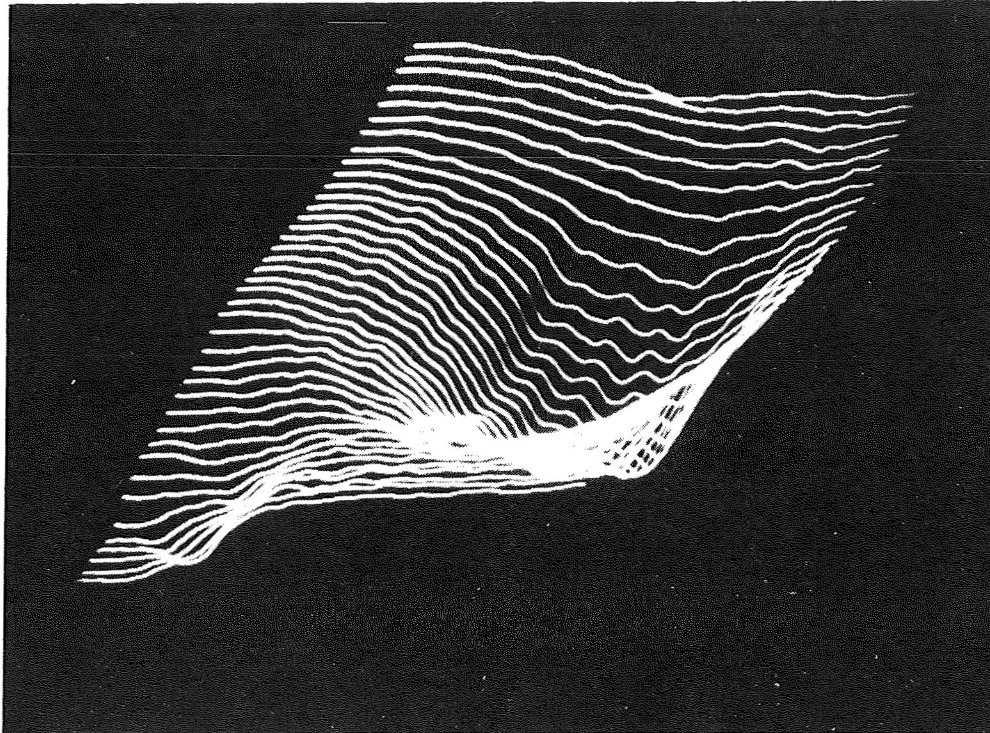


Fig. 13 Spatial response of detector in Fig. 12. Increasing response is downward. Response in lower left is an artifact due to light reflecting from bonding wire.

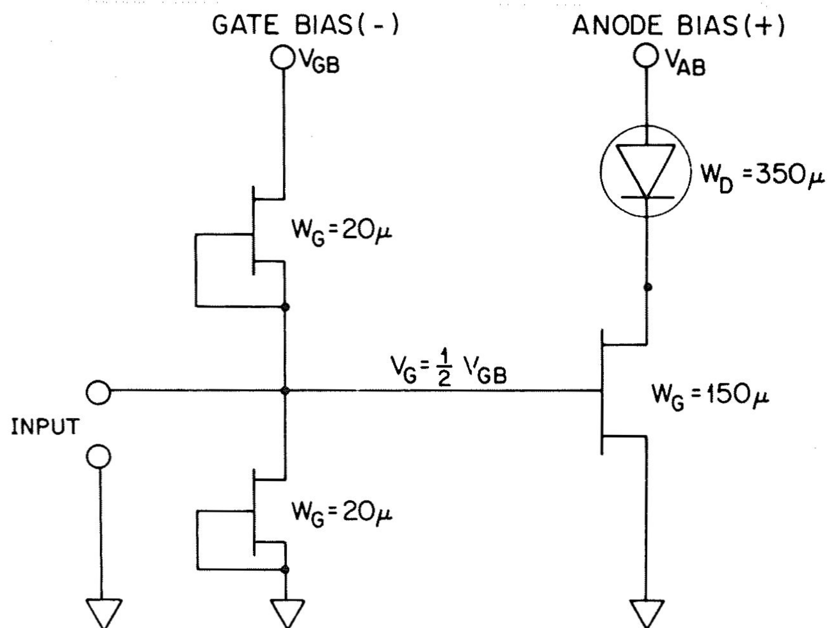


Fig. 14 Circuit diagram for an integrated laser-driver circuit being constructed in materials systems of Fig. 2.

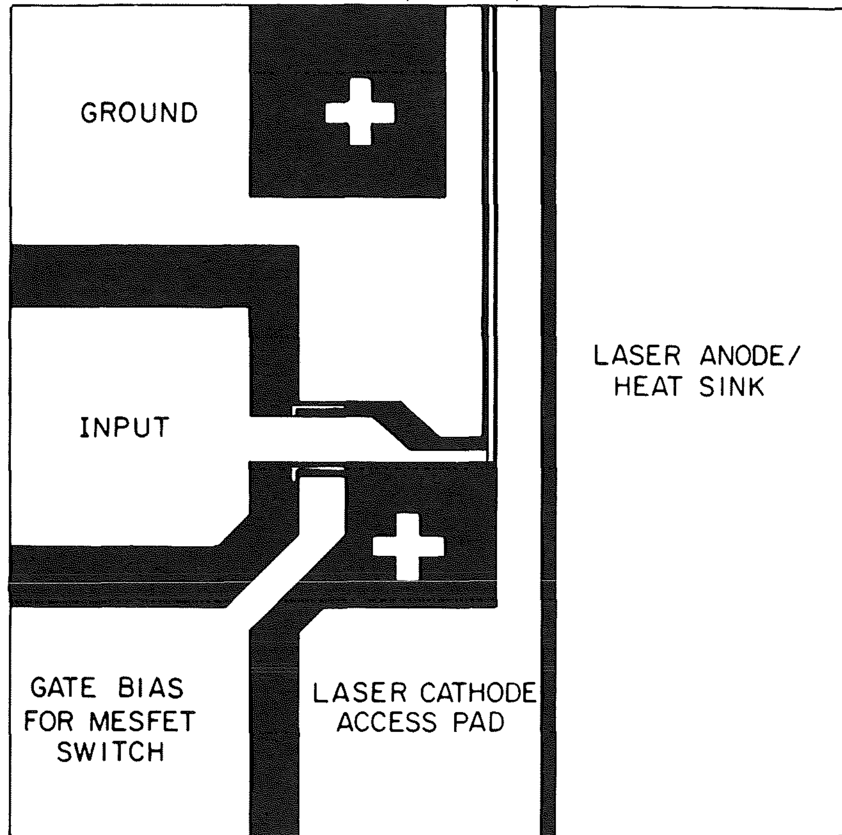


Fig. 15 Layout of circuit of Fig. 14.