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HIGH-VOLTAGE POWER-TRANSISTOR DEVELOPMENT

by P. L. Hower and Y. C. Kao

Westinghouse Electric Corporation

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16. Abstract

This program has been successfully completed and a total of 50 transistors that meet the specifications has been shipped to NASA Lewis Research Center. Twelve extra devices that were sent to Westinghouse AED, Lima, Ohio, for experimental work on NASA Remote Power Controller Program have been performing satisfactorily in the breadboard circuits.

This final report describes work performed under this contract. Technique improvements such as controlling the electric field at the surface and perserving lifetimes in the collector region have advanced the state of the art in high-voltage transistors. These improvements can be applied directly to the development of 1200-volt, 200-ampere transistors.

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1. INTRODUCTION

The major objective of this program has been to develop a technology for fabricating large-area, high-voltage transistors for use in advanced power-switching applications. The device was to be 33 mm in diameter with a collector-emitter sustaining voltage V_{CEO} (sus) lying between 1000 and 1200 volts. Also, it was to be capable of switching a collector current of 30 amperes at a voltage of at least 900 volts, corresponding to a "power-switch-product' of 81 kVA.

The program was intended to make use of processing technology developed under NASA Contract NAS3-18916. The success of that program has resulted in the development of a new production line of high-power switching transistors at the Westinghouse Semiconductor Division. Under that contract, many of the problems associated with adapting high-power thyristor technology for making the transistor were solved, and a number of advances in the art of designing, fabricating, and evaluating high-power switching transistors were achieved. Under the present contract, such new advances have been extended to high-voltage transistors. In addition to developing new processing methods for achieving high-voltage junctions and high lifetime in the collector region, new methods of in-process testing and rating of high-voltage switching performance have been included.

This program has been successfully completed and a total of 50 transistors that meet the specifications of the contract requirement (for target specifications, see Appendix A) have been shipped to NASA. Furthermore, 12 extra transistors have been sent to Westinghouse Aerospace Electrical Division (AED), Lima, Ohio, for experimental work on the NASA Remote Power Controller Program. Devices have been performing satisfactorily in the breadboard circuit.

This final report describes the work performed under this contract. Following this introductory section is a description of the design considerations (Section 2), the fabrication processes (Section 3), the results (Section 4), the applications (Section 5), and the summary and conclusion (Section 6).

2. DESIGN CONSIDERATIONS

Previous studies[1,2] have established that the design of transistors requires a compromise. A higher blocking voltage leads to a smaller collector current I_C at a given current gain h_{FE}. To fulfill both the blocking voltage and the collector current requirements, it is advantageous to treat the effective emitter area A_E as an independent parameter so that other device parameters can be determined to satisfy the blocking-voltage requirement. Once such device parameters are chosen, A_E can be determined to meet the collector-current requirement at a given h_{FE}. For this reason, design considerations for high-voltage transistors will be taken up in two separate parts: the device parameters and the emitter geometry design.

2.1 Device Parameters

Based on the optimum design for high-voltage switching transistors,[1] device parameters such as the collector impurity concentration, N_D, and the collector width, W_C, can be determined at a minimum effective emitter area, A_E. A computer program[2] has been established to obtain this optimization. Using this program, calculated results for a npn transistor with $V_{CEO(sus)}$ = 1000 and 1200 volts are listed in Table 1, where calculations were made under the conditions that emitter-collector volts V_{CE} = 2.5 volts, electron mobility μ_n = 1300 $cm^2/v\text{-}sec$, and the emitter junction Gummel number $G_E = 5 \times 10^{13}$ cm^{-4}/sec. Values of I_o in Table 1 were calculated from the equation[3] that

$$I_o = q\mu_n V_{CE} A_E N_D / W_c \qquad [1]$$

Table 1. Optimum Design Results

$V_{CEO(sus)}$ volts	V_{CBO} volts	h_{FE}	I_C Amp	A_E cm^2	N_C cm^{-3}	ρ ohm-cm	W_C μm	h_{FEO}	I_o Amp
1200	2408	12	20	4.96	4.9×10^{13}	97	159	23.6	8.05
1000	2013	12	30	4.43	6.1×10^{13}	79	129	24.0	10.7

Note: Calculations were made with

(a) $V_{CE} = 2.5$ volts

(b) $\mu_n = 1300$ $cm^2/V\text{-}S$

(c) $G_E = 5 \times 10^{13}$ cm^{-4}/sec

(c) $I_o = q\mu_n V_{CE} A_E N_D/W_C$

The impurity distributions and the device parameters are diagrammed in Fig. 1. In addition to N_C and W_C, other device parameters such as W_{BO}, X_{JBC}, and the impurity distributions of the base and the emitter regions are the same as that developed previously under contract NAS3-18916.

2.2 Emitter Geometry Design

It is well known that transistors require narrow emitter width and long perimeter length to improve the switching performance. However, for the process developed for making D60 transistors, when a molybdenum preform is used to achieve contact to the emitter area, excessive reductions in emitter width will lead to difficulties in attaching the preform to the emitter area. Furthermore, with reduced emitter width and extended emitter perimeter length, the resistive drop along a very thin, narrow base strip may exceed the tolerable limit to cause a nonuniform current distribution. Practical difficulties have restricted the freedom in choosing emitter geometries. Conventionally, for a given device size the emitter design should have:

(a) an emitter width no less than the dimension that can be handled easily with the molybdenum preform,

(b) an emitter perimeter as long as possible, and

(c) a wide enough spacing in the base contacting area to minimize the lateral resistive drop caused by the base current.

Within these guidelines, three different emitter designs designated as A, B, and C, as shown respectively in Fig. 2, 3, and 4, have been used for the high-voltage transistors.

Figure 2 shows the geometry of design A. The clear area at the center is the base area; narrow, clear strips are the emitter areas; the dark lines separate the emitter from the base areas. The emitter width, the perimeter length, and the area are 635 μm (25 mils), 73.5 cm, and 2.65 cm^2, respectively. A wide emitter width eases the difficulty in attaching the molybdenum preform. The pattern of the emitter strips

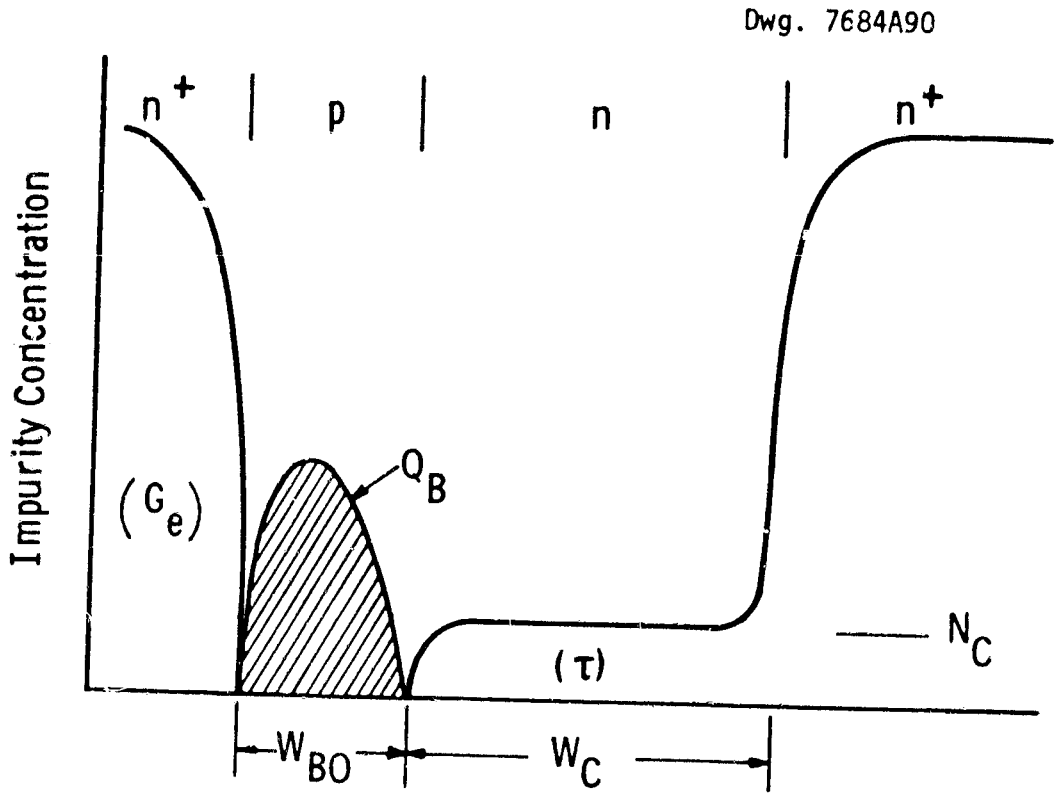

Figure 1. General shape of the triple-diffused impurity profile

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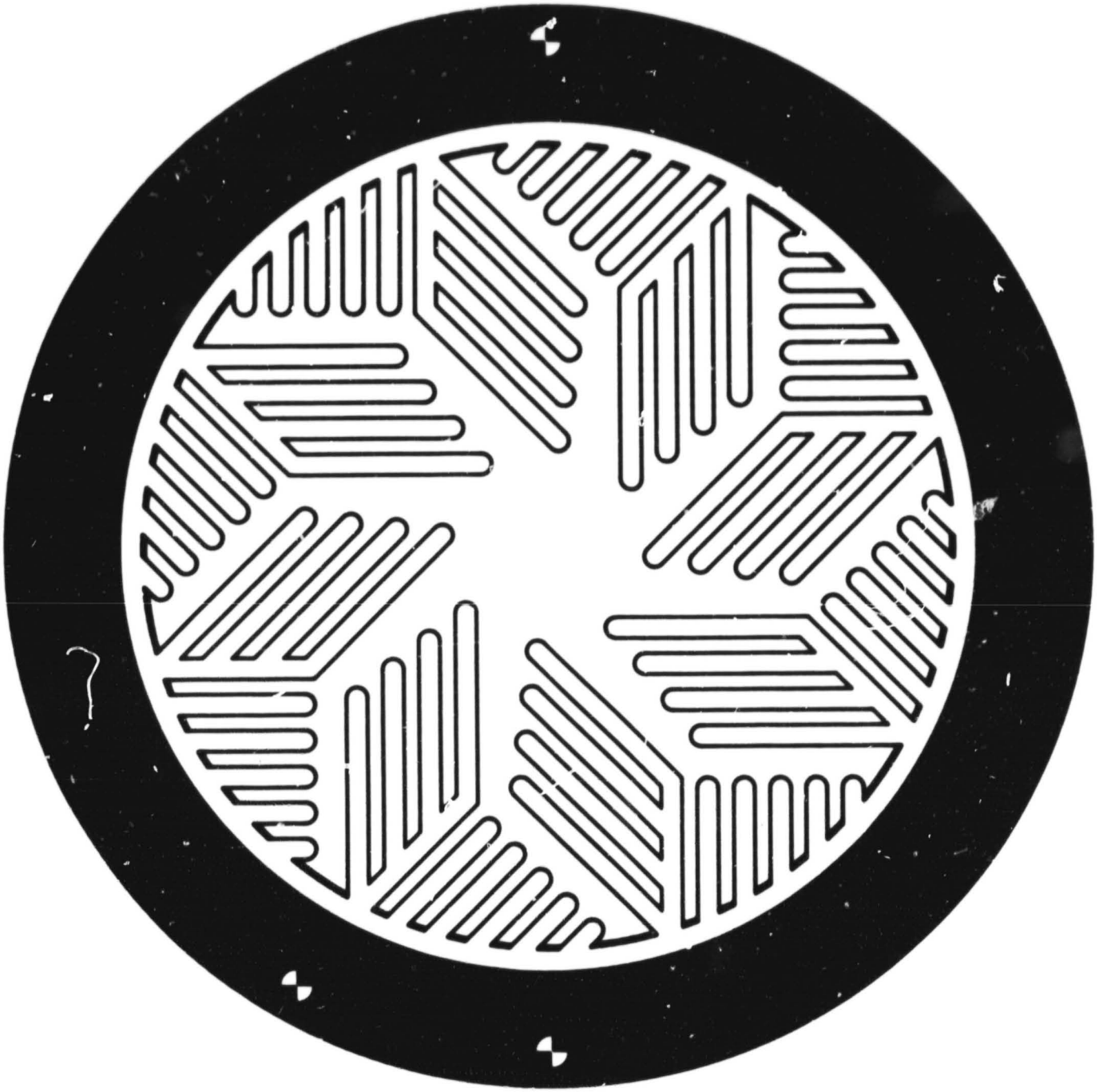

Figure 2. Mask design A for high-voltage transistors

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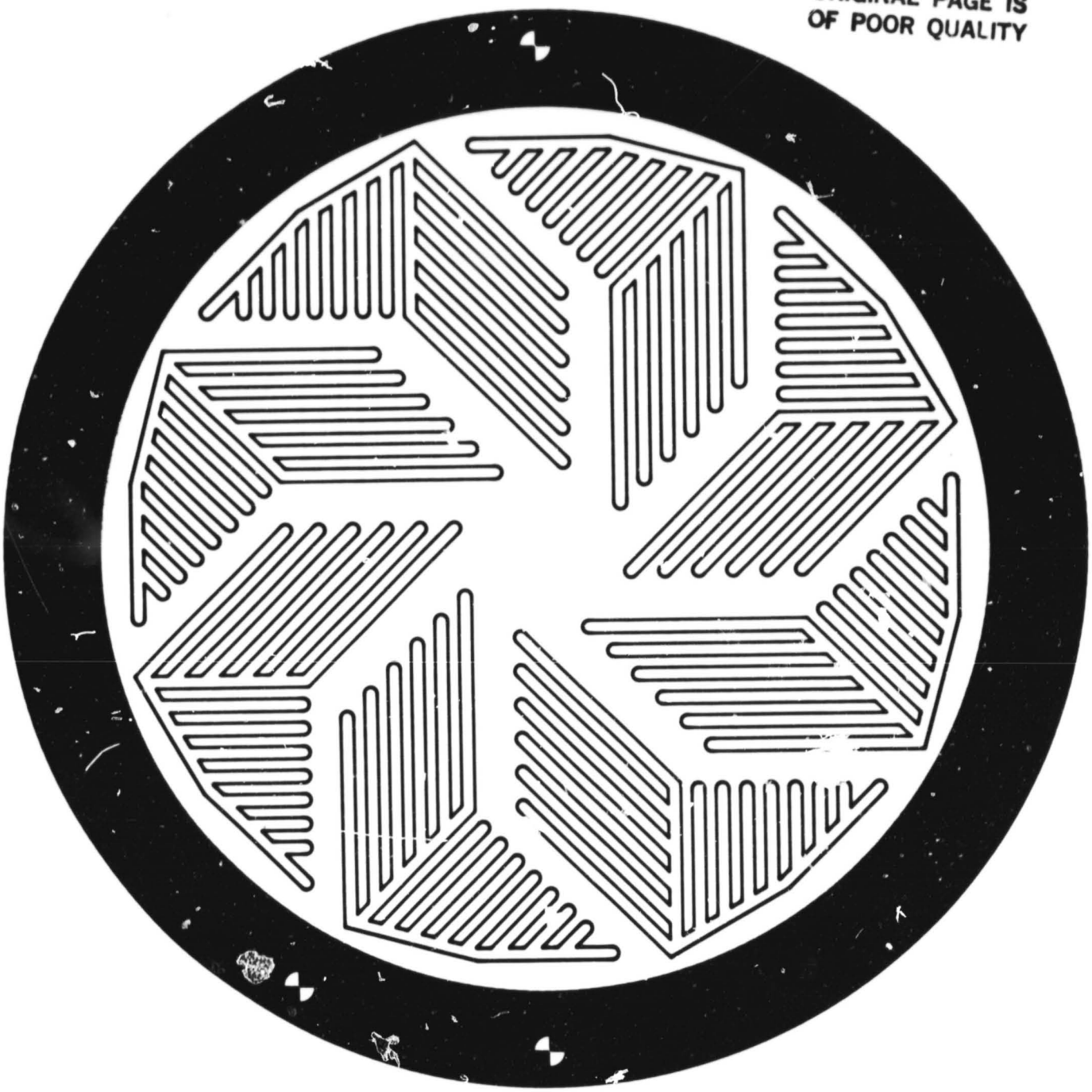

Figure 3. Mask design B for high-voltage transistors

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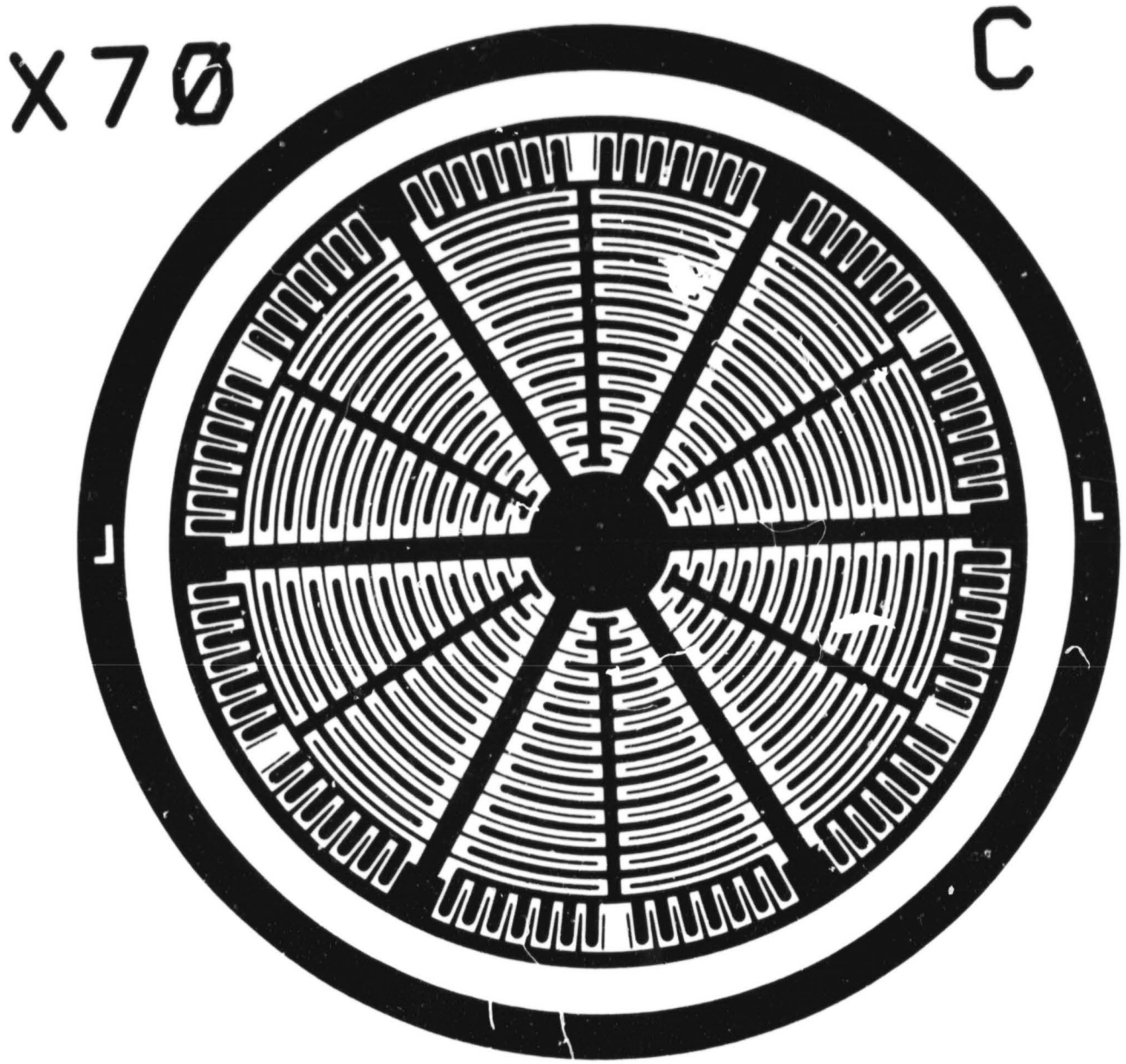

Figure 4. Mask design C for high-voltage transistors

permits the arrangement to have an equal distance between the base contact at the center and the different parts of the emitter areas at the outer rim. In addition, a large spacing between the emitter strips aims at lowering the base resistance. This spacing increases with decreasing diameter to tolerate an increase in base currents at the center.

Figure 3 shows the geometry of design B, which is the same as that shown in Fig. 2. The clear area at the center is the base; the narrow strips, the emitter; and the dark lines, the separation. Design B has eight separate sections, each surrounded by the base area so that the base current has access to the emitter strips at the outer rim. This design features a much narrower emitter width, a longer perimeter length, and a much larger spacing between the emitter strips to minimize the base drop. The emitter width, the perimeter length, and the area are 381 μm (15 mils), 117.9 cm, and 2.19 cm^2, respectively. A smaller width lengthens the perimeter but reduces the emitter area.

Because it has a narrower emitter width and eight separate sections, this design requires a different molybdenum preform. The preform must have one side etched with a pattern that is a mirror image of the emitter. The etched depth is less than the total preform thickness. This way, one preform can make contact to all eight sections. Also, the outside edge of the preform should have straight lines in the same way as that of the emitter pattern in order to ease the difficulty in aligning the preform with the emitter.

Various masking and delineation problems were encountered with designs A and B, and it was decided to use an already existing pattern to fabricate transistors within the time available for the program.

Figure 4 shows the emitter diffusion mask used for the high-current devices[2] (NAS3-21380). The dark spokes connected to the dark circle at the center are the base areas; the narrower dark concentric rings, the emitter area; and the clear area, the separations between them. As described in detail in the final report,[2] this design has a

special feature whereby the preform lowers the base resistance, thus improving the current gain at high currents. This design has been used successfully in developing high-current transistors to carry a base current of 170 amperes. The emitter width, the perimeter length, and the area are 508 μm (20 mils), 121 cm, and 3.3 cm^2, respectively. This design has yielded excellent devices.

A comparison of dimensions and special features of these three designs are listed in Table 2. Results listed in Table 2 indicate that design C is superior to designs A and B. The use of a special preform has maximized both the emitter area and the emitter perimeter length. Otherwise, the emitter areas decrease with increasing emitter perimeter length so more and more area is taken up by the base contact.

Table 2 - A Comparison of Three Emitter Designs

Design	Width μm/mils	Perimeter length cm	Area cm^2	Preform
A	635/25	73.5	2.65	Regular
B	381/15	117.9	2.19	Special
C	508/20	121	3.3	Special

3. FABRICATION PROCEDURES

Two different fabrication processes were investigated under this program. The first one, done primarily at the R&D Center, involves the use of boron diffusion to form the base-collector junction. The objective of this approach was to simplify the diffusion steps (for details see Appendix B, Table B-1). However, after several trial runs, the result was not successful. After boron diffusion, the junction showed excessive leakage current, and the process was abandoned later when such poor I-V characteristics did not improve with phosphorus diffusion and gettering.

The second process, used primarily at Westinghouse Semiconductor Division at Youngwood, Pa., is the same as that developed under contract NAS3-18916 (for details see Appendix B, Table B-2). Most of the steps are conventional silicon-processing procedures, where steps such as deep phosphorus deposition and drive, single-side lapping and polishing, silicon-molybdenum alloying, surface bevelling, etc. are peculiar to high-power device fabrication processes.

The starting materials were n-type silicon wafers, 33 mm in diameter with a resistivity between 80 and 100 ohm-cm corresponding to a doping concentration of 3.8 to 5 x 10^{13} cm^{-3}. The thickness after cleaning and etching was 343 $\pm$ 10 μm (16.5 $\pm$ 0.4 mils). After deep phosphorus diffusion and drive, wafers were machine lapped and polished on one side to the desired thickness, then diffused to form the base-collector and the emitter-base junctions. Two-point spreading resistance measurements were used to determine the impurity profile after each diffusion step. When the diffusions were completed, the collector was attached onto a piece of molybdenum disc by alloying and the emitter was metallized with evaporated aluminum. The emitter-base

junction characteristics were screened and the devices were surface bevelled, etched, and passivated. After attaching the preform on the emitter, they were tested and packaged. Pictures of a diffused and a packaged device are shown in Figs. 5 and 6, respectively.

During the process, the lifetime of the collector region was monitored at each step by using open-circuit decay measurements. Invariably, the lifetime increases with phosphorus diffusion.

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Figure 5. 33-mm transistor fusion

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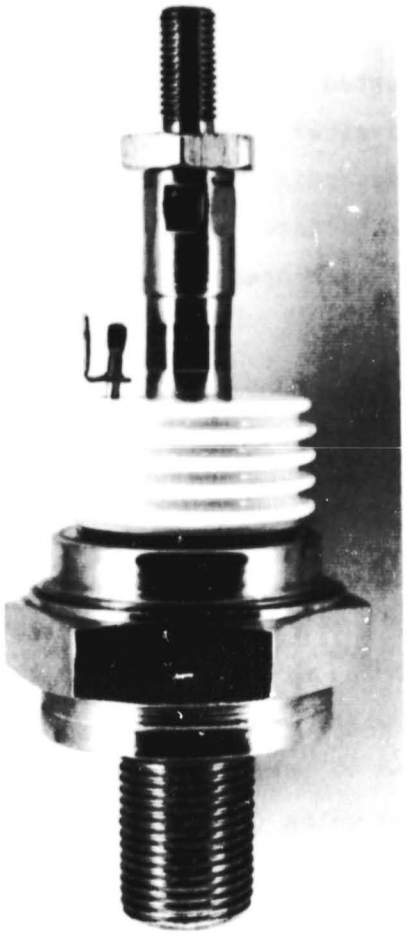

Figure 6. Package used for the high-voltage transistor

4. EVALUATION

Devices were tested for their $V_{CEO(sus)}$, V_{CBO}, and h_{FE} values at different I_C before and after packaging. Such results on two batches of devices are listed in Appendix C (Table C-1 and Table C-2). Other tests including the current-gain data, switching performance, switching power losses, and the forward safe-operating area are described separately below.

4.1 Current-Gain Data

Figures 7 and 8 show the switching waveforms at three current levels, respectively, for device #1 from run 10/11 and for device #39 from run 14. In each figure, the upper photo shows the current gain at low current, the middle photo at moderate current, and the lower photo at high-current levels. The differences between these runs are: devices from run 10/11 have a $V_{CEO(sus)}$ at ~ 1200 volts (with $W_C \approx 140$ μm) and a lifetime at around 40 to 60 μsec, whereas devices from run 14 have a $V_{CEO(sus)}$ at around 1000 volts (with $W_C \approx 90$ μm) and a lifetime at around 50 to 100 μsec.

Figures 9, 10, and 11 show the measured h_{FE} as a function of I_C for six different devices. Fig. 9 shows results of devices #1 and #3 from run 10/11. With lifetimes in the range between 40 and 50 μsec and the $G = h_{FE}I_C$ emitter area of 3.3 cm^2 for the mask design C, the value of I_o was 5.1 amperes. Figs. 10 and 11 show results of devices from run 14 with moderate and very high lifetimes. In both cases, the G was higher than 360 amperes. The calculated value of I_o is 7.6 amperes.

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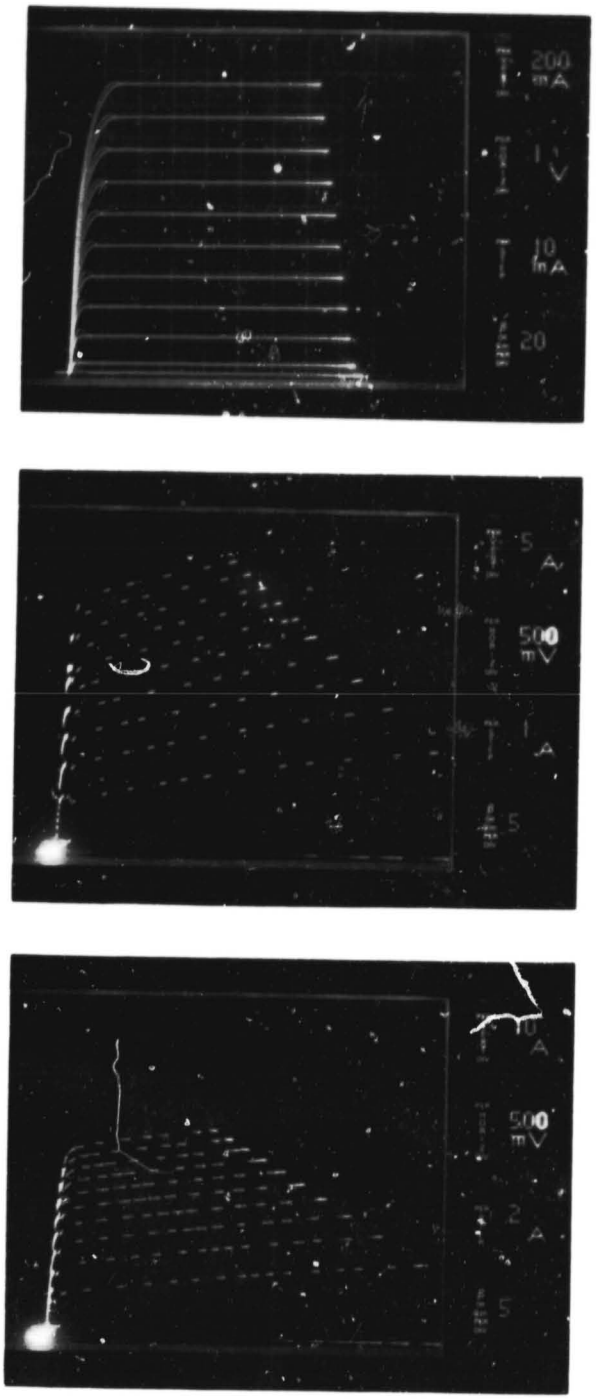

Figure 7. Collector characteristics for device 10/11-#1 at three different current levels

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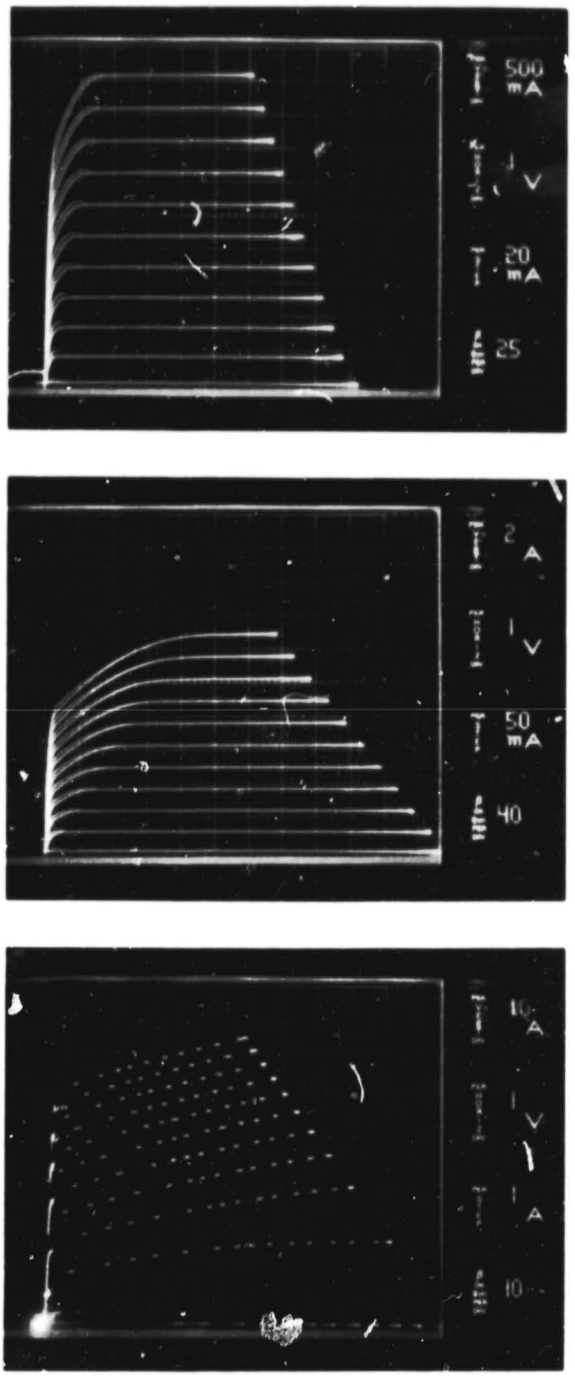

Figure 8. Collector characteristics for device 14-#39 at three different current levels

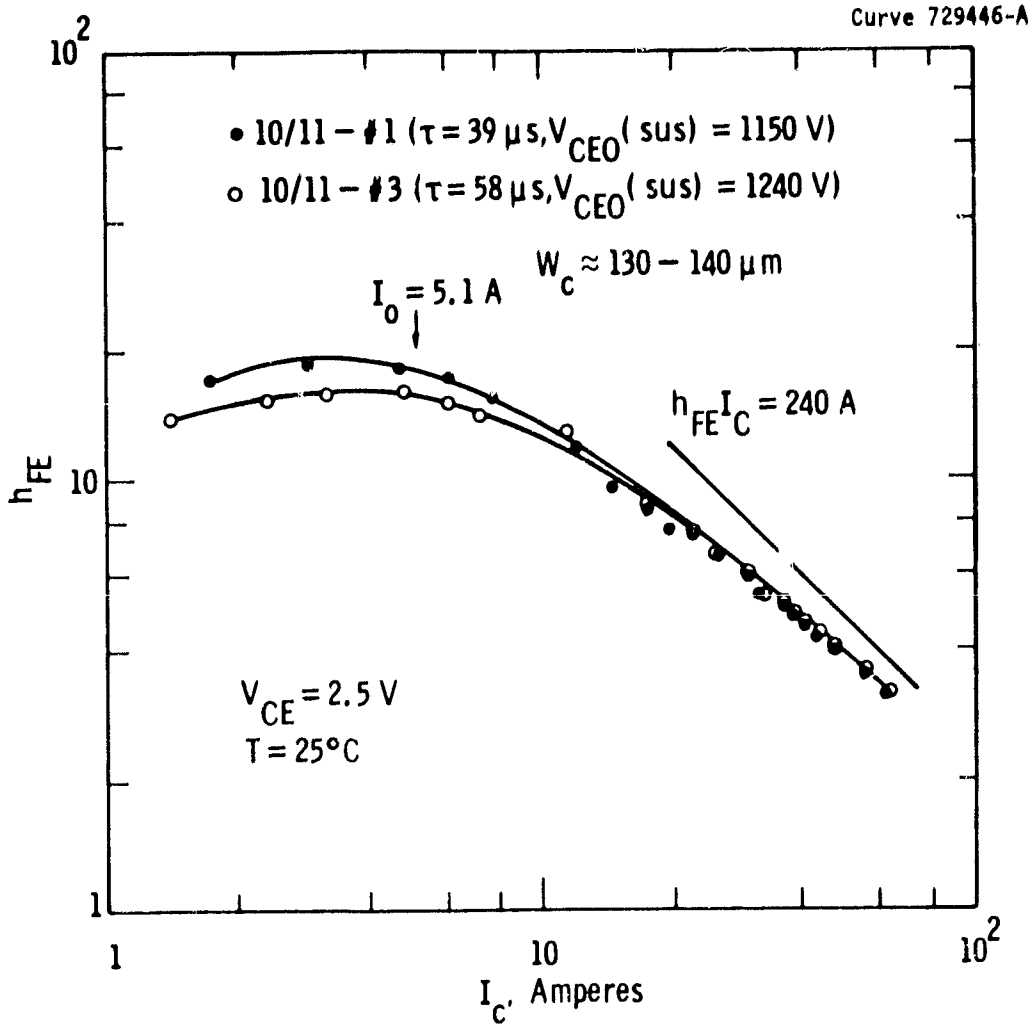

Figure 9. Measured h_{FE} vs. I_c for devices from run 10/11

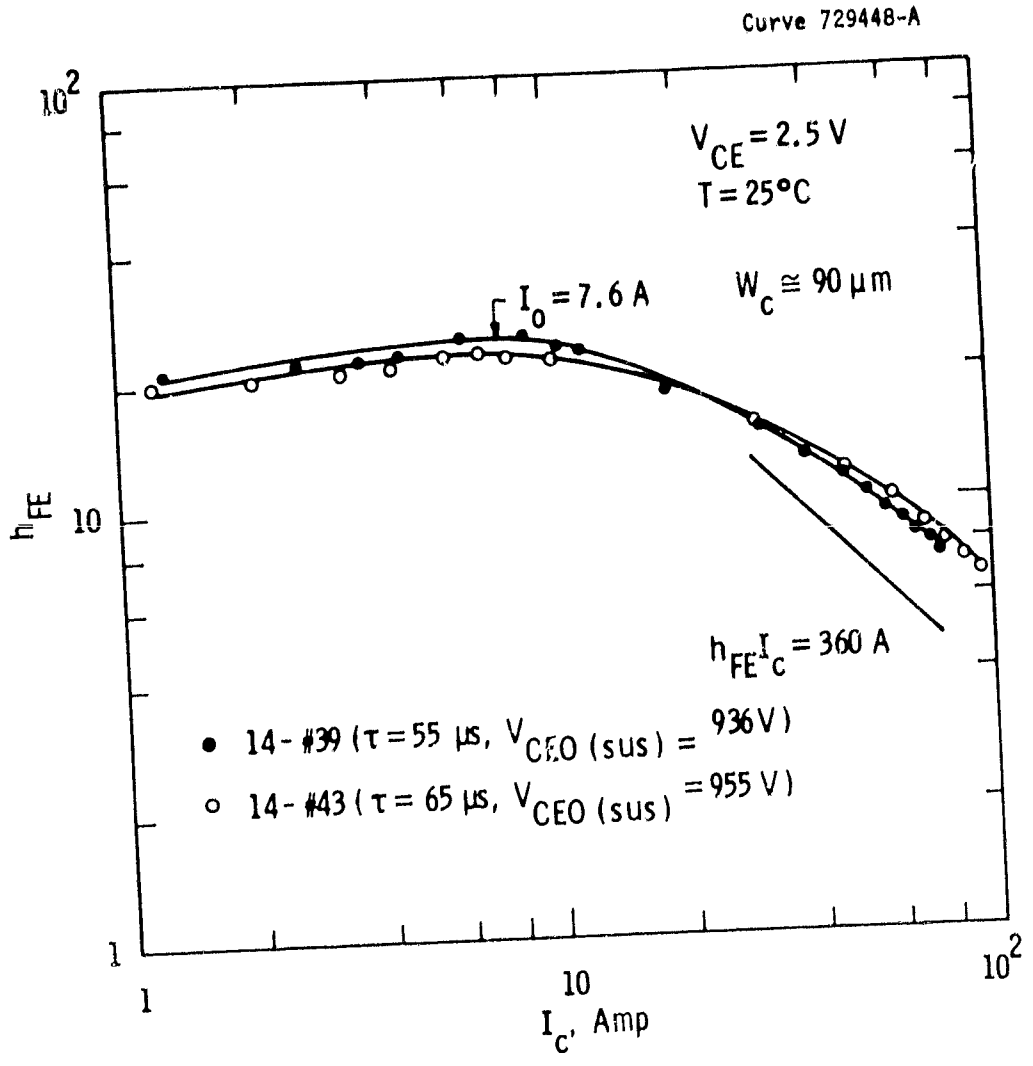

Figure 10. Measured h_{FE} vs. I_c for devices from run 14 with moderate lifetime in the collector region

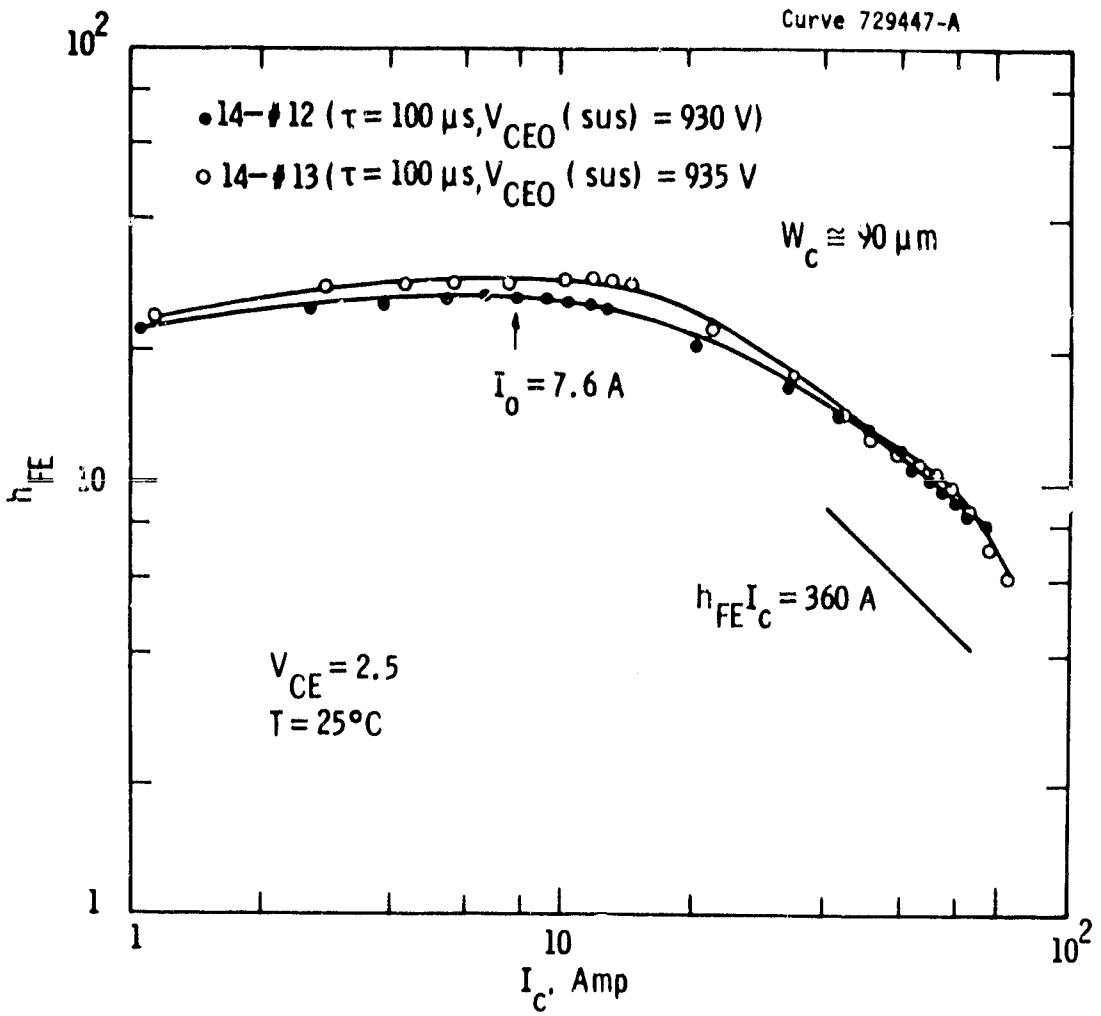

Figure 11. Measured h_{FE} vs. I_c for devices for run 14 with very good lifetimes in the collector region

Figures 9, 10, 11 show that the desired gain current product was exceeded for run 14 ($W_C \approx 90$ μm) but, for run 10/11, measured G was slightly less than the goal of 240 amperes. The most likely reason for this behavior is the lifetime difference which appears to influence G_e, the emitter Gummel number.(2) Larger values of τ generally give larger G_e.

4.2 Switching Performance

Figure 12 shows the testing circuit used for switching-performance evaluations. The base drive consists of widely spaced pulse trains which permit steady-state conditions to exist in the inductor but with low average-power loss. Low power losses minimize the temperature fluctuation during measurements of the turn-on and the turn-off losses.

Figure 13 shows the turn-on and the turn-off switching waveforms of device 14-#39. Fig. 13(a) is a photo covering the entire switching cycle; Fig. 13(b) at the turn-on; Figure 13(c) at the turn-off. At turn-on, I_C increases slowly but V_{CE} falls within half a microsecond. The circuit inductance limits the rate of rise of I_C. At turn-off, I_C falls within 0.5 μsec.

Figure 14 shows the effect of the circuit inductance in I_C. The rate of rise of I_C remained the same when V_{CE} was increased from 300 to 500 volts and I_C from 40 to 60 amperes. I_B had no effect on I_C when it was increased from 4 to 10 amperes.

Figures 15 and 16 show the turn-off waveforms for devices 14-#12 and 14-#13. In both Fig. 15(a) and (b), with an increase in V_{CE} the device did not turn off until sometime later at the end of the base current. This delay disappeared, as shown in Fig. 15(c), at higher I_B and even at much higher I_C. Since this delay in turn-off occurred only on devices 14-#12 and 14-#13, the long lifetime in these two devices' areas is probably responsible for such behavior.

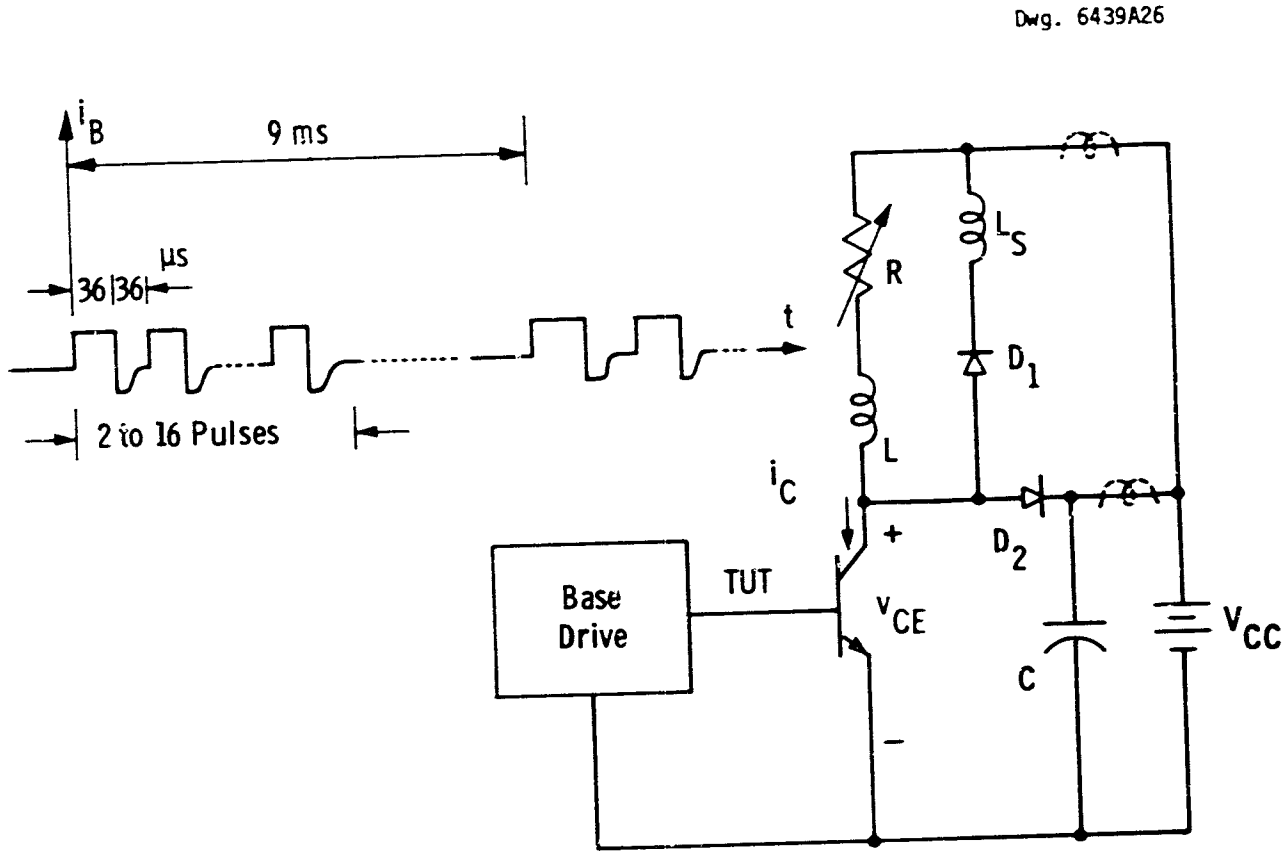

Figure 12. Test circuit used for switching-performance evaluation

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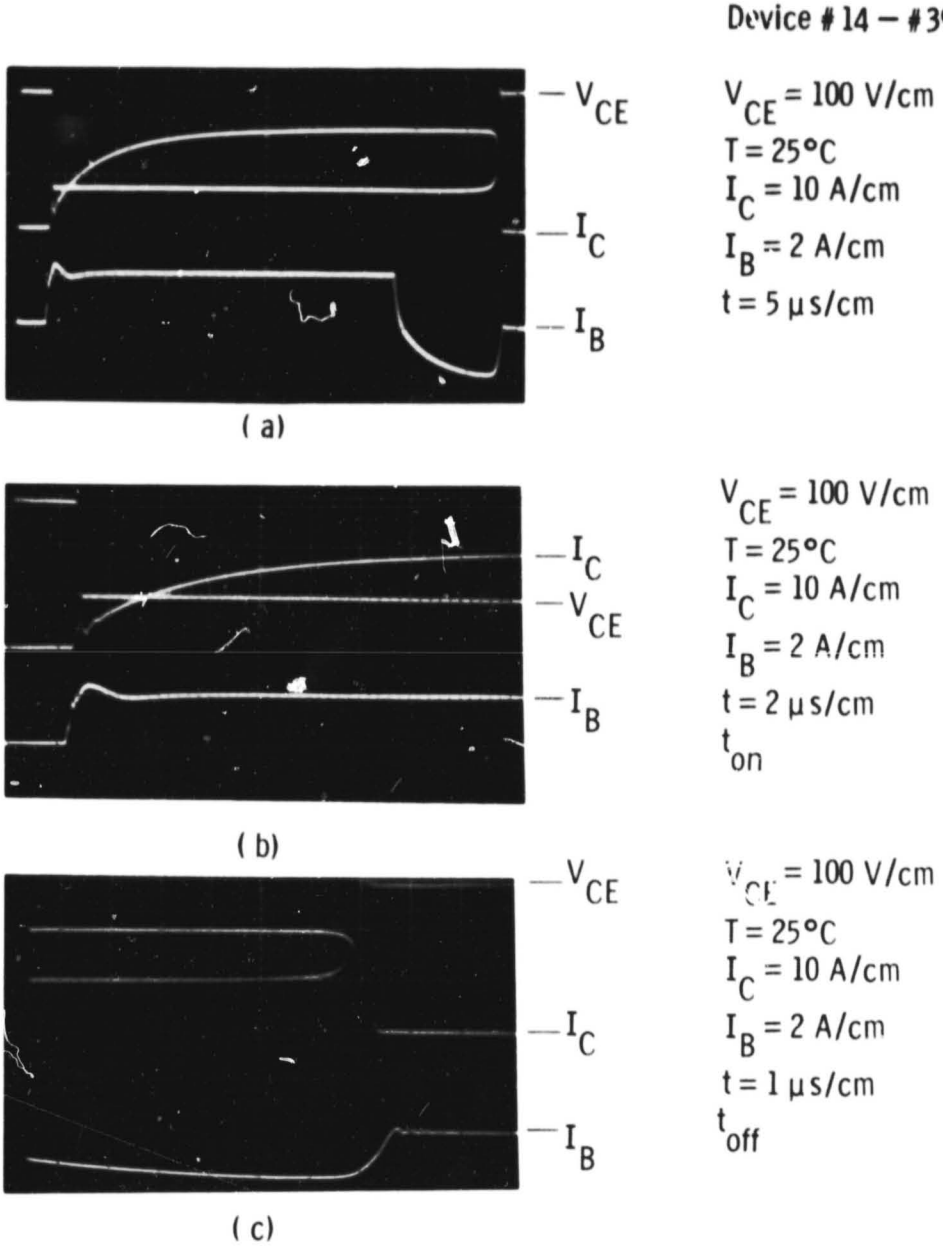

Figure 13. The turn-on and the turn-off switching waveforms of transistor 14-#39

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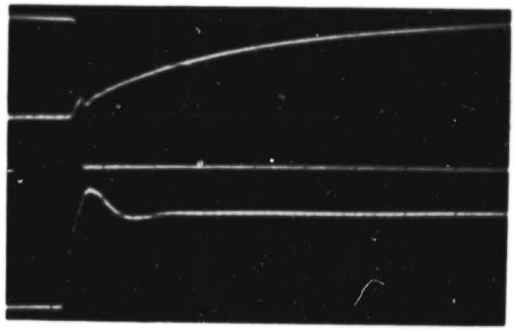
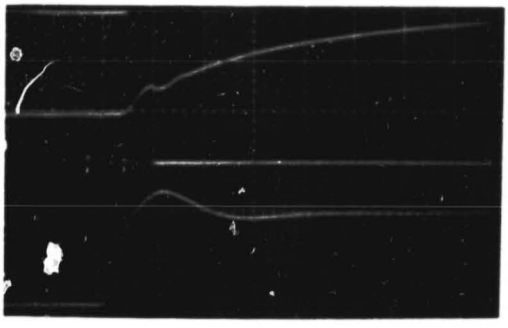
Device # 14-25



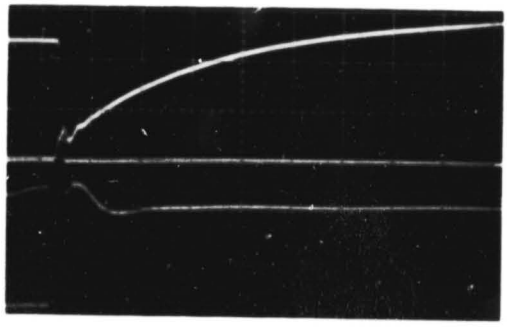
I_C V_{CE} = 100 V/cm
T = 25°C
I_C = 20 A/cm
V_{CE} I_B = 2 A/cm
I_B t = 2 μs/cm

(a)



I_C V_{CE} = 100 V/cm
T = 25°C
I_C = 20 A/cm
V_{CE} I_B = 2 A/cm
I_B t = 1 μs/cm

(b)



I_C V_{CE} = 200 V/cm
T = 25°C
I_C = 20 A/cm
V_{CE} I_B = 2 A/cm
I_B t = 2 μs/cm

(c)

Figure 14. The rate of rise of I_C is independent of V_{CE}, I_C, and I_B

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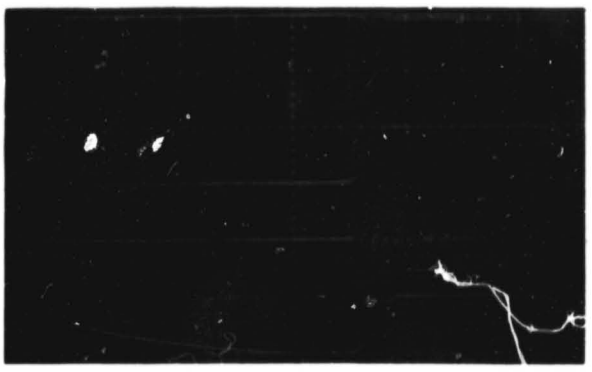
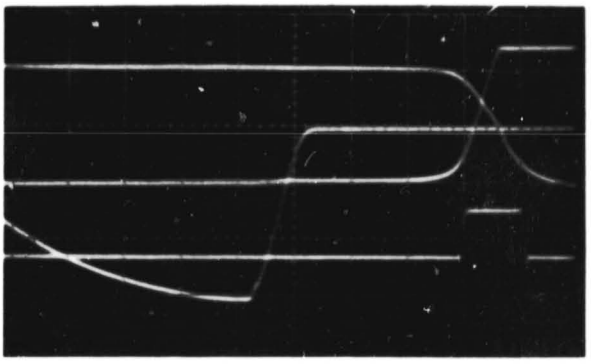
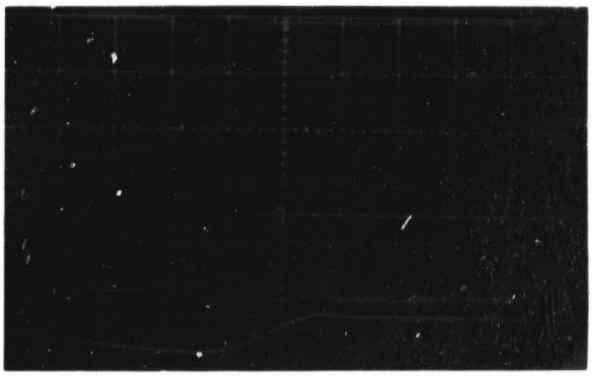
Device 14 – #12



V_{CE} = 100 V/cm
T = 25 °C
I_C = 10 A/cm
I_B = 5 A/cm
t = 2 µs/cm
E = 0.5 V/cm with a
Scale Factor = 5 kVA



V_{CE} = 200 V/cm
T = 25°C
I_C = 10 A/cm
I_B = 2 A/cm
t = 2 µs/cm



V_{CE} = 200 V/cm
T = 25°C
I_C = 20 A/cm
I_B = 10 A/cm
t = 0.5 µs/cm
E = 2.0 V/cm with a
Scale Factor = 5 kVA

Figure 15. Turn-off delay on device 14-#12 as affected by C_{BE}, I_C, and I_B

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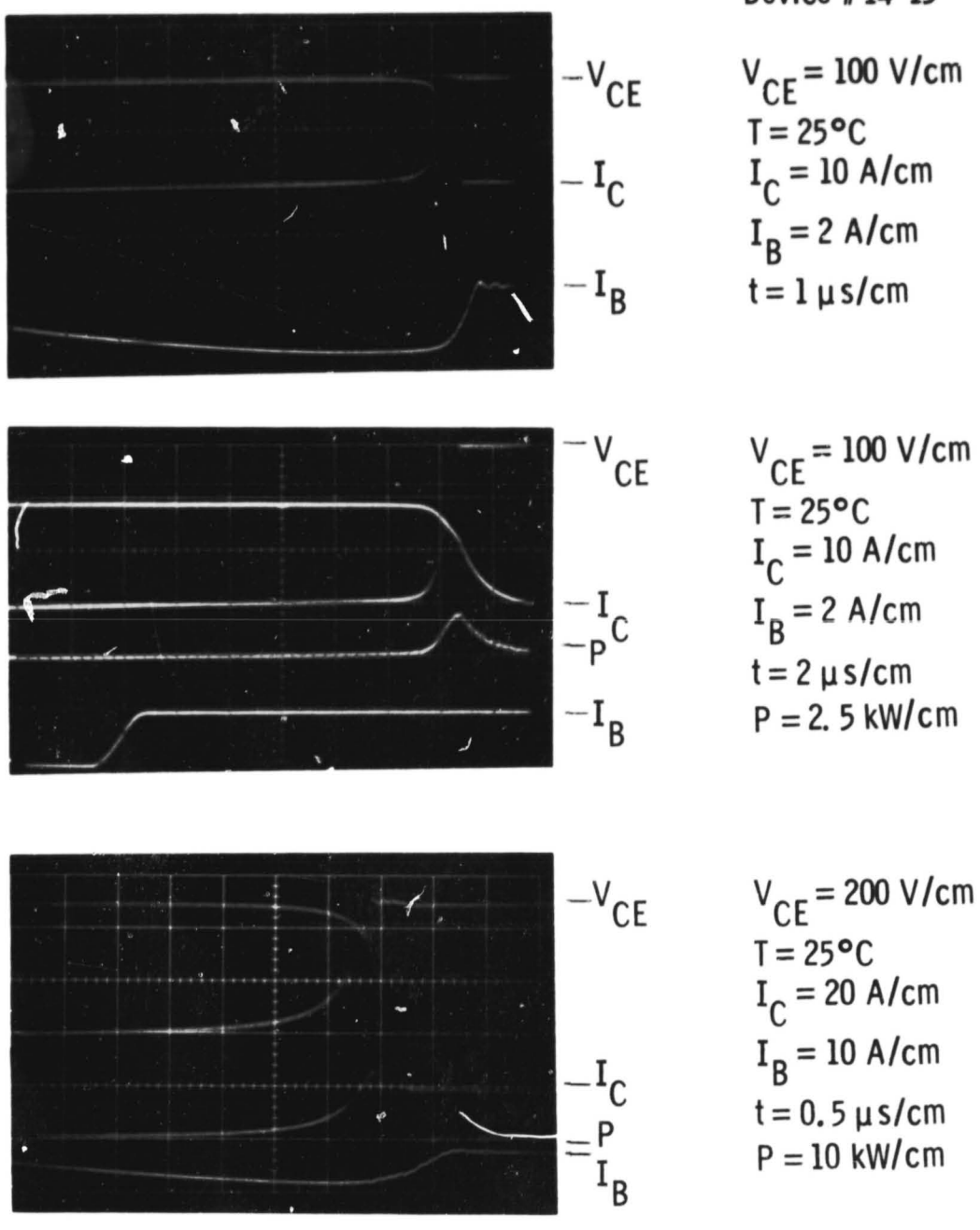

Figure 16. Turn-off delay on device 14-#13 as affected by V_{CE} and I_B

Figure 17 shows the turn-off waveform for device 10/11-#1. The waveforms labelled P and t_g as shown in Figs. 15 to 17 are measurements of the switching-power loss in the turn-off period. The following section describes such measurements in detail.

4.3 Switching Power Loss

Figure 18 shows the block diagram for energy-loss measurement. The pulse waveforms labelled P as shown in Fig. 17(a) and (c) are products of V_{CE} and I_C. During the turn-off period, the gate pulse as shown in Fig. 17(b) is the gate period in which the integration is performed. The dc-volt meter reading gives directly the energy loss during the gate period.

Energy losses were measured at t_g = 2, 3, and 4 μsec. For consistency, the gate shuts off always at the time that the base current ends. As observed in Fig. 17(b) and (c), a 2-μsec gate covers essentially all of the energy loss. Increasing t_g to 3 and 4 μsec only gave a small correction in losses. Figs. 19, 20, and 21 show the measured results on devices 10/11-#1, 14-#39, and 14-#13, respectively. In each figure, (a) shows the turn-off energy loss E_{off} vs. I_C, with V_{CE} as a parameter; (b), E_{off} vs. the reverse base current I_{BR} with I_C as a parameter. Among the devices, 14-#39 has the lowest loss; 10/11-#1 the highest.

4.4 Forward Safe-Operating Area

Figure 22 shows a comparison between the calculated forward safe-operating area (SOA) for different pulse times assuming a single pulse of duration t_p and measured results. The solid lines are the calculated curves obtained by using measured, transient thermal-impedance data together with the criterion that the transistor becomes thermally unstable at a particular junction to case temperature. (The temperature will be a function of I_C and impedance R_E.) Since the transistor must be in a thermally unstable mode for some time before it

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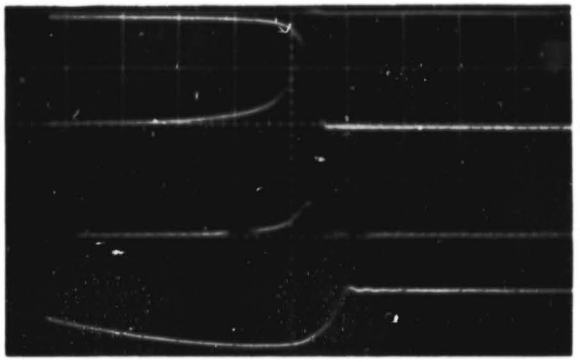
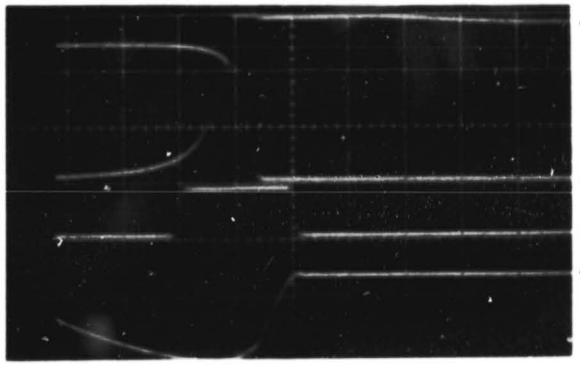
Device # 10/11 - #1



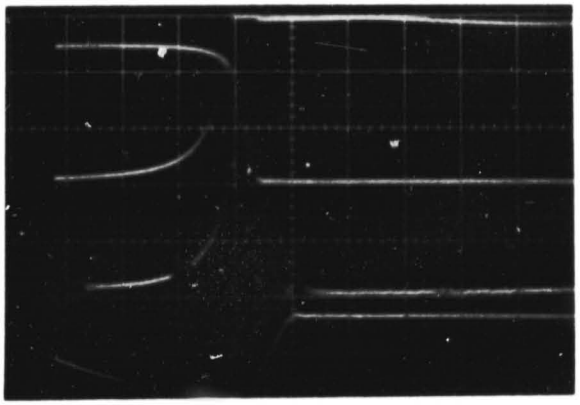
V_{CE} = 100 V/cm
T = 25°C
I_C = 10 A/cm
I_B = 2 A/cm
t = 1 μs/cm
P = 2.5 kW/cm

(a)



V_{CE} = 100 V/cm
T = 25°C
I_C = 20 A/cm
I_B = 5 A/cm I_{B1} = 6 A
t = 1 μs/cm

(b)



V_{CE} = 100 V/cm
T = 25°C
I_C = 20 A/cm
I_B = 5 A/cm
t = 1 μs/cm
P = 2.5 kW/cm

(c)

Figure 17. Turn-off waveforms and power losses measured from device 10/11-#1

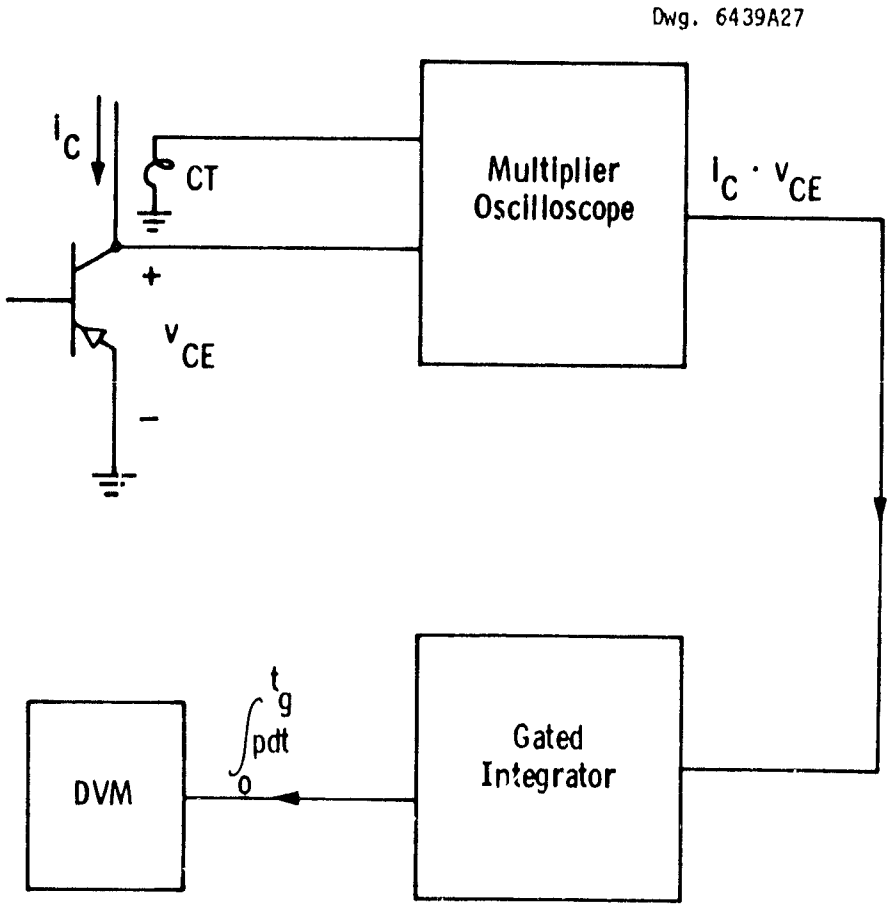


Figure 18. Block diagram for energy-loss measurement

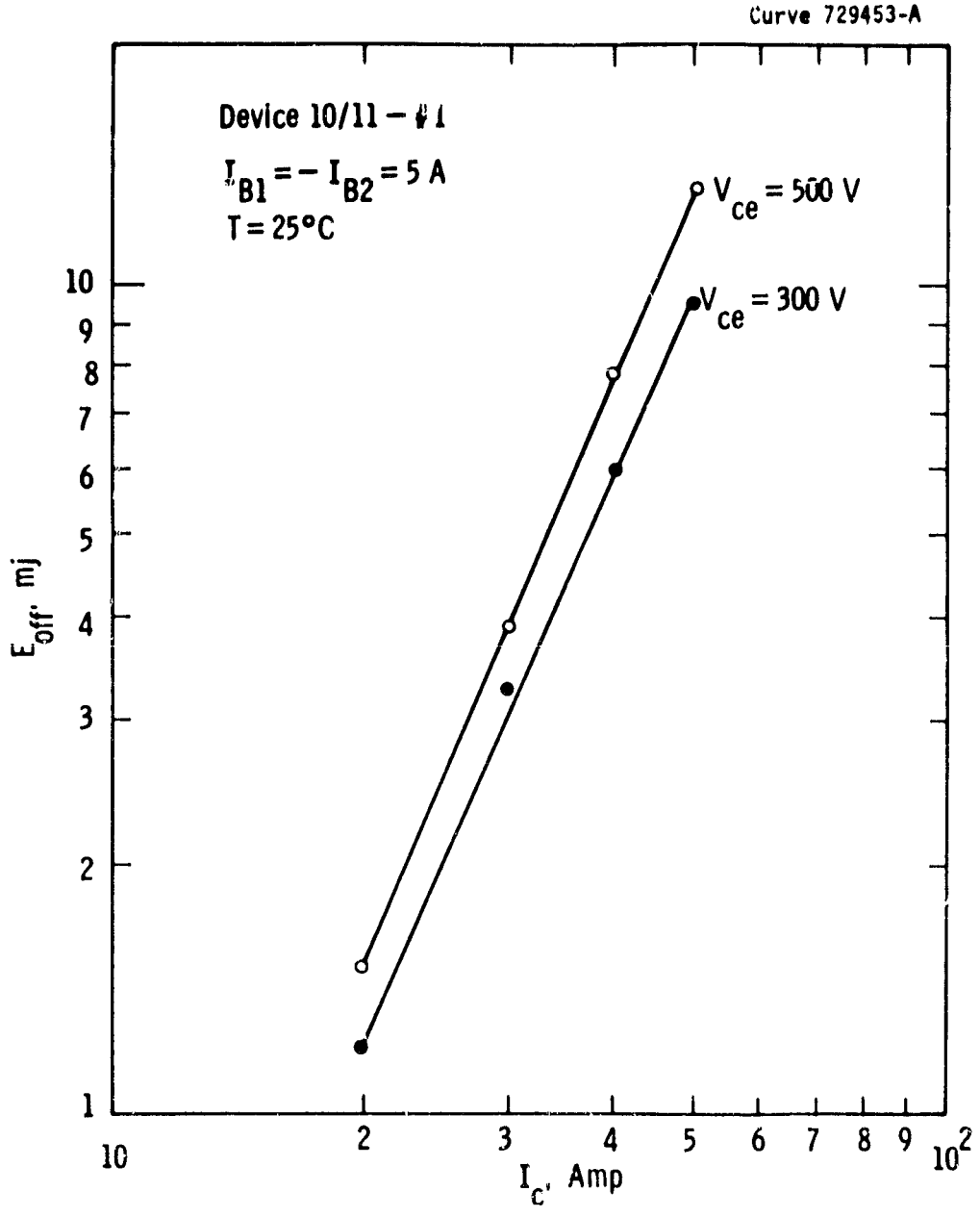


Figure 19(a) E_{off} vs. I_c for device 10/11-#1

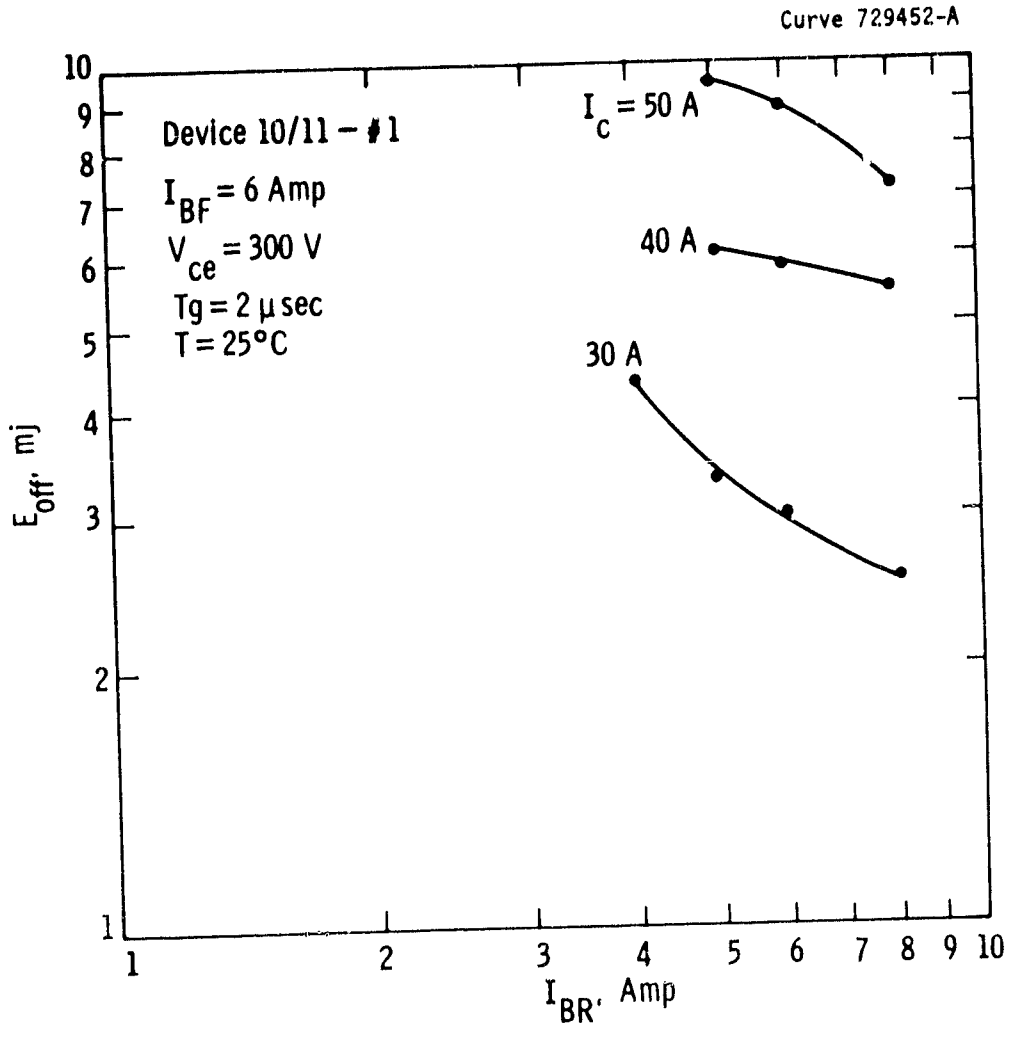


Figure 19(b) E_{off} vs. I_{BR} for device 10/11-#1

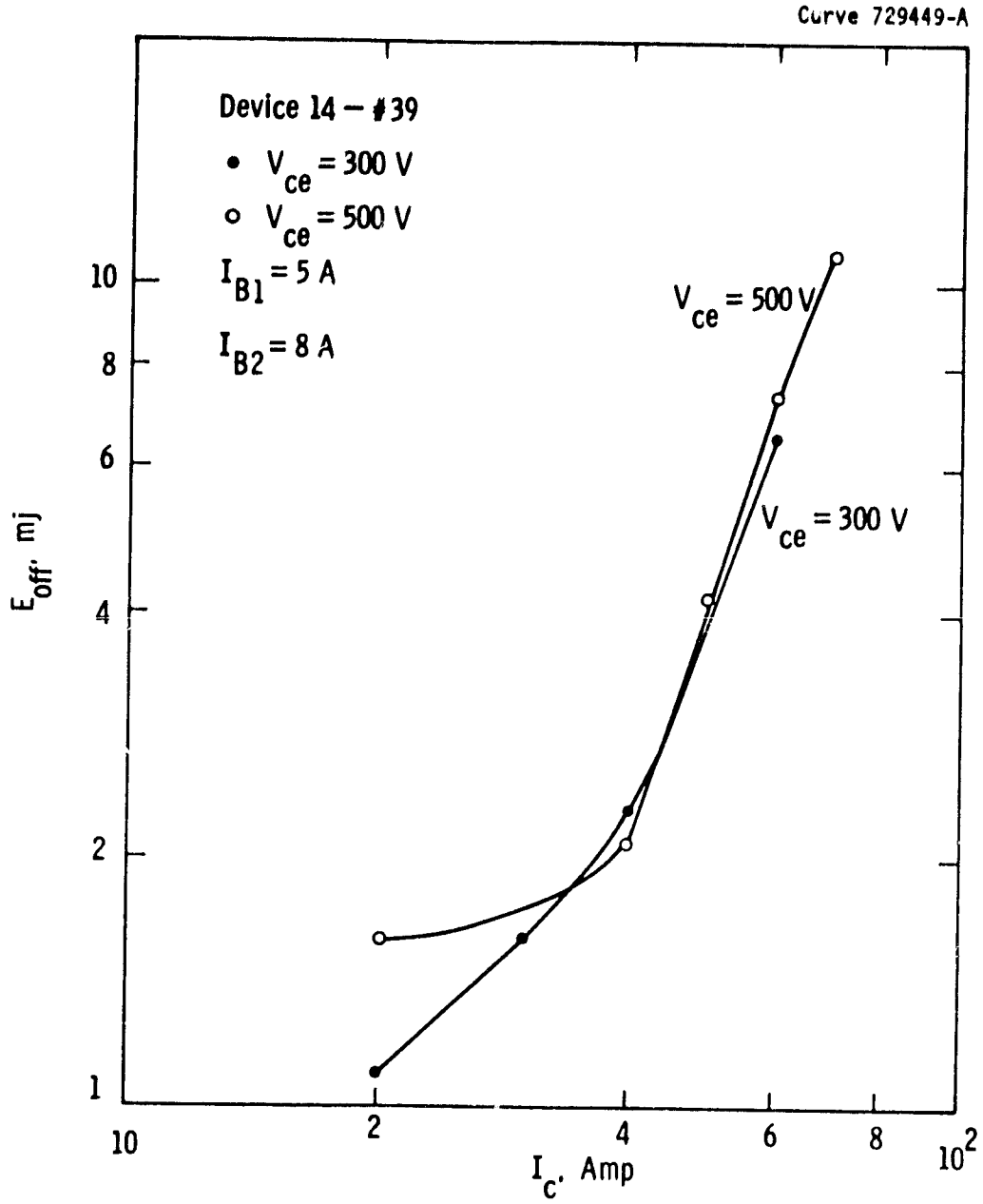


Figure 20(a) E_{off} vs. I_c for device 14-#39

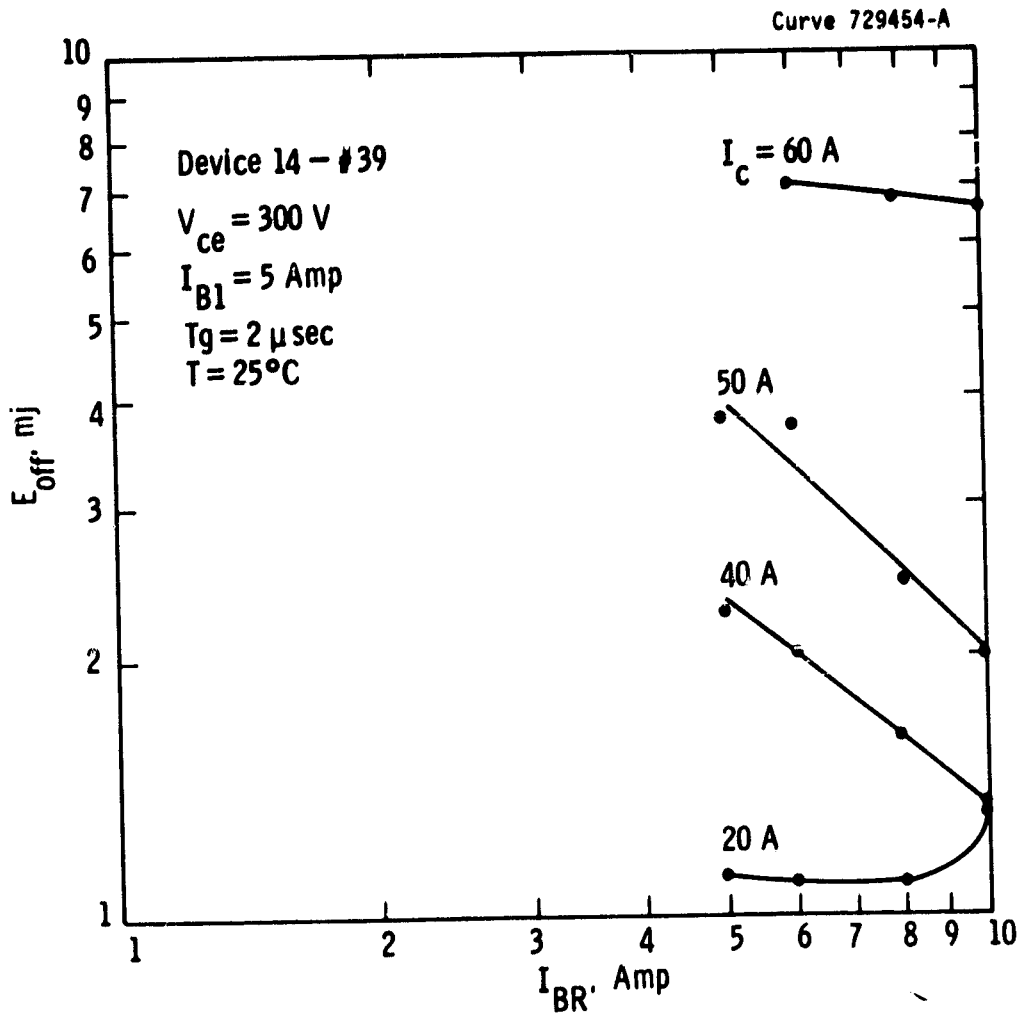


Figure 20(b) E_{off} vs. I_{BR} for device 14-#39

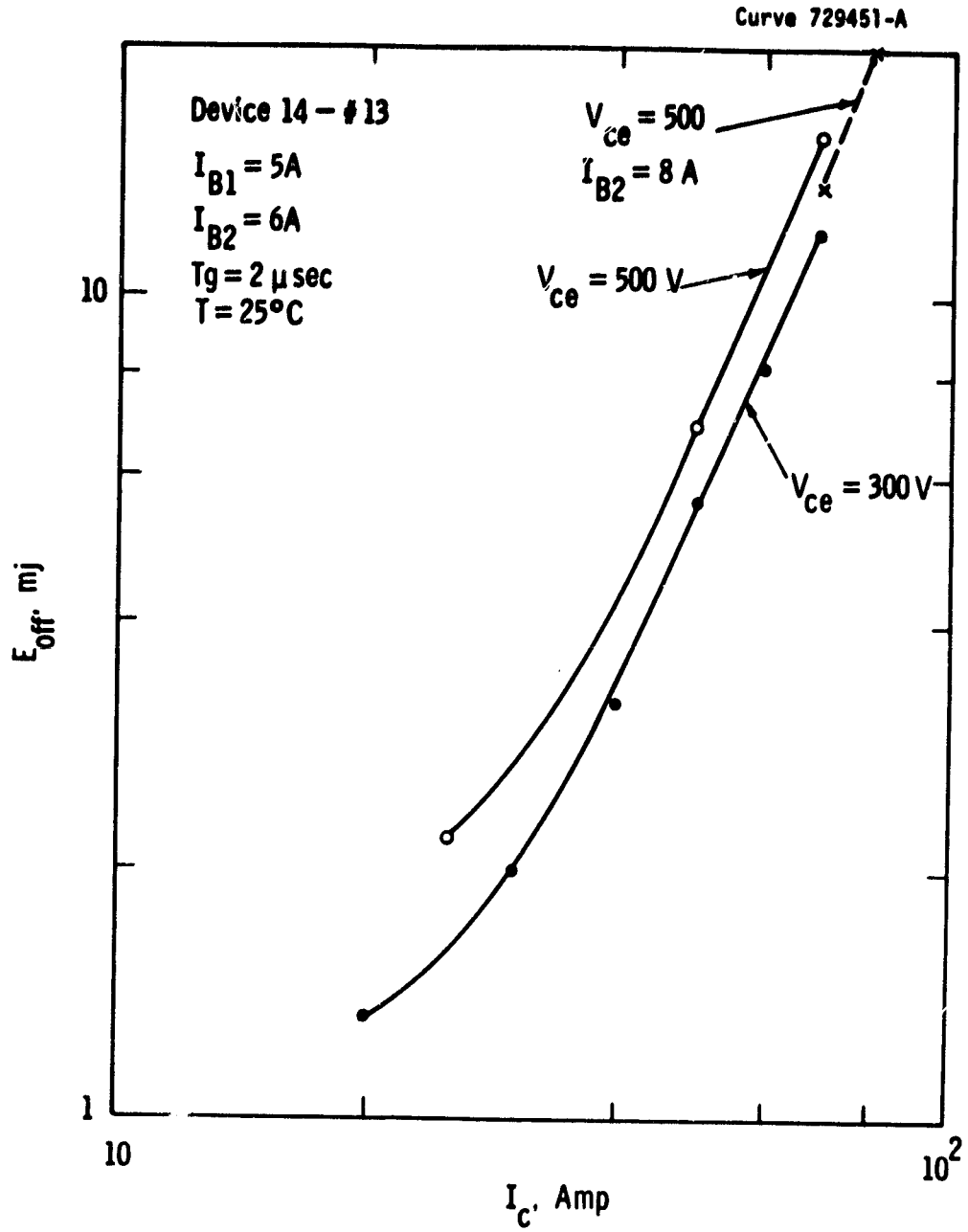


Figure 21(a) E_{off} vs. I_c for device 14-#13

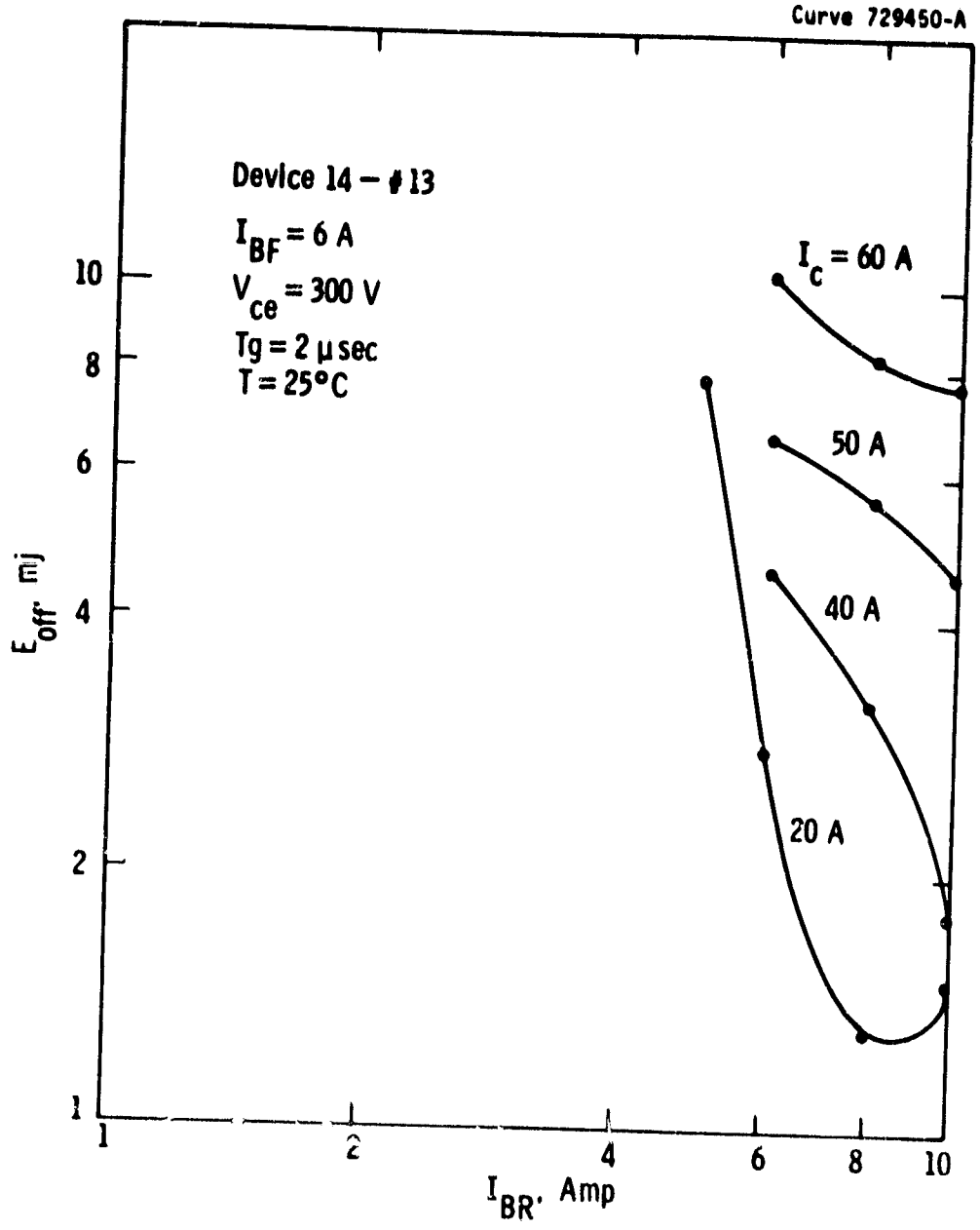


Figure 21(b) E_{off} vs. I_{BR} for device 14-#13

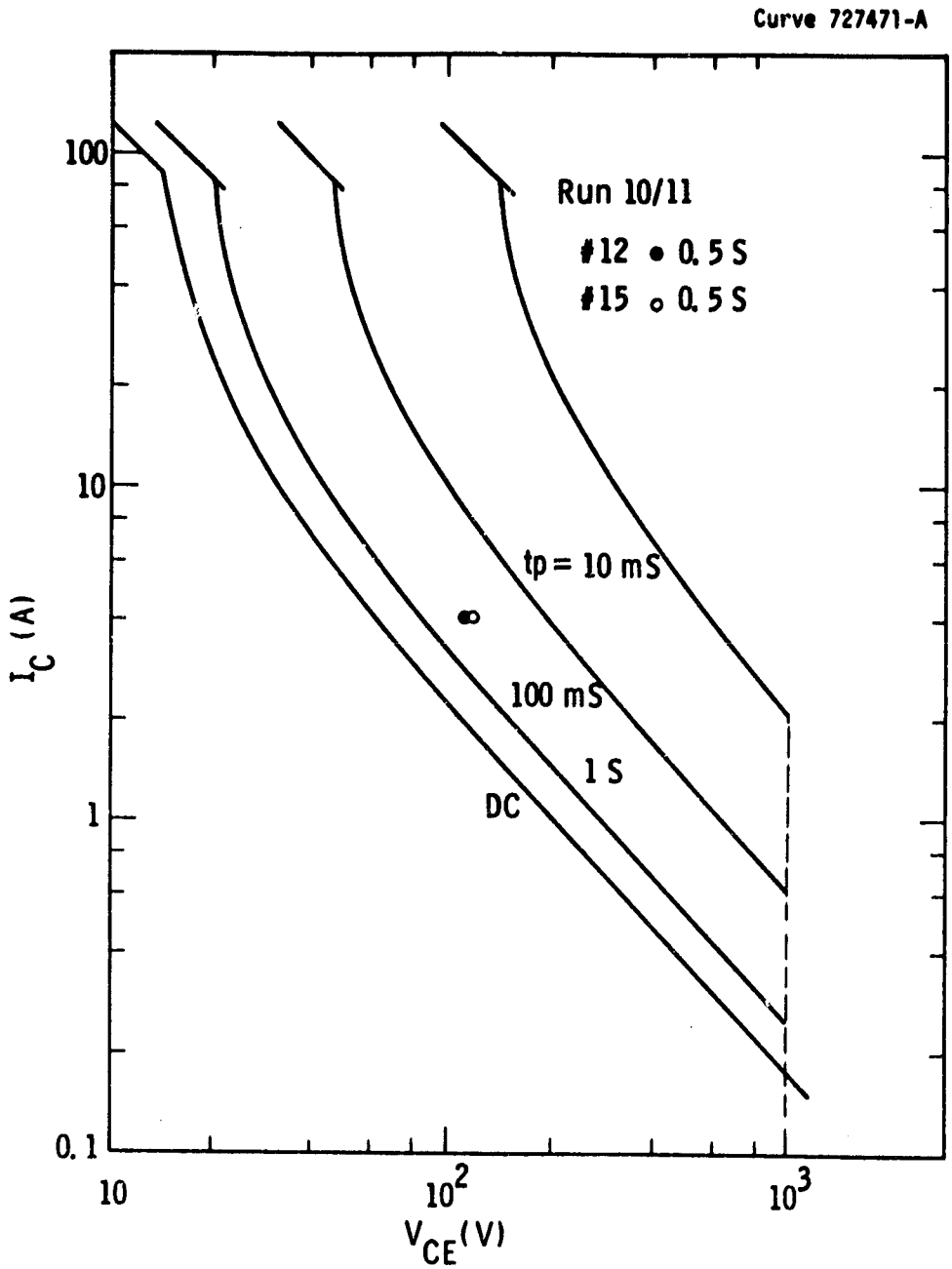


Figure 22. A comparison of calculated and measured forward SOA

reaches second breakdown, these predictions will be conservative for short pulse times, e.g., $t_p \leq 1$ ms. The dot and the circle in Fig. 22 are the measured results at the onset of thermal instability for devices 10/11-#12 and 10/11-#15, respectively. Devices went into second breakdown after thermal instability, i.e., they did not show stable hot spots. Measurements for both devices agree well with theory.

5. APPLICATIONS

Earlier this year, six devices from run 10/11 were sent to Westinghouse AED, Lima, Ohio, for experimental work on the NASA Remote-Power Controller program. Devices are operated in a circuit with a normal load of 25 amperes at 900 volts. In transient, when switching off a short circuit into a 900-volt blocking condition, devices may carry currents up to 150 to 200 amperes for a few μsec. With proper circuit protection, devices functioned adequately in such applications. However, after a period of time, all six devices were destroyed when operated under conditions without protective circuits.

Earlier, one (or two) device was destroyed under normal operating condition. It was not known that during the turn-off period, without voltage applied, the turn-off time was as long as 100 μsec. It was speculated that such long turn-off time was responsible for over-heating the device. This problem has been rectified by applying voltage (4 to 5 volts) at the collector during the turn-off time. With applied voltage to sweep out the carriers, the observed turn-off time was down to 10 μsec.

Subsequently, another six units from run 14 were sent to AED. These devices have been functioning satisfactorily for this application.

6. SUMMARY AND CONCLUSION

We have successfully demonstrated our ability to fabricate transistors with $V_{CEO(sus)}$ in the range between 900 to 1200 volts and with current-gain products in the range between 200 and 400 amperes. Starting with the process developed under contract NAS3-18916, improvements have been made in controlling the electric field at the surface and in preserving the lifetime in the collector region. With these improvements, we have obtained devices with V_{CBO} as high as 1800 volts and lifetimes as high as 100 μsec. We are confident that these improvements can be applied to 1200-volt, 200-ampere transistors on 50-mm diameter fusions.

We have fulfilled the contract requirements. A total of 50 prototype transistors that meet the target specifications have been delivered to NASA. A complete listing of test results is contained in Appendix C, Table C-1 and Table C-2. In addition, we have supplied transistors to AED, Lima, for the experimental work on NASA's Remote-Power Controller Program. These devices have been functioning satisfactorily in the breadboard circuit.

7. REFERENCES

1. P. L. Hower, "Optimum Design of Power Transistor Switches," IEEE Trans. on Elect. Dev. ED-20, 1973 pp. 426.

2. P. L. Hower, "High-Current, Fast-Switching Transistor Development," Final Report, NASA Contract NAS3-21380.

3. R. J. Whittier and D. A. Tremere, "Current Gain and Cut-Off Frequency Fall-Off at High Currents," IEEE Trans. on Elect. Dev. ED16, 1969, pp. 39.

APPENDIX A

TABLE A-1 - TARGET SPECIFICATIONS FOR HIGH-VOLTAGE POWER-SWITCHING TRANSISTORS

	Symbol	Characteristics with Test Conditions	RFP Value	Proposed Value	Units
1.	V_{CEO} (sus)	Collector-emitter Sustaining Voltage at I_C = 200 mA, I_B = 0, 300 µs pulse	1000 min 1200 max	Same as RFP	V V
2.	V_{CBO}	Collector-base Voltage at I_C = 200 mA	$\geq V_{CEO}$(sus)	Same as RFP	V
3.	$h_{FE}I_C$	Max Gain-Collector Current Product at V_{CE} = 2.5 V			
		• V_{CEO}(sus) = 1000 V	360	Same as	A
		• V_{CEO}(sus) = 1200 V	235	RFP	A
4.	I_B	Max Base Current			
		• Pulsed (<2% duty cycle)	40	Same as	A
		• Continuous dc	20	RFP	A
5.	I_C (peak)	Max Collector Current, pulsed at V_{CE} = 2.5 V			
		• V_{CEO}(sus) = 1000 V	120	150	A
		• V_{CEO}(sus) = 1200 V	80	100	A
6.	I_C (continuous)	Max Collector Current, continuous at V_{CE} = 2.5 V			
		• V_{CEO}(sus) = 1000 V	60	Same as	A
		• V_{CEO}(sus) = 1200 V	40	RFP	A
7.	h_{FE}	Direct current gain for V_{CEO} (sus) = 1000 V • I_C = 30 A, V_{CE}=2.5V	12		
8.	h_{FE}	Direct current gain for V_{CEO} (sus) = 1200 V • I_C = 20 A, V_{CE}=2.5V	12		
9.	V_{CE} (sat)	Collector-emitter Saturation Voltage at I_C = 20 A, I_B = 2 A	1.0		V
10.	V_{BE} (sat)	Base-emitter Saturation Voltage at I_C = 20 A, I_B = 2 A	1.2		V
11.	$R_{\theta JC}$	Thermal Resistance Junction to Case	0.1		°C/W
12.	P_T	Power Dissipation at Case Temp., T_C = 75 °C	250		W
13.	T_J	Operating and Storage Junction Temp. Range	-50 to 200		°C
14.	t_D*	Turn-on Delay	0.1		µs
15.	t_r*	Rise Time (10 to 90% I_C)	0.5		µs
16.	t_s*	Storage Time	2.5		µs
17.	t_f*	Fall Time (90 to 10% I_C)	0.5		µs
18.		Operating environment	Typical Space Vacuum and Zero "g"		
19.		Non-operating Survivability	Typical Spacecraft Launch Shock and Vibration		

*All switching times measured with resistive load, supply voltage, V_{CC} = 200 V, I_C = 20 A, I_{B1} = I_{B2} = 2A using 100 µs pulses with duty cycle <2%.

APPENDIX B

TABLE B-1 - PROCESS FLOWCHART WITH BORON DIFFUSION

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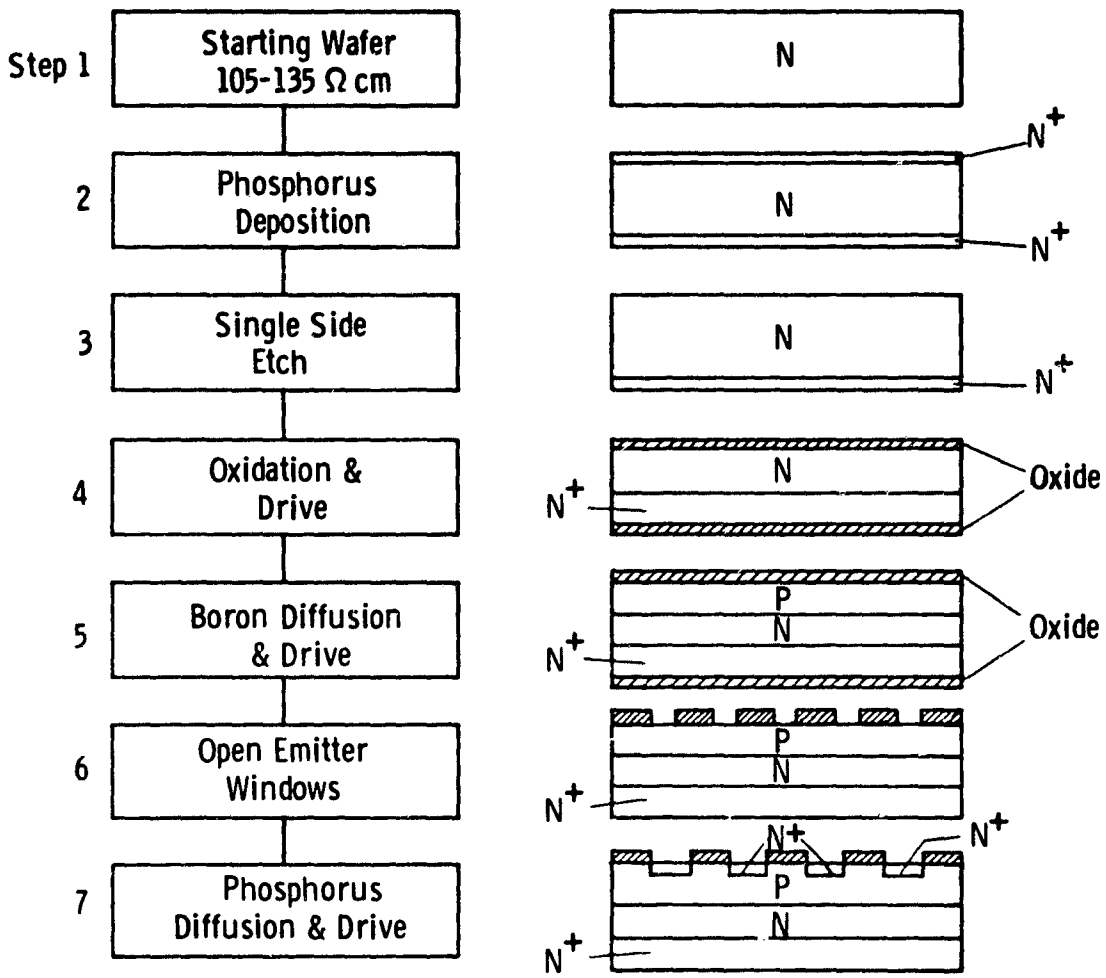
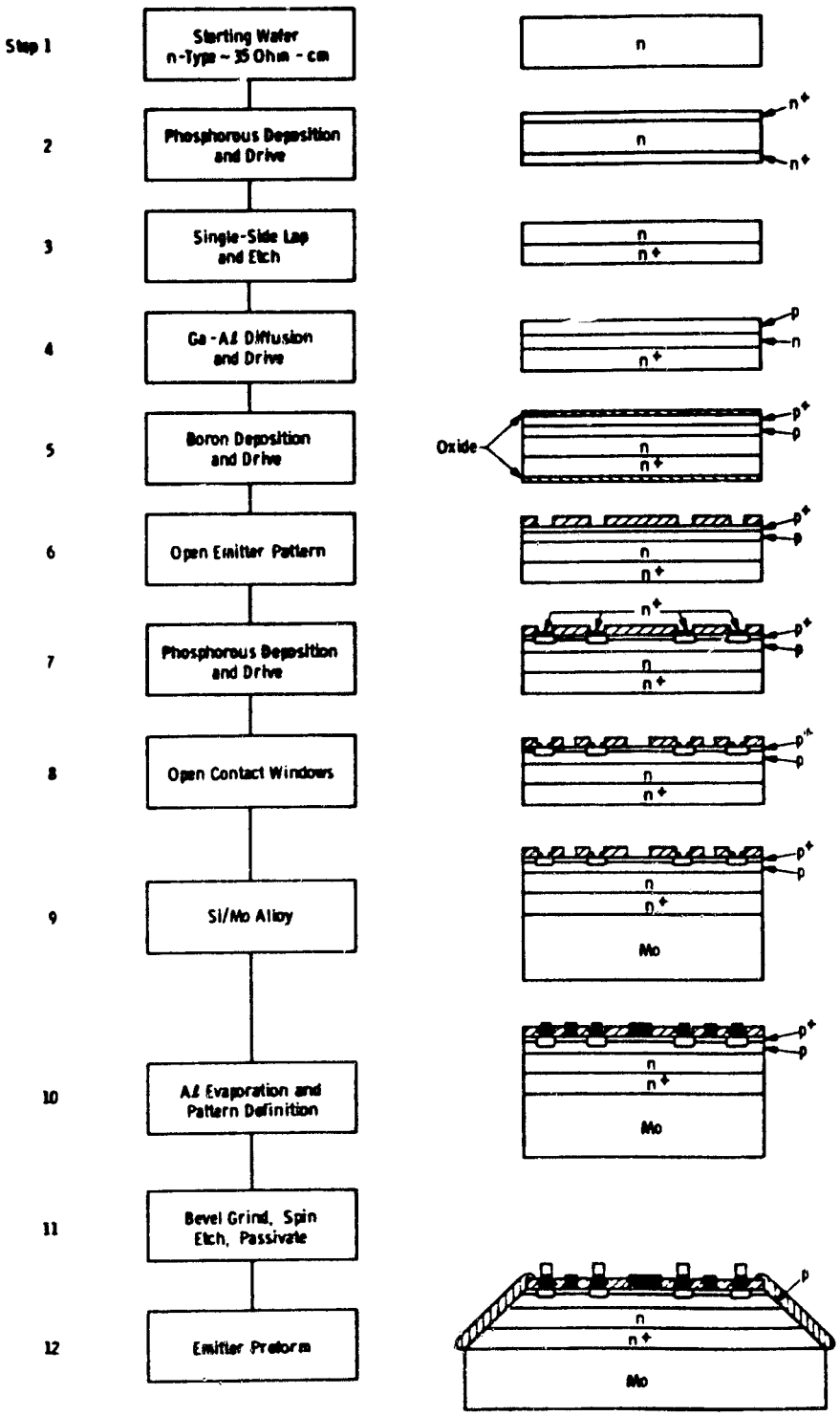


Note: Remaining steps same as steps 8 to 12 as shown in Table B-2

APPENDIX B

TABLE B-2 - PROCESS FLOWCHART DEVELOPED UNDER CONTRACT NAS3-18916



APPENDIX C

TABLE C-1 - TEST RESULTS ON UNITS FOR RUN 10/11

No.	Lifetime (sec)	Packaged 25° (Volts)	$V_{CEO(sus)}$ (Volts)	I_B @ I_C = 40A†	50A†	60A†	Remarks
11	38	2270	975	5.5	8.3	11.8	
12	40	595	975	6.0	9.0	12.9	Lima
13	33	1520	1000	8.2	11.9	16.7	
14	40						Broke down
15	18	1080	1050	13.7	22.2	31.1	Lima
16	48	1590	1040	7.4	10.8	15.2	Lima
17	36	1550	1000	6.5	9.7	13.8	Lima
21	43	1260	1020	9.9	15.8	23.0	
22	34	1390	1000	6.9	10.9	16.0	
23	41	1650	1050	9.5	15.2	21.2	
24	45	1710	1075	8.2	12.3	17.7	
25	70	1740	1060	7.5	11.2	16.1	
26	34	1320	1050	10.6	16.2	23.0	
27	42	1320	1050	10.9	16.4	23.6	
28	36	1410	1050	12.1	18.6	26.5	
29	36	1470	1050	10.0	15.1	22.0	
30	41	1720	1050	10.2	15.7	22.8	
31	22	1240	1050	13.7	21.6	30.2	
32	42	1300	1050	8.5	12.8	18.4	
1	39	(Shakey) 900V/2.5 mA	1150	8.9	12.8	1.84	
2	29	1125V/.25 mA	1240	9.8	12.9	18.4	
19	30	1160V/.5 mA	1210	6.1	9.0	12.9	
20	45	1070V/.5 mA	1150	5.1	7.7	10.7	

†V_{CG} = 2.5V

TABLE C-2 - TEST RESULTS ON UNITS FOR RUN 14

Unit Number	τ	I_B @ I_C = 30A	40A	50A	75A	V_{CEO}(sus)	V_{CBO}	Packaged	V_{EBO}	h_{FE}
5	74 µs	1.8	2.9	4.2		969V	1370V/.5 mA	✓	7V/25 mA	25
7	54 µs	2.1	3.3	4.9		951V	1000V/8.0 mA	✓	7V/0	25
10	77 µs	1.7	2.8	4.2		925V	1200V/2.5 mA	✓	7V/0	24
11	66 µs	1.6	2.5	3.8	7.8	969V	1200V/1.0 mA	✓	7V/40 mA	28
12	80 µs	1.8	3.0	4.5		1010V	1250V/2.5 mA	✓	7V/90 mA	26
15	86 µs	1.7	2.7	4.0		959V	1220V/2.5 mA	✓	7V/60 mA	24
21	61 µs	1.6	2.6	4.0		937V	1050V/1.1 mA	✓	7V/40 mA	27
LIMA 22*	74 µs	1.7	2.5	3.7		882V	1000V/7 mA	✓	7V/50 mA	30
14-1	79 µs	2.1	3.4	4.9		968V	1280V/.25 mA	✓	7V/0	15
14-2	73 µs	1.7	2.7	4.1		935V	1360V/.25 mA	✓	8V/.5 mA	22
14-5	73 µs	1.7	2.8	4.1		943V	1400V/.5 mA	✓	7V/3 mA	28
14-6	68 µs	1.4	2.4	3.6		870V	1280V/.25 mA	✓	7V/0	34
14-8	83 µs	1.7	2.8	4.2		948V	1330V/.25 mA	✓	7V/0	26
14-9	83 µs	1.8	2.8	4.1		947V	1400V/.25 mA	✓	7V/20 mA	22
14-10	85 µs	1.5	2.4	3.6		944V	1310V/.25 mA	✓	8V/0	28
14-12	100 µs	1.7	2.7	4.0		929V	1290V/.25 mA	✓	8V/0	23
14-13	100 µs	1.5	2.5	3.6		956V	1400V/.6 mA	✓	7V/20 mA	24
14-14	61 µs	1.7	2.9	4.3		914V	1270V/1 mA	✓	7V/30 mA	23
14-15	85 s	1.7	2.9	4.4		943V	1430/.5 mA		9V/0	26

*V_{CG} = 2.5V

Unit Number	τ	I_B @ I_C = 30A†	40A†	50A†	75A	V_{CEO}(sus)	V_{CBO}	Packaged	V_{EBO}	h_{FE}
14-16	84 µs	1.7	2.8	4.1		956V	1360V/.25 mA	✓	7V/0	24
14-17	90 µs	1.5	2.7	4.0		982V	1360V/1.0 mA	✓	7V/30 mA	24
14-18	76 µs	1.9	3.0	4.4		968V	1400V/2.0 mA	✓	7V/0	24
14-19	69 µs	1.8	2.9	4.3		956V	1250V/5.0 mA	✓	8V/0	24
14-24	105 µs	1.7	2.7	4.0		961V	1280V/2.5 mA	✓	7V/0	20
14-29	87 µs	1.6	2.8	4.4		935V	1350V/.5 mA	✓	7V/1 mA	27
14-31	103 µs	1.8	3.0	4.3		940V	1300V/.5 mA	✓	7V/0	20
14-32	41 µs	3.0	4.7	7.0		1024V	1400V/2.5 mA	✓	9V/0	19
14-33	81 µs	1.7	2.7	4.0		910V	1320V/2.5 mA	✓	8V/0	26
14-34	71 µs	2.0	3.1	4.6		961V	1350V/.5 mA	✓	9V/0	28
14-35	63 µs	1.9	2.9	4.3		961V	1360V/.5 mA	✓	9V/0	26
14-36	55 µs	2.0	3.2	4.7		993V	1440V/.5 mA	✓	7V/1 mA	20
14-37	87 µs	1.5	2.5	3.6		956V	1440V/.5 mA	✓	8V/0	32
14-39	55 µs	2.1	3.3	4.9		936V	1350V/.5 mA	✓	7V/2 mA	19
14-40	61 µs	1.7	2.6	3.9		903V	1200V/5.0 mA	✓	7V/0	30
14-41	69 µs	2.0	2.9	4.4		953V	1250V/2.5 mA	✓	9V/0	33
14-43	65 µs	2.2	3.3	4.9		955V	1290V/2.5 mA	✓	7V/0	22

†V_{CG} = 2.5V

ACKNOWLEDGEMENTS

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