16 X 16 ELEMENT EXTRINSIC SILICON DETECTOR ARRAY

CONTRACT NAS2 - 10792

PREPARED FOR

NASA AMES RESEARCH CENTER
MOFFETT FIELD, CA 94035

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1. GENERAL INFORMATION

This section contains general information concerning two long wavelength infrared (LWIR) focal planes equipped with mosaic arrays featuring 16x16 detector elements, and an associated electronics unit that is required to operate the devices. Included are descriptions of the focal plane configurations and of the electronics unit.

1.1 System Description

An LWIR detection system is created by interconnecting either of the two focal plane assemblies (FPAs) with the electronics unit as shown schematically in Figure 1.1. The on-focal plane scanning electronics chips are controlled by timing signals generated by the electronics unit, and a wide range of sample or frame rates can be obtained by using the internal or an external clock.

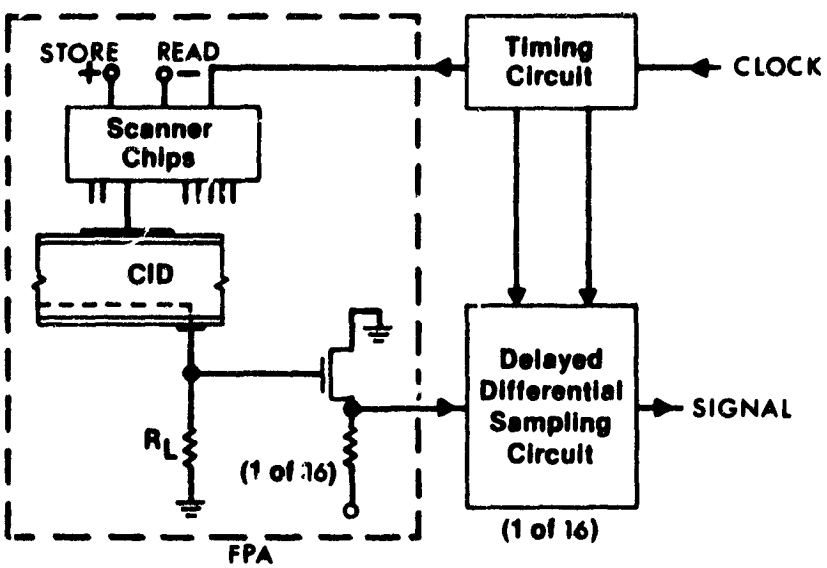


Figure 1.1 System configuration

The outputs from on-focal plane pre-amplifiers (source followers) are processed by correlated double sampling (CDS) circuits contained within the electronics unit; the CDS signal processing scheme is also referred to as delayed differential sampling.

The system is energized by a low-voltage power supply mounted inside the electronics unit, and it is operated from a standard 110V/60 Hz source.

1.2 Focal Plane Descriptions

The focal planes both consist of a 16x16 element bismuth-doped silicon charge-injection-device (CID) array, scanning electronics chips to control the CID readout, 16 low-noise MOSFET source followers (one for each row output), and a resistance thermometer.

The detector array configuration is shown in Figure 1.2. A 16x16 element CID (MOS capacitor) is obtained by implanting 16 transparent strip electrodes (row electrodes) on the front surface of a Si:Bi wafer, and placing 256 square ($5x5\ mil^2$) aluminum contacts on top of an approximately 2,000 angstrom units thick oxide layer on the rear wafer surface. These contacts, as indicated in the figure, are interconnected along columns.

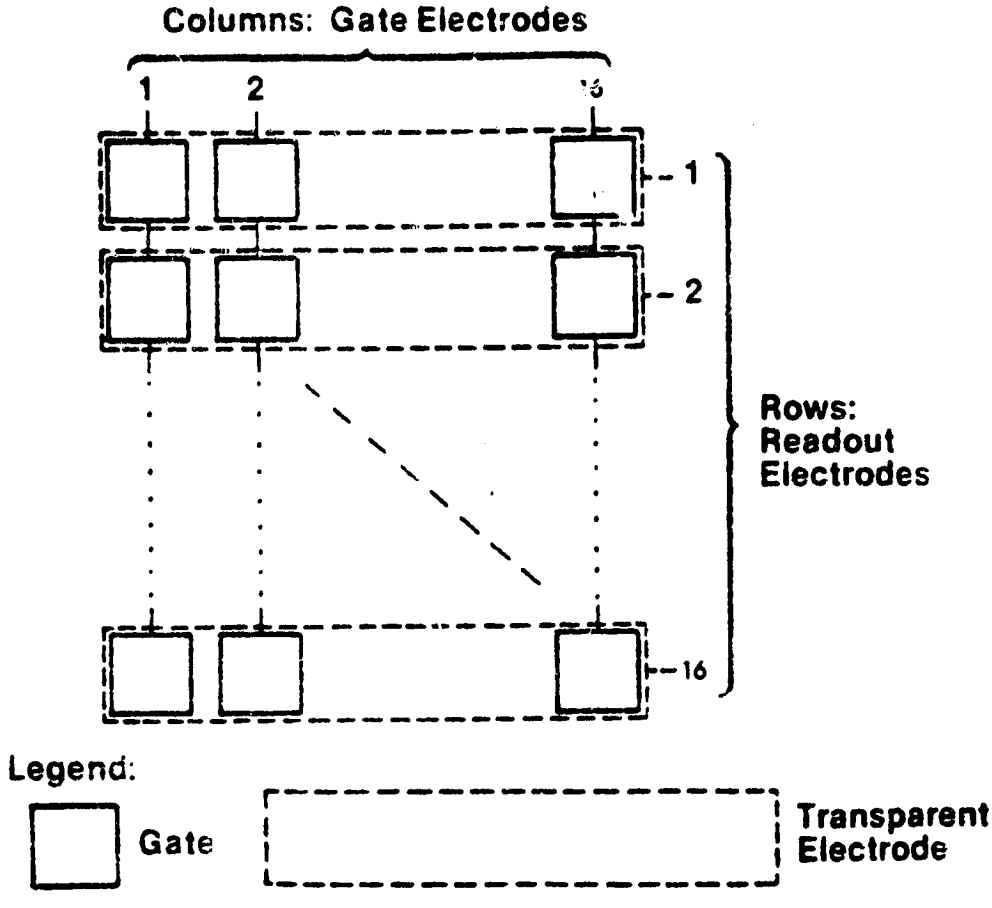


Figure 1.2 16x16 element CID array configuration

In addition to the contact pads (gate contacts), the rear surface also contains a guard ring structure in the form of a conductive trace which surrounds the gate contacts and serves to delineate the effective size of a detector element by shaping the internal electrical field distribution. The overall geometry of the rear surface configuration is sketched in Figure 1.3, and details of the transparent electrode strips are presented in Figure 1.4.

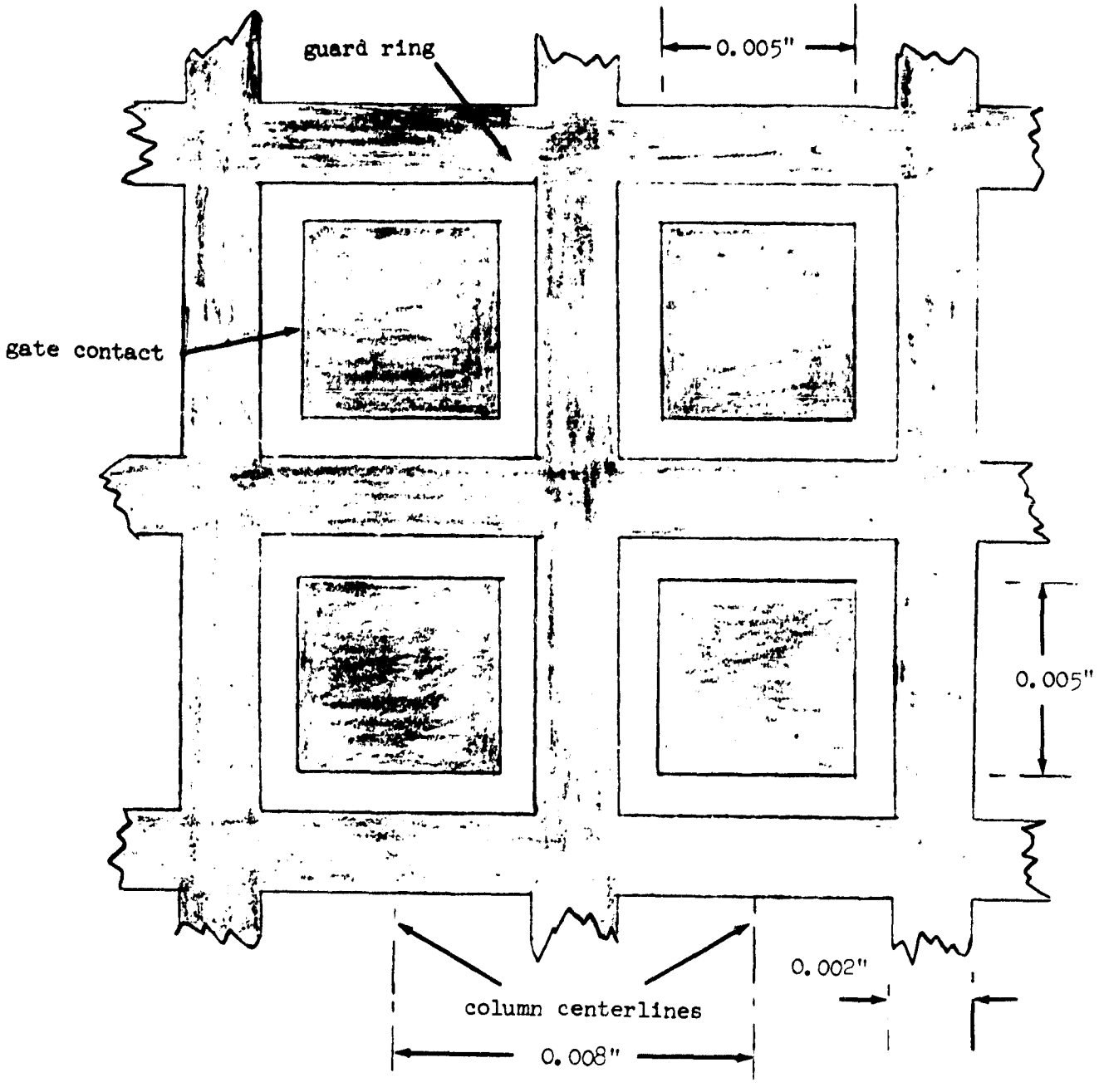


Figure 1.3 Rear surface electrode geometry

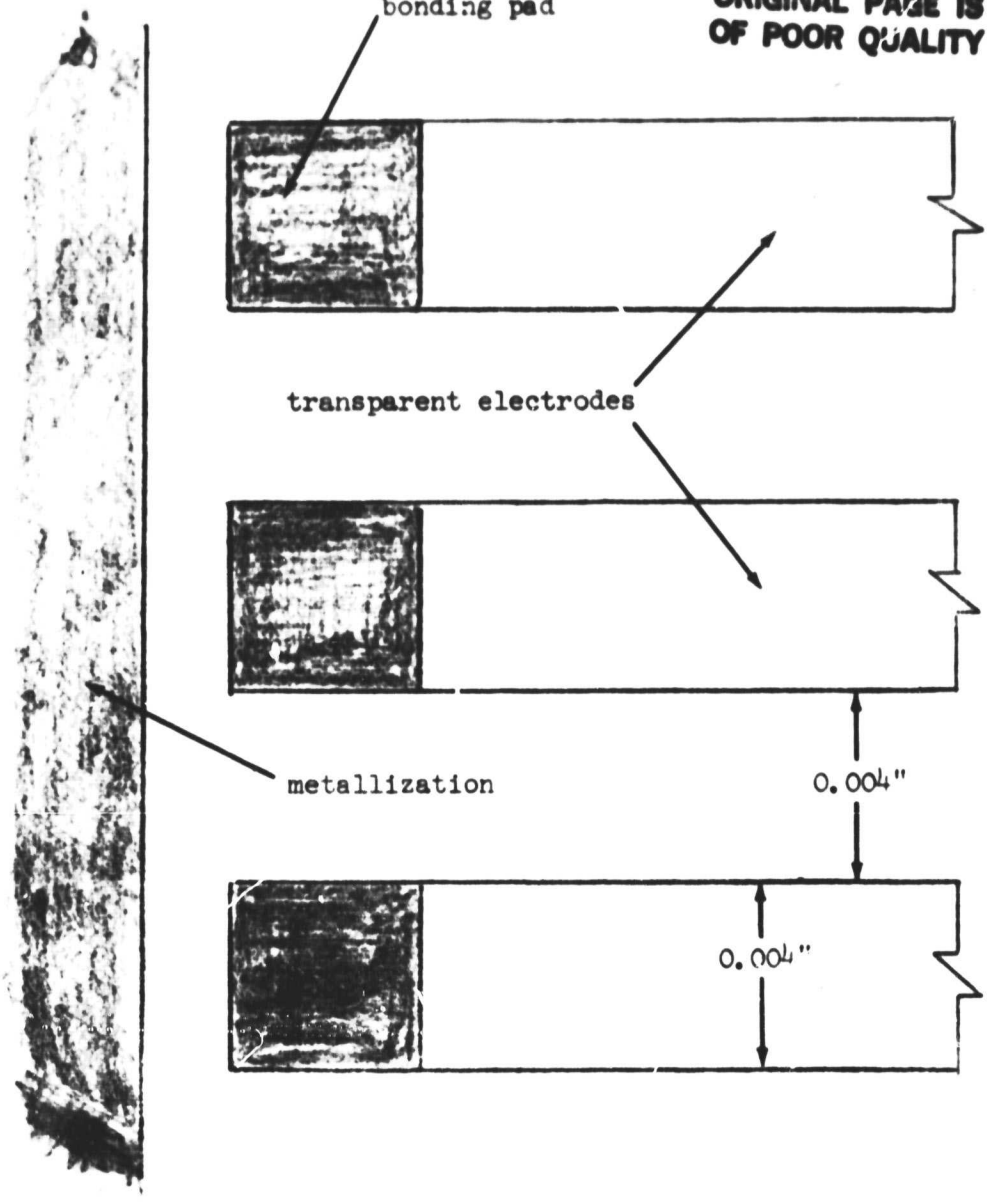


Figure 1.4 Transparent electrode geometry

The hook-up of the scanning electronics which consists of two chips is shown in Figure 1.5. The read (V_{ss}) and store (V_{cc}) voltages are generated by the electronics unit, and they may be adjusted for optimum system performance.

The gates of the 16 MOSFET source followers are connected to individual transparent electrode bonding pads.

Each FPA is equipped with a calibrated Allen-Bradley resistance thermometer.

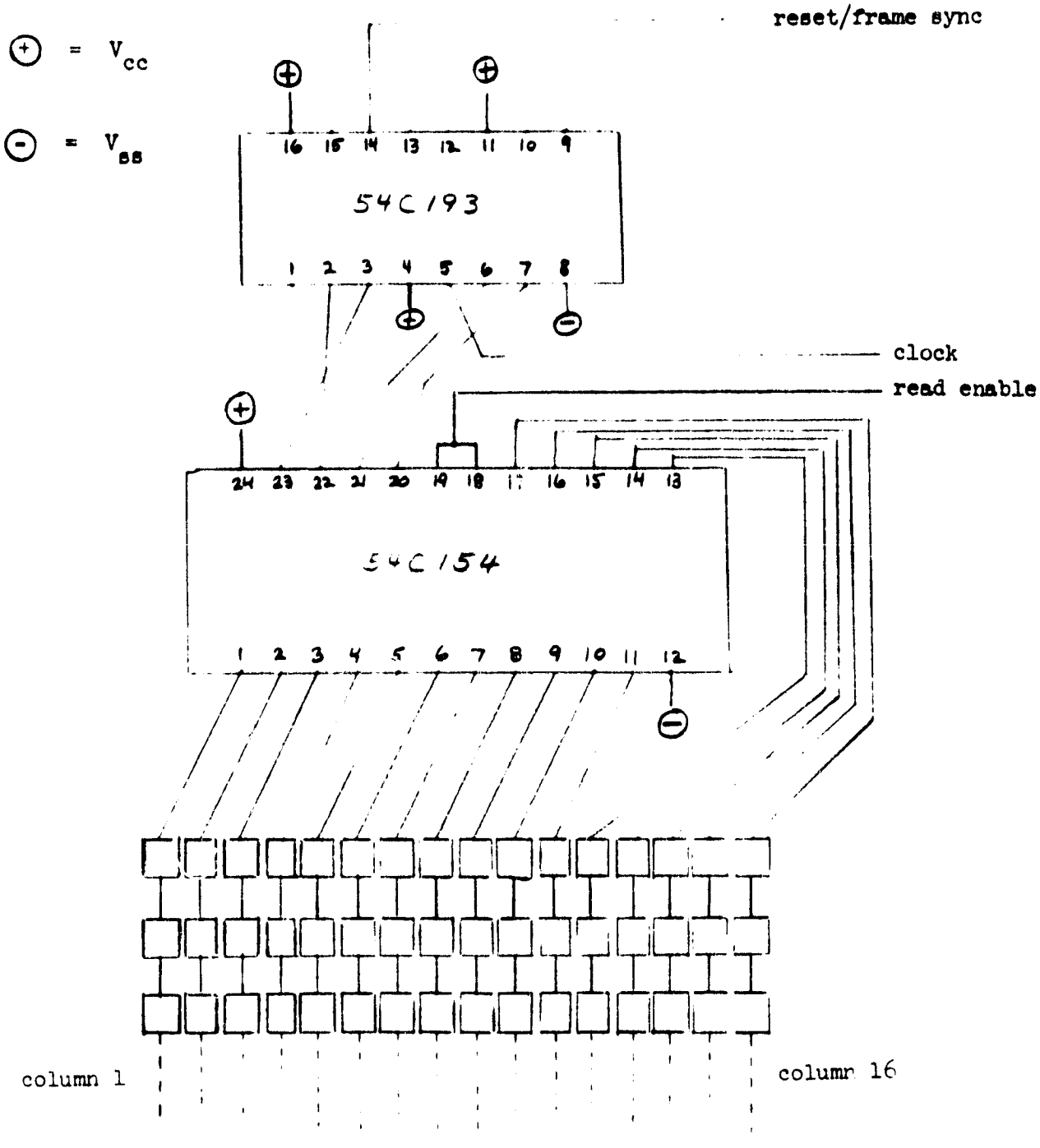


Figure 1.5 Hook up of focal plane scanner chips

Calibration data for these thermometers are given in Appendix A.

The two focal planes are identified as Unit #1 and Unit #2. The manner in which Unit #1 is packaged is indicated in Figure 1.6 along with information on pin connections. The unit consists of two conventional flatpacks mounted back-to-back. One flatpack houses the scanner chips, and the other flatpack contains the 16x16 element detector array, the 16 MOSFET source followers and associated 40 MΩ load resistors (distributed with eight MOSFETs on either side of the array), and the resistance thermometer. The terminals identified as row A and row B are connected to the transparent electrodes adjacent to the row 1 and row 16 electrodes, respectively. The terminals for the resistance thermometer have not been identified in the figure, but they may be easily determined by visual examination of the unit.

The packaging configuration of Unit #2 is completely different from that of Unit #1. Figure 1.7 shows that the array, the scanner chips, and the MOSFET/load resistor combinations in two groups of eight are mounted in individual flatpacks which in turn are mounted on a one-quarter inch thick, circular aluminum disk equipped with a 191 ohm heater. Figure 1.7 also provides the unit's pin connections. The terminals identified as row A and row B are connected to the transparent electrodes adjacent to the row 1 electrode, such that row A corresponds to "row 0" and row B corresponds to "row -1". Similarly, the row C terminal is connected to the transparent electrode adjacent to the row 16 electrode.

1.3 Description of Electronics Unit

The electronics unit provides timing pulses, signal processing, and supply voltages, thereby creating a stand-alone unit for most applications. The unit also features a frequency counter used to measure frame rates and a multi-meter, both of which are built-in. Furthermore, it is constructed using a conventional circuit card cage that is attached to a standard 19 inch wide rack panel.

The layout of the unit's front and rear panels is shown in Figures 1.8 and 1.9, respectively. Detailed circuit diagrams are presented in Appendix B.

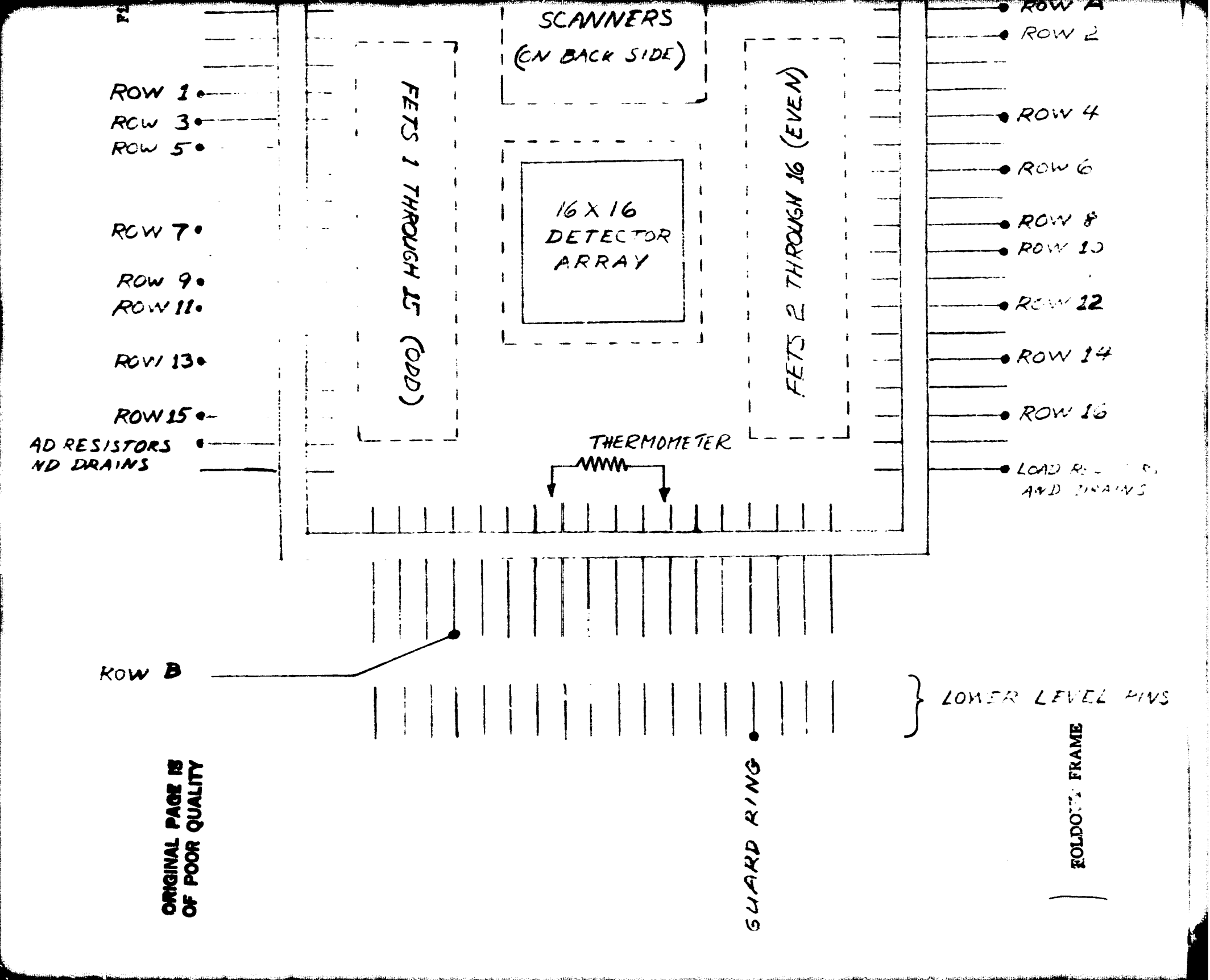
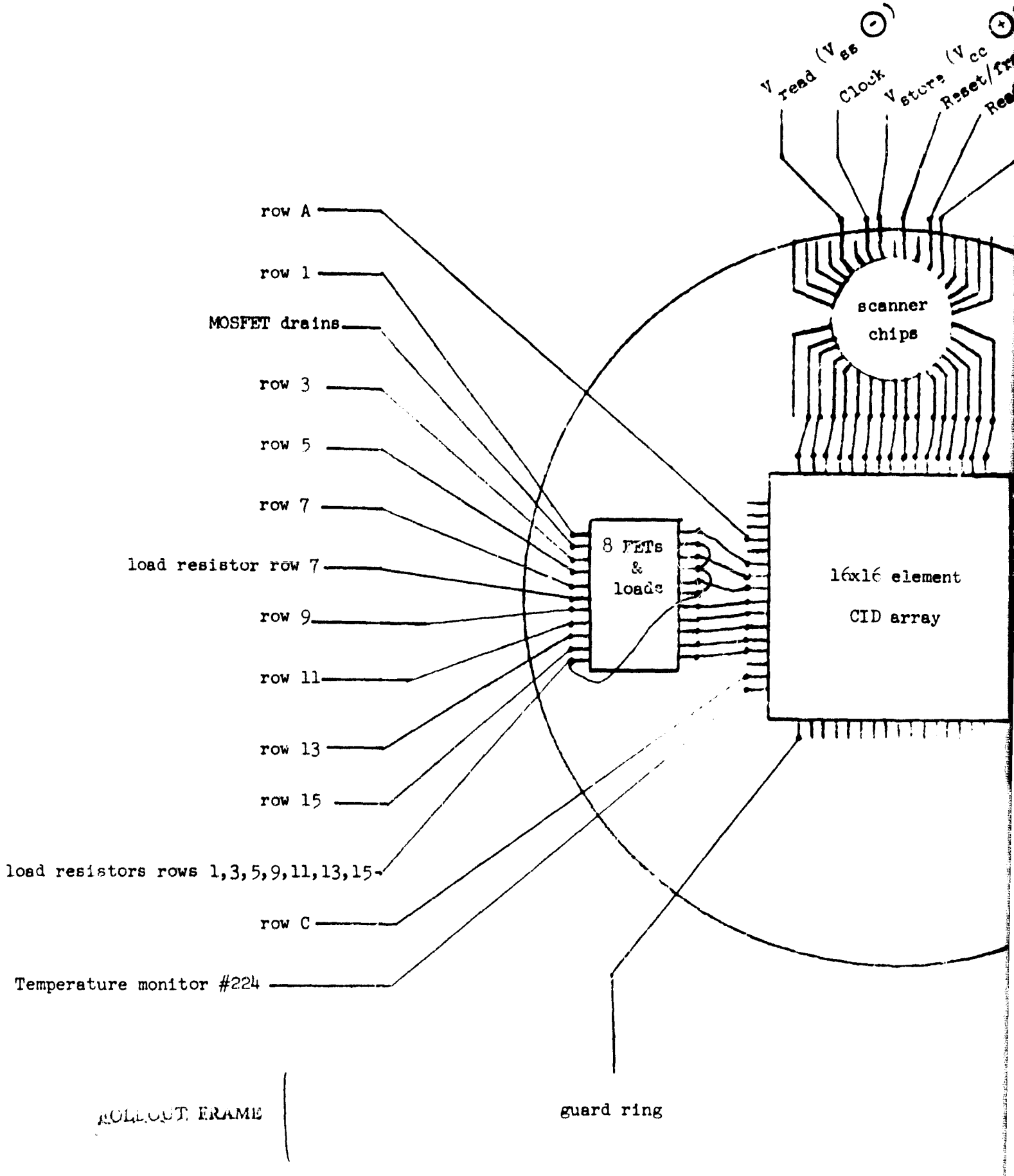


Figure 1.6 Packaging configuration of FPA #1


V read (V ss
Clock
V store (V cc
Reset/fr
Rea
row A
row 1
MOSFET drains
row 3
row 5
row 7
load resistor row 7
row 9
row 11
row 13
row 15
load resistors rows 1,3,5,9,11,13,15
row C
Temperature monitor #224
scanner chips
8 FETs & loads
16x16 element CID array
guard ring
ROLLOUT FRAME

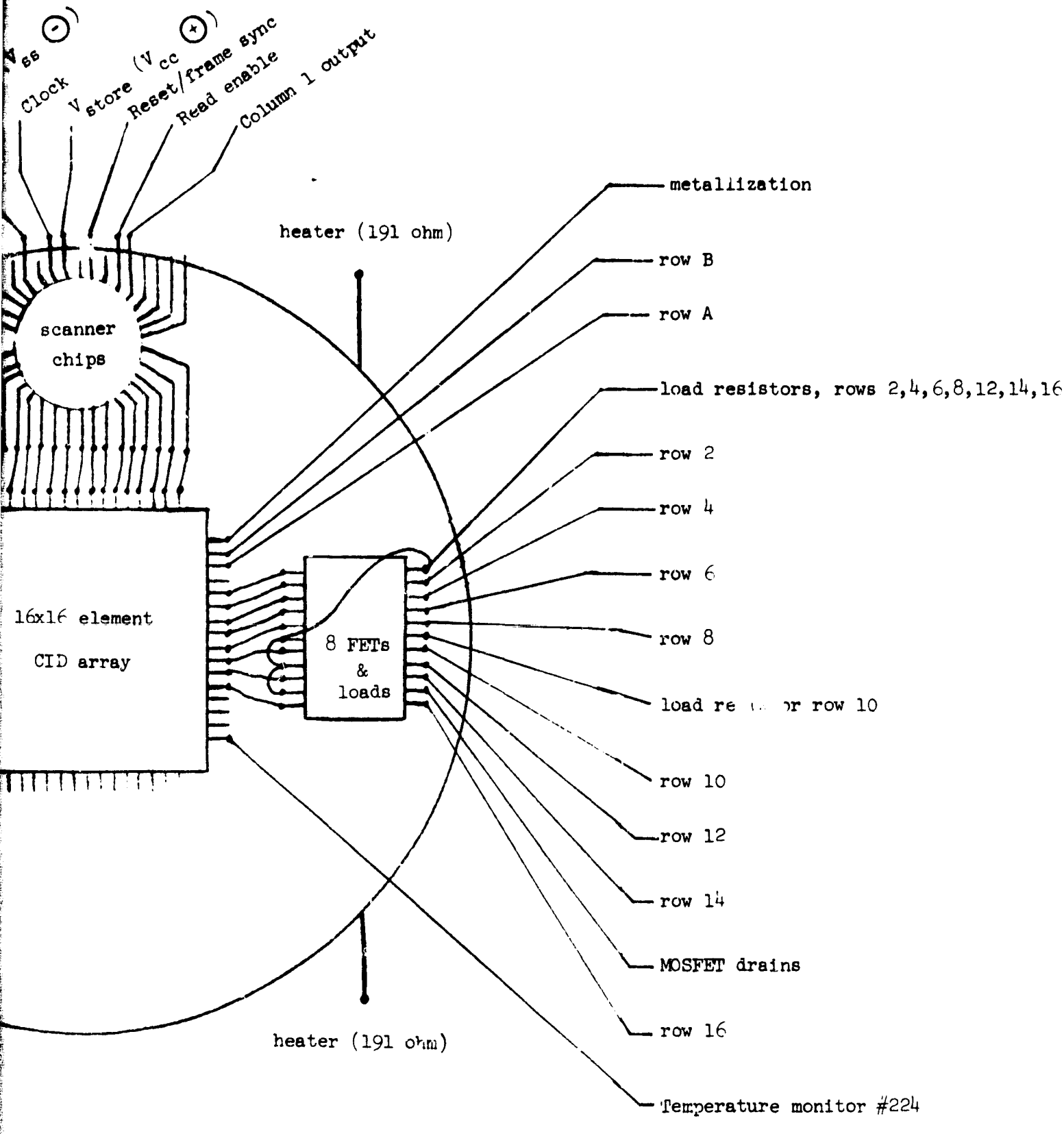
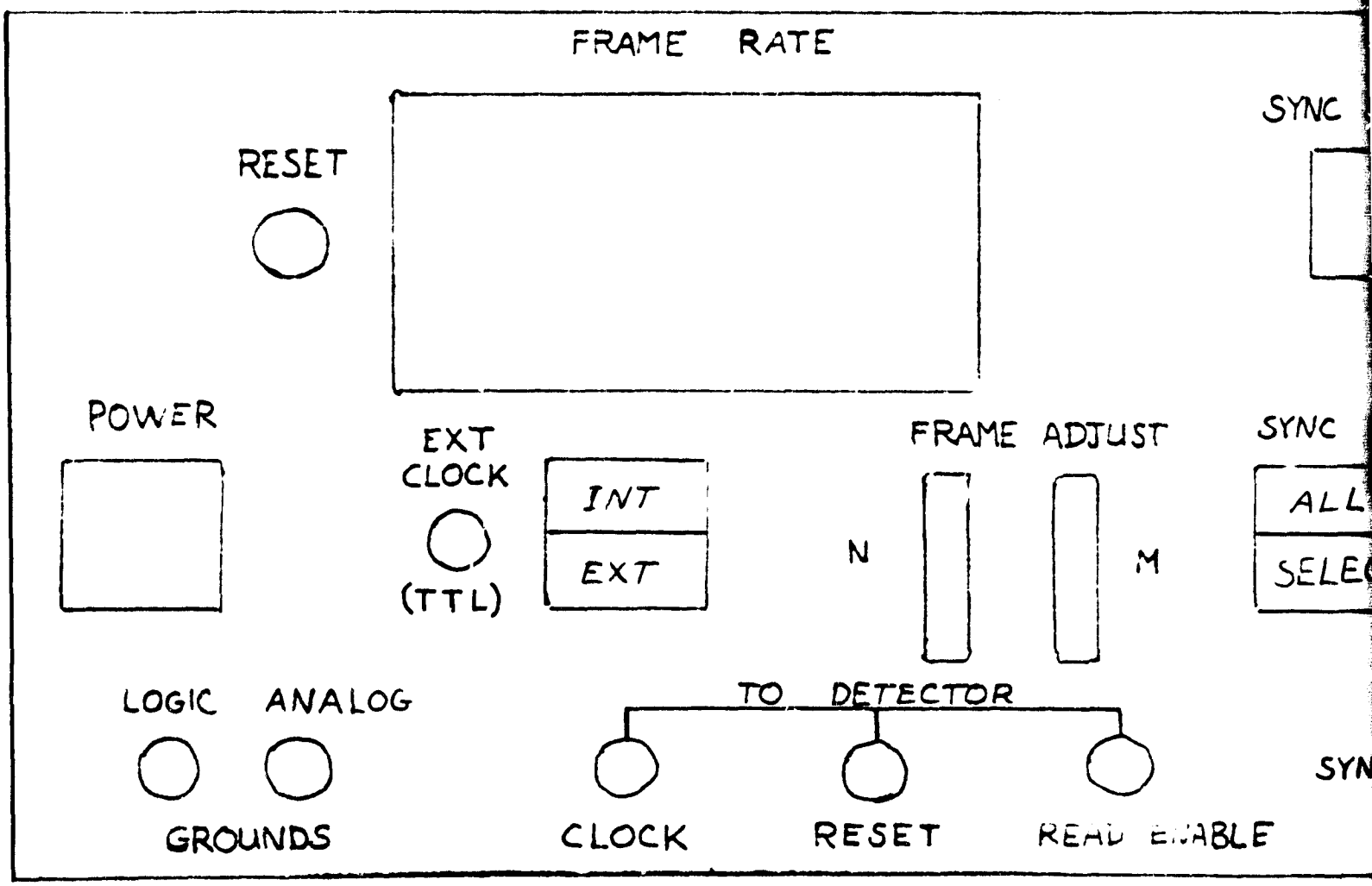


Figure 1.7 Packaging configuration of FPA #2

FOLDOUT FRAME 2



FOLDOUT FRAME

NOTE: All connectors are type BNC female

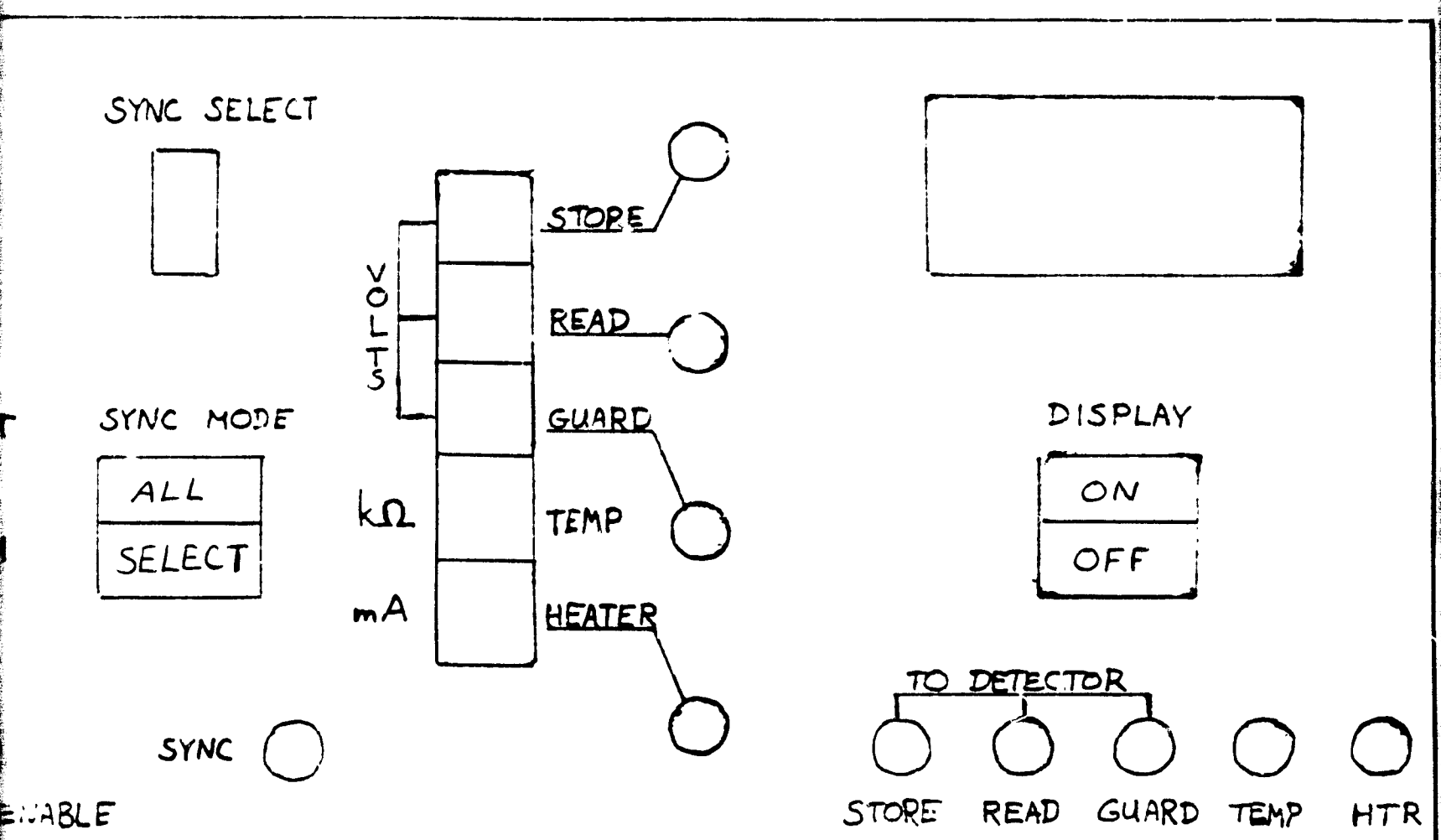
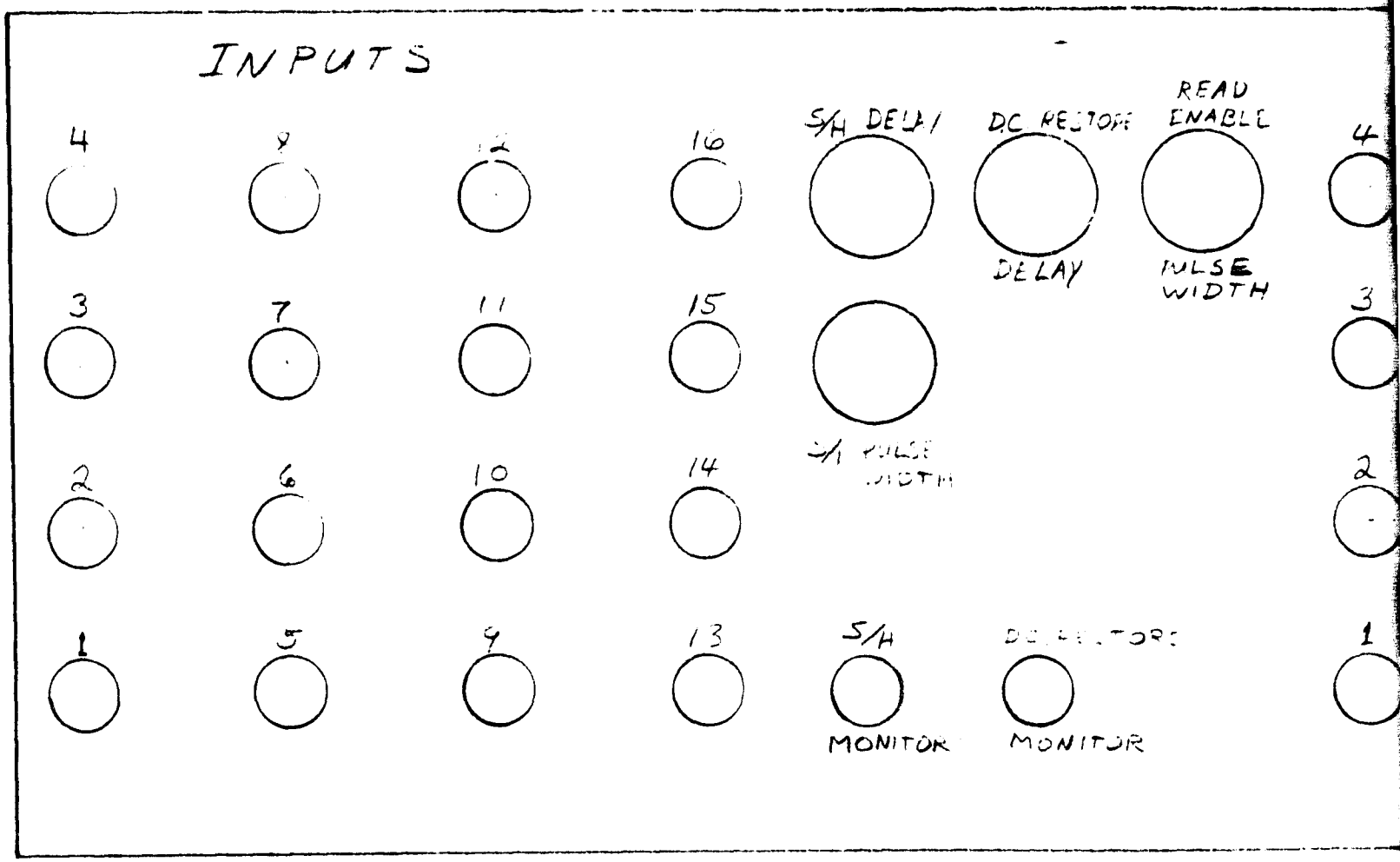


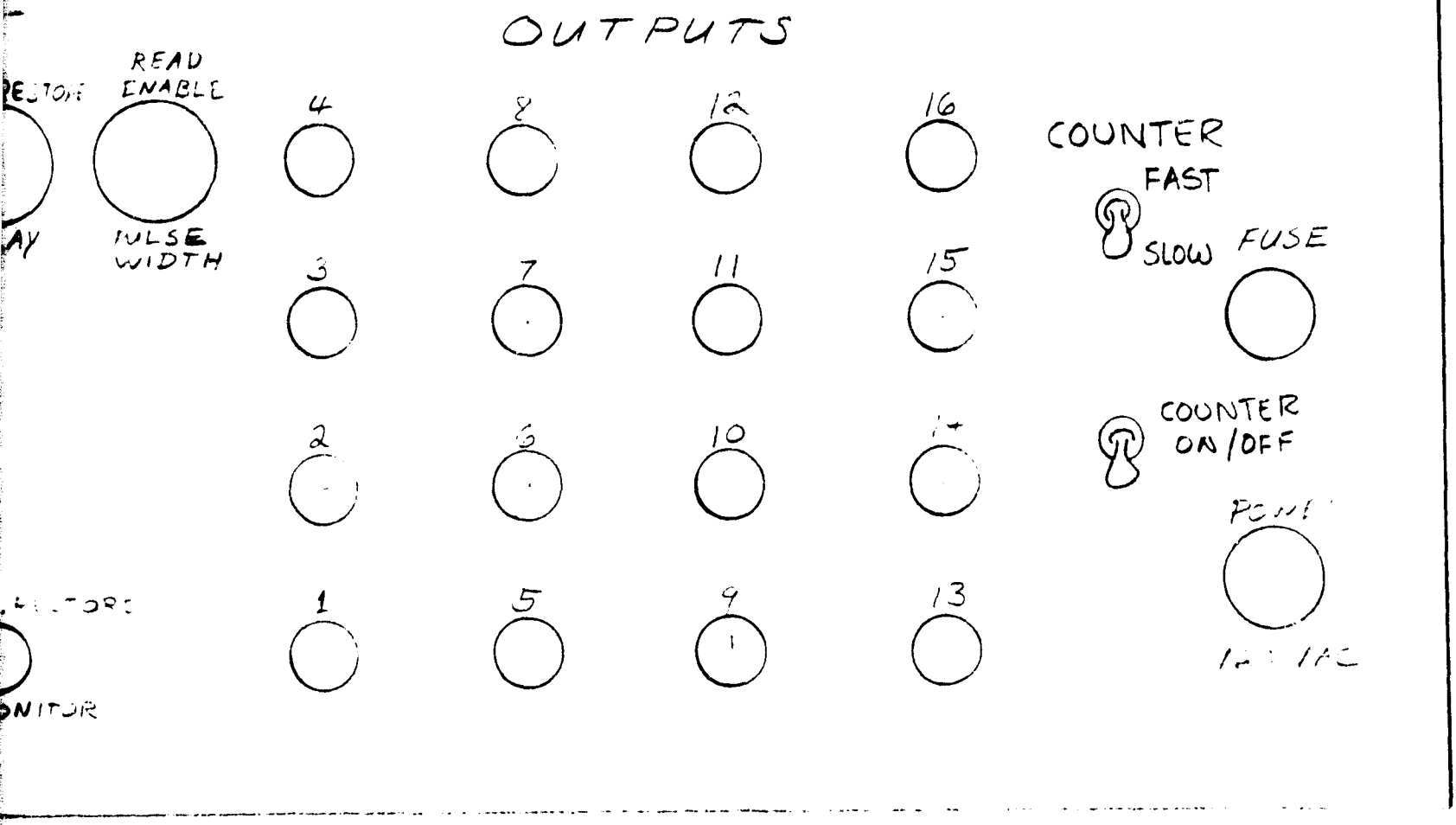
Figure 1.8 Front panel layout of electronics unit

FOLDOUT FRAME 2



FOLDOUT FRAME

NOTE: All connectors are type BNC female



FOLDOUT FRAME 2

Figure 1.9 Rear panel layout of electronics unit

2.0 OPERATING INSTRUCTIONS

This section details the manner in which either of the focal plane assemblies are interconnected with the electronics unit, and contains explanations of how the LWIR system may be operated.

2.1 System Setup

In preparation for test, the focal plane is mounted and wired into a suitable liquid helium Dewar vessel. It is preferable to employ a Dewar mount which permits the FPA to be temperature controlled because the performance of the CID detector elements is strongly temperature dependent with performance peaking around 11 K. The Dewar wiring task is in practice the most difficult part of the setup, and wiring errors are not uncommon. For this reason it is recommended that a room-temperature checkout of the system be made prior to cool-down. Although detector performance cannot be assessed at room temperature, proper functioning of the scanning electronics and the MOSFET source followers can easily be verified by monitoring the FPA output signal using an oscilloscope.

With the exception of the Dewar wiring, the interconnection scheme is very simple. All timing and supply voltages, i.e. all inputs necessary for operation of the FPA, are available on the front panel of the electronics unit. FPA output signals, in contrast, are connected to terminals on the electronics unit's rear panel. The hook-up is shown diagramatically in Figure 2.1.

The internal clock allows for operation at fixed frame rates of about $10^3/2^N$, where N = 0, 1, 2,3... . If different frame rates are desired for particular applications, an external, variable frequency square wave generator may be connected to the front panel; the operating frequency of the external generator must be 16 times higher than the desired frame rate. A switch is provided on the front panel to change from internal to external clock operation.

To complete the setup, it is recommended that the timing of the dc-restore, sample and hold (S/H), and read commands be measured and recorded in a Test Log

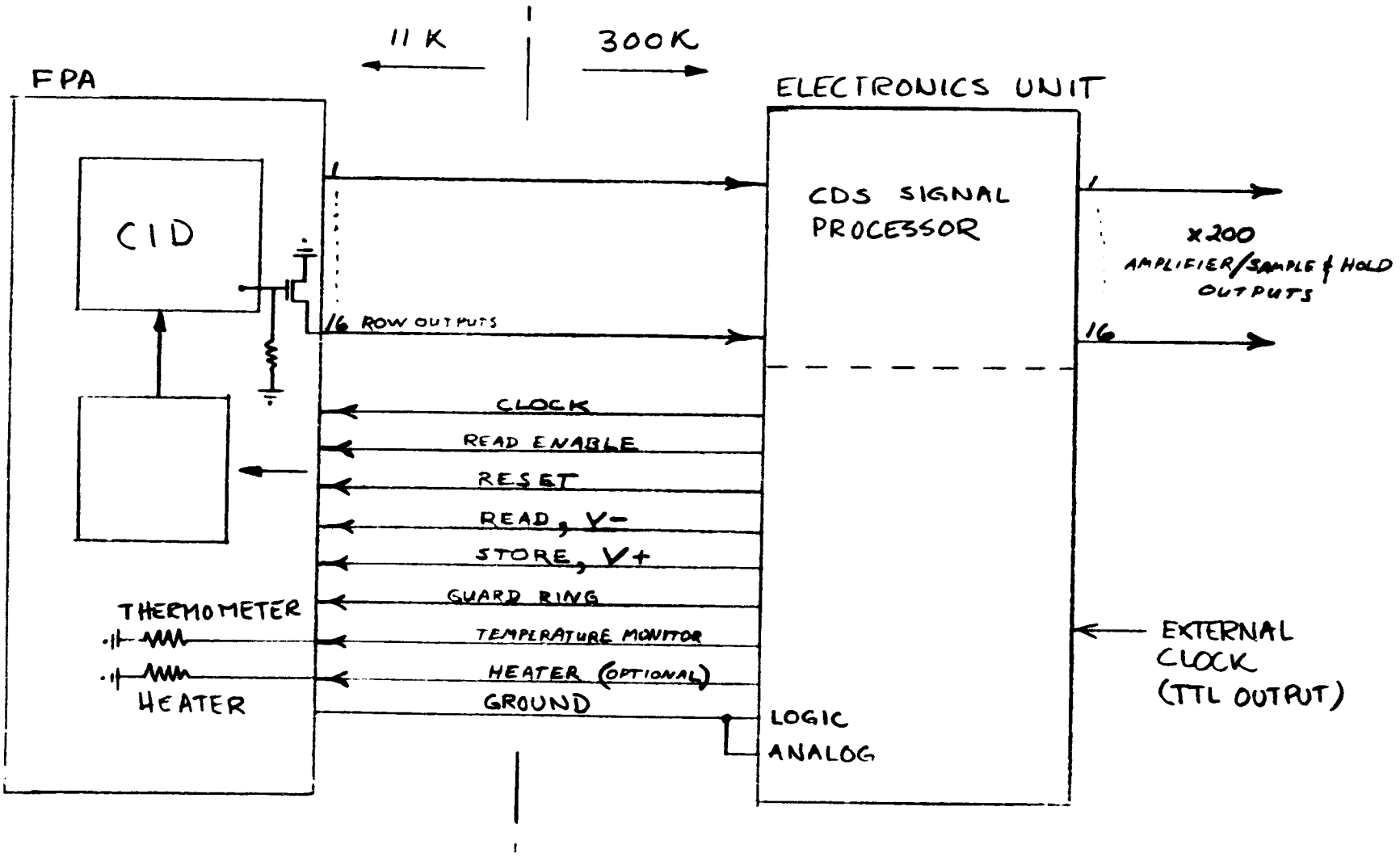


Figure 2.1 Hook-up of focal plane assembly and electronics unit

Book for future reference because noise voltages and output levels, including zero-signal baseline levels, depend on them. Recall that the dc-restore and S/H commands control the operation of the CDS signal processor, while the read command is the pulse which momentarily effects inversion-mode conditions (as opposed to accumulation-mode conditions) at the CID's oxide-semiconductor interface. The significance of the timing of these commands becomes clear if one considers a typical CID output signal prior to CDS signal processing; such a signal is shown in Figure 2.2.

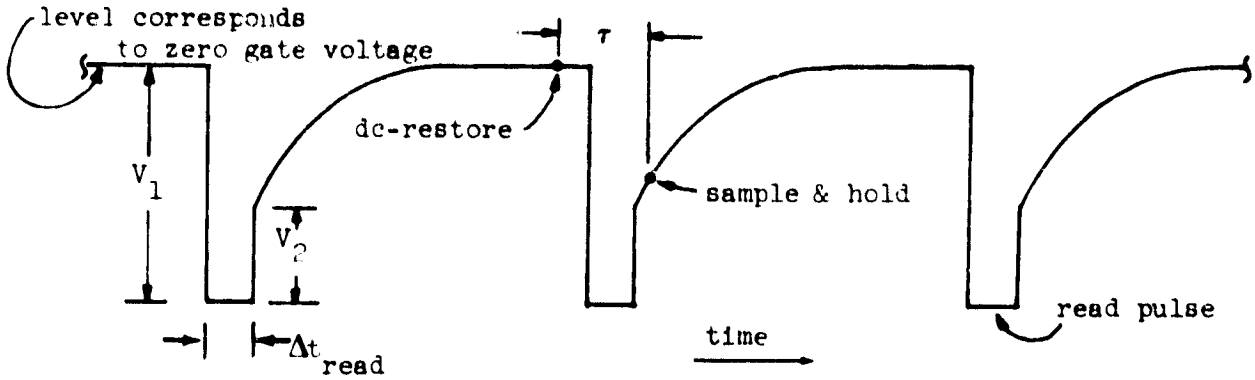


Figure 2.2 Waveform of typical CID output signal

Near the end of an integration period the gate voltage on a MOSFET source follower has decayed to nearly zero volts because its input capacitance has been discharged through the load resistor. Accordingly, the exact timing of the dc-restore pulse relative to that of the read pulse is not critical. The relative timing of the S/H pulse, in contrast, is important and may be critical if the LWIR system is used for precise radiometric measurements.

First, because the signal of interest, i.e. $V_1 - V_2$, decays with time, the measured value of this voltage difference depends on the time separation between its acquisition by the S/H circuit and the completion of the read command pulse. Second, the delay, τ, between dc-restore and S/H commands determines the transfer function of the CDS signal processor; one finds that 1/f-noise components are minimized by choosing τ as small as possible. In practice, τ cannot be smaller than the minimum acquisition time of the S/H circuit chip used in the CDS signal processor, or about 5 microseconds.

Finally, because the read, store, and guard ring voltages can only be optimized when the FPA is at operating temperature, it is recommended that the room temperature checkout be performed initially with the following bias settings:

$$V_{read}\ (V_{ss}) = -3\ V$$
$$V_{store}\ (V_{cc}) = +3\ V$$
$$V_{guard} = 0\ V.$$

2.2 Operating Instructions

Following setup and room temperature checkout, the FPA must be cooled to about 11 K before the system can be operated. It is convenient to have a calibrated IR source available when performing the initial system adjustments. To begin, a desired frame rate is chosen. The choice will depend on the required detector integration period, which, in turn, is a function of the IR irradiance; large IR signals will require a short integration period, and vice versa. Recall that the integration period, T, is approximately equal to the reciprocal of the frame rate.

For a given clock frequency (obtained from either the internal or an external clock), the frame rate may be changed by factors of two using the "Frame Adjust" control switches marked "N" and "M", and which are located on the front panel of the electronics unit. Briefly, the function of these switches are as follows: For M = 0, the frame rate equals $f_{clock}/(16x2^{N})$, where N is the setting of the "N" switch. Furthermore, the readout of the 16 detectors in each row requires a whole integration period because the read-commands of adjacent detectors are spaced T/16 seconds apart. For the long integration periods necessary when measuring extremely low-level IR signals, one may wish to read a row of detectors out nearly simultaneously rather than have the readout occur equidistantly in time throughout one frame. Such a "burst"-type readout may be obtained by using the switch marked "M"; the frame rate is given by $f_{clock}/(16x2^{N+M})$ in this case. The duration of the "burst", expressed as a fraction of the integration period, for different switch settings is most easily established by monitoring a row output signal on an oscilloscope. A synchronization signal available on the front panel is used to trigger the oscilloscope. The "Sync Select" control switch permits one to trigger on and to display any of the 16 column channels contained in individual row outputs.

Slight differences in the characteristics of FPA #1 and FPA #2 may dictate that optimum performance requires different voltage and temperature values for the two arrays. As mentioned, peak performance is achieved at an operating temperature of about 11 K. The precise temperature must be established experimentally by varying the FPA temperature from approximately 8 K to around 13 K.

Signal and noise levels are functions of read, store, and guard ring voltages. Again, optimum performance settings must be determined experimentally. The operator may use Figures 2.3, 2.4, and 2.5 as a rough guide to bias voltage adjustment; these figures display the results of evaluation tests in which larger than normal bias voltages were used. Caution is advised before attempting operation at large bias voltages ($\pm$ 7 V or larger) because damage to the scanner chips may result. A built-in digital multimeter is provided on the front panel to help perform quick measurements of bias settings.

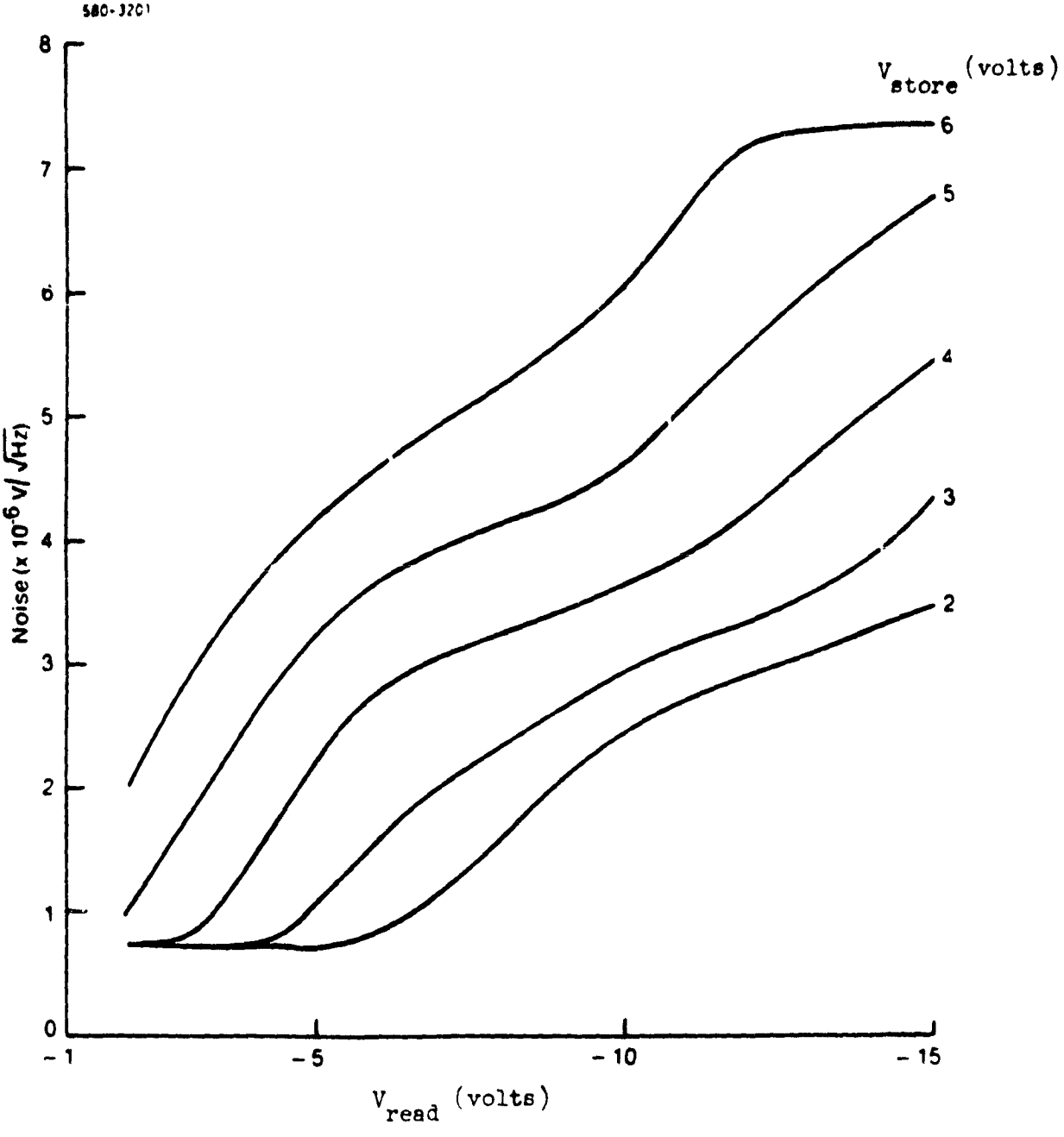


Figure 2.3 Noise output plotted as function of V_{store} and V_{read}

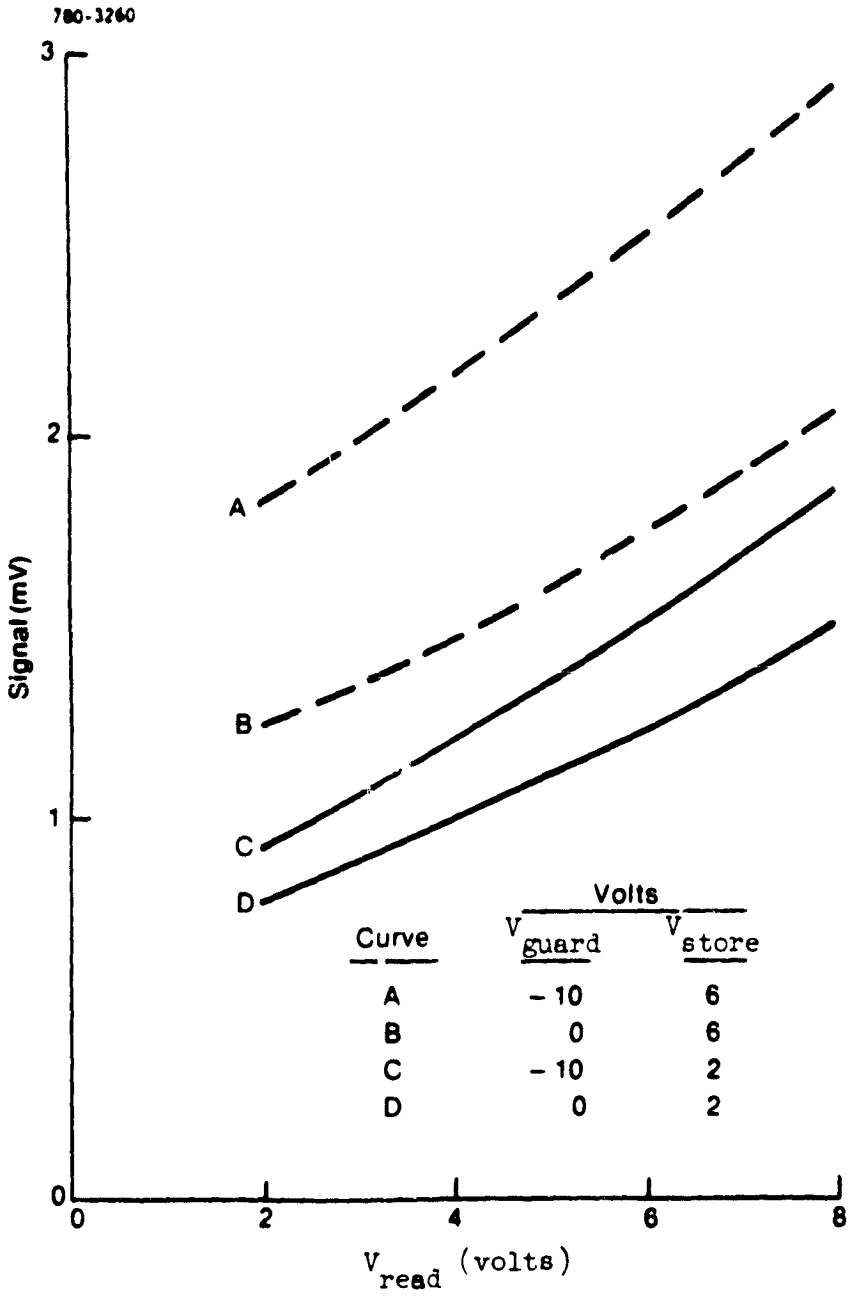


Figure 2.4 Relative signal output level as function of bias voltages

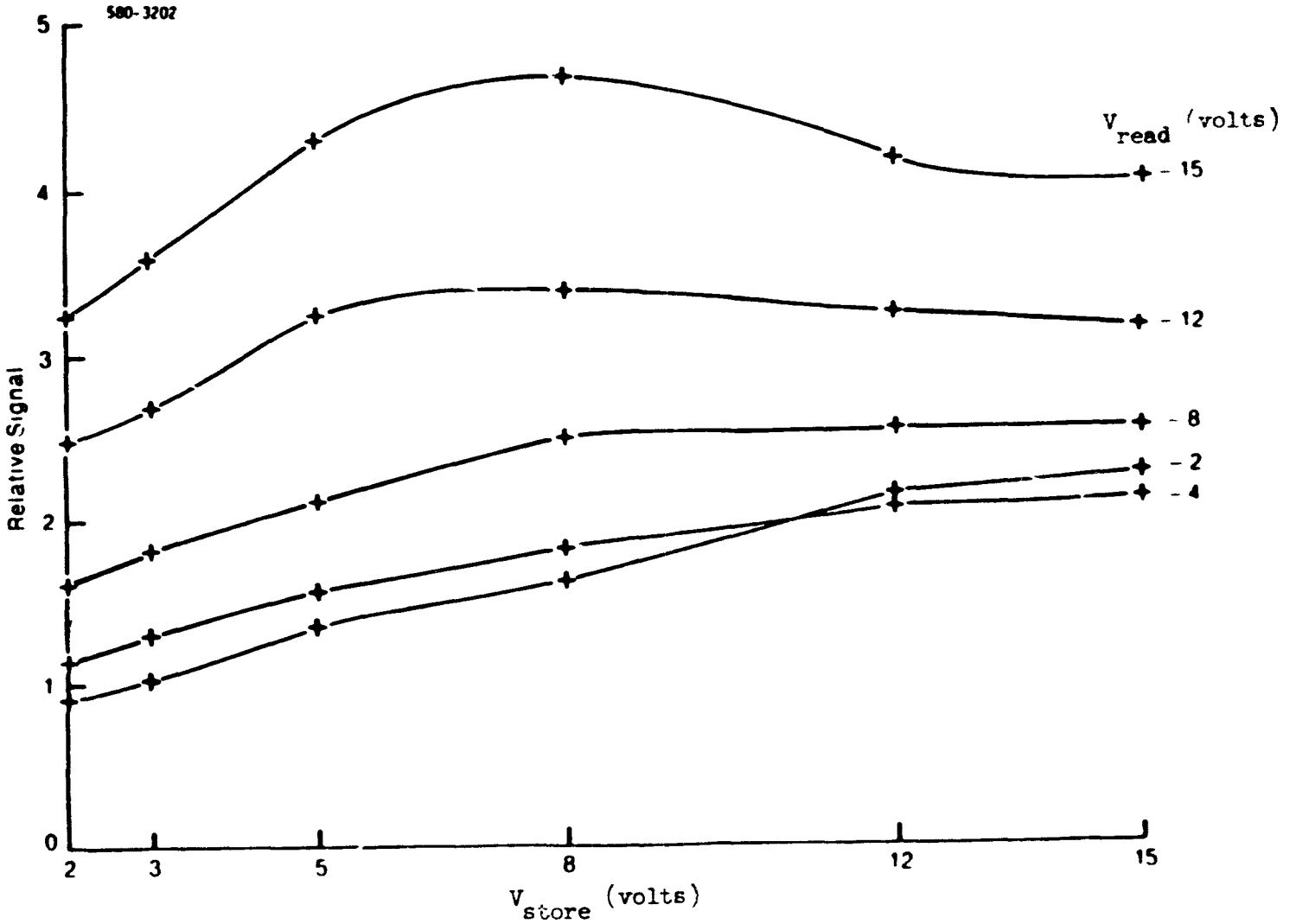


Figure 2.5 Relative signal output level as function of read and store voltages

3. FUNCTIONAL TEST

The two focal planes and the electronics unit were functionally tested prior to delivery.

Figures 3.1a through 3.1d for FPA #1 and Figures 3.2a through 3.2d for FPA #2 display oscilloscope photographs of each of the 16 row output signals as observed during the functional tests. For convenience, each photograph contains two different row output signals, each of which is shown for both signal-on and signal-off conditions.

The light-emitting-diode (LED) source used to flood the array was modulated with a 7 Hz square wave. The upper trace for each row output corresponds to signal-off, while the lower trace represents signal-on. Column #1 is at the left side of each photograph and is repeated following readout of the 16^{th} column. The test conditions for FPA #1 were: V_{read} = -5 V, V_{store} = 5 V, V_{guard} = -1.9 V, f_{frame} = 250 Hz and the operating temperature was 7 K. Similarly, the test conditions for FPA #2 were: V_{read} = -8 V, V_{store} = 2 V, V_{guard} = -2 V, f_{frame} = 250 Hz, and the focal plane operating temperature was 6 K.

The functional test of FPA #1 verified that all 256 detector elements were active. The result of the functional test of FPA #2 was that operation of 254 detector elements were verified. Two detector elements in column 15, specifically the elements in rows 15 and 16 were non-operational.

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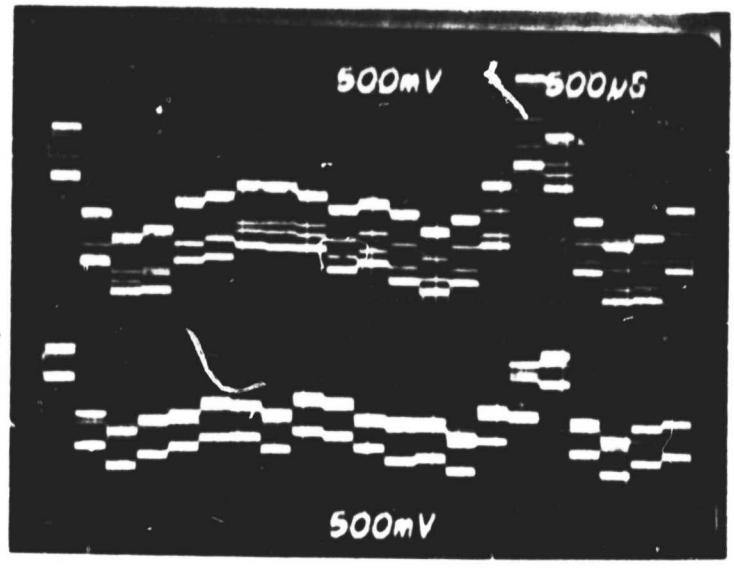
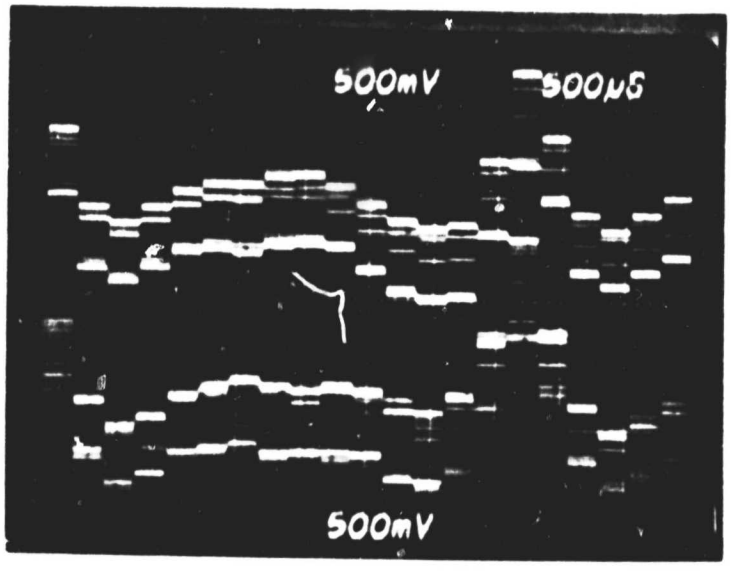


row 3

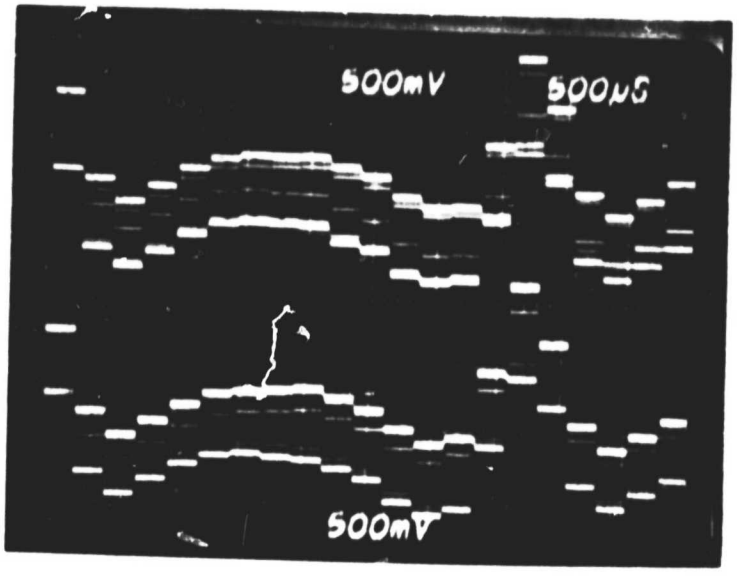
row 1



row 7

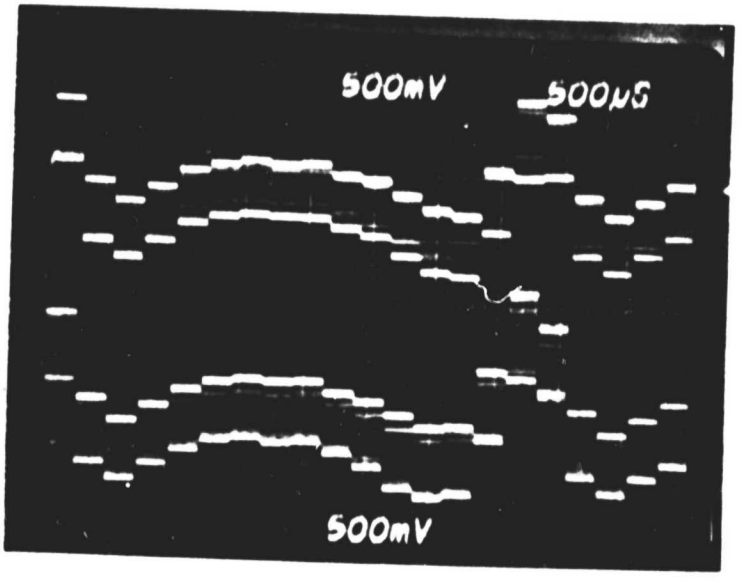
row 5

Figure 3.1a FPA #1 - Output signals from rows 1, 3, 5, and 7



row 11

row 9



row 15

row 13

Figure 3.1b FPA #1 - Output signals from rows 9, 11, 13, and 15

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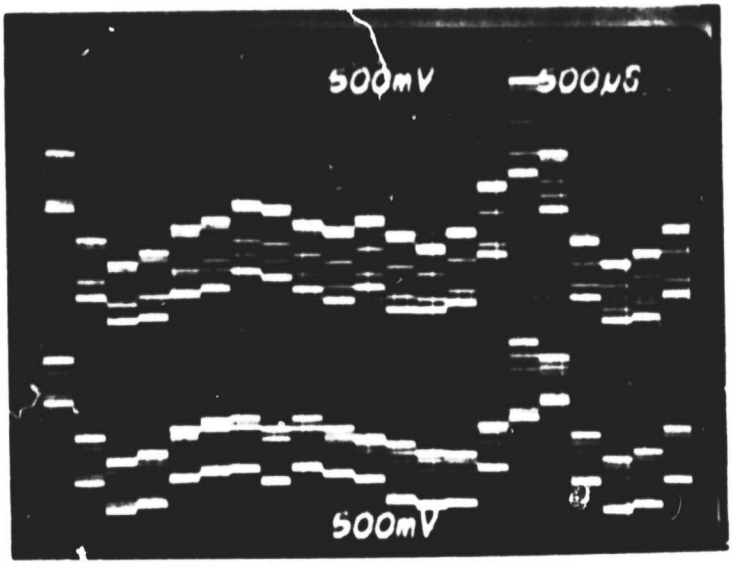
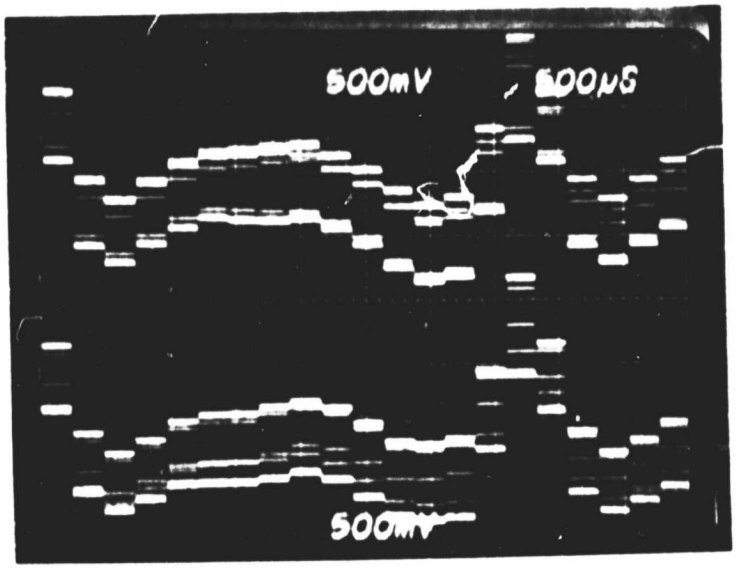


row 4

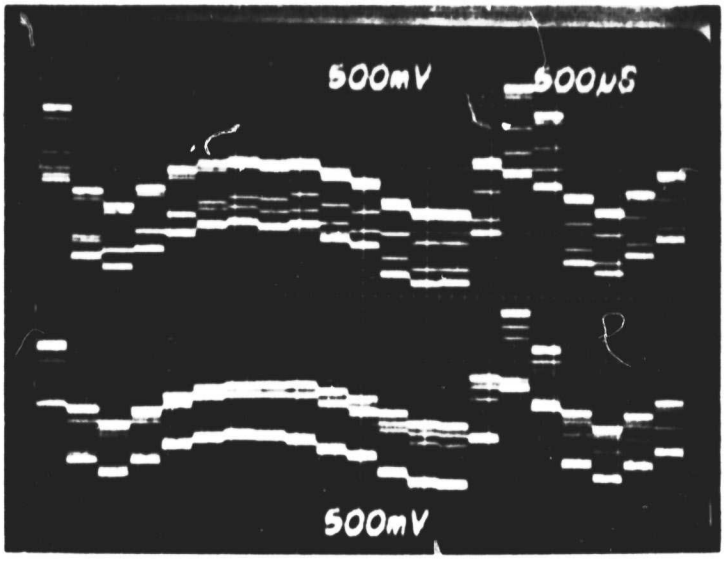
row 2



row 8

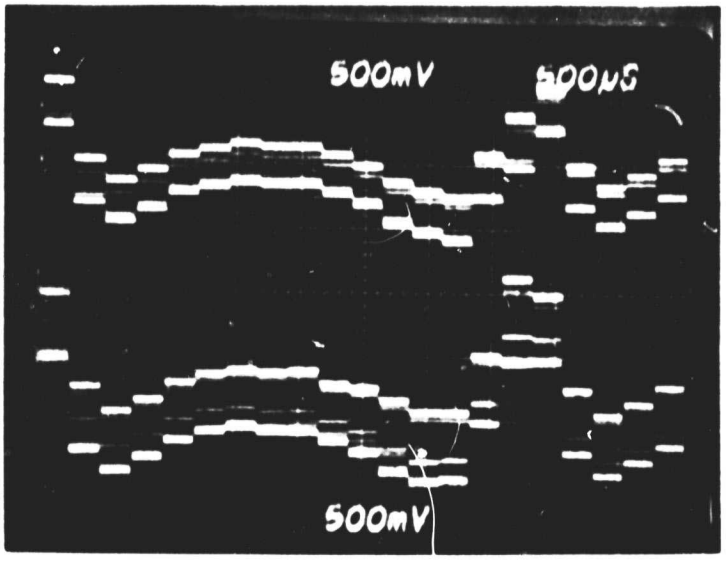
row 6

Figure 3.1c FPA #1 - Output signals from rows 2, 4, 6, and 8



row 12

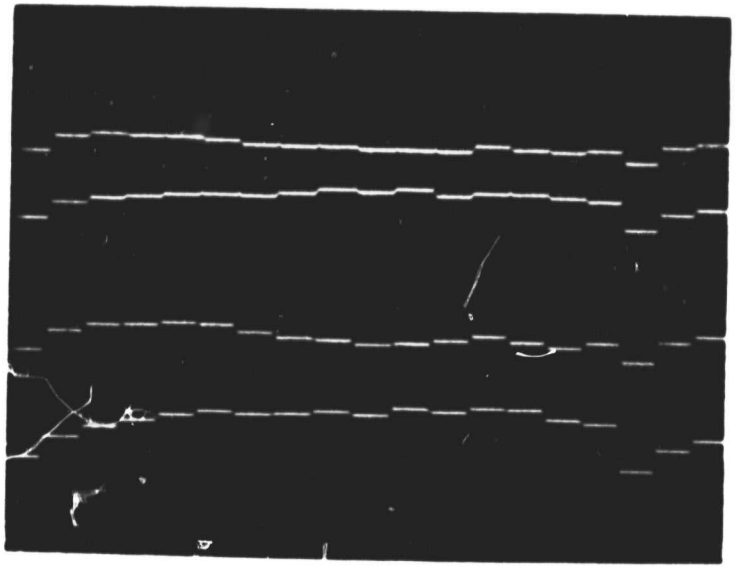
row 10



row 16

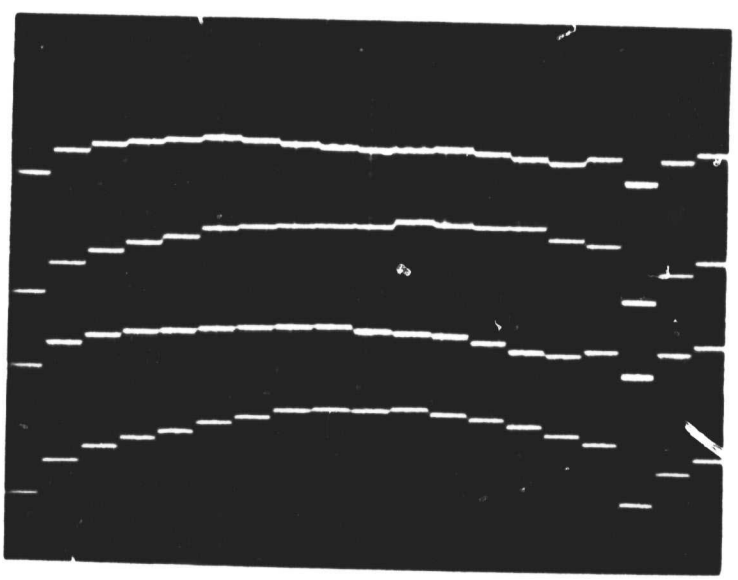
row 14

Figure 3.1d FPA #1 - Output signals from rows 10, 12, 14, and 16



row 1

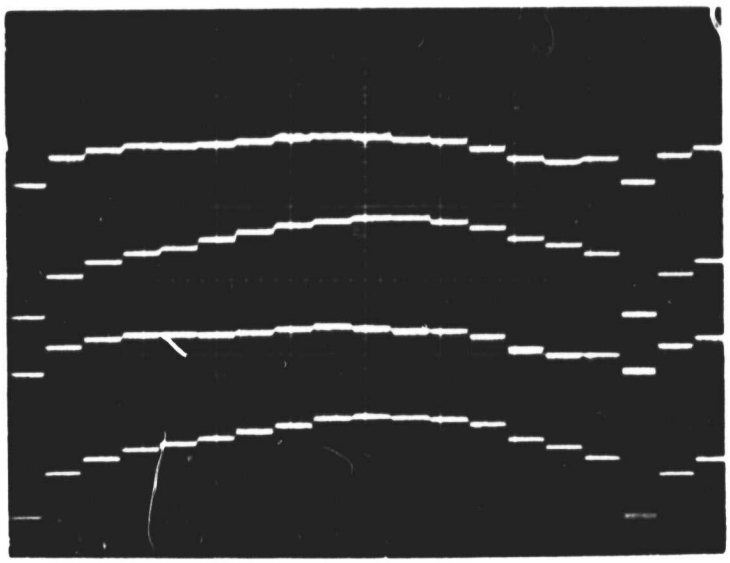
row 2



row 3

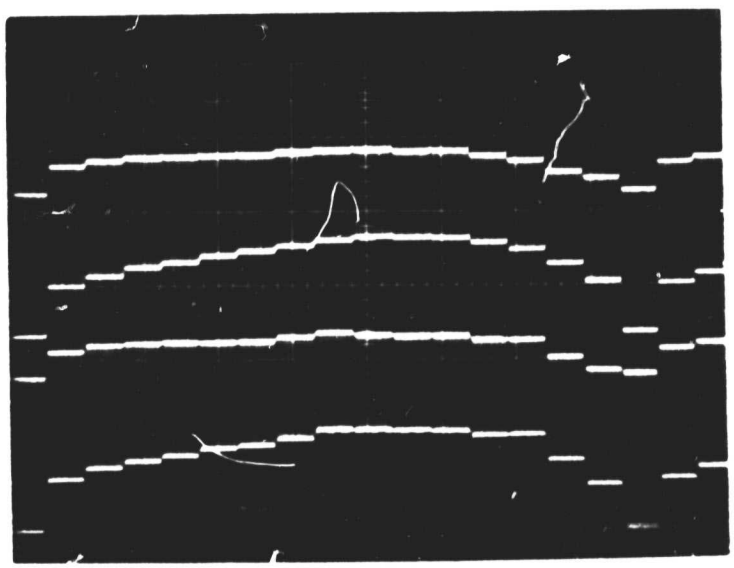
row 4

Figure 3.2a FPA #2 - Output signals from rows 1, 2, 3, and 4



row 5

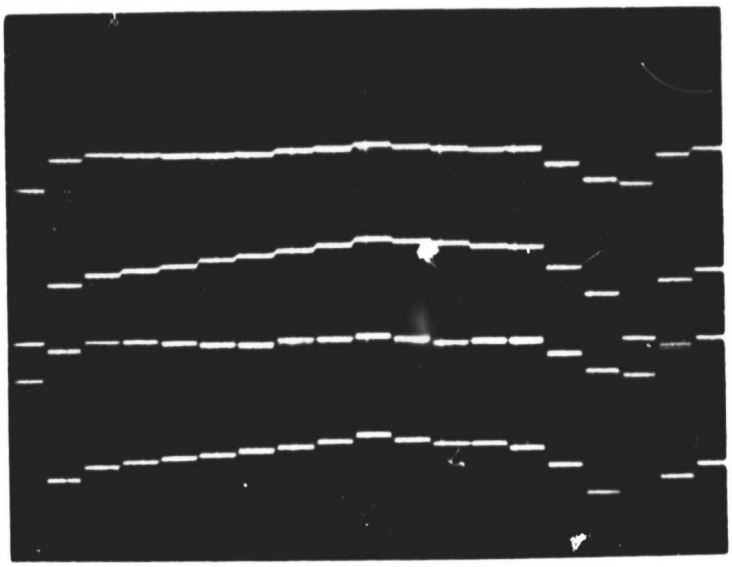
row 6



row 7

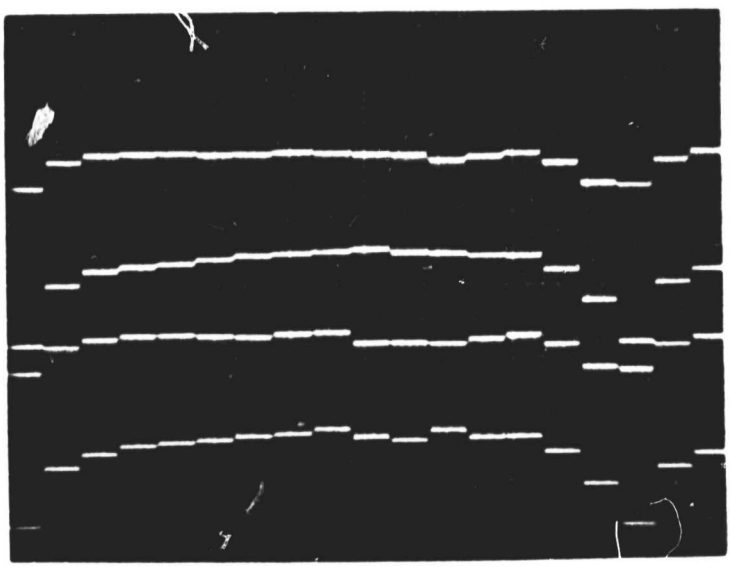
row 8

Figure 3.2b FPA #2 - Output signals from rows 5, 6, 7, and 8



row 9

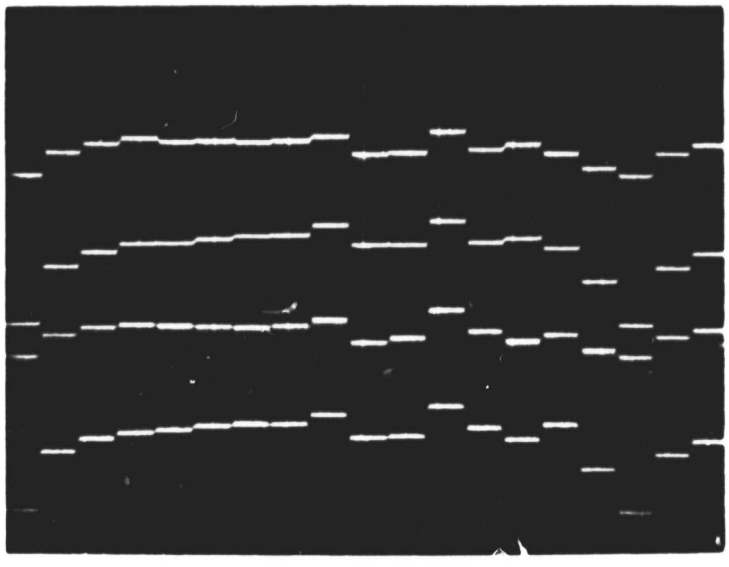
row 10



row 11

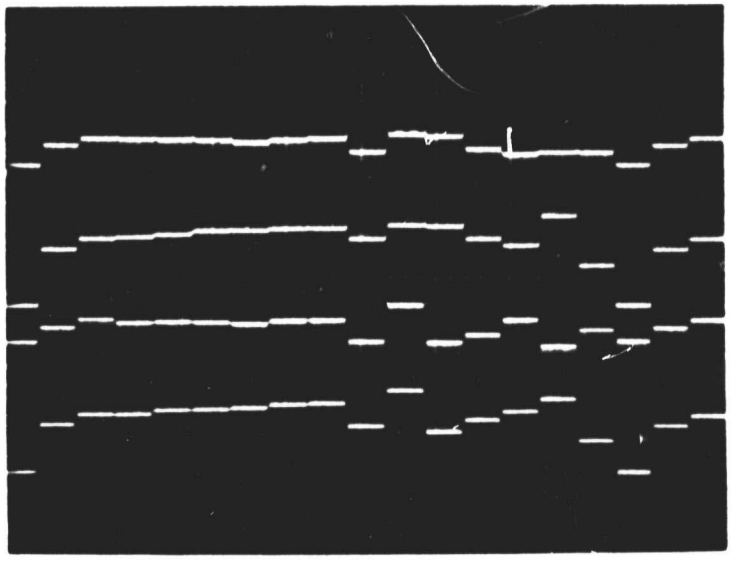
row 12

Figure 3.2c FPA #2 - Output signals from rows 9, 10, 11, and 12



row 13

row 14



row 15

row 16

Figure 3.2 FPA #2 - Output signals from rows 13, 14, 15, and 16

APPENDIX A

CALIBRATION DATA FOR TEMPERATURE MONITORS

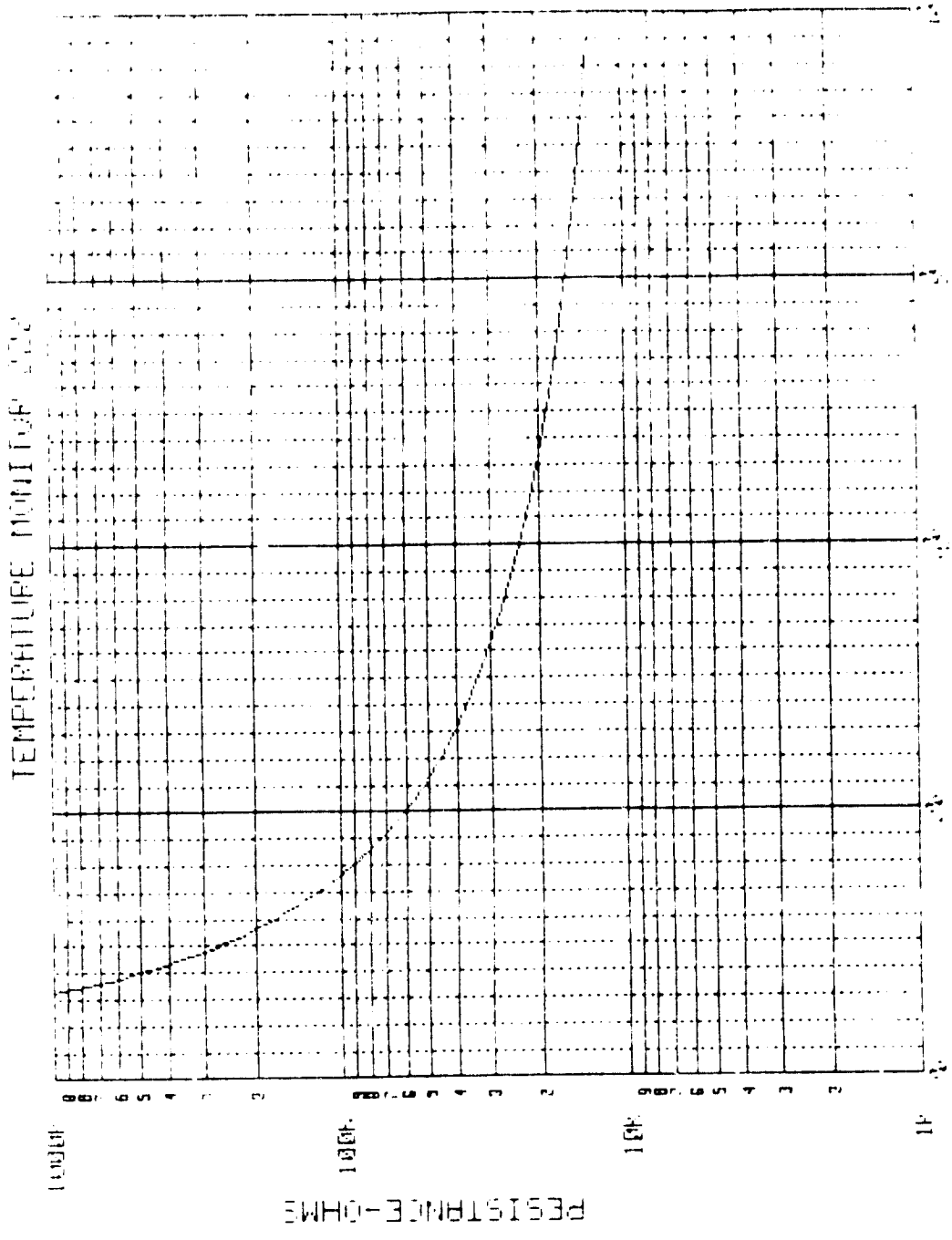


Figure A-1 Calibration curve for FPA #1 temperature monitor

Table A-1 Calibration data for FPA #1 temperature monitor

TEMPERATURE MONITOR 222	
TEMPERATURE (DEGREES K)	RESISTANCE (OHMS)
4.3	416.50
27.2	17.45
77.4	8.37
4.0	502.80
5.0	266.66
6.0	169.23
7.0	119.86
8.0	91.28
9.0	73.14
10.0	60.82
11.0	52.01
12.0	45.46
13.0	40.42
14.0	36.45
15.0	33.25
16.0	30.62
17.0	28.42
18.0	26.57
19.0	24.98
20.0	23.61
21.0	22.41
22.0	21.36
23.0	20.43
24.0	19.59
25.0	18.85
26.0	18.17
27.0	17.57
28.0	17.01
29.0	16.50
30.0	16.04

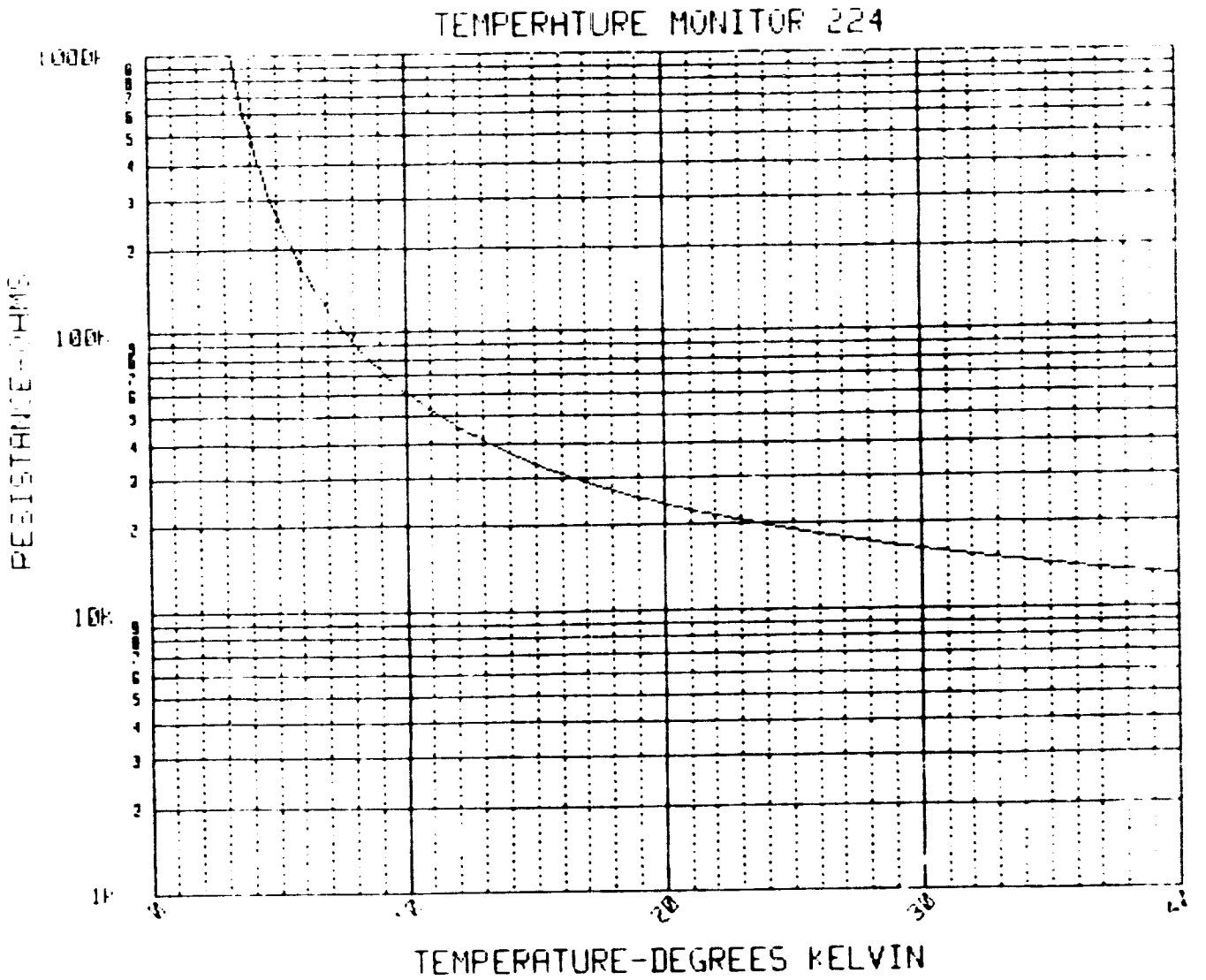


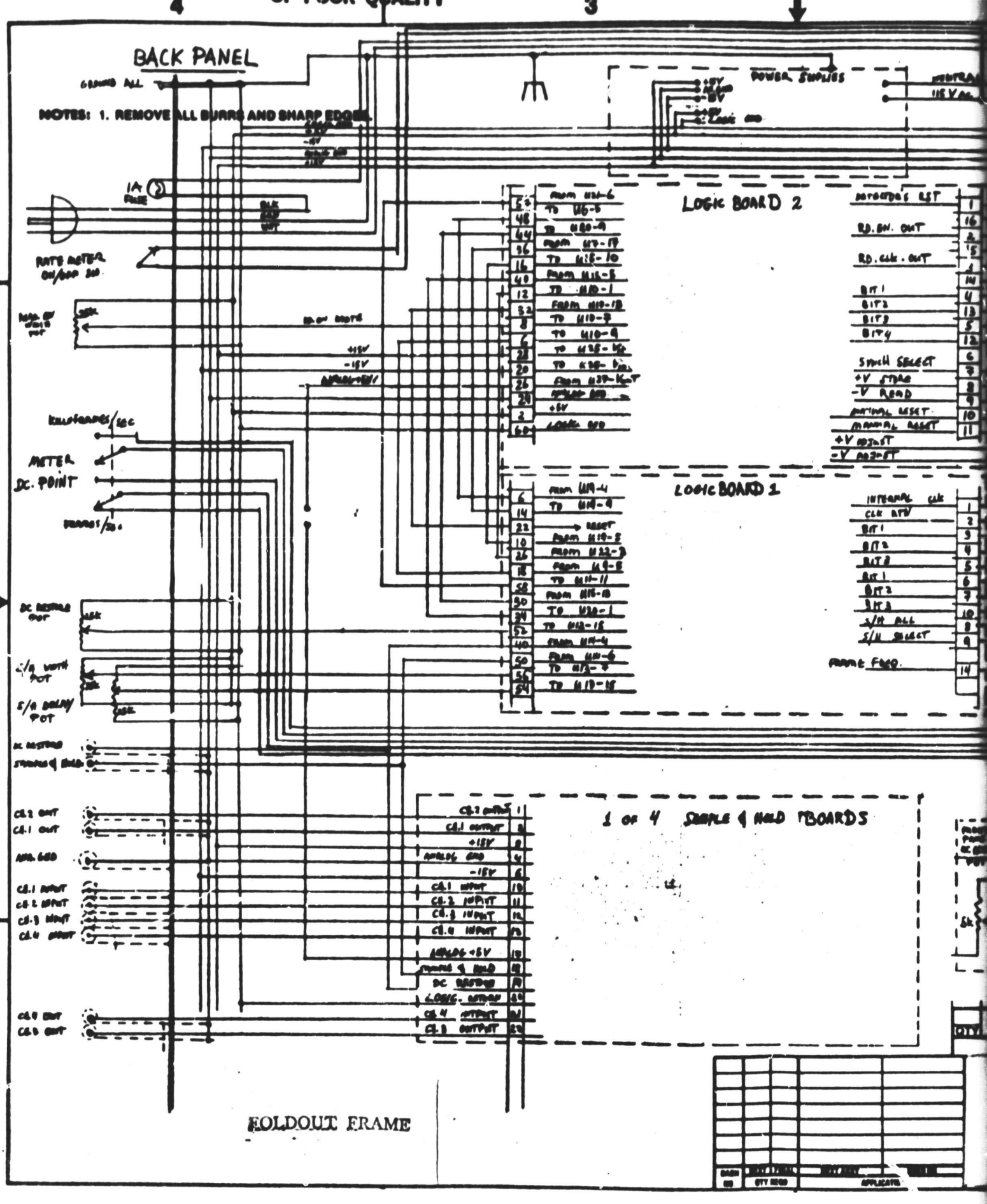
Figure A-2 Calibration curve for FPA #2 temperature monitor

Table A-2 Calibration data for FPA #2 temperature monitor

TEMPERATURE MONITOR 224	
TEMPERATURE (DEGREES K)	RESISTANCE (KOHMS)
4.3	417.40
27.2	17.65
77.4	8.97
4.0	503.46
5.0	267.74
6.0	170.22
7.0	120.71
8.0	92.01
9.0	73.77
10.0	61.38
11.0	52.51
12.0	45.91
13.0	40.83
14.0	36.83
15.0	33.60
16.0	30.95
17.0	28.73
18.0	26.86
19.0	25.26
20.0	23.87
21.0	22.66
22.0	21.60
23.0	20.66
24.0	19.82
25.0	19.06
26.0	18.38
27.0	17.77
28.0	17.21
29.0	16.69
30.0	16.22

APPENDIX B

DETAILED CIRCUIT DIAGRAMS



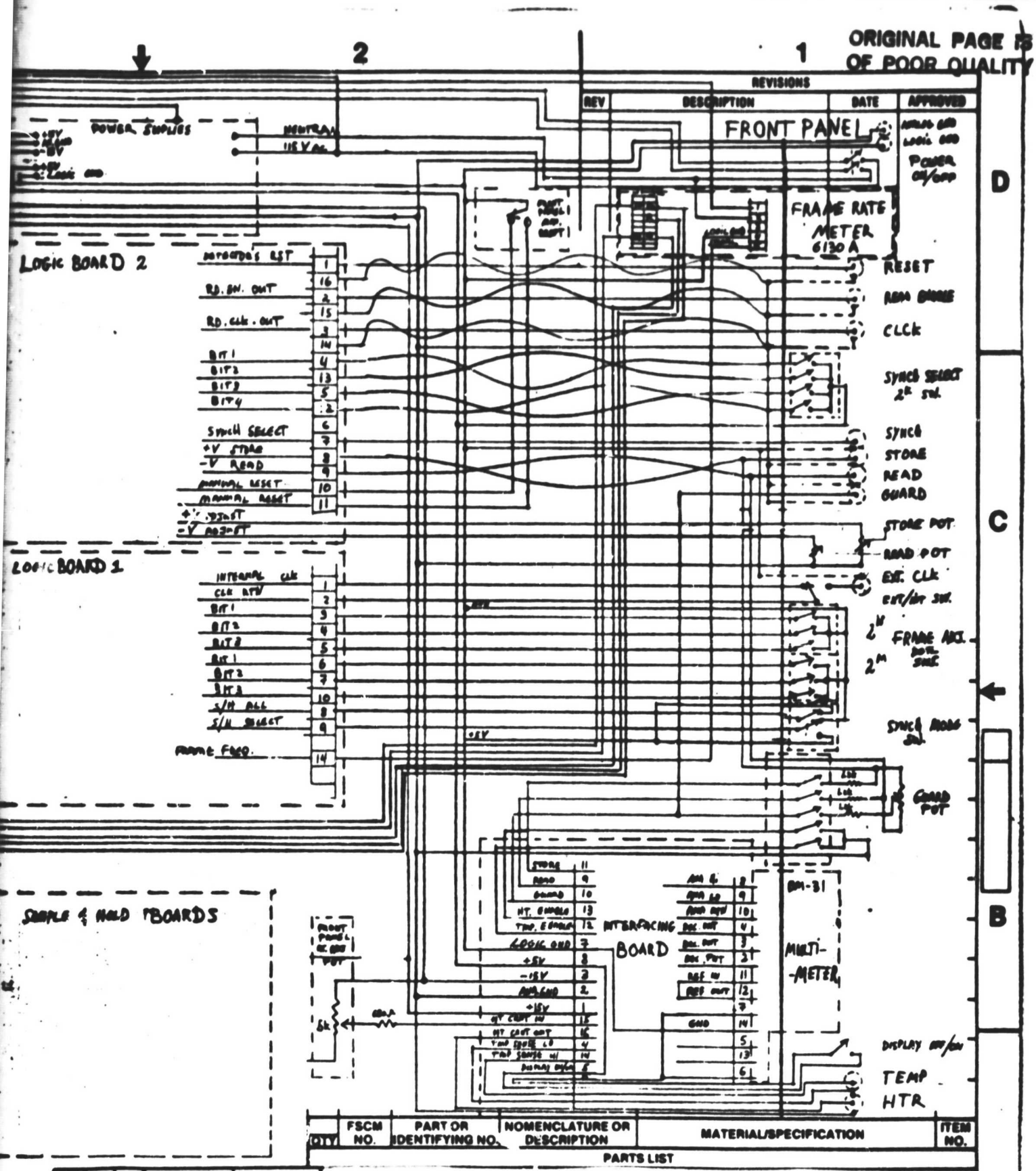


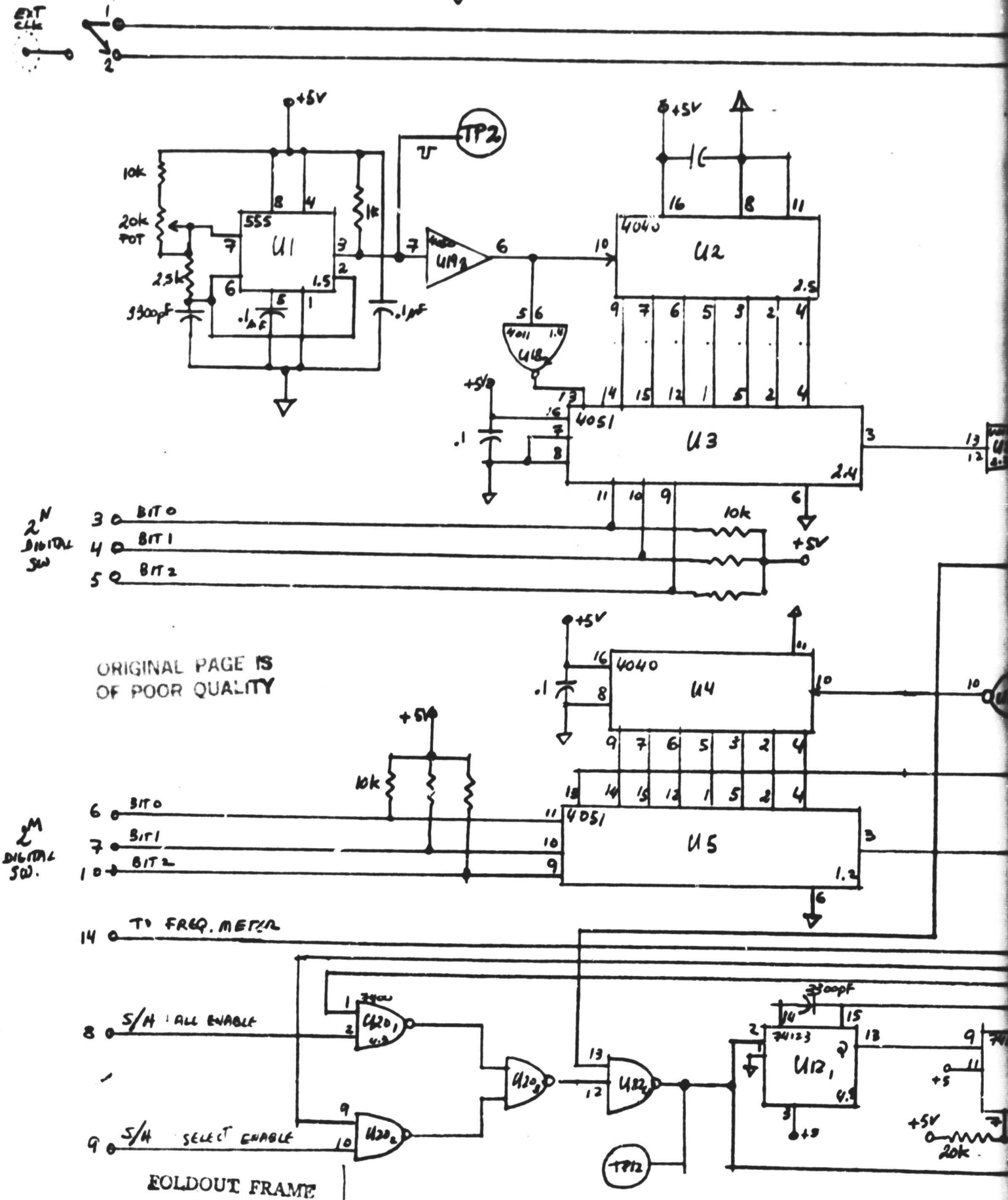
Figure B-1 Wiring diagram of electronics unit

FOLDOUT FRAME

16-PIN DIP
FRONT CONNECTOR

NOTE: RST = SYSTEM RESET
TP = NUMERICALLY MARKED TESTING POINTS ON FRONT EDGE OF CARD.
⏚ DIGITAL GND.

Figure B-2 Wiring diagram



FOLDOUT FRAME

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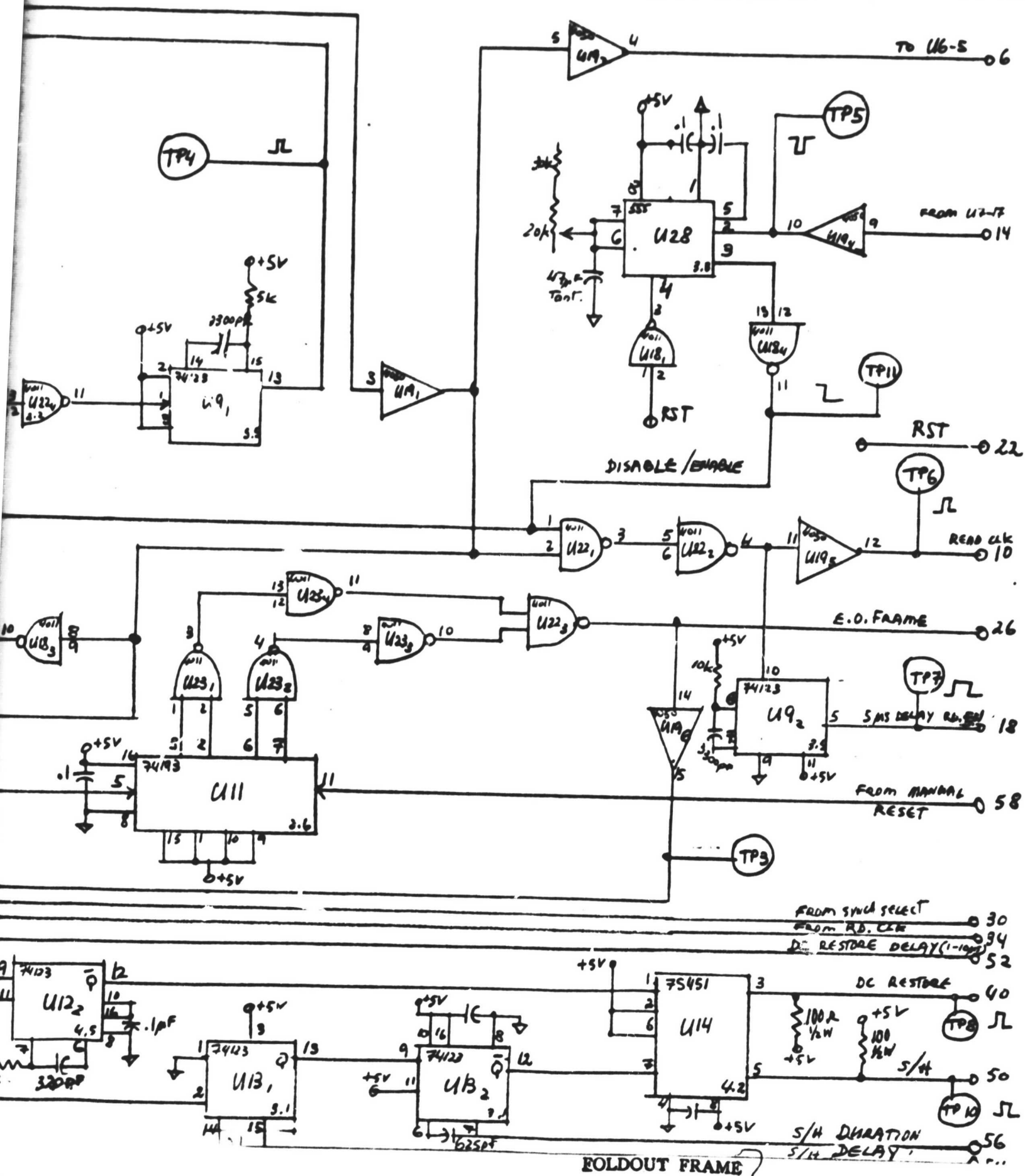
BACK EDGE CONNECTOR



FOLDOUT FRAME

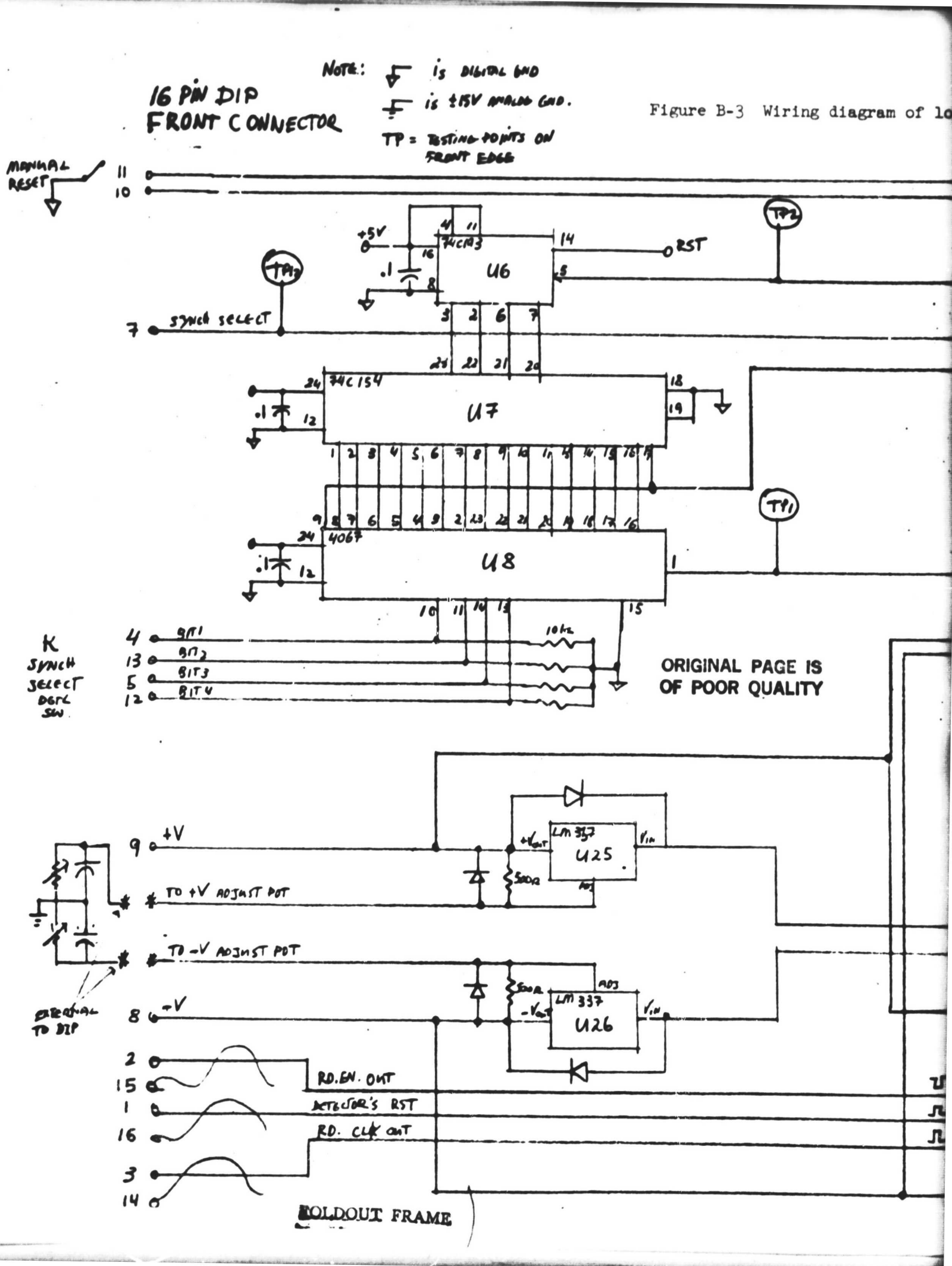
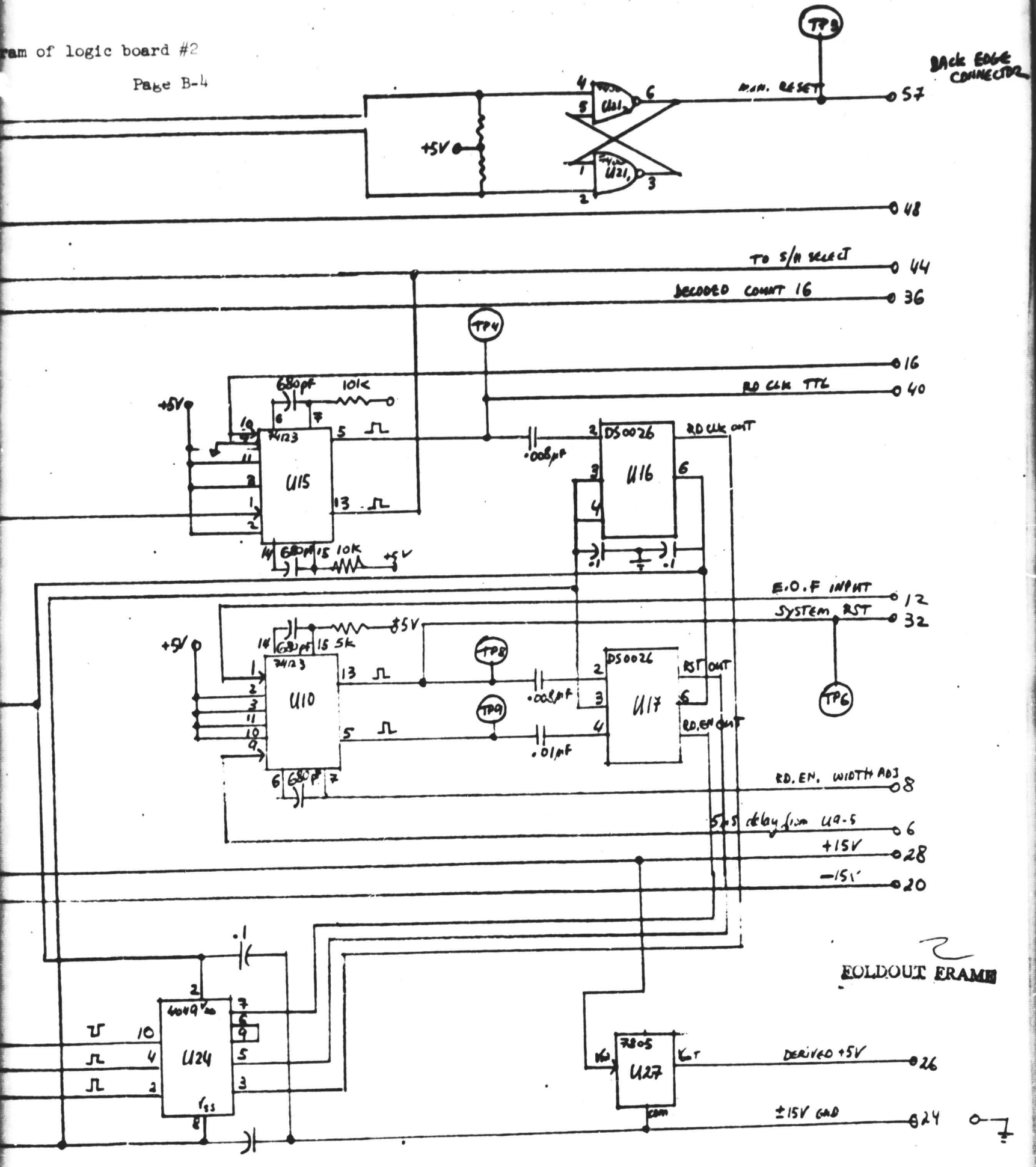


Figure B-3 Wiring diagram of lo


TP3
BACK EDGE CONNECTOR
MAN. RESET
57
+5V
U21
48
TO S/N SELECT
44
DECODED COUNT 16
36
TP4
16
RD CLK TTL
40
680pf
101K
74123
U15
.008μf
DS0026
U16
RD CLK OUT
10K
.1
E.O.F INPUT
12
SYSTEM RST
32
15.5K
U10
TP8
TP9
U17
RST OUT
TP6
RD.EN OUT
.01μf
RD. EN. WIDTH ADJ
8
5±.5 delay from U9-5
6
+15V
28
-15V
20
FOLDOUT FRAME
4049
U24
7805
U27
DERIVED +5V
26
±15V GND
24

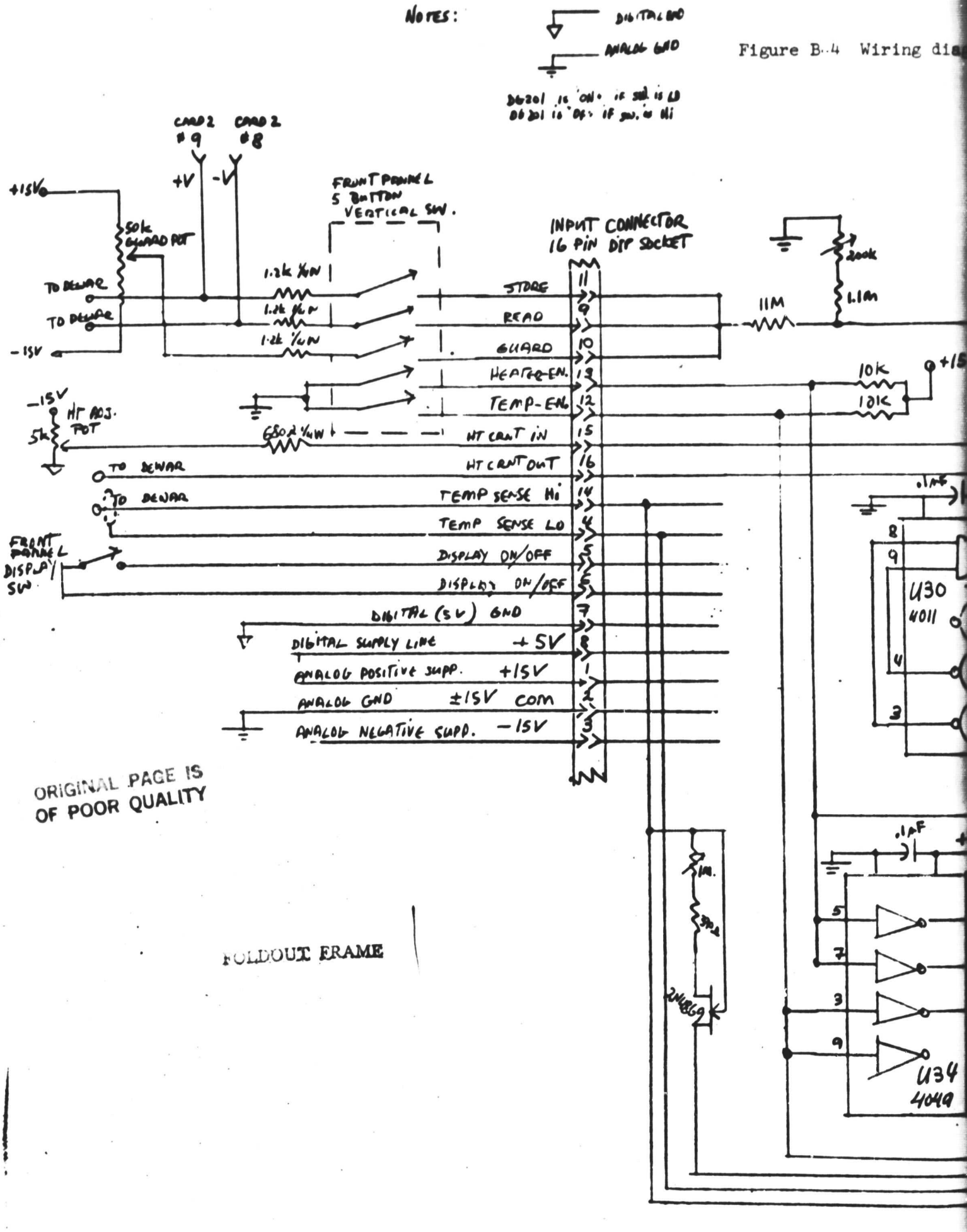


Figure B-4 Wiring dia

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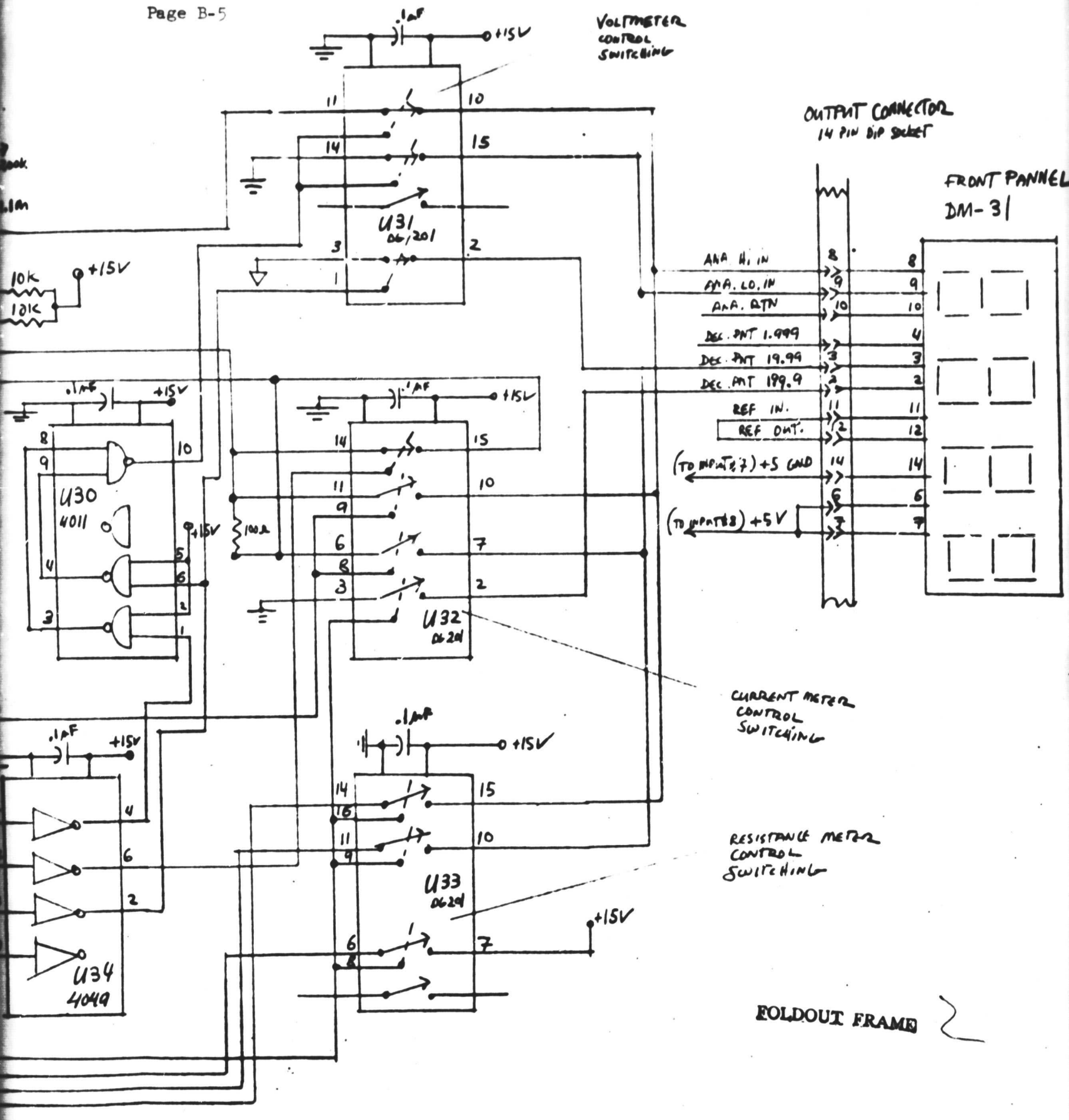
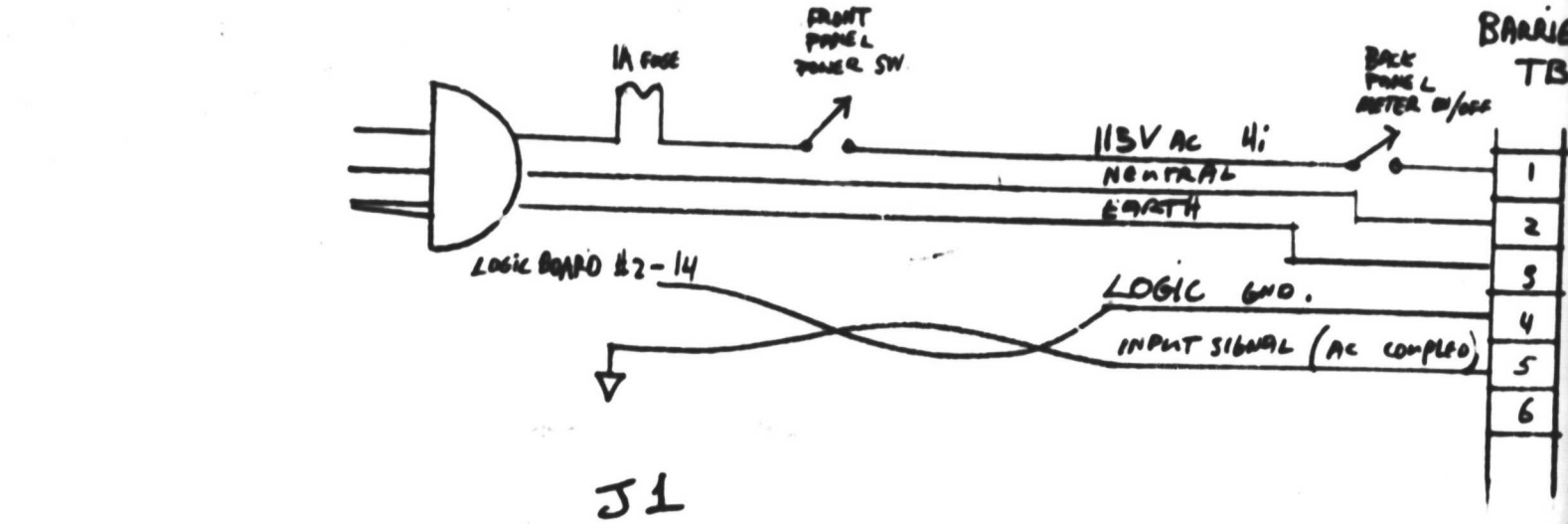
FOLDOUT FRAME

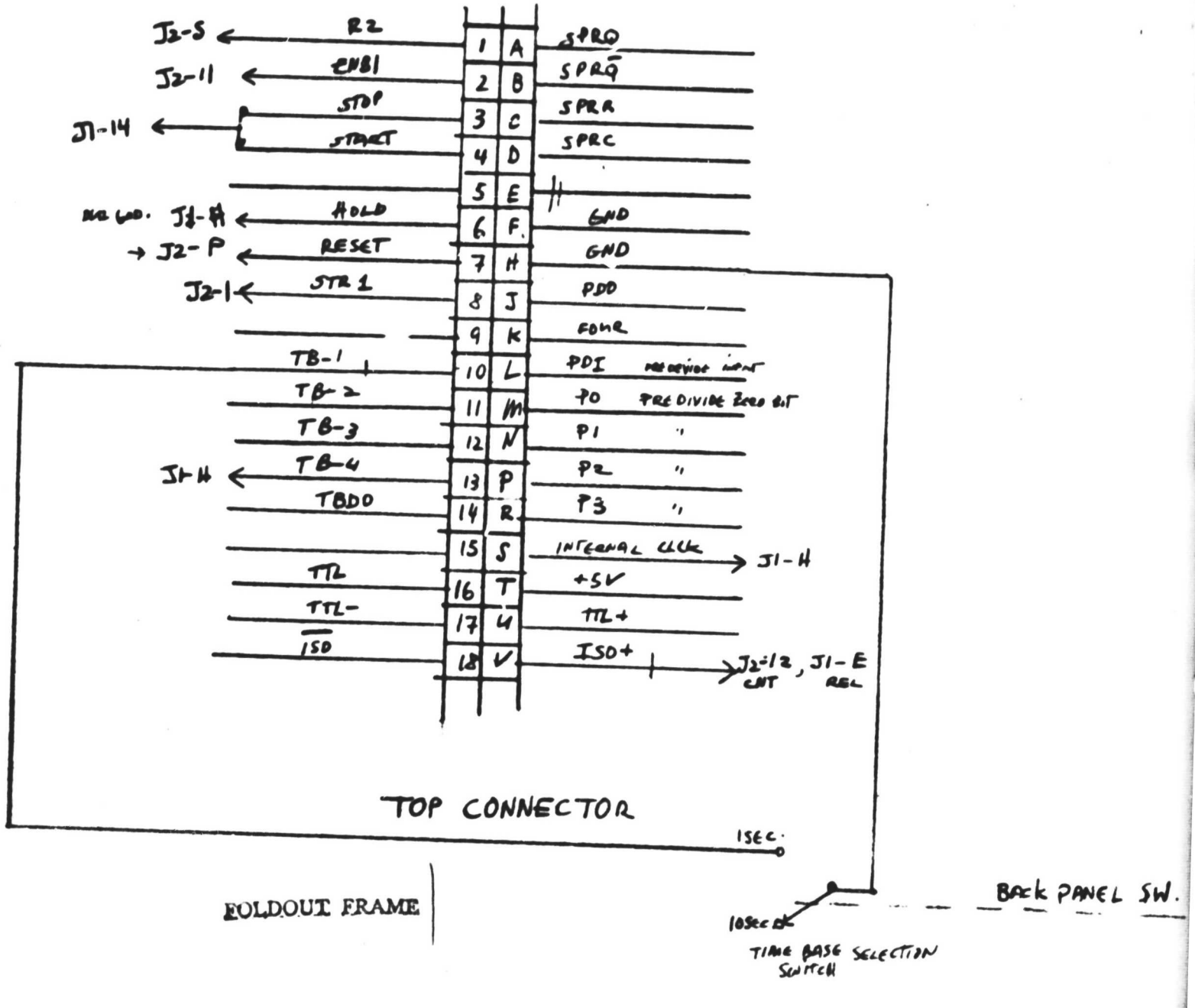
Wiring diagram of DM-31 interfacing board



FOLDOUT FRAME


1A FUSE
FRONT PANEL POWER SW
BACK PANEL METER ON/OFF
BARRIER TB
115V AC Hi
NEUTRAL
EARTH
LOGIC BOARD #2-14
LOGIC GND.
INPUT SIGNAL (AC COUPLED)
1
2
3
4
5
6

J1


J2-S
R2
J2-11
ENBI
J1-14
STOP
START
HOLD
RESET
J2-1
STR 1
TB-1
TB-2
TB-3
J1-H
TB-4
TBDO
TTL
TTL-
ISD
SPRQ
SPRQ̄
SPRA
SPRC
GND
GND
PDD
FDNR
PDI
PO
P1
P2
P3
INTERNAL CLCK
+5V
TTL+
ISO+
J1-H
J2-12, J1-E
TOP CONNECTOR
ISEC.
FOLDOUT FRAME
BACK PANEL SW.
10SEC
TIME BASE SELECTION SWITCH

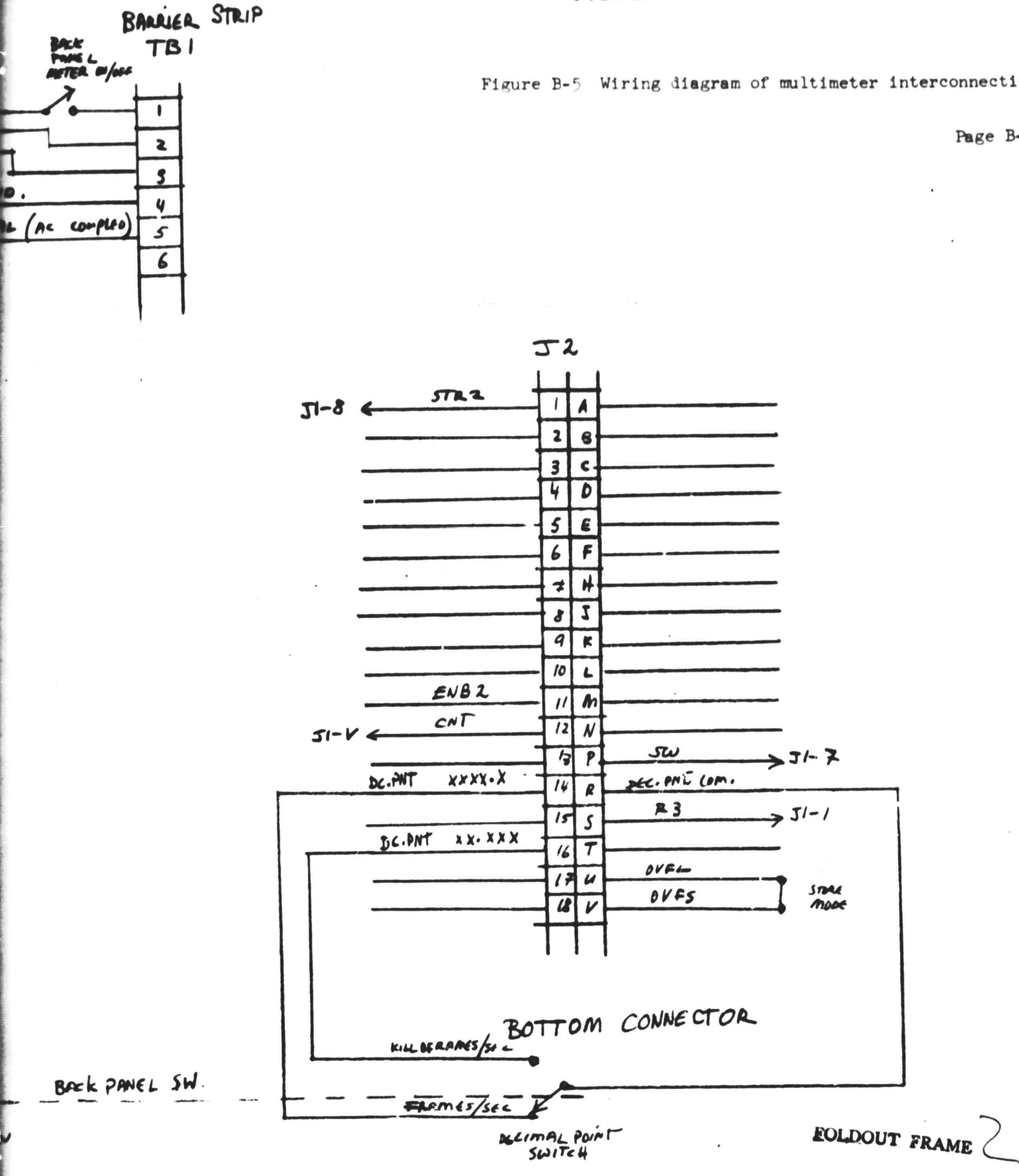


Figure B-5 Wiring diagram of multimeter interconnections

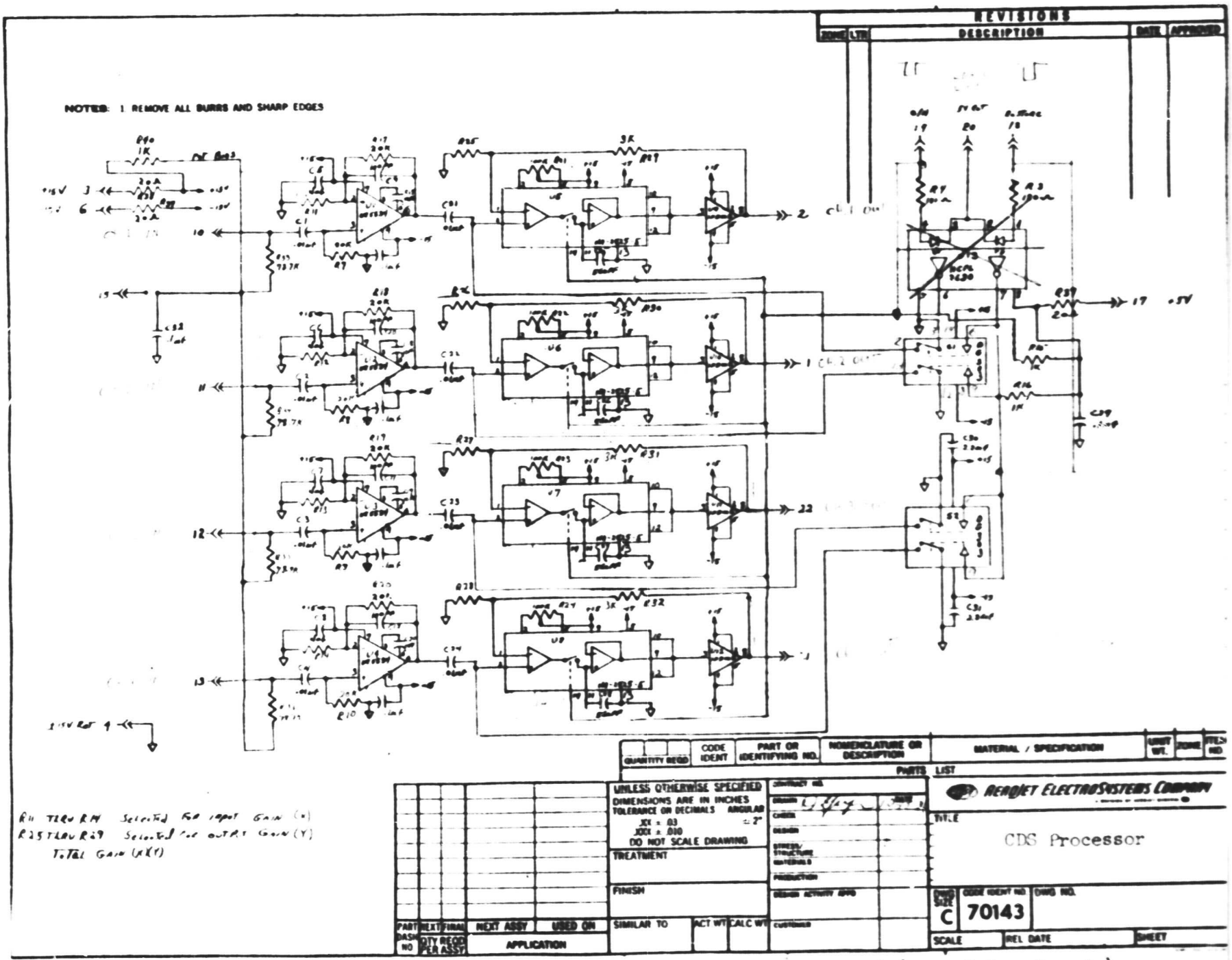


Figure B-6 Wiring diagram of CDS signal processor board (one of four boards)