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THE FEASIBILITY OF MINIATURIZING THE VERSATILE PORTABLE SPEECH PROSTHESIS: A MARKET SURVEY OF COMMERCIAL PRODUCTS

November 1981

Prepared for:

National Aeronautics and Space Administration
Technology Transfer Division
Code: ETT6
Washington, D.C. 20546

Attention: Ray L. Gilbert

Contract NAS2-10143

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Prepared by:

Tracy Walklet

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SRI Project 8134

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I INTRODUCTION AND BACKGROUND

The Technology Utilization Office at NASA Ames Research Center requested that the SRI Technology Applications Team (TATeam) quickly (in 1 month) analyze the feasibility of a miniature versatile portable speech prosthesis (VPSP) and gather information on its potential users and on other similar devices. The VPSP is a device that incorporates NASA speech synthesis technology. The objective of SRI's research was to provide information sufficient for NASA to decide whether it has valuable technology to contribute to the miniaturization of the VPSP and whether or not it should fund the development of a mini-VPSP. The scope of the TATeam's research encompassed identifying the needs of potential users, evaluating the development status of technologies similar or related to those used in the VPSP, and determining whether comparable computer-based speech synthesis devices are already available, or will soon be available, in smaller size.

In May 1978, the design of the VPSP, a computer-based speech synthesis system that would fit on a wheelchair, was initiated at the Rehabilitation Engineering Center of Children's Hospital at Stanford. The primary purpose of the project was to produce a device that would provide communication assistance--in educational, vocational, and social situations--to speech-impaired individuals. It was expected that the VPSP would be an especially valuable aid for persons who are also motor-impaired, thus the placement of the system on a wheelchair. The project was funded under a grant from the NASA Technology Transfer Division, Washington, D.C; the funds were routed through the NASA Ames Research Center University Affairs Office to Children's Hospital. Contributors to the project included staff of the Rehabilitation Engineering Center, consultants with expertise in psycho-linguistics and electronics, staff and patients of the Stanford Speech and Language Clinic and the San Francisco State University Department of Special Education, and equipment manufacturers. The Stanford University Biomedical Applications Team (BATeam) provided coordination between NASA and Children's Hospital. A single prototype VPSP system was constructed and tested between May and November 1979. Representatives of the potential user community had experimented with the VPSP by May 1980.

A second phase of the VPSP project was initiated in late 1979 and early 1980 with additional NASA funding. Hardware and software components of the system were refined, a videotape of its operation was made, a demonstration was held for equipment manufacturers, a request for proposals was distributed to organizations potentially interested in manufacturing the VPSP, and Computers for the Physically Handicapped (CPH) was selected to produce the VPSP commercially.

The VPSP is essentially a talking word-processing system, built around a specially designed operating system that is tailored to the abilities of a range of severely physically disabled persons. Figure 1 is a photograph of the system. It visually displays on a CRT (cathode ray tube) the user's control options and text and permits the user to generate, speak, edit, store, and retrieve text messages of unlimited vocabulary. The hardware components, placed in a metal box that fits on the back of the wheelchair, are an S-100 cardcage (housing a Cromemco floppy disc controller, a dynabyte 16K static memory board, a Cromemco Z-80 CPU card, and a custom interface board), a 5-1/4-inch disc drive, and a fan and its power inverter. Other hardware components include a Votrax ML-1 speech synthesizer (disassembled and repackaged in another metal box), a third metal box containing the power supply, a standard Hitachi 5-inch television set (this is the video monitor), and a 5-inch Realistic speaker. Four different user controls--a single switch, a five-switch arm, a joystick, and a keyboard--can be attached to the wheelchair with brackets, velcro strips, or clamps, as needed.

Three different software packages are available for the VPSP. One is designed primarily for those who can only operate a switch, another is designed for input via a standard (typewriter) keyboard, and a third is controlled by a joystick or a five-switch arm. The joystick/five-switch and the single-switch versions have some characteristics in common. In fact, because the software is modular, all three packages have many similar modules.

Although the VPSP is suitable for a certain (nonambulatory) user population, nonvocal persons who are ambulatory could benefit from a more portable and lightweight speech synthesis device. In November 1980, a NASA RTOPS (Research and Technology Objectives and Plans) was prepared proposing a feasibility study to consider whether designing a person-portable versatile speech prosthesis is possible; in effect, it would be a mini-VPSP that achieves the same functions and has the performance characteristics of the wheelchair VPSP prototype. The RTOPS has been revised and NASA is still evaluating it.

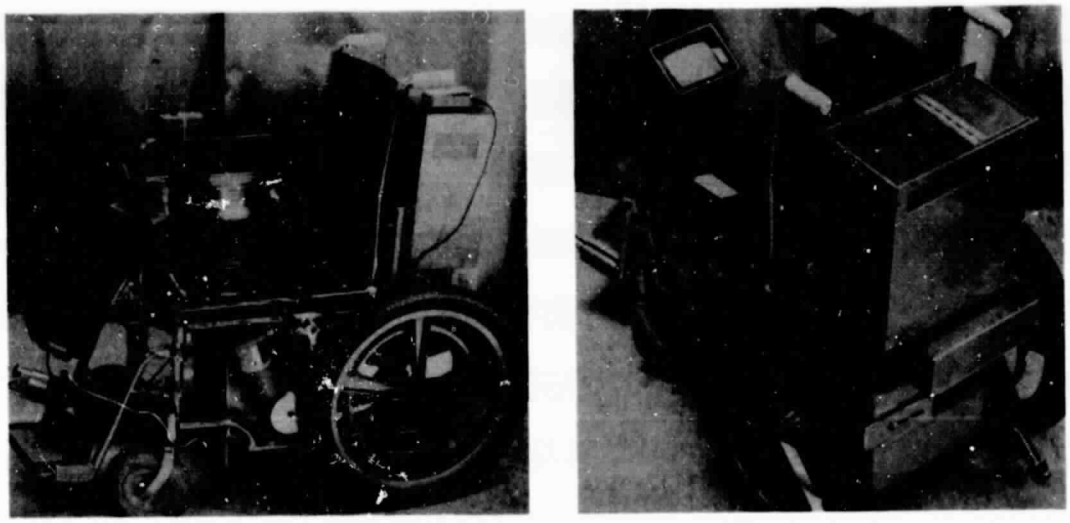


FIGURE 1 THE VERSATILE PORTABLE SPEECH PROSTHESIS

II PROBLEM DEFINITION AND APPROACH

The VPSP was designed as a tool for victims of cerebral palsy, multiple sclerosis, Parkinson's disease, muscular dystrophy, or cancer of the larynx and for stroke victims suffering from residual brain damage. A brief clinical evaluation with cerebral palsy and stroke victims revealed that the device is relatively useful, requires a short training period, and satisfies the needs of certain users.

The VPSP, however, also presents problems. During testing, the device proved to be somewhat awkward to operate, to be fragile (with wires becoming damaged and the memory disc unit drifting out of alignment), and, for a few users, to be too complex. For example, some users had difficulty in adjusting to the scanning cursor. In addition, the VPSP is too large and too heavy to be useful to ambulatory nonvocal persons.

The questions that must be addressed, then, are:

- What does the potential user population really need and want?
- Do the hardware and software components that comprise the VPSP represent the state of the art?
- Are these components available now or will they soon be available in smaller size; and, if so, is the quality of the more miniature components inferior, comparable, or superior to those currently incorporated in the VPSP prototype?
- Has anyone else made, or is anyone else designing, a smaller and lighter text-to-speech synthesis device that incorporates all or most of the VPSP functions?

The SRI TATeam's approach to achieving its research objectives and to answering some of the questions associated with the VPSP was twofold:

- To interview participants in the original VPSP project as well as other pertinent experts.
- To conduct a survey of the marketplace to determine the status of relevant technology development.

SRI TATeam members interviewed approximately 16 people by telephone and in person. Exhibit 1 lists the VPSP project staff and other speech synthesis experts who were interviewed. Exhibit 2 lists the equipment manufacturers that were contacted as part of the market survey.

In addition to the discussions with the people named in Exhibits 1 and 2, the TATeam obtained and reviewed product information from the companies listed in Exhibit 3.

Exhibit 1

PEOPLE WHO WERE INTERVIEWED

Participants in the Original VPSP Project

Gary Steinman, Assistant Director
Luke Brennan, Biomedical Engineer
Stanford University Biomedical Applications Team (NASA BATeam)
730 Welch Road, Suite 214
Palo Alto, California 94304
(415) 497-5353

Maurice LeBlanc, Chief
Rehabilitation Engineering Center
Children's Hospital at Stanford
520 Willow Road
Palo Alto, California 94304
(415) 327-4800, ext. 345

Carol Simpson
Psycho-Linguistic Research Associates
2055 Sterling Avenue
Menlo Park, California 94025
(415) 854-1771

People Involved with Speech Synthesis

Professor John Eulenberg
Artificial Language Laboratory
Computer Science Department
Michigan State University
East Lansing, Michigan 48824
(517) 353-6622

Dan Christinaz, Electronics Engineer
(Care of Dr. Kenneth Colby)
Department of Psychiatry
University of California at Los Angeles (UCLA)
Westwood, California
(213) 825-0043

Exhibit 1 (Concluded)

Gregg Vanderheiden
Cerebral Palsy Communication Group
Trace Center
University of Wisconsin
Madison, Wisconsin
(608) 262-6966

David Kolbus, Computer Speech Communication Expert
SRI International
(415) 859-2802

David Fylstra, Software Engineer
SRI International
(415) 859-2816

Exhibit 2

MANUFACTURERS CONTACTED DURING THE MARKET SURVEY

Votrax Division, Federal Screw Works
John McDaniel, Marketing Consultant
JHM Marketing Associates
216572 Matias
Mission Viejo, California 92675
(714) 586-9876

Texas Instruments
Kun-Shan Lin
Consumer Products Group
P.O. Box 10508, MS 5893
Lubbock, Texas 79408
(806) 741-2350

Texas Instruments
Laurie Kane
Speech Products Marketing Group
Midland, Texas
(915) 685-6683

Telesensory Speech Systems
Alan Yatagai, Marketing Manager
3408 Hillview Avenue
Palo Alto, California 94304
(415) 856-TALK
Jeff Ward, Sales Representative
(415) 964-9300

International Business Machines
Mike Manning, Sales Representative
San Mateo, California
(415) 573-3100

Hycom (a subsidiary of Sharp)
Dick Trembly, Marketing Manager
Special Products
16841 Armstrong Avenue
Irvine, California 92714
(714) 557-5252

Basic Communications
Tom Cannon
Ft. Collins, Colorado
(303) 226-4688

Exhibit 3

COMPANIES THAT PROVIDED PRODUCT INFORMATION

National Semiconductor
Santa Clara, California

EPSON (a subsidiary of Seiko)
Torrance, California

General Instrument
Hicksville, New York

Intel Magnetics
Santa Clara, California

Micro Switch (a division of Honeywell)
Freeport, Illinois

Cherry Electrical Products
Waukegan, Illinois

Kurzweil Computer Products
Cambridge, Massachusetts

Harris Semiconductor
Palo Alto, California

H-C Electronics
Mill Valley, California

III FINDINGS: COMMERCIAL PRODUCTS

This section presents the findings of the market survey conducted by the SRI TATeam. A variety of companies involved in the manufacture of components of the VPSP were surveyed. In some cases, discussions were held with company representatives and information was obtained on currently available and planned products; in other cases, only product literature was obtained. Some of the product literature is appended to this report.

The hardware components of the VPSP were identified, for the purposes of the survey, as follows: user control, microcomputer, display screen, speech synthesizer, memory, speaker, and power supply.

This section also addresses the software component of the VPSP and describes other speech prosthesis devices that are commercially available or that are currently being developed.

Hardware Components

User Control

Numerous standard keyboards as well as versatile, modifiable boards are available from Cherry Electrical Products. Cherry also produces snap-action switches that could be used as an alternative control mechanism with a device like the VPSP.

Micro Switch manufactures a combined key panel and printed circuit (PC) board, shown in Figure 2, on which alternative keyboard modules can be used. The keyboards can be as small as 12 inches x 4 inches x 2 inches and can weigh as little as 1.75 pounds.

Companies can be contacted to manufacture custom-made user controls, such as a headset or joystick; the joystick and five-switch arm for the VPSP were custom made. Figure 3 illustrates the user controls (other than the keyboard) for the VPSP.

Microcomputer

Microcomputers/microprocessors are available as standard items. The Z-80 and 8080 microprocessing units were used in the VPSP prototype. Others that have been used with speech synthesizers are the Intel 8085 microprocessor, the Motorola 6808 microprocessor, and the National Semiconductor COP400 microcontroller.

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

FIGURE 2 A MICRO SWITCH KEYBOARD

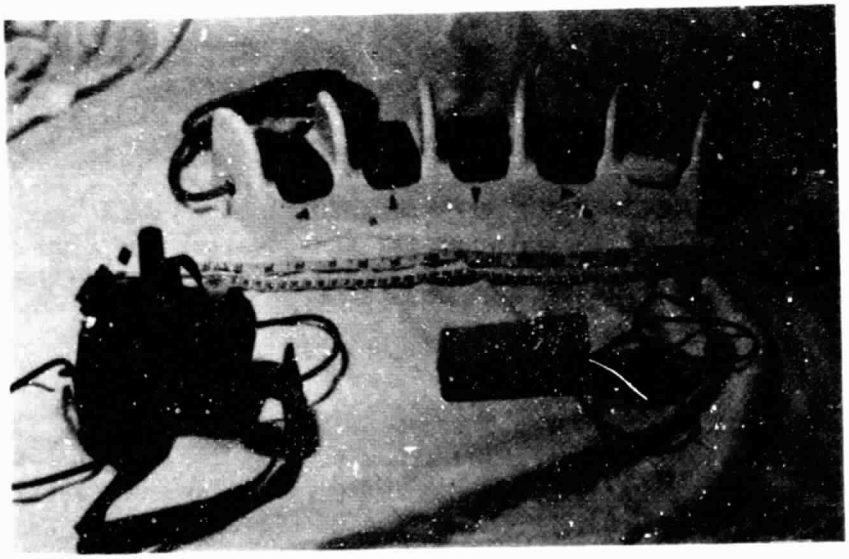


FIGURE 3 SWITCH AND JOYSTICK CONTROLS

Display Screen

Hycom, a subsidiary of Sharp, currently is marketing two types of model electroluminescent (EL) display panels; actual production of these panels will begin in 1982. Both models have full-field display and are available for alpha- numerics. Each weighs about 2 pounds. The larger is 4.8 inches x 10.1 inches x 1.5 inches and has 24 lines with 53 characters per line; it requires 13 watts of power and costs $2,900. After production begins, the prices will be $600 each for 5,000 units. The smaller EL panel is 1.8 inches x 7.1 inches x 1.7 inches and has 12 lines with 80 characters per line; it requires 11 watts of power and costs $2,800. When production starts, 5,000 EL panels will cost $550 each. Figure 4 is an example of the type of EL panel Hycom produces. Hycom is not planning to produce smaller EL panels. The current interface of these panels is different from that of an RS232 (a serial interface). To adapt the electronics to make the panels suitable for such applications as the VPSP, a $250 to $300 interface board would be required.

Epson produces alphanumeric liquid crystal display (LCD) modules that can be connected directly to any microprocessor, character generator, and random access memory (RAM). The largest is 7.09 inches x 2.72 inches x 0.75 inches and has four lines with 32 characters per line; a cursor can be displayed at any place by addressing it to the module. Figure 5 is a photograph of the larger Epson LCD module.

Popular Science (June 1981) reported that Hitachi, Toshiba, and Matsushita are expected to begin marketing LCD panels in 1982. None of these companies, however, provided the TATeam with information on their plans. The same article indicated that Sinclair Research (a British company) plans to introduce in 1982 a flattened CRT with half the volume of a conventional picture tube. This 3-inch CRT would be used on Sinclair's $125 Microvision minitelevision and may also be combined with the "ultra-compact" Sinclair personal computer.

Speech Synthesizer

Votrax is currently selling a Versatile Speech Module (VSM/1), a single board that costs approximately $995 and measures 12 inches x 6 inches. It incorporates a microprocessor (6800 Microprocessing Unit) that is programmable, storage capability, a SC-01 speech synthesizer, interfacing electronics, and amplifying electronics (8 ohm, 1 watt). The quality of speech from the VSM/1 is not as good as that from the ML-1 Votrax unit now used in the VPSP (the transitions are not as smooth and the sound production is not as accurate). Both systems are based on the formant speech synthesis technique.

Votrax also has a slightly larger single board synthesizer (the SVA) that provides more accurate speech and better transitional quality. It comes with a keyboard in suitcase size but does not have a display panel. The SVA board has an unlimited vocabulary text-to-speech synthesizer, a microprocessor, and amplifying electronics, but it has no storage capability for specific words and phrases.

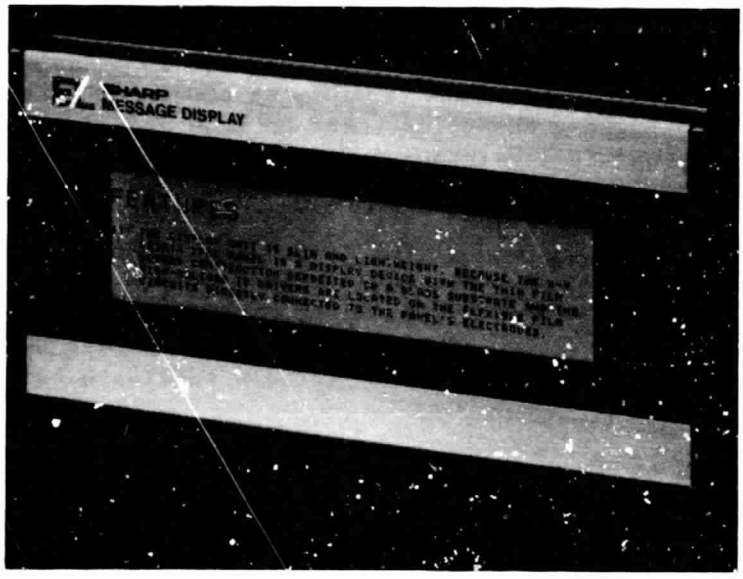


FIGURE 4 A SHARP EL MESSAGE DISPLAY UNIT

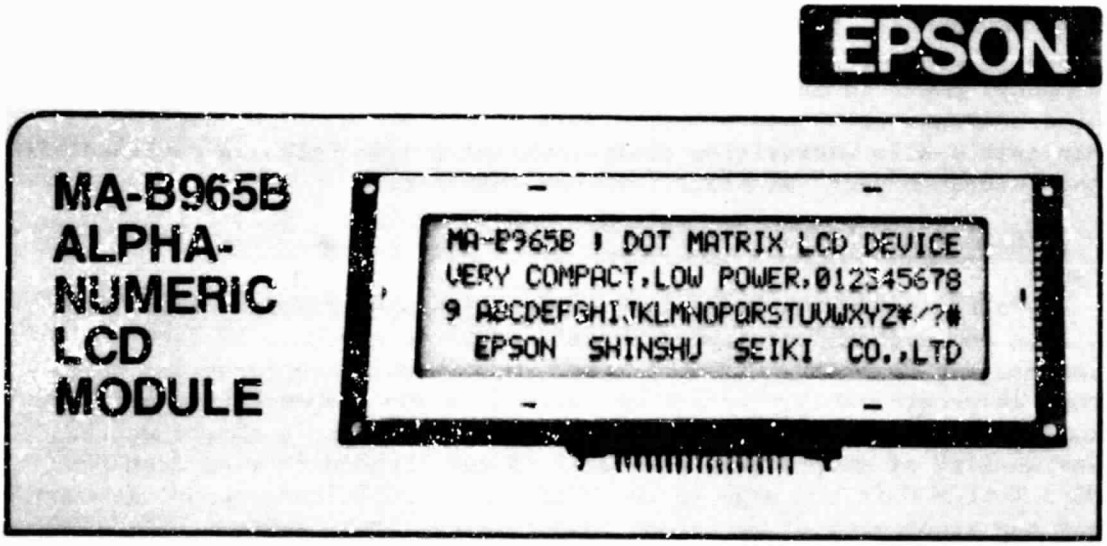


FIGURE 5 AN EPSON LCD MODULE

According to Mr. John McDaniel of Votrax, the VSM or SVA boards could be reduced to a single chip with synthesizer capability, for purposes of a system like the VPSP. This chip could be combined with other off-the-shelf chips for interface, amplifying, microprocessing, and storage.

Votrax plans to introduce a new speech synthesizer, the SC-02, that will have more human-sounding qualities than the SC-01 synthesizer. It will probably not be more expensive than, and is designed to replace, the SC-01. At present, Votrax intends to introduce the SC-02 in late 1982 or early 1983, but the company would be interested in cooperating with another organization to develop and introduce the SC-02 earlier than planned.

Telesensory plans to introduce a new speech synthesizer based on the formant technique in the spring of 1982. The synthesizer would be a single board 12 inches x 7 inches x 1 inch in size. The estimated price of the synthesizer will be between $3,000 and $4,000. The unit will have an unlimited vocabulary and a 1,500-word dictionary capacity. The board will have an RS232 connector and will be usable with American Standard Code for Information Interchange (ASCII) input; however, it will require a microcomputer and a memory device. The company is not planning to reduce the size of the board to a chip because it does not believe this would be cost-effective or that the technology for reducing a board to chip is satisfactory at this time. Within the next several years, however, Telesensory does plan to produce a better quality speech generator.

Texas Instruments has large-scale integration (LSI) voice synthesis processors (VSP) and voice synthesis memories (VSM) in volume production now. The TMS5200 single-chip VSP interfaces with 8- and 16-bit microprocessors; has an on-chip first-in, first-out (FIFO) buffer that allows speech data to be stored in the host microprocessor system or off-line on bubble memory or floppy disk; or can be used with the TMS6100 VSM for storage of 3,000 words of speech. The TMS5100 single chip interfaces with 4-bit microprocessors and can be used with up to 16 TMS6100 voice synthesis memories to store up to 30 minutes of speech. The TMS5100 and TMS6100 two-chip set is expected to cost $13 in late 1981. All TI speech synthesizers use the linear predictive coding (LPC) technique and can be be integrated with microprocessors, display, and interface functions in a custom module or board.

A TM990/306 speech module without standard vocabulary can be produced without erasable programmable read-only memory (EPROM), allowing the user to install solid-state speech vocabularies developed for his or her own application. However, for high-volume applications, user-specific vocabularies can be implemented on mask-programmed ROMs. The TI speech synthesizer provides more intelligible and more

human-sounding speech than the Votrax or Telesensory synthesizers; however, it does not have the unlimited vocabulary capability of the other two synthesizers.

The National Semiconductor DIGITALKER speech synthesis system is more limited in capability than the others. Based on the waveform digitization technique, it is more natural sounding; however, the MM54104 speech processor chip, for example, has only 256 possible addressable expressions.

Memory

Small memory units are available as chips in magnetic bubble form. According to an article in the May 1980 issue of IEEE Spectrum, bubbles are more reliable and smaller than disks (a single chip comes in a package not much larger than a semiconductor chip package), and they consume less power and have shorter access times. They also fit on the same board with a microprocessor.

Intel manufactures a bubble memory device capable of storing 1 megabyte of information on a 10 cm x 10 cm printed circuit board, as shown in Figure 6. It is available for less than $1,000 for one and for less than $600 for volume orders. Intel's bubble memory chip is 14 mm x 14 mm. Intel also produces other bubble memory sizes; the smallest, has a 128K capacity and provides nonvolatile storage.

National Semiconductor and Hitachi also produce bubble memory devices. The Hitachi unit plugs into the bus of such microprocessors as the 6800 and the 8080. National Semiconductor's bubble memory expansion module board measures 2.8 inches by 3.7 inches by 1 inch and weighs 3 ounces.

Speakers

Minispeakers are widely available, one manufacturer being Intervox. They have been in use for some time in such products as computer education toys. However, the quality of smaller speakers is not as good as that of the Radio Shack speaker currently used on the VPSP.

Power Supply

Rechargeable batteries are available in all sizes.

Software

The software for the VPSP seems to be the most sophisticated currently in use. There does not appear to be another speech synthesis system or device on the market or near development that has the scanning capability or rule-making capability of the VPSP. The device being

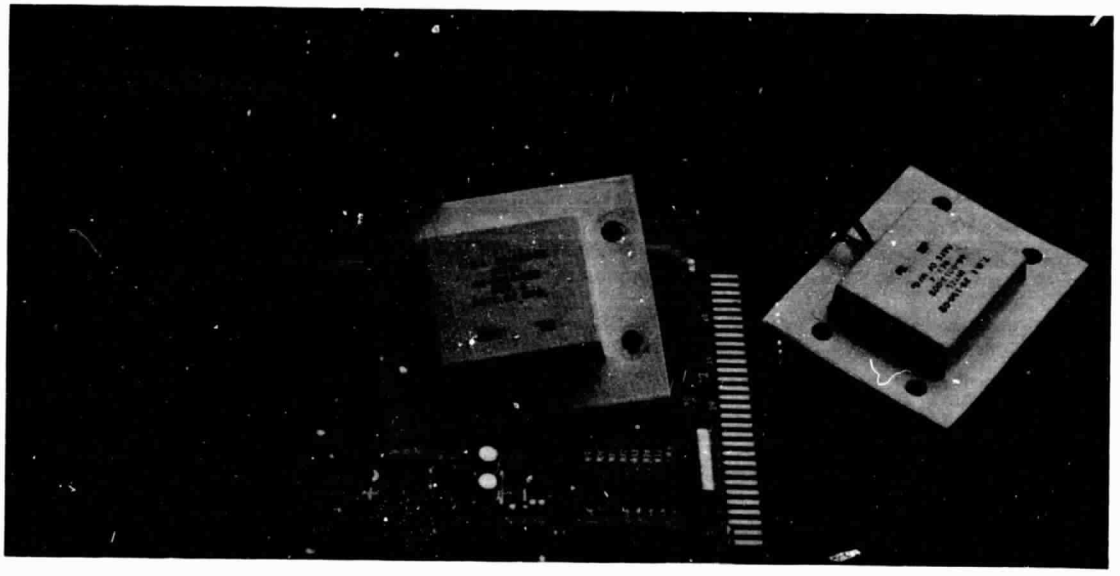


FIGURE 6 AN INTEL BUBBLE MEMORY BOARD

developed by Mr. Dan Christinaz at UCLA may have some (e.g., correction of misspelled words) but not all of the functions in the VPSP software package. Mr. Gregg Vanderheiden of the Cerebral Palsy Communication Group at the University of Wisconsin believes that the scanning algorithm and other combined functions of the VPSP make it the most advanced text-to-speech device available.

The SRI TATeam is not qualified to evaluate the possibilities of adapting the VPSP software package for use with much smaller hardware components. For example, we do not know the implications for the software of using a 128-character display screen or of using bubble memory storage. These uncertainties can best be answered by Carol Simpson of Psycho-Linguistic Research Associates.

Other Text-to-Speech Prosthesis Devices

A number of text-to-speech synthesis devices are currently being designed, demonstrated, or produced for speech-impaired and other handicapped people. The one that most closely resembles a mini-VPSP is the prototype device just constructed by Dr. Kenneth Colby (Department of Psychiatry) and Mr. Dan Christinaz (electronics engineer) at UCLA. It is a portable speech prosthesis device that is 5 inches x 10 inches x 3 inches in size (not including the battery and speaker) and weighs 7 pounds (not including the 3 to 4 pound battery). The device has the following components:

- A Votrax VSM single-board speech synthesizer with speech intonation, 3 inches x 5 inches in size (between $400 and $500).
- A Cherry alphanumeric keyboard similar to those used on terminals or typewriters ($100).
- An EPSON liquid crystal display (LCD) screen, 1-5/8 inches x 5-1/2 inches in size, with four lines and 32 characters per line ($250).
- RAM and EPROM memory chips, 38K to 40K in all, providing 2-1/2 months of memory life with two small batteries (donated by Texas Instruments).
- A 6-volt rechargeable Gates battery that lasts about 2-1/2 hours, contained in a 3- to 4-pound box attached to the device with a cord so that it can be hung around the waist of the user.
- An Intervox speaker, 1-1/2 inches x 2-1/2 inches square (of not very good quality) that can be used as a neck ornament and attached by a cord to the device.
- A serial RS232 port so that a control switch can also be used.

- A PC board ($200 to $300).

- Software that allows the user to program and store words or phrases but does not have menu selection.

The total cost of assembling this device, called the IST-1, was about $2,000 and the parts were purchased in single quantities. The reason for designing the speaker to be worn as a neck ornament is that people communicating with the user tend to talk to the speaker in the device rather than to the person operating it. With the speaker component around the neck, people will be more likely to respond to the user rather than to the device itself. Mr. Christinaz hopes to make 10 of these and provide them to potential users for testing. One reason for such tests would be to evaluate the sturdiness and reliability of the hardware package.

In addition to building and testing the IST-1 devices, Mr. Christinaz is attempting to construct more complex software that would predict words the user is spelling, that would correct misspelled words, and that would generally be more accurate. However, he is concerned that such a program would require an extensive memory (in the range of 256,000 bytes) and thus significantly more power--perhaps so much power that the battery would be too heavy to carry in conjunction with the other components.

Mr. Christinaz is anxious to find an organization that would help fund the construction of the 10 demonstration units and assist in the test program. Computers for the Physically Handicapped, among others, however, has not indicated much interest in providing such support.

Mr. Gregg Vanderheiden, at the University of Wisconsin, is attempting to develop a wearable keyboard that produces speech and printed text because he believes that nonvocal people need both types of outputs. He did not provide the details on this device.

According to Mr. John McDaniel, Votrax is currently selling the Type 'n Talk (TNT), which can be used in conjunction with a computer, for $345 (see Figure 7). The TNT has a microprocessor-based text-to-speech algorithm, unlimited vocabulary, a 750-character buffer, a 1-watt audio amplifier, RS232C interface, the SC-01 chip, and data echo of ASCII characters. The TNT is fairly compact but, unlike the VPSP, is not an independent system. Mr. McDaniel believes, however, that a speech synthesis system comparable to the VPSP could be packaged in calculator size with computer, display, and speaker included.

Telesensory has a prototype text-to-speech system called the TTS-X packaged in a 14 inch x 17 inch x 20 inch enclosure. It includes a 4-inch speaker (8 ohm), a 5-amp (110-volt) battery, and two LSI boards. A product demonstrator with a Litronix display panel and a Keytronics keyboard is currently being shown around the country. The speech

FIGURE 7 THE VOTRAX TYPE 'N TALK UNIT

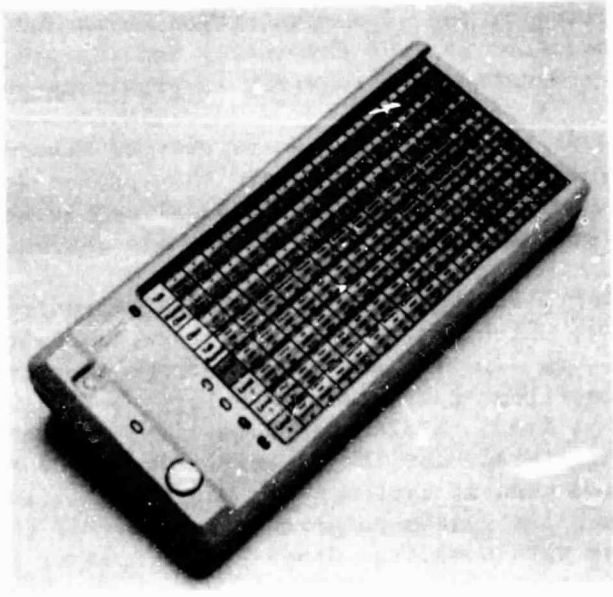


FIGURE 8 THE H-C ELECTRONICS HANDIVOICE

synthesizer is based on the formant code and sounds very much like the VPSP voice. Telesensory plans to have a commercial text-to-speech synthesizer available in early 1982 on a single 12 inch x 7 inch x 1 inch board. Telesensory may incorporate the soon-to-be-commercial speech synthesis board with its Autocom Lapboard Communication Aid, a device that is built for use on a wheelchair and has a magnetic board. When a pointer is used to touch a key indicating a word, letter, or number, it appears on a display or can be printed out.

H-C Electronics is currently marketing the Phonic Mirror Handivoice device, shown in Figure 8. The HC110 features 128 touch-sensitive display areas/keys on a flat board and two operating memories, each storing 50 entries for a total of 100 entries. Through the use of 373 words, 26 letters, 13 morphemes, and 16 common usage phrases, a kind of unlimited vocabulary is available. The Handivoice weighs 6 pounds and is 16-3/4 inches x 7-3/8 inches x 2-3/4 inches in size. However, it does not have a display screen or many of the qualities of the VPSP, such as menu selection.

Prof. John Eulenberg of the Artificial Language Laboratory at Michigan State University believes that the commercially available speech prosthesis devices do not particularly suit the needs of the users. He has built a variety of wheelchair-portable speech synthesis and printout systems, but he would also like to see more person-portable devices on the market. Specific features he is working on are a keyboard (with as few as 10 keys) strapped to the body and operable with one hand and a system that is based on body movements as the only user control.

IV CONCLUSIONS

User Needs

Mr. Vanderheiden believes that the menu selection and scanning cursor method used in the VPSP is too slow for most ambulatory speech-impaired persons and that many would like to have a faster-talking device. He feels that "high" technology such as the menu selection and scanning capability is not what is needed by the ambulatory speech-impaired user. Mr. Vanderheiden believes the best kind of device for such users would be one that can be programmed to suit an individual's speech needs and that is still portable. He believes that duplicating the VPSP in miniature would be difficult and that only with fewer functions could it be made portable.

Mr. Christinaz believes that the user and the people with whom the user communicates are more comfortable if the source of the speech (the speaker) is more naturally placed close to the head of the user rather than at a distance from the user inside the speech synthesis device. Otherwise, people are more likely to address themselves to the device rather than to the user.

Most of the people the TATeam interviewed agreed that those users who will be ambulatory will probably be able to use a keyboard control; the majority will not require another user control mechanism such as a switch because, if they have the motor control to walk, they will very likely be able to operate a keyboard.

Unfortunately, the TATeam could not conduct a detailed survey of user needs within the short time frame of this study. However, it would probably be advisable to do so before a decision is made on whether or not to proceed with miniaturization of the VPSP.

Is Miniaturization Feasible?

It appears that all the hardware components that would be required to make the VPSP person-portable are available. In some cases, the miniature components are more advanced than their counterparts used in the VPSP prototype. What remains to be done is determining the feasibility of adapting the software package for use with smaller hardware components and, if this can indeed be done, evaluating whether the result is the most suitable device for ambulatory speech-impaired persons.

Another uncertainty expressed by an SRI software engineer is the possibility of combining all the off-the-shelf components into a workable, well-packaged product. He was concerned about the complexity of "plugging in" all the hardware of varying sizes into a compact one-piece device. Not all the components are standardized at present.

Mr. McDaniel believes that it would be possible to design and build a calculator-size speech synthesis device with the SC-01 or SC-02 Votrax chip, a minicomputer, display panel, small speaker, and keyboard; but he believes that the menu selection function in the software would be a roadblock. Mr. McDaniel also said that Votrax would be interested in discussing the possibility of collaboration with NASA or others on such a project. If this were to occur, Votrax might be willing to accelerate development of its new, more intelligible SC-02 speech synthesizer chip.

Before such an effort is initiated, it would be advisable to examine and evaluate in greater detail the devices being developed by Mr. Christinaz at UCLA and by Mr. Vanderheiden at the University of Wisconsin. These two devices are the closest in capability to the VPSP and are designed for ambulatory speech-impaired persons.

Appendix

PRODUCT LITERATURE

TELESENSORY
Speech Systems
3408 Hillview Avenue • PO Box 10099
Palo Alto, California 94304
Our new phone number is (415) 856-TALK • Telex: 348352

SPECIFICATIONS OF PROTOTYPE TEXT-TO-SPEECH TTS-X

The text-to-speech prototype system will be constructed as a complete stand alone unlimited speech peripheral device. This system will consist of two TSI wire wrap boards, one TSI printed circuit board and nine printed circuit boards made by DEC mounted in a card cage. The card cage, power supply, speaker and tape cartridge will be packaged in a 14" x 17" x 20" enclosure. External user controls (switches, potentiometers, etc.) will be mounted on the front panel. The RS-232C connector used for I/O, the AC power cord and the fuse holder will be arranged on the back panel.

TSI will use materials and construction techniques consistent with the quality and reliability requirements of a laboratory evaluation prototype. The electronic hardware will be purchased from reputable manufacturers as OEM boards, OEM subsystems and components. The enclosures and other hardware required will be bought as "off the shelf" products -- TSI does not intend to fabricate them. The engineering staff at TSI will assemble, test, debug, and service the units we construct.

The specifications of the text-to-speech prototype are as follows:

1. Function -- The system will receive full words as strings of characters in ASCII format. These words are spoken in either lexical, prosodic, or spell mode.

> Lexical mode produces speech in which each word is pronounced with full normal stress (based on the lexical stress rules for words) without regard to the surrounding words.
>
> Prosodic mode produces speech which more closely resembles human speech in conversation; an entire phrase is analyzed before speech begins and each word is stressed with relationship to the surrounding words.
>
> Spell mode names each character in the input string.

The mode of operation shall be selected input control characters (ASCII). If the spell mode is not selected, the system will operate in the lexical mode for incoming text in ASCII format. The prosodic mode is used when the user wishes to replay a series of words which were received and stored in the 1000 character RAM buffer. This RAM buffer automatically stores the last 1000 characters received via the RS-232C input port. Using the appropriate ASCII control code the user may position a pointer to a word in the RAM buffer which will be the starting word for replay in the prosodic mode.

2. Vocabulary Size -- The text-to-speech system will speak an unlimited English vocabulary. The device incorporates a dictionary of 1500 exceptional words.

This dictionary is used for words which are most common in the English language and words which do not follow the typical phonetic rules of the language. Along with this dictionary is a set of algorithms which convert the other words to phonemes. A phonetic synthesis subsystem converts the resulting phoneme, stress, and duration data to speech parameters which drive the PDSP synthesizer to create the synthetic speech.

3. Maximum Vocabulary Length -- If the text-to-speech system is operated in the lexical mode (text being inputted to the system via the RS-232 port), the system can speak indefinitely at a maximum speaking rate of 200 words per minute. The minimum speaking rate is 50 words per minute. The speech rate is controlled from a front panel potentiometer.

For prosodic mode operation the maximum amount of words which can be read out is determined by the number of words that can be stored in the 1000 character RAM buffer. If we assume the average word length is seven characters, the total number of words is about 143. Because the text-to-speech system can speak any English word, any word or words can be stored in the RAM buffer.

In addition, the system has the ability to expand and pronounce common abbreviations. For example, "Dr." is expanded and pronounced as "drive" or "doctor" depending upon the context. Time, dates and monetary amounts are spoken as in conversational speech (e.g., "$13.26" is pronounced as "thirteen dollars and twenty-six cents"). Capitals embedded in lower case text are spelled (e.g., "the TSI speech board" is pronounced as "the T-S-I speech board").

4. Response Time -- The text-to-speech system's speech output will keep up with sentence input up to a rate of 200 words per minute.

5. Interface -- The text input will be in ASCII format at 1200 baud based on RS-232C specifications. The external user's control consists of variable speech rates between 50 - 200 words per minute, volume control, spell mode switch, buffer points control (forward and back). The power required is 110 V, 60 Hz, 4-5 amps.

6. Electronics - Three microcomputers (1x8085, 2xLSI-11), RAM, tape cartridge, Programmable Digital Signal Processor (PDSP) chips.

Because this prototype system will produce speech output given ASCII text string as input, the only equipment that should be prepared is a machine that can serve as an ASCII text string generator. The TSI text-to-speech system will do everything else.

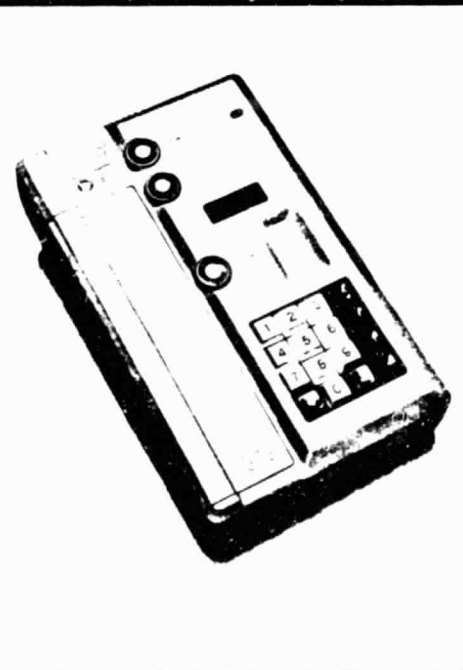
******

Lapboard style for Visual Display of Vocabulary. Uses interchangeable overlays of words, symbols or graphics.

373 words
45 phonemes (speech sounds for creating words)
26 letters (entire English alphabet)
13 morphemes (word prefixes/suffixes)
16 common usage phrases (i.e. "My name is . . .")

Features:

128 touch-sensitive display areas
4 selections per display area
8 selective functions including memory and repeat
2 operating memories with each storing 50 entries for a total of 100 entries
5 overlays: one thru four are illustrated and coordinated to the four individual instructional levels, and one blank overlay (grid) to accommodate symbols and graphics as desired in lieu of written language
Unlimited vocabulary through the combined use of morphemes, phonemes (prefixes/suffixes, sounds), letters and words
Portable and Manageable; weight 6 lbs. (2.72 kg), length 16¼" (41.25 cm), width 7⅜" (18.75 cm), depth 2¾" (7 cm)



Calculator style. All selections are initiated through 3 digit coding. Accommodates auxiliary switch systems.

888 words
45 phonemes (speech sounds for creating words)
26 letters (entire English alphabet)
13 morphemes (word prefixes/suffixes)
16 common usage phrases (i.e. "I want . . .")

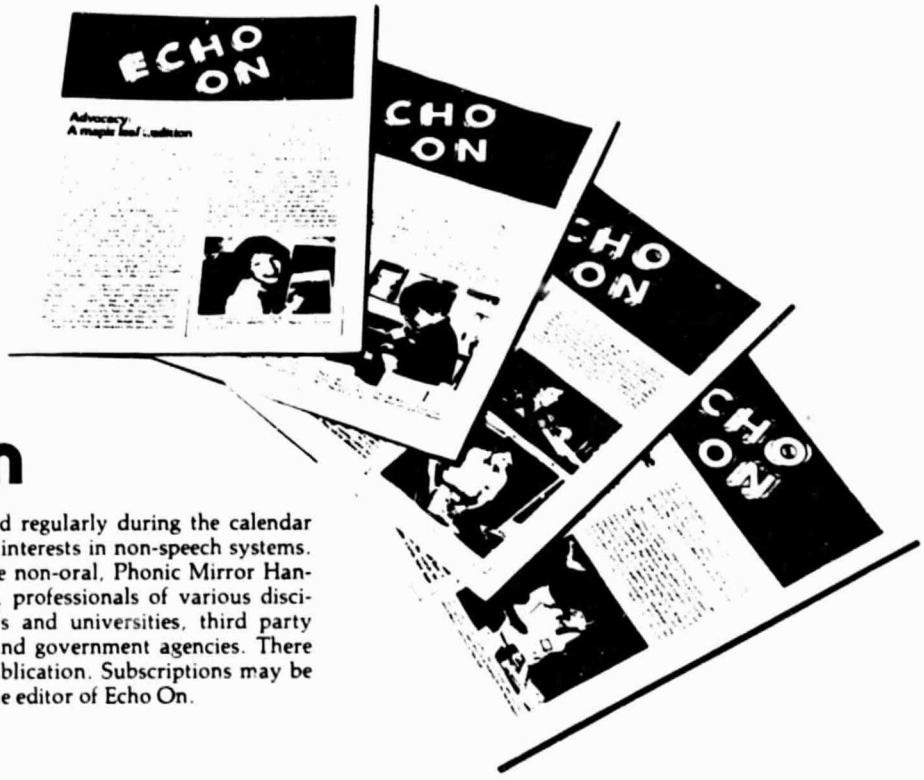
Features:

16 button keyboard
11 selective functions including memory and repeat
2 operating memories, with one storing 60 entries and the other storing 35 entries for a total of 95 entries
Audible and silent automatic storage and scanning when used with auxiliary controls.
Auxiliary breath, muscle or hand switch controls to accommodate the severely physically impaired to maximize their available motor abilities
Unlimited vocabulary through the combined use of morphemes, phonemes (prefixes/suffixes, sounds) letters and words
Portable and Manageable; weight 5½ lbs. (2.49 kg), length 11⅜" (29 cm), width 7⅛" (18 cm), depth 2¾" (7 cm)

In a world of instant communication the need and right to communicate vocally is essential. A segment of the population has been denied this basic tool because of various kinds of birth defects, brain damage, or injuries. Space-age technology has produced the Phonic Mirror HandiVoice, a portable electronic voice synthesizer that can communicate verbally virtually any word in the English language. For non-oral people the opportunity to communicate like their peers means more than just talking with an artificial voice. It marks the beginning of a new and meaningful life style. It can be an important beginning in reducing the physical limitations of non-oral people. Basic communication dependence is diminished while opportunities for schooling and jobs are realistically increased. For many the Phonic Mirror HandiVoice will become an augmentative means of verbal communication, while for others it will be a diagnostic instrument, and educational aid, or a therapy tool. For the family and friends it will enhance communications leading to better understanding for all concerned. Whatever its role, the Phonic Mirror HandiVoice will give non-oral people the opportunity to enlarge their participation within their particular environment.

Technology has resulted in a variety of speech prostheses. The Phonic Mirror HandiVoice, with its synthesized speech output, is not intended to be the panacea for all non-oral individuals. However, the first step is the professional assessment of the non-oral person's cognitive and motor skills together with an evaluation of the potential user's wants and needs. If the assessment and evaluation indicates that the non-oral person, in due time, can sufficiently upgrade his or her communications output, either model of the Phonic Mirror HandiVoice might be recommended. Consideration also must be given to a proper training program, a follow up program, and family involvement if the non-oral person is to derive full benefit from the Phonic Mirror HandiVoice. To this end both models of the Phonic Mirror HandiVoice are available at established Assessment/Evaluation centers throughout North America. All centers are staffed by accredited speech pathologists and occupational therapists. The Assessment/Evaluation center will assist the non-oral person and his family in selecting the most appropriate communications prosthesis to meet his present and future needs.

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH



Echo On

Echo On is published regularly during the calendar year for all those with interests in non-speech systems. Readership includes the non-oral, Phonic Mirror HandiVoice users, parents, professionals of various disciplines, medical schools and universities, third party funders, foundations and government agencies. There is no charge for the publication. Subscriptions may be entered by writing to the editor of Echo On.

Voice Pals

The Voice Pals program was instituted as a communications vehicle for Phonic Mirror HandiVoice users. Voice Pals is an updated version of pen pals, wherein Phonic Mirror HandiVoice users send and exchange cassette recordings with fellow users and sports, entertainment, and government personalities. Echo On serves as the clearing house for all Voice Pals. Voice Pals become more proficient with their Phonic Mirror HandiVoices while gaining a measure of self-esteem and self-confidence in knowing that their peers and famous personalities are receiving their communications and responding. Phonic Mirror HandiVoice users become Voice Pals by completing a general interest questionnaire and requesting cassettes and mailing cartons, for which there is no charge. 3 M contributes the cassettes and Phonic Mirror provides the special mailing cartons.

After an 18 month wait, I received my HandiVoice. Now I can call my girlfriend on the phone. Now that I have my HandiVoice, I hope to find a new job, possibly typing, and a new apartment. Right now I make jewelry and sell it to the public at the local Fairs.

- *USER*

We take the HandiVoice everywhere - to school, doctor, meetings. He even appeared on TV Easter Seal Telethon. We think the HandiVoice is the best thing ever to happen to our Cerebral Palsy son, 20 years old. Mounted on his wheelchair, the HandiVoice has become a part of him.

- *PARENT*

My best friend's speech deteriorated to a point where our telephone conversations and private talks were no longer possible. Our contacts had all but stopped. Then suddenly one evening I got this telephone call and a deep monotone voice announced "Laura this is Judi". I couldn't believe it! Judi . . .talking! It was a wonderful feeling to know that once more we could share our worlds of private thoughts.

- *FRIEND OF USER*

Before the students had the Phonic Mirror HandiVoice, they had to be mute while riding in cars because their mothers or drivers could not read "word boards" the students used. They never talked in the car before. Today they talked all the way down to San Diego.

- *SPEECH THERAPIST*

Because of the HandiVoice, my son has now been able to be mainstreamed into a public school, has been able to communicate with friends in person and on the telephone, has secured part-time jobs, can tape reports for his school projects by programming the machine with his thoughts and then tapingsthem for presentation in school.

- *PARENT*

The neighborhood children now accept my son without fear and reservation because they now can understand him and found he likes the same things they like. The Phonic Mirror HandiVoice has helped him to better accept himself. He was constantly frustrated trying to express himself and trying to invent ways for others to accept him. So the HV has undoubtedly become his link to the fun of really being understood, and enjoying participating with others. It's been one more key to us for unlocking the spasticity that holds our son captive.

- *PARENT*

Once the parent saw his child and the Phonic Mirror HandiVoice interface, the parent became enthusiastic. In one instance a child's vocabulary went from 5 to 200 words — the parent's expectations were fulfilled and communication at home increased dramatically.

- *LINGUIST*

Communication aids, such as the HandiVoice, are not luxuries; they are necessities. I know of no other physical handicap as great or having as great an effect on a person's psychological and sociological development as being unable to communicate. . . . The person who can't speak is a person who is ignored and a person who is ignored is a person who is stunted in his sociological development.

The names of the above are on file at the offices of Phonic Ear Inc. - *USER*

USA:
PHONIC EAR INC.
250 Camino Alto
Mill Valley, CA 94941
415/383-4000 TLX 172 164

Canada:
PHONIC EAR LTD.
7475 Kimbel Street Unit 10
Mississauga, Ont L5S 1E7
Canada
416/677-3231
TLX 06-968754
Phonicear MSGA

Outside North America:
PHONIC EAR INTERNATIONAL A/S
Formervangen 34
DK 2600 Glostrup
Copenhagen, Denmark
Phone (02) 45 85 66 TLX 33245 phonic dk

Printed in USA

822 2741-01 10R1

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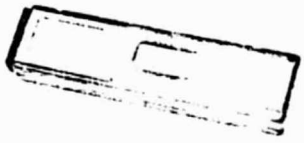
HandiVoice™

HC 120
Accessories

AT 135 Battery Pack



Rechargeable battery pack provides long life and reliability. Powers the unit for up to 10 hours of continuous use. Battery pack may be charged while the unit is operating but *only use the charger provided with the unit to prevent damage.*

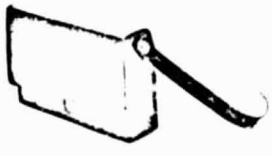
AT 141 Battery Charger

UL and CSA approved for 120V ~ 60 Hz operation. D, S and N approved for 220V ~ 50 Hz operation. Specify voltage when ordering. *Use only the battery charger provided with the unit.*

AT 151 Keyguard

Snaps over the keyboard to allow people with limited motor skills to accurately activate the keys. Provides separation to prevent activation of more than one key at a time.

AT 152 Carrying Case



Custom-fitted real leather case provides good protection for the unit. Easy-opening flap gives access to controls and keyboard without removing case. Comes with adjustable carrying strap and mounting hardware.

AT 140 Carrying Strap

Adjustable shoulder strap for easy carrying of the unit. Attaches to built-in threaded bosses on either the sides or ends of the unit. Mounting hardware supplied with the strap.

AT 153 Vocabulary Card Kit

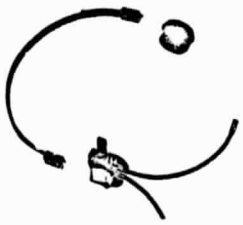
Seven vocabulary card set provides easy access and reference to words, sounds and phrases. Included are numeric and alphabetic vocabulary listings, sample word combinations, common male and female names, phonetic key and vocabulary categories.

AT 168 Accessory Kit

Includes AT 133 Sound Switch, AT 134 Pedal Switch, AT 160 Touch Switch, AT 161 Leaf Switch, two AT 162 Cable Assemblies, one AT 151 Keyguard and one AT 140 Carrying Strap.

823-2828 1-01 778

AT 133 Sound Switch



Activated by any sound: grunting, tongue clicking or blowing. Lightweight (1 oz.). Durable steel headband and soft foam temple pads provide stability and comfort. Headband and microphone are fully adjustable. Comes with permanently attached cable assembly.

AT 134 Pedal Switch

Activated by gross movements of hand or foot. Gives good audible reinforcement and physical feel of the switching function. Requires less than 5 ounces of force applied to center. Provides large target area and rugged construction. Can be screw-mounted for stable positioning. Comes with AT 162 Cable Assembly.

AT 160 Touch Switch

For use by people with extreme motor limitations. Activated by very light touch and small deflection. Deflection required can be adjusted. Can be screw-mounted for head or hand operation. Comes with AT 162 Cable Assembly.

161 Leaf Switch

For use by people with moderate motor limitations. Can be activated by chin, lateral arm movements or other movements with moderate control. Deflecting leaf in either direction activates switch. Can be rod- or screw-mounted in any position. Comes with AT 162 Cable Assembly.

AT 162 Cable Assembly

Used with AT 134 Pedal Switch, AT 160 Touch Switch or AT 161 Leaf Switch. Cable is 6 feet long with 3.5 mm Mini-Phone plug molded on each end.

HC Electronics, Inc.
250 Camino Alto
Mill Valley, CA 94941
415/383-4000

PHONIC EAR LTD.
2688 Slough Street
Mississauga, Ont., L4T 1G3
416/677-3231

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DK 2600 Glostrup Copenhagen
Phone (02) 45 85 66

TYPE-'N-TALK™ IS T.N.T.

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- **Built-in text-to-speech algorithm**
- **70 to 100 bits-per-second speech synthesizer**

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English text is automatically translated to electronically synthesized speech with Type-'N-Talk™. ASCII code from your computer's keyboard is fed to Type-'N-Talk™ through an RS-232C interface to generate synthesized speech.

Just enter English text and hear the verbal response (electronic speech) through your audio loud speaker. For example: simply type the ASCII characters representing "h-e-l-l-o" to generate the spoken word "hello."

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Type-'N-Talk™ has its own built-in microprocessor and a 750 character buffer to hold the words you've typed. Even the smallest computer can execute programs and speak simultaneously. Type-'N-Talk™ doesn't have to use your host computer's memory, or tie it up with time-consuming text translation.

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Place Type-'N-Talk™ between a computer or modem and a terminal. Type-'N-Talk™ can speak all data sent to the terminal while online with a computer. Information randomly accessed from a data base can be verbalized. Using the Type-'N-Talk™ data switching capability, the unit can be "de-selected" while data is sent to the terminal and vice-versa — permitting speech and visual data to be independently sent on a single data channel.

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Look what you get for $345.00. TYPE-'N-TALK™ comes with:

- Text-to-speech algorithm
- A one-watt audio amplifier
- SC-01 speech synthesizer chip (data rate: 70 to 100 bits per second)
- 750 character buffer
- Data switching capability
- Selectable data modes for versatile interfacing
- Baud rate (75-9600)
- Data echo of ASCII characters
- Phoneme access modes
- RS-232C interface
- Complete programming and installation instructions

The Votrax Type-'N-Talk™ is one of the easiest-to-program speech synthesizers on the market. It uses the least amount of memory and it gives you the most flexible vocabulary available anywhere.

Order now. Toll free.

Call the toll-free number below to order or request additional information. MasterCard or Visa accepted. Charge to your credit card or send a check for $345.00 plus $4.00 delivery. Add 4% sales tax in Michigan.

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Votrax

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Type-'N-Talk™ is covered by a limited warranty. Write Votrax for a free copy.

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMS 5100 VOICE SYNTHESIS PROCESSOR DATA MANUAL

PRELIMINARY
OCTOBER 1980

TEXAS INSTRUMENTS
INCORPORATED

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1. INTRODUCTION

The TMS 5100 is a PMOS voice synthesis processor (VSP). Speech is synthesized by processing an externally provided variable-data-rate bit stream of encoded speech data and converting the result to an audible output with an on-chip eight-bit D/A converter and push-pull amplifier. The TMS 5100 was designed to be used with one or more TMS 6100 128K-bit (ROM) voice synthesis memories (VSM) and therefore outputs all control signals necessary for direct interface. Control of the VSP is normally provided by an external device (e.g., TMS 1000) through four control pins and a command clock.

2. THEORY OF OPERATION

2.1 LINEAR PREDICTIVE CODING

Linear predictive coding (LPC) synthesizes human speech by recovering from the original speech enough data to construct a time-varying digital filter modeling the voice tract and exciting this filter with a digital representation of either glottal air impulses or the rush of air that produces unvoiced sounds.

The TMS 5100 design is based on a 40-Hz frame rate (the rate at which new speech data -- a maximum of 49 bits/frame -- is obtained from the external memory), and an 8-kHz sample rate which corresponds to a maximum output frequency of 4 kHz. Each 49-bit frame defines excitation and filter characteristics that are linearly interpolated (every 3.125 millisecond) to be smoothly time-varying throughout the 25-millisecond interval between frames. This allows a relatively low (1960 bits/sec maximum) data rate to produce high-quality speech. The data rate is actually slower than this since certain speech parameters are not necessary in some instances, as described in the next section.

DATA FORMAT – FRAMES

Each 49-bit frame is composed of 13 parameters:

(1) Energy (amplitude – four bits);
(2) Repeat bit;
(3) Pitch (frequency – five bits);
(4) Ten reflection coefficients (K parameters – K1, and K2, five-bits each; K3-K7, four-bits each; K8-K10, three-bits each).

The K parameters are used to define the vocal tract transfer function.

A full set of parameters for each frame would require a data rate of 40 Hz X 49 bits = 1960 bits/second. Three special cases, in which a full frame is not necessary, allow the data rate to be considerably reduced:

(1) Since the vocal tract changes shape relatively slowly, it is often possible to repeat previous reflection coefficient data. If the repeat bit is set to a 1, the K parameters from the previous frame are used and no more data is accessed from memory. This makes repeated frames only 10 bits in length (4 energy, 1 repeat, 5 pitch)

(2) Unvoiced sounds (such as s, f, t, sh) require fewer reflection coefficients. When pitch = 00000, only K1-K4 are used. K5-K10 are internally zeroed, making an unvoiced frame of 28 bits (4 energy, 1 repeat, 5 pitch, K1 and K2 – five bits each, K3 and K4 – four bits each).

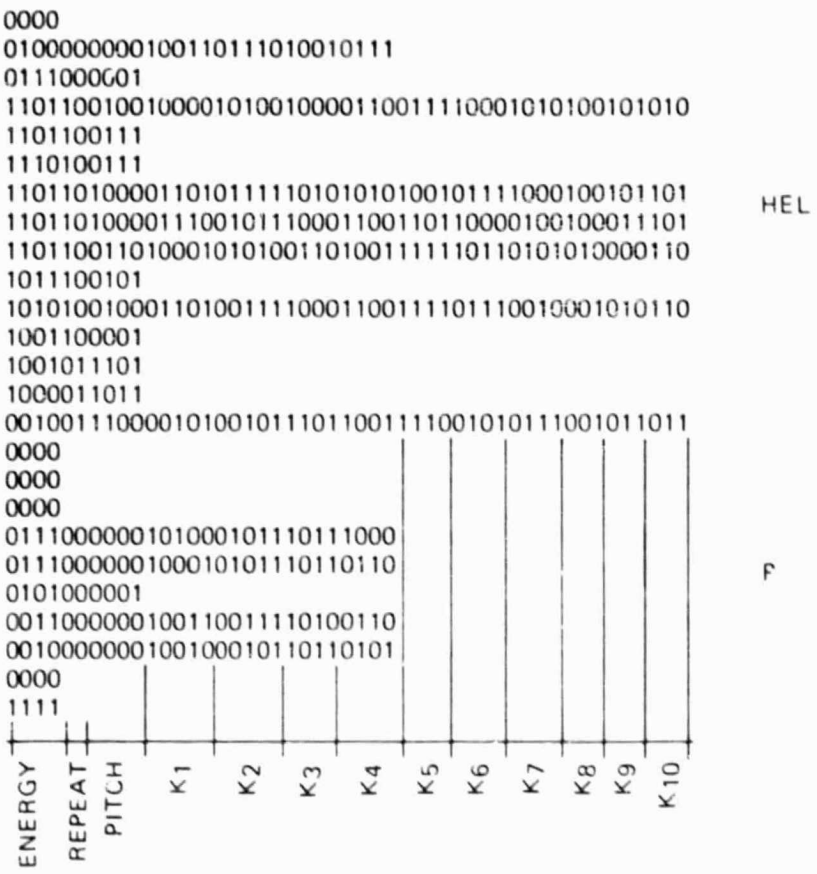
(3) When energy = 0000, no other data is required. Energy is zero during interword or intersyllable pauses. When energy = 1111, it is detected as an end-of phrase and the TMS 5100 stops talking. Both of these cases yield a four-bit frame.

The combination of these three cases has reduced the average data rate to nominally 1200 bits/sec.

EXAMPLE PHRASE – "HELP"

Table 1 shows the word "HELP" bit by bit, frame by frame.

TABLE 1 – HELP



2.2 TMS 5100

The TMS 5100 is controlled by commands on five pins: the Control Bus (CTL 1,2,4,8) and the processor data clock (PDC) (see Table 2). A command is first set up on the Control Bus (with the PDC low), then strobed into the device by toggling the PDC (low – high – low). Multi-nibble commands, such as Load Address, are executed by strobing in the command first, then setting up the data on the Control Bus and toggling the PDC. The beginning of each command description gives the binary form of each command.

TABLE 2 – TMS 5100 COMMAND LIST

NAME	CONTROL BUS CONTENTS CTL8 (MSB)	CTL4	CTL2	CTL1 (LSB)	PDC'S REQUIRED
RESET	0	0	0	X	1
LOAD ADDRESS	0	0	1	X	2
OUTPUT	0	1	0	X	3
READ BIT	1	0	0	X	1
SPEAK	1	0	1	X	1
READ & BRANCH	1	1	0	X	1
TEST TALK	1	1	1	X	3

X = don't care

2

RESET

The Reset command (000X) is used to synchronize a command sequence. Since there are some multi-nibble commands (such as Load Address, which requires a Load Address command followed by address data), the TMS 5100 may not be ready to accept a command, for example, when the device is expecting data in a load address sequence. The Reset command must be executed three times to ensure that the next toggling of the PDC will strobe in a command, not data.

The Reset command can also be used to halt speech. The execution of the Reset command while the TMS 5100 is talking completely halts the device but does not clear any internal registers. This allows the rest of the phrase to be spoken upon subsequent execution of the Speak command.

LOAD ADDRESS

This command (001X) loads the address of a phrase contained in a VSM, i.e., TMS 6100. This is a two-nibble command, the first nibble is the Load Address command (001X). Once that has been toggled in, the TMS 5100 expects the data on the Control Bus to be four address bits. Upon toggling the PDC, the chip gates this address (along with the proper control signals) to the VSM. This two-nibble sequence is repeated as many times as necessary to complete loading of the VSM address register. For example, the TMS 6100 requires five Load Address sequences, i.e., it takes exactly ten toggles of the PDC to load an address.

READ & BRANCH

This instruction (110X) is an "indirect load address" command for a single ROM system. First an address is loaded. This is the address of a word in the VSM that contains the address of data that the user desires. The Read and Branch command is now executed and the VSM address register is loaded with the contents of the ROM byte (specified in the Load Address sequence), and the next consecutive byte. In this manner a look-up table of phrase addresses can be stored in the VSM and easily accessed. The execution of this command also performs a dummy read so that a Read Bit or Speak command can be immediately executed to access data or begin speech. (Note: the addressed byte holds the MSB's of the VSM address. The next sequential byte holds the eight LSB's of the VSM address.) The VSM uses only the 14 LSB's of these two bytes, and therefore the Read and Branch command is local to only one VSM, i.e., a look-up table for data must be on the same chip as the data itself.

SPEAK

This command (101X) is used to start the TMS 5100 talking. After an address has been loaded and a dummy read performed (see Figure 1), this command is toggled into the TMS 5100 and it immediately begins transferring data from the VSM and talking. The speech can now be interrupted by the Reset command, if desired, and restarted later by simply toggling the Speak command into the device again. If no Reset command is issued during the speech, the device continues talking until it detects an end of phrase datum (see Sections 4.2 and 4.3).

TEST TALK

The Test Talk command (111X) was created so that the controlling device would know when the TMS 5100 is finished talking. This is a three PDC command: the first PDC clocks in the command, the second gates the status of the talk latch in the device to CTL1 and enables the CTL output buffers, the third returns the CTL pins to inputs. After the falling edge of the second PDC, CTL1 will be high if the TMS 5100 is talking, and as soon as the device detects an end of phrase datum, it will go low indicating the end of speech. Note that no commands will be understood by the device until the third PDC is used, since the CTL output buffers are enabled. (See Figure 1). Also note that the method of issuing two Reset commands (see Reset command section) would also guarantee the next toggle of the PDC to mean a command exists on CTL.

READ BIT/OUTPUT

The Read Bit command (100X) is used for two reasons: (1) reading data out of the VSM in conjunction with the Output command (010X), and (2) changing the direction of the ADD8/Data line from VSP output to VSP input (a "dummy read" option prior to using a "Speak" command).

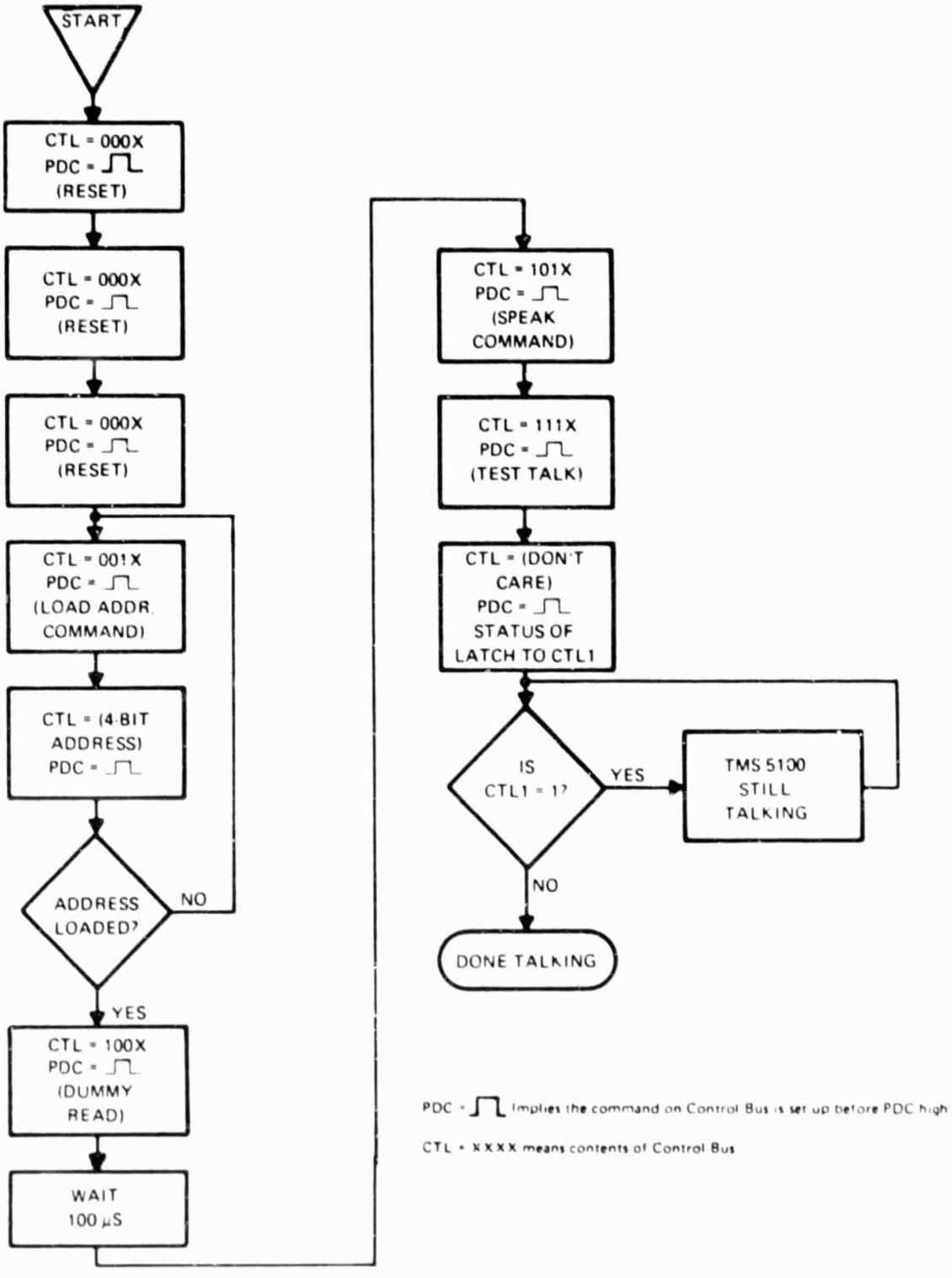


FIGURE 1 – OPERATION FLOW – TALK COMMAND SEQUENCE

Data can be read out of the VSM by

(1) Loading a 20-bit address,
(2) Performing a dummy read,
(3) Performing four Read Bit commands sequentially to load the 4-bit data buffer in the TMS 5100,
(4) Toggling the PDC with an Output command on CTL,
(5) Toggling the PDC again to return the CTL pins to inputs,
(6) Toggling the PDC again to return the CTL pins to inputs,
(7) Going to step 4 and repeating until all needed data is obtained.

Data is transferred between the VSM and the speech synthesizer over the ADD8 pin. Since this pin is usually an input on the VSM and an output on the TMS 5100, a dummy read is required to reverse the data flow so that data is now transferred in the other direction. This need only be performed when a new address is loaded, as the correct direction of data flow will still be set in cases such as interrupted speech or in between sequential data reads (see M0 Transfer Bit section).

3. OPERATION OF TMS 5100 VS/P WITH TMS 6100 VS/M

This section is intended as an aid for those who may desire to interface the TMS 6100 ROM to the TMS 5100. The following sections describe the timing of the control signals (ADD1, ADD2, ADD4, ADD8, ROMCLK, M0, and M1) that the TMS 5100 provides to the ROM. It is suggested that the reader obtain a copy of the TMS 6100 specification to further clarify this discussion.

DESCRIPTION OF THE TMS 6100

The TMS 6100 contains an auto incrementing address register; no further load address sequences are needed if the data is sequentially positioned in the ROM. See Figure 2 for operation flow.

The TMS 6100 is a mask programmable 128K bit Read-Only Memory internally organized as 16K words of 8 bits; externally it appears as 128K X 1. Once the 20 bit address (14 bits to select a byte within the device, 4 chip select bits, 2 bits ignored) is loaded through ADD1, ADD2, ADD4, and ADD8 in five Load Address sequences, data is read out bit wise by toggling a control pin M0. The ROM contains an on-chip address counter which is incremented every eight bits (eight toggles of M0). The four internal chip select bits are a mask programmable option, and allow parallel connection of up to 16 ROMs (about 30 minutes of speech) without the need of external select circuitry.

M1 – LOAD ADDRESS

The TMS 5100 loads an address to the TMS 6100 using the ADD bus and M1 control pin. As the PDC is brought high during the address portion of a load address sequence, the TMS 5100 brings M1 high and gates the CTL bus to the ADD bus. When the PDC is brought low, M1 goes low and the TMS 6100 stores the nibble in its address register. This 18-bit register is filled after five toggles of M1 (ten toggles of the PDC, as M1 stays low when the Load Address command (001X) is clocked in).

M0 – TRANSFER BIT

Data is transferred from the ROM to the TMS 5100 over the ADD8 pin. Toggling M0 instructs the ROM to transfer the next required bit. As the PDC is brought high during a Read Bit command, the TMS 5100 toggles M0 and accepts the new bit into its four bit buffer over the ADD8 pin. The first M0 after a load address sequence changes the direction of the ADD8/Data line.

ROM CLOCK

The TMS 6100 requires a clock input of from 100 kHz to 200 kHz. This clock is used to perform shifting and locating of data within the device. All pulses of M0 or M1 must be made in synchronization with this clock as shown in the timing diagrams.

It is suggested that any circuitry emulating the TMS 6100 be designed to be synchronous with the ROM CLK output of the TMS 6100, or inconsistent results may be obtained.

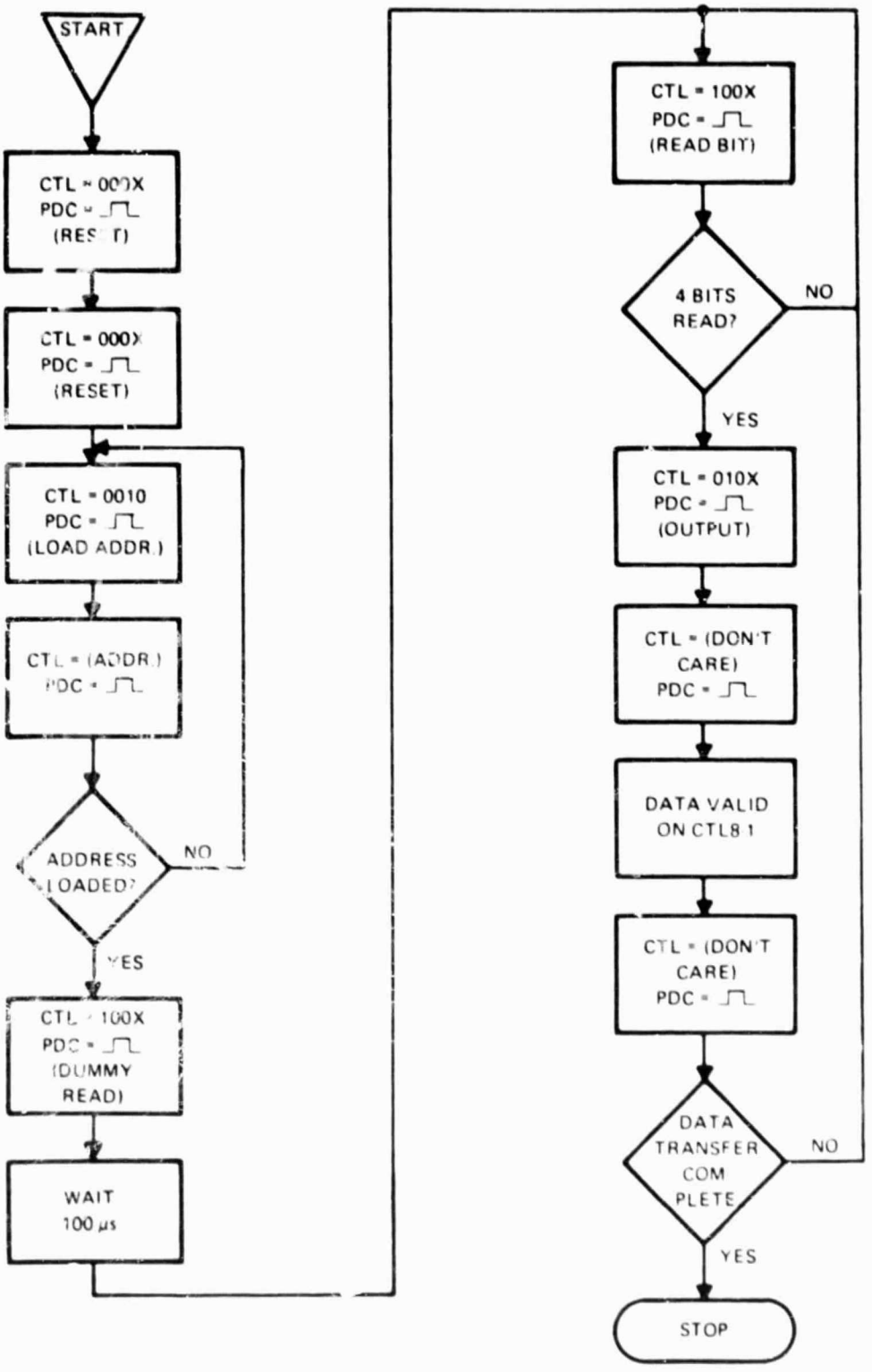


FIGURE 2 – OPERATION FLOW – READ/OUTPUT COMMAND SEQUENCE

4. TMS 5100 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS* OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply Voltage, V_{DD} (see Note 1)	−20 V to +0.3 V
Voltage applied to any device pin	−24 V to +0.3 V
Storage temperature	−30°C to +125°C
Operating temperature	0°C to +70°C
Continuous power dissipation	600 mW

NOTE 1: All voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or beyond those listed under the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may effect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	−8.3	−9	−9.7	V
High-level input voltage (see Note 2)	−0.7		0	V
Low-level input voltage (see Note 2)	V_{DD}		−4	V
Oscillator frequency (external RC)	608	640	674	kHz
Operating free-air temperature, T_A	0	25	70	°C

4.3 ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE, V_{DD} = −9 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX (See Note 2)	UNIT
V_{IH}	High-level input voltage	ADD8		−0.7		0	V
		CTL1, CTL2, CTL4, CTL8, PDC		−0.95		0	
V_{IL}	Low-level input voltage, all inputs			−24		−4	V
V_{OH}	High-level output voltage	ROM CLK, CPU CLK, I0, I1, ADD1, ADD2, ADD4, ADD8	I_{OH} = 100 μA	−0.5		0	V
		CTL1, CTL2, CTL4, CTL8		−0.7		0	
V_{OL}	Low-level output voltage, all outputs		I_{OL} = 100 μA	V_{DD}		−5	V
I_{IH}	High-level input current		V_I = 0 V			100	μA
I_{IL}	Low-level input current		V_I = −21 V			50	μA
I_{DD}	Supply current		All inputs and outputs open		20	45	mA
	Power output to speaker		100 Ω speaker load, 50 Ω each output	30			mW

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4.4 TIMING REQUIREMENTS, DATA OUTPUT AND I/O MODE SWITCHING (TEST TALK, OUTPUT) SEE FIGURE 3

PARAMETER		MIN	MAX	UNIT
t_{sv}	CS setup time	0		μs
t_{wH}	Pulse width, PDC high	1		cycle
t_{wH}	Pulse width, PDC high, f_{osc} = 640 kHz	6.25		μs
t_{wL}	Pulse width, PDC low	1		cycle†
t_{wL}	Pulse width, PDC low, f_{osc} = 640 kHz	6.25		μs

† Typical values are at T_A = 25°C.

‡ Cycle refers to the equivalent time in CPU clock cycles.

4.5 TIMING REQUIREMENTS, COMMAND AND DATA TRANSFER (LOAD ADDRESS, RESET, READ BIT, READY BRANCH, SPEAK) SEE FIGURE 4

	PARAMETER	MIN	MAX	UNIT
t_{su}	Data and CS setup time	0		μs
t_h	Data hold time	1.75		cycle†
t_h	Data hold time, f_{osc} = 640 kHz*	10.9		μs
t_{wH}	Pulse width, PDC high	1		cycle†
t_{wH}	Pulse width, PDC high, f_{osc} = 640 kHz	6.25		μs
t_{wL}	Pulse width, PDC low	1		cycle†
t_{wL}	Pulse width, PDC low, f_{osc} = 640 kHz	6.25		μs

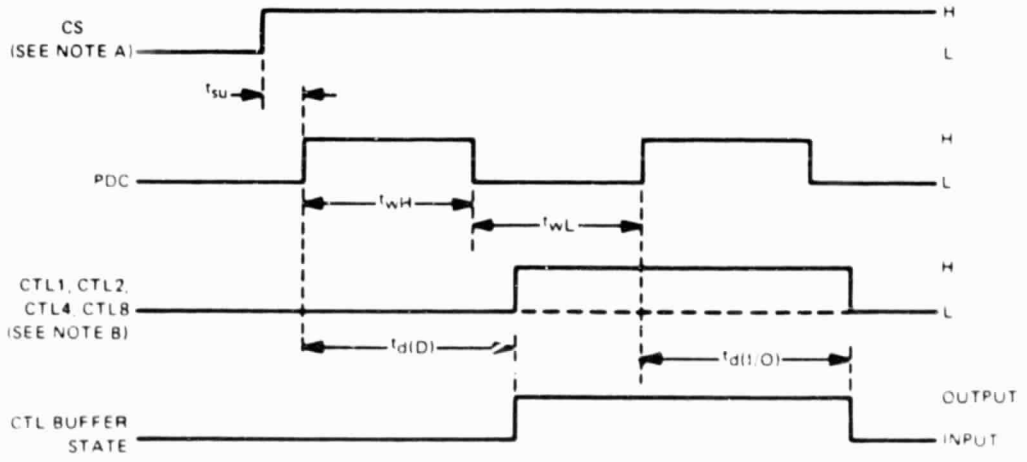
* The system clock is set by using the ROM clock (160 kHz).

4.6 SWITCHING CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE, V_{DD} = −9

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{osc}	Oscillator frequency		608	640	674	kHz
$t_{d(D)}$	Data output time		1.25			cycle†
$t_{d(D)}$	Data output time	f_{osc} = 640 kHz	7.8		8.1	μs
$t_{d(I/O)}$	Output buffer switching time		1.25			cycle†
$t_{d(I/O)}$	Output buffer switching time	f_{osc} = 640 kHz	7.8		8.1	μs

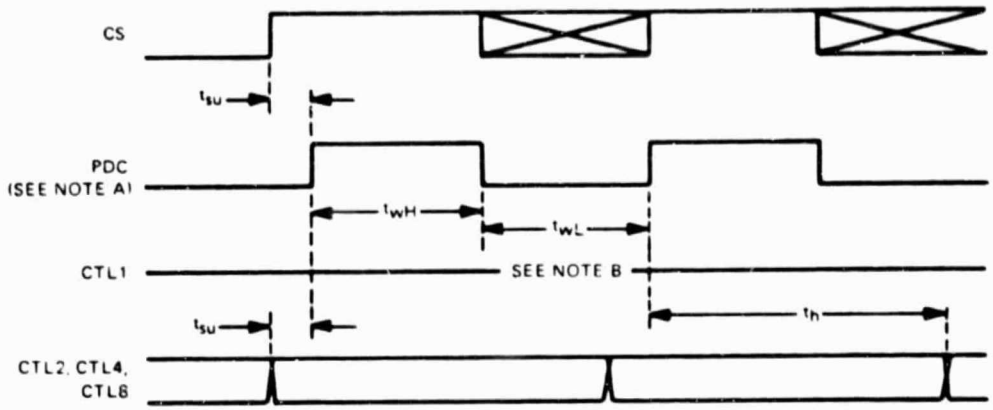
† Typical values are at T_A = 25°C.

† Cycle refers to the equivalent time in CPU clock cycles.



NOTES A. Output buffers are enabled only while CS is high. Turn-on and turn-off delays are equivalent to 0.75 instruction cycle.
B. For TEST TALK, only CTL1 is active.

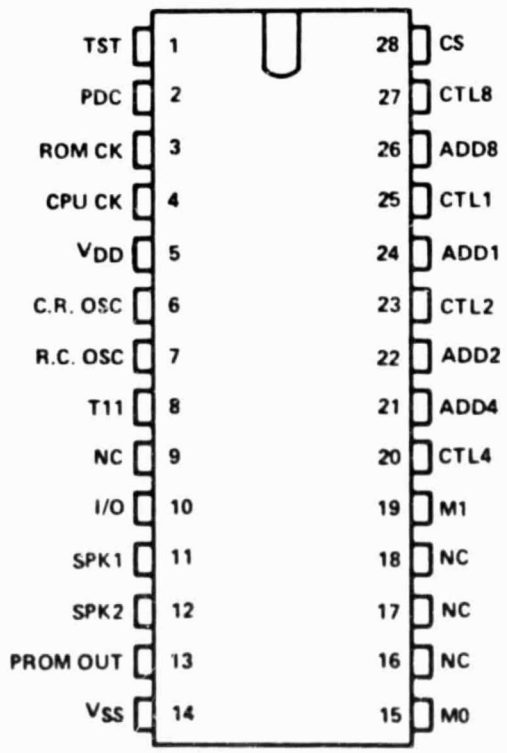
FIGURE 3 – TIMING DIAGRAM, DATA OUTPUT AND I/O MODE SWITCHING



NOTES A. Refer to command descriptions for PDC requirements.
B. CTL1 is irrelevant (don't care) for command transfer, same as CTL2, CTL4, CTL8 for address transfer.

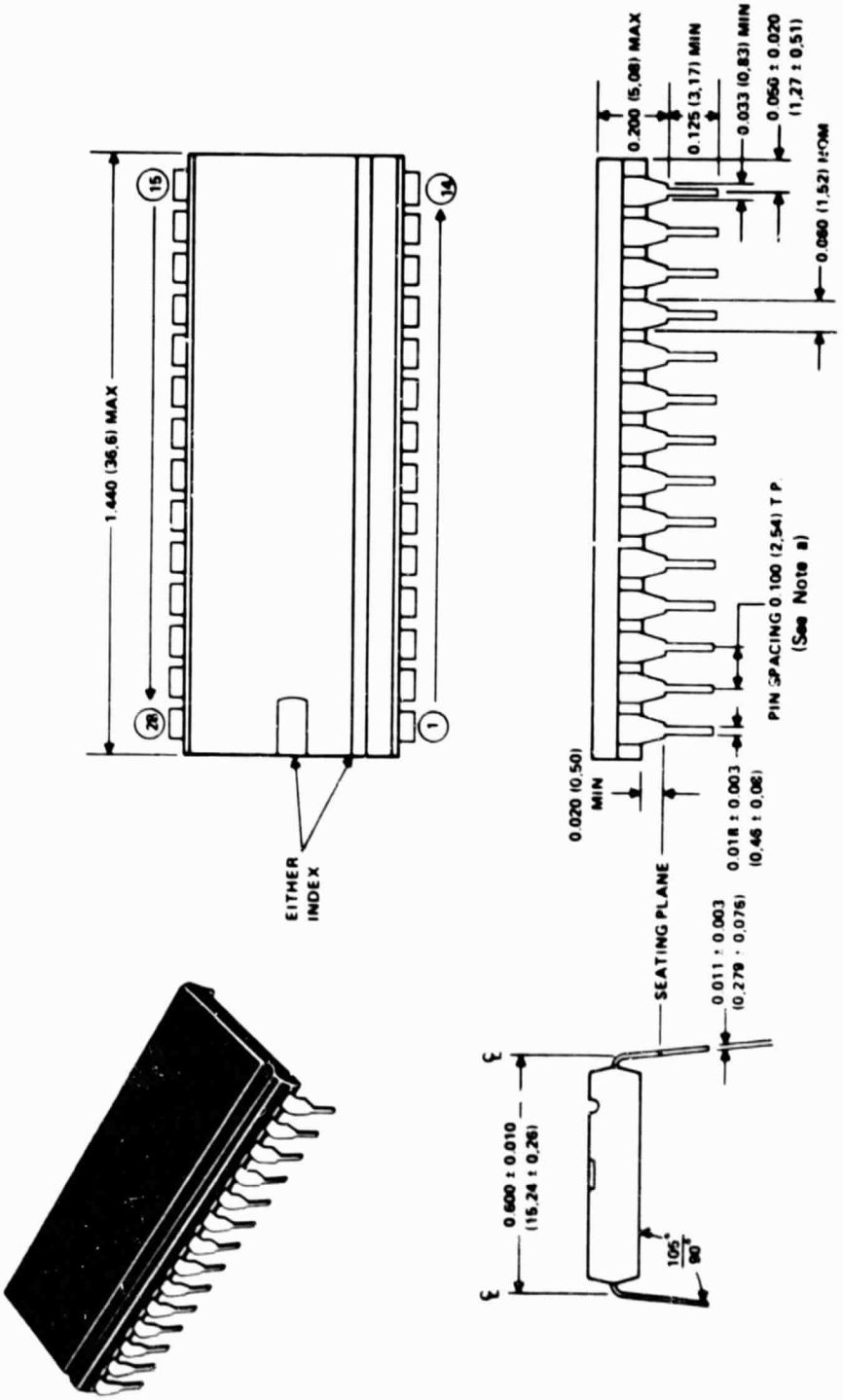
FIGURE 4 – TIMING DIAGRAM, COMMAND AND DATA TRANSFER

5. TERMINAL ASSIGNMENTS



6. MECHANICAL DATA

TMS 5100 28-PIN 600-MIL PLASTIC PACKAGE (100-MIL PIN SPACING)

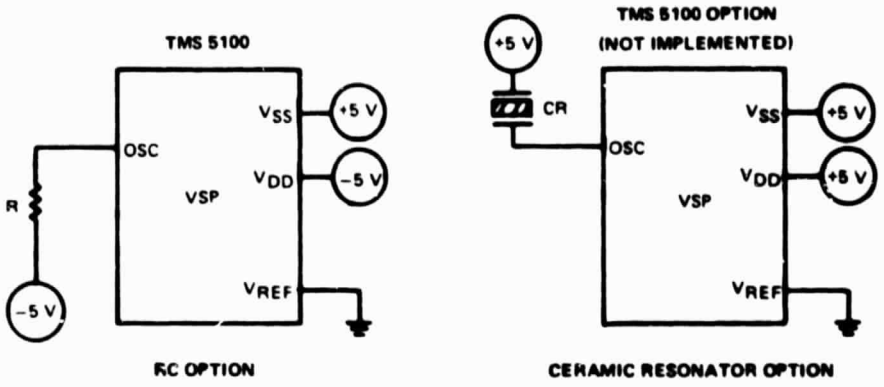


NOTES a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.

b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

APPENDIX

SYSTEM CLOCKS*



*The system clock is set by using the ROM CLK (160 kHz)

FIGURE A-1 – TMS 5100 OSCILLATOR OPTIONS

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMS 6100
VOICE SYNTHESIS
MEMORY
DATA MANUAL

TENTATIVE DATA
JUNE 1980

TEXAS INSTRUMENTS
INCORPORATED

1. INTRODUCTION

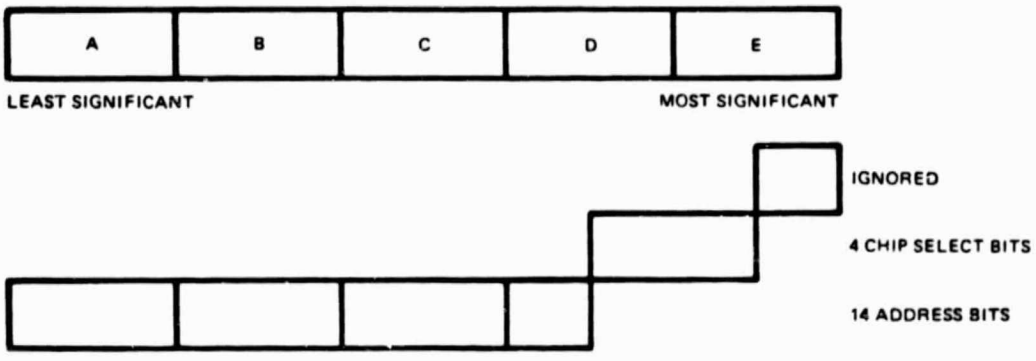
The TMS 6100 is a PMOS 128K ROM internally organized as 16K x 8. Externally it appears as either a one-bit (serial) or four-bit (parallel) output. Once the 14-bit address (of any eight-bit byte) is written into the device, data is read out one bit or one nibble (half byte) at a time by toggling a control pin. After eight bits or two nibbles have been read, the address is internally incremented. This allows quick download of the ROM starting at one address (at f_{clk} = 200 kHz, the ROM can be read completely in 1.3 seconds). The output (one-bit or four-bit) is a mask programmable option as is an internal chip select allowing parallel connection of up to 16 ROMS (256K bytes).

2. THEORY OF OPERATION

Figure 1 shows the block diagram of the TMS 6100. M1 and M0 are control signals (formerly called I0 and I1) and determine the mode of operation of the device. The clock input to the device should be a maximum of 200 kHz.

For proper operation of the TMS 6100, it must be initialized after power is applied. This is accomplished by performing a dummy "load address' and then a dummy "data transfer". The dummy load address is done by pulsing M1 once in accordance with the device's timing constraints. The dummy data (read) transfer is done by pulsing M0 once and then waiting 80 microseconds.

In this state the device is ready to accept its first address. The address is loaded as shown in the timing diagram. Five nibbles (one nibble is four bits) must be loaded into the TMS 6100 constituting one address. Each nibble is first set up on the data pins and then clocked with one pulse of M1. This address can be broken down as follows.



The least significant nibble (LSN),A, is loaded into the ROM first and the most significant nibble (MSN),E, is loaded last. The nibbles A thru C and half of D as shown in the diagram make up fourteen bits of address used internally to address the memory array. These bits define one of 16,384 possible internal addresses. At each address there are eight bits of data. This data is read from the addressed location in either two or eight read cycles. If the one-bit output is selected, each M0 pulse puts a new bit on ADD8; eight pulses per byte. If the four-bit output is selected, each M0 pulse puts four new bits on ADD8 through ADD1, two pulses per byte. The data is read out from LSB to MSB or from LSN to MSN. After a byte has been read, the internal address counter is incremented. (Note that only the least significant bit or nibble can be directly addressed. The rest of the byte must be accessed through pulsing of the M0 pin; however, after one address is loaded data can be dumped sequentially by continued pulsing of M0.)

When the TMS 6100 is used singly, an indirect address technique is available. After a load address sequence is completed both M0 and M1 are pulsed simultaneously. This causes the contents of the addressed byte and the following byte to be loaded into the internal address counter and an access initiated. After a 320-ns wait, a "data transfer" pulse or series of pulses will cause the output of data stored in the indirectly addressed byte. No dummy data transfer is needed.

It should be noted that all wait times specified are proportional to ROM clock period, e.g., a 20 ns wait at 200 kHz is a 100 ns wait at 160 kHz.

The TMS 6100 has an internal chip select as well as an external select. The four address bits constituting the most significant half of D and the least significant half of E in the diagram make up the internal chip select. They can be thought of as an extention of the address resistor. When an address is loaded that is lower than the one that enables the device, the part does not respond to any request for data in the form of reading from the device, but if sufficient reads are performed to increment the address to that value enabling the device, it will respond. Similarly, if an address is loaded that enables the device and sufficient reads are performed incrementing the address beyond that which enables the device, the device will disable itself and not respond to any further reads. It is in this way that the internal chip select acts as a bank decoder, allowing 16 devices (one from each bank) to be bussed together.

The internal chip select can be programmed as one of 16 values. The value for this code appears in the gate placement deck as "BANK". The value specified here is a hexadecimal number between 0 and F. This corresponds to a decimal number between 0 and 15.

The external chip select is active low and may be bused to 16 devices (one from each bank). This is also programmable and can be programmed as a select or programmed open. In the open mode the device is always enabled if the internal chip select is valid regardless of the state of the external select.

An additional feature is the exclusive-OR option. When programmed in the gate placement deck (EXOR = 1), the MSB of the internal chip select is EXOR'ed with the $\overline{CS}$ pin. The result is AND'ed with the internal and external chip selects to select the chip. This allows connection of up to 16 devices without extra select circuitry.

EXCLUSIVE-OR OPTION TRUTH TABLE

$\overline{CS}$	MSB OF INTERNAL SELECT	ACTUAL * CHIP SELECT
L	0	1
L	1	0
H	0	0
H	1	1

Actual Chip Select = $\overline{CS} \oplus$ Internal Chip Select

* Assuming correct lower 3 internal chip select bits

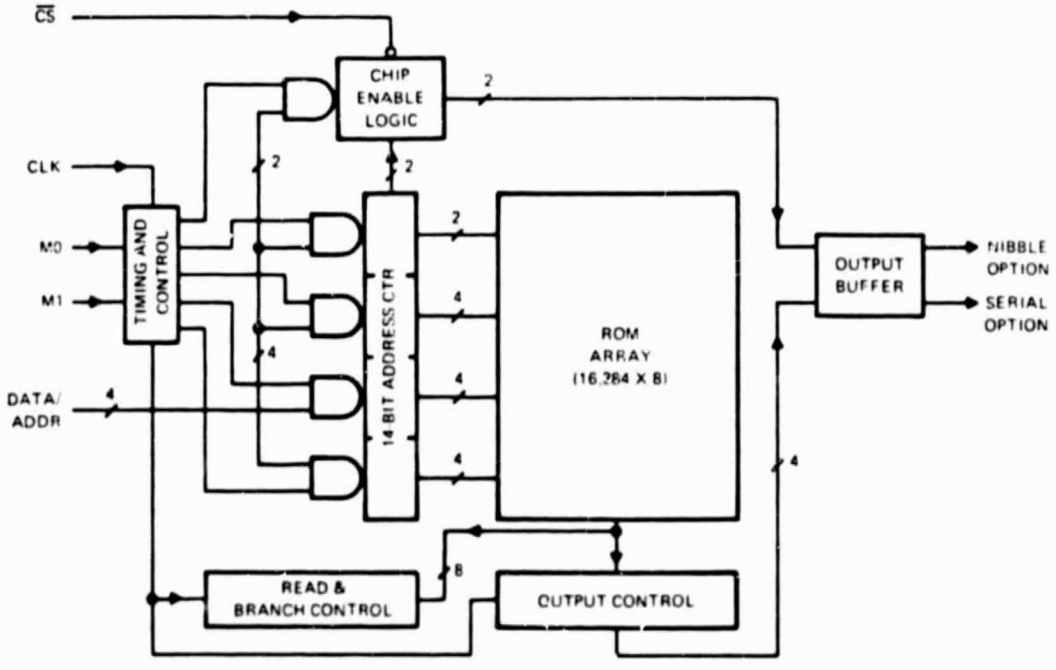
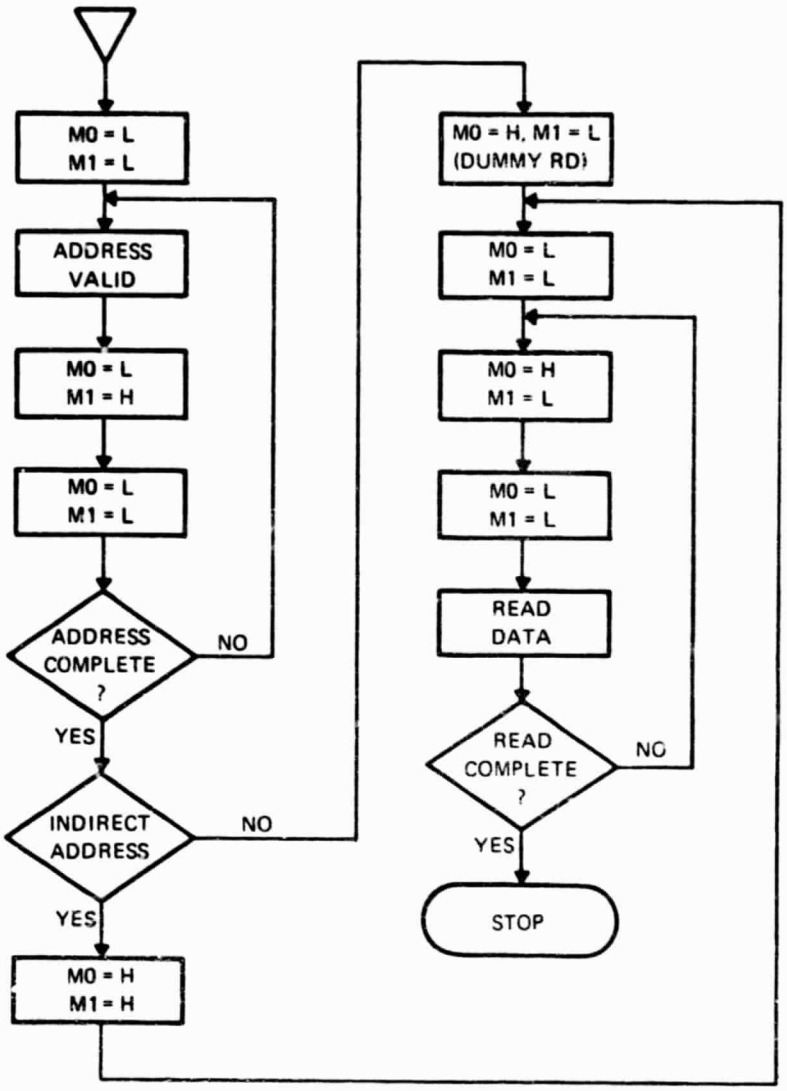


FIGURE 1 – TMS 6100 BLOCK DIAGRAM



H = high, L = low

FIGURE 2 – OPERATION FLOW

3. TMS 6100 ELECTRICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS* (OVER FREE-AIR TEMPERATURE RANGE)

Voltage applied to any device pin (see Note 1) . . . . . −15 V to +0.3 V
Supply voltage range, V_{DD} . . . . . −15 V to +0.3 V
Continuous power dissipation . . . . . 300 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −30°C to 125°C

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM (See Note 2)	MAX	UNIT
V_{DD}	Drain supply voltage	−8.3	−9	9.7	V
V_{SS}	Substrate supply voltage		0		V
V_{IH}	High-level input voltage	−1		V_{SS}	V
V_{IL}	Low-level input voltage	V_{DD}		−4	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. Voltage values are with respect to V_{SS}
2. The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

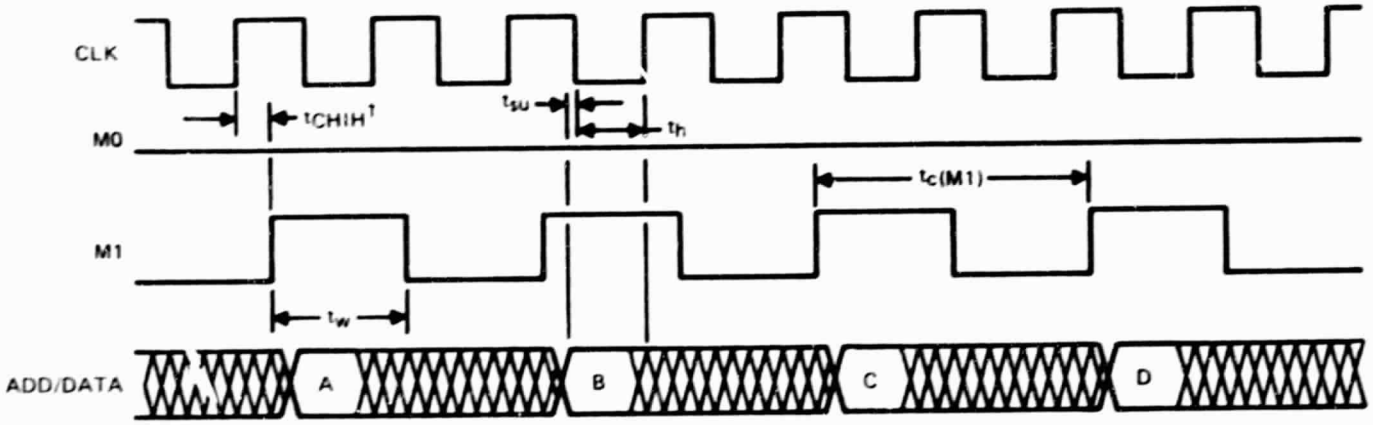
3.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE AND AT −9 V V_{DD} OPERATING VOLTAGE

PARAMETER		TEST CONDITIONS		MIN	MAX (See Note 2)	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 µA	V_{DD} = −9 V	−0.6		V
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			−4.2	V
I_{IH}	High-level input current	V_{IH} = −0.6 V			10	µA
I_{IL}	Low-level input current	V_{IL} = −4.2 V			−10	µA
I_O	Output current	V_I = V_{SS} to V_{DD}			±10	µA
I_{DD}	Drain supply current				10	mA

3.4 TIMING REQUIREMENTS

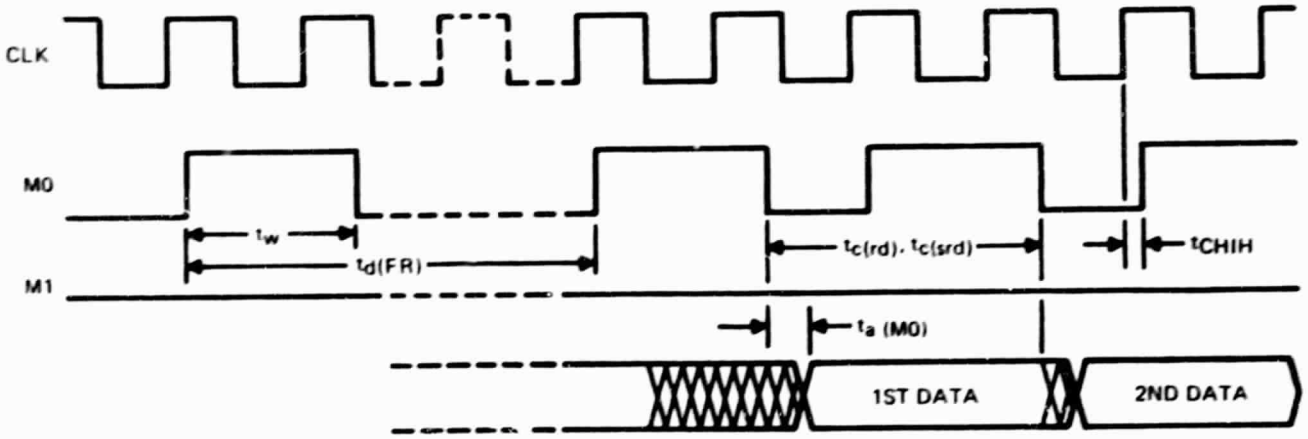
PARAMETER		MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency	100	160	200	kHz
t_{CHIH}	Delay time, clock high to control (I0 or I1) high	0		1	µs
$t_{c(M1)}$	M1 cycle time	10†			µs
t_w	M0, M1 pulse width	5†			µs
t_{su}	Address setup time	2.5†			µs
t_h	Address hold time	5			µs
$t_{d(FR)}$	First read delay	80†			µs
$t_{d(IA)}$	Indirect address delay	320†			µs
$t_{c(rd)}$	Parallel-data read cycle time	40†			µs
$t_{c(srd)}$	Serial-data read cycle time	10†			µs

† These requirements are for f_{clk} = 200 kHz. Times are inversely proportional to f_{clk}.



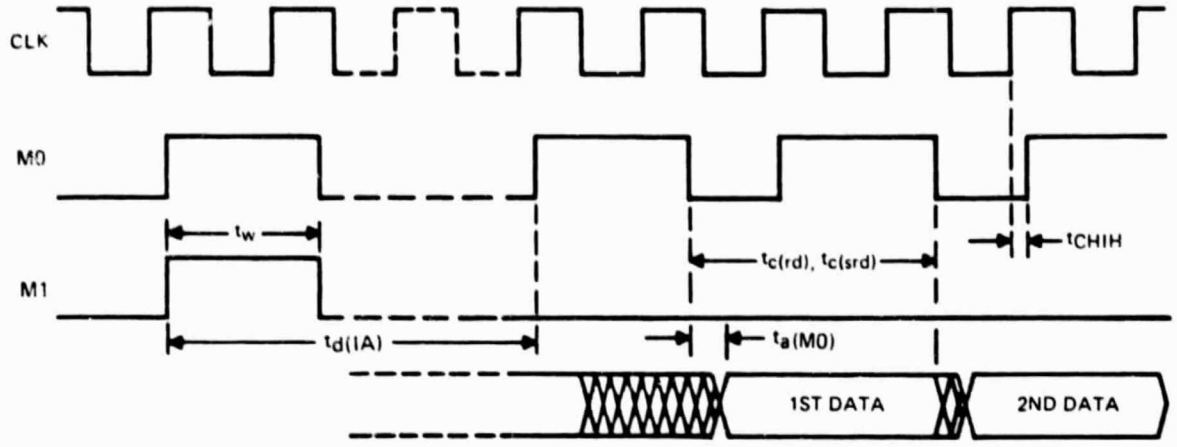
5 NIBBLES OF DATA, A-E, ARE LOADED COMPRISING A 20-BIT ADDRESS

LOAD ADDRESS TIMING



READ DATA TIMING
FIGURE 3

†M0 and M1 pulses should be synchronized with the rising edge of the clock.

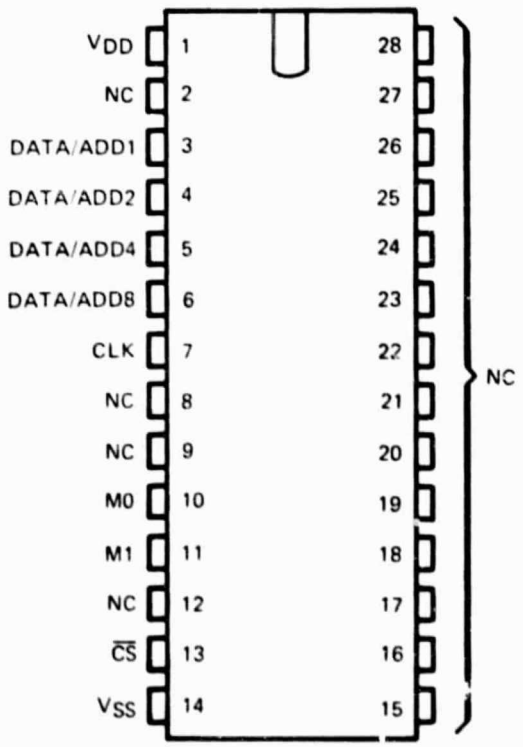


INDIRECT ADDRESS TIMING
FIGURE 4

3.5 SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, V_{DD} = – 9 V

PARAMETER		MIN	MAX	UNIT
$t_{a(M0)}$	Access time from control M0		2	µs

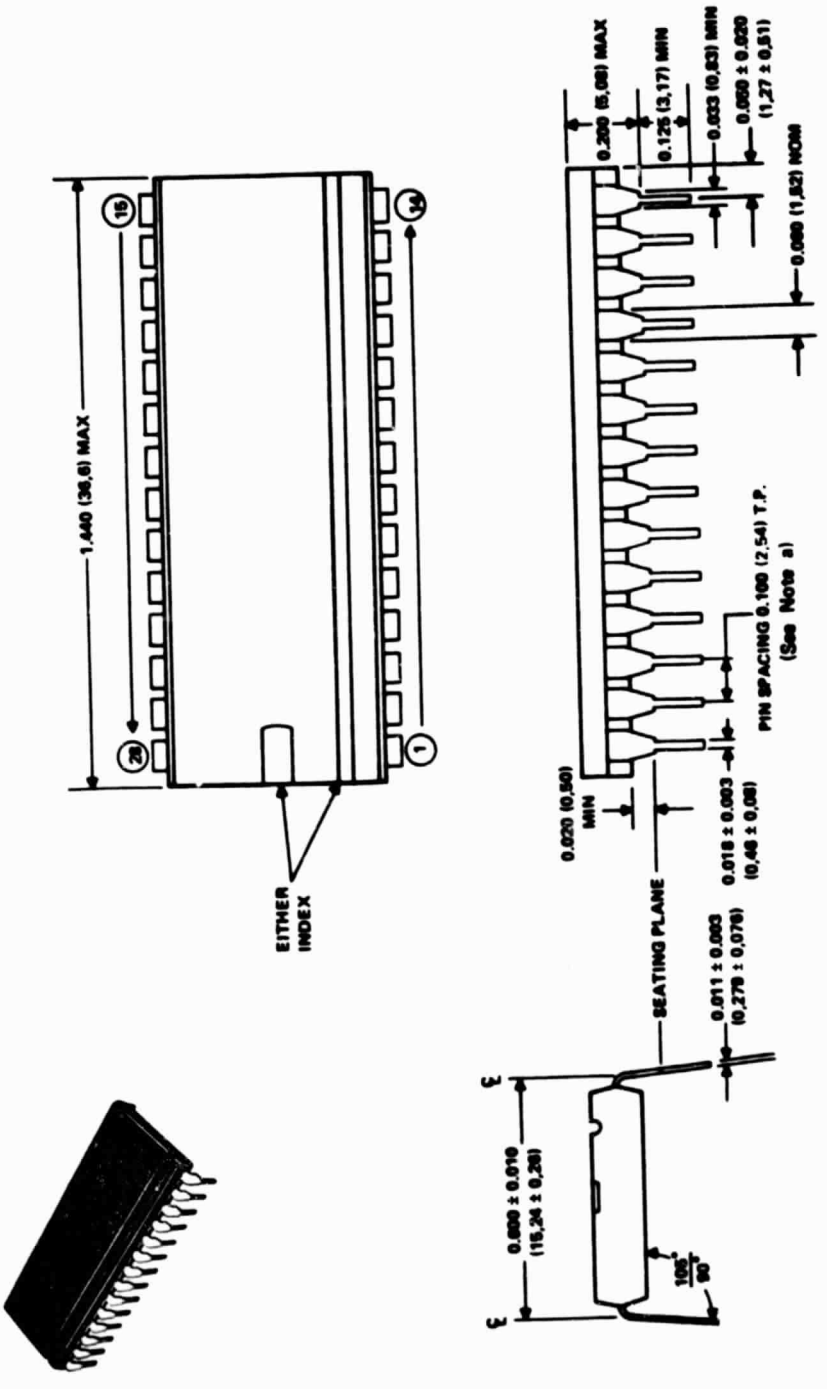
4. TERMINAL ASSIGNMENTS



NC = no internal connection

5. MECHANICAL DATA

TMS 6100 – 28-PIN 600-MIL PLASTIC PACKAGE (100-MIL PIN SPACING)



NOTES: a. Each pin centerline is located within 0.010 inch (0,25 millimeter) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters). Inch dimensions govern.

CL545

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The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

MOS INTEGRATED CIRCUITS FOR VOICE SYNTHESIS

JUNE 1980

TEXAS INSTRUMENTS
INCORPORATED

1. FEATURES

- High quality speech at low data rate.
- Performance and reliability of electronic systems based on integrated circuits.
- Cost effective fabrication process – PMOS.
- Minimum external components.
- Simple external interface.
- Low power consumption: Battery Operated.
- Efficient coding permitting storage of a large number of messages.
- Suitable for synthesis of Speech and Sound effects.

2. SYSTEM DESCRIPTION

The VOICE SYNTHESIS SYSTEM described herein utilizes a method of speech encoding known as pitch excited linear predictive coding (LPC). The speech is synthesized by exciting a time varying digital filter modelling the human vocal tract with a digital representation of glottal air impulses for voiced sounds, or the rush of the air for unvoiced sounds.

A typical three-chip system consisting of the TMS 5100 voice synthesis processor (VS/P), the TMS 6100 ROM voice and the TMS 1000 family controller is shown in Figure 1. The TMS 5100 is designed to synthesize speech from a variable-data-rate bit stream provided by the 128K read-only memory, the TMS 6100. Up to 16 TMS 6100 ROMs may be used in a single system, providing the potential of storing 2 million bits, or 30 minutes of speech, or a vocabulary of over 2500 words. The multifunction controller, a 4 bit microcomputer, spends very little time on speech synthesis itself; this is due to the simplicity of external interface required by the synthesizer. It can, therefore, fullfill easily its primary objective-control of peripherals, such as keyboard, displays, or sensors.

2.1 VOICE SYNTHESIS PROCESSOR

The TMS 5100 chip is designed for a 40-Hz frame rate (the rate at which new speech data-typically 49-bits – obtained from the speech ROM) and a 8-kHz sampling rate, which corresponds to a 4 kHz voice-band. A block diagram of the synthesizer is given in Figure 2.

The ten-stage digital filter shown in simplified form in Figure 3 has the excitation signal applied at the input of stage 10, and produces samples representing synthesized speech at the output of stage 1. The digital filter structure is that of two-multiply lattice filter, performing two's complement arithmetic with 10-bit time varying reflection coefficients and 14-bit intermediate results. The calculations performed in each stage are represented in Figure 4. Recoding pipeline multiplier performs these overlapping multiplies at a rate of one every 6.25 microseconds. For voiced sounds, a 6.25 millisecond long excitation signal is applied to the input at a time interval equal to the pitch period. For unvoiced sounds, the excitation has a constant magnitude and pseudo-random sign.

The 12 synthesis parameters (the reflection coefficients K1-K10, pitch, and energy) are stored in the speech ROM in coded form. Each parameter can assume only a certain number of values from the 2^{10} available. As the number of allowed levels is related to the number of code bits required in the speech ROM, a compromise has been made between speech quality and data storage. The distribution of the number of levels (and, consequently the number of code bits) among the synthesis parameters is given in Table 1.

A full set of parameters for each frame would require a data rate of 1960 bits/second. In three special cases, i.e., slowly varying shape of the vocal tract, generation of unvoiced sounds, and during an inter-word or inter-syllable pause, the data rate can be further reduced. The combined effect of these three special cases reduces the average data rate to only 1100 bits/second.

In most cases it is desirable for speech parameters to vary smoothly from frame to frame, rather than be updated every frame period. To this end, the TMS 5100 contains all necessary logic to do an approximately linear interpolation of all parameters at eight equidistant points within each frame.

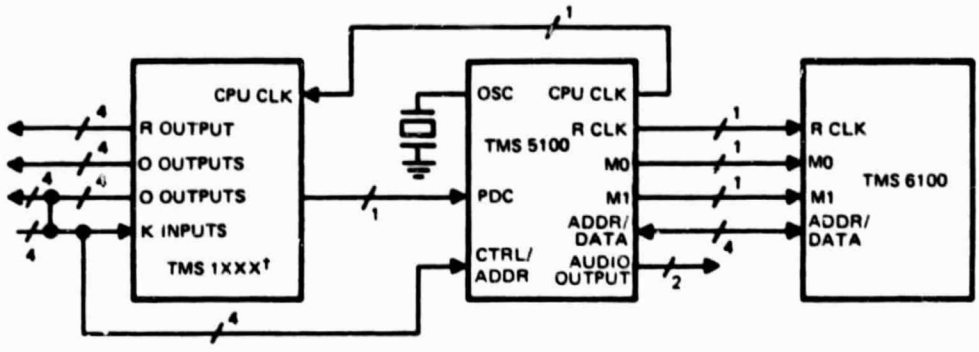
The TMS 5100 contains an 8-bit digital-to-analog converter with one-half LSB accuracy. It also incorporates a 36-milliwatt push-pull speaker driver.

The TMS 5100 has a six line control interface partitioned as follows: four bidirectional lines CTL 1-8 for transfer of commands and ROM addresses to the TMS 5100, or of speech status, or of ROM data to the TMS 5100; one processor data clock line (PDC) to transfer the data on CTL 1-8; and, one chip select (CS) line to enable the foremen-tioned five lines.

2.2 VOICE SYNTHESIS MEMORY

In order to store a relatively large vocabulary in a single-integrated circuit, the speech synthesis system makes use of the TMS 6100 – a 16,384 X 8 mask-programmable read-only memory. The chip features a multiplex addressing scheme with an internal 18 bit-address counter/register. Fourteen bits of the address go directly to the ROM array, while the remaining four MSB's address four programmable gates to select 1 of 16 chips.

There are two control lines M0 and M1, and four data lines ADD 1-8. While ADD 1-8 constitute a four-bit wide input, ADD 8 acts also as the serial-data-output line.



†One of several TMS 1000 Family products may be used and the number of R-output lines depends on the particular product type used.

FIGURE 1 – TYPICAL THREE-CHIP SYNTHESIS SYSTEM

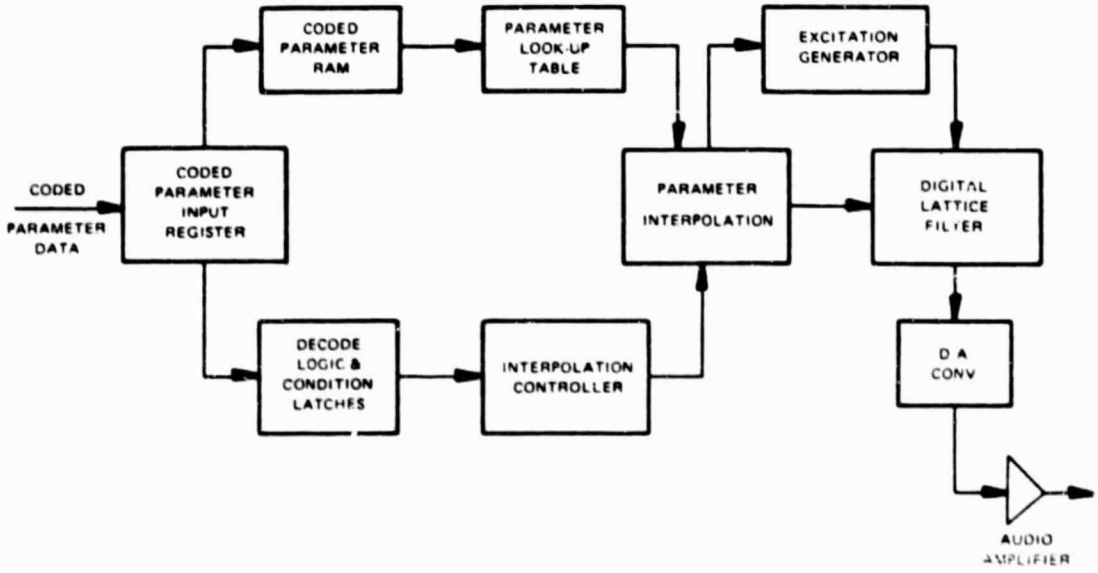


FIGURE 2 – SYNTHESIZER BLOCK DIAGRAM

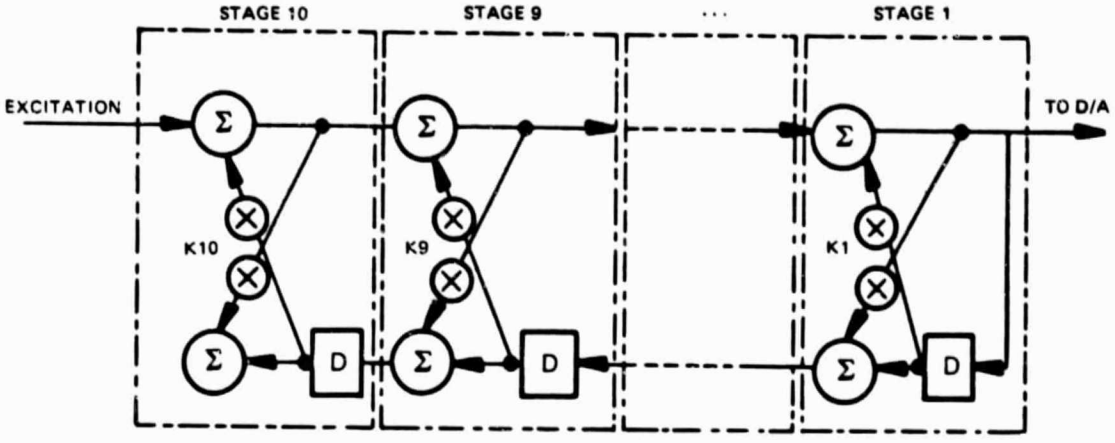
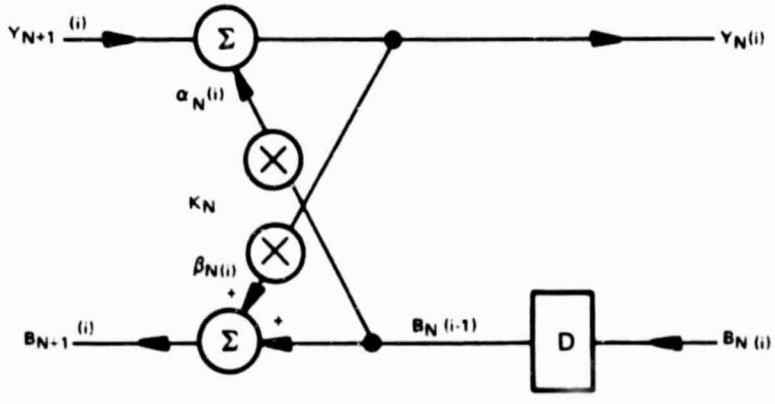


FIGURE 3 – TEN-STAGE DIGITAL LATTIC . FILTER



α_N (i) = K_N·B_N (i-1)

β_{N+1}(i) = K_N Y_N(i)

Y_N(i) = Y_{N+1}(i) - α_N(i)

B_{N+1}(i) = B_N(i-1) + β_N(i)

FIGURE 4 – CALCULATIONS WITHIN A SINGLE STAGE

TMS 5100 PIN DESIGNATIONS

NO.	SIGNATURE	DESCRIPTION
1	TST	Test
2	PDC	Processor-data-clock input
3	ROM CK	ROM-clock output (160 KHz)
4	CPU CK	CRU-clock output (320 KHz)
5	V_{DD}	Drain supply voltage
6	C.R. OSC	Oscillator input
7	R.C. OSC	Oscillator input
8	T11	Test sync
9	NC	No internal connection
10	I/O	Test/digital output
11	SPK1	Speaker drive
12	SPK2	Speaker drive
13	PROM OUT	Test
14	V_{SS}	Substrate supply voltage
15	M0	Command bit to TMS 6100
16	NC	No internal connection
17	NC	No internal connection
18	NC	No internal connection
19	M1	Command bit to TMS 6100
20	CTL4	TMS 1XXX control
21	ADD4	TMS 6100 address
22	ADD2	TMS 6100 address
23	CTL2	TMS 1XXX control
24	ADD1	TMS 6100 address/data in
25	CTL1	TMS 1XXX control
26	ADD8	TMS 6100 address
27	CTL8	TMS 1XXX control
28	CS	TMS 6100 chip select

TABLE 1 – LPC –10 SPEECH SYNTHESIS CODING

PARAMETER NUMBER	PARAMETER	NUMBER OF ALLOWED VALUES	NUMBER OF CODE BITS
1	AMPLITUDE	15	4
2a.	REPEAT BIT	2	1
2b.	PITCH	32	4
3	K1	32	5
4	K2	32	5
5	K3	16	4
6	K4	16	4
7	K5	16	4
8	K6	16	4
9	K7	16	4
10	K8	8	3
11	K9	8	3
12	K10	8	3

3. TMS 5100 SPECIFICATIONS

3.1 TMS 5100 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage range, V_{DD} (see Note 1) . . . . . –20 V to +0.3 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –30°C to 125°C

3.2 TMS 5100 OPERATING CONDITIONS AND CHARACTERISTICS (FOR COMPLETE CONDITIONS AND CHARACTERISTICS, SEE THE DETAIL SPECIFICATION FOR THIS DEVICE)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	–8.3	–9	–9.7	V
Supply current, I_{DD}			45	mA
High-level input voltage	–0.7†		0	V
Low-level input voltage	V_{DD}		–4	V
Voltage applied to any input/output terminal			–24	V
Oscillator frequency (external RC)	608	640	674	kHz

† The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this document for logic voltage levels only.

NOTE 1: All voltage values are with respect to V_{SS}.

4. TMS 6100 SPECIFICATIONS

4.1 TMS 6100 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage range, V_{DD} (see Note 1) . . . . . −20 V to +0.3 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −30°C to 125°C

4.2 TMS 6100 OPERATING CONDITIONS AND CHARACTERISTICS (FOR COMPLETE CONDITIONS AND CHARACTERISTICS, SEE THE DETAIL SPECIFICATION FOR THIS DEVICE)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	−8.3	−9	−9.7	V
Supply current, I_{DD}			10	mA
High-level input voltage*	−1		0	V
Low-level input voltage*	V_{DD}		−4	V
Pulse duration, ROM clock			0.5	µs
Fall time, ROM clock			0.5	µs

* The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this document for logic voltage levels only.

NOTE 1: All voltage values are with respect to V_{SS}.

TMS 6100 PIN DESIGNATIONS

NO.	SIGNATURE	DESCRIPTION
1	V_{DD}	Drain supply voltage
2	NC	No internal connection
3	ADD1	Address input
4	ADD2	Address input
5	ADD4	Address input
6	ADD8	Address input/Data out
7	ROM CK	Clock input
8	NC	No internal connection
9	NC	No internal connection
10	M0	Command bit 0 input
11	M1	Command bit 1 input
12	NC	No internal connection
13	CS	Chip select
14	V_{SS}	Substrate supply voltage
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	NC	No internal connection
22	NC	
23	NC	
24	NC	
25	NC	
26	NC	
27	NC	
28	NC	

Printed in U. S. A.

Speech Synthesis

National Semiconductor
Application Note 252
Jim Smith
Dave Weinrich
December 1980

INTRODUCTION

Electronic speech circuits offer a new dimension of sophistication to many modern machines. As annunciators in trains, elevators, office buildings, autos, airplanes, terminals, toys and games, etc., electronic speech circuits provide a more direct and natural announcement than bells, buzzers or lights. With electronic voice signals, complex directions can be clearly given in any language and with a minimum of effort.

In the past, electronic announcement systems required elaborate tape mechanisms. These systems were expensive and troublesome, so their use was limited to the small number of applications that required speech announcements (e.g., telephone announcement systems). The first all-electronic systems used analog to digital conversion techniques to convert actual voice into digital signals. These digital speech signals were then stored as PCM or delta modulation signals in semiconductor memories. The major problem with this arrangement was the massive memory required for a moderate amount of announcement time. One second of digital speech, in this configuration, required from 16k to 100k bits of memory.

The latest solution to electronic speech is known as speech synthesis. This technique provides a dramatic reduction in the memory required for one second of speech. Memory requirements range from 400 bits to 2000 bits per second depending on the desired speech attributes and overall quality. The synthesizer technique takes advantage of the fact that speech signals are highly redundant and predictable. By coding only the slowly varing coefficients of speech or by dramatic compression of digitized speech, significant bandwidth reductions in the digitized signal can be realized. These techniques, coupled with LSI semiconductor technology, make true voice synthesis practical.

The National Semiconductor speech processor chip (SPC) provides the complete speech synthesis reproduction circuitry needed to generate high quality and natural speech (male, female or a child's voice), electronic tones or music. A complete chip set is called the DIGITALKER™. It consists of the speech processor chip and a speech ROM. The applications for this chip set are endless, but to name a few:

- Voice interactive computer terminals
- Automotive, nautical and aeronautical instrumentation annunciators
- Voice-back units for banking, weather and time announcements, answering machines, etc.
- Elevators, trains, subway systems, etc.
- Consumer appliances, toys and games
- Warning systems for fire and police emergency

All of these applications benefit from the lower overall cost, high reliability, excellent performance and fast control response afforded by the National Semiconductor DIGITALKER™ system. The remainder of this note will be devoted to a description of the MM54104 SPC, the technique used to synthesize speech and finally a review of the major DIGITALKER™ applications.

SPEECH SYNTHESIS

The basic phonological element of speech is the phoneme. The phoneme represents a simple sound that by itself cannot distinguish different words. Phonemes, together with speaker inflection, volume, emphasis, etc. are the fundamental building blocks of speech. The overall quality of any speech synthesizer, therefore, is directly controlled by its ability to faithfully reproduce all of the necessary speech attributes and not just phoneme reproduction.

The common American English language consists of approximately 38 to 40 phonemes — 14-16 vowel sounds and 24 consonant sounds. Each phoneme is generated with either a voiced sound, as in "eye", or an unvoiced sound like the sh in "shy". This difference between a voiced and unvoiced sound is very important because the unvoiced sounds are generally fewer in number and less dependent upon the physiological characteristics of the speaker. A speech synthesizer, it turns out, can exploit this important difference. Finally, normal speech rates are approximately 10 to 15 phonemes per second (including silence intervals). Since 38-40 phonemes can be coded using 6 bits, the normal bit rate for phoneme reproduction is approximately 60 to 90 bits per second. This bit rate, however, contains only phoneme information which is only one of the many important speech attributes.

Since phoneme reproduction is a basic element in any speech synthesizer, an understanding of phoneme construction would be useful. Speech synthesis models use two driving functions, an impulse source for voiced sounds and a noise source (hiss noise) for unvoiced sounds. Each of these driving signals are filtered into specific frequency bands or formants by time-varying filters. The net result, for any particular set of valid filter coefficients, is a formant sound. In the human vocal tract system, the driving function consists of the lungs as the energy source, and the vocal cords for generating a voiced sound. The driving function for an unvoiced sound relies on the noise generated as air rushes through the vocal chambers and not on vocal cord vibrations. The formants are then generated by the resonant chambers of the throat, mouth and nasal cavities. By controlling the physical nature of these chambers with mouth position, tongue position and throat orifice size, a speaker can control the formants to generate a phoneme. It should be noted, however, that formants are identified by distinctive frequency bands. The unvoiced sounds do not generate these distinctive bands and therefore do not necessarily require the "normal" formants for a faithful reproduction. These sounds are characterized by a noise or hiss with very little resonance. This unvoiced resonance is normally identified as a fricative formant (e.g., the "sh" sound) and is characterized by an unusually large content of high frequencies.

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A formant-based speech synthesizer, as described previously, would normally use at least three formant filters for voiced sounds and one formant filter for fricative sounds. An additional resonance, called nasal resonance, may be included but no dynamic formant function is usually associated with the nasal resonator. For the synthesis of a normal English vowel using a male voice, the three basic formants would fall into the approximate frequency bands of 200 Hz to 800 Hz, 900 Hz to 2300 Hz and 2400 Hz to 3000 Hz. The fricative formant is typically a pulse of high frequency noise in the band from approximately 2500 Hz to 8000 Hz, with the higher frequency fricatives like "th" usually much lower in relative amplitude when compared to the "sh" fricative sound.

The basic formant synthesizer requires formant filter coefficient data, amplitude control data and driving function control data. This minimum system could synthesize speech, but would not control inflection or emphasis. Its quality, therefore, can be very disappointing. Normal memory requirements for a minimal system are approximately 400 bits for one second of speech.

A second approach to speech synthesis does not automatically break speech into its minimum phonological elements. Instead, the speech waveform is sampled, digitized and compressed by the elimination of symmetrical redundancy and silent intervals, the use of adaptive delta modulation, and the adjustment of phase information in the digitized speech. In this way, speech elements can be synthesized as phonemes, phoneme groups, words or even whole phrases. Also, the attributes of the original speaker can be maintained if the synthesized elements are not broken down incorrectly (i.e., inflection can modify the sound of a phoneme if it occurs at the end of a word or phrase rather than at the beginning).

In a speech compression system, unvoiced sounds can be standardized. During the compression algorithm, the voiced and unvoiced sounds are separated and the voiced sounds are compressed. Unvoiced sounds, however, are compared to the available sounds and synthesized by substitution. This approach is successful because unvoiced sounds have very few speaker defined characteristics. As a result, a relatively small set of unvoiced sounds can be used repeatedly.

This speech compression technique offers excellent quality at a low data rate. The synthesis of a male voice, using English, will usually require an average of 1000 bits per word. Because this technique can be applied to any voice frequency signal, it is also capable of synthesizing women's and children's voices, music and tones. This flexibility, plus the realistic quality of the synthesized speech, make this technique very attractive.

THE NSC SPEECH PROCESSOR CHIP (SPC)

The National Semiconductor speech synthesis system consists of the SPC device plus the speech memory (ROM) required to assemble a complete DIGITALKER™ kit. To this kit a customer must add a clock input signal or the necessary oscillator components, an audio filter and amplifier and the control circuit function. This would represent the minimum configuration shown in *Figure 1*. The maximum amount of directly addressable speech memory accessible by the SPC is 128k bits, but external page addressing by the control circuit function can increase this ROM field as required

The SPC utilizes the speech compression synthesis technique. As mentioned earlier, this technique reduces the amount of memory needed to store electronic speech by removing the excess or redundant data from the

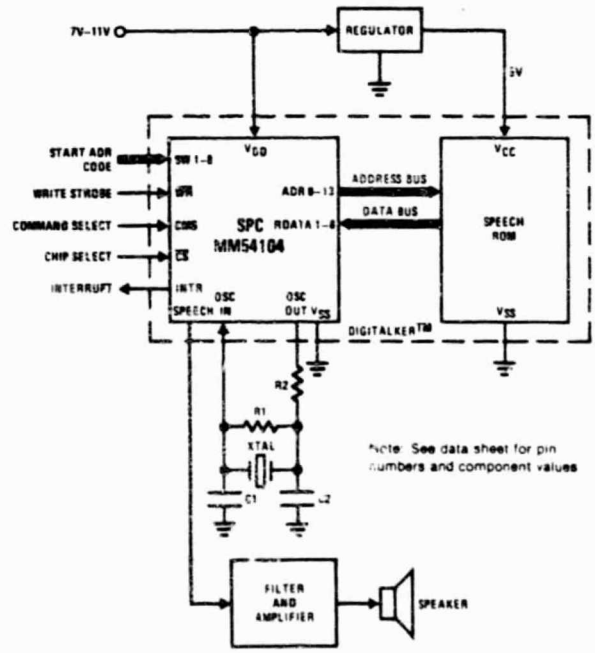


FIGURE 1. DIGITALKER™ Minimum Configuration

speech signal. The four main techniques to perform that task are:

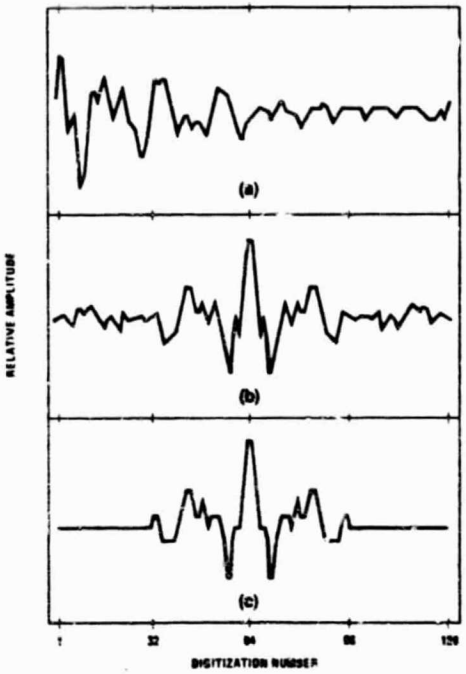
1. Elimination of redundant pitch periods
2. Adaptive delta modulation coding to minimize bandwidth and memory requirements
3. Phase angle adjustments to create mirror image symmetry
4. Replacing the low level portion of a pitch period with silence (half-period zeroing)

National Semiconductor uses an elaborate computer program to analyze a high fidelity tape recording and generate a ROM pattern that will faithfully synthesize the original voice message.

Figure 2 contains a block diagram of the MM54104 SPC. The eight-bit start address bus allows up to 256 separately defined sounds or expressions to be stored in the speech ROM. The control interface to the start address port can take the form of decoding logic, a MICROBUS™ port or mechanical switches.

When the $\overline{WR}$ goes high, the start address code is loaded into the control word address register. The SPC uses this control address to fetch the control word from ROM for the first block of speech data. The control word contains waveform information, repeat information and the address of the speech data. This address is loaded into the phoneme address register and is used to fetch the speech data used to recreate the speech waveform. Before the synthesis takes place, the waveform data must be decoded to provide information such as male or female, voiced or unvoiced, half-period zeroed or not half-period zeroed and silence.

The unsynthesized waveform for a typical voiced pitch period might look like the signal shown in *Figure 3a*. In the process of converting this signal to a synthetic form, several operations are performed. First, the phase delay of the signal can be adjusted to create a symmetrical waveform about the center of the pitch period as shown in *Figure 3b*. The next step will replace the low level beginning and ending quarters of the waveform with silence *(Figure 3c)*. The result is a compression factor of 4 to 1 on the original voice data. Now, delta modulation is applied and the results are shown in *Figure 3c*. Synthesis of the waveform starts with a period of silence (no speech data required), a quarter period of adaptive delta modulation-generated speech followed by the same speech data



(a) Original Speech Waveform
(b) Phase Angle Adjusted to Create Mirror Symmetry
(c) Half-Period Zeroed and Delta Modulated

FIGURE 3. SPC Waveforms (After Mozer [2])

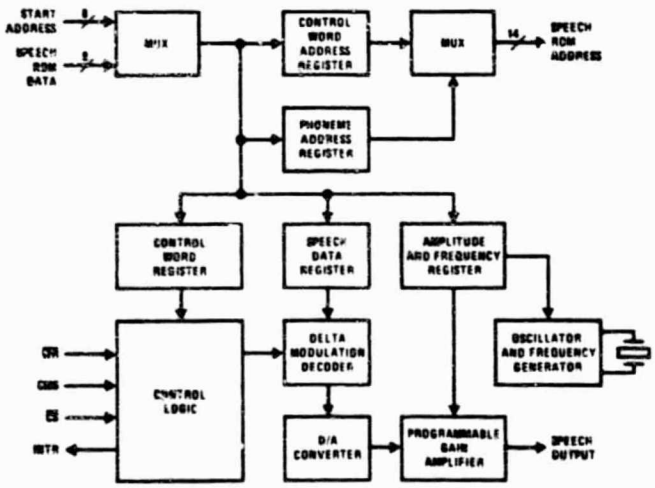


FIGURE 2. MM54104 Block Diagram

MICROBUS™ is a trademark of National Semiconductor Corp.

fetched in reverse. Finally, the SPC will finish the last quarter cycle of the speech block period with silence. This phase modified speech data sounds the same as the original speech.

At the end of a waveform or speech block, the SPC makes a decision about repeating the sequence. Each waveform of a typical voiced signal may be repeated an average of 3 to 4 times. The typical unvoiced waveform may be repeated approximately 7 to 8 times. Once the proper number of repeats has been generated, the SPC will begin a new speech block sequence. This operation continues until the SPC has executed all control words associated with the original eight-bit start address code.

SPC speech signals are stored as adaptive delta modulation data. This encoding technique exploits the relatively predictible and slowly changing characteristic of voiced speech. Because of the small differential between successive speech samples, a delta value rather than an absolute value can be used to determine the actual speech signal. Addition of the delta value to previously accumulated values will result in a new output waveform signal level. An adaptive technique is used so that the delta step size can change in response to slope variations. This technique uses multiple delta modulation step sizes to obtain a more accurate resolution and yet, the required amount of stored data remains lower than the information required for a more conventional encoding scheme.

The internal SPC clock is derived from a programmable frequency generator. Variations in the frequency of this clock, through the control word, allow the SPC to add a rising and falling pitch to speech sounds and syllables. This derived pitch variation adds a natural inflection to the synthetic speech.

Just as pitch variations are used to increase realism, so must the SPC use gain variations. Both techniques are controlled by data stored at the beginning of a speech block and the programmable oscillator and output amplifier circuit blocks of the SPC.

Use of the DIGITALKER™ is quite straightforward and will be outlined in the next section. However, a point on application that must be covered in this note concerns the frequency response of the output speech. The ultimate quality of the DIGITALKER™ will strongly depend upon the filter, amplifier and speaker choices made by the user. For that reason, it is important to understand the output characteristics of the device.

Because the synthesized speech data is derived from a differentiated and sampled input signal, it is necessary to pass the output waveform of the MM54104 through a low-pass filter with a cutoff frequency of approximately 200 Hz and an attenuation characteristic of 20 dB/decade. This compensates for the high frequency pre-emphasis used in the synthesis technique. If the system of interest has a natural rolloff near 200 Hz, this low-pass filter can be eliminated. The important item is that the entire audio system should have a cutoff frequency of approximately 200 Hz. The placement of the cutoff frequency may be adjusted for the particular type of voice being synthesized. A low pitched man's voice might sound better with a 100 Hz cutoff point while women's and children's voices may show improvements with a 300 Hz cutoff. *Figure 4a* shows a filter and amplifier circuit for this minimum frequency response characteristic.

As an example of how the overall frequency response of a particular application can minimize the need for extra filtering, consider the DIGITALKER™ as a voice announcement circuit in a telephone system.

In this case, the telephone network provides a natural attenuation to high frequencies that balances the SPC high frequency pre-emphasis. As a result, the low-pass filter previously mentioned can be eliminated. However, because signal frequencies above 3 kHz must be attenuated before they are allowed to pass into the telephone network, a cutoff filter of 3400 Hz may be required in place of the previously mentioned 200 Hz low-pass filter. A good filter for this application is the National Semiconductor AF133 active filter.

In addition to the 200 Hz to 3400 Hz low-pass filter, an extra stage of filtering can be used for frequencies above 7 kHz. This filter is optional and is normally only used to further reduce sampling noise. Most systems can omit this filter, especially if the overall system bandwidth is not very wide. A second optional filter can be included to limit the overall low frequency response of the system. This high-pass filter would normally cutoff below 200 Hz (adjusted to match the 200 Hz low-pass if provided). This high-pass filter limits low frequency noise, and can usually be omitted if system characteristics do not require this function. A circuit having the full frequency response characteristic is shown in *Figure 4b*. *Figure 5* shows the recommended overall speech synthesis system frequency response.

APPLICATIONS

While the variety of synthetic speech applications are numerous, the actual implementation in any single application is usually limited to one of the following three techniques:

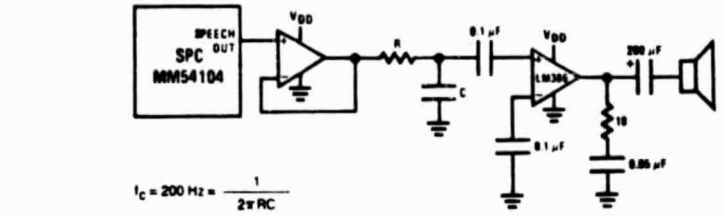
(a) Single channel, hardware control logic
(b) Single channel, software control logic
(c) Multichannel, hardware or software control logic

Each of these circuit approaches for the SPC will be discussed in this section. Particular emphasis will be placed on items (b) and (c), however, because of the broad application possibilities for these two techniques.

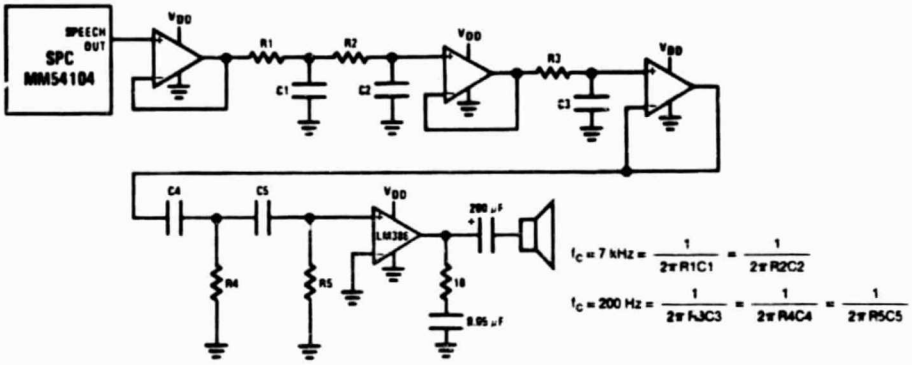
Certain applications require a relatively small number of sentences or announcements with very little similarity between the different sentences. An example of this application might be a talking elevator controller where the messages are brief and non-redundant (e.g., "going up, first floor, second floor", etc.). In this application, certain words are used repeatedly but the number of messages is limited and the length of each message is short. This application and others just like it, do not require the assembly of short phrases into complete sentences, nor do they require a dynamic message structure as would be required with an automatic bank teller (e.g., "your change is ten dollars") where a monetary amount may change from message to message. This fixed message application, therefore, may only require the minimum control circuit as shown in *Figure 6*.

In *Figure 6*, the SPC receives a separate coded input for each complete sentence or message that is synthesized. This input code is received by the SPC through the SW 1-8 port.

The circuit shown in *Figure 6* uses a mechanical switch group to interface the SPC while the *Figure 7* circuit uses a hardware logic controller to input the coded message control data.



(a) Minimum Low-Pass Filter/Amplifier



(b) Maximum Filter Response Configuration

FIGURE 4. SPC Filter and Amplifier

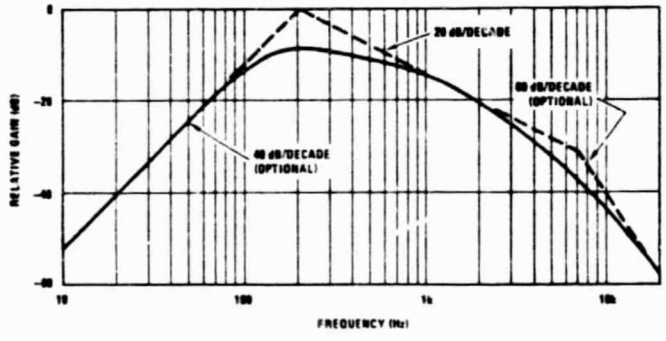


FIGURE 5. Recommended Frequency Response of Entire Audio System for MM54104 SPC

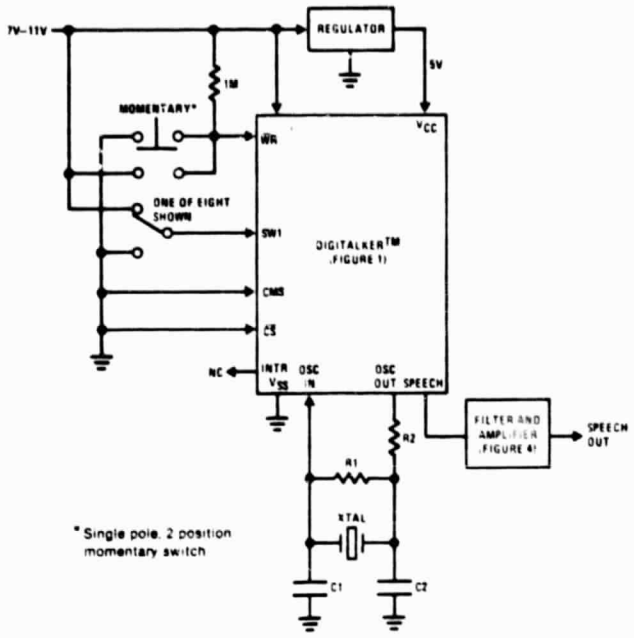


FIGURE 6. DIGITALKER™ with Switch Interface

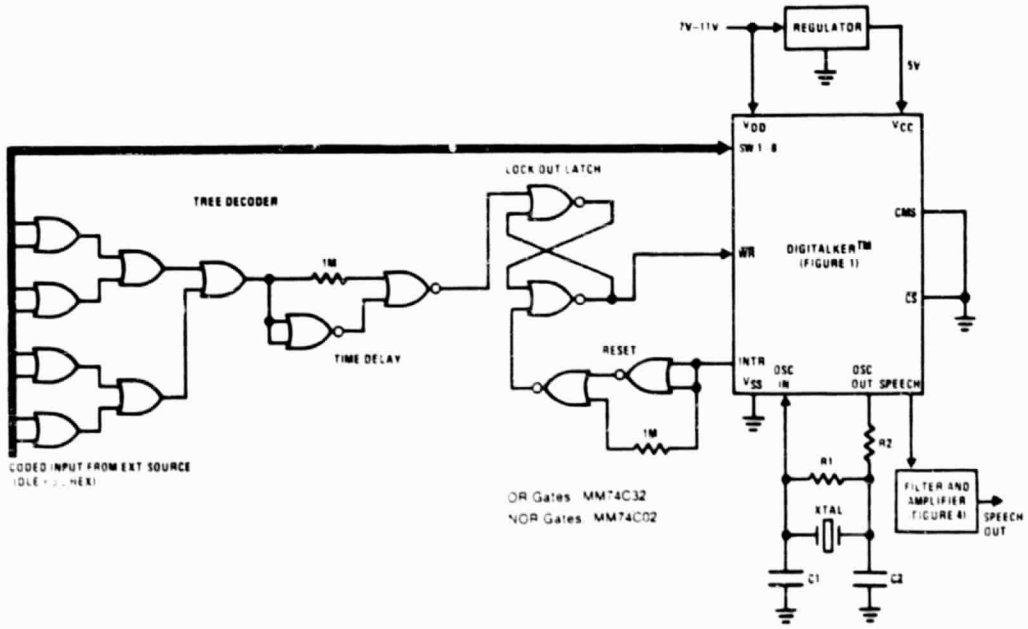


FIGURE 7. DIGITALKER™ with Logic Control Interface

After the proper message address is established on the SW 1-8 port, a momentary pulse must be applied to the $\overline{WR}$ line. If this signal is applied with a momentary action switch, as shown in *Figure 6*, then an external pull-up resistor should be used to pull the $\overline{WR}$ line up to logic high and complete the on-chip switch debounce circuitry. The suggested value of this resistance is one megohm. The $\overline{WR}$ input signal will latch the coded message address into the SPC on the rising edge of $\overline{WR}$ and initiate the synthetic speech message. Since each complete message uses a unique address code of the SW 1-8 port, no further control action is required after this point. The SPC will synthesize the requested message and return to the idle state. If a new input command signal is received, either during or after a message is synthesized, the SPC will immediately abort the current message and begin the new one. The circuit in *Figure 7* shows a lock-out circuit to prevent the aborting of a current message so that messages must be completed before a new message can be initiated.

In *Figure 7*, a message is initiated whenever a valid code word is applied to the eight-bit SW 1-8 port of the SPC. The valid code is detected by the combinational logic decoder and timed to insure all transitions have died. Once the valid code is timed, an S-R latch is set and a $\overline{WR}$ rising edge is generated to start the SPC. This latch circuit also prevents retriggering of the SPC until after the present speech message is completed. Once the synthesized message has ended, the SPC will set the INTR line to the logic one state and a reset pulse will be generated to reset the lock-out latch. A new speech message can now be started by momentarily applying an idle address code followed by a valid code on the SW 1-8 input port.

The SPC will directly address up to 128k bits of speech memory. *Figure 8a* shows a typical speech ROM configuration of 128k using two 64k ROMs. The types of ROMs used have mask programmable chip selects, therefore, no extra decode logic is required for memory requirements of less than 128k. Although this memory size is usually sufficient for most applications, certain systems may require added speech ROM addressing. The circuit in *Figure 8b* shows how the speech ROM of an SPC kit can be expanded in 128k bit pages or modules. Each page is arranged to contain a complete portion of the entire speech library for a particular system. Each single speech data block, as addressed via the start address port of the SPC, must be contained within one ROM page. No page boundaries can be crossed during the synthesis of a speech expression.

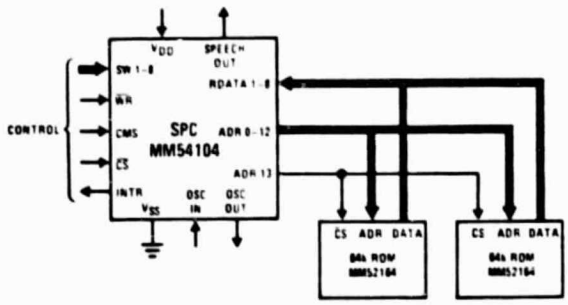


FIGURE 8a. Typical Speech ROM Configuration

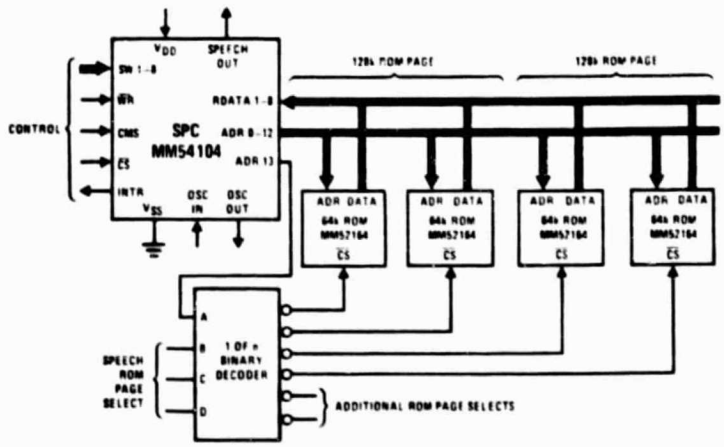


FIGURE 8b. Speech ROM Expansion Configuration

While the simple control schemes discussed so far can be used in many applications, a far more important group of applications will take advantage of the SPC's ability to construct sentences from a group of words, sounds and phrases. This type of application uses an intelligent controller or a microprocessor to string together a group of synthesized phrases to form a complete sentence. The electronic bank teller, previously mentioned, is a good example of this application. The microprocessor controls the stringing of SPC code addresses and applies them, one at a time, to the SW 1-8 port of the SPC. Handshake timing between the microprocessor and the SPC is provided with the INTR line. This microprocessor interface arrangement is known as MICROBUS™ and the configuration is shown in *Figure* 9.

The use of a microprocessor controller expands the versatility of the SPC tremendously. Messages that are composed of numerical responses or fixed phrases in random sequence can be easily constructed from a library speech memory. In addition, various tones or warnings can be synthesized and added before, during, or after an announcement to identify the urgency of each message. For example, an automobile message may state that "oil pressure is low". Alone, that message may only mean that pressure has dropped but no immediate hazard exists. If, however, pressure has dropped below a critical value, the message could be compounded to say "warning, oil pressure is low, pull over and stop the engine". In this latter case, phrases of high urgency are added to the initial message to increase its level of importance. Of course, the second message is not completely separate from the first but is, instead, an expansion of the first. This technique allows fewer input address codes to initiate a larger number of messages without assigning a separate address code for each message and for each of its derivatives. This would be particularly important to an electronic bank teller since a large number of monetary amounts must be synthesized for a relatively small number of finished sentences.

When preparing a speech ROM for an SPC that will synthesize whole sentences from groups of phrases, it is important to note the desired inflections. The SPC has the ability to synthesize all of the important speech attributes including pitch and gain variations, emphasis, inflection, etc. This leads to very high quality life-like synthetic speech if the stringing of phrases does not result in an artificial emphasis or inflection. It is important to choose phrases carefully and to record them with the attribute required for a realistic sentence string. The stringing of phonemes should be avoided whenever possible because the natural inflection is usually lost in such an arrangement.

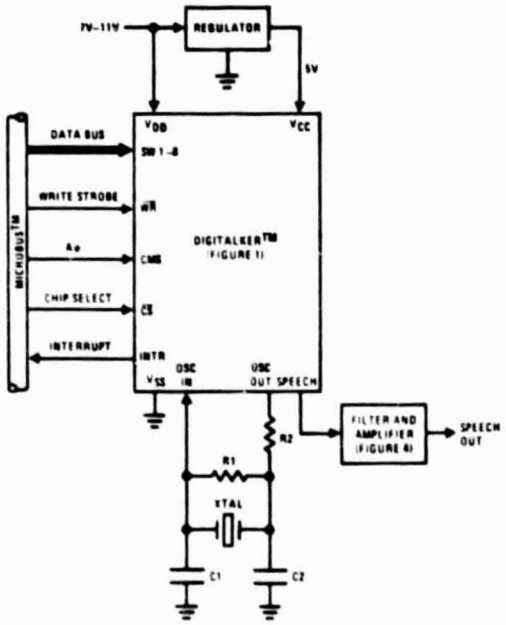


FIGURE 9. DIGITALKER™ with Microprocessor (MICROBUS™) Interface

A low cost intelligent controller for the SPC is one of the COP400 series of microcontrollers. *Figure 10* shows one possible arrangement of an SPC system and a COP420. The COP provides all of the advantages associated with a MICROBUS™ interface at a relatively low cost. Because of its limited I/O structure, the COP's serial I/O port is expanded as required to obtain the desired number of input lines.

The final application technique to be covered is the multichannel configuration. The previous arrangements used an SPC and a dedicated set of speech ROMs to provide a single channel of synthetic speech. Appliances, autos, toys and games, terminals, etc. would probably use a single channel SPC arrangement. But an entirely different group of products could take advantage of a multiple channel approach to reduce the ROM requirements. This group of products includes multiple elevator controllers, electronic bank tellers, multiple pupil learning centers, voice response telephone answering equipment, telephone switching system call announcement centers, etc. In this application, each channel would use a separate SPC and amplifier circuit, but several channels would share a common controller and speech library ROM. A typical configuration is shown in *Figure 11*.

The library ROM of *Figure 11* is shared over eight SPC channels. Each SPC channel is scanned once in 16 μs as

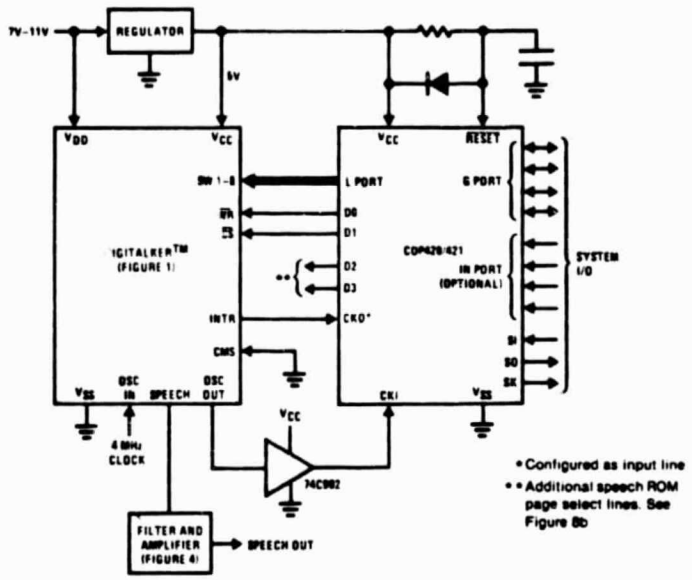


FIGURE 10. DIGITALKER™ with COP420/COP421 Interface

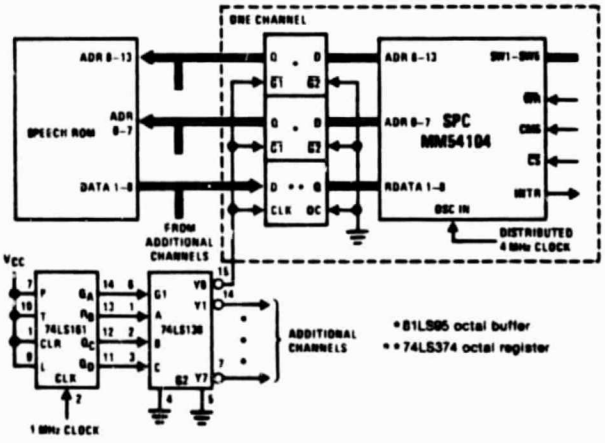


FIGURE 11. Multichannel Speech Synthesizer

shown in *Figure 12*. During each channel period of 2 μs, an SPC output address is presented to the ROM address input port via a pair of octal TRI-STATE* bus drivers. After one μs, the data from the ROM is clocked into the channel's octal data latch, the output of which is connected to the SPC ROM data input port. The remaining 1 μs of each channel cycle is provided for bus settling time.

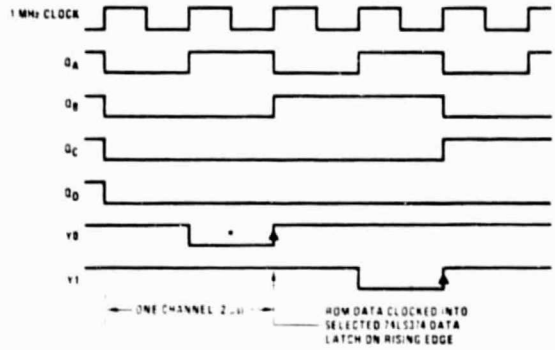
When the speech library ROM is shared over many channels, the actual number of shared channels is controlled by the MM54104 SPC memory cycle timing. Because the channel scanning is asynchronous to the SPC cycle timing, it is necessary for each channel to be scanned at least once during the high interval of the $\overline{\text{ROMEN}}$ signal. As shown in *Figure 13*, this signal is high for at least 20 μs of each memory fetch cycle. Thus, a scanning rate of one channel every 16 μs will insure that each channel is scanned at least once while the $\overline{\text{ROMEN}}$ signal is high.

One final note is necessary about the configuration in *Figure 11*. Simple modifications to the counter and decoder circuitry would allow this circuit to handle sixteen channels. A four-line to sixteen-line decoder would replace the three to eight decoder and the clock would directly enable the decoder during the logic low clock period. All sixteen channels would be scanned every 16 μs and the scan interval for each channel would be one μs — one-half μs of memory access time and one-half μs of bus guard time.

The last multichannel circuit is shown in *Figure 14*. This scheme reduces the number of wires needed between the speech ROM and each SPC channel. By multiplexing address and data over the same parallel bus, fewer wires are needed. This approach is particularly attractive when each SPC channel is located on an individual circuit card. A telephone central office or PABX announcement system is a typical example of a channel per card arrangement. *Figure 14* represents that type of system.

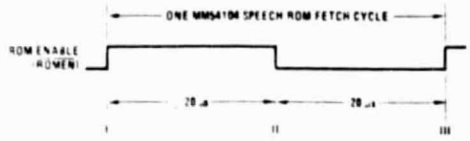
As shown in *Figure 15*, each channel of the unified bus approach is scanned for one μs. As many as sixteen channels, therefore, can be scanned during the $\overline{\text{ROMEN}}$ high cycle of any SPC. During each channel scan, the bus is gated to transmit the ROM address to latches on the ROM circuit board. The address is sent in two bytes. After a brief delay of one-half μs, the bus is gated to return the requested ROM data to the same SPC channel. This data is then latched on the SPC channel card. This scheme is very straightforward. It exchanges reduced interconnect wiring for additional logic circuits.

To minimize interconnect wiring when using a unified bus structure, the SPC control logic would probably be configured on a per channel basis. The COP microcontroller,



*Note: Selected 81LS95 output enabled during this interval. Output is current ROM address code from SPC.

FIGURE 12. Multichannel Timing Diagram



I SPC about to output the next ROM address. Address will remain valid for remainder of the cycle.

II Valid ROM data must be available to SPC shortly after this point.

III Cycle ends, new cycle begins immediately.

FIGURE 13. MM54104 SPC Speech Memory Cycle Timing

TRI-STATE® is a registered trademark of National Semiconductor Corp.

once again, is a logical choice for this function. The COP controller initiates and assembles a group of fixed messages. Because of general similarities between the various messages, phrase strings are used to construct each finished message. Also, the circuit in *Figure 14* allows one message to contain a non-fixed message—a telephone number. The COP controller reads a group of program switches or receives a down-loaded number from the switching system's central processor. It then inserts this number into the appropriate place during the synthesis of the following typical message—"The number you are calling has been changed. The new number is 555-3434". The ROM library in this case contains the phrases required for message construction and the data needed to synthesize the name of each decimal digit. The library could also contain the names of the teen digit pairs, and the words "hundred" and "thousand". These would be used to synthesize the words "thirteen hundred" or "two thousand", etc.

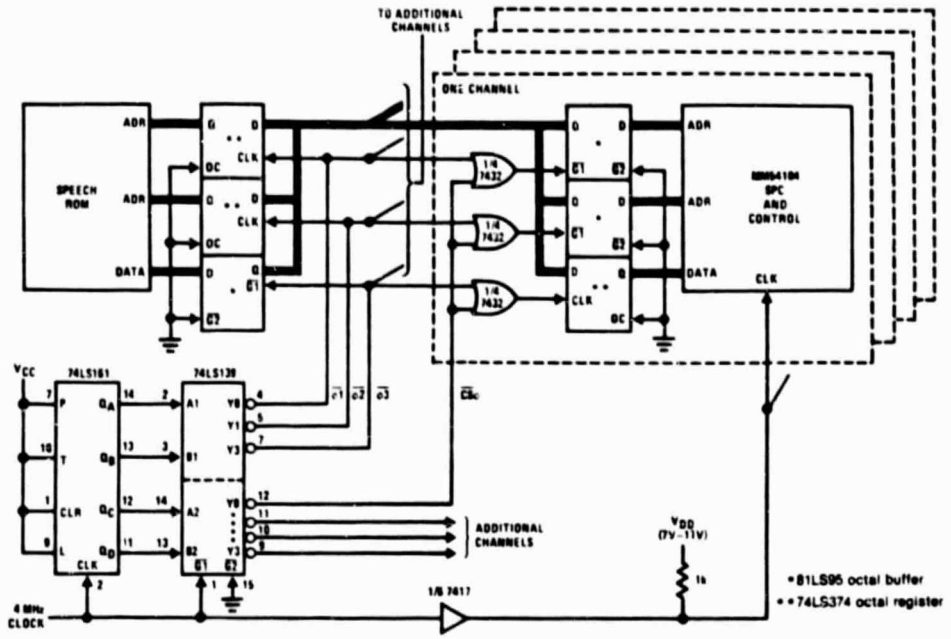


FIGURE 14. Multichannel Synthesizer with Unified Bus

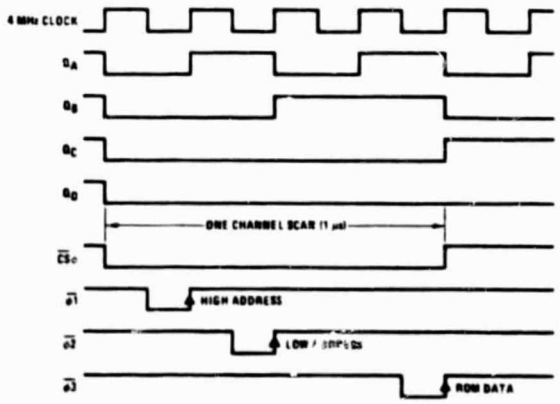


FIGURE 15. Multichannel (Unified Bus) Timing Diagram

SUMMARY

This application note describes some of the versatility and flexibility of the National Semiconductor DIGITALKER™ System. This system provides low cost speech and tone synthesis for products ranging from consumer items to computers. It provides a reliable alternative to mechanical systems (i.e., tape decks) without sacrificing voice quality. Also described in this note are a few of the most popular circuit arrangements possible with the DIGITALKER™. Of particular interest are the methods outlined to assemble whole messages from phrase groups and the schemes used for multichannel synthesizer systems. This latter application is particularly interesting because of the memory savings for the multichannel user.

REFERENCES

1. Morris, Dennis E. and Weinrich, David W., *A New Speech Synthesis Chip Set*, IEEE International Conference on Acoustics, Speech and Signal Processing, 1980.
2. Mozer, Forrest, *Method and Apparatus for Speech Synthesizing*, Pending US Patent.
3. Weinrich, David W., *A Speech Synthesis Chip Set Using Compression Techniques*, Electronics, April 10, 1980.

National Semiconductor

December 1980

MM54104 DIGITALKER™ Speech Synthesis System

General Description

The DIGITALKER is a speech synthesis system consisting of multiple N-channel MOS integrated circuits. It contains an MM54104 speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed. This can be expanded with minimal external logic.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

Encoding (digitizing) of custom word or phrase lists must be done by National Semiconductor. Customers submit to the factory high quality recorded magnetic reel to reel tapes containing the words or phrases to be encoded. National Semiconductor will sell kits consisting of the SPC and ROM(s) containing the digitized word or phrases.

Features

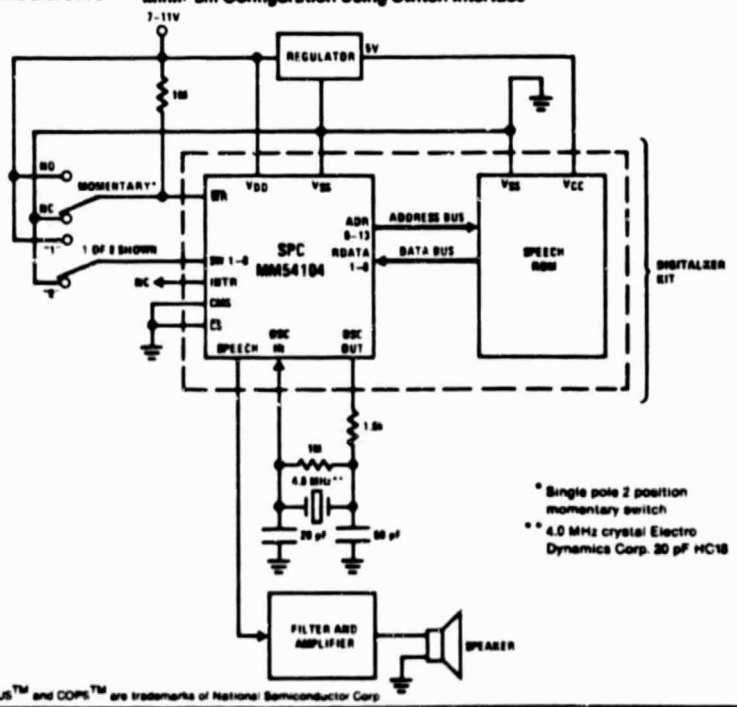
- Designed to be easily interfaced to most popular microprocessors
- 256 possible addressable expressions
- Male, female, and children's voices
- Any language
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- MICROBUS™ and COPS™ compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Easily expandable to greater than 128k ROM
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Ability to store silence durations for timing sequences

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



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Ref-FL30M120/Printed in U.S.A.

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C	Voltage at Any Pin	12V
Operating Temperature Range	−40°C to 85°C	Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
V_{DD}-V_{SS}	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics T_A = 0°C to 70°C, V_{DD} = 7V-11V, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IL}	Input Low Voltage	T_A = −40°C to 85°C	−0.3		0.6	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IH}	Input High Voltage	T_A = −40°C to 85°C	2.2		V_{DD}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −100 μA	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
V_{OLX}	Clock Output Low Voltage	Typical Crystal Configuration and 10M Load on Pin 2			1.2	V
V_{OHX}	Clock Output High Voltage	Typical Crystal Configuration and 10M Load on Pin 2	5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{DD}	Power Supply Current	T_A = −40°C to 85°C			50	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			0.45 V_{DD}		V
V_{OUT}	Peak to Peak Speech Output	V_{DD} = 11V		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

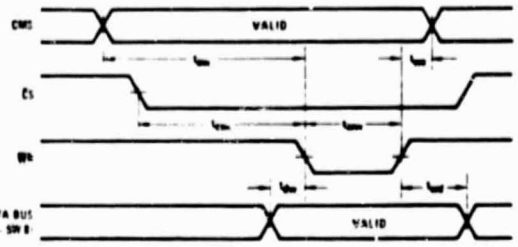
AC Electrical Characteristics T_A = 0°C to 70°C, V_{DD} = 7V-11V, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{sw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{ws}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{rod}	$\overline{\text{ROMEN}}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

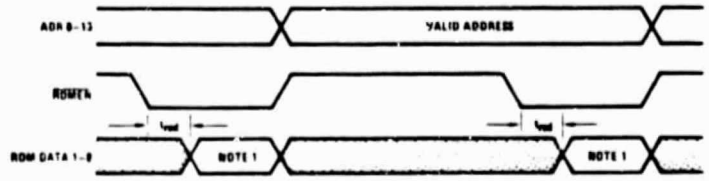
Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.

Timing Waveforms

Command Sequence



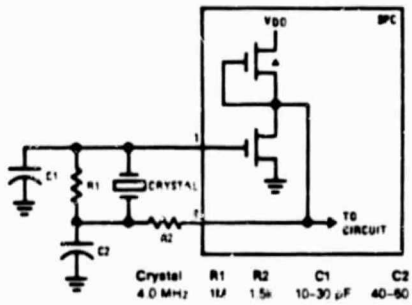
ROM Data Timing



Note 1: ROM data 1–8 can go valid any time after ADR 0–13 changes, however it must be valid within the t_{rad} specifications and remain valid until $\overline{ROMEN}$ goes high

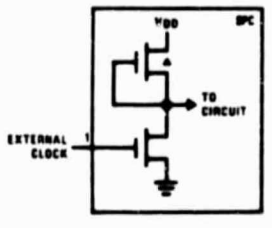
Crystal Circuit Information

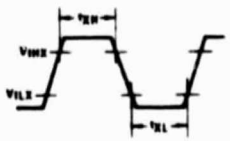
Typical Crystal Oscillator Network



Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10–30 pF	40–60 pF

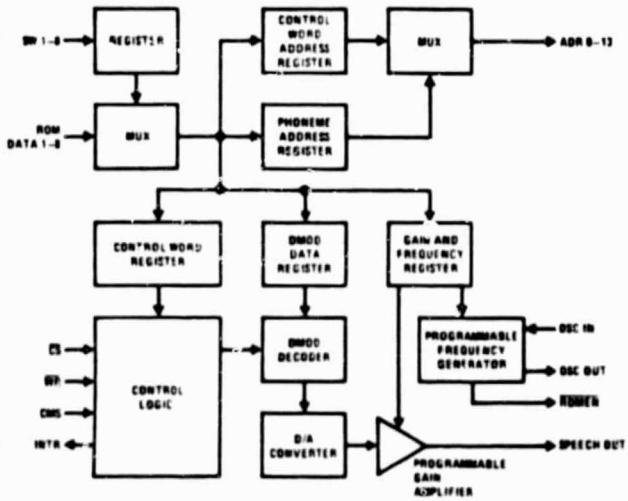
External Clock Input (4.0 MHz)



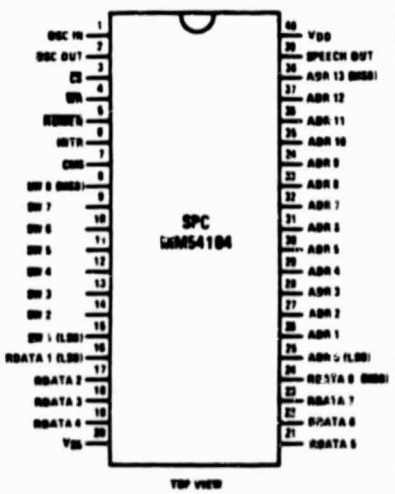


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

Block and Connection Diagrams

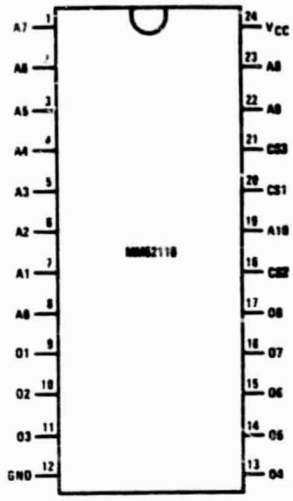


Dual-In-Line Package



Connection Diagrams (Continued) (V_{CC} = 4.75V–5.25V)

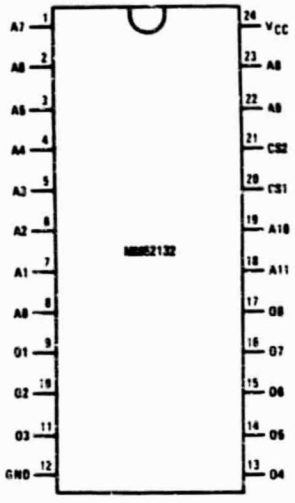
Dual-In-Line Package



TOP VIEW

16k

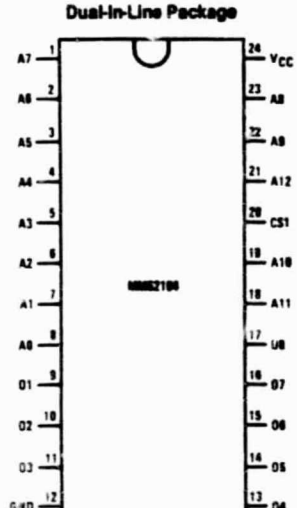
Dual-In-Line Package



TOP VIEW

32k

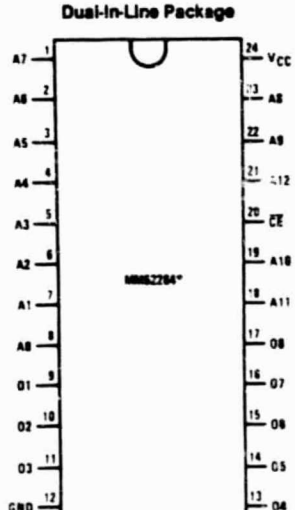
Dual-In-Line Package



TOP VIEW

64k

Dual-In-Line Package



TOP VIEW

* Future product

For specific ROM device information, see MM52116, MM52132, MM52164 or MM52264 data sheets.

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1-8): This is an 8-bit parallel data bus which contains the starting address of the speech data. Unused inputs must be tied to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW1-SW8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch is must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1-8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0-ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

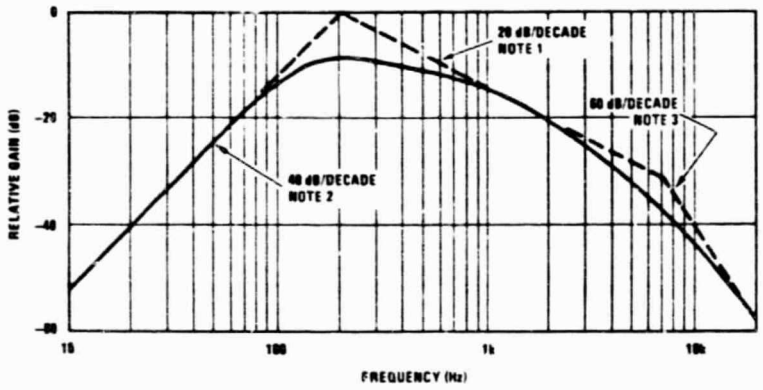
Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

Applications Information

Frequency Response of Combined Amplifier and Speaker



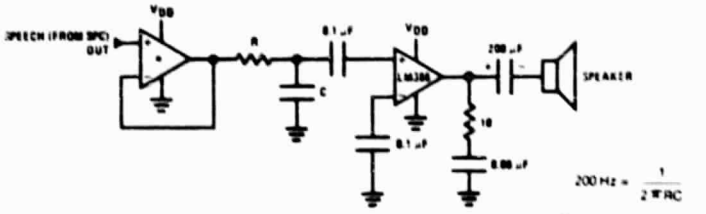
Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz-8000 Hz.

Typical Applications (Continued)

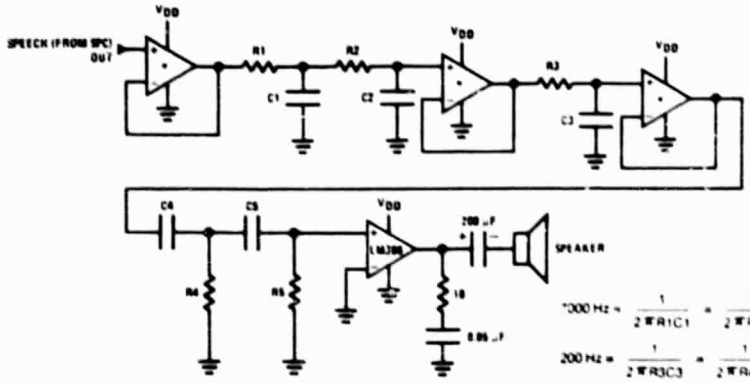
Minimum Filter Circuit



$$200\ Hz = \frac{1}{2\pi RC}$$

* LM348 or equivalent

Filter Circuit to Produce Maximum Frequency Response

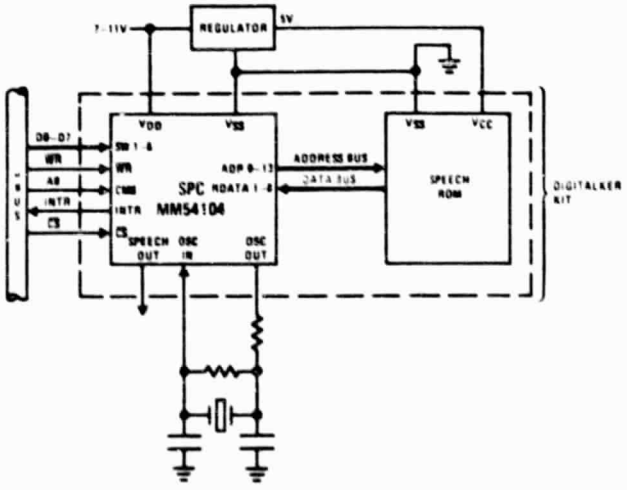


$$2000\ Hz = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

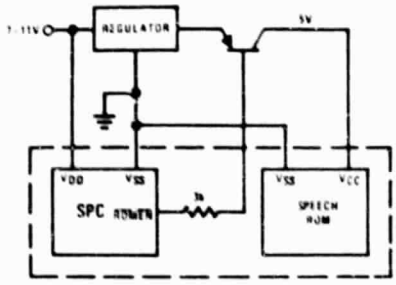
$$200\ Hz = \frac{1}{2\pi R3C3} = \frac{1}{2\pi R4C4} = \frac{1}{2\pi R5C5}$$

* LM348 or equivalent

DIGITALKER™ System Utilizing MICROBUS™ Interface

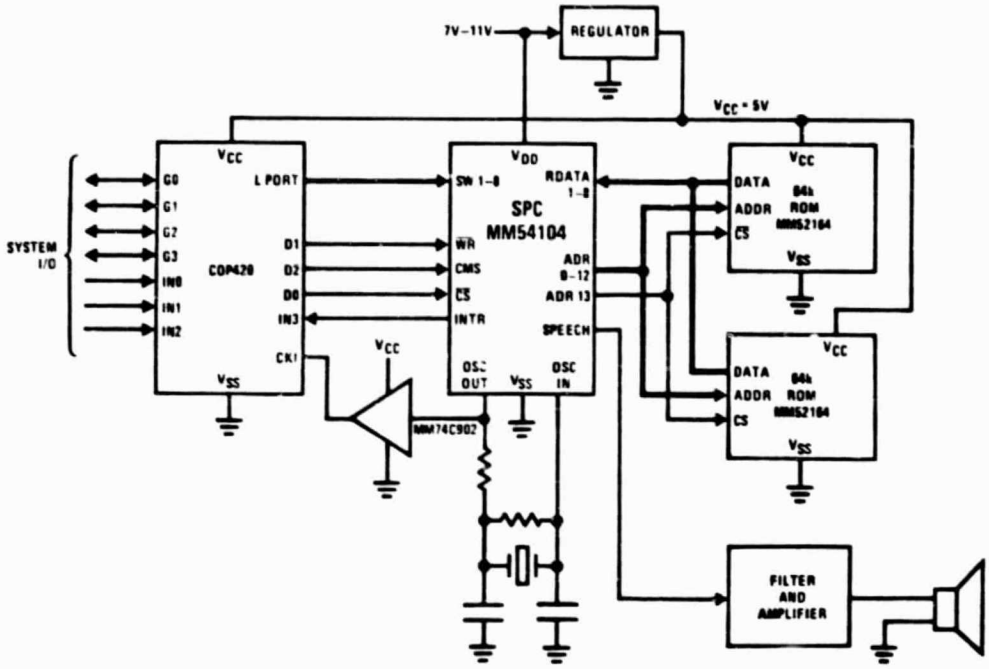


Low Power Configuration Using Static ROM

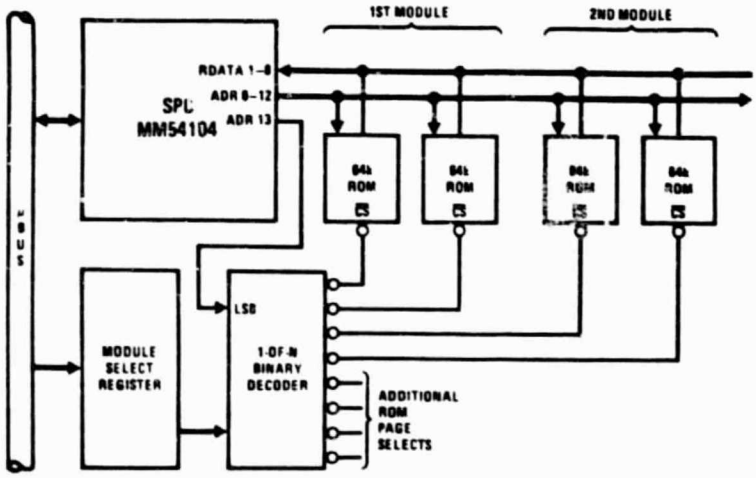


Typical Applications (Continued)

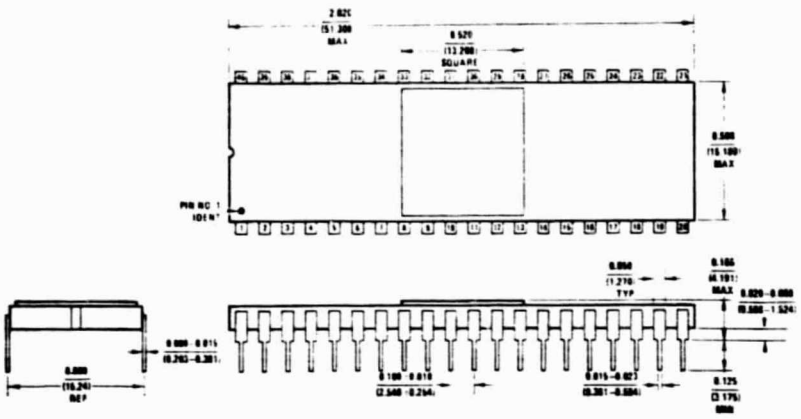
DIGITALKER™ System Using COP420 Interface



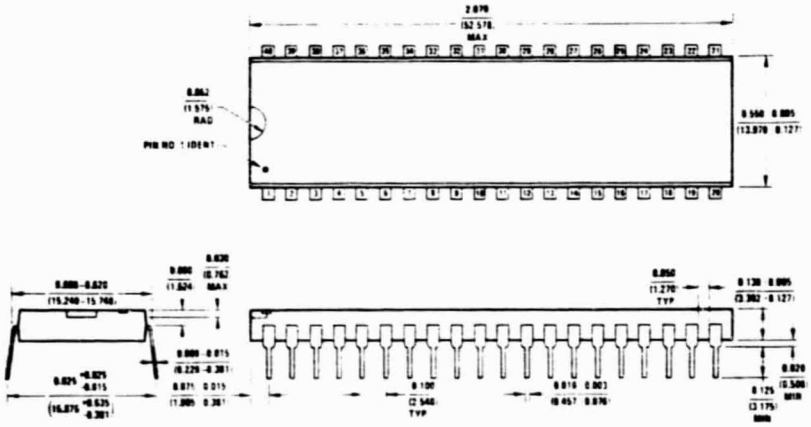
Speech ROM Expansion for Requirements Greater Than 128k Bits



Physical Dimensions inches (millimeters)



Cavity Dual-In-Line Package (D)
NS Package Number D40C



Molded Dual-In-Line Package (N)
NS Package Number N40A

National Semiconductor Corporation
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Santa Clara, California 95051
Tel: (408)737-5000
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National Semiconductor

December 1980

DT1050 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1050 is a standard DIGITALKER kit encoded with 137 separate and useful words, 2 tones, and 5 different silence durations. (See the Master Word List Table I). The words and tones have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1050 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

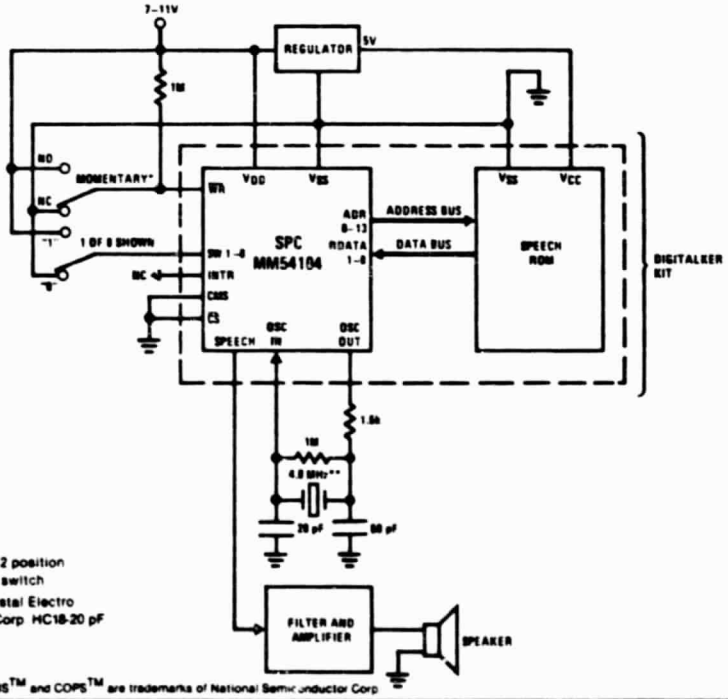
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- 144 addressable expressions, including numbers
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp HC18-20 pF

Absolute Maximum Ratings*

Storage Temperature Range	−65°C to +150°C	Voltage at Any Pin	12V
Operating Temperature Range	0°C to 70°C	Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
V_{DD}-V_{SS}	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics* T_A = 0°C to 70°C, V_{DD} = 7V-11V, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −100 μA	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			0.45 V_{DD}		V
V_{OUT}	Peak to Peak Speech Output	V_{DD} = 11V		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

AC Electrical Characteristics* T_A = 0°C to 70°C, V_{DD} = 7V-11V, V_{SS} = 0V, unless otherwise specified.

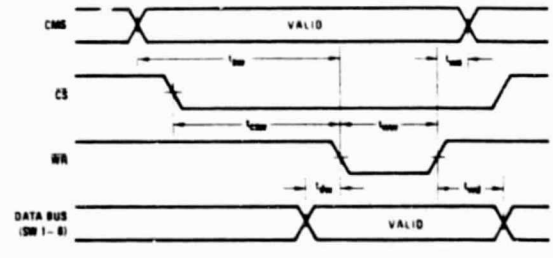
Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{rod}	$\overline{\text{ROMEN}}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_I	External Clock Frequency	3.92	4.08	MHz

Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.

*SPC characteristics only. ROM characteristics covered by separate data sheet for MM52164.

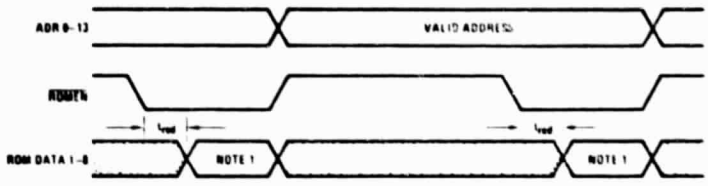
Timing Waveforms

Command Sequence



Timing Waveforms (Continued)

ROM Data Timing



Note 1: ROM Data 1-8 can go valid any time after ADR 0-13 changes, however it must be valid within the t_{red} spec and remain valid until $\overline{ROMEN}$ goes high.

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1–8): This is an 8-bit parallel data bus which contains the starting address of the speech data.

Data bus inputs SW 1–SW 8 accept an 8-bit binary address which is the address of the word which is to be "spoken" from the DIGITALKER output. See the Master Word List (Table I) for the complete listing of words and their respective addresses. If the entire word list is not used, unused inputs must be connected to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW 1–SW 8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch, it must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1–8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0–ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

PHRASE QUALITY

In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. Since several durations of silence are provided in the Master Word List, the actual quality of any phrase can be significantly improved by adding durations of silence (also assigned addresses) between the words. As one thinks about how the phrase is actually spoken, one might assume the approximate duration of silence between each word, and insert the closest duration of silence from the word list. A hint in this area would be that for words beginning with the letters, K, T, P, B, D, and G insert 80 milliseconds silence prior to the words, and for words ending in the same letters as above, 40 milliseconds silence following the word is recommended.

Functional Description (Continued)

TABLE I. DT1050 MASTER WORD LIST

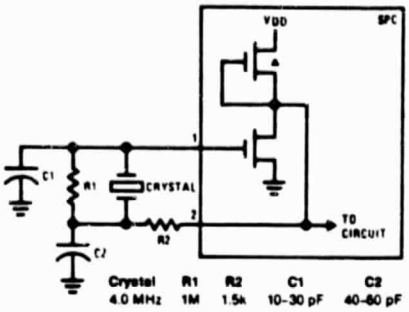
Word	8-Bit Binary Address SW8 SW1		8-Bit Binary Address SW8 SW1		8-Bit Binary Address SW8 SW1
THIS IS DIGITALKER	00000000	Q	00110000	IS	01100000
ONE	00000001	R	00110001	IT	01100001
TWO	00000010	S	00110010	KILO	01100010
THREE	00000011	T	00110011	LEFT	01100011
FOUR	00000100	U	W0110100	LESS	01100100
FIVE	00000101	V	00110101	LESSER	01100101
SIX	00000110	W	00110110	LIMIT	01100110
SEVEN	00000111	X	00110111	LOW	01100111
EIGHT	00001000	Y	00111000	LOWER	01101000
NINE	00001001	Z	00111001	MARK	01101001
TEN	00001010	AGAIN	00111010	METER	01101010
ELEVEN	00001011	AMPERE	00111011	MILE	01101011
TWELVE	00001100	AND	00111100	MILLI	01101100
THIRTEEN	00001101	AT	00111101	MINUS	01101101
FOURTEEN	00001110	CANCEL	00111110	MINUTE	01101110
FIFTEEN	00001111	CASE	00111111	NEAR	01101111
SIXTEEN	00010000	CENT	01000000	NUMBER	01110000
SEVENTEEN	00010001	400HERTZ TONE	01000001	OF	01110001
EIGHTEEN	00010010	80HERTZ TONE	01000010	OFF	01110010
NINETEEN	00010011	20MS SILENCE	01000011	ON	01110011
TWENTY	00010100	40MS SILENCE	01000100	OUT	01110100
THIRTY	00010101	80MS SILENCE	01000101	OVER	01110101
FORTY	00010110	160MS SILENCE	01000110	PARENTHESIS	01110110
FIFTY	00010111	320MS SILENCE	01000111	PERCENT	01110111
SIXTY	00011000	CENTI	01001000	PLEASE	01111000
SEVENTY	00011001	CHECK	01001001	PLUS	01111001
EIGHTY	00011010	COMMA	01001010	POINT	01111010
NINETY	00011011	CONTROL	01001011	POUND	01111011
HUNDRED	00011100	DANGER	01001100	PULSES	01111100
THOUSAND	00011101	DEGREE	01001101	RATE	01111101
MILLION	00011110	DOLLAR	01001110	RE	01111110
ZERO	00011111	DOWN	01001111	READY	01111111
A	00100000	EQUAL	01010000	RIGHT	10000000
B	00100001	ERROR	01010001	SS (Note 1)	10000001
C	00100010	FEET	01010010	SECOND	10000010
D	00100011	FLOW	01010011	SET	10000011
E	00100100	FUEL	01010100	SPACE	10000100
F	00100101	GALLON	01010101	SPEED	10000101
G	00100110	GO	01010110	STAR	10000110
H	00100111	GRAM	01010111	START	10000111
I	00101000	GREAT	01011000	STOP	10001000
J	00101001	GREATER	01011001	THAN	10001001
K	00101010	HAVE	01011010	THE	10001010
L	00101011	HIGH	01011011	TIME	10001011
M	00101100	HIGHER	01011100	TRY	10001100
N	00101101	HOUR	01011101	UP	10001101
O	00101110	IN	01011110	VOLT	10001110
P	00101111	INCHES	01011111	WEIGHT (Note 2)	10001111

Note 1: "SS" makes any singular word plural

Note 2: Address 143 is the last legal address in this particular word list. Exceeding address 143 will produce pieces of unintelligible invalid speech data.

Crystal Circuit Information

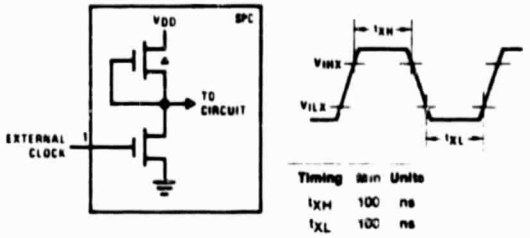
Typical Crystal Oscillator Network



Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10-30 pF	40-60 pF

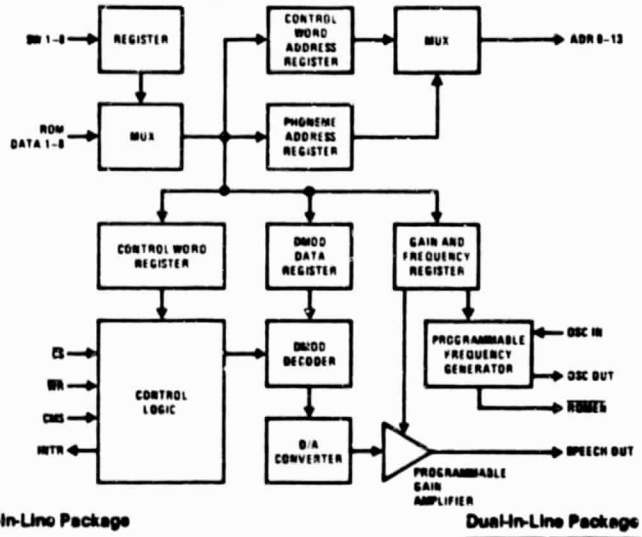
(4.0 MHz crystal manufactured by Electro Dynamics Corp P/N HC18-20 pF)

External Clock Input (4.0 MHz)

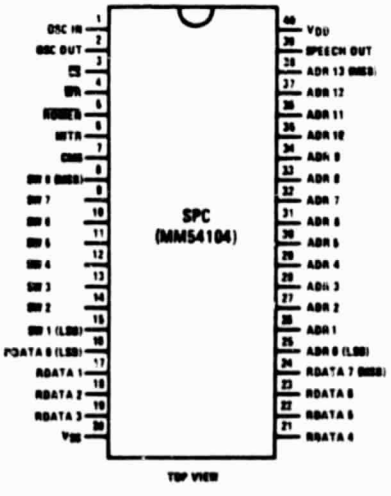


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

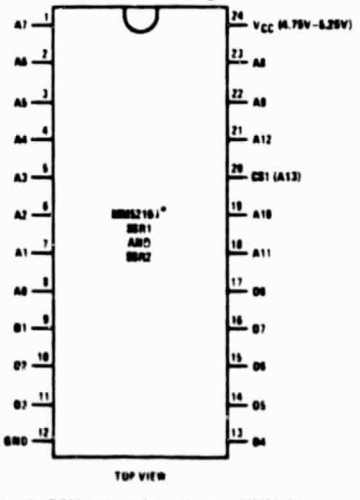
SPC Block and Connection Diagrams



Dual-In-Line Package

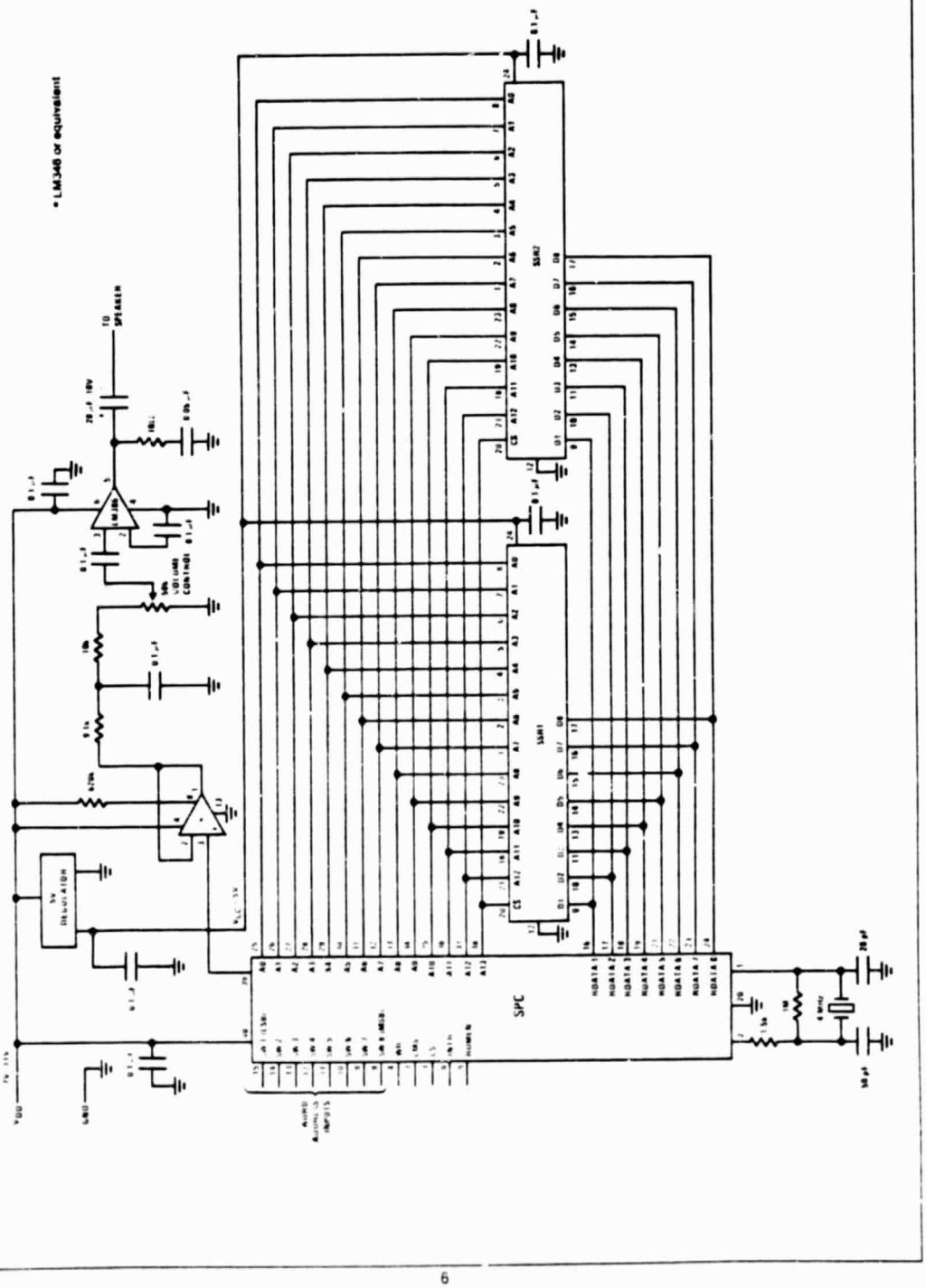


Dual-In-Line Package



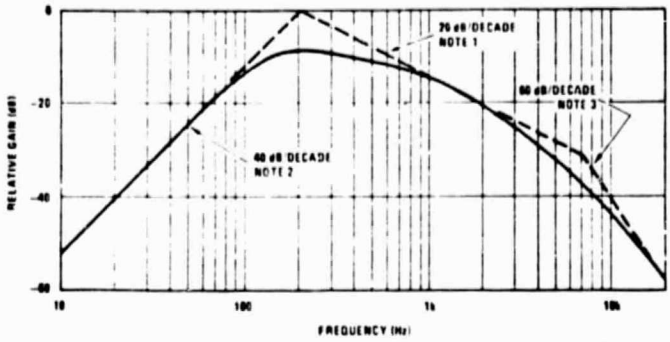
* For specific ROM device information, see MM52104 data sheet.

Recommended Schematic Diagram



Applications Information

Frequency Response of Combined Amplifier and Speaker



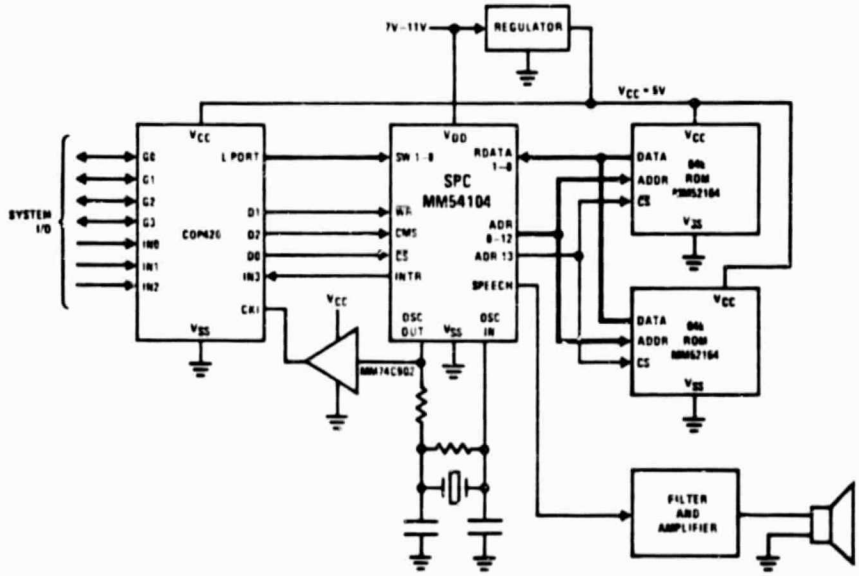
Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

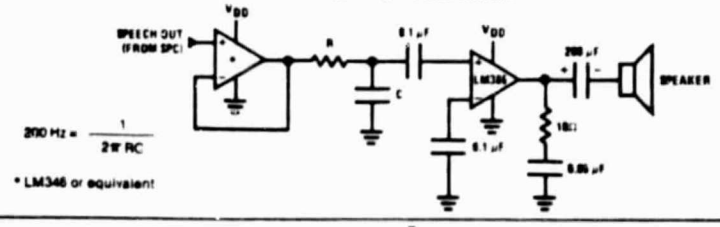
Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz–8000 Hz.

Typical Applications (Continued)

DIGITALKER System Using COP420 Interface



Minimum Filter Circuit

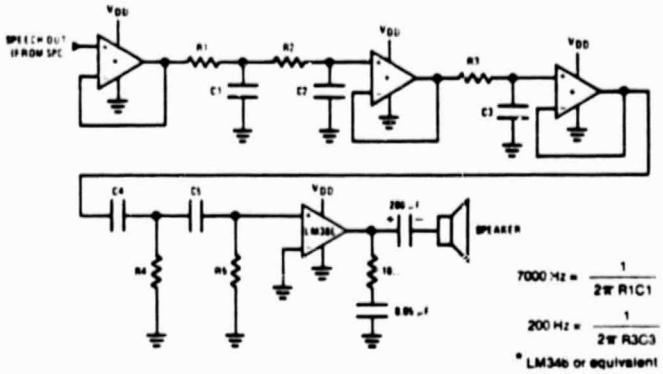


$$f_{3dB} = \frac{1}{2\pi RC}$$

* LM346 or equivalent

Typical Applications (Continued)

Filter Circuit to Produce Maximum Frequency Response

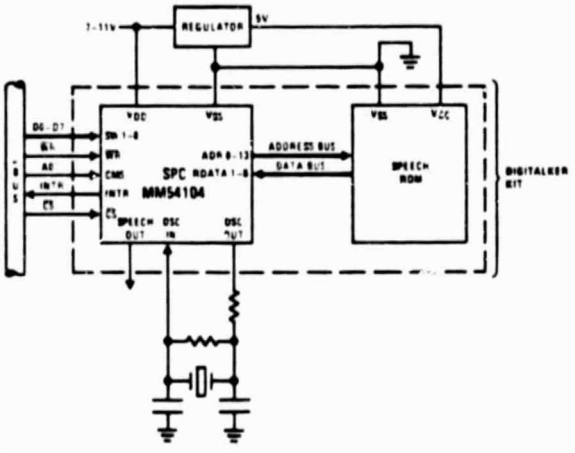


$$7000\ Hz = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

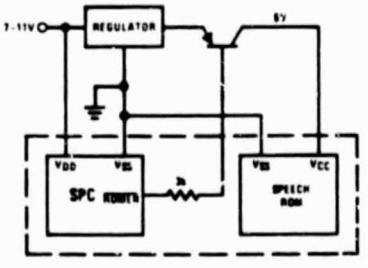
$$200\ Hz = \frac{1}{2\pi R3C3} = \frac{1}{2\pi R4C4} = \frac{1}{2\pi R5C5}$$

* LM34b or equivalent

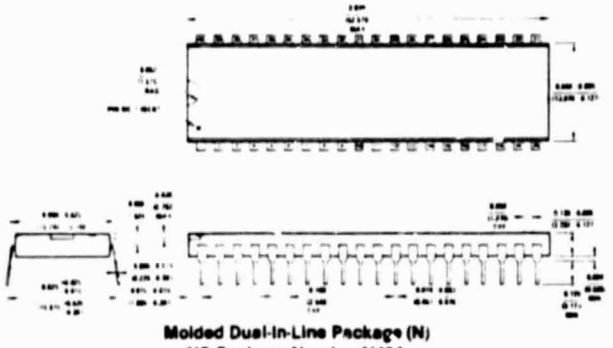
DIGITALKER System Utilizing MICROBUS™ Interface



Low Power Configuration Using Static ROM



Physical Dimensions inches (millimeters)

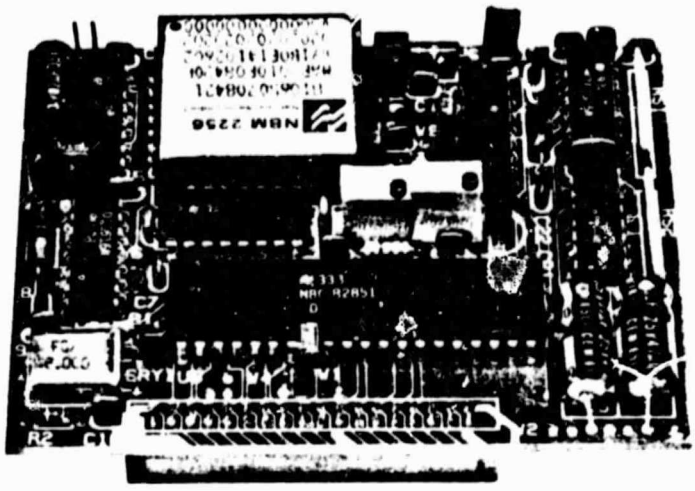


Molded Dual-In-Line Package (N)
NS Package Number N40A

National Semiconductor

PRELIMINARY
May 1981

BLX-9252
32K-Byte Bubble Memory Expansion Module Board



- BLX bus-compatible memory expansion module
- Smallest bubble memory subsystem
- 32K-bytes non-volatile storage
- 5.8 ms average access time
- Error detection and correction
- Removable
- Polled, interrupt, or DMA data transfers
- Operation to 70°C

Product Overview

The BLX-9252 is a member of the new line of BLX bus-compatible expansion module products from National Semiconductor. The BLX-9252 plugs directly onto any BLX bus-compatible host board offering low cost, incremental, on-board expansion. National offers several BLX bus-compatible host boards, such as the BLX-86/12B, BLX-80/11A/12A/14A, and BLX-80/116. The board offers the reliability and non-volatility of bubble memory technology, coupled with compatibility to the popular and convenient BLX bus.

The BLX-9252 features 32K-bytes of non-volatile storage capacity that can be configured into either 64-byte pages or 256-byte sectors. Data reliability is reinforced with a 12-bit Fire Code capable of detecting up to three random errors or an error burst up to 12 bits in length, and capable of correcting any error bursts of up to 3 bits in length. Data transfer can be accomplished in either polled or interrupt driven modes; or the BLX-9252 can be used as a channel to a DMA controller located on the host board. The BLX module is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance, freeing the host system's bus traffic for other system resources. Incremental power consumption is minimal, requiring only 4.6 watts.

Functional Description

Figure 1 is a functional block diagram of the BLX-9252. The board uses the NBM2256 Bubble Memory, its associated interface circuits, and the NBC82851 Bubble Memory Controller, all from National Semiconductor Corporation. The NBM2256 Bubble Memory provides 256K-bits of non-volatile storage which is formatted into 32K-bytes by the NBC82851 Controller. The Bubble Memory Controller generates the complex timing necessary to drive the Bubble Memory and also provides the user interface. The system

DA-B25M51/Printed in U.S.A.

software communicates with the BLX-9252 across the BLX interface, using I/O read/write commands to the Bubble Memory Controller's eight user accessible registers.

User Accessible Registers

Communication with the BLX-9252 is through the Bubble Memory Controller's eight user accessible registers; these are addressed as an 8-byte block of the host CPU's I/O space (see Specifications—I/O Addressing). Commands are issued by writing into the CMND register. Data is transferred through the FIFO register which accesses the current byte of the internal 16-byte FIFO. The address and length of the data block in the Bubble Memory is written into the Sector Address Registers (SAR) and the Multiple Sector Register (MSR); these registers are updated during a data transfer operation. The Status register (STR) may be read to monitor execution and error status (see Specifications—Device Status). The Residual Control Register (RCR) is provided to set various modes of controller operation (see Specifications—Residual Control). The System Features Register (SFR) also sets controller modes, but should always be set to zero in the BLX-9252.

Command Functions

The BLX-9252 has commands to Read and Write Data, Correct Data, and Position for minimum latency. The data space can be arranged into 512 pages of 64 bytes or 128 sectors of 256 bytes with the SECTOR/ PAGE ADDRESSING mode flag; a sector or a page is the minimum transfer size. Data is transferred through the FIFO as it is requested by the Data Request flag (DRQ).

System commands are available to initialize and shut down the BLX-9252. Initialization involves synchronizing the Bubble Memory and Controller, plus getting the Redundancy Map Information (RMPI) which is used to map out extra (redundant) storage locations in the Bubble Memory. For diagnostic and maintenance purposes, commands are also provided to read and write this RMPI, and to read and write data without mapping. RMPI data is also transferred through the FIFO.

The BLX-9252 command set is shown in Table I.

Data Transfer Modes

Three modes of data transfer to the BLX-9252 are possible: Program Controlled or Polled, Interrupt Driven, and DMA Controller Driven. These modes require various levels of host software intervention. In the Program Controlled mode, the Status register flags CNTRL NOT BUSY and DRQ are continuously polled by the host. CNTRL NOT BUSY indicates that the BLX-9252 has completed any operations and can accept a new command. DRQ indicates that the controller is ready to transmit or receive another byte of data. In the Interrupt Driven mode, the Bubble Memory Controller generates interrupts based on these flags, freeing the host from the need to continuously monitor the STR. The ENABLE NBUSY INT mode flag permits CNTRL NOT BUSY to generate an interrupt on MINTR0. The ENABLE DRQ INT flag permits DRQ to also generate an interrupt on MINTR0. The DRQ line can be connected to MINTR1, generating a MINTR1 interrupt upon a Data Request. In the DMA mode, the BLX-9252 is used as a channel to a DMA controller on the host board. The DMA controller is programmed with the data block parameters for the host system and the BLX-9252 with

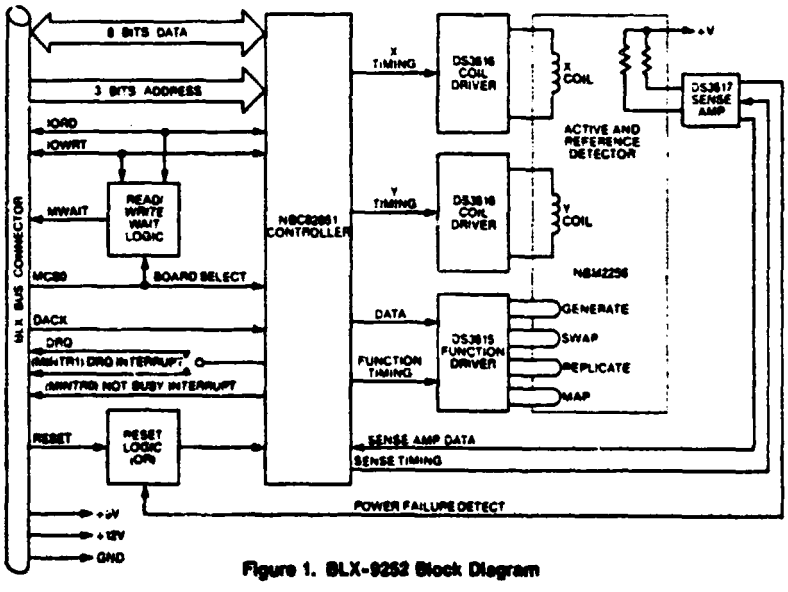


Figure 1. BLX-9252 Block Diagram

C-2

the appropriate transfer parameters. Issuing a transfer command to the BLX-9252 then causes data to be transferred under control of the host's DMA controller without program intervention.

Initialization and Reset

The BLX-9252 is initialized upon receipt of an initialize command or a low to high transition of the RESET line. Shutdown of all Bubble Memory operation is accomplished with the Terminate Immediate command. Terminate Immediate executes an orderly shutdown of the BLX-9252 within 30 µs. A Terminate Immediate is also accomplished by a high to low transition of the RESET line. The RESET line is ORed with a Power Fail signal which is activated when the on-board sense amplifier detects a power fail condition. The trip level of this sense circuit is adjusted by the PFA potentiometer which is preset at the factory between 95% and 90% of nominal supply level. When either the 5 V or the 12 V supply fails below the set percentage, the PFA signal is activated, generating a Terminate Immediate.

Host Bus Interface

The following is a brief description of the input/output signals of the BLX-9252.

Signal	Description
IORD/, IOWRT/	Active low Read and Write Command Signals. An active command line coupled with a chip select indicates that the address lines are valid and the BLX-9252 should perform the read or write.
MA0-MA2	Active high address lines, generally the three least significant bits of the I/O address. These lines address the eight user accessible registers of the BLX-9252.
MCS0/	Active low Module Card Select line which is the result of host I/O address decode logic. Note: If the MCS0/ signal glitches, BLX-9252 logic may cause a glitch on MWAIT/. MWAIT/ will be settled in less than 75 ns after MCS0/ settles.
RESET	Active High reset signal. Generates an orderly shutdown of the Bubble Memory System. When this signal makes a high to low transition, the system is initialized.
MD0-MD7	Active high bidirectional data lines. Used to transmit commands and to transfer data. MD0 is the least significant bit.
MWAIT/	Active low wait signal which indicates that the BLX-9252 has not yet completed the bus operation. MWAIT/ is activated immediately upon receipt of an MCS0/ signal. If the bus operation was a read, MWAIT/ will be deactivated after the data has been placed on the bus; if it was a write, MWAIT/ will be deactivated after the data has been written into the controller.
MPST/	Active low Module Present signal. This line is grounded on the BLX-9252.
MINTR0, MINTR1	Active high interrupt lines. Can be used to make interrupt requests to the host. A MINTR0 interrupt is generated by an interrupt from the Bubble Memory Controller. Mode flags in the RCR select the type of interrupt as a NBUSY interrupt, DRQ interrupt, or both. When Jumper W7 is closed between 1 and 2, a MINTR1 interrupt is generated by the DRQ line.
MDRQT, MDACK/	DMA handshake signals. MDRQT is an active high data transfer request signal from the BLX-9252 to the host's DMA controller which is enabled when jumper W7 is closed between 2 and 3. MDACK/ is an active low request acknowledge signal from the DMA controller. MDACK/ acts as the chip select for the Bubble Memory Controller and automatically selects the FIFO for data transfer independent of the address lines. The direction of data transfer will be determined by IORD/ and IOWRT/.

Installation

The BLX-9252 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 2 and 3).

BLX-9252 Jumper Options

Prior to use, all jumpers on the BLX-9252 should be set to system requirements. Jumper location is shown in Figure 3.

Jumper	Description
W1, W2 W4, W5	Always closed (provided for debugging).
W3, W6	Normally closed between 2 and 3. These two jumpers are closed between 1 and 2 only if it is desired to give a write map command and remain closed between 1 and 2 only during write map command.
W7	Normally closed between 2 and 3 to connect the controller DRQ to MDRQT/. Closed between 1 and 2 to connect DRQ to MINTR1.

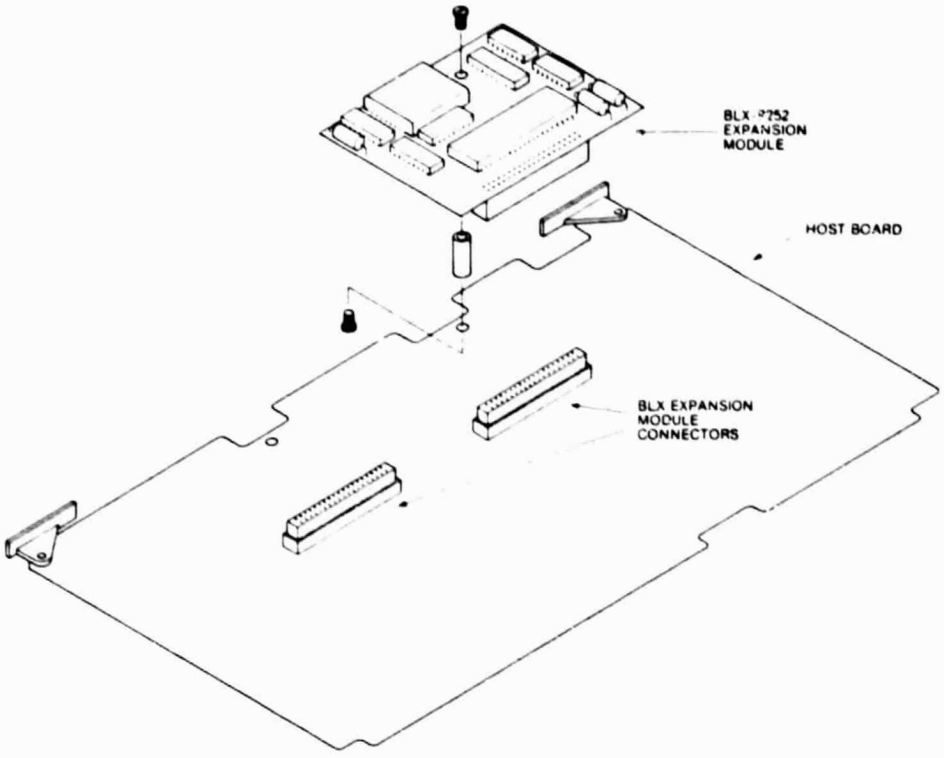


Figure 2. Installation of BLX-9252 Module on Host Board

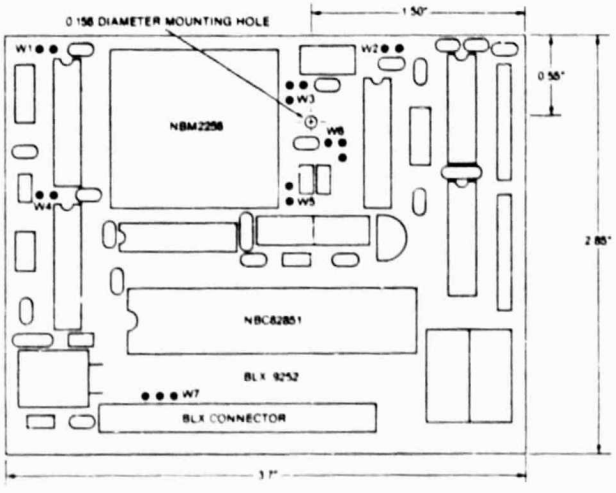


Figure 3. BLX-9252 Physical Dimensions and Component Placement

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Table I. BLX-9252 Command Set

Command Options	Hex Code	Registers[1]		Description	Bytes Transferred[2]		Status Flags Affected[3]
		Loaded	Altered		Page	Sector	
Read[4,5]	00	R,S	S	Read one P/S	64	256	C,D,O,E,R
RDM	08	R,S	S	Read one P/S without mask	71	282	C,D,O,E,R
SSD	04	R,S	S	Read one P/S but do not transfer	0	0	C,D,O,E,R
MS	10	R,S,M	S,M	Read multiple P/S	64*N	256*N	C,D,O,E,R
MS,RDM	18	R,S,M	S,M	Read multiple P/S without mask	71*N	282*N	C,D,O,E,R
MS,SSD	14	R,S,M	S,M	Read multiple P/S, no transfer	0	0	C,D,O,E,R
Write[4,5]	40	R,S	S	Write one P/S	64	256	C,D,O,R,W
WRM	48	R,S	S	Write one P/S without mask	71	282	C,D,O,R,W
SAD	44	R,S,F	S	Write one P/S, no data transfer	0	0	C,D,O,R,W
MS	50	R,S,M	S,M	Write multiple P/S	64*N	256*N	C,D,O,R,W
MS,WRM	58	R,S,M	S,M	Write multiple P/S without mask	71*N	282*N	C,D,O,R,W
MS,SAD	54	R,S,F,M	S,M	Write Multiple P/S, no transfer	0	0	C,D,O,R,W
Position	28	S		Position for zero read latency	0	0	C
W	68	S		Position for zero write latency	0	0	C
Initialize	F4			Synchronize without loading RMPI	0	0	C,M
LM	FC			Synchronize and load RMPI	0	0	C,E,M
Terminate	02		F	End any process at end of page	0	0	*
I	03		F	End any process immediately	0	0	
Read Map	80			Read RMPI	64	64	C,D,O,E
C	88			Read RMPI, compare to Map buffer	36	36	C,D,O,E,M
Write Map	C0			Write RMPI into map loop 2	64	64	C,D,O,W
M	C8			Write RMPI into map loop 1	64	64	C,D,O,W
Read Corrected[4]	0C	[7]	S,M	Read one P/S, correct any errors	64	64*NPTE	C,D,O,E,N,S

Notes:

1) Nomenclature: Residual Control Register (R), Sector Address Register (S), Multiple Sector Register (M), FIFO Register (F). Command Register is loaded and Status is altered by all commands and thus not listed.

2) Number of Pages or Sectors (N). Number of Pages to Error (NPTE)

3) Nomenclature: CNTRL NOT BUSY (C), DRQ (D), OVERRUN (O), ERROR IN DATA (E), NON-CORRECTABLE ERROR (N), MAP COMPARE OR SYNC ERROR (M), RANGE ERROR (R), WRITE PROTECTED MBM (W), SOFT ERROR CONDITION (S).

4) The Read, Write, and Read Corrected commands will execute for sectors if the SECTOR/PAGE ADDRESSING bit in the RCR is not set, pages if it is, although Read Corrected is normally only used in page mode. P/S = Pages or Sectors.

5) Setting both RDM and SSD or WRM and SAD options is not permitted.

6) Termination status after Terminate command is the same as the status of the terminated command.

7) No registers may be modified between Read Sector command and Read Corrected Command.

Table II. BLX-9252 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	Signal Ground	36	+5V	+5 Volts
33	MD0	MDATA Bit 0	34	MDRQT	M DMA Request
31	MD1	MDATA Bit 1	32	MDACK/	M DMA Acknowledge
29	MD2	MDATA Bit 2	30		
27	MD3	MDATA Bit 3	28		
25	MD4	MDATA Bit 4	26		
23	MD5	MDATA Bit 5	24		
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20		
17	GND	Signal Ground	18	+5V	+5 Volts
15	IORD/	I/O Read Command	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Command	14	MINTR0	M Interupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10		
7	MA2	M Address 2	8	MPST/	ISBX Multimodule Board Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Ground	4	+5V	+5 Volts
1	+12V	+12 Volts	2		

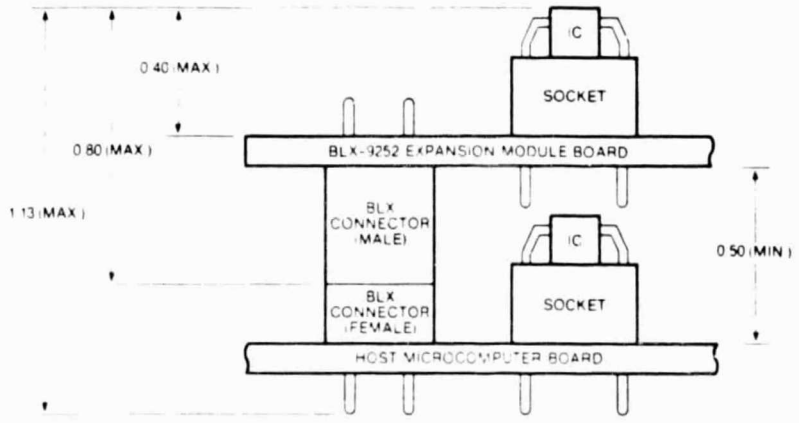

Figure 4. BLX-9252 Expansion Module Mounting Clearances (inches)

Specifications

DC Power Requirements

		Operating	Standby	Max.
V_{CC} = +5V ± 5%	I_{CC} =	200 mA	300 mA	400 mA
V_{DD} = +12V ± 5%	I_{DD} =	300 mA	70 mA	400 mA

Power supply voltage fall time from 95% to 90% of specified value shall not be less than 150 µs

DC Electrical Characteristics

Parameter	Description	Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = Max.		0.5	V
V_{OH}	Output High Voltage	I_{OH} = Min.	2.4		V
I_{IL}	Input Low Current	MD0-MD7, MA1-MA2 MCS0/, RESET, OPT0 MDACK/, IORD/, IOWRT/		−0.5 −1.6 −1.0	mA mA mA
I_{IH}	Input High Current	MD0-MD7, MA0-MA2 MCS0/, RESET, MDACK/, IORD/, IOWRT/, OPT0,		70 100	µA µA
I_{OL}	Output Low Current	MD0-MD7 MINTR0, MINTR1, MDRQT MWAIT/		2.5 2.0 1.6	mA mA mA
I_{OH}	Output High Current	MD0-MD7 MINTR0, MINTR1, MDRQT, MWAIT/		−200 −100 −50	µA µA µA

Note: Stated limits do not apply to MPST/ on the BLX-9252, as it is connected to Ground.

AC Electrical Characteristics

Symbol	Parameter	Min. (ns)	Max. (ns)
t_1	Address stable before read	50	
t_2	Address stable after read	30	
t_3	Read pulse width (with MWAIT/)	500	
t_4	Data valid from read		350
t_5	Data float after read		30
t_7	CS stable before read	25	
t_8	CS stable after read	30	
t_{9a}	Power supply in spec to RESET	25 ms	
t_{9b}	Rising edge of RESET to data bus disabled		50 ms
t_{10}	Address stable before WRT	50	
t_{11}	Address stable after WRT	30	
t_{12}	Write pulse width (with MWAIT/)	500	
t_{13}	Data valid to write	350	
t_{14}	Data valid after write	30	
t_{15}*	Data valid from falling edge of write		150
t_{17}	MWAIT/ pulse width	525	1.5 µs
t_{18}	Reset pulse width	25 ms	
t_{19}	MCS/ to MWAIT/ valid	0	75
t_{20}	DACK set up to I/O read or write	100	
t_{21}	DACK hold	30	
t_{22}	Read or write to MDRQT		200
t_{24}	MWAIT/ to valid read data		0
t_{25}	MWAIT/ to end of write		0

*This does not conform to the BLX bus specification

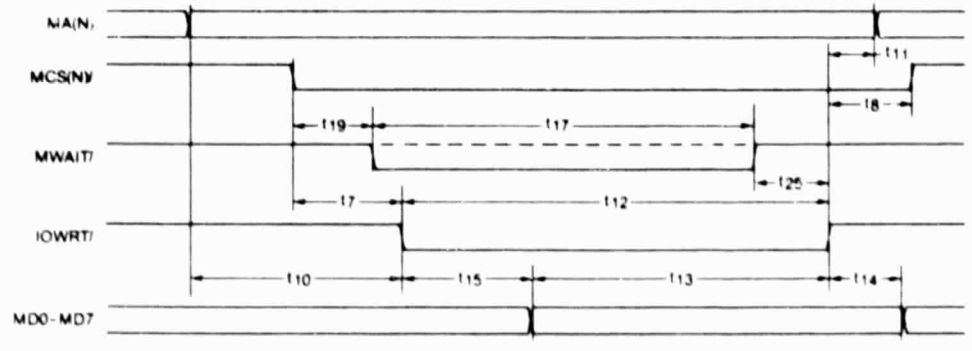

Figure 5. BLX-9252 Board I/O Write Timing

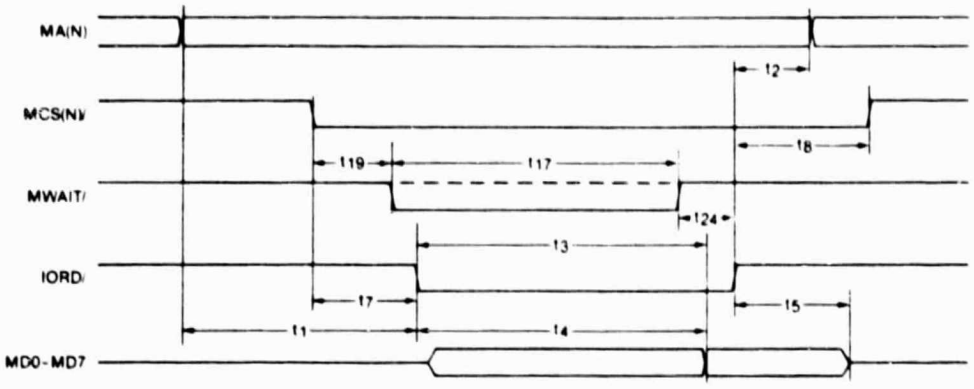

Figure 6. BLX-9252 Board I/O Read Timing

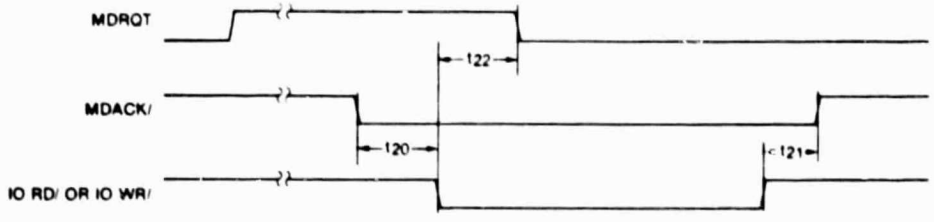

Figure 7. BLX-9252 Board I/O DMA Timing

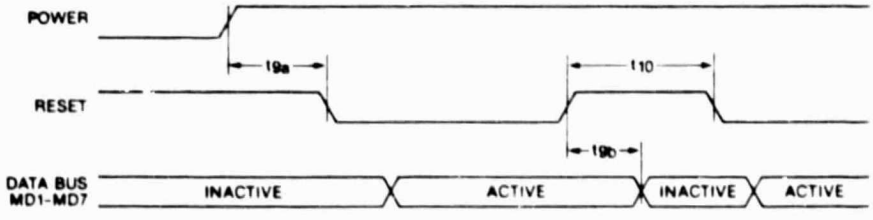

Figure 8. Board Reset Timing

Word Size

Data — 8 bits

I/O Addressing

Register Name	Symbol	Type of Operation	Connector Port Address
Command	CMDR	Write	X0
Multiple Sector	MSR	Read/Write	X1
Sector Address bits 0-7	SAR 0-7	Read/Write	X2
Sector Address bits 8-15	SAR 8-15	Read/Write	X3
Residual Control	RCR	Write	X4
System Features (not used)	SFR	Write	X5
Status	STR	Read	X6
FIFO (data transfer)	FIFO	Read/Write	X7

Note: The port addresses are determined by the host microcomputer. Refer to the Hardware Reference manual for your microcomputer to determine the first digit (X) of the connector port addresses.

Device Status Register

S	W	M/R	N	E	O	D	C

7 0

C — CNTRL NOT BUSY indicates that the controller is currently not executing a command (1 = Not Busy).

D — DRQ indicates a Request to transfer data (1 = Data Request).

O — DATA OVERRUN indicates a FIFO overflow (underflow) or an illegal attempt to transfer data (1 = Error).

E — ERROR DETECTED indicates that the data or RMPI just read contains an error. For READ CORRECTED command, indicates that an error exists in another ECC block of the same sector (1 = Error).

N — ERROR NOT CORRECTABLE indicates that READ CORRECTED could not correct the error (1 = Error).

R — END OF RANGE indicates that the last page address is being accessed (1 = Last Page).

M — MAP COMPARE or INIT ERROR indicates that the RMPI in the Bubble Memory does not match the RMPI in the controller or contains no sync code (1 = Error).

Note: (R) and (M) are wire-ORed onto bit 5, as they occur under different commands, they will never occur together.

W — WRITE PROTECT indicates that an attempt to write to a write-protected board occurred (1 = Error).

S — SOFT ERRORS PRESENT indicates that a different error has been detected in a READ CORRECTED command (1 = Error).

If the CNTRL NOT BUSY bit in the Status Register is a zero, the only other bit that is defined is DRQ; if one, the operation is complete and the other status bits are defined as given above.

Residual Control Register

—	F	S	H	N	D	A	W

7 0

W — WRITE PROTECT inhibits writing to the Bubble Memory (1 = Protected).

A — SECTOR/PAGE ADDRESSING selects addressing mode (1 = Sector, 0 = Page).

D — ENABLE DRQ INTERRUPT enables the DQR flag to MINTR0 (1 = Enabled).

N — ENABLE NBUSY INTERRUPT causes CNTRL NOT BUSY to activate MINTR0 (1 = Enabled).

H — FIFO HALF FULL (EMPTY) inhibits DRQ until the FIFO is half-filled or half empty instead of immediate (1 = Half, 0 = Immediate).

S — STERD (Stop if Error Detected) terminates a read at the end of the current page when an error is detected. Must be on to use READ CORRECTED (1 = Stop on Error, 0 = Do not Stop).

F — READ FIFO ENABLE permits reading but not writing FIFO when CNTRL NOT BUSY; otherwise writing but not reading is permitted. Must be cleared before executing a command (1 = Read OK, 0 = Write OK).

Data Rates

Average Data Rate — 13.5K-bytes/s

Average Access Time — 5.8 ms

Max. Response Time to DRQ — FIFO HALF FULL on: 512 µs
FIFO HALF FULL off: 1024 µs

Interrupt Requests — Two optional interrupt requests: DRQ on MINTR1 and NBUSY or DRQ on MINTR0 as selected in the RCR. The NBUSY interrupt is set by CNTRL NOT BUSY, and is reset by a bus read or write.

Interfaces

BLX Bus — All signals TTL compatible

Physical

Length: 2.83 in. (7.19 cm)
Width: 3.70 in. (9.40 cm)
Depth:
BLX-9252 including connector
0.80 in. (2.04 cm)
BLX-9252 plus Host Board
1.13 in. (2.86 cm)
Weight: 3.07 oz. (87 gm)

Environmental

Temperature:
Operating: 0°C to 50°C at 100% duty cycle (see figure 10)
0°C to 70°C at negligible duty cycle
Non-volatile storage:
−40°C to 100°C
Relative Humidity: 90% maximum, non-condensing
Air Cooling: 10 CFM recommended
Thermal Shock: ±30°C/hr. max. rate

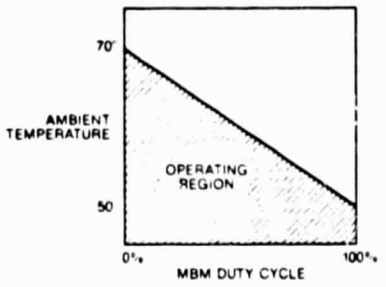

Figure 9. Bubble Memory Maximum Operating Temperature

Duty cycle constraint must be satisfied over any interval where the total time of operation, which may or may not be contiguous, exceeds one minute. Thus a 10% duty cycle may consist of up to 1 minute of operation total and 9 minutes of standby during any 10 minute interval.

Ordering Information

BLX-9252	32K-Byte Bubble Memory Expansion Module

Documentation

420400014-000	NBC82851 User's Manual (order separately)

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VERSATILE SPEECH MODULE™ (VSM/1)

Votrax®
PRODUCT DATA

FEATURES

- **True synthetic speech technology** and a built in microcomputer eliminate the constraints of a small fixed vocabulary speech module
- **Ultra low bit rate** of the SC-01 maximizes ROM word storage capabilities
- **Large lexicon** of commonly used words with industrial engineering base stored in EPROM
- **Built in prefix/suffix table** for prestored words
- **Additional vocabulary** can be created and permanently stored
- **Phoneme accessing capability** for unlimited vocabulary
- **Speech rate and pitch** dynamic programming for stress patterns and simulation of multi-voice environments
- **Sound effects**, from gunfire to musical sequences can be easily created from prestored sound macros. Additional sound macros can be user defined and EPROM stored for even greater flexibility.
- **Expandable** via interface ports
- **Parallel and RS232 compatible serial interfacing** with selectable baud rates and terminal modes
- **Foreground and background** simultaneous operation for speech and voxOS (voice operating system)
- **Built in microcomputer** can also simultaneously perform monitoring activities and execute speech commands

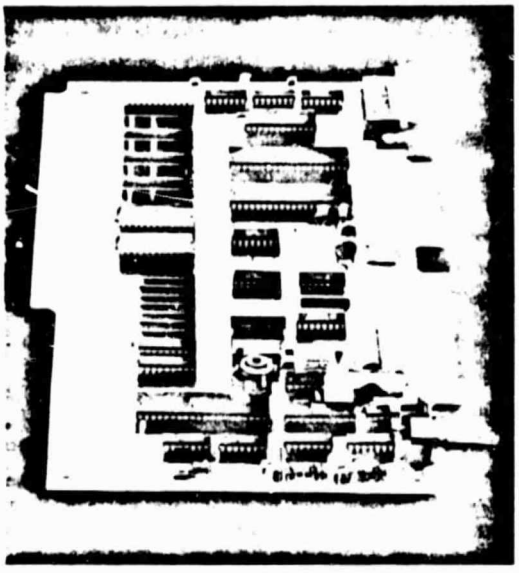

Figure 1. Votrax **VSM/1'™** (Versatile Speech Module)

APPLICATIONS

- The **VSM/1'™** can be used as a **microcomputer** to simulate or develop talking products, such as a talking calculator or talking games. It can also be used for unlimited real time speech synthesis while simultaneously executing commands and performing monitoring activities.
- The **VSM/1'™** can plug directly into the card cage of an industrial control computer to provide **prompting for operating personnel** (instructions for a real time situation). Typical applications are chemical processing plants, nuclear power stations, aircraft systems, seismic monitoring stations and automated warehousing.

Votrax®
Division of Federal Screw Works
500 Stephenson Highway, Troy, Michigan 48084
Phone (313) 588-2050

APPLICATIONS (continued)

- The **VSM/1'™** can operate in a computer-to-computer mode for **task downloading** in addition to voice synthesis. It is a smart peripheral which can be used in a distributed processing mode. Instructions and activities can be dynamically supplied from another computer or from a user ROM.

DESCRIPTION

The Votrax **VSM/1'™** introduces a new level of computer speech module performance and flexibility. It removes the constraints imposed by small fixed vocabulary speech modules typically used by designers. The **VSM/1'™** is based on the truly synthetic speech technology of the SC-01.

The SC-01 is a completely self-contained solid state device which phonetically synthesizes speech from low data rate inputs. Over 1,300 industrial/engineering based words can be stored in as little as 8K bytes of ROM. By using the built in prefix/suffix table, a repertoire of several thousand words can be created. Additional vocabulary, tailored to the user's specific needs can be permanently configured on up to 8K bytes of EPROM via on board sockets.

Using the phoneme capabilities of the SC-01, along with the prestored words, the **VSM/1'™** can produce an unlimited vocabulary. Speech rate, pitch and pause controls can be dynamically programmed, via control codes, to produce stress patterns. By altering the master clock controls, many human voice effects can be programmed to simulate a multi-voice environment.

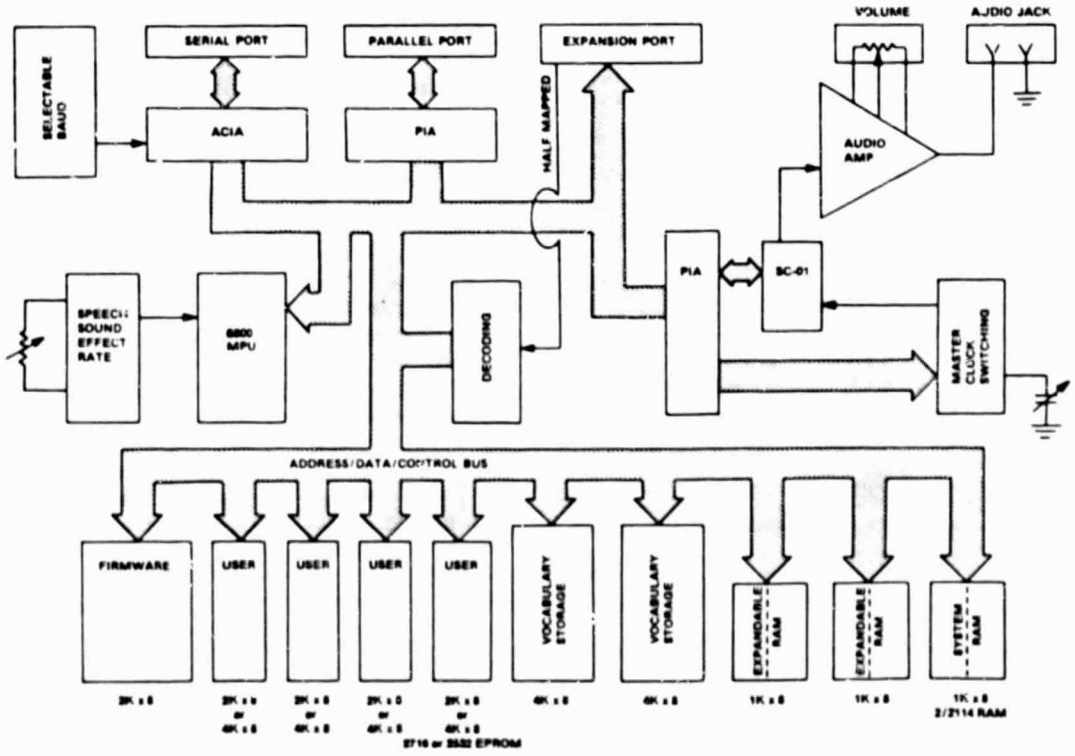

Figure 2. **VSM/1'™** Flow Diagram

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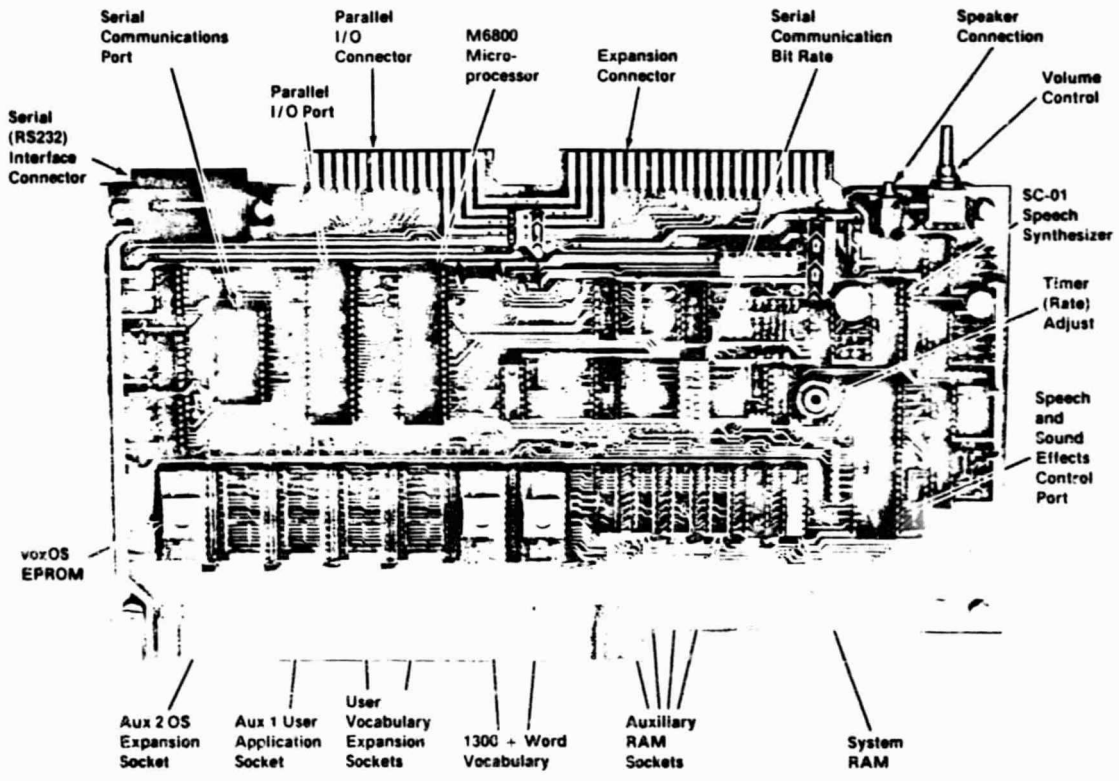

Figure 3. **Versatile Speech Module™** Circuit Card

The **VSM/1™** can produce a multitude of sound effects from prestored sound macros. Space sounds, gunfire, explosions, race cars and even musical sequences can be easily created. For additional flexibility, additional sound macros can be user defined and stored in the EPROM's.

The voice operating system (voxOS) may be user bypassed. The user can supply the necessary firmware to change the system function. This change, for example, can be from an experimental system to an actual application.

The **VSM/1™** has four audio sequence memories for loading speech callout codes, system controls, prestored speech and/or sound effects. System changes can be accomplished by placing a user supplied EPROM in one of the vacant card sockets on the **VSM/1™**

The **VSM/1™** can be used as a microcomputer to talk and execute commands, or as a smart peripheral that is expandable by interface ports. System functions can be changed by downloading a 6800 compatible code segment.

VERSATILE SPEECH MODULE™ – VSM/1

SPECIFICATIONS

General

- 1,300 + prestored vocabulary
- Prefix/suffix modifiers
- Phoneme mode
- Sound effects
- Speech stress
- Usable as a general purpose controller/simulator

Hardware

- SC-01 phoneme synthesizer
- Powerful 6800 MPU (microprocessor unit) based design
- Parallel and serial (RS232) interface (selectable baud rate of 75 - 9600 bits per second)
- 1K byte RAM (sockets for additional 2K bytes)
- 2K byte voxOS operating system
- 8K byte prestored vocabulary ROM
- Expansion sockets for an additional 8K bytes (2716) to 16K bytes (2532) of jumper selectable EPROM's
- On board audio amplifier, 8 ohm, 1 watt, with volume control
- Half memory plane expansion connector (32K locations out of 64K. Customer access to 32K locations via the microcomputer data address bus.)
- Form compatible with a popular microcomputer board
- Variable speech rate clock
- Variable master clock frequency circuitry for pitch control

voxOS

- Full feature byte oriented editor (insert, delete change and move data pointer)
- Computer and terminal prompting modes
- Phonemes, sound effects, controls and prestored speech may be intermixed in any audio sequence memory
- 4 audio sequence memories + 1 sound effects control memory (16 blocks of 8 parameters each)
- Memory dump
- Execute 6800 operating code sequence (for downloading or overriding operating system)
- 12 prestored sound macros (to provide basic waveshapes for user selection of features)
- 4 user definable sound macros (to reside in user supplied ROM firmware)
- 48 programmable MCRC (master clock resistor capacitor) settings for continuous dynamic manipulation of audio parameters (instantaneous course controls)
- 4 MCRC transitioned trim controls (slowly step toward target)
- voxOS bypass (to jump into user supplied firmware)

Audio Sequence Commands

- Prestored speech callout (16K byte direct access range)
- Two phoneme execution modes (fixed inflection and transitioned inflection)
- 4 fixed inflection levels (instant)
- 4 transitioned inflection levels (step)
- 16 sound effect (commands) control blocks (load control memory and pick 1 of the 16)
- 8 speech rates (will not affect sound effects)
- 8 pause durations
- 8 prompting sounds (canned sound effects)
- Prestored prefix/suffix word modifiers

Votrax®
Division of Federal Screw Works
500 Stephenson Highway, Troy, Michigan 48084
Phone (313) 588-2050

Votrax
A Division of Federal Screw Works
500 Stephenson Highway
Troy, Michigan 48084

SC-01 SPEECH SYNTHESIZER DATA SHEET

Votrax® CMOS Phoneme Speech Synthesizer

GENERAL DESCRIPTION

The SC-01 Speech Synthesizer is a completely self-contained solid state device. This single chip phonetically synthesizes continuous speech, of unlimited vocabulary, from low data rate inputs. Figure 1.

Speech is synthesized by combining phonemes (the building blocks of speech) in the appropriate sequence. The SC-01 Speech Synthesizer contains 64 different phonemes which are accessed by a 6-bit code. It is the proper sequential combination of these phoneme codes that creates continuous speech.

The SC-01 Speech Synthesizer is cost-effective, consumes minimal power and enables in-house product development without vendor dependency. Signals from the SC-01 are applied to an audio output device to amplify and distribute the synthesized speech. See Figure 2.

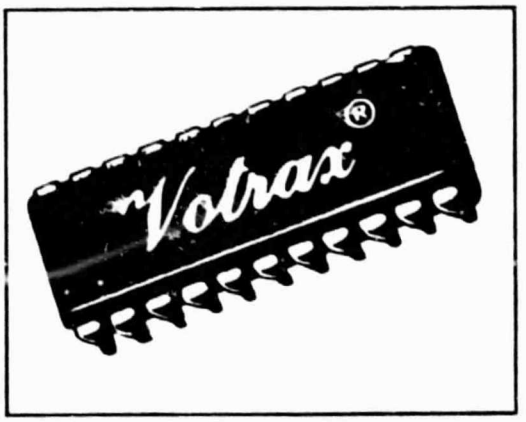

Figure 1. Votrax® SC-01 Speech Synthesizer

FEATURES

- Single CMOS chip
- 70 bits per second
- 22 pin package
- 9 mA current drain
- Wide voltage supply range
- Latched 5V compatible inputs
- Digital pitch level inputs
- Automatic inflection
- On-chip master clock circuit
- Optional external master clock
- Variety of voice effects
- Sound effects
- Customer product security

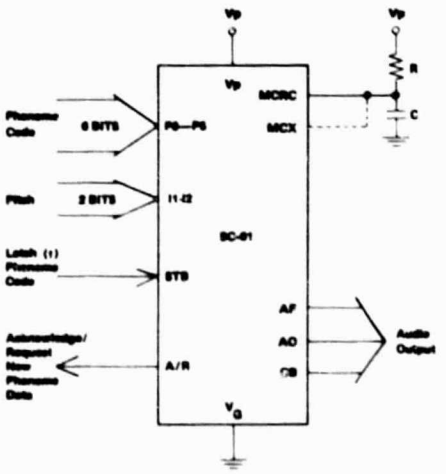

Figure 2. SC-01 Flow Diagram

PHYSICAL DESCRIPTION

The SC-01 Speech Synthesizer is a 22 pin Large Scale Integrated Circuit which contains all the circuitry necessary to generate phonetically synthesized speech. The SC-01 is fabricated using CMOS technology, which offers high input impedance and low power drain.

ELECTRICAL DESCRIPTION

The SC-01 Speech Synthesizer is a program-compatible with existing Votrax® phoneme synthesizers. It requires 70 bits of data per second for continuous speech production. The 6-bit phoneme codes are 5 volt logic compatible and are latched for data bus applications. A phoneme-construction algorithm and filters, within the chip, create the synthesized audio output.

PHONEME DESCRIPTION

Table 1 lists the 64 phonemes produced by the SC-01. Each phoneme code is accompanied by its symbol, average duration time, and an example. The underlined segments of the example word demonstrate the phoneme use, i.e., sound to be pronounced.

Table 2 subdivides the 64 phoneme symbols into seven categories. Each category represents a different production feature. The first six categories are characterized by voiced, fricative (expired voice), and nasal sounds. The seventh category is characterized by phonemes with no sound output.

PHONEME PROGRAMMING

Manual Operations: Votrax® maintains a library of phonetically programmed words. Reference to this library and programming manuals will aid in word synthesis.

Automatic Operations: Votrax® can supply a micro-computer system for automatic conversion of English text into phoneme sequences. This system is particularly useful for in-house vocabulary development and product security. Contact Votrax® for further information.

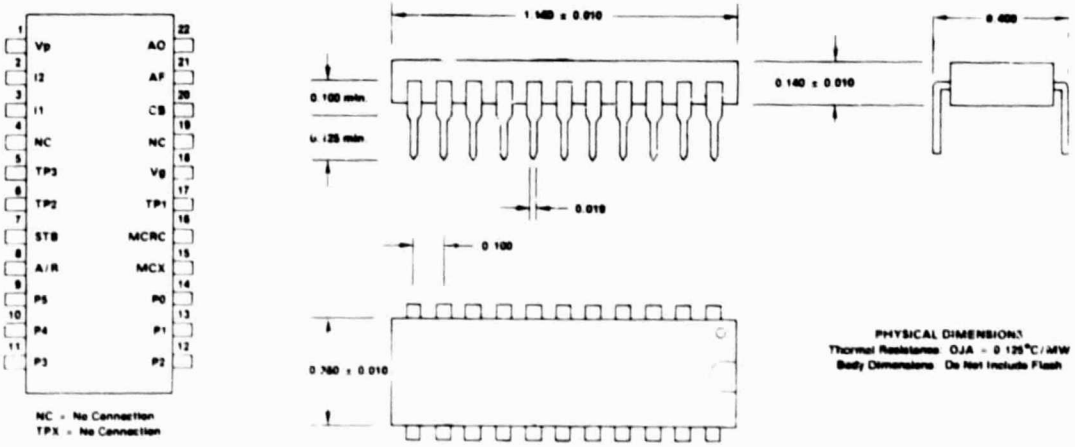

Figure 3 SC-01 Footprint and Outline Dimensions

Table 1 Phoneme Chart

Phoneme Code	Phoneme Symbol	Duration (ms)	Example Word
00	EH3	59	jacket
01	EH2	71	enlist
02	EH1	121	heavy
03	PA0	47	no sound
04	DT	47	butter
05	A2	71	made
06	A1	103	made
07	ZH	90	azure
08	AH2	71	honest
09	I3	55	inhibit
0A	I2	80	inhibit
0B	I1	121	inhibit
0C	M	103	mat
0D	N	80	sun
0E	B	71	bag
0F	V	71	van
10	CH*	71	chip
11	SH	121	shop
12	Z	71	zoo
13	AW1	146	lawful
14	NG	121	thing
15	AH1	146	father
16	OO1	103	looking
17	OO	185	book
18	L	103	land
19	K	80	trick
1A	J*	47	judge
1B	H	71	hello
1C	G	71	get
1D	F	103	fast
1E	D	55	paid
1F	S	90	pass

Phoneme Code	Phoneme Symbol	Duration (ms)	Example Word
20	A	185	day
21	AY	65	day
22	Y1	80	yard
23	UH3	47	mission
24	AH	250	mop
25	P	103	past
26	O	185	cold
27	I	185	pin
28	U	185	move
29	Y	103	any
2A	T	71	tap
2B	R	90	red
2C	E	185	meet
2D	W	80	win
2E	AE	185	dad
2F	AE1	103	after
30	AW2	90	salty
31	UH2	71	about
32	UH1	103	uncle
33	UH	185	cup
34	O2	80	for
35	O1	121	aboard
36	IU	59	you
37	U1	90	you
38	THV	80	the
39	TH	71	thin
3A	ER	146	bird
3B	EH	185	get
3C	E1	121	be
3D	AW	250	call
3E	PA1	185	no sound
3F	STOP	47	no sound

T must precede CH/ to produce CH sound

D must precede /J/ to produce J sound

Table 2 Phoneme Categories According to Production Features

Voiced					'Voiced' Fricat.	'Voiced' Stop	Fricative Stop	Fricative	Nasal	No Sound
E	EH	AE	UH	OO1	Z	B	T	S	M	PA0
E1	EH1	AE1	UH1	R	ZH	D	DT	SH	N	PA1
Y	EH2	AH	UH2	ER	J	G	K	CH	NG	STOP
Y1	EH3	AH1	UH3	L	V		P	TH		
I	A	AH2	O	IU	THV			F		
I1	A1	AW	O1	U				H		
I2	A2	AW1	O2	U1						
I3	AY	AW2	OO	W						

SIGNAL DESCRIPTION (See Figures 4 and 5)

Phoneme 6-Bit Selection Code (P0-P5): Data input is to six pins. Latching is controlled by the strobe (STB) signal.

Strobe (STB): Latching occurs on rising edge of strobe signal.

Inflection Level Setting (I1, I2): Instantaneously sets pitch level of voiced phonemes.

Acknowledge/Request ($\bar{A}$/R): Acknowledges receipt of phoneme data (signal goes from high to low one master clock cycle following active edge of STB signal). Also indicates timing out of old phoneme concurrent with request for new phoneme data (signal goes from low to high).

NOTE

If external phoneme timing is desired, phoneme requests can be ignored. However, best speech is realized with internal timing.

Master Clock Resistor-Capacitor (MCRC): This input determines the internal master clock frequency. Select R-C values for 720 kHz to achieve standard phoneme timing. Connect this input to MCX when using internal clock; ground when using external clock.

NOTE

Varying clock frequency varies voice and sound effects. As clock frequency decreases, audio frequency decreases and phoneme timing lengthens. Figures 6 and 7 illustrate manual and DAC (Digital to Analog Converter) voice variation schematics, respectively.

Master Clock External (MCX): Allows control by an external clock signal.

NOTE

Ground MCRC during MCX operation.

Audio Output (AO): Supplies analog signal to audio output device.

Audio Feedback (AF): Used with Class A or Class B transistor audio amplifiers for added stability.

Class B (CB): Current source for Class B transistor audio amplifier.

Table 3. Timing Specifications

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input Setup Time (P_I to STB)	T_S	450			NS
Input Hold Time (P_I to STB)	T_H	0			NS
Rise Time of STB Edge (.8V to 4V)	T_{RS}			100	NS
A/R Width ($\bar{A}$/R Connected to STB) *	T_{ARW}	1	1.3	2	µs
STB Width	T_{SW}	200			NS
STB Low*	T_{SL}				NS
Propagation Delay (STB to A/R after T_{ARW})	T_{DAR}			500	NS
A/R Rise Time (Capacitive load = 30pf)	T_{RAR}			100	NS
A/R Fall Time (Capacitive load = 30pf)	T_{FAR}			100	NS
Time from $\bar{A}$/R Request to STB Service)	T_{ARS}	0		500	µs
Time of Phoneme Duration *	T_{PH}	47	107	250	MS

* *Dependent on Master Clock frequency. 720k Hz*

* Strobe must remain low (72x Master Clock Period) before rising edge

Votrax® reserves the right to alter its product line at any time, or change specifications or design without notice and without obligation.

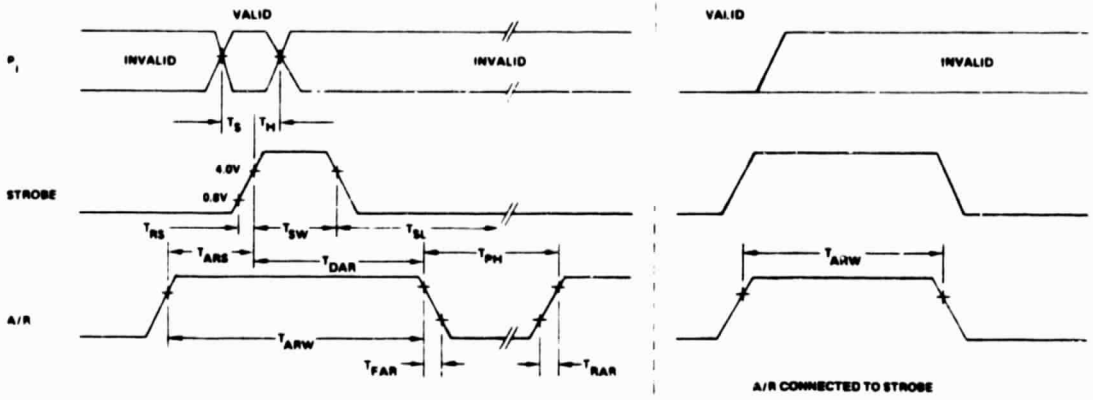

Figure 4. Timing Diagram

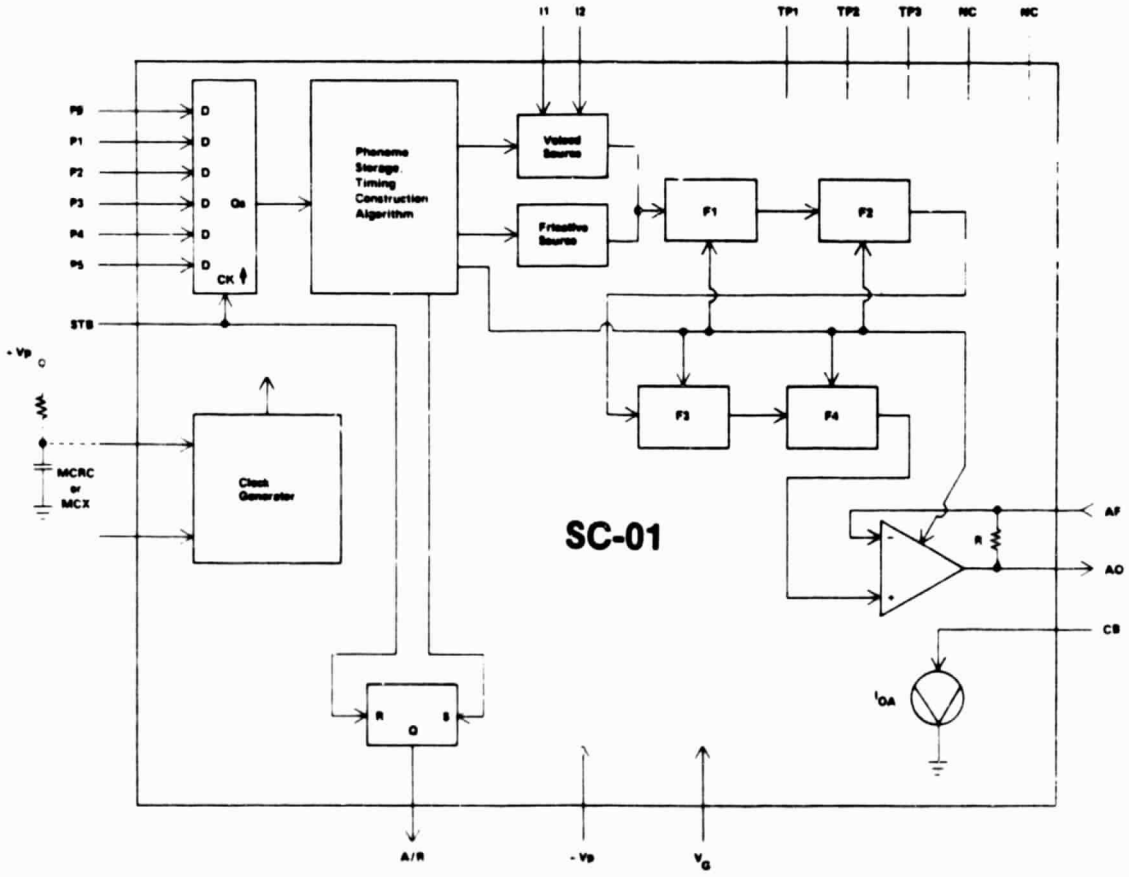

Figure 5. SC-01 Block Diagram

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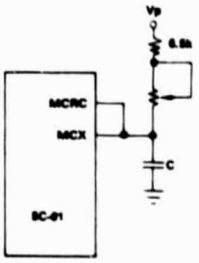

Figure 6. Variable Voice by Potentiometer Control

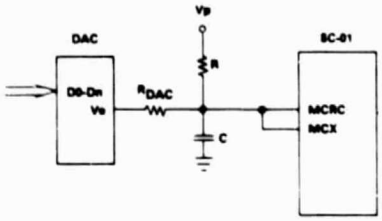

Figure 7. Variable Voice by DAC Current Injection

TYPICAL APPLICATIONS

General: The SC-01 Speech Synthesizer is easily designed into systems ranging in complexity from ROM/counters to microprocessor controllers.

Single Message System: See Figure 8. When the counter is released (START is TRUE) the message is clocked out of the ROM by the A/R signal. The system must be stopped when DONE is TRUE. Note: When using A/R tied to STB, connect a .01 uf capacitor to TP3 to insure power up reset of SC-01.

NOTE

Data at address 0 must be a pause phoneme code.

Multiple Message, Fixed Block Size: See Figure 9. Message address block is loaded into the counter. The message is then clocked out of the ROM by the A/R signal.

NOTE

Message Block = 2^n maximum.

Multiple Message, Variable Block Size: See Figure 10. The microprocessor loads phonemes into a data bus. The A/R signal generates an interrupt request for each new phoneme.

CONNECTING THE AUDIO OUTPUT DEVICE

Audio Output: The AO signal has a maximum peak to peak voltage swing of .26 times Vp, depending upon the phoneme selected, and the AO signal is D.C. biased.

Class A Amplifier: See Figure 11. For a single transistor amplifier, the selection of R, C, or R_s values depends upon the value of Vp and the desired audio level.

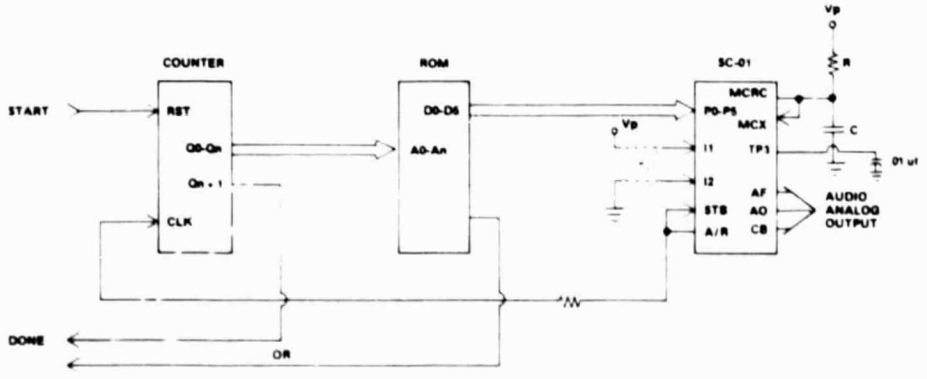

Figure 8. Single Message System

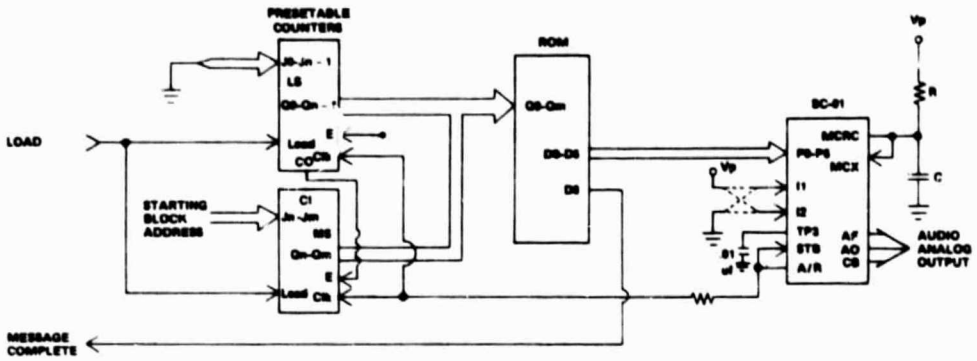

Figure 9. Multiple Message, Fixed Block Size

Class B Amplifier: See Figure 12. A current source (CB) is required for this push-pull amplifier.

NOTE

Minimum power is consumed when speech is inactive. When Vp = +12.0 volts and R_s = 40 ohms, the bias current drain is approximately 3.5 milliamps.

Controlling Audio Output Power: See Figure 13. A resistor or potentiometer from the speaker to ground can be used to control the audio output power.

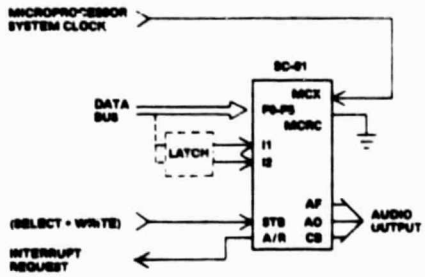

Figure 10. Multiple Message, Variable Block Size

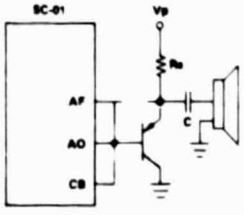

Figure 11. Class A Amplifier

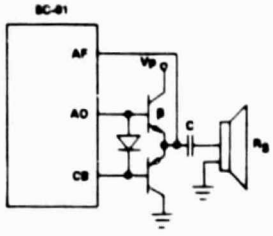

Figure 12. Class B Amplifier*

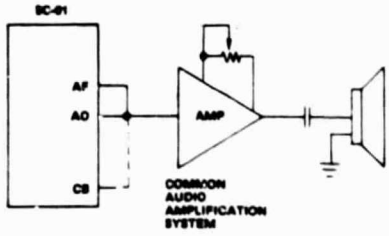

Figure 13. Controlling Audio Output Power

*For Class B Amplifier: (β) x (R_s min.) = 81.6 x (Vp) where β is beta or current gain of transistor. The AO line is protected by an internal series current limiting resistor of 90 ohms maximum. If more current is required of the SC-01, then the above formula indicates distortion will occur.

Table 4. Analog Output Specifications

CHARACTERISTIC	MIN	MAX	UNIT
Output Voltage (AH Phoneme)	18 x Vp	26 x Vp	Vp-p
Output Bias Current ** (1.6V< CB< Vp)	3.5	7.3	mA

ELECTRICAL CHARACTERISTICS: T_o = 0 to 70°C, Vp = 7 to 14 V_{DC}

CHARACTERISTIC		MIN	TYP	MAX	UNIT
Digital Input Impedance		1 meg			Ohm
Input Capacitance (P_1, STB)				3	pf
Input Capacitance (I1, I2, MCX)				8	pf
Digital Input Logic "0" (except I1, I2, MCX)		V_G - 0.5		V_G - 0.8	V_{DC}
Digital Input Logic "0" (MCX)				V_G - 1.0	V_{DC}
Digital Input Logic "0" (I1, I2)				2 x Vp	V_{DC}
Digital Input Logic "1" (except I1, I2, MCX)		V_G + 4.0		Vp - 0.5	V_{DC}
Digital Input Logic "1" (I1, I2)		8 x Vp			V_{DC}
Digital Input Logic "1" (MCX)		4.6			V_{DC}
Digital Output Logic "0" (I sink = 0.8mA)				V_G +0.5	V_{DC}
Digital Output Logic "1" (I source = 0.5mA)		Vp-0.5			V_{DC}
Power Supply Current	Vp = 9V		9.1		mA
	Vp = 9V**		11	18	mA
	Vp = 14V**		18	27	mA
*Master Clock Frequency			720K		Hz
MCX Input Duty Cycle		60-40		40-60	%
Master Clock Resistor Value (MCRC)***		6.5k			Ohm
Master Clock Capacitor Value (MCRC)***				300	pf

**Variable*

***With CB, AF, AO connected for Class B audio amplifier (see APPLICATION NOTES)*

****Frequency of Master Clock* ≃ 1.25 / RC

Note: TP1, TP2 must be left open for normal operation.

Table 5 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS *

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	Vp	20	V_{DC}
Power Dissipation at 25°C	P_{DM}	650	mW
Derating Above 25°C		5	mW °C
Operating Ambient Temperature	T_o	0 to 70	C
Storage Temperature	T_{STG}	−55 to 125	°C
Input Voltage	V_{INM}	−0.5 to Vp+0.5	V_{DC}
DC Current Max. Above Vp+0.5V	I_{INM}	1.0	ma
Lead Temperature (soldering 10 sec.)	T_L	300	°C

* *Operation above these limits could damage the device.*

NORMAL OPERATING CONDITIONS $7v \leq Vp \leq 14v$, $0°C \leq T_o \leq 70°C$

Votrax

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EL display unit specifications

For EL display, the EL graphic display unit (S-1021A) and EL message display unit (S-1050) are available.

Display specifications

	EL graphic display unit (S-1021A)	EL message display unit (S-1050)
Effective display area	60mm (L) × 120mm (W)	44.8mm (L) × 179.2mm (W)
Number of matrix electrodes	240 horizontal electrodes × 320 vertical electrodes	128 horizontal electrodes × 512 vertical electrodes
Number of picture elements	76,800 (240 × 320)	65,536 (128 × 512)
Picture element size	0.225mm (L) × 0.275mm (W)	0.20mm (L) × 0.25mm (W)
Picture element pitch	0.375mm (common to lengthwise and widthwise)	0.35mm (common to lengthwise and widthwise)
Display color	Orange-yellow (peak wavelength 5850Å)	Orange-yellow (peak wavelength 5850Å)
Brightness*	25 f-L (without filter)	30 f-L (without filter)
Viewing angle	More than 120°	More than 120°

*The brightness value achieved at standard frame frequency.

Operating specifications

	EL graphic display unit (S-1021A)	EL message display unit (S-1050)
Standard frame frequency	60Hz	70Hz
Frame frequency range	50—65Hz	50—82Hz
Input signal level	LS TTL level	LS TTL level
Power consumption**	7.5W (min.)—14.5W (max.)	5W (min.)—8.5W (max.)

**When operated at the standard frame frequency, power consumption varies according to display between the listed minimum and maximum values.

Ambient temperatures

Operating temperature	0—50°C	Storage temperature	−20—70°C

Dimensions and weight

	EL graphic display unit (S-1021A)	EL message display unit (S-1050)
Outline dimensions	166mm (W) × 166mm (L) × 39mm (D)	256mm (W) × 122mm (L) × 39mm (D)
Weight	Approx. 1.2kg	Approx. 1.2kg

Optional devices

A power supply unit and two different interface circuit boards for microcomputer use are available for convenient incorporation of EL display unit.

Interface circuit boards

An interface circuit board for full graphic display (S-1026F) is available, as well as an interface circuit board for coded graphic displays (S-1026C).

Function and circuit configuration

	Interface circuit board for coded graphic display (S-1026C)	Interface circuit board for full graphic display (S-1026F)
Function	1. Generation of four signals required for EL display unit 2. Write and read of display data 3. Scroll control 4. Reversal display control 5. Cursor control	1. Generation of four signals required for EL display unit 2. Write and read of display data 3. Scroll control 4. Reversal display control
Circuit configuration	CRT controller, buffer RAM (2K × 8 bits) for code memory, pattern generator (EPROM 2K × 8 bits), oscillator circuit, counter, multiplexer, I/O buffer circuit, I/O counter circuit, CRTC initializing circuit, P/S converter circuit	Counter timer circuit (CTC), buffer RAM (16K × 8 bits) oscillator circuit, counter, multiplexer, data latch circuit, address latch circuit, timing control circuit, P/S converter circuit, CTC initializing circuit

Power supply unit (S-1040)

Input requirements: single-phase, 50/60Hz, 90—127VAC

Output requirements:

Parameter	+5V	+30V	+200V
Variable voltage range	Fixed	Fixed	185—215V
Rated current	0.4A—1.2A	0—0.4A	8mA—25mA
Constant voltage accuracy	±3%	±3%	±3%
Ripple noise	50mVp-p or less	600mVp-p or less	2Vp-p or less

This unit can be applied to both EL display units, S-1021A and S-1050

*Design and specifications subject to change without notice.

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THE INTEL BUBBLE STORAGE 1981 SEMINAR

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INTRODUCED
THE WORLD'S FIRST
MILLION-BIT
BUBBLE MEMORY
AND A COMPLETE
SYSTEM SOLUTION

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IN 1980 INTEL MAGNETICS SHIPPED THOUSANDS OF BUBBLE MEMORY KITS AND BOARDS FOR PROTOTYPING AND PRODUCTION IN APPLICATIONS SUCH AS

- NUMERICAL CONTROL MACHINE TOOLS
- PROCESS CONTROL
- AIRCRAFT NAVIGATION
- CABLE TELEVISION

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IN 1981 MEGABIT BUBBLE MEMORIES WILL BE DESIGNED INTO

- ROBOTICS
- OIL EXPLORATION
- PORTABLE INSTRUMENTS
- TELECOMMUNICATIONS
- POINT OF SALE TERMINALS
- WORD PROCESSORS
- MILITARY COMMUNICATIONS

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THE MEGABIT BUBBLE MEMORY IS

- ✓ COMPACT
- ✓ SOLID STATE
- ✓ NON VOLATILE
- ✓ SILENT
- ✓ LOW POWER
- ✓ RELIABLE IN HARSH ENVIRONMENT

AND THE SUPPORT CIRCUITS ARE DESIGNED FOR EASY INTERFACING WITH MICROPROCESSORS.

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THE MEGABIT BUBBLE MEMORY INTRODUCED BY INTEL IN 1979 IS NOW A MATURE PRODUCT.

IT IS THE NATURAL MASS STORAGE FOR LSI MICROPROCESSOR BASED SYSTEMS.

BUBBLE STORAGE CAN BE DESIGNED INTO YOUR PRODUCTS NOW, MEETING THE CHALLENGES OF THE MARKETS OF THE 1980'S.

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WITH BUBBLE STORAGE YOUR NEW PRODUCT GAINS A COMPETITIVE EDGE BY:

- OFFERING IMPROVED RELIABILITY
- REQUIRING LESS MAINTENANCE
- PROVIDING SPECIAL FEATURES
- ELIMINATING BATTERY BACKUP
- REDUCING SIZE AND WEIGHT
- INCREASING FLEXIBILITY IN HARSH ENVIRONMENTS—
  - TEMPERATURE RANGE
  - AIR POLLUTION
  - VIBRATION

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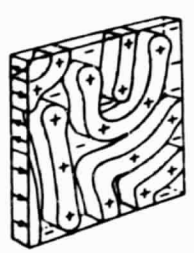
INTEL MAGNETICS IS MAKING BUBBLE MEMORIES EASY TO USE RELIABLE LOW IN COST.

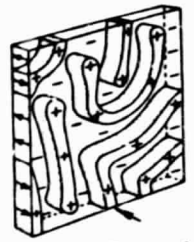
TODAY WE WILL LOOK AT

- HOW BUBBLE MEMORIES WORK
- CHARACTERISTICS OF THE 7110 MEGABIT BUBBLE MEMORY
- HOW THE MEGABIT SYSTEM WORKS
- EXPANSION TO MULTI-MEGABYTE SYSTEMS
- TODAY'S PRODUCTS
- RELIABILITY RESULTS
- COST TRENDS
- COMPARISONS WITH OTHER TECHNOLOGIES
- FUTURE PRODUCTS

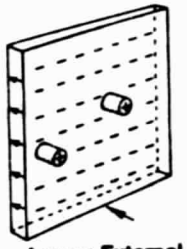
HOW BUBBLE MEMORIES WORK



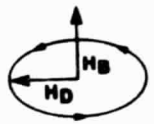
No External Magnetic Field

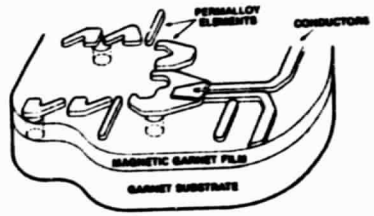


Small External Magnetic Field

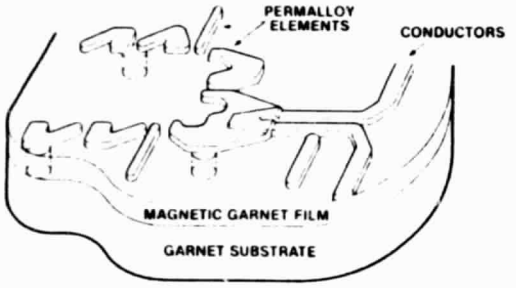


Larger External Magnetic Field

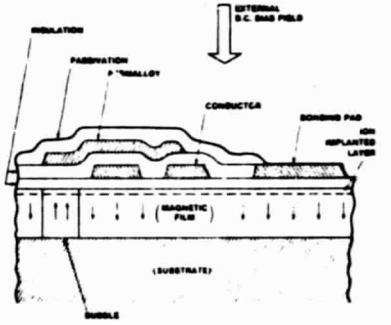


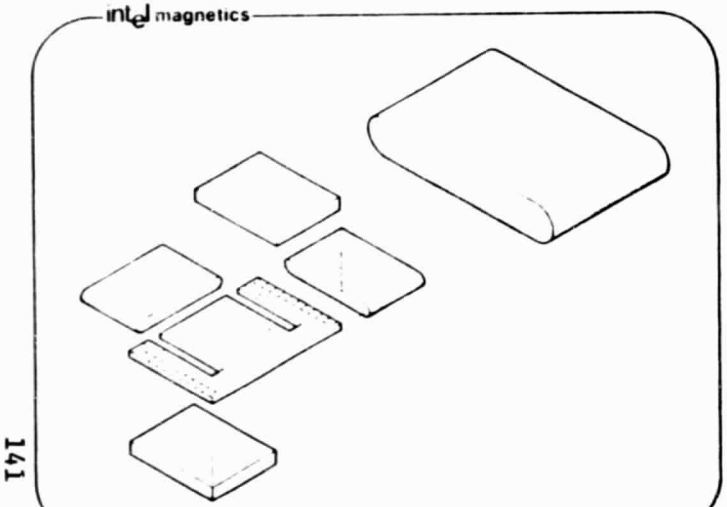


Field Access Propagation by Chevron



Field Access Bubble Memory Chip





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CHARACTERISTICS OF THE INTEL MAGNETICS 7110 1 MEGABIT BUBBLE MEMORY

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INTEL MAGNETICS 7110
1 MEGABIT BUBBLE MEMORY

- 1,048,576 BITS OF USABLE DATA STORAGE
- 1,310,720 BITS OF GROSS CAPACITY
- BINARY ORGANIZATION
  - 512 BIT PAGE AND 2048 PAGES
- SERIAL-PARALLEL-SERIAL
  - 256 DATA LOOPS EACH CONTAINING 4096 BITS PER LOOP
  - SEPARATE READ AND WRITE TRACKS

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IM'S 7110 MBM CHARACTERISTICS

- ONE MEGABIT BINARY DEVICE
- PAGE LENGTH 512 BITS
  - 2048 PAGES
- TOTAL OF 320 LOOPS WITH 4096 BITS/LOOP
  - 256 DATA LOOPS
  - 16 ERROR CODE LOOPS
  - 48 REDUNDANT LOOPS
- BLOCK REPLICATE FOR READ AND BLOCK SWAP FOR WRITE
- BOOTLOOP FOR LOOP MAP AND INDEX ADDRESS; HAS SEPARATE REPLICATE AND SWAP PINS
- X2 I/O STRUCTURE
- SINGLE CHIP DUAL IN-LINE LEADLESS PACKAGE AND SOCKET

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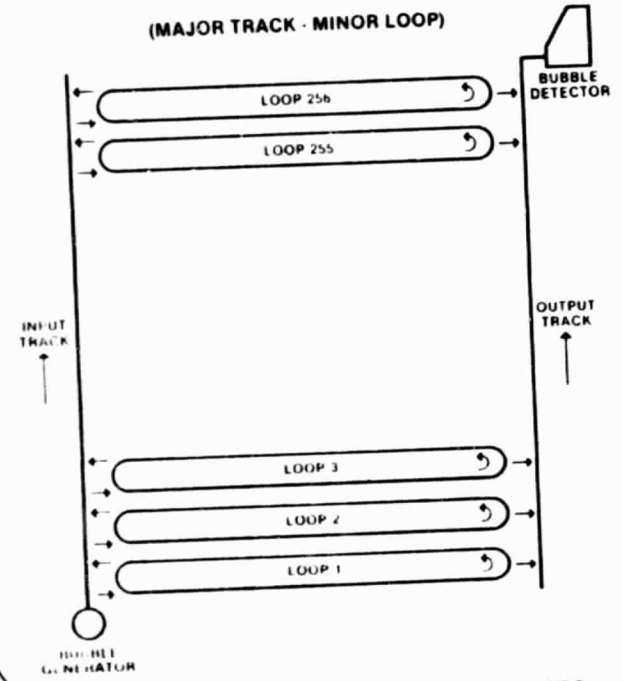
BASIC BUBBLE MEMORY SERIAL IN - PARALLEL LOOPS - SERIAL OUT ORGANIZATION

(MAJOR TRACK - MINOR LOOP)



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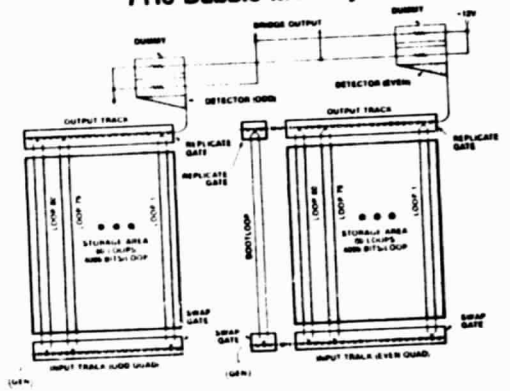
Architecture of 7110 Bubble Memory



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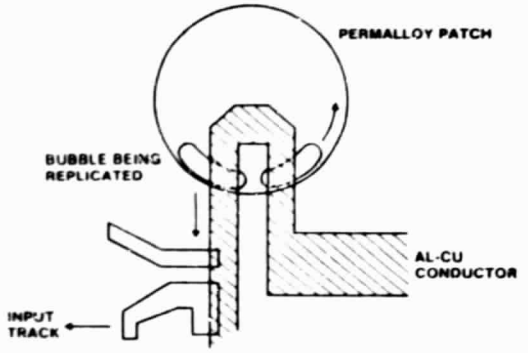
REPLICATING GENERATOR



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Magnetic Bubble Device Tradeoffs

0°-70° (Ambient) vs Rotating Field Frequency

+12V (only) vs Loop Length

Replication Generator — Free

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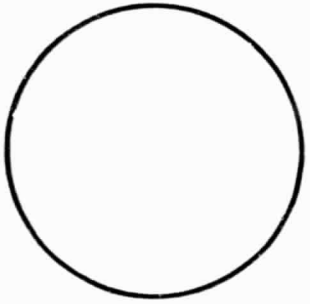
THE 3 INCH DIAMETER WAFER



ENABLED INTEL MAGNETICS TO GET EARLY START ON 1M PRODUCTION BECAUSE:

- EACH 2 SQ CM CHIP HAS MANUFACTURABLE TOLERANCES
- A 15% SPARE LOOP ALLOWANCE WAS CHOSEN TO MAXIMIZE PRODUCTION YIELD
- WE HAVE 12 FULL-SIZED MEGABIT CHIPS.

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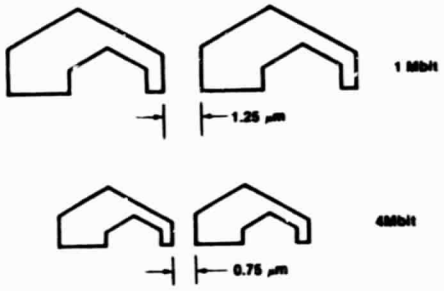

- X-Ray Lithography
- Contact Printing
- High Performance Stepper

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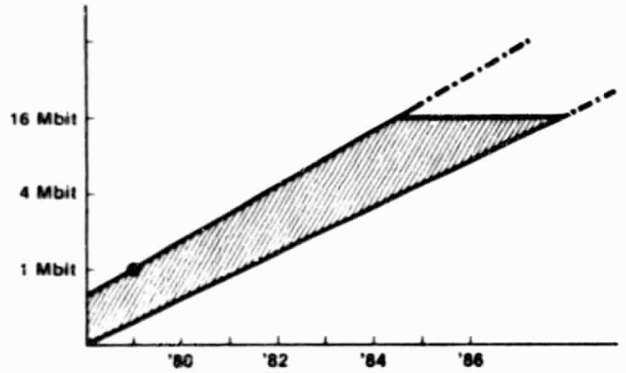
FUTURE TRENDS



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IM'S MBM PERFORMANCE CHARACTERISTICS

	7110	UNITS
ROTATING FIELD RATE	50	KHz
MAXIMUM DATA RATE	100	KBITS/SEC
AVERAGE DATA RATE	68	KBITS/SEC
AVERAGE ACCESS TIME $\frac{4096}{2} \times \frac{1}{\text{FIELD RATE}}$	40	MS

- ☐ SINGLE POWER SUPPLY +12 VOLTS
- ☐ POWER DISSIPATION

2.5W Max.
1.9W Typ.

100% DUTY CYCLE

7110 FAMILY

7110	0°-50°C AMBIENT
7110-1	0°-70°C AMBIENT
7110-2	10°-50°C AMBIENT

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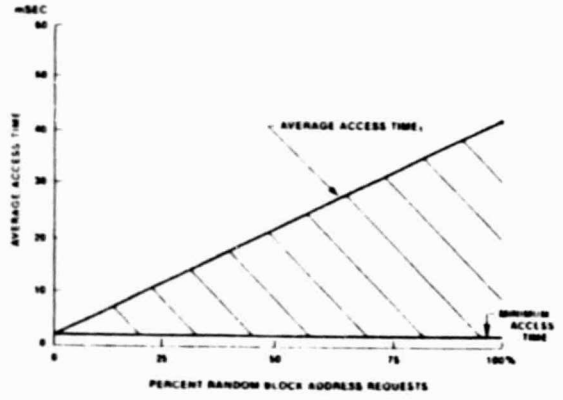
AVERAGE ACCESS TIME
VS.
PERCENT OF RANDOM BLOCK ADDRESS REQUESTS



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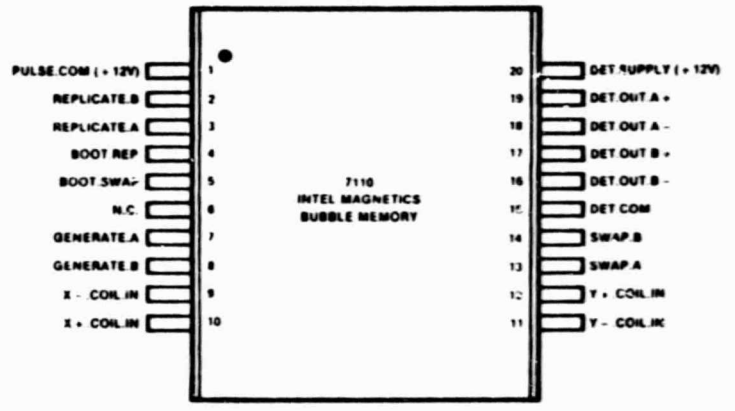
IM'S 7110 PINOUT



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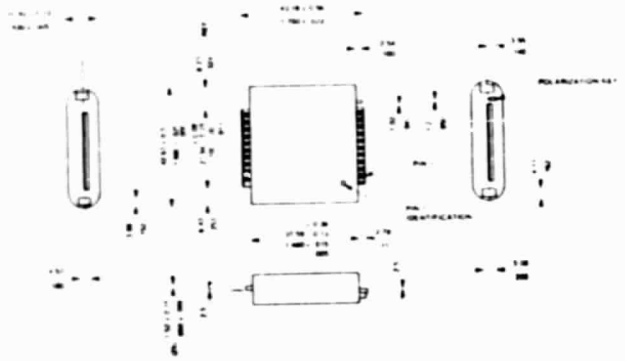
IM'S 7110 LEADLESS PACKAGE OUTLINE



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HOW THE INTEL MEGABIT BUBBLE STORAGE SYSTEM WORKS

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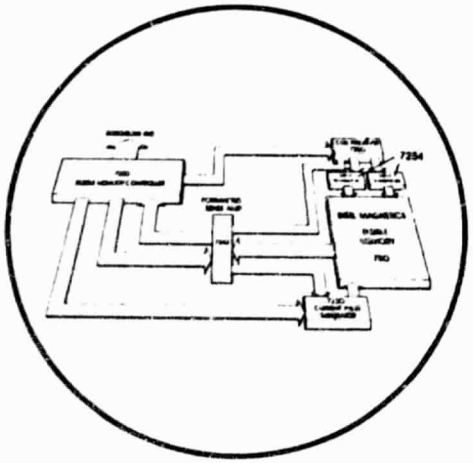
NOT JUST A BUBBLE MEMORY



BUT A SYSTEM

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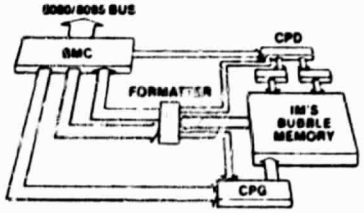
128K BYTE MINIMUM BUBBLE MEMORY SYSTEM BLOCK DIAGRAM



- 7110 1 MEGABIT MAGNETIC BUBBLE MEMORY (MBM); 20-PIN; 12V
- 7230 CURRENT PULSE GENERATOR (CPG) BIPOLAR; 22-PIN; 5 & 12V
- 7250 COIL PRE-DRIVER (CPD); CMOS; 16-PIN; 12V
- 7254 QUAD VMOS TRANSISTOR PACK; 14-PIN; 12V
- 7242 DUAL FORMATTER/SENSE AMPS (FSA); NMOS; 20-PIN; 5 & 12V
- 7220 BUBBLE MEMORY CONTROLLER (BMC); HMOS; 40-PIN; 5V
  - EXPANDABLE — ONE BMC CAN CONTROL EIGHT MBMs, RESULTING IN A 1 MEGABYTE SYSTEM

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FEATURES OF IM'S BUBBLE MEMORY SYSTEM

- COMPLETE SET OF SUPPORT CIRCUITS FOR EASE OF USE
- ADVANCED LSI TO MINIMIZE SYSTEM PART COUNT
- TRANSPARENT REDUNDANCY
- AUTOMATIC ERROR CORRECTION
- STANDARD BUS INTERFACE (8080/8085/8088/8086)
- EASY PARALLELING OR MULTIPLEXING OF UP TO EIGHT MBMs WITH ONE CONTROLLER
- DMA HANDSHAKE CAPABILITY
- SINGLE OR MULTIPLE PAGE BLOCK TRANSFERS
- SENSE AMPLIFIERS INTEGRATED INTO FORMATTER
- POWER FAIL RESET FOR MAXIMUM PROTECTION OF BUBBLE MEMORY
- SMALL PHYSICAL VOLUME

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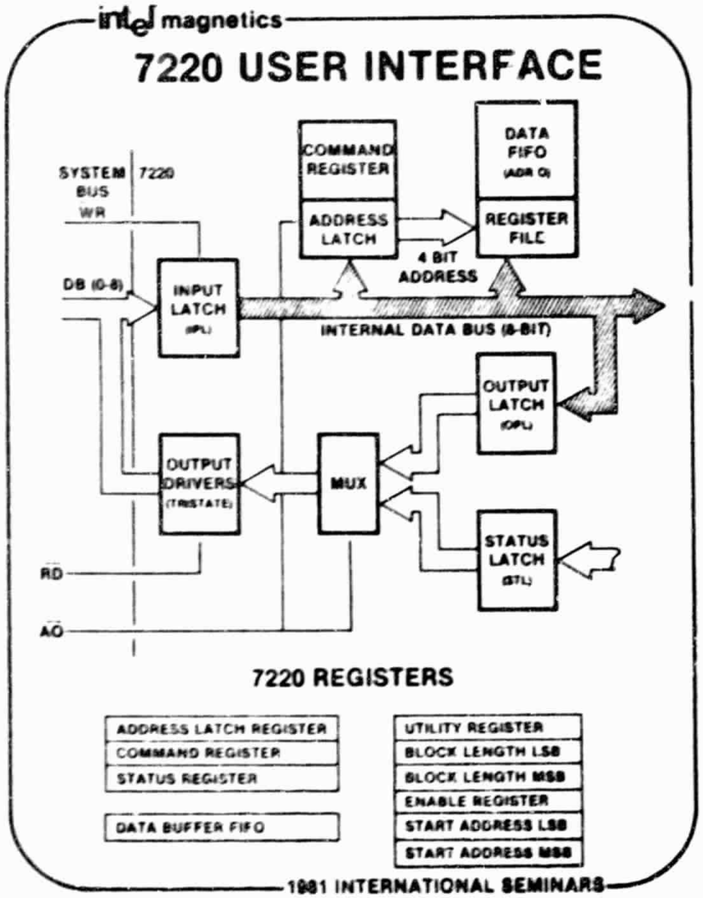
IM'S BUBBLE MEMORY MINIMUM SYSTEM

- 128K BYTES OF NON-VOLATILE STORAGE CAPACITY
- ONE EACH
  - 7110 MBM, TWO EACH QUAD TRANSISTOR PACK
  - 7230 CPG
  - 7242 FSA
  - 7250 CPD
  - 7220 BMC
- MAX DATA RATE 100K BITS/SEC
- AVG DATA RATE 68K BITS/SEC
- AVG ACCESS TIME 40 MSEC
- POWER SUPPLIES +12, +5 VOLTS ONLY
- POWER DISSIPATION 5.0 WATTS
- PHYSICAL SIZE 15 SQ. INCHES
- TRANSPARENT REDUNDANCY
- AUTOMATIC ERROR CORRECTION
- STANDARD BUS INTERFACE (8080/8085/8088/8086)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7220 USER INTERFACE
SYSTEM BUS
7220
WR
DB (0-8)
INPUT LATCH (IPL)
COMMAND REGISTER
ADDRESS LATCH
4 BIT ADDRESS
DATA FIFO (ADR 0)
REGISTER FILE
INTERNAL DATA BUS (8-BIT)
OUTPUT LATCH (OPL)
STATUS LATCH (STL)
MUX
OUTPUT DRIVERS (TRISTATE)
RD
A0
7220 REGISTERS
ADDRESS LATCH REGISTER
COMMAND REGISTER
STATUS REGISTER
DATA BUFFER FIFO
UTILITY REGISTER
BLOCK LENGTH LSB
BLOCK LENGTH MSB
ENABLE REGISTER
START ADDRESS LSB
START ADDRESS MSB
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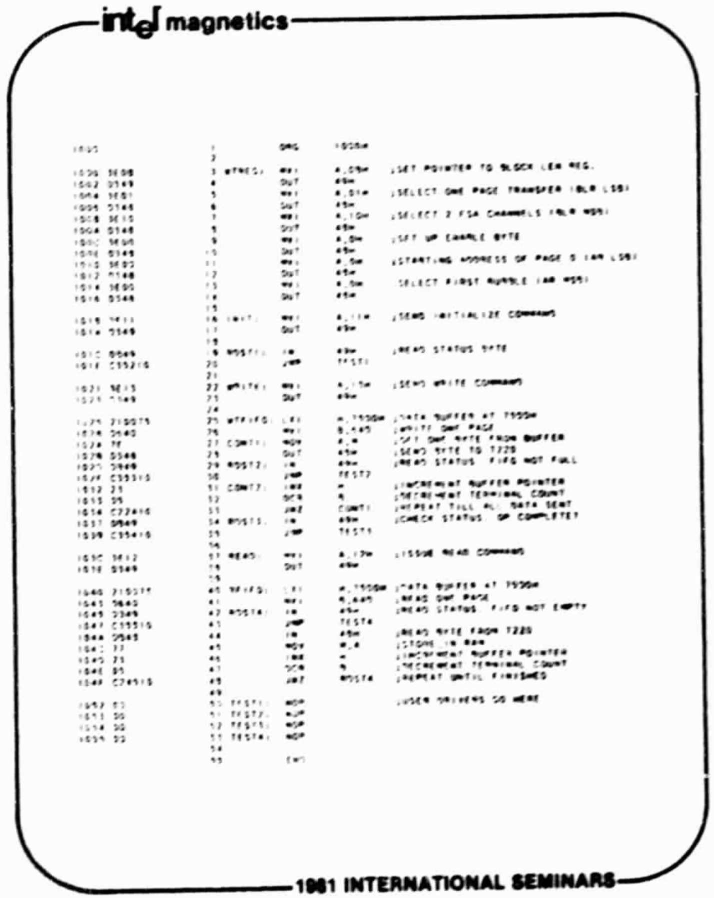
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EXPANSION TO MULTI-MEGABYTE SYSTEMS

1 MEGABYTE SYSTEM

- 1,024K x 8 NON-VOLATILE MASS STORAGE
- ONE BUBBLE MEMORY CONTROLLER (BMC) CONTROLLING EIGHT BURBLE MEMORY CELLS
- EACH CELL CONTAINS 1 EACH 7242, 7250, 7230, 7110, TWO 7254s
- PERFORMANCE
  - — 68K BYTES AVG DATA RATE
  - — 40 MSEC AVG ACCESS TIME
- TRANSPARENT REDUNDANCY
- AUTOMATIC ERROR CORRECTION
- PHYSICAL SIZE 90 SQ. INCHES (580 SQ. CM.)

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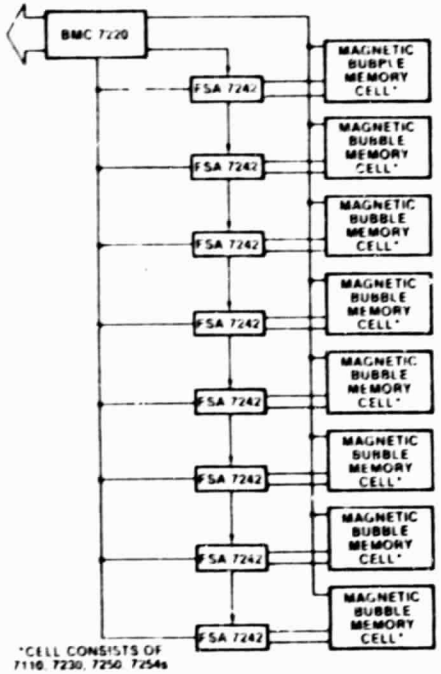
1 MEGABYTE BUBBLE MEMORY SYSTEM



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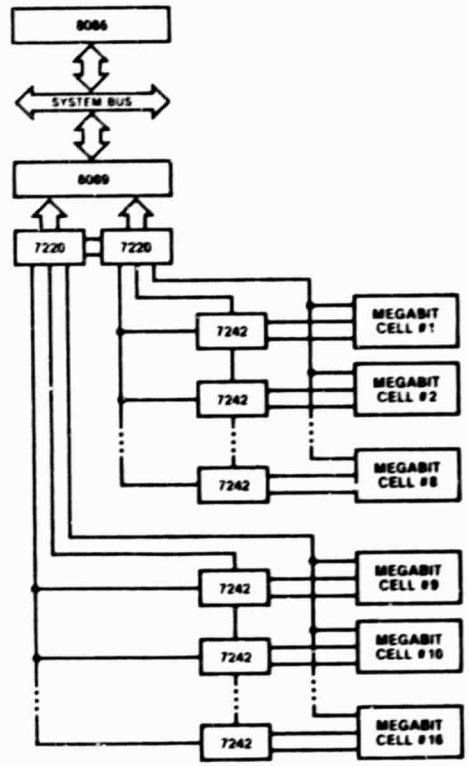
1024K x 16-BIT BUBBLE MEMORY SYSTEM



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Bubble Memory System Power Requirements (absolute maximums)

128K Bytes — 6.2 Watts

1 Megabyte — 45 Watts

Bubble Memory Power Requirements

Configuration		Capacity	Power (watts)		
BPK-72	BPK-72	(bytes)	+12V	+5V	Total
1	0	128K	4.72	1.43	6.15
1	1	256K	9.44	2.26	11.70
1	2	384K	14.16	3.09	17.25
1	3	512K	18.88	3.92	22.80
1	4	640K	23.60	4.75	28.35
1	5	768K	28.32	5.58	33.90
1	6	896K	33.04	6.41	39.45
1	7	1024K	37.76	7.24	45.00
Breakdown by Device					
		7110	1.740	—	1.740
		7220	—	0.600	0.600
		7230	0.420	0.225	0.645
		7242	0.360	0.600	0.960
		7250	0.900	—	0.900
		7254 (2)	1.300	—	1.300
			4.720	1.425	6.145

Data Organization — Small 8 Bit Systems

#16 Bit MBM's	# Pages	Bytes/Page	Data Rate (K Byte/Sec.) Burst	Average
1	2048	64	12.5	6.5
2	2048	128	25	17
2	4096	64	12.5	6.5
4	2048	256	50	34
4	4096	128	25	17
4	8192	64	12.5	6.5
8	2048	512	100	68
8	4096	256	50	34
8	8192	128	25	17
8	16384	64	12.5	6.5

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TODAY'S RANGE OF BUBBLE STORAGE PRODUCTS FROM INTEL

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Design Approach for High Data Rates

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PRODUCT RANGE

- BPK 72 — KIT OF PARTS TO BUILD UP TO 128K BYTE SYSTEM INCLUDES. BUBBLE MEMORY CELL AND 7220 CONTROLLER AND P.C.B. WITH FULL DOCUMENTATION.
- BPK 70 — KIT OF PARTS TO BUILD BASIC MEMORY CELL FOR PRODUCTION USE. DOES NOT INCLUDE 7220 PCB OR DOCUMENTATION.

TEMP RANGES
- 0 — 0°C to +50°C
- 1 — 0°C to +70°C
- 2 — +10°C to +50°C
- 3 — +10°C to +35°C

- D 7220 — BUBBLE-MEMORY CONTROLLER AVAILABLE SEPARATELY FOR PRODUCTION USE WITH MULTIPLE BPK 70.
- SBC 254 — OEM BOARD WITH UP TO 512K BYTE CAPACITY. MULTIBUS COMPATIBLE
  - 1 = 128K BYTE
  - 2 = 256K BYTE
  - 4 = 512K BYTE

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BUBBLE PROTOTYPE KIT BPK72

PROTOTYPE KIT CONSISTS OF:

- ☐ ONE EACH
  - 7110 MBM
  - 7220 BMC
  - 7230 CPG
  - 7242 FSA
  - 7250 CPD
- ☐ TWO EACH 7254 VMOS DRIVERS
- ☐ 4" x 4" PRINTED CIRCUIT BOARD
- ☐ DOCUMENTATION
  - USER'S MANUAL
  - BUBBLE MEMORY DESIGN HANDBOOK
- ☐ SPECIAL TOOLS FOR INITIAL ASSEMBLY, CHECK-OUT AND DEBUG

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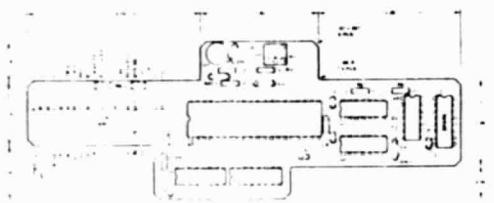
PRELIMINARY

7220BRD
BUBBLE MEMORY CONTROLLER

- 8080/8085/8088/8086 Microprocessor Interface
- Interfaces Up to Eight BPK70 Bubble Storage Subsystems
- Self-Contained Timing
- DMA Handshake Capability
- Single or Multiple Page Block Transfers
- Plug Directly Into a Standard 40-Pin Dual In-Line Socket



INTRODUCING iSBC 254™ BOARD

- 1, 2 or 4 1M Bit Bubbles
- 128KB, 256KB, or 512KB Capacity
- Multibus Compatibility
- Supported Under
  RMX 80 and RMX 86
  Real Time, Multitasking
  Operating Systems
- Operates in DMA, Interrupt, or Polled Modes

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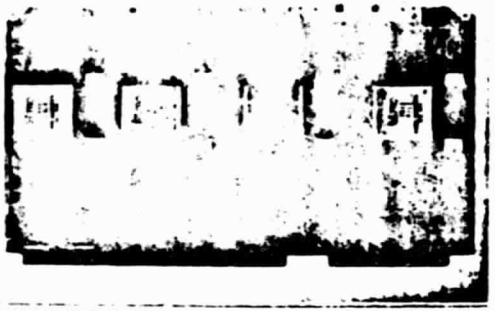
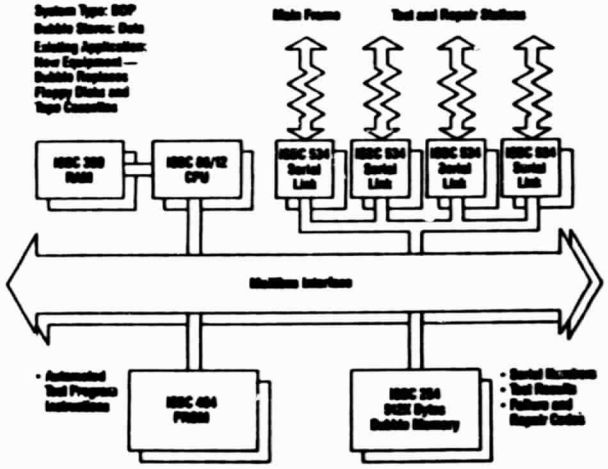
PRELIMINARY

iSBC 254™
BUBBLE MEMORY BOARD

- Capacity up to 512K Bytes of Bubble Memory Storage
- Automatic Error Correction
- Operates from Standard 5V and 12V Power Supplies
- High-Density Storage
- DMA Capability
- Non-Volatile Storage
- Average Access Time of 40ms
- Burst Data Rate up to 80K Bytes per Second
- Software Compatible with the iRMX™ Operating System
- Powerfail Data Protection
- Low Power Consumption (32 Watts per ½ Megabyte)



ON THE PRODUCTION FLOOR



TEST EQUIPMENT

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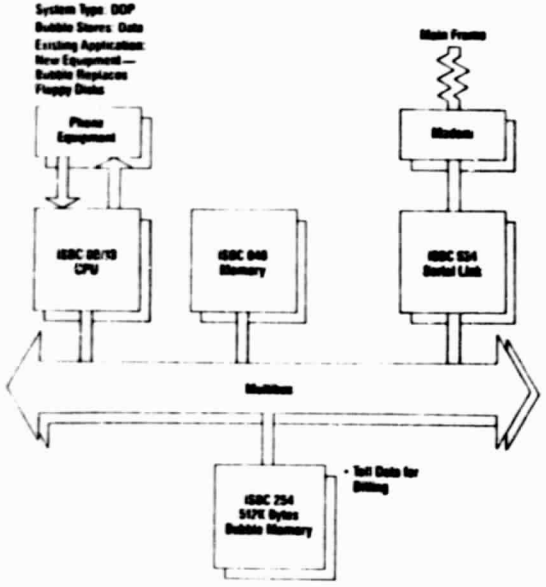
IN COMMUNICATIONS NETWORKS



TELECOMMUNICATIONS

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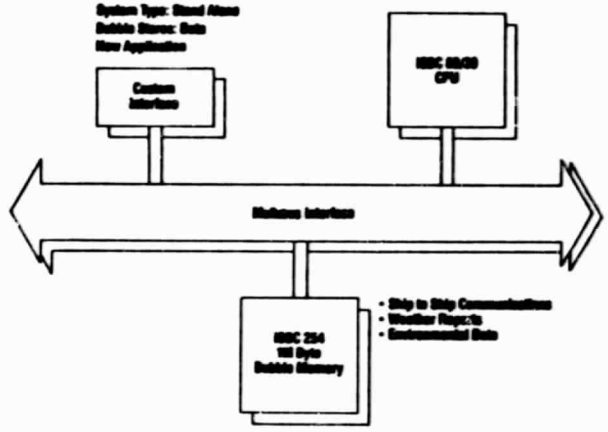
IN THE NAVY



SHIPBOARD SYSTEM

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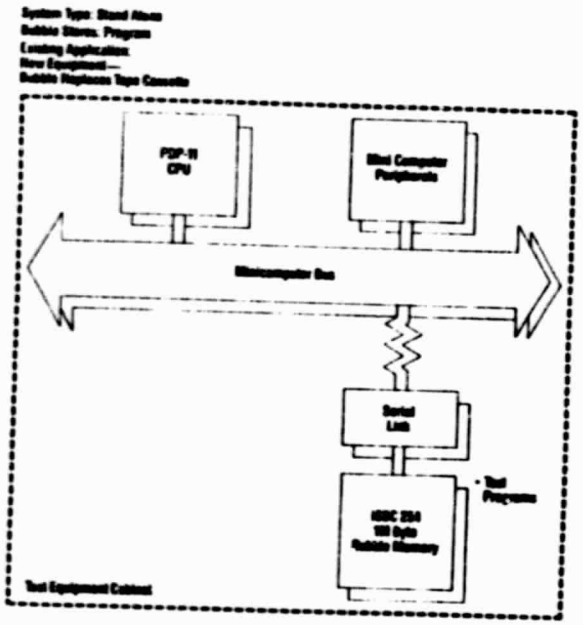
FOR FIGHTER PLANE CHECKOUT



TEST SYSTEMS

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RELIABILITY RESULTS

ENVIRONMENTAL LIMITS
ERROR RATES
FAILURE RATES

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Environmental Test Summary

Test	Conditions	Results
Steam 85°C/85% RH	15 PSI, 125°C Pins Unbiased Pins Biased, No Current Flowing Pins Biased, 0.3 W Dissipating	MTTF > 100 Hours MTTF > 1000 Hours > 1000 Hours > 5000 Hours
Bake	150°C, 168 Hours	No Failures
Temperature Cycle	-65°C to +150°C 10 Cycles 100 Cycles	15% Failures* No Further Failures
Shock	200 g, 3 Axes	No Failures
Vibration – Non-Operating – Operating	2 Hz-2 KHz, 20 g, 3 Axes 2 Hz-2 KHz, 3 Axes	No Failures *Mean Failure Point >20 g

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Environmental Limits of the 7110 One Megabit Bubble Memory

Ambient Operating Temperature:	0° → 70°C
Nonvolatile Storage Temperature	−40° → +100°C
External Magnetic Field	20 Oersteds
Non-Operating Handling Shock	200 G
Operating Vibration:	20 G
Humidity	85°C/85%, MTTF > 1 Khr

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Magnetic Field

- 20 OE. Any direction has no effect on error rate.
- Typical Magnetic Fields

⅛" From Ringing Telephone Earpiece	12 OE.
½" From Large Printer Motor	12 OE.
¼" From Power Bus Bar	2 OE.

intel magnetics

Electromagnetic Susceptibility

- Simulate Noisy Environment by
  - 7 KV Discharge on System Chassis
  - Operate Power Equipment (drill, motors, lamp starter, printer cable) within ½" of 7110

No measurable effect on error rate even at extremes of Voltage Operating Margins.

intel magnetics

Power Loss

- To Protect Data, Shutdown is initiated if

  $V_{CC} < 4.6\,V$
  $V_{DD} < 11.2\,V$

- Power Loss Simulated by

  Removing Power to System Chassis
  Pulling Bubble Card out of Chassis

- Many systems have been thru several hundred power loss cycles with perfect data retention.

intel magnetics

Data Storage Reliability

- 4096 Bit Loops
  - 256 Data
  - 48 Redundant
  - 14 Error Code
- Determine defective loops then use extreme stress to add weak loops to redundancy maximum
- 50,000 device-hours of data storage at
  - −40°C
  - +150°C

  Sampled Parts have 9 months storage without error
- System power level sensing protects data against
  - Power Fail
  - Low Power Levels

1981 INTERNATIONAL SEMINARS

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LIFETESTING WITH THE iSBC 250 AND iSBC 254

- INITIALIZE 1,000 TIMES.
- WRITE RANDOM PATTERN FILLING ALL STORAGE LOOPS AND READ PATTERN 100 TIMES (TOTAL OF 10^9 READS).
- SWAP FULL MEMORY PATTERN AND REPEAT COMPLETE MEMORY READ.

ERRORS ARE LOGGED BY LOOP NUMBER, COUNT AND TYPE.

TO DATE – 3000 DEVICES HAVE BEEN LIFETESTED FOR OVER 300,000 TOTAL DEVICE-HOURS.

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7110 Bubble Memory Error Rate Evaluation

	Frequency of Occurrence/Bit Read	
	25°C Nominal Power Supplies	50°C, 0°C Worst Case Supplies
Isolated Single-Bit Read	10^{-9}	10^{-7} to 10^{-8}
Isolated Single-Bit Data	10^{-11}	10^{-9}
80% — Bubbles Lost 15% — Slippage 5% — Additional Bubbles		
Multiple Error Modes E.G. Stripe-Out	$<10^{-14}$	

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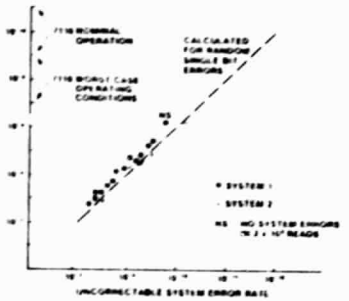
7110 Error Rate



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Projected Read Error Rates

	Read Error Rate		Time to Error	
	Before Correction	After Correction*	Before Correction	After Correction*
25°C Nominal Supplies	10^{-9}	10^{-16}	4 Hours	$>10^{3}$ Yrs.
0, 50°C Worse Case Power Supplies	$10^{-7} - 10^{-8}$	$10^{-12} - 10^{-14}$	2.5-25 Mins.	30 Weeks-60 Years

*Assumes that errors in Stored Data are corrected (by a rewrite of the block) immediately after their detection and not left to accumulate.

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Chip Metallurgy

- Bonding

  Thermosonic Au to AlCu, NiFe
  Bond pull and ageing at 200°C
  MTTF > 30 years (max temperature)

- Conductors

  Electromigration study on 10,000 lines
  Stressed temperature, duty factor, current density
  MTTF ~ 100 years (max temperature)

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Component	Estimated Failure Rate, 70°C % per 1000 Hours	Source of Data
7220	.02	RR 18
7242	.10	RR 19
7230	.005	Internal ELT Data
7254	.06	RR 2978 (vendor)
7250	.10	Internal ELT Data
7110	MTTF > 30 Years	RR22

Overall 1 Megabit System ~ 0.6% per 1000 Hours (70°C)
(Consistent with data from 300,000 system-hours of lifetesting).

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At 70°C We estimate the following Failure Rates (% per 1000 Hours) PER MEGABIT

7110 Bubble Memory System	0.6
Dynamic RAM	1.1
EPROM	4.0

Low Bubble System Failure Rate attributed to

- Minimum Part Count
- Use of 15% Redundancy on large 7110 chip

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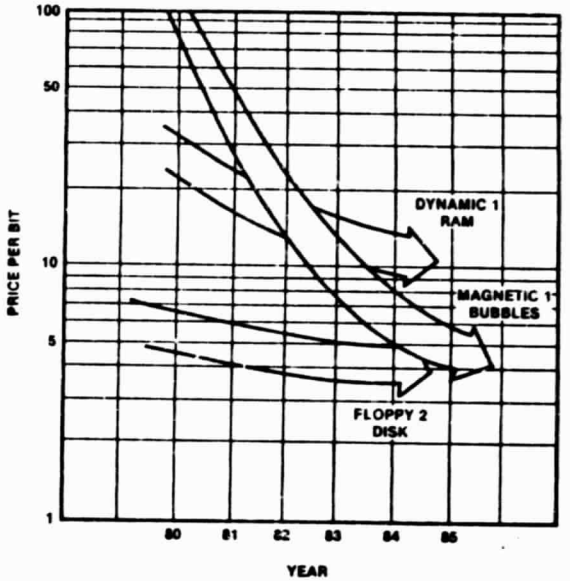
Summary

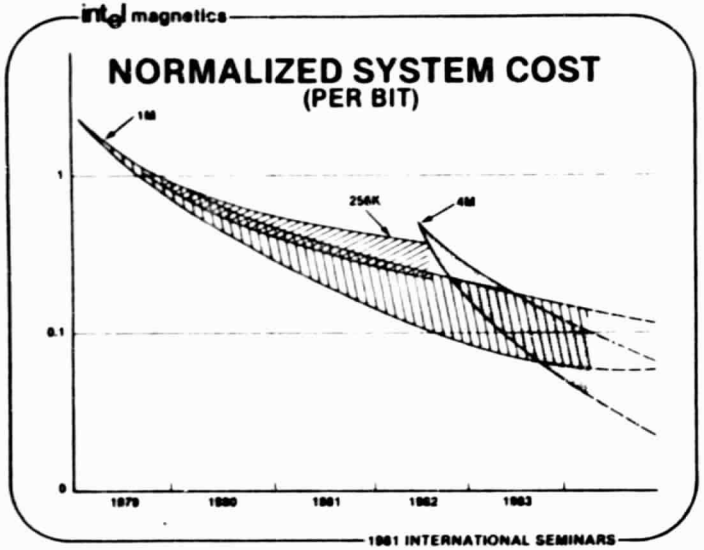
- Compared to Solid State Memory, Bubbles have
  - Equivalent system level error rate
  - Lower failure rate per megabit
  - Infinite non-volatility
- Compared to Magnetic Media, Bubbles have
  - Equivalent or better error rate
  - Durability in harsh environments
  - Low Maintenance

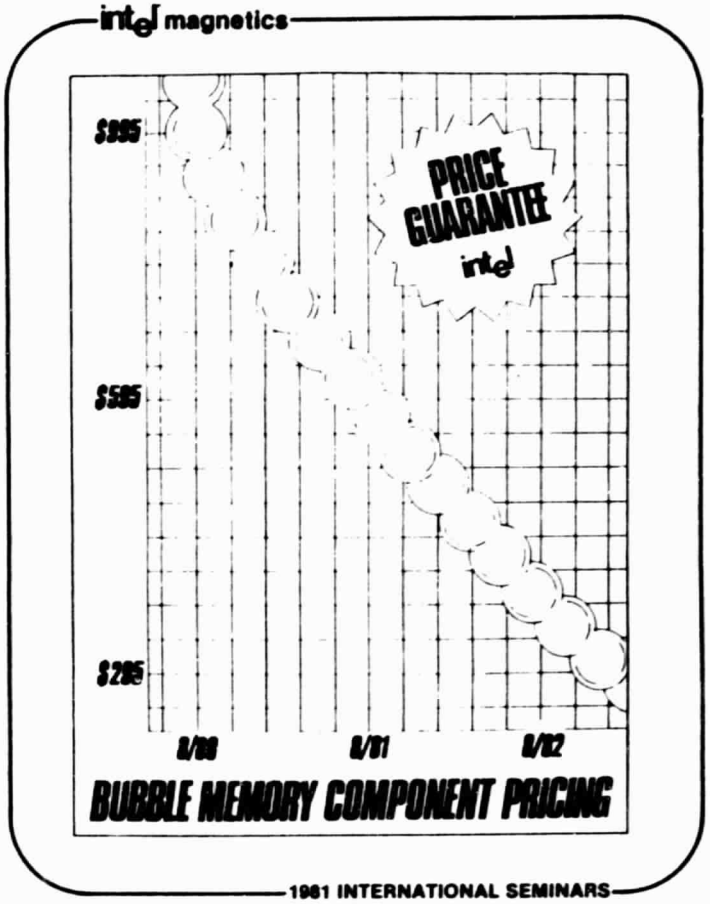
COST TRENDS

PRICE PER BIT OF MAGNETIC BUBBLE MEMORIES



1. PRICE PER BIT OF MEMORY DEVICE
2. PRICE PER BIT OF FLOPPY DISK DRIVE


intel magnetics
NORMALIZED SYSTEM COST
(PER BIT)
1M
256K
4M
1
0.1
0
1979
1980
1981
1982
1983
1981 INTERNATIONAL SEMINARS


intel magnetics
$995
$595
$295
PRICE
GUARANTEE
intel
1/80
1/81
1/82
BUBBLE MEMORY COMPONENT PRICING
1981 INTERNATIONAL SEMINARS

Bubble Price Break

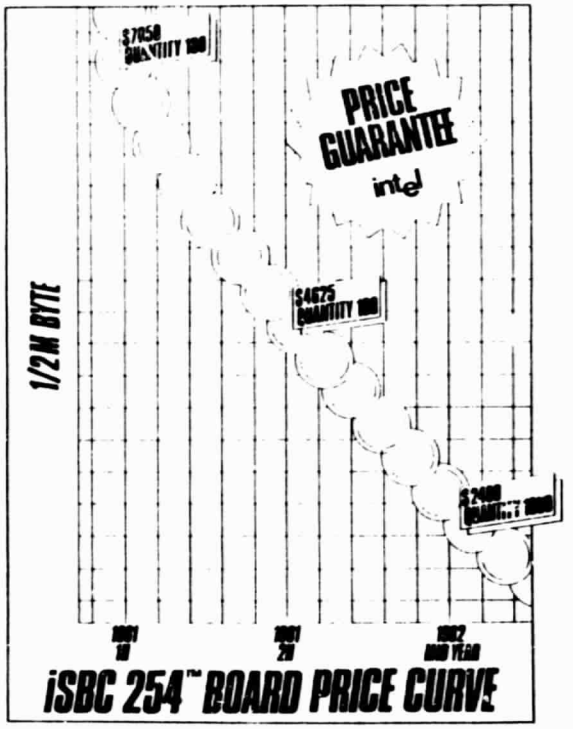
Intel reduces prototyping prices of 1-megabit bubble memories by 40% now. And guarantees a volume price of $595 for complete component sets by August 1981.

Add more value to your product

Start designing now

Get more than bubbles

intel delivers solutions.



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COST OF OWNERSHIP

A MANUFACTURER OF OFFICE EQUIPMENT AND FLOPPY DISKS IS SWITCHING TO BUBBLES BECAUSE:

256K BYTES OF FLOPPY DISKS COST $500 TO BUY AND $500 MORE TO REPAIR OVER A 5 YEAR PERIOD. THE MTBF IS ONLY 6 MONTHS. SERVICE CALLS ARE COSTLY AS PRODUCTS ARE PLACED IN REMOTE AREAS AND TRANSPORTATION COSTS INCREASE.

256K BYTES OF INTEL BUBBLE MEMORY COST $1000 TO BUY AND HAVE 14 YEAR MTBF AT 50°C. NO SERVICE CALLS.

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COMPARISONS WITH OTHER TECHNOLOGIES

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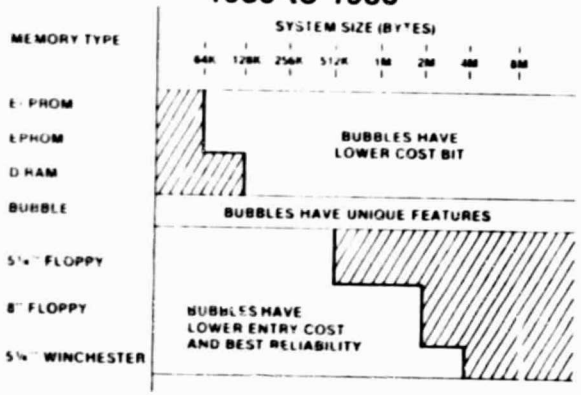
RECOMMENDED BUBBLE USAGE
1980 to 1983



1981 INTERNATIONAL SEMINARS

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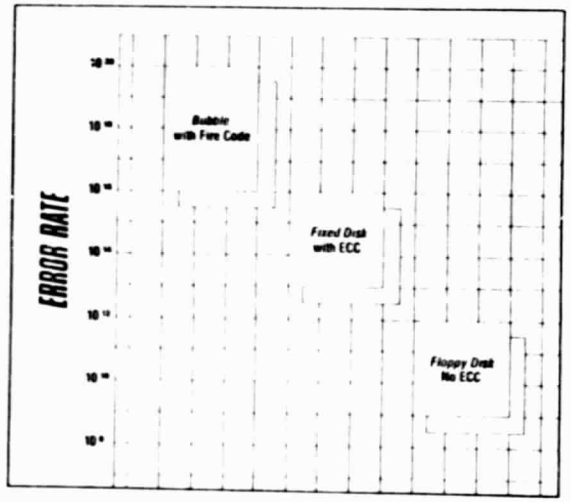
MASS STORAGE MEDIA COMPARISON

Media/Peripheral	Average[1] Access Time (MS)	Burst Transfer Rate (K Bytes/S)	Formatted Capacity (M Bytes)
Intel Bubble iSBC 254-4	48	50	5
5-IN Floppy Shugart SA-450	413	31	.35
8-IN Floppy Shugart SA-851	174	62	1.2
Microwinchester Shugart Technology ST-506 (5-IN)	193	625	5
Minwinchester IMI 7710 (8-IN)	58	648	10
Tape Cassette 3M DCD 3	several seconds	6	10

1 To First Byte

1981 INTERNATIONAL SEMINARS

ERROR RATE COMPARISON, BUBBLES VS. DISK TECHNOLOGY



DISKS VS BUBBLES

BUBBLES	DISKS
HARSH ENVIRONMENT	LARGE CAPACITY
RELIABILITY	LOW COST PER BIT USED
FAST ACCESS	
LOW ENTRY COST	

FLOPPY AND BUBBLE COMBINATION

ARCHIVAL CAPABILITY
EASY MAILING OF DATA
RELIABILITY
FAST ACCESS

FLOPPY DISKS OFFER LOW COST, "MAILABLE", EASILY ARCHIVED STORAGE.

BUBBLE MEMORIES OFFER SUPERIOR FIXED MEDIA BECAUSE OF IMPROVED RELIABILITY AND ACCESS TIME.

YOU CAN CONVERT A TWO-DISK SYSTEM INTO A "FLUBBLE".

ENJOY THE BEST OF BOTH WORLDS!

FUTURE TRENDS

1 MEGABIT DEVICES

- 0° – 70°C OPERATION NOW
- – 20° – + 85°C OPERATION LATE 1981

4 MEGABIT TECHNOLOGY

- STANDARD PERMALLOY TECHNOLOGY
- FIRST SAMPLES, EARLY 1982
- 4 MEGABIT DEVICE UPWARD COMPATIBLE WITH PRESENT SUPPORT CIRCUITS
- 1 MEGABIT COST REDUCTION, PERFORMANCE ENHANCEMENT, 1982

BUBBLE MARKET SIZE

- $30 MILLION 1980, DOUBLING IN 1981. AS TERMINAL AND TELECOMMUNICATION APPLICATIONS GROW THE MARKET WILL EXCEED $300M BY 1984.

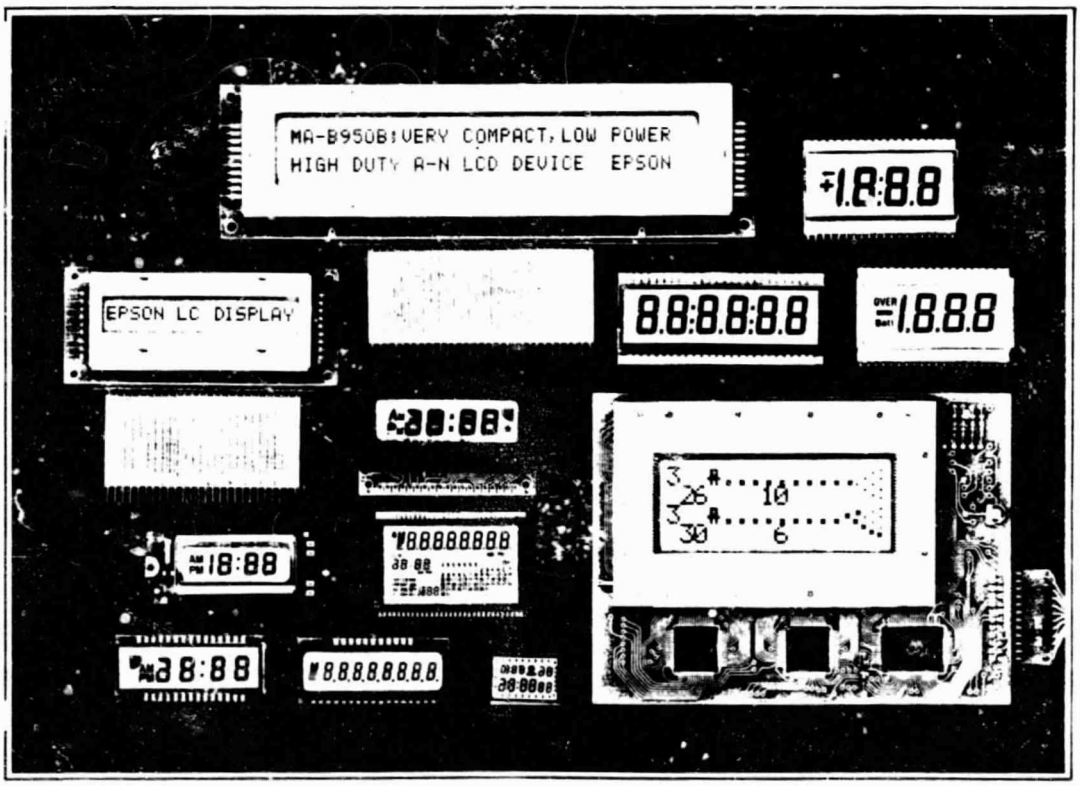
TOTAL BUBBLE MEMORY SOLUTION

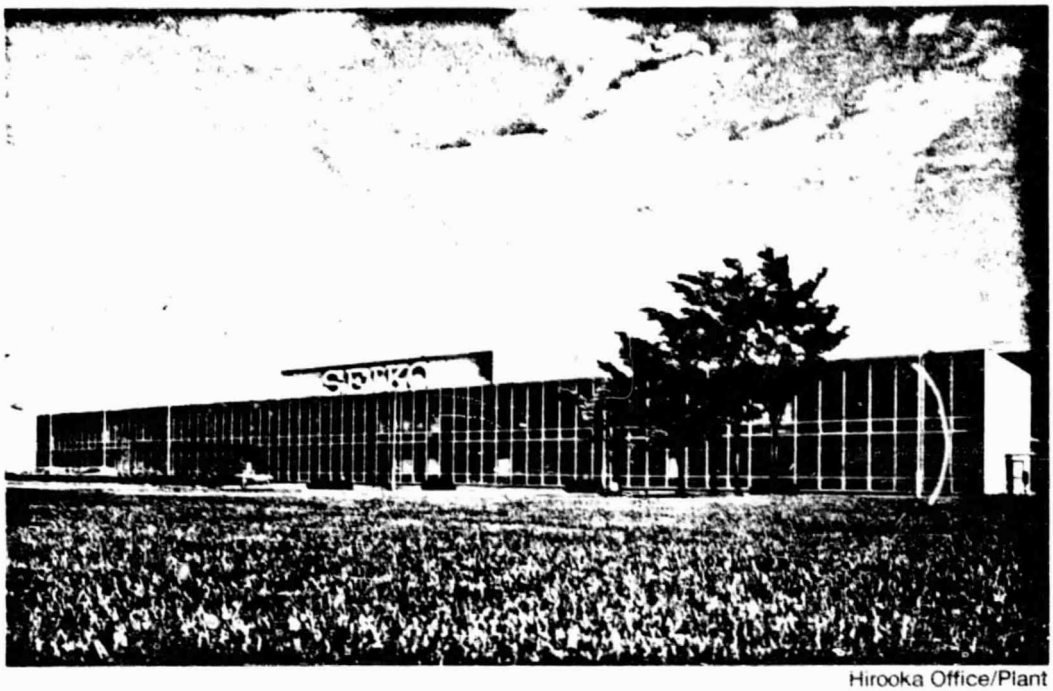
- **BUBBLE MEMORIES FOR MICROPROCESSOR BASED SYSTEMS**
  - COMPLETE LSI SUPPORT CHIP SET
  - MINIMUM CHIP COUNT SYSTEM
  - EXPANDABLE SYSTEM FROM 128 KBYTES TO 1 MBYTE
  - CONTROLLER CHIP INTERFACES TO MULTIBUS™
- **INTEL MAGNETICS DELIVERS SOLUTIONS**
  - BUBBLE SYSTEM HARDWARE COMPATIBLE WITH: 8080, 8085, 8086, 8088, 8089
  - BUBBLE SYSTEM SOFTWARE INVESTMENT CAN BE EXTENDED TO FUTURE PROCESSORS
  - BUBBLE SYSTEM WILL BE UPWARD COMPATIBLE FOR 4M BIT DEVICE
- **CHOICE OF FULLY ASSEMBLED TESTED BOARD: iSBC254 OR PRODUCTION AND PROTOTYPE COMPONENTS KITS: BPK70 AND BPK 72**

WE DELIVER THE TOTAL SOLUTION!

EPSON

LIQUID CRYSTAL DISPLAY





Hirooka Office/Plant

An introduction

In 1961, Shinshu Seiki Co., Ltd., was established as a member of Suwa Seiko Group, maker of Seiko watches, to manufacture watch parts. Subsequently, in 1969, the company was redirected to develop, manufacture and market general information processing equipment. Embracing the advanced principles that had propelled its parent to world leadership in fine watches, Shinshu Seiki, now EPSON, proceeded to become the largest producer of small electric digital printers and liquid crystal displays.

EPSON has succeeded in commercially producing the world's first long-life liquid crystal displays, making possible the first long-life pocket-size electronic calculators. This breakthrough was the result of many years of concerted R&D effort to refine low voltage operation, low power consumption and other critical points affecting liquid crystal display life. We offer diversified lines of liquid crystal products made under a highly efficient production system-ranging from displays for panels and ultraslim pocket calculators, to displays for watches, audio equipment, measurement instruments and computer terminals.

Matsumoto Division

Mural Division

I. STANDARD LIQUID CRYSTAL DISPLAY MODULS

Model No.	Description (LSI example)		Module Size	Page
ALPHANUMERIC				
MA-B950B	64 chara	(32 × 2 line)	180 × 50 × 19mm	6
MA-B952B	40 chara	(20 × 2 line)	147 × 47 × 19mm	6
MA-B955B	16 chara	(16 × 1 line)	93 × 38 × 14.5mm	6
MA-B956B	32 chara	(16 × 2 line)	115 × 47 × 19mm	6
MA-B965B	128 chara	(32 × 4 line)	180 × 69 × 20.5mm	7
MA-B967E	80 chara	(80 × 1 line)	260 × 47 × 21mm	7
MA-B8901A	40 chara	(40 × 1 line)	210 × 50 × 17mm	7
MA-B8902A	80 chara	(40 × 2 line)	210 × 50 × 17mm	7
TIMEPIECES				
MB-B163B	3-1/2 digit,	7mm	58 × 24 × 7.4mm	15
MD-G163B	3-1/2 digit,	7mm	58 × 24 × 6.6mm	15
SMC-2001A (TSC-2001A)	3-1/2 digit,	8mm or 10mm	60.2 × 38 × 10mm	15
SMC-2300 (TSC-2300)	3-1/2 digit,	8mm	60.2 × 38 × 10.5mm	15

II. STANDARD LIQUID CRYSTAL DISPLAY PANELS

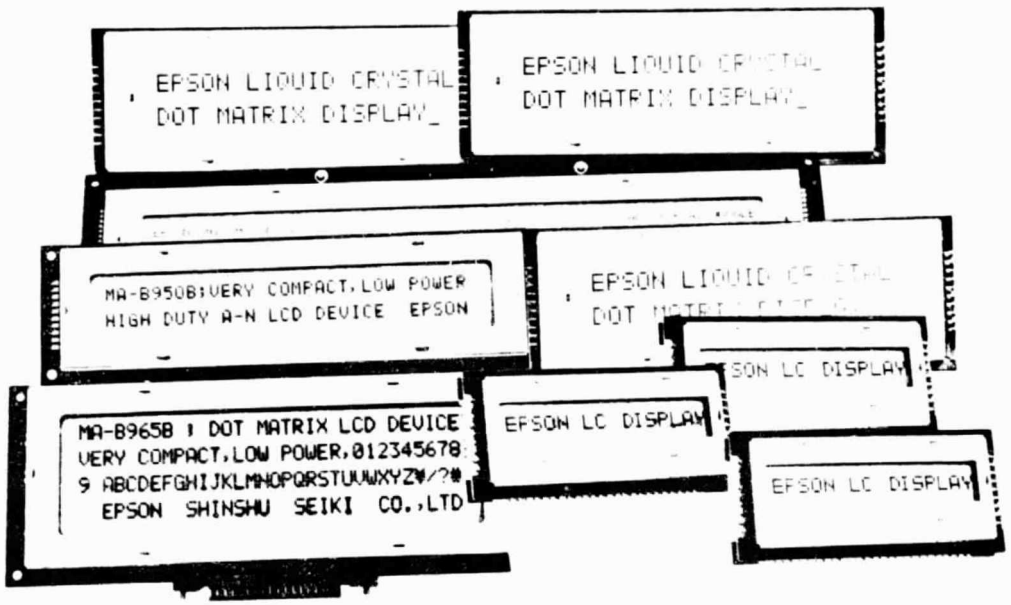
Model No.	Description (LSI example)		Glass Size(Thickness)	Page
GENEARL PURPOSE				
LD-B709BZ	3-1/2 digit,	12.7mm (Intersil ICL 7106)	52 × 30.5 (1.1)mm	10
LD-H7915A/AY/AZ(715)	3-1/2 digit,	12.7mm (Intersil ICL 7106)	50.8 × 30.5 (1.1)mm	10
LD-H7938A/AZ	3-1/2 digit,	12.7mm (Intersil ICL 7106)	50.8 × 30.5 (1.1)mm	10
LD-H7916A/AY/AZ(716)	4 digit,	12.7mm (OKI MSM5829GS)	50.8 × 30.5 (1.1)mm	10
LD-H7918A/AY/AZ(718)	6 digit,	12.7mm (RCA CD4055A)	69.8 × 30.5 (1.1)mm	10
LD-H7922A/AZ(722)	3-1/2 digit,	8.89mm (Intersil ICL 7106)	50.8 × 22.86 (1.1)mm	11
LD-H7923A/AZ(723)	4 digit,	8.89mm (OKI MSM5829GS)	50.8 × 22.86 (1.1)mm	11
LD-H7924A/AZ(724)	4-1/2 digit,	8.89mm (ICM 7224(A))	50.8 × 22.86 (1.1)mm	11
LD-H7992AZ	3-1/2 digit	17.78mm (Intersil ICL 7106)	69.85 × 38.1 (1.1)mm	11
LD-H7994AZ	4 digit,	17.78mm (OKI MSM5829GS)	69.85 × 38.1 (1.1)mm	11
LD-H7995AZ	5 digit,	17.78mm (RCA CD4055A)	81.3 × 38.1 (1.1)mm	11
LD-H7996AZ	6 digit	17.78 (RCA CD4055A)	93.85 × 38.1 (1.1)mm	11
LD-H9003E	100 elements bar -graph		70 × 22 (1.1)mm	11
LD-H7926A(726)	8 digit,	7mm (Intersil ICM7231)	52 × 22 (6.1)mm	12
LD-H7927A(727)	10-1/2 digit,	7mm (Intersil ICM7232)	61 × 22 (1.1)mm	12
LD-H7928A(728)	8 digit,	7mm (Intersil ICM7233)	70 × 22 (1.1)mm	12
LD-B210B	8 digit,	9 mm (ITT SAA6002)	70 × 30 (1.1)mm	12
LD-B8003	8 digit,	7mm (NEC UPD7225G)	52 × 22 (1.1)mm	12
LD-H7960A	4-1/2 digit,	10mm (Intersil ICM7231)	50.8 × 30.5 (1.1)mm	12
FOR CALCULATORS				
LD-B615	8 digit,	5mm (Toshiba T6014)	40 × 18 (1.1)mm	13
LD-666	8 digit,	6mm (NEC UPD1832G)	52 × 15 (1.1)mm	13
LD-626	8 digit,	6mm (NEC UPD1832G)	52 × 17.3 (1.1)mm	13
LD-326	8 digit,	6mm (NEC UPD1832G)	52 × 22 (1.1)mm	13
LD-B370	8 digit,	6mm (NEC UPD1831G)	52 × 22 (1.1)mm	13
LD-B395	8 digit,	4.3mm (NEC MPD1032G)	40 × 18 (0.7)mm	13
LD-B689	8 digit,	4.5mm (Toshiba T3821)	40 × 18 (0.7)mm	13
LD-B682	8 digit,	6mm (Toshiba T3922)	52 × 22 (1.1)mm	13
LD-B690	8 digit,	6mm (Toshiba T3821)	52 × 22 (1.1)mm	13
LD-B480	Calender	6mm (Toshiba T3923)	52 × 35 (1.1)mm	13
LD-B613	8 digit,	6mm (NEC UPD1852G)	52 × 22 (1.1)mm	14
LD-B657	8 digit,	6mm (NEC UPD1854G)	52 × 22 (1.1)mm	14
LD-B676	11 digit,	6mm (Toshiba T6755)	52 × 22 (1.1)mm	14
LD-B685	8 digit,	6mm (Toshiba T3918)	52 × 22 (1.1)mm	14
LD-372	11 digit,	5.5mm (NEC UPD1856G)	61 × 22 (1.1)mm	14
LD-B412	8 digit,	5.5mm (Toshiba T6705)	52 × 22 (1.1)mm	14
LD-B622	10 digit,	8mm (Toshiba T6701)	70 × 22 (1.1)mm	14
LD-B818	10 digit,	9.5mm (Toshiba T6701)	90 × 30 (1.1)mm	14
LD-B820	12 digit,	9mm (Toshiba T6701)	103 × 30 (1.1)mm	14
LD-B884	10 digit,	10mm (NEC UPD1033G)	90 × 30 (1.1)mm	14
TIMEPIECECS				
LD-B122	3-1/2 digit,	6.3mm (NEC UPD833G)	40 × 18 (1.1)mm	15
LD-B130	3-1/2 digit,	10mm (Mitsubishi M58412P)	52 × 22 (1.1)mm	15
LD-B168	6 digit,	8.4mm (OKI MSM5557RS)	52 × 22 (1.1)mm	15
LD-B154	6 digit,	9mm (Toshiba TC8208AF)	52 × 22 (1.1)mm	15
LD-B171	6 digit,	9.1mm (Toshiba TC8202AF)	52 × 22 (1.1)mm	15
LD-B137	6 digit,	8mm (NEC UPD1993G)	70 × 30 (1.3)mm	15
LD-B116	3-1/2 digit	12mm (NEC UPD833G)	70 × 30 (1.3)mm	15
LD-B089E	5-1/2 digit,	5mm (SUWA SEIKO S5789)	23.8 × 13.9 (0.7)mm	15

Specifications are subject to change without notice.
Ask EPSON for the latest specifications and product line up.

3

EPSON

ALPHANUMERIC LCD MODULES



FEATURES

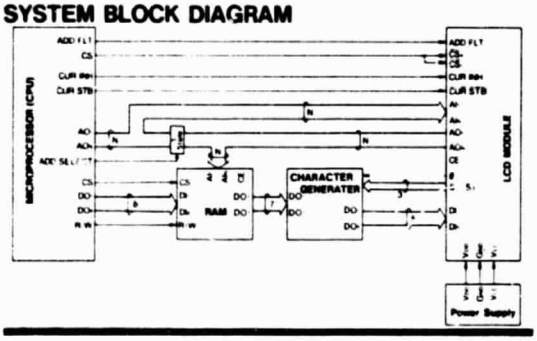
- 1/8 or 1/16 multiplex drive LCD
- High contrast and readability
- Compact size and light weight
- Easy-to-read character size (5×7 dot matrix format)
- Low power consumption

DESCRIPTION

Epson Alphanumeric LCD Module consists of a Liquid Crystal Display, CMOS LSI to control and drive the LCD, and a power distribution circuit with temperature compensation circuit. A 1/8 Multiplex Drive using a newly developed FEM twisted nematic type liquid crystal presents complete 5×7 dot matrix alphanumeric characters and a cursor. The combination of LCD and CMOS LSI affords the benefits of extremely low power consumption, compact size and light weight. The Module can be connected directly to any microprocessor, character generator, and random access memory (RAM). This inexpensive display module, suitable for a wide variety of applications requiring alphanumeric display, is an outgrowth of Epson's highly proven technology in 1/3 Multiplex and 8-digit display developed for the hand-held calculator field.

The LCD Module has two kinds of CMOS LSI: X driver and Y driver. The X driver takes care of driving 40-column lines (8 characters), and the Y driver takes care of row lines (8 backplanes). The Y driver also controls the whole module operation. Basically, the Y driver addresses and selects the information contained in RAM. It accepts the data input through a character generator and displays it. New display information is written by addressing the memory by the CPU after turning the address bus of the module to high impedance state by an ADD FLT signal. A cursor can be displayed at any place by addressing it to the module.

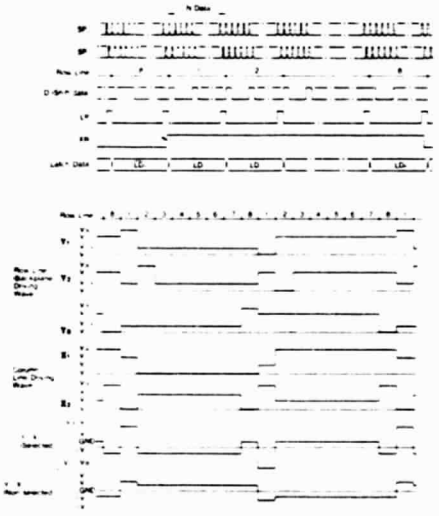
SYSTEM BLOCK DIAGRAM



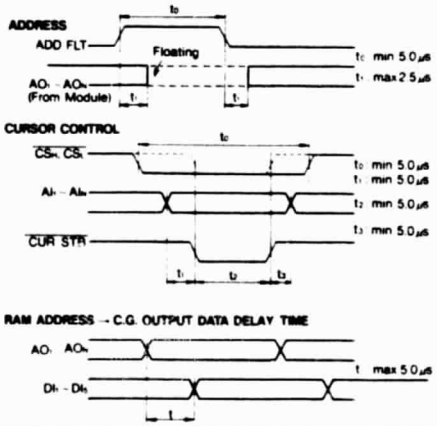
INPUT/OUTPUT SIGNAL

ADD FLT	(INPUT)	: Address floating bus
$\overline{\text{CUR STB}}$	(INPUT)	: Cursor address signal
CUR INH	(INPUT)	: "O" when cursor is used "I" when cursor is not used
AO_1 to AO_n	(OUTPUT)	: Address bus of character data to RAM
AI_1 to AI_n	(INPUT)	: Address bus for cursor input
Ø	(OUTPUT)	: Synchronous signal to character generator if necessary
S_1 to S_3	(OUTPUT)	: Row select signal to character generator
$\overline{CS}_H$, $\overline{CS}_L$	(INPUT)	: Select signal for module at cursor address input
DI_1 to DI_5	(INPUT)	: Parallel data of character for column line
CE	(OUTPUT)	: Synchronous signal with memory if using semi-static RAM
V_{DD}	(INPUT)	: Power supply for logic circuit
V_{LC}	(INPUT)	: Power supply for LC driving

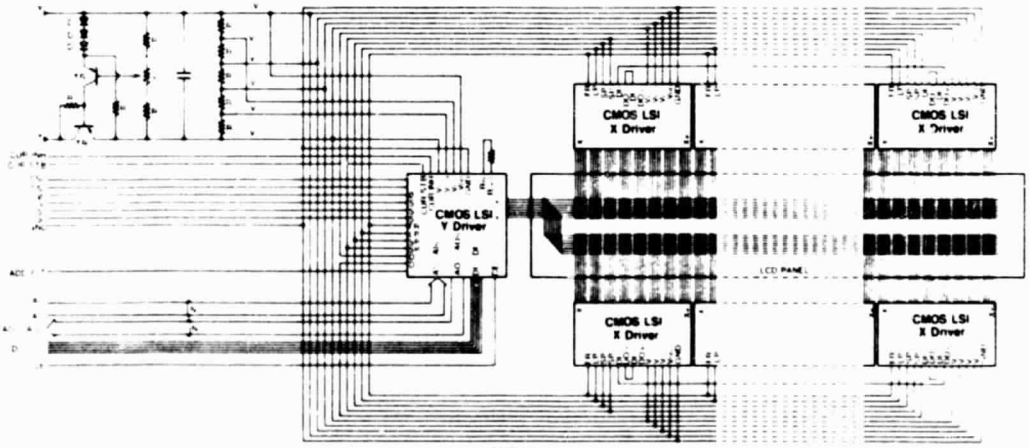
X DRIVER & DRIVING WAVE FORM



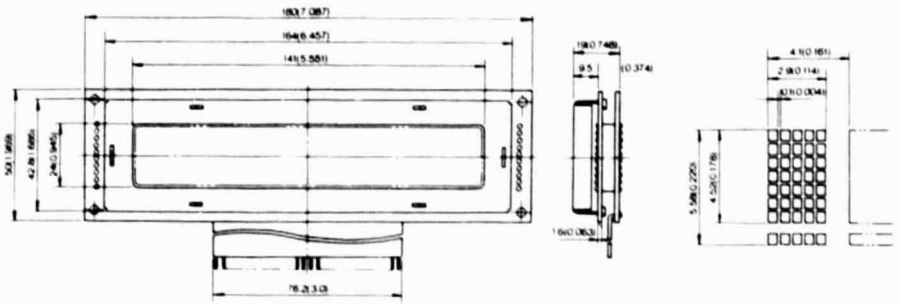
TIMING CHART



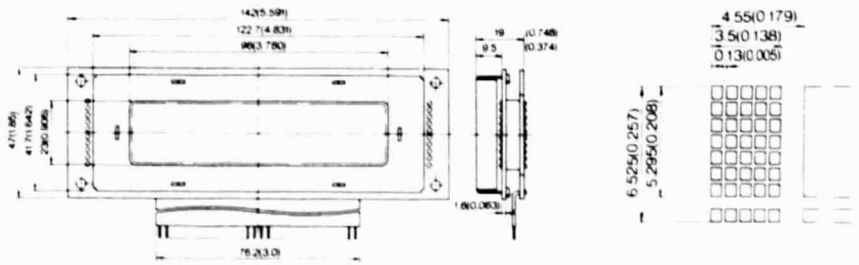
SCHEMATIC DIAGRAM OF MODULE



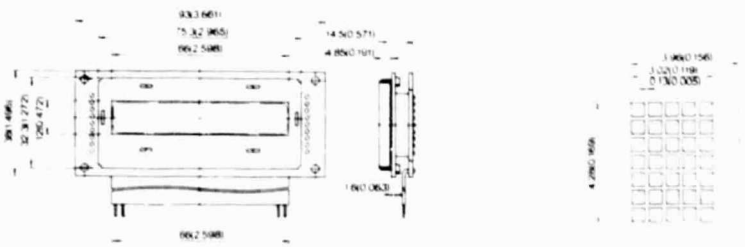
ALPHANUMERIC MODULES



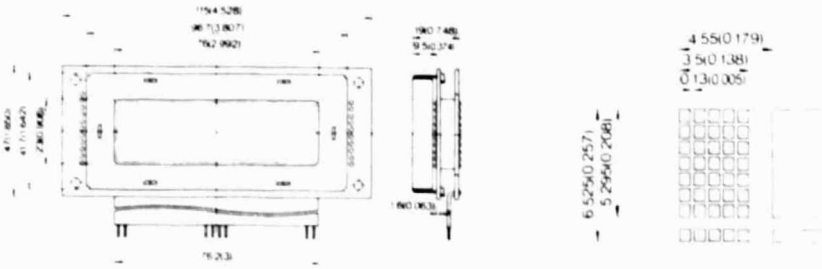
MA-B9508



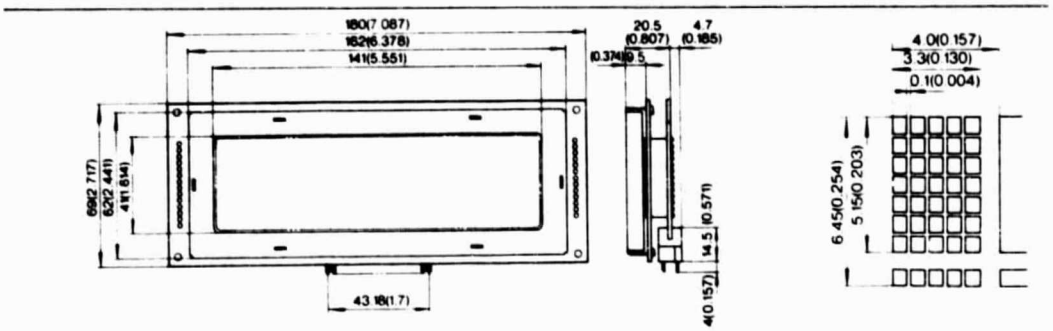
MA-B9528



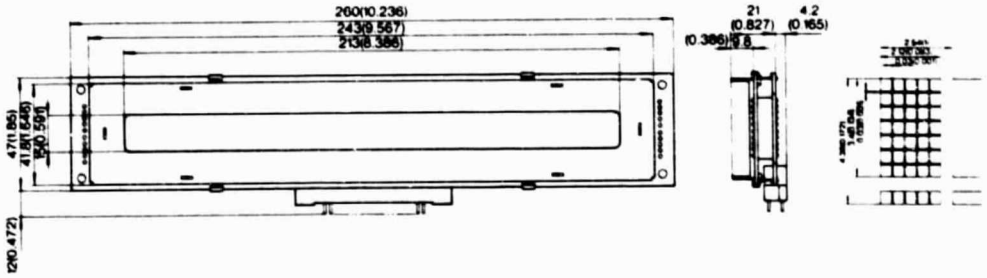
MA-B9558



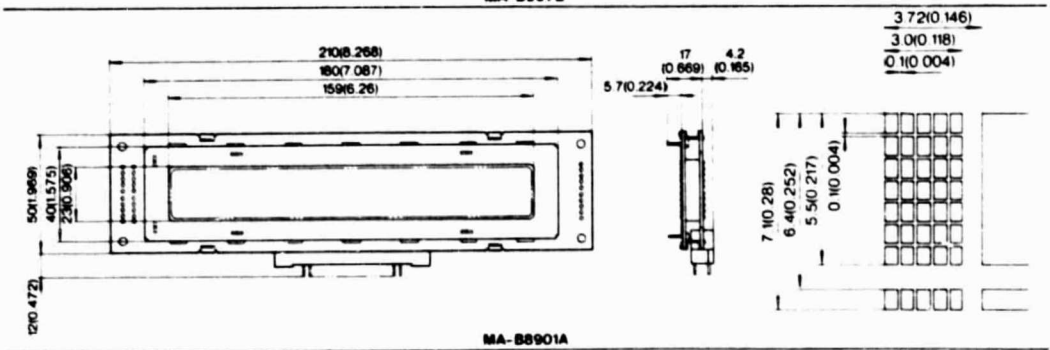
MA-B9568



MA-B9658



MA-B9678



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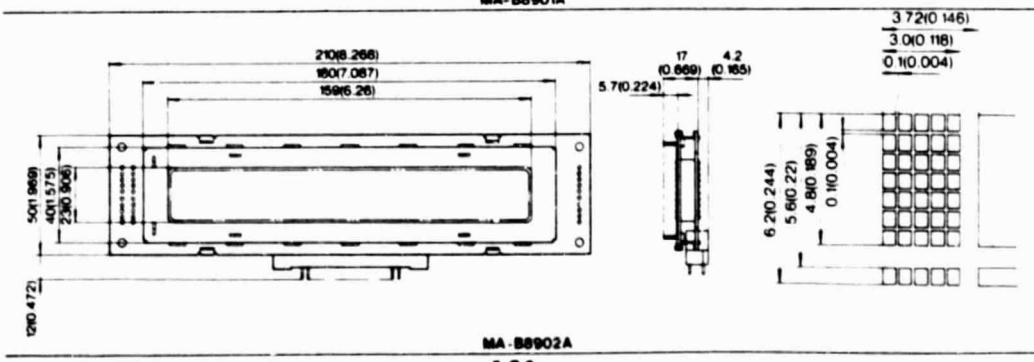


MA-B8902A

EPSON

EPSON LCD'S FEATURE

- Ultra Low Power Consumption
- Excellent Readability/Wide Viewing Angle
- C-Mos/TTL Compatible
- Multiplex/Direct Drive Technology
- 100,000 Hour Expected Life
- Wide Temperature Range (−30°C to +80°C)
- Proven Reliability/Excellent Quality Assurance
- High Contrast/Bright Backgrounds
- MIL-STND Connector Pins
- Reflective/Transmissive/Transflecfive Versions
- DIL Pin/Spring Pin/Pinless Version

TYPICAL PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings (with polarizers)

Parameter	Liquid Crystal Material						Unit
	Commercial			Wide Temperature			
	Static I	Static II	Multiplexed I	Static A	Static B	Multiplexed A	
Applied Voltage, AC	10	10	10	20	20	20	Vrms
Applied Voltage, DC	3.5	3.5	3.5	7	7	7	V
Operating Temperature Range	−10 ~ +55	−10 ~ +55	−10 ~ + 55	−30 ~ +80	−30 ~ +80	−10 ~ +60	°C
Storage Temperature Range	−20 ~ +60	−20 ~ +60	−20 ~ +60	−40 ~ +85*	−40 ~ +85*	−40 ~ +85*	°C
Operating Frequency Range	30 ~ 180	30 ~ 180	60 ~ 300	30 ~ 180	60 ~ 180	60 ~ 300	Hz

* In case of DIL pin connector type, the range is −30 ~ +80

Recommended Operationg Conditions (with polarizers)

Parameter	Liquid Crystal Material																		Unit
	Commercial									Wide Temperature									
	Static I			Static II			Multiplexed I			Static A			Static B			Multiplexed A			
Operating Voltage	2.7	3.1	3.3	3	5	7				3.5	5	7	3.5	5	7				
Operating Voltage	5.4	6.2	6.6	6	10	14				7	10	14	7	10	14				Vpeak-peak
Operating Voltage							2.95	3.1	3.26								4.5	*1	V
Saturation Voltage								*2									*3		
Operating Frequency Range	30		120	30		120	80		180	30		120	30		120	60		180	Hz
Operating Temperature Range	0	25	40	0	25	40	0	25	40	−20	25	80	−30	25	80	−10	25	60	°C

*1 Temperature compensation is required.
*2 Von = 1.88V(min), Voff = 1.09V(Max), Conditions 0 ~ 40°C
*3 Von = 2.84V(min), Voff = 1.45V(Max), Conditions −10 ~ 60°C

Typical Operating Characteristics (on typical conditions)

Parameter	Liquid Crystal Material						Unit
	Commercial			Wide Temperature			
	Static I	Static II	Multiplexed I	Static A	Static B	Multiplexed A	
Operating Current 12.7mm(0.5") chara height	1.2	1.5	1.2	1.5	1.5	1.5	μA/digit
Operating Response Time							
Tr (Ta = 60°C)	—	—	—	25	25	—	
Tf (Ta = 60°C)	—	—	—	40	30	—	
Tr (Ta = 25°C)	120	100	120	45	40	120	
Tf (Ta = 25°C)	100	100	150	75	50	100	
Tr (Ta = 0°C)	600	400	500	150	100	300	
Tf (Ta = 0°C)	400	500	400	300	120	300	
Tr (Ta = −20°C)	—	—	—	1000	350	—	
Tf (Ta = −20°C)	—	—	—	1800	400	—	
Tr (Ta = −30°C)	—	—	—	—	800	—	
Tf (Ta = −30°C)	—	—	—	—	800	—	ms
Contrast Ratio	20:1	20:1	20:1	20:1	20:1	20:1	
Expected Life	50,000	50,000	50,000	100,000	100,000	100,000	Hours

Note Above are typical specifications for your reference. Please ask for an individual specifications of each model for defintion and confirmation before design.

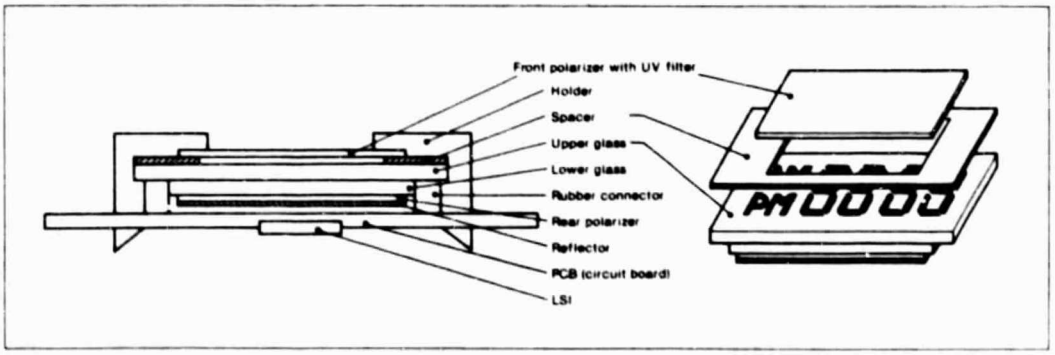
Typical Environmental Test Specifications

Parameter	Liquid Crystal Material			Unit
	Static I, II, Multiplexed I	StaticA, Multiplexed A	Static B	
Temperature/Humidity				
A. No Polarizers				
80°C, 95% Relative Humidity	> 100	> 200	> 200	H
60°C, 70% Relative Humidity	> 500	> 2,000	> 2,000	H
B. Polarizers glued				
60°C, 70% Relative Humidity	> 300	> 1,000	> 1,000	H
40°C, 90% Relative Humidity	> 200	> 500	> 500	H
Thermal shock				
α°C for 30minutes, 25°C for 5minnutes β°C for 30minutes, 20°cycles.	$\alpha = -20$ $\beta = 60$	$\alpha = -40$ $\beta = 85$	$\alpha = -40$ $\beta = 85$	
Pressure (Altitude) exceeds MIL-STD-883 section 1001 Grade E. The LCD will operate above X kilometers if within the operating temp. range	X = 30	X = 30	X = 30	km

Mechanical Specifications

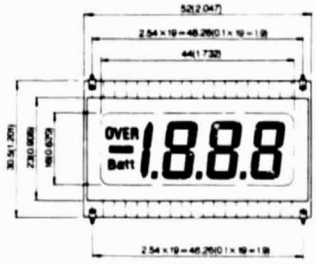
Parameter	Min.	Typ.	Max.	Unit
Mechanical Shock Mechanical shock consisting of 500 Gs @ 1 millisecond of half wavefoom in three mutually perpendicular axes. The LCD is fixed in position on its front surface.		1		Cycle
Vibration One Logarythmic frequency sweep from 10 to 500 Hz (sinusoidal) at 10 Gs, or 1.52mm amplitude (whichever is smaller) during a 15 minute time period. One sweep is required in each of three mutually perpendicular axes. The LCD is fixed in position on its front surface.		36		Sweeps
Connector Pin Bend Test With an 7 ounce weight attached to the pins, the pin must exceed three 90° bends before breaking.		3		Bends

Example of assembly (Reflective type)



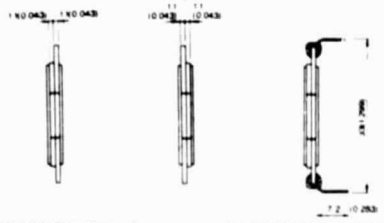
Note
- Treat panels as carefully as glass.
- Avoid direct sunlight.
- Do not store panels in high temperature and/or high humidity environment.
- Clean panels with wet or alcohol cloth and polarizers with wet or dry cloth.
- The size of housing-window should be less than the display size of panel.
- A transparent protector (for example, clear acryl plate) should be provided on the finishing housing to protect display from physical damage.
- Display should not be driven by a direct current load.
- In case of soldering, dipping of pins in solder at 260 – 300°C for about 5 seconds is recommended.

GENERAL PURPOSE LCDs



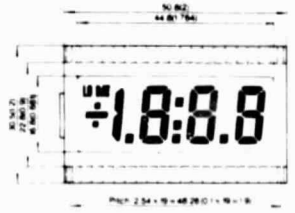
LD-B7098Z

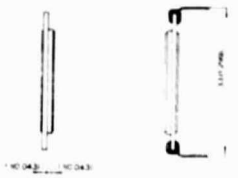
LD-H7915A (LD-B7158Y)



LD-H7915AY (LD-B7158)

LD-H7915AZ (LD-B7158Z)

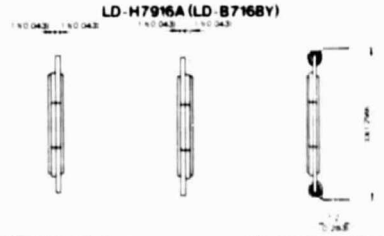




LD-H7938A

LD-H7938AZ

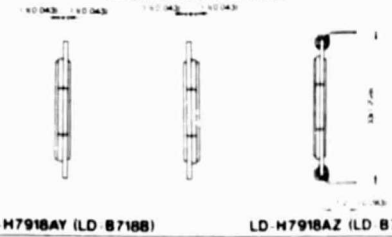
LD-H7916A (LD-B7168Y)



LD-H7916AY (LD-B7168)

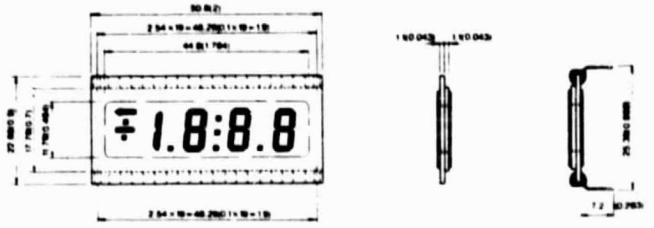
LD-H7916AZ (LD-B7168Z)

LD-H7918A (LD-B7188Y)



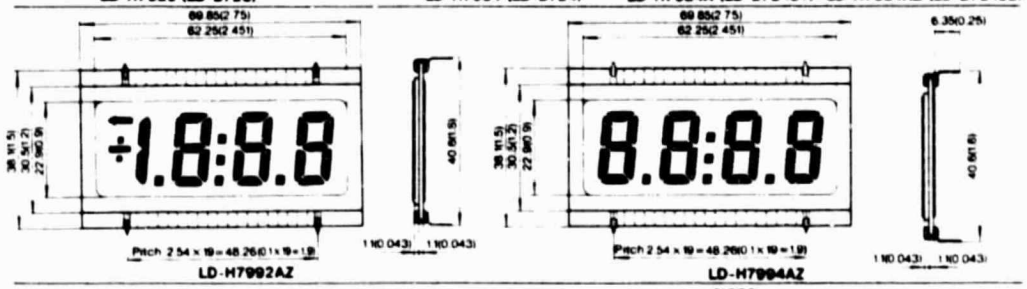
LD-H7918AY (LD-B7188)

LD-H7918AZ (LD-B7188Z)

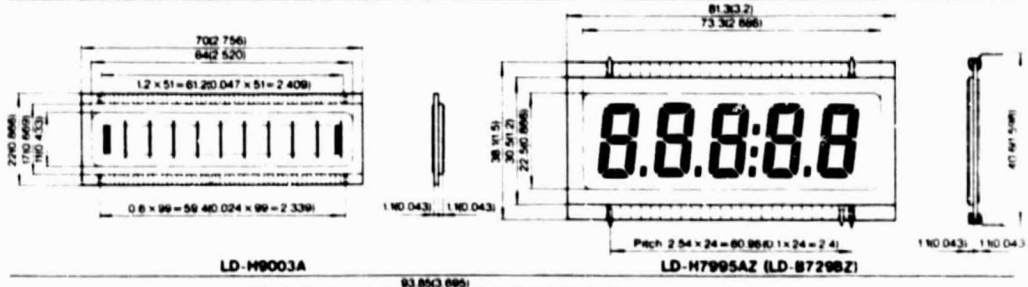


LD-H7922A (LD-B722BY) LD-H7922AZ (LD-B722BZ)

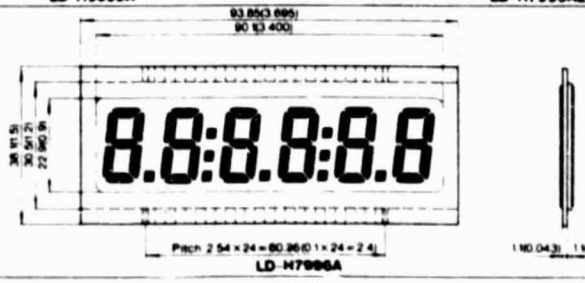
LD-H7923 (LD-B723) LD-H7924 (LD-B724)
LD-H7923A (LD-B723BY) LD-H7923AZ (LD-B723BZ)
LD-H7924A (LD-B724BY) LD-H7924AZ (LD-B724BZ)



LD-H7992AZ LD-H7994AZ

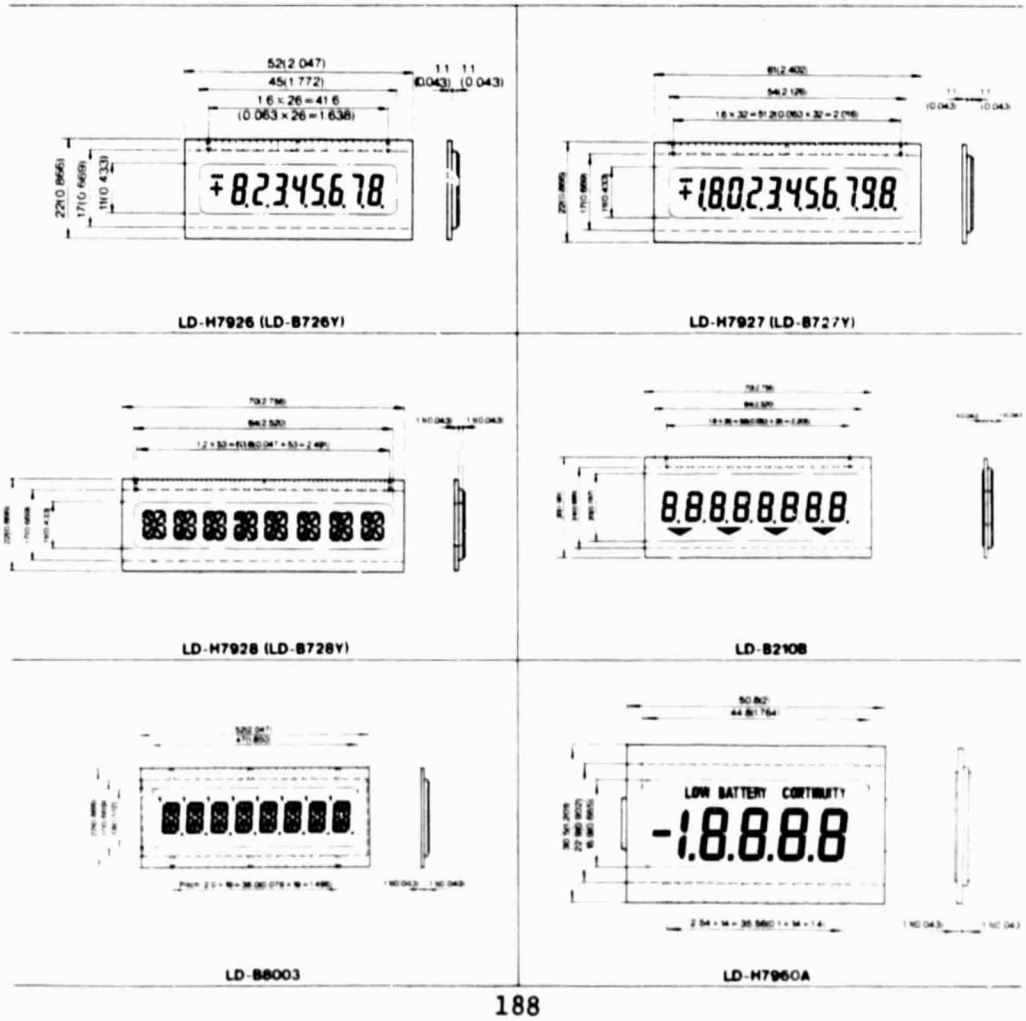


LD-H9003A LD-H7995AZ (LD-B729BZ)



LD-H7996A

GENERAL PURPOSE MULTIPLEXED LCDs



LD-H7926 (LD-B726Y)

LD-H7927 (LD-B727Y)

LD-H7928 (LD-B728Y)

LD-B2108

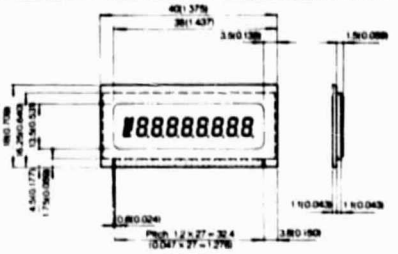
LD-B8003

LD-H7960A

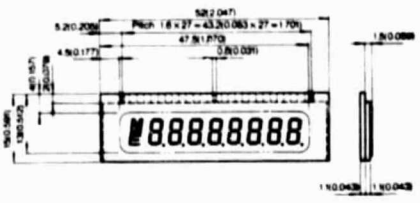
EPSON

FOR CALCULATORS

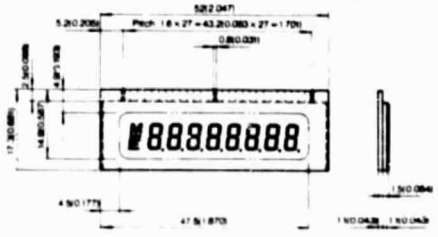
■FOR 8 DIGITS CALCULATOR



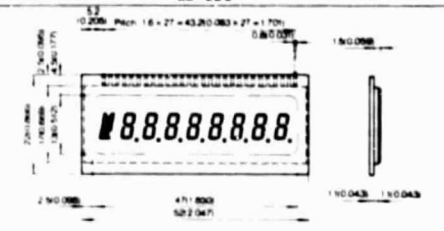
LD-B615



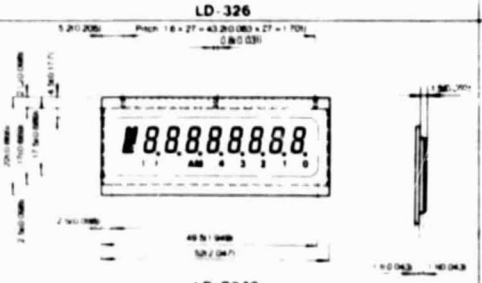
LD-666



LD-626

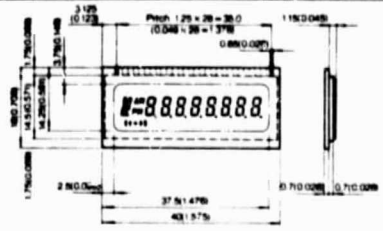


LD-326

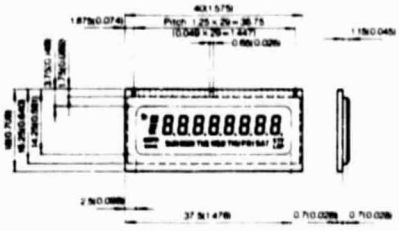


LD B370

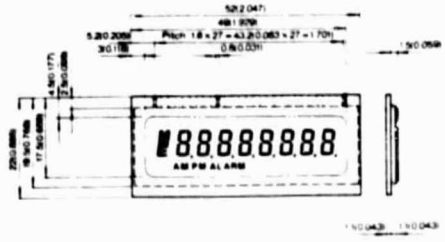
■FOR 8 DIGITS CALCULATOR WITH CLOCK



LD B395

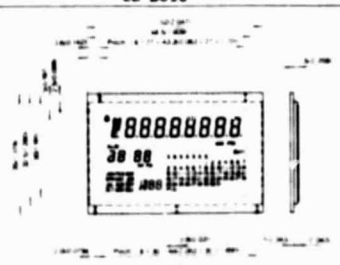


LD B689



LD B682

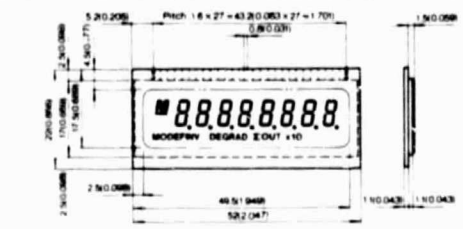
LD B690



LD B480

EPSON

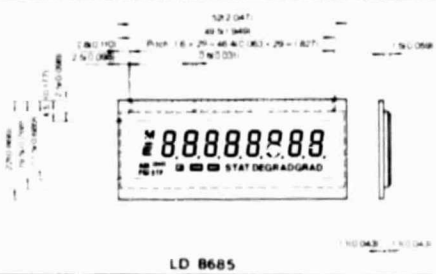
■FOR SCIENTIFIC CALCULATOR



LD B613

LD B657

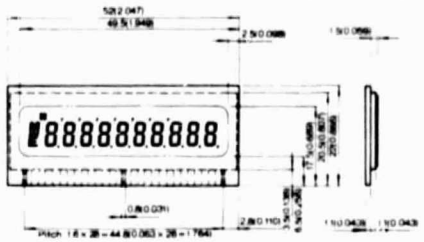
LD B676



LD B685

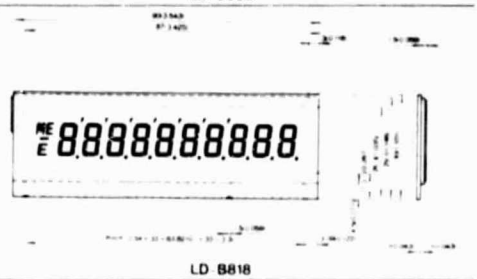
LD 372

■FOR DESK TOP CALCULATOR

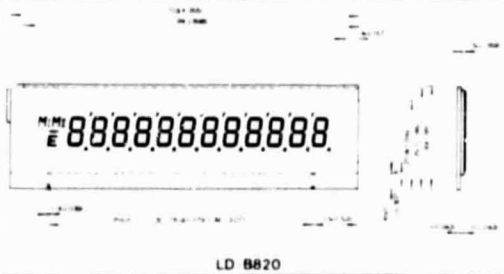


LD B412

LD B622



LD B818

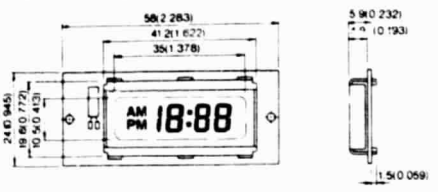


LD B820

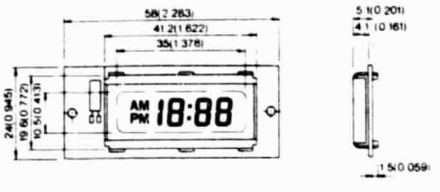
LD B884

EPSON

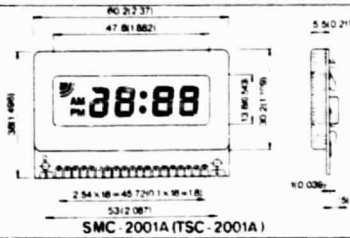
TIMEPIECES



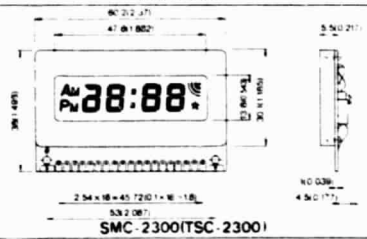
MB-B163B



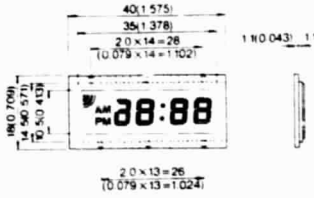
MD-G163B



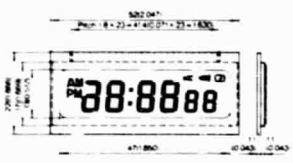
SMC-2001A (TSC-2001A)



SMC-2300(TSC-2300)



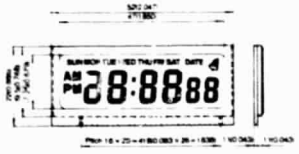
LD-B122



LD-B168

LD-B130

LD-B154



LD-B171

LD-B116

LD-B137

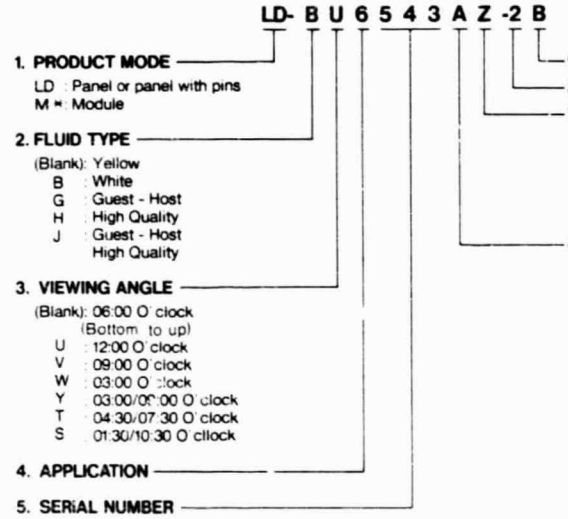
LD-B089E

15

FOR REFERENCE OF MODEL NUMBER STRUCTURE

EPSON LCD model numbers are structured based on the following

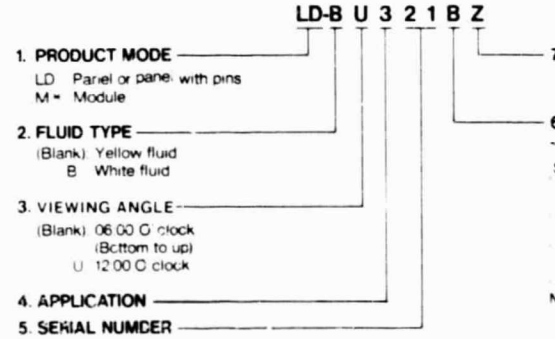
I. NEW MODEL CODE



Symbol	Type	Upper Parts	Rear Parts
Blank	Reflective		
A			
B			
C	Cell Only		
D	Transmissive		
E			
F			
G	Transflective		
J			
K			

Note 1. ○ Glued, △ Attached, - Excluded
2. ✱ Upper Parts Upper polarizer with U.V. filter
✱ Rear Parts
1) Reflective Polarizer with reflector
2) Transmissive Polarizer with U.V. filter
3) Transflective Polarizer with U.V. filter and transflector

II. OLD MODEL CODE



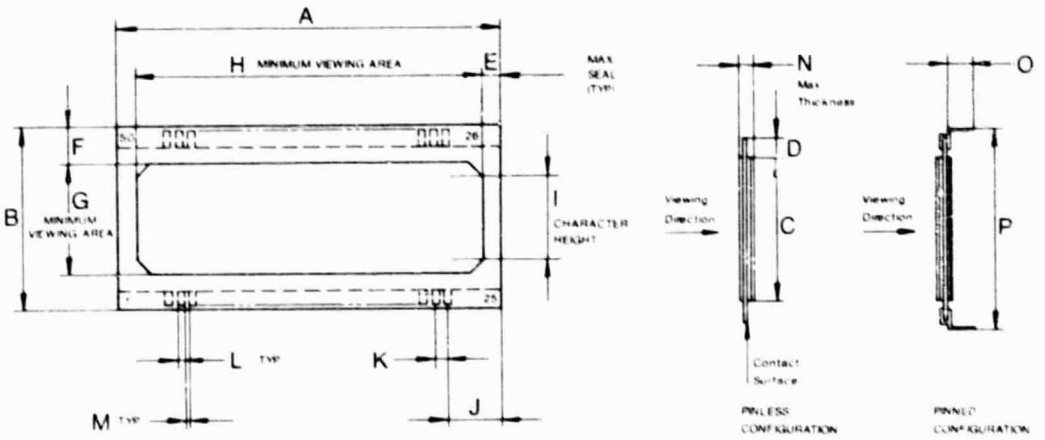
Symbol \ Parts	UV Filter	Upper polarizer	Rear polarizer	Reflecter
(Blank)				
A				
B				
C				
D				
E				

Note 1. (○ Glued, △ Attached, - Excluded)
2. Rear polarizer which is not attached by (reflector includes UV filter)

EPSON

CUSTOM
Liquid Crystal Displays

- Contact EPSON representative in your territory or head office for delivery and pricing information.



Dimensions:

A.	Glass length: _____ mm	I.	Character height: _____ mm
B.	Glass width: _____ mm	J.	Glass edge to first contact pad: _____ mm
C.	Backglass width: _____ mm	K.	Pitch of contact pads: _____ mm
D.	Contact plane offset: _____ mm	L.	Contact pad width: _____ mm
E.	Typical seal width: _____ mm (3mm is recommended)	M.	contact pad space: _____ mm
		N.	Panel thickness: _____ mm
F.	Glass edge to viewing area: _____ mm	O.	Connector pin length: _____ mm
G.	Min. height of viewing area: _____ mm	P.	Row-to-row spacing of connector pins: _____ mm
H.	Min. length of viewing area: _____ mm		

Operating Conditions

Parameter	Min.	Typ.	Max.
Operating Voltage			
Operating Frequency Range			
Operating Temperature Range			

Driving Method

- Direct drive
- 1/2 multiplex
- 1/3 multiplex
- 1/4 multiplex
- 1/8 multiplex
- 1/16 multiplex

Viewing Angle

- 6:00 O'clock (STND., bottom + up)
- 12:00 O'clock
- 9:00 O'clock
- 3:00 O'clock
- 3:00/9:00 O'clock
- 4:30/7:30 O'clock
- 1:30/10:30 O'clock

Polarizers

- Commercial
- High quality
- Laminated
- Loose

Reflector

- Brushed aluminum foil (STND)
- Silver beads
- Transflector

Connector Type

- Elastmer (Rubber)
- Spring pin (Teledyne: snap-on)
- DIL pin

Compatible LSI: _____

Application: _____

EPSON

SHINSHU SEIKI CO.,LTD.

HEAD OFFICE & PLANT: 80 Hirooka, Shiojiri-City, Nagano, 399-07 Japan. Tel: 02635-2-2552 Telex: 0334-2214(SHINH J)

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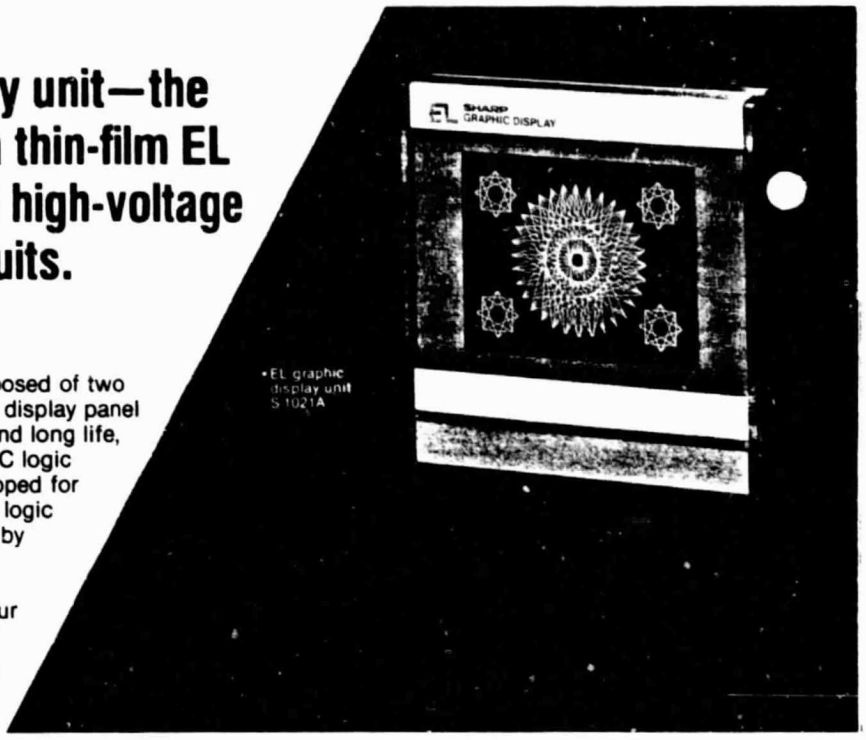
SHARP S-1021A/S-1050

EL Display Units

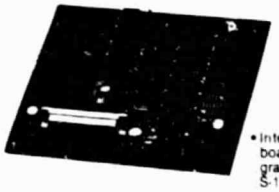
Sharp's electronic technology makes possible new computer systems, with a slim, clear EL display unit

Sharp's EL display unit—the consolidation of a thin-film EL display panel and high-voltage MOS IC logic circuits.

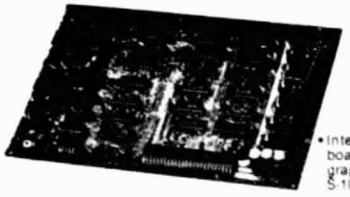
Sharp's EL display unit is composed of two parts: an advanced thin-film EL display panel known for its high brightness and long life, and reliable high-voltage MOS IC logic circuits which have been developed for panel drive. The unit also has a logic circuit which can be controlled by external signals. Graphics and messages can be displayed by three DC power sources and four input interface signals supplied at the LS TTL level (data signal, data transfer clock, horizontal synchronizing signal, and vertical synchronizing signal). Moreover, the EL display unit is clear, thin and has a wide viewing angle. It allows incorporation of various terminal equipment to form a new system.



•EL graphic display unit S-1021A



•Interface circuit board for coded graphic display S-1026C

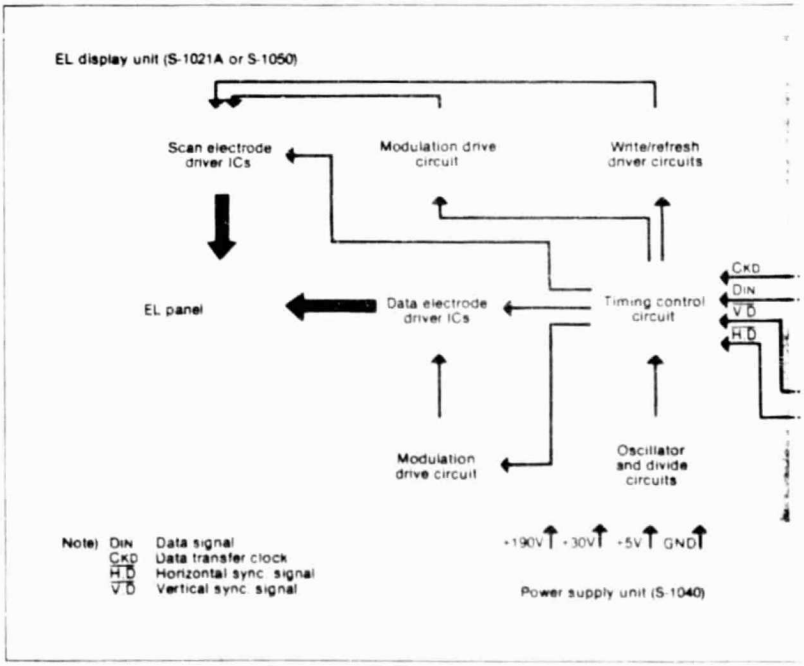


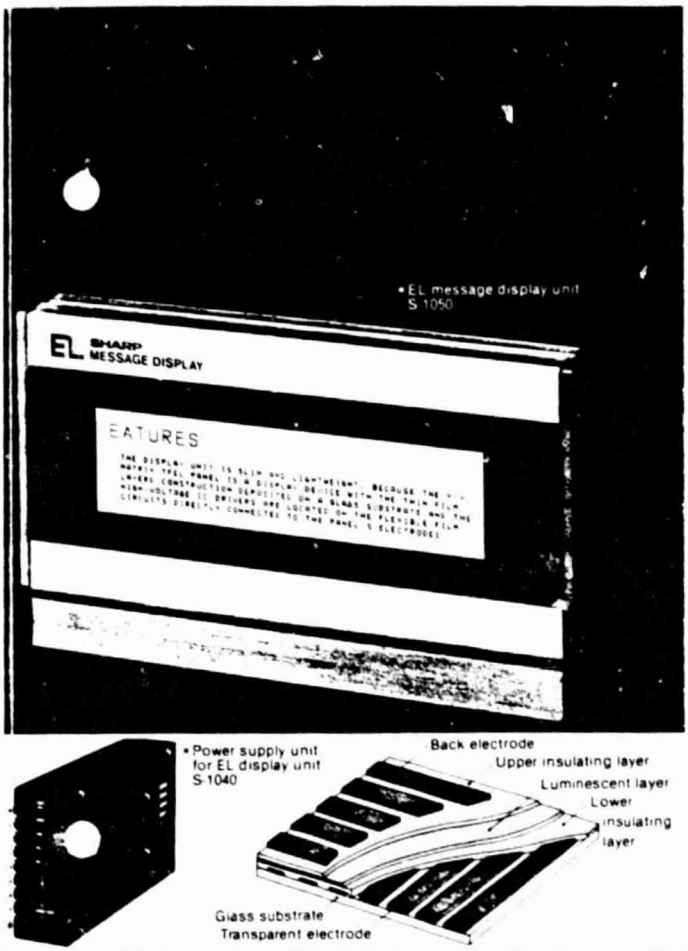
•Interface circuit board for full graphic display S-1026F

System configuration of EL display units
The sample system configuration illustrated here is for a full graphic display using a Z-80 microcomputer.

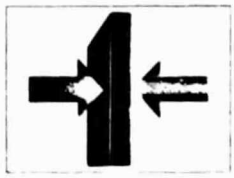
•Main applications
With various terminal equipment—
Online terminals, bank terminals, POS terminals, office computers, personal computers, word processors, electronic typewriters, and educational equipment.

With measuring equipment—
Logic status analizers, manufacturing process control monitors, NC's, and measuring equipment for medical electronics.





• Power supply unit for EL display unit S-1040



Features

•Slim and light in weight Due to the consolidated construction of a thin film EL display panel and IC logic circuits, the unit is very light and compact.

•Clear and stable display The desired display position is specified by selecting some of intersections of the vertical and horizontal electrodes in the X-Y matrix panel. This means that the display image is clear and stable without distortion, drift or glare.

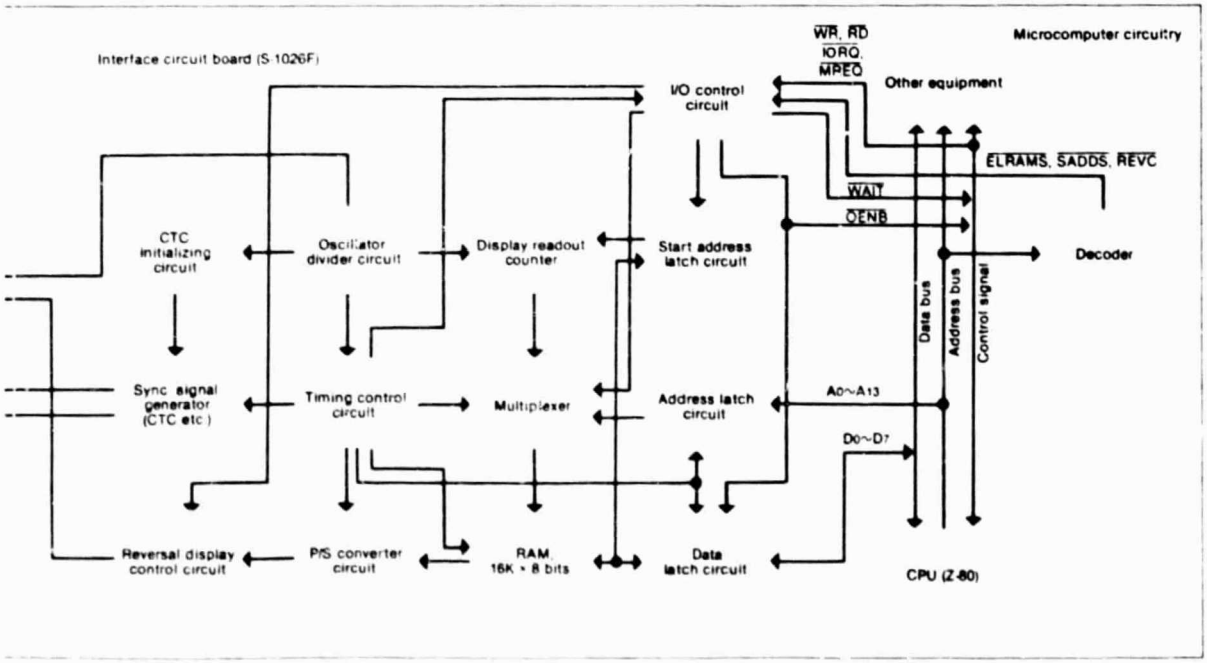
•Wide viewing angle Thanks to the thin film's luminescent elements, the viewing angle is wide and convenient.

•Easy-to-read display The orange-yellow readout is very effective in minimizing eye strain.

•Complete display with a full-line electrode configuration Since the X-Y matrix electrodes constitute a full-line configuration, graphic displays as well as character and symbol displays are provided.

The structure of the X-Y matrix type EL panel

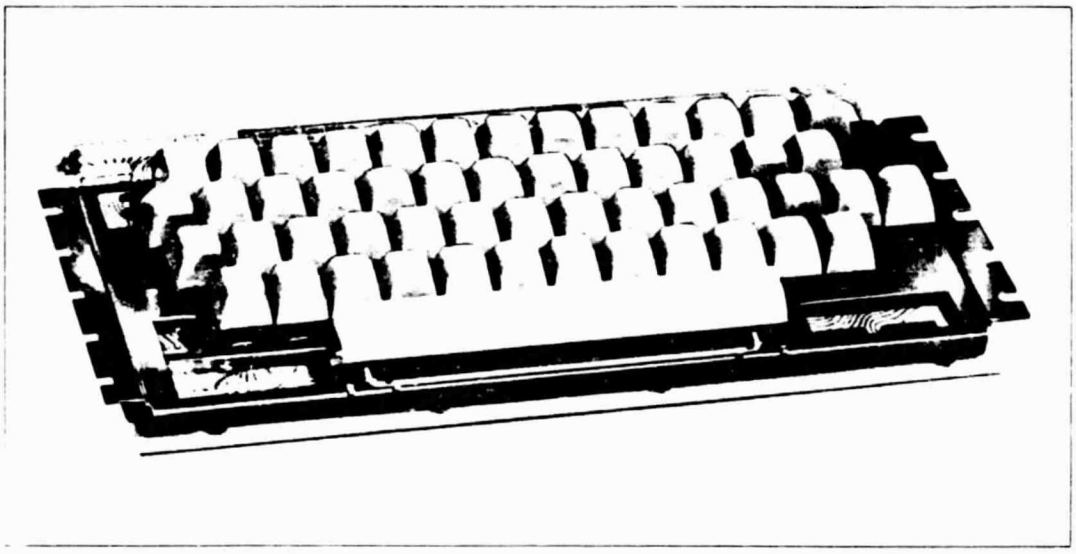
The EL panel has a multi-layer construction consisting of an EL layer sandwiched between upper and lower insulating layers. All these thin films of the panel, except the back A1 electrodes, are transparent. The electrodes are arrayed so as to intersect with each other at right angles and form an X-Y matrix. When AC pulses are applied across these two electrode groups and a high electric field is applied to the specified electrode intersections, the corresponding picture elements emit light to form the desired image.



MICRO SWITCH

product sheet **53SD5-2**

MOS ENCODED COMMUNICATIONS SOLID STATE KEYBOARD



The 53SD5-2 is a low-profile, modestly priced keyboard, ideally suited to conversational time sharing terminals for online inquiry. The keyboard utilizes the time-proven technology and reliability that made MICRO SWITCH the number one solid state keyboard manufacturer. The keyboard incorporates the proven approach of MICRO SWITCH Hall-effect solid state keys coupled to MOS encoding, thus eliminating all moving parts except the key plunger. MOS increases the number of functions the keyboard can perform, while at the same time allowing significant cost reduction by reducing the number of components required.

The "Model 33" array, similar to typewriter keyboards, is familiar to thousands of operators and thus trained touch typists will readily adapt. Every aspect of the keyboard is designed for maximum operator throughput. This includes operating force, key spacing, button shapes, legending, and silent operation. In addition, an electronic two-key rollover is built into the keyboard circuit. It allows the operator to roll keys during "burst speed" typing of familiar words without entering an erroneous code.

The keyboard is encoded with the USASCII code. There are four modes of operation:

Mode 1, unshifted, the code for the characters appearing as the bottom characters on the keytop is generated.

Mode 2, shifted, the code for the characters appearing as the top characters on the keytop is generated.

Mode 3, control, the code for non-printing functions is generated.

Mode 4, control and shift, the code for special non-printing control functions is generated. The code and character assignments are given on page 3.

features

HALL EFFECT SOLID STATE KEYS COUPLED TO MOS ENCODING . . . Gives greater reliability with significant cost reduction.

FAMILIAR "MODEL 33" ARRAY . . . Ideally suited for on-line inquiries.

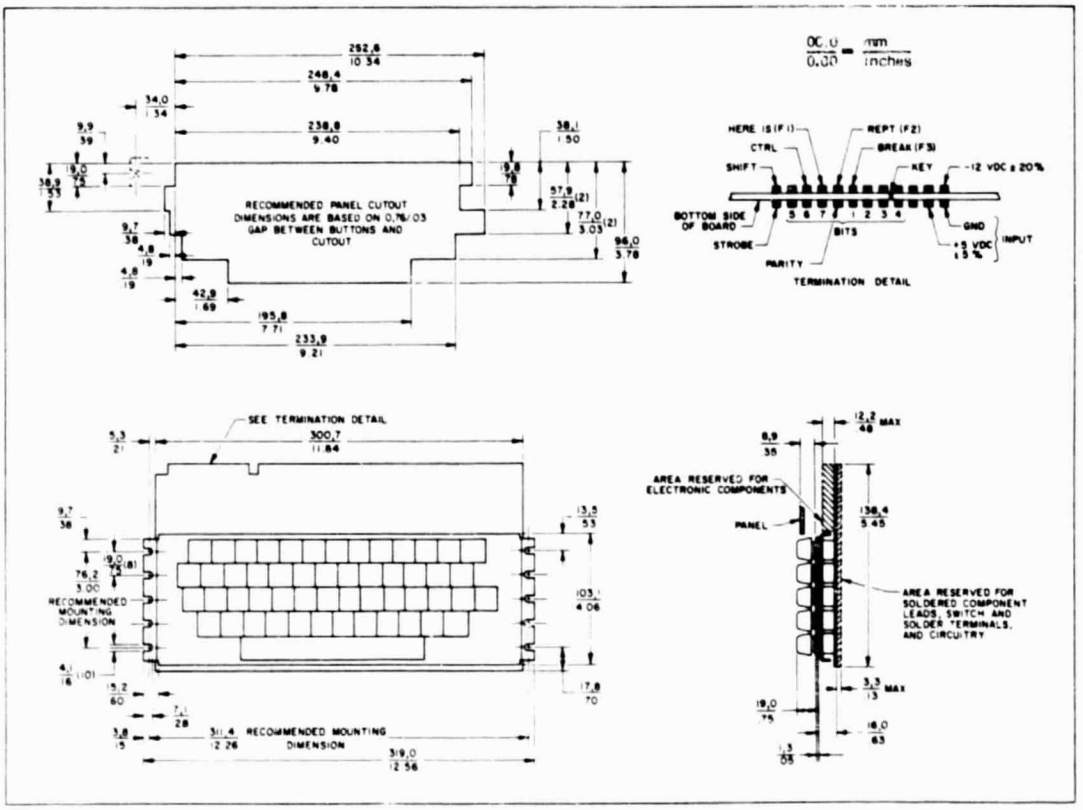
USASCII CODE ASSIGNMENT . . . With four modes of operation.

TWO-KEY ROLLOVER . . . Permits high speed operation.

QUIET OPERATION . . . Only moving part is the key plunger.

MOS ENCODED COMMUNICATIONS SOLID STATE KEYBOARD

MOUNTING DIMENSIONS (For Reference Only)



SPECIFICATIONS

ELECTRICAL DATA

Power Requirements	+5 VDC ±5% @ 500 mA max., 250 mA Typ. −12 VDC ±20% @ 50 mA max., 40 mA Typ. Keyboard Ground @ 0 Volts Note: Tolerances include ripple
Data Key Outputs (Positive Logic)	*Logic "0"*: 0.40 VDC max. @ 16 mA max. (sinking). *Logic "1"*: +2.4 VDC min. @ 400 µA max. (sourcing). Data bits are held in memory until the next key is depressed.*
Function Key Outputs	*Key Operated: 0.4 VDC max. @ 8 mA max. (sinking)* *Key Unoperated: 2.4 VDC min. @ 200 uA max. (sourcing)* F1 = HERE IS (Station 17) F2 = REPT (Station 56) F3 = BREAK (Station 57)
STROBE	(DC Level Strobe will go to a logic "1" .5 microseconds minimum after data bits are stable.

TERMINATION

Card edge output with gold plated terminals accepts standard connectors such as: Cinch 251-12-30-160 with Type II Key. (No connector is furnished with this listing.)

BUTTONS

MICRO SWITCH double-shot molded truncated buttons, medium gray with white legends for touch typing keys and dark gray with white legends for all control and function keys. All buttons have a matte finish.

KEY ROW OFFSET

3/8 – 3/16 – 3/8 inch

KEY SPACING

Keys spaced 3/4 inch center-to-center

BUTTON ORIENTATION

Sloped

WEIGHT

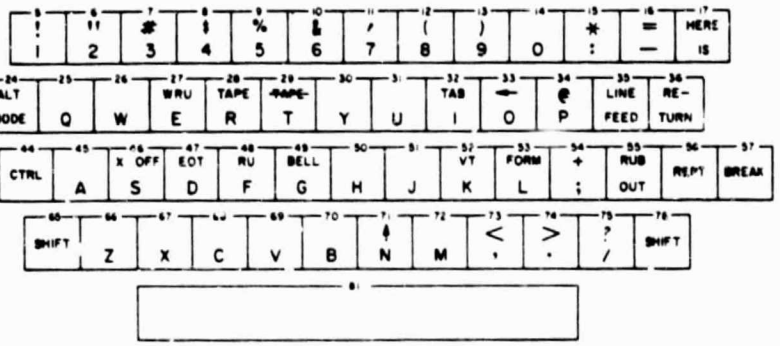
With Enclosure and Connector: 7.5 lbs. Approx. (53SD5-1)
Without Enclosure and No Connector: 1.75 lbs. Approx. (53SD5-2)

*Bit 7 is always latched in Modes 1 and 2. Bit 7 will be latched in Modes 3 and 4 for keys 25 thru 34 and 46 thru 53 only while the Control key (44) is held depressed.

MOS ENCODED COMMUNICATIONS SOLID STATE KEYBOARD

product sheet 53SD5-2

CHARACTER ASSIGNMENT



KEY NO.	MODE 1				MODE 2				MODE 3				MODE 4			
	CHAR.	P	765	4321	CHAR.	P	765	4321	CHAR.	P	765	4321	CHAR.	P	765	4321
5	1	0	011	0001	!	1	010	0001	1	0	011	0001	!	1	010	0001
6	2	0	011	0010	"	1	010	0010	2	0	011	0010	"	1	010	0010
7	3	1	011	0011	#	0	010	0011	3	1	011	0011	#	0	010	0011
8	4	0	011	0100	$	1	010	0100	4	0	011	0100	$	1	010	0100
9	5	1	011	0101	%	0	010	0101	5	1	011	0101	%	0	010	0101
10	6	1	011	0110	&	0	010	0110	6	1	011	0110	&	0	010	0110
11	7	0	011	0111	'	1	010	0111	7	0	011	0111	'	1	010	0111
12	8	0	011	1000	(	1	010	1000	8	0	011	1000	(	1	010	1000
13	9	1	011	1001	)	0	010	1001	9	1	011	1001	)	0	010	1001
14	@	1	011	0000	@	1	011	0000	@	1	011	0000	@	1	011	0000
15	:	1	011	1010	*	0	010	1010	:	1	011	1010	*	0	010	1010
16	-	1	010	1101	=	0	011	1101	-	1	010	1101	=	0	011	1101
17	(F1) FUNCTION OUTPUT															
24	)	1	111	1101	)	1	111	1101	)	1	111	1101	)	1	111	1101
25	Q	0	101	0001	Q	0	101	0001	DC1	1	001	0001	DC1	1	001	0001
26	W	0	101	0111	W	0	101	0111	ETB	1	001	0111	ETB	1	001	0111
27	E	0	100	0101	E	0	100	0101	ENQ	1	000	0101	ENQ	1	000	0101
28	R	0	101	0010	R	0	101	0010	DC2	1	001	0010	DC2	1	001	0010
29	T	0	101	0100	T	0	101	0100	DC4	1	001	0100	DC4	1	001	0100
30	Y	1	101	1001	Y	1	101	1001	EM	0	001	1001	EM	0	001	1001
31	U	1	101	0101	U	1	101	0101	NAK	0	001	0101	NAK	0	001	0101
32	I	0	100	1001	I	0	100	1001	HT	1	000	1001	HT	1	000	1001
33	O	0	100	1111	_	1	101	1111	SI	1	000	1111	US	0	001	1111
34	P	1	101	0000	@	0	100	0000	DLE	0	001	0000	NUL	1	000	0000
35	LF	1	000	1010	LF	1	000	1010	LF	1	000	1010	LF	1	000	1010
36	CR	0	000	1101	CR	0	000	1101	CR	0	000	1101	CR	0	000	1101
44	CTRL (MODE SELECTION KEY)															
45	A	1	100	0001	A	1	100	0001	SOH	0	000	0001	SOH	0	000	0001
46	S	1	101	0011	S	1	101	0011	DC3	0	001	0011	DC3	0	001	0011
47	D	1	100	0100	D	1	100	0100	EOT	0	000	0100	EOT	0	000	0100
48	F	0	100	0110	F	0	100	0110	ACK	1	000	0110	ACK	1	000	0110
49	G	1	100	0111	G	1	100	0111	BEL	0	000	0111	BEL	0	000	0111
50	H	1	100	1000	H	1	100	1000	BS	0	000	1000	BS	0	000	1000
51	J	0	100	1010	J	0	100	1010	LF	1	000	1010	LF	1	000	1010
52	K	1	100	1011	[	0	101	1011	VT	0	000	1011	ESC	1	001	1011
53	L	0	100	1100	\	1	101	1100	FF	1	000	1100	FS	0	001	1100
54	;	0	011	1011	+	1	010	1011	;	0	011	1011	+	1	010	1011
55	DEL	0	111	1111	DEL	0	111	1111	DEL	0	111	1111	DEL	0	111	1111
56	(F2) FUNCTION OUTPUT															
57	(F3) FUNCTION OUTPUT															
65	SHIFT (MODE SELECTION KEY)															
66	Z	1	101	1010	Z	1	101	1010	SUB	0	001	1010	SUB	0	001	1010
67	X	0	101	1000	X	0	101	1000	CAN	1	001	1000	CAN	1	001	1000
68	C	0	100	0011	C	0	100	0011	ETX	1	000	0011	ETX	1	000	0011
69	V	1	101	0110	V	1	101	0110	SYN	0	001	0110	SYN	0	001	0110
70	B	1	100	0010	B	1	100	0010	STX	0	000	0010	STX	0	000	0010
71	N	1	100	1110	^	0	101	1110	SO	0	000	1110	RS	1	001	1110
72	M	1	100	1101	]	0	101	1101	CR	0	000	1101	GS	1	001	1101
73	,	0	010	1100	<	1	011	1100	,	0	010	1100	<	1	011	1100
74	.	1	010	1110	>	0	011	1110	.	1	010	1110	>	0	011	1110
75	/	0	010	1111	?	1	011	1111	/	0	010	1111	?	1	011	1111
76	SHIFT (MODE SELECTION KEY)															
81	SP	0	010	0000	SP	0	010	0000	SP	0	010	0000	SP	0	010	0000

USASCII CODE ASSIGNMENT

MODE SELECTION

SHIFT LINES		
SHIFT	CONTROL	MODE
0	0	1 (Unshifted)
0	1	3 (Control)
1	0	2 (Shift)
1	1	4 (Shift-Control)

Note: The keyboard panel must be electrically tied to system chassis ground to prevent electrostatic damage and noise pickup.

MOS ENCODED COMMUNICATIONS SOLID STATE KEYBOARD

product sheet 53SD5-2

OPTIONS

Additional flexibility has been engineered into the 53SD5-2 design to inexpensively provide the optional features:

1. Key Number 24 (ALT MODE)
   a. Code change to "ESC" – (0011011)
   b. Function key terminating on connector pin "C".
2. Key Number 35 (LINE FEED)
   a. Function key terminating on connector pin "D".
3. Key Number 36 (RETURN)
   a. Function key terminating on connector pin "E".
4. Key Number 55 (RUB OUT)
   a. Function key terminating on connector pin "F".
5. Negative logic for data bits and strobe.
6. Even or odd parity.
7. Tri-shot buttons, with legends in two different colors, may be specified for visual separation of keys that generate control codes.
8. If an enclosure and connector are desired, order catalog listing 53SD5-1.
9. NKRO (N-Key Rollover)

SYSTEM INDICATION AND CONTROL

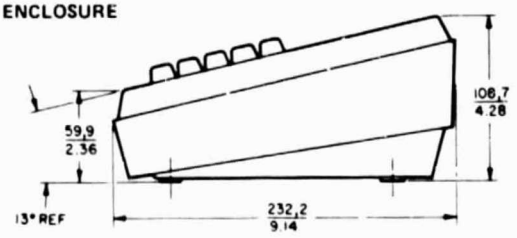
1. Control: The keyboard can be externally shifted between Modes 1 thru 4 by providing an open-collector TTL gate at pin 'N' (Shift) and pin 'L' (Control) of the connector and by supplying the following drive capability:

   Input active, 0.4 VDC max. @ 4.8 mA max. sinking.
   Input inactive, 2.4 VDC min. @ 200μA max. leakage.

2. Indication: The shift and control lines can also be used as mode identification to your system. These outputs are TTL compatable and capable of driving the following load:

   Mode active, 0.4 VDC max. @ 3.2 mA max. sinking.
   Mode inactive, 2.4 VDC min. @ 200μA max. leakage.

ENCLOSURE



As an option MICRO SWITCH offers an enclosure and connector as illustrated in the dimension drawing. The cover is dark gray high strength ABS and the base is light gray cast aluminum alloy. If an enclosure is needed order catalog listing 53SD5-1.

ORDERING INFORMATION

MICRO SWITCH field engineers in branch offices throughout the United States and Canada are ready to work with you in satisfying your keyboard requirements: proper selection, pricing and delivery scheduling. These keyboard experts will provide sound and practical answers to your needs. If you market or purchase in Europe, MICRO SWITCH provides professional sales-engineering service in key European cities.

While we provide application assistance on all MICRO SWITCH products, personally and through our literature, it is up to the customer to determine the suitability of the product in his application.

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