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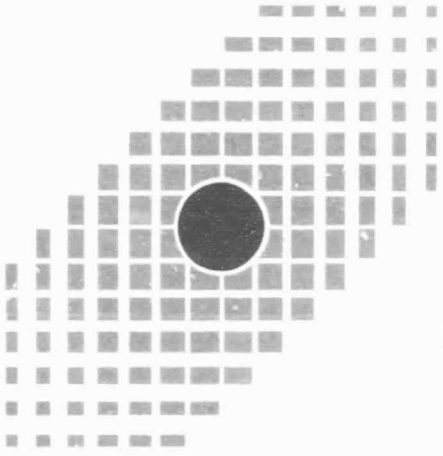

RESEARCH ON DESIGN FEASIBILITY OF HIGH-POWER LIGHT-WEIGHT DC-TO-DC CONVERTERS FOR SPACE POWER APPLICATIONS

Ninth Semiannual Status Report
November 30, 1981

Prepared for

National Aeronautics and Space Administration
Lewis Research Center
Research Grant No. NSG-3157

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Durham, N.C. 27706

Thomas G. Wilson, P.I.

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1. BACKGROUND

The size and weight of the central power-processing systems for spacecraft applications has been an ongoing concern from the systems design standpoint which has grown with the increasing requirements in power-processing capability anticipated for future large spacecraft. Such spacecraft will require compact and lightweight power systems capable of supplying regulated high-voltage outputs to loads which range into the hundreds of kilowatts. In anticipation of these future power system requirements, research into the design feasibility of high-power light-weight dc-to-dc converters for space power applications was initiated by personnel in the Department of Electrical Engineering at Duke University on July 1, 1977.

The original design goal of this research called for the development of a 10-kW module capable of parallel operation with nine other such modules to form a 100-kW system. Each module would provide regulated outputs of +400 V and -400 V dc with respect to the neutral of a three-wire distribution system. Research has progressed in stages at progressively higher power levels as allowed by the limits of currently-available device technologies, and our understanding of the complex interactions involved. Current focus is on the development of a single-output 250-V 2.5-kW power stage with an input voltage operating range of 110 to 180 V dc.

A system design constraint which has been maintained throughout the course of this research has been the selection of 100 kHz as the switching frequency of the converter, intended for the purpose of effecting a size and weight reduction in the converter energy-storage elements. This selection of a 100-kHz conversion frequency, in combination with the high-voltage and high-power operating requirements of the system, has tested the limits of current component technologies, particularly in the area of semiconductor power

devices. The efficient and reliable operation of power semiconductors in a high-stress environment such as the current circuit application presents a complex and formidable design problem. It is precisely the study of this problem, including the circuit phenomena which affect the operation of the converter power semiconductors, which is the primary focus of our research efforts at this time.

2. PERSONNEL

During the period covered by this report, the following personnel were associated with the research project:

Faculty: Dr. Thomas G. Wilson, Principal Investigator; Dr. Harry A. Owen, Jr., Associate Investigator; and Dr. Rhett T. George, Jr., all part-time.

Graduate Research Assistants: Mr. Paul M. Wilson, full-time, and Mr. Ronald C. Wong, approximately half-time. Mr. Wilson and Mr. Wong are candidates for the Ph.D. degree in Electrical Engineering.

3. DOCUMENTATION

(1) A paper entitled "Parametric Study of Minimum Reactor Mass in Energy-Storage DC-to-DC Converters," by Ronald C. Wong, Harry A. Owen, Jr., and Thomas G. Wilson, was presented at, and published as a part of the proceedings of, the 1981 Power Electronic Specialists Conference, PESC '81 Record, IEEE Publication 81CH1652-7, pp. 99-111 (June 1981).

(2) A paper entitled "High-Frequency High-Voltage High-Power DC-to-DC Converters," by Thomas G. Wilson, Harry A. Owen, Jr., and Paul M. Wilson, was presented at, and published as a part of the proceedings of, the U.S.-Japan Cooperative Science Seminar on Analysis and Design in Power Electronics held in Kobe, Japan, November 25 through 28, 1981, Analysis and Design in Power Electronics 1981, pp. 89-98 (November 1981).

4. RESEARCH SUMMARY

4.1 Overview

Utilizing knowledge gained from past experience with experimental current-or-voltage step-up dc-to-dc converter power stages operating at output powers up to and in excess of 2 kW, a new experimental current-or-voltage step-up power stage using paralleled bipolar junction transistors (BJTs) as the controlled power switch, was constructed during the current reporting period. The major motivation behind the construction of this new experimental power stage was to improve the circuit layout so as to reduce the effects of stray circuit parasitic inductances resulting from excess circuit lead lengths and circuit loops, and to take advantage of the layout improvements which could be made when some recently-available power components, particularly power diodes and polypropylene filter capacitors, were incorporated into the design.

The new converter layout helped diminish some of the problems associated with parasitic stray inductance, particularly with respect to the semiconductor switch protection circuitry, but it also opened up some new areas for investigation which had not previously surfaced. For example, a preliminary effort was made to examine the relationship between converter series parasitic inductance (which includes both circuit stray inductance and transformer leakage inductance), transistor power dissipation, and overall converter efficiency.

Two types of recently-developed fast-recovery high-voltage power diodes were made available to project personnel in quantities sufficient for research purposes, and the suitability of each diode with respect to the present design requirements was examined.

Work continues to focus on the protection circuitry associated with the

power transistor and the power diode which is necessary for efficient and reliable converter operation. It is hoped that the outcome of this work will provide information which will enable the circuit desginer to select protection circuitry components so as to maximize overall converter efficiency while maintaining a high degree of reliability.

Finally, closed-form analytical solutions for minimum reactor mass, which were previously developed for a two-winding current-or-voltage step-up converter, have also been derived for three other commonly-used energy-storage dc-to-dc converters -- the voltage step-up (boost) converter, the current step-up buck) converter, and the single-winding current-or-voltage step-up (buck-boost) converter. In addition, work has begun which has as its objective the minimization of overall converter power loss with respect to the design of the energy-storage reactor and the converter switching frequency.

4.2 Power Diode Investigations

As mentioned in the Eighth Semiannual Status Report (May 31, 1981), there is a clear need in the case of the present application for very-fast-recovery power diodes with breakdown voltages in the range of 800 to 1200 V. High-voltage devices with the required reverse-recovery times were unavailable to project personnel prior to the current reporting period; therefore, instead of using a single higher-voltage device, two lower-voltage devices (Motorola type MR1386) were connected in series to form the secondary-circuit power switch.

This series arrangement has at least two distinct disadvantages. One, the two diodes must be closely matched both statically and dynamically under reverse-bias conditions in order to insure reliable operation. Two, the added power loss due to the forward voltage drop of the second diode results in decreased converter efficiency as well as possible additional heatsinking and/or layout complications.

During the current reporting period, two different power diodes were evaluated with respect to their suitability as the secondary-circuit power switch. The first device evaluated was the fast-recovery high-voltage diode developed by the Power Transistor Company (PTC) under NASA contract NAS3-22539, samples of which were supplied to Duke University by NASA Lewis Research Center personnel. The second device evaluated was the Semicon Corporation type SUES 810 power diode, samples of which were supplied to research personnel at Duke University by the manufacturer. The specifications for the Semicon 800-series diodes are included in Appendix A.

Fig. 1(a) and (b) are oscillograms showing the secondary-circuit diode current during the reverse-recovery period for a single PTC diode and a single Semicon diode, respectively. The schematic diagram for the converter circuit which was used to test the two diodes is shown in Fig. 1(c). The two oscillograms were taken under approximately identical circuit operating conditions, which are given in Table 1. No protection circuitry, such as a voltage clamp or snubber, was used in conjunction with the diode under test in either case. In addition, because the PTC diode was only available as a reverse-polarity (anode-case) device, the Semicon diode used in the comparison was also of the reverse-polarity type, so that for the experimental comparison one diode could be simply substituted for the other, therefore eliminating the possibility of circuit layout effects fouling the results of the comparison.

Note from Fig. 1 that the peak reverse current for the PTC diode is nearly twice as large in magnitude as that for the Semicon diode, and that there is a large difference in the time duration of the reverse-recovery transient. Because of the large reverse-recovery current transient associated with the PTC diode, the device appears to be unsuitable for the present application. Present plans are to use a single Semicon type SUES 810 diode as

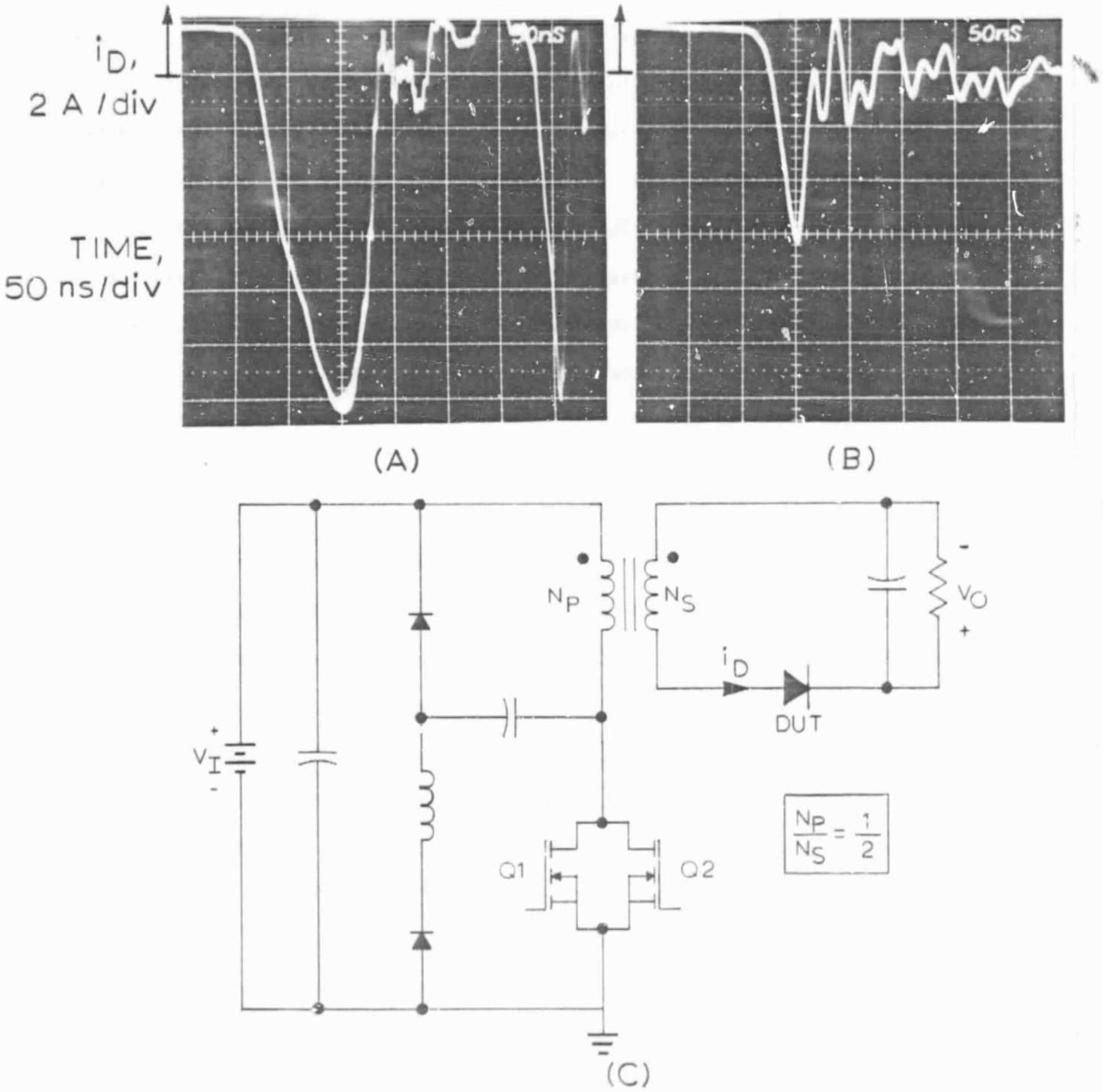


Fig. 1. (a) and (b): Oscillograms of diode current i_D versus time during the diode reverse-recovery transient for the PTC and Semicon SUES 810 power diodes, respectively, with scale factors as indicated. (c): Schematic diagram of the converter test circuit used for experimental comparison of the two types of power diodes.

Table 1. Converter Operating Conditions Corresponding to Figure 1

Controlled power switch: Two IRF350 MOSFETs in parallel.

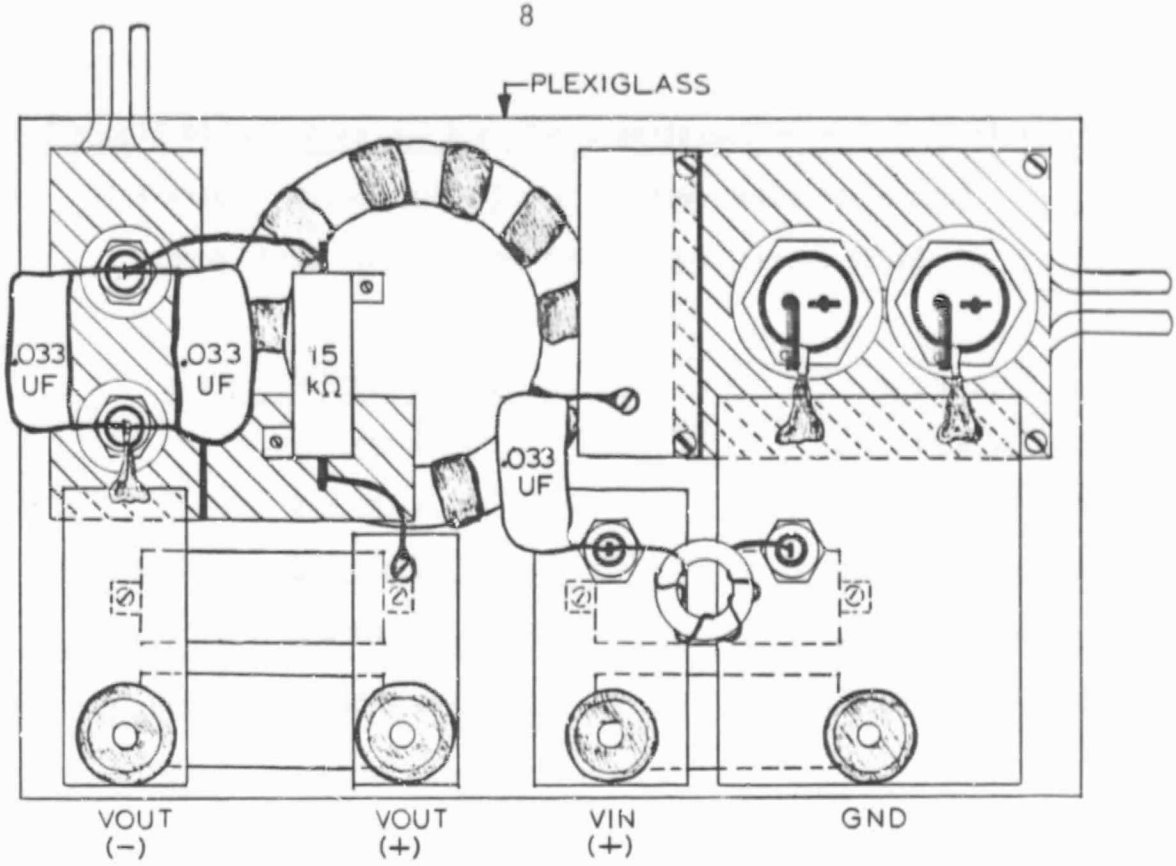
Diode overvoltage protection circuitry used: None.

PTC diode	Semicon SUES 810 diode
V_I = 123.1 V	V_I = 122.0 V
V_O = 152.2 V	V_O = 153.0 V
P_I = 600.5 W	P_I = 571.6 W
P_O = 503.6 W	P_O = 503.4 W
Eff. = 83.9 %	Eff. = 88.1 %

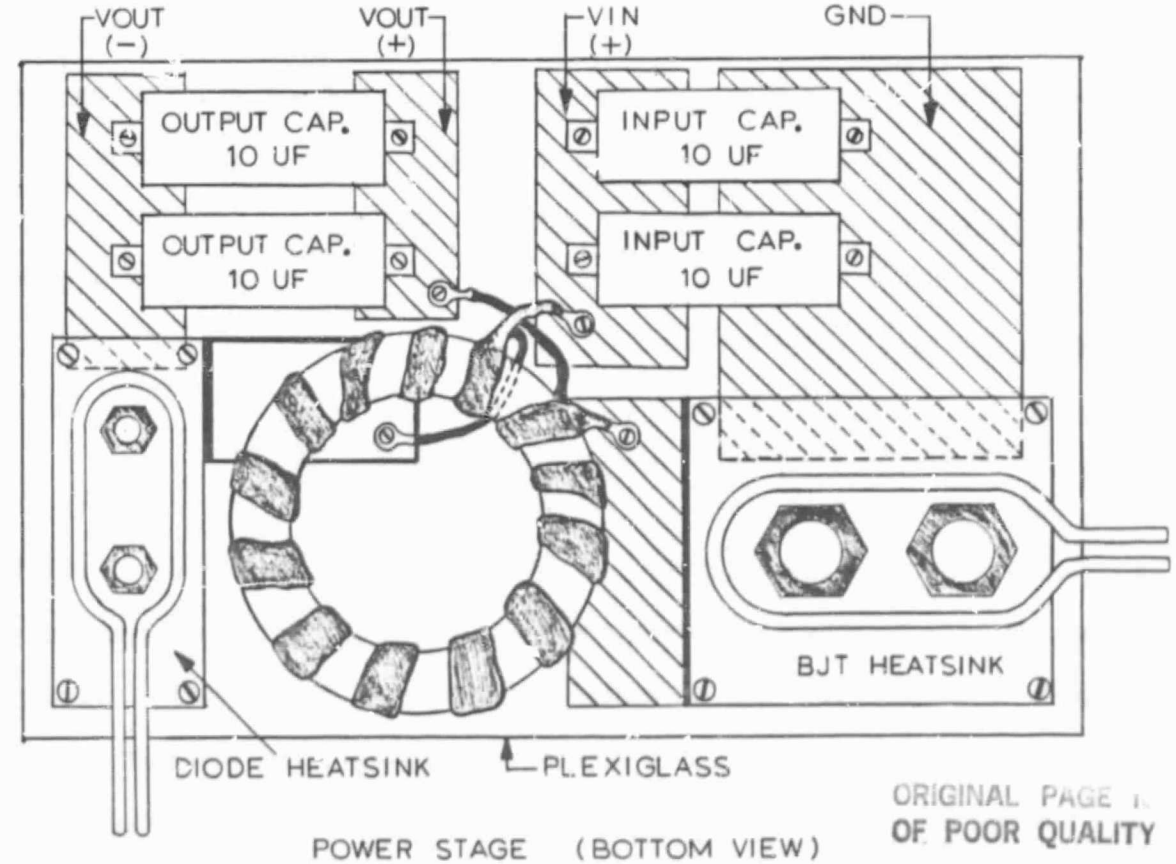
the secondary-circuit power switch until a device with a higher reverse-voltage rating but with a similar reverse-recovery time becomes available to project personnel. The Semicon SUES 811, the specifications of which are also included in Appendix A, should become available in sample quantities in 1982, according to sources at Semicon Corporation. The Semicon SUES 811 possesses a reverse breakdown-voltage rating of 1000 V, whereas the SUES 810 has a breakdown-voltage rating of 800 V.

4.3. Fabrication of New Experimental BJT Converter Layout

During the current reporting period, a new experimental converter layout was fabricated with the objective of minimizing the size of critical circuit loops and lead lengths to alleviate some of the problems associated with stray circuit inductances. The converter layout, many of the major features of which are depicted in Fig. 2, is mounted on a plexiglass plate which sits on an aluminum chassis, with wide copper strips serving as power-component



POWER STAGE (TOP VIEW)



POWER STAGE (BOTTOM VIEW)

Fig. 2. Top and bottom views of the new experimental BJT converter layout. The top edge of the upper figure (top view) corresponds to the bottom edge of the lower figure (bottom view).

interconnections. A fan mounted on the underside of the chassis provides cooling for components inside the chassis (principally the energy-storage reactor and filter capacitors), and separate water-cooled heat sinks provide cooling for both the power transistors and the secondary-circuit power diode. A voltage-clamp circuit, similar to the one shown in Fig. 7 of the Eighth Semiannual Status Report, is used in conjunction with the secondary-circuit power diode to provide a means for limiting the reverse voltage across the power diode. The power diode and the voltage-clamp diode are of opposite polarities to permit the mounting of both diodes on the same heat sink. This arrangement then results in a minimum voltage-clamp/power-diode circuit loop. The input and output filter capacitances are each made up of two parallel Sprague Type 735P 10-μF 400-V capacitors (metallized polypropylene). The energy-storage reactor is of the coaxially-wound type with a turn ratio $N_p:N_s$ of 1:2 on a 125 μ molypermalloy powder core, Arnold Engineering number A-127259 (See Seventh Semiannual Status Report, November 30, 1980).

The converter uses two International Rectifier HPT545 BJTs connected in parallel for the primary circuit active power switch, and employs both an LC-type and an actively-switched RC-type transistor turn-off snubber (See Sixth Semiannual Status Report, May 31, 1980). Bipolar junction transistors were selected for the new converter layout because fewer devices were required to be connected in parallel to achieve the 2.5-kW output-power design goal than was the case with metal-oxide semiconductor field effect transistors (MOSFETs).

Evaluation and testing of the new BJT-switched power stage is not yet complete. As expected, the improved layout resulted in lower magnitudes of parasitic inductance with a corresponding reduction in deleterious effects caused by parasitic inductances. On the other hand, some unexpected results

appeared in conjunction with the testing of the new power stage, and these results are discussed in the next sections.

As a final note concerning the new converter layout, one of the disadvantages which results from improving the circuit layout is that because of short lead lengths and the close spacing of the circuit components, many circuit measurements, particularly current measurements using a current probe, become inaccessible or nearly so. For this reason, a version of a MOSFET-switched converter, capable of delivering up to 1 kW and more of output power, was retained for experimental verification purposes. This version of an experimental MOSFET-switched converter provides similar conditions to the new BJT-switched converter for examining many circuit-related phenomena, yet retains the accessibility for making many critical circuit measurements. Thus, where the presence or absence of circuit-layout-related phenomena is not critical, the MOSFET-switched converter serves as a proving ground for new circuitry, components, and parameter-variation experiments.

4.4 Baker-Clamp Circuit Investigations

Previous efforts to promote equal current-sharing between two BJTs connected in parallel consisted of carefully matching both the static and dynamic characteristics of the devices under consideration. Although this procedure is by no means optimum, it did provide the means for exploring phenomena associated with converter operation at output-power levels up to 2 kW and higher. Just prior to the completion of the construction of the new converter layout, a base-drive power supply associated with the old BJT-switched converter failed, precipitating the failure of one device out of a well-matched pair of BJTs, and prompting the immediate changeover to the new converter layout.

Out of the small remaining selection of International Rectifier HPT545 BJTs available to project personnel, it was not possible to obtain good current sharing, particularly at transistor turn-OFF, between any pair of devices by parameter matching alone. The major source of the current-sharing problem was not due to differences in transistor switching times or to differences in transistor ON-resistances, but to differences in transistor storage times. In an effort to try to minimize differences in storage times, the circuitry identified in Fig. 3, commonly referred to as a Baker clamp, was implemented. This circuit had been previously employed in conjunction with the use of a slower BJT (See Fifth Semiannual Status Report, November 30, 1979). At that time, a large low-frequency oscillation superimposed on the regular switching waveforms resulted when the converter was operated in the continuous-conduction mode.

In conjunction with the use of the Baker clamp with the HPT545, the problem of oscillations again surfaced under certain circuit operating conditions. In order to understand the circumstances under which the oscillations occur, refer again to Fig. 3. The input filter shown in Fig. 3, which is used not only to reduce the amount of 100-kHz switching ripple introduced back into the 60-Hz power source through the input power supply, but to provide additional filtering of the power supply output voltage, consists of an inductance L_1 and a 2900 μF electrolytic capacitor C_1. Simply for convenience because it was available, L_1 is the primary inductance of a 5-KVA 60-Hz transformer. As shown, capacitor C1 is in parallel with the pair of 10-μF capacitors designed to form the converter input filter capacitance. The location of L_1 and C_1 is in close proximity to the output terminals of the input power supply, some distance away from the pair of parallel 10-μF capacitors which are located at the converter input terminal connections. The Baker-clamp circuit, as

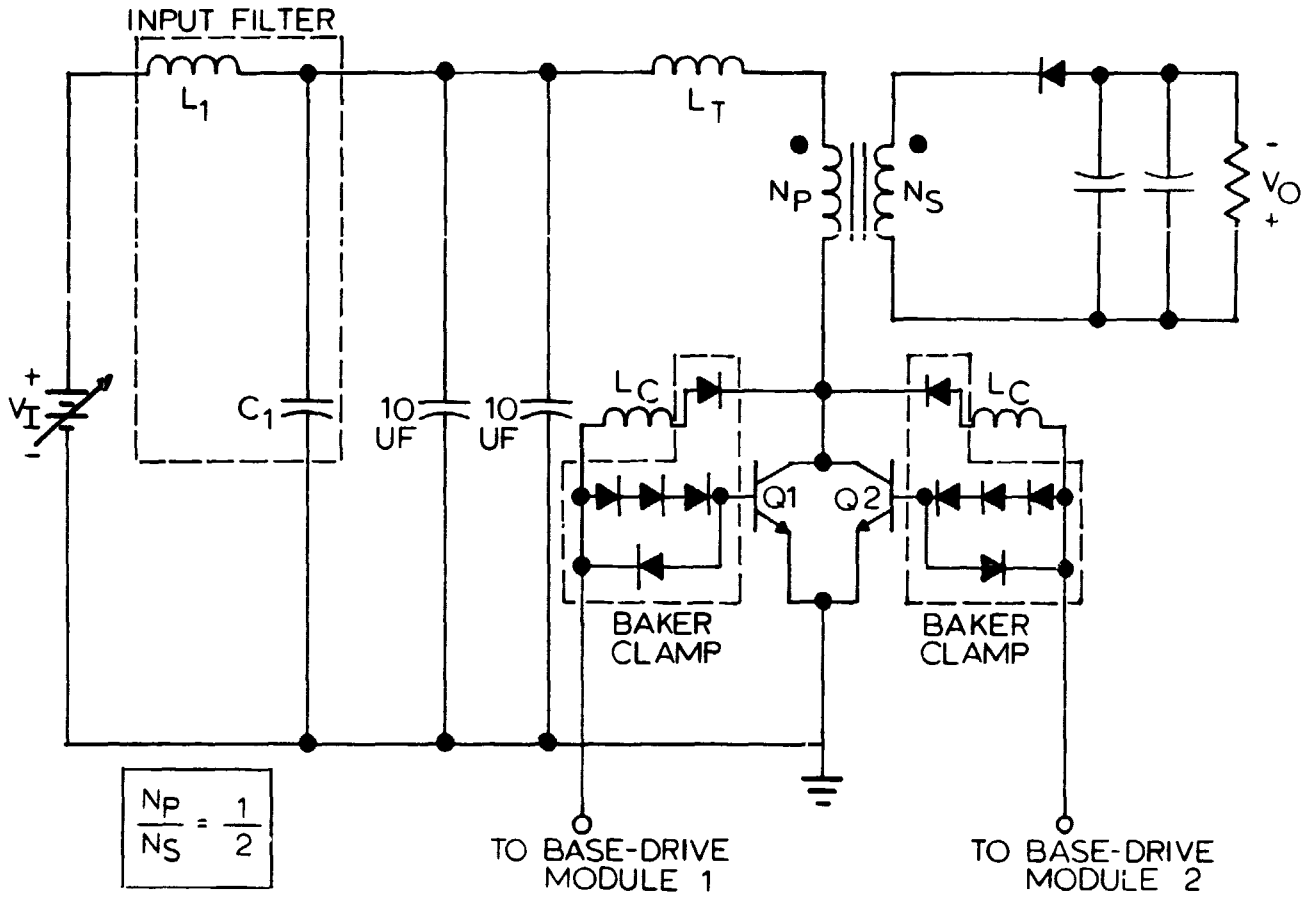


Fig. 3. Schematic diagram of the two-BJT converter showing input filter, Baker-clamp circuits, and inductances L_T and L_C.

depicted in Fig. 3, can assume different forms, where as many as three or more diodes, or as few as zero, may be connected between each transistor base and the transistor base-drives. Experimental versions of the circuit were implemented with zero, one, two, and three series Baker-clamp base diodes. As the number of series Baker-clamp base diodes is increased, the transistors operate further into the active region during the ON-time of the transistors, accompanied by a corresponding decrease in the amount of charge stored in the base-collector junctions and in a decrease in the duration of the transistor storage times. Thus, as the number of Baker-clamp base diodes is increased, the

storage times of the two transistors are decreased. The idea, in the present instance, is to minimize the difference in storage times between the two transistors by minimizing the storage time of each of the two devices. The relationship between the number of Baker-clamp base diodes and the equalization of transistor storage times will be discussed later in this section.

Finally, two inductances which relate to the oscillation problem are depicted in Fig. 3. The first, designated L_T, normally consists of transformer leakage inductance and stray circuit inductance. For experimental purposes, L_T can be increased in a discrete manner, which in this case consists of adding a one-turn reactor in the form of a small toroidal molypermalloy powder core in series with the power transistor. The second inductance, designated L_C, is connected in series with the Baker-clamp collector diode, and although L_C affects the operation of the Baker-clamp circuit, this element is not considered a part of the Baker clamp. Ferrite beads of various sizes and permeabilities were used for L_C.

All of the above elements are in some way related to the presence or absence of the oscillation, and if present, to the converter output-power level at which the oscillation begins to occur. No explanation for the cause of the oscillation is being offered, since we do not at the present time fully understand all of the interactions taking place. Our limited objective for the present is to summarize the circumstances under which the oscillation problem was encountered, as well as to provide information which may help to circumvent the oscillation problem.

The following data summarizes the experimental observations which were made with respect to the oscillation which occurred when the Baker clamp was used in conjunction with the International Rectifier HPT545 BJT. In describing how a particular circuit change affects the oscillation, the terms detri-

mental and beneficial will be used. Since the converter was run open-loop in the continuous-mmf mode with a fixed load resistance, and with a fixed input voltage, except where appropriate for examining the influence of input voltage on the oscillation problem, the converter output-power level was varied by changing the transistor duty-cycle via a pulse generator. The output-power level at which the onset of the oscillation began was dependent on the particular circuit conditions and parameters. A beneficial circuit change will then be defined as a circuit change for which, all else being equal, it was possible to achieve a higher converter output-power level immediately prior to the onset of the oscillation than was possible before the change was made. Conversely, a detrimental circuit change will be defined as a change for which it was not possible to achieve as high an output-power level immediately prior to the onset of the oscillation as was possible before the change was made. With these definitions, the following statements can be made concerning the oscillation problem:

(1) The oscillation appeared as a low-frequency sinusoid (approximately 2.5 kHz for all conditions where the output filter capacitance was equal to 20 μF) superimposed on the converter switching waveforms. The frequency of oscillation was independent of converter switching frequency. In fact, the only circuit element which was found to affect the frequency of oscillation was the converter output-filter capacitance, and the effect of a change of this capacitance on the oscillation frequency was nonlinear and unpredictable, although the oscillation frequency did monotonically decrease as the output capacitance was increased. The converter energy-storage reactor was not changed during the course of the experiments, so the relationship between the inductance of the energy-storage reactor and the oscillation frequency is not known.

(2) The input filter element L_1 largely determines the presence or absence of the oscillation at any converter output-power level. If L_1 was bypassed by a short-circuit, the oscillation did not appear under any of the circuit conditions considered. If L_1 was not bypassed by a short-circuit, adding additional capacitance in shunt with the two Sprague 10-μF input capacitors was beneficial in reducing the oscillation problem. In fact, the oscillation problem surfaced only because it was felt that the two 10-μF capacitors would be sufficient for filtering the input voltage to the converter, and that C_1 was unneccessary and could be removed from the circuit. L_1, however, was not also removed in conjunction with the removal of C_1. The point here is that as the source impedance of the input supply to the converter looked more inductive due to the presence of L_1, it became necessary to increase the input capacitance of the converter in order to eliminate the oscillation. The current experimental converter now utilizes both L_1 and C_1 as an input filter, since it has been learned that the converter does otherwise contaminate the 60-Hz power line via the input power supply with 100-kHz noise.

(3) Under the condition where the large inductance L_1 is present, but where C_1 has been removed, the circuit will begin to oscillate at some converter output-power level. Under these conditions, circuit changes which were found to be <u>beneficial</u> are as follows:

(a) Increasing the effective magnitude of parasitic inductance by increasing L_T;

(b) Increasing the inductance L_C in series with the Baker clamp collector diode;

(c) Increasing the forward base-drive current level; and

(d) Increasing the converter input-filter capacitance.

(4) Under the conditions in (3), the following circuit changes were found to be detrimental:

(a) Increasing the converter input voltage;

(b) Increasing the number of Baker-clamp base diodes; and

(c) Increasing the converter output-filter capacitance.

In summary, the oscillation associated with the use of the Baker clamp may potentially occur when the input to the converter is very inductive. From there, any circuit parameter change which causes the power transistors to operate further into the active region during the transistor ON-time or to operate in the active region for a longer period of time, particularly during the transistor turn-ON switching interval, will enhance the possibility of oscillation. Conversely, any circuit-parameter change which causes the power transistors to operate for shorter durations of time in the active region increases the likelihood of stable converter operation.

Turning now to the original problem of dynamic and static current imbalance between two BJTs connected in parallel, it has been suggested in the literature that the use of the Baker clamp is a viable method for promoting current sharing between two transistors during the transistor turn-OFF interval [1]. So far, the experimental work with the Baker-clamp circuit has not borne out this theory, and for a very simple reason. The typical experimentally-observed storage-times of the HPT545 BJT range between 1 and 2 μsec. The use of the Baker-clamp circuit in conjunction with the HPT545 can reduce the experimentally-observed storage times to between 200 and 500 nsec, depending on the number of Baker-clamp base diodes used, the circuit operating conditions, and the particular dynamic characteristics of the devices under test. The collector-current fall-time of the HPT545 at transistor turn-off, however, is typically less than 120 nsec. The result is that even

though use of the Baker-clamp circuit can reduce transistor storage times by an order of magnitude or more, the resulting storage times of the two devices connected in parallel are of the same magnitude or greater than the respective collector-current fall-times. The difference between the two transistor storage times may then be of the same magnitude as the collector-current fall-times, resulting in large transistor current imbalances at transistor turn-OFF. The practicality of the situation is that unless storage-times, and therefore differences in storage-times, can be reduced to the point where these time intervals are small with respect to transistor collector-current fall-times, there is little advantage to the use of the Baker clamp to solve the problem of dynamic current sharing at transistor turn-OFF.

Furthermore, just as the number of Baker-clamp base diodes determines the duration of the transistor storage-time interval, so do the static characteristics of the Baker-clamp collector and base diodes. Small differences in the dc current-vs-voltage characteristics of the Baker-clamp diodes result in significant differences in the amount of charge stored in the two transistors, with corresponding differences in the storage times of the two devices. This problem is further complicated by the variation of the current-vs-voltage characteristics of the Baker-clamp diodes with temperature. As a result, the use of the Baker-clamp circuit with unmatched Baker-clamp diodes may make a difficult situation worse by further increasing the difference in storage-times of two transistors connected in parallel.

The current two-BJT experimental converter uses a Baker-clamp circuit associated with each BJT. Each clamp circuit has a single diode connected between each transistor base and the common collector connection. Versions of the Baker-clamp circuit often appear in the literature with only a single base-to-collector diode which is shared by both transistors, eliminating the

possibility of variations in the characteristics of this particular circuit element causing transistor current-sharing problems. This scheme requires that the two transistor base-circuit connections be made common at the anode side of the Baker-clamp collector diode, which eliminates the advantage of using separate base-drive modules for the purpose of providing equal transistor base currents (see Seventh Semiannual Status Report, Nov. 30, 1980). The current Baker-clamp circuit does not use any base diodes; consequently, the transistor storage times are reduced but not minimized.

In the above arrangement, the Baker-clamp collector diodes serve to compensate for, rather than to eliminate, differences in transistor storage times. This process is brought about by first matching as closely as possible the dynamic characteristics of two transistors, and then by selecting through trial and error the particular Baker-clamp collector diodes which further minimize the difference in storage times. So far, this approach has been serviceable in that it has permitted converter operation at output-power levels significantly above 1 kW for the purpose of examining circuit-related phenomena, but the need for a better solution to the problem of transistor current sharing is well recognized by project personnel. During the upcoming report period, the use of a current-sharing transformer, also referred to as a "bucking inductor," in the common emitter connection of two transistors will be examined as a possible solution to the problem of transistor current sharing when two BJTs are connected in parallel [1].

4.5 Effects of Parasitic Inductance on Converter Performance

Many of the problems which have arisen with respect to the present design and implementation of a high-frequency high-voltage high-power current-or-voltage step-up power stage have had as their basis the inevitable presence of parasitic series inductance. Parasitic series inductance is defined here

as any circuit inductance, aside from the energy-storage transformer magnetizing inductance, appearing in series with the converter primary-circuit and secondary-circuit power switches. Normally, parasitic inductance consists of transformer leakage inductance and of stray circuit inductance due to circuit lead lengths and circuit loops, and can be treated as a lumped circuit element which may be referred to either the primary side or to the secondary side of the converter circuit for the purpose of analysis.

During the current reporting period, a paper enumerating the design considerations relating to the presence of significant amounts of parasitic inductance in high-frequency high-voltage high-power converters was prepared and published [2]. To briefly summarize some of the salient points of this paper, the presence of significant amounts of parasitic inductance produces several beneficial as well as detrimental effects on the overall performance of the converter. Some of these effects directly influence the amount of power dissipation within the converter semiconductor power switches, or within the circuitry, such as the transistor turn-OFF snubber, designed to protect the power switch from otherwise potentially catastrophic circuit conditions. Three of the effects relating to parasitic inductance are:

(1) The power dissipation in the power switching transistor during the turn-ON switching interval can be reduced by increasing the effective magnitude of parasitic inductance, either by purposely introducing more transformer leakage inductance through the selection of an appropriate winding technique, or by adding a discrete inductance in series with the power transistor. The latter method is by far the more practical from an experimental point of view, and is similar to the addition of a discrete inductance in the form of a series transistor turn-ON snubber often used in conjunction with nontransformer-isolated circuits.

(2) The presence of parasitic inductance directly influences the power dissipation both in the power switching transistor during the turn-OFF switching interval, and, to a greater extent, in the transistor turn-OFF snubber circuitry. As the magnitude of parasitic inductance increases, so does the power dissipation in these circuit locations.

(3) The power dissipation in the secondary-circuit power diode during the power-diode reverse-recovery transient can be reduced by increasing the effective magnitude of parasitic inductance. Power dissipation in the secondary-circuit power diode protection circuitry, however, will be increased as the effective magnitude of parasitic inductance is increased.

The above effects of parasitic inductance are not totally inseparable, and may be counteractive. For example, because the magnitude of parasitic inductance helps to determine the current and voltage waveshapes of the power transistor during the transistor turn-ON interval, and helps to determine the waveshapes associated the power diode during the diode reverse-recovery transient, these effects become interrelated simply because they occur at the same time.

The overall effects of increasing or decreasing parasitic inductance on converter efficiency are difficult to predict because of the complex nonlinear relationships involved in the dynamics of the semiconductor power switches. However, it is interesting to note that even in a transformer-coupled converter topology which will necessarily contain significant amounts of parasitic inductance, the minimization of parasitic inductance through reactor winding techniques or circuit layout considerations does not necessarily provide for optimum converter efficiency or reliability. This idea surfaced primarily because of the experimental work with the new BJT-switched converter layout. The new converter circuit layout contained significantly less parasitic

inductance than the previous design, and consequently, the problems associated with leakage inductance, transistor turn-OFF, and transistor turn-OFF protection circuitry were far less severe. Transistor power dissipation during the turn-ON interval, on the other hand, was significantly increased. It was then decided to experimentally determine whether an increase in the effective magnitude of parasitic inductance would prove to be beneficial to overall converter performance. The effective magnitude of parasitic inductance was increased by introducing a discrete inductance L_T into the primary circuit in the form of a one-turn toroidal core which may or may not be designed to saturate, as depicted in Fig. 4. For the nonsaturating circuit, a small molypermalloy powder core was used; a small supermalloy tape-wound core was used in the case of the saturating circuit. An LC-type snubber has also been included in the circuit diagram of Fig. 4 to indicate that the added inductor L_T should be located in a position such that the energy stored in L_T is absorbed by the LC-type snubber capacitor during the transistor turn-OFF interval. As previously mentioned, the addition of the inductance L_T is similar to the addition of a transistor turn-ON snubber to a nontransformer-coupled circuit topology. Additional discharge circuitry for L_T is unnecessary because of the presence of the LC-type snubber.

The use of a saturable reactor for L_T is a somewhat novel idea which takes advantage of the nonlinearity of such a circuit element. During most of the transistor turn-ON interval, L_T is unsaturated, and due to the high impedance of L_T in this condition, much of the primary-circuit voltage appears across L_T rather than across the power transistor. At some point in time, the primary-circuit current reaches the point where L_T saturates, having stored very little energy in L_T in the process. The fact that a saturable reactor, as opposed to a nonsaturable reactor, stores very little energy is

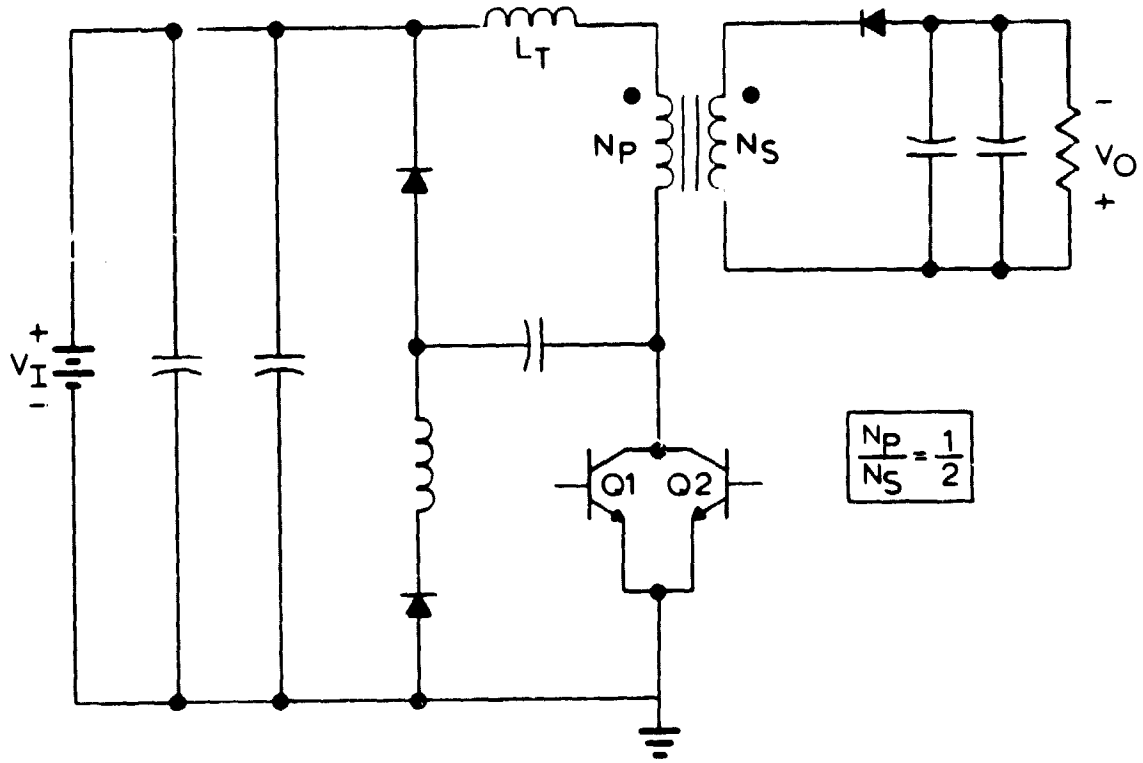


Fig. 4. Schematic diagram of the two-BJT converter showing the location of the inductance L_T (saturating or nonsaturating) with respect to the LC-type snubber.

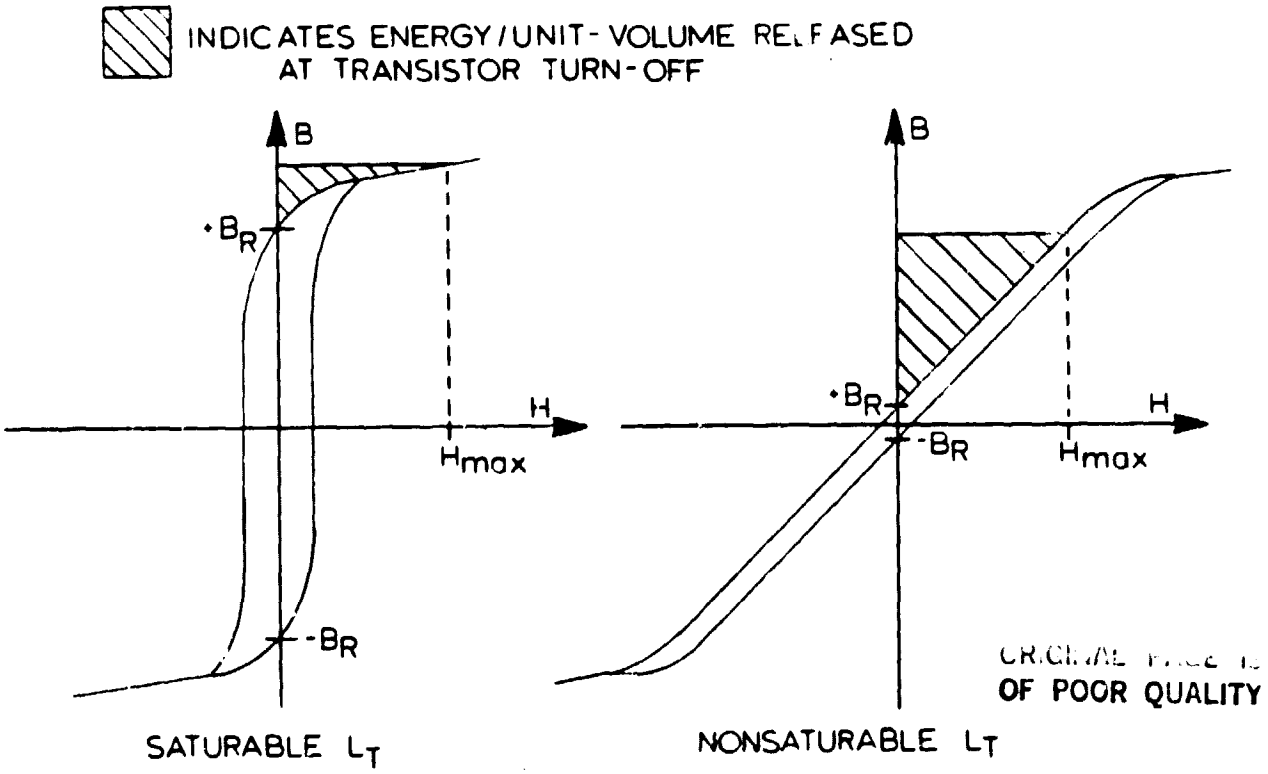


Fig. 5. Illustration of how the choice of magnetic material determines the amount of energy stored in the reactor L_T immediately prior to transistor turn-OFF. Figures are not drawn to scale.

advantageous from the standpoint that whatever energy is stored in L_T must be processed by the LC-type snubber at transistor turn-OFF, adding to the power dissipation in the snubber network. Also, the use of a nonsaturating reactor for L_T will result in a higher voltage overshoot across the power transistor at turn-OFF unless the LC-type snubber capacitance is increased accordingly. The difference in energy stored by the two types of reactors, saturating and nonsaturating, is depicted in Fig. 5.

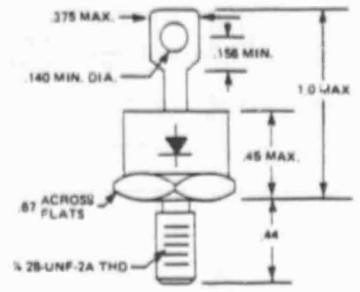
Oscillograms of the two power transistor emitter currents, i_{E1} and i_{E2}, and the common transistor collector-to-emitter voltage v_{CE} are shown in Fig. 6(a), (b), and (c) for similar converter operating conditions, but with three different conditions imposed on the nature of the inductance L_T. Fig. 6(a) is a set of reference oscillograms taken under the condition where no additional inductance has been added to the circuit, i.e., $L_T = 0$. Corresponding oscillograms for the saturable-reactor and nonsaturable-reactor cases are shown in Figs. 6(b) and 6(c), respectively. Circuit operating conditions for the three cases are given in Table 2.

Table 2. Circuit Conditions and Efficiencies Corresponding to Fig. 6

	$L_T = 0$	Saturable L_T	Non-Saturable L_T
V_I :	137.6 V	137.6 V	137.4 V
V_O :	171.5 V	170.7 V	170.7 V
P_I :	1198.5 W	1193.0 W	1193.6 W
P_O :	1065.0 W	1063.5 W	1061.8 W
EFF.:	88.9 %	89.1 %	89.0 %

High Voltage Silicon Very Fast Recovery Rectifiers A1

MECHANICAL DATA



CONFORMS TO JEDEC OUTLINE DO5
ALL DIMENSIONS IN INCHES

NOTES:
- Standard Polarity is Cathode common to case
- Add Suffix LTR "R" for Common Anode

FEATURES

- 35 AMPERES
- LOW V_F
- HIGH SURGE
- LOW LEAKAGE
- P.I.V. TO 1000 VOLTS
- VERY FAST

MAXIMUM RATINGS

I_F (Ave.)	I_{FSM}(Surge) 8.3 mSec-60 Hz	$V_{RM(rep)}$, $V_{RM(wkg)}$, V_R IN VOLTS					Case Style
Amperes	Amperes	500	600	700	800	1000	
35	400	SUES807	SUES808	SUES809	SUES810	SUES811	DO5

ELECTRICAL CHARACTERISTICS

DEVICE CHARACTERISTICS	Symbol	Max. Value	Units
SUES807 thru SUES811			
D.C. Forward Voltage (I_F = 35 Adc, T_C = 25°C, & 125°C, 807 thru 809)	V_F	1.25/1.15	Volts
(I_F = 35 Adc, T_C = 25°C, & 125°C, 810 thru 811)	V_F	1.3/1.2	Volts
D.C. Reverse Current (@ Rated V_R, T_C = 25°C & 150°C, 807 thru 811)	I_R	.10/40	MA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Junction Operating Temp. Range	T_J	-65 to +150	°C
Maximum Storage Temperature Range	T_{STG}	-65 to +175	°C

*SUES807-811 T_{rr} = 50 nsec max, C_j Typ 175 pf @ -10 V
*I_F = 1/2 A, I_R = 1.0 A, I_{REC} = 1/4 A

Semicon INC

SEMICONDUCTOR DEVICES

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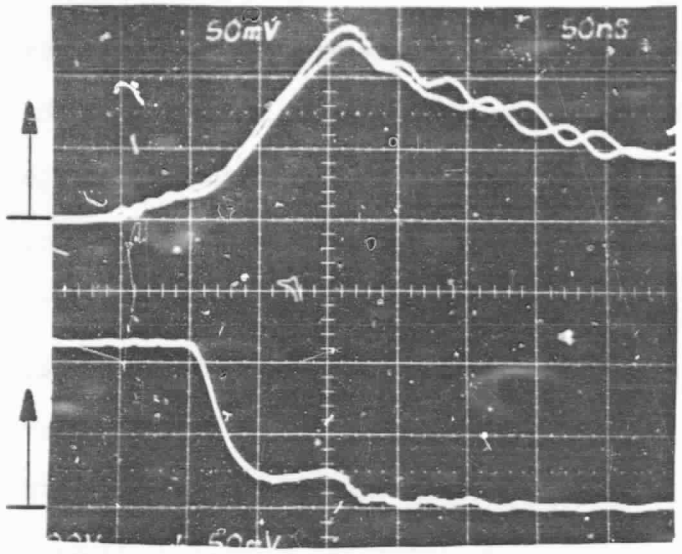
(C) NONSATURABLE L_T

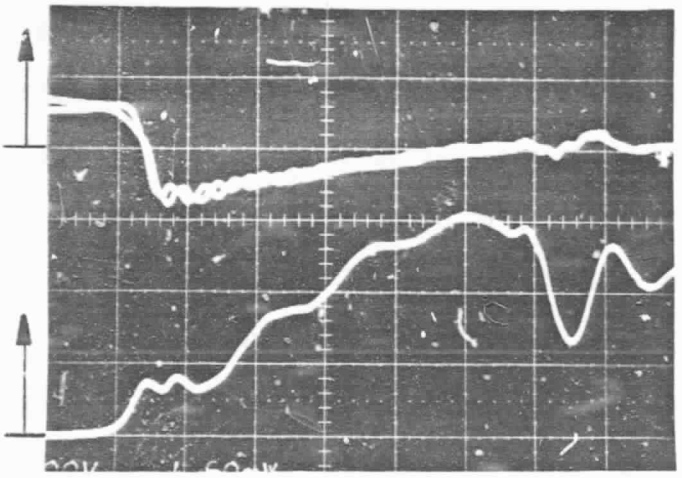


TURN-ON

i_{E1}, i_{E2}: 10 A / div

TIME: 50 ns / div

v_{CE}: 100 V / div

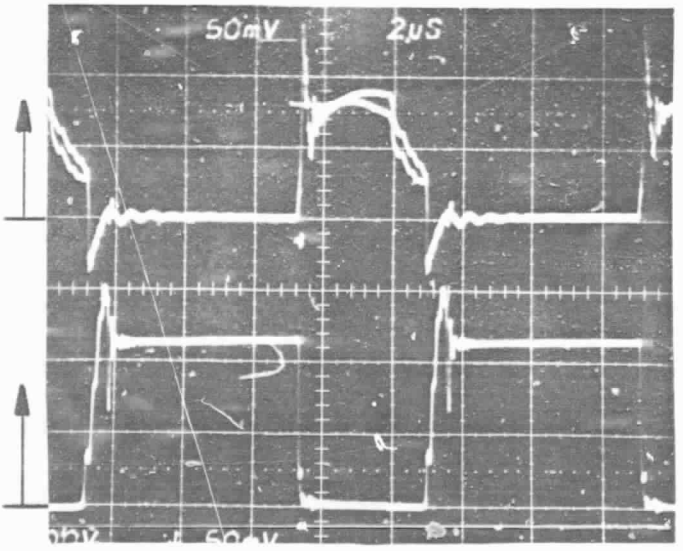


TURN-OFF

i_{E1}, i_{E2}: 10 A / div

TIME: 100 ns / div

v_{CE}: 100 V / div



FULL-CYCLE

i_{E1}, i_{E2}: 10 A / div

TIME: 2 μs / div

v_{CE}: 100 V / div

FIGURE 6, CONT'D.

From Table 2 it can be seen that overall converter efficiency was approximately the same for all three conditions imposed on the nature of the inductance L_T. This fact varies somewhat from the idea that a reduction in the effective magnitude of parasitic inductance, particularly transformer leakage inductance, should be beneficial to overall converter operation. Furthermore, referring to the oscillograms corresponding to the transistor turn-ON interval, it is seen that transistor power dissipation during this interval has been significantly decreased for the two cases where $L_T \neq 0$. On the other hand, referring to the oscillograms coresponding to the transistor turn-OFF interval, the voltage overshoot at transistor turn-OFF is increased slightly for the two cases where $L_T \neq 0$, more so in the case where L_T is nonsaturating.

Of even greater interest is the effect of the saturable reactance on the entire transistor voltage waveshape. Comparing the oscillograms of Fig. 6(a) through (c) for the full-cycle switching waveforms, we see that the oscillatory ringing appearing during the transistor turn-OFF interval has been greatly reduced in the case where L_T is a saturable reactor. The exact mechanism by which L_T becomes reset to $-B_R$ has not yet been fully analyzed from a design point of view, but it would appear that the core is reset by the voltage appearing across L_T during the reverse-recovery period of the LC-type snubber diode D_{S1}. A principal disadvantage of using a saturable reactor for L_T is that the saturable reactor is a very lossy element, and will experience a very large temperature rise.

The use of an additional discrete reactance, saturable or nonsaturable, for improving the waveshapes associated with the principal converter power switches, as well as the effects of this reactance on the converter power-switch protection circuitry is a very interesting topic, as evidenced by the various oscillograms shown in Fig. 6. During the upcoming research period,

this area will be further explored, particularly in conjunction with the on-going research efforts geared towards the protection of the converter semiconductor power switches.

4.6 Design of Transistor Turn-OFF Snubber Capacitor

Work continues to focus on the complex relationships between converter parasitic inductance, the presence of which mandates that snubber and/or clamping networks be used to protect the converter semiconductor power switches from overvoltages, and on the design of these protection circuits, as well as the power losses associated with these circuits. One of the more prominent areas which invites further exploration is the LC-type transistor turn-OFF snubber, a relatively new circuit which has not yet been fully examined in the literature, particularly from the standpoint of the present high-frequency application where the dynamic losses of such a circuit are of significant importance.

The critical circuit element in the design of the LC-type snubber circuit is the snubber capacitor, the size of which has been experimentally found to profoundly affect converter efficiency. As an example, at a converter ouput-power level of approximately 1 kW, quadrupling the size of the LC-type snubber capacitor experimentally reduced converter efficiency by as much as 4 %. As can be seen from Equation (1) below, quadrupling snubber capacitance corresponds to a 50 % reduction in the overshoot voltage associated with the power switching transistor. However, such an increase in snubber capacitance requires that four times as much energy be processed by the LC-type snubber network, which would also include the power switching transistor due to the operation of the LC-type snubber.

Because the proper design of the LC-type snubber capacitance is of utmost importance in maximizing overall converter efficiency, a re-examination of the design guides available in the literature for selecting snubber capacitance was made. It was found that generally there is some information which is lacking in such discussions, and as a result, a preliminary analysis for determining the proper selection of snubber capacitance was begun.

The principal design equation normally used for selecting snubber capacitance, which is applicable to either the RC-type or LC-type transistor turn-OFF snubbers, is

$$C_S = L_{PAR} \left[\frac{I_{PB}}{V_{OS}} \right]^2 ; \qquad (1)$$

where L_{PAR} is the sum total of converter parasitic inductance, taking into account the transformer turn ratio involved; I_{PB} is the peak transistor current immediately prior to transistor turn-OFF; and V_{OS} is the allowable transistor voltage overshoot, equal to the difference V_{PK}-V_{OFF} between the maximum transistor peak voltage V_{PK} and the static transistor OFF-voltage $V_{OFF} = V_I + (N_P/N_S)V_C$.

Normally, information given in the literature either suggests using a maximum value for I_{PB} and a minimum value for V_{OS} corresponding to a maximum value of input voltage V_I, or simply gives little guidance as to the values which should be used when the converter input voltage varies over a wide range. However, in the case of the current-or-voltage step-up converter, maximum values of I_{PB} and V_I do not occur simultaneously over the input voltage operating range for a given converter output-power level, and in fact, occur at opposite ends of the input voltage range.

The analytical investigation initiated during the current reporting period examines the relationship between required snubber capacitance as a function of converter input voltage, in order to determine the values of I_{PB} and V_{OS} which should be used in Equation (1). The analysis, which is straightforward but rather too lengthy for the scope of this report, assumes that the converter is lossless. C_S is determined as a function of a number of circuit variables, including L_{PAR}, P_O, V_I, V_O, V_{PK}, and (N_P/N_S). The partial derivative $\partial C_S/\partial V_I$ is then determined in order to find the converter input voltage requiring the maximum value of C_S, thereby giving the values of V_{OS} and I_{PB} to be used in Equation (1).

For a given set of converter input-output specifications, the determining factor on the proper selection of C_S from this analysis appears to be the peak allowable transistor voltage V_{PK}. Depending on the value of V_{PK}, the partial derivative $\partial C_S/\partial V_I$ derived in this manner will either be:

(1) less than zero, indicating that C_S should be selected using the values of I_{PB} and V_{OS} corresponding to minimum converter input voltage;

(2) greater than zero, indicating that C_S should be selected using the values of I_{PB} and V_{OS} corresponding to maximum converter input voltage; or

(3) equal to zero, indicating that C_S may be selected at any converter input voltage, and for a given converter output-power level (normally maximum for the purpose of selecting C_S), the sum of V_{OFF} and V_{OS} will remain constant over the converter input-voltage range.

The significance of this simple analysis is that by choosing C_S for maximum values of both I_{PB} and V_I, one is overdesigning for a given requirement on peak transistor voltage, leading to decreased converter efficiency because of

unwarranted additional power loss in the snubber circuitry. The amount of overdesign depends on a number of circuit variables, including the range of converter input voltage and the type of transistor turn-OFF snubber used. However, it is safe to say that in the case of the present application, the additional losses incurred by the overdesign of the snubber capacitance is significant enough to warrant attention to this problem, even in the case of the LC-type snubber where it is difficult to obtain an analytical approximation for the power loss resulting from overdesign.

4.7 Analytical Design Considerations for Energy-Storage Reactor

It was reported in the Seventh and Eighth Semiannual Status Reports that the minimum reactor mass for a two-winding current-or-voltage step-up (buck-boost) converter configuration operating under the constant-frequency control law is given by

$$m_{T,min} = K_1 \left(P_{O,max} / f_S \right)^{3/4} \qquad (2)$$

where $m_{T,min}$ is the minimum total reactor mass, $P_{O,max}$ is the maximum output power, and f_S is the switching frequency. K_1 is a proportionality constant dependent upon a set of system parameters which includes, for example, the input voltage, the output voltage, and the maximum allowable flux density for the core material. The design of a minimum-mass reactor under a set of specified system parameters for the two-winding current-or-voltage step-up converter can be obtained from the equations given in [3]. These equations are repeated in Appendix B. Optimization of some other converter or system criteria such as efficiency or total system mass, has also been reported [4,5,6].

In the research period covered by this report, the development of the closed-form analytical minimization of reactor mass was extended to three other commonly-used energy-storage dc-to-dc converters -- the voltage step-up (boost) converter, the current step-up (buck) converter, and the single-winding current-or-voltage step-up (buck-boost) converter. Although the converter topologies are different, the expression for the minimum reactor mass given in (2) is found to be applicable to these three converters as well. The value and the expression for the constant K_1, however, are different from one converter to another. Since K_1 is independent of the maximum output power $P_{O,max}$ and the switching frequency f_S, the validity of (2) implies that the minimum reactor mass for these four commonly-used energy-storage dc-to-dc converters is proportional to the maximum output power raised to the power 3/4 and inversely proportional to the switching frequency raised to the power 3/4.

Besides the minimization of reactor mass, the minimization of the total power loss in a dc-to-dc converter is another design objective that is commonly sought by design engineers. Due to the complicated nature of the various loss models for the semiconductor devices, capacitors, and energy-storage reactors, the derivation of a closed-form solution to the problem of minimizing the total converter power loss appears to be nearly impossible. Consequently, the design problem of minimizing the total converter loss is usually achieved through numerical minimization techniques. Slow convergence and lengthy computation time are, however, inherently associated with the numerical minimization of a constrained problem involving a large number of variables.

The subject of minimization of total converter power loss was re-examined in this research period through a combination of analytical and numerical

minimization procedures. There have been various reports on the minimization of converter loss in the literature [4,6]. These minimization studies are usually carried out numerically due to the complicated loss models for various components. The objective of this re-examination is to minimize the total converter loss with a more efficient approach than that which is available in the literature. Although the number of design variables is large and the nature of the problem is very complex, it was found out that, under certain well-justified assumptions, the total converter loss can be minimized analytically with respect to a subset of the design variables -- core cross-sectional area A, mean magnetic path length ℓ, absolute permeability μ, and number of turns N in the winding. As a result, the minimization is divided into two stages. In the initial stage, the total converter loss is minimized with respect to the aforementioned subset of design variables, incorporating all design constraints associated with the energy-storage reactor. After this initial stage, the four variables A, ℓ, μ, and N are eliminated, and the converter loss is expressed as a function of the remaining design variables. In the final stage, the total converter loss is minimized numerically with respect to these remaining design variables which, for example, include the switching frequency and the critical output power. Not only is the number of design variables in the final stage of minimization reduced, the number of design constraints is also reduced in this stage because the design constraints associated with the energy-storage reactor have been incorporated in the initial stage. Such a combination of analytical and numerical minimization procedures alleviates considerably the problems of slow convergence and lengthy computation time.

5. FUTURE WORK

Throughout the course of this research, an area which has received a great deal of attention with respect to the efficient and reliable operation of high-frequency high-voltage high-power converters has dealt with design considerations for the converter semiconductor power switches, particularly in relation to the circuitry necessary for protecting the semiconductor power switches from the otherwise disastrous circuit conditions resident in the current circuit application. Out of a variety of potential candidates, a subset of semiconductor protection circuits has emerged which appears to be applicable to the present high-frequency high-voltage high-power converter circuit. During the upcoming reporting period, work will continue to focus on the design and analysis of this subset of semiconductor switch protection circuits, with the intention of providing design information geared towards two separate problems. One, where more than one circuit seems potentially applicable to performing a specified task, such as limiting the peak voltage appearing across a power semiconductor, guidelines will be developed for selecting the most power-efficient circuit from among the potential candidates for the range of circuit conditions and parameters most applicable to the present application. Two, where a full understanding of the operation of a given protection circuit is lacking, particularly with respect to the present high-frequency high-voltage high-power application, efforts will be made to fill in the gaps between what information is already available in the literature, and what additional information is necessary for the present application. Closely related to this topic will be work leading to the identification of power losses within the converter circuit, and of circuit parameters affecting the various power losses. In addition, attention will be given to how changes in certain circuit parameters, particularly

parasitic inductance, influence the distribution of power losses within the converter semiconductor power switches and protection circuitry.

Finally, present and past work with respect to the design of the converter energy-storage reactor has dealt with two separate minimization problems. In the first problem, the mass of the energy-storage reactor was minimized for a given set of converter specifications. In the second problem, the design equations for the energy-storage reactor have been sought which would minimize overall converter power loss. It is proposed that during the upcoming reporting period an investigation be conducted into how these two minimization procedures might be combined, so that for a given reactor mass versus converter power-loss trade-off ratio, design equations for the energy-storage reactor resulting in minimum overall power-system mass could be developed.

6. REFERENCES

[1] Marvin W. Smith, "Application of High Power Darlington Transistors," Powerconversion International, Sept./Oct. 1979, pp. 32-40.

[2] Thomas G. Wilson, Harry A. Owen, Jr. and Paul M. Wilson, "High-Frequency High-Voltage, High-Power DC-to-DC Converters," Analysis and Design in Power Electronics 1981, Proceedings of the U.S. - Japan Cooperative Science Seminar on Analysis and Design in Power Electronics, Kobe, Japan, November 1981, pp. 89-98.

[3] Ronald C. Wong, Harry A. Owen, Jr., and Thomas G. Wilson, "Parametric Study of Minimum Reactor Mass in Energy-Storage DC-to-DC Converters," PESC '81 Record, Proceedings of the 1981 Power Electronic Specialists Conference, IEEE Publication 81CH1652-7, June 1981, pp. 99-111.

[4] J.J. Biess, Y. Yu, R.D. Middlebrook, and A.D. Schoenfeld, "Modeling and Analysis of Power Processing Systems," Final Report, NASA CR-134686, July 1974.

[5] F.C. Lee, S. Rahman, R.A. Carter, C.H. Wu, Yuan Yu, and R. Chang, "Modeling and Analysis of Power Processing Systems (MAPPS)," Final Report, Volume I, NASA CR-165538, Aug. 1980.

[6] T.G. Wilson, Jr., E.W. Whelan, Jr., R. Rodriguez, and J.M. Dishman, "DC-to-DC Converter Power-Train Optimization for Maximum Efficiency," PESC '81 Record, Proceedings of the 1981 Power Electronic Specialists Conference, IEEE Publication 81CH1652-7, June 1981, pp. 166-179.

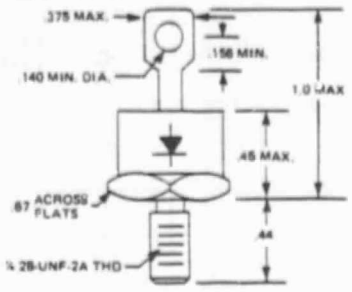
Appendix A

Semicon 800-Series Diode Specifications

High Voltage Silicon Very Fast Recovery Rectifiers

A1

MECHANICAL DATA



CONFORMS TO JEDEC OUTLINE DO5
ALL DIMENSIONS IN INCHES

NOTES:
- Standard Polarity is Cathode common to case
- Add Suffix LTR "R" for Common Anode

FEATURES

- 35 AMPERES
- LOW V_F
- HIGH SURGE
- LOW LEAKAGE
- P.I.V. TO 1000 VOLTS
- VERY FAST

MAXIMUM RATINGS

I_F (Ave.)	I_{FSM}(Surge) 8.3 mSec-60 Hz	$V_{RM(rep)}$, $V_{RM(wkg)}$, V_R IN VOLTS					Case Style
Amperes	Amperes	500	600	700	800	1000	
35	400	SUES807	SUES808	SUES809	SUES810	SUES811	DO5

ELECTRICAL CHARACTERISTICS

DEVICE CHARACTERISTICS	Symbol	Max. Value	Units
SUES807 thru SUES811			
D.C. Forward Voltage (I_F = 35 Adc, T_C = 25°C, & 125°C, 807 thru 809)	V_F	1.25/1.15	Volts
(I_F = 35 Adc, T_C = 25°C, & 125°C, 810 thru 811)	V_F	1.3/1.2	Volts
D.C. Reverse Current (@ Rated V_R, T_C = 25°C & 150°C, 807 thru 811)	I_R	.10/40	MA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Junction Operating Temp. Range	T_J	-65 to +150	°C
Maximum Storage Temperature Range	T_{STG}	-65 to +175	°C

*SUES807-811 T_{rr} = 50 nsec max, C_j Typ 175 pf @ -10 V
*I_F = 1/2 A, I_R = 1.0 A, i_{REC} = 1/4 A

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SEMICONDUCTOR DEVICES

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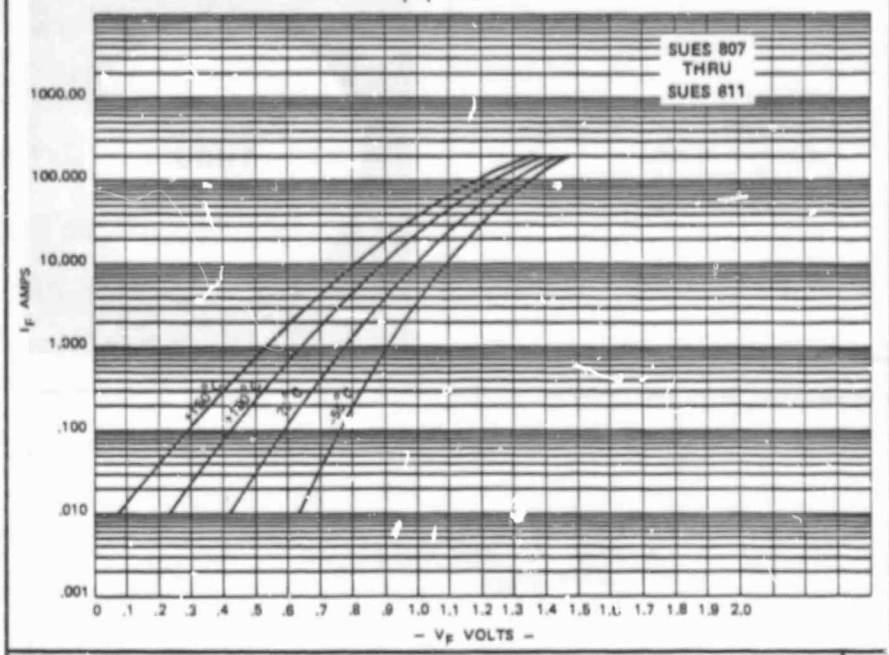
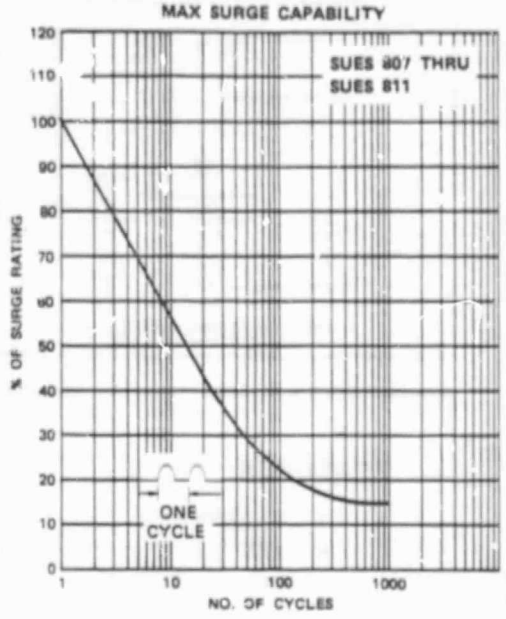
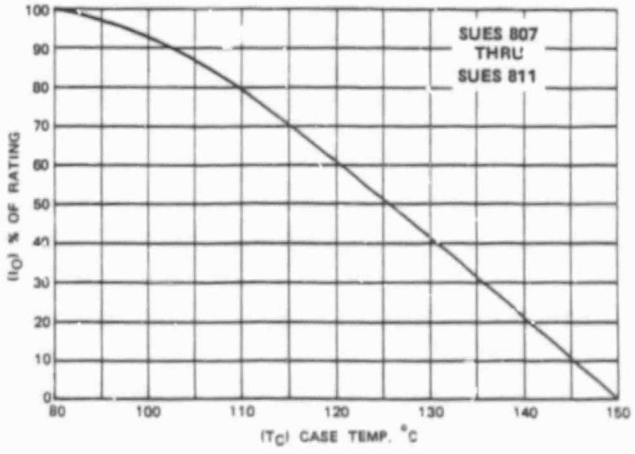
V_F/I_F TYPICAL



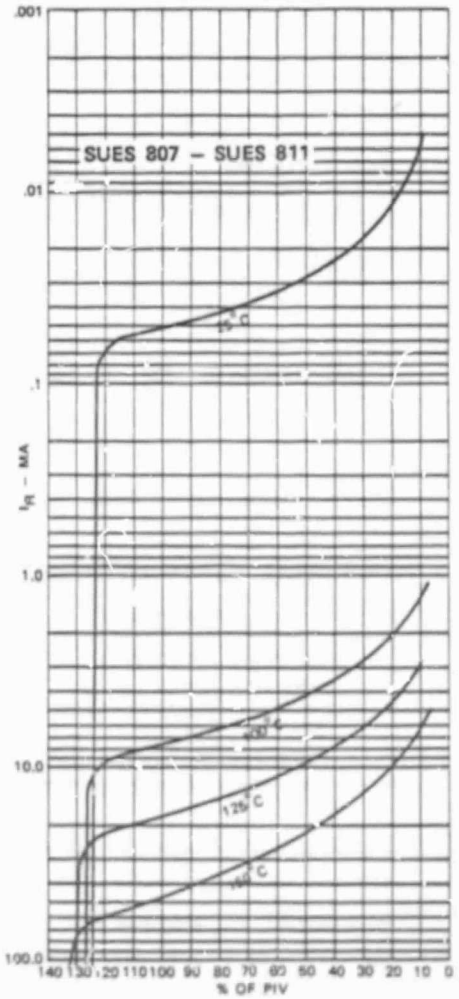
MAX SURGE CAPABILITY



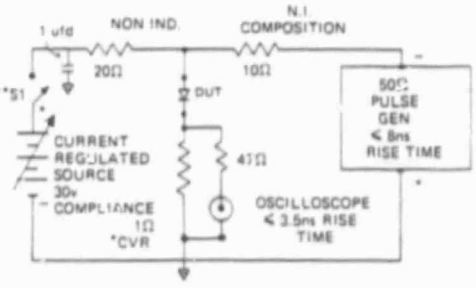
OUTPUT CURRENT vs. CASE TEMPERATURE



TYPICAL REVERSE CURRENT vs. REVERSE VOLTAGE



REVERSE RECOVERY TEST CIRCUIT



*CVR MUST BE A NON-INDUCTIVE RESISTOR. COAXIAL CONSTRUCTION PREFERRED.

**S1 CLOSED ONLY LONG ENOUGH TO MAKE MEASUREMENT DEVICE HEATING WILL OCCUR IF LEFT CLOSED. HEATING WILL RESULT IN LONGER THAN NORMAL TRR TIME. S1 MAY BE AN ELECTRONIC SW AND CLOCKED TO PULSE GEN.

Appendix B

Results of Minimum-Mass Reactor Optimization

Results of Minimum-Mass Reactor Optimization

Definition of Symbols

A	Cross-sectional area of the core in m^2.
B_{max}	Specified maximum allowable flux density in T.
B_R	Specified residual flux density in T.
d_m	Specified density of the magnetic core in kg/m^3.
d_{wr}	Specified density of the magnet wire in kg/m^3.
F_c	Specified ratio of mean length per turn of winding to the perimeter of the cross section of the core, numeric.
f_S	Switching frequency in Hz.
$F_{w,max}$	Specified maximum allowable winding factor, numeric.
K	Specified reciprocal current density in m^2/A.
ℓ	Mean magnetic path length of the core in m.
m_T	Total reactor mass in kg.
N_P	Number of turns on the primary winding, numeric.
N_S	Number of turns on the secondary winding, numeric.
$P_{O,crit}$	Specified minimum output power level above which the converter is required to operate in continuous-mmf mode over the entire range of input voltage in W.
$P_{O,max}$	Specified maximum output power of a converter in W.
V_D	Diode forward voltage drop in V.
$V_{I,max}$	Maximum input voltage of a converter in V.
$V_{I,min}$	Minimum input voltage of a converter in V.
V_O	Output voltage of a converter in V.
V_Q	Transistor saturation voltage drop in V.
T_S	$= 1/f_S$, conversion period in s.
γ	$= N_S/N_P$, turn ratio, numeric.
μ	Absolute permeability of the core in H/m.

Defining the numerical constant

$$a = \frac{\left(\gamma + \dfrac{V_0 + V_D}{V_{I,min} - V_Q}\right) P_{0,max}^{1/2}}{\left(\gamma + \dfrac{V_0 + V_D}{V_{I,max} - V_Q}\right) P_{0,crit}^{1/2}}$$

the design constants for the minimum-mass reactor are given by

$$A_{opt} = \frac{\Delta}{3}\left\{\frac{c_1 c_2}{\pi F_{w,max}}\right\}^{1/2}$$

$$\ell_{opt} = \frac{2\,\pi^{3/4}\,3^{1/2}}{\Delta^{1/2}}\left\{\frac{c_1 c_2}{F_{w,max}}\right\}^{1/4}\left(1 + \frac{\Delta}{6}\right)$$

$$\mu_{opt} = \frac{2\,\pi^{1/4}\,\Delta^{1/2}}{3^{1/2}\,c_1^{1/2}}\left\{\frac{c_2}{F_{w,max}}\right\}^{3/4}\left(1 + \frac{\Delta}{6}\right)$$

where

$$c_1 = \frac{T_s\,P_{0,max}\,(V_0 + V_D)}{2\,V_0\,(B_{max} - B_R)^2}\left\{a + \frac{1}{a}\right\}^2$$

$$c_2 = \frac{K(B_{max} - B_R)}{(a + a^{-1})}\sqrt{\frac{[\gamma(V_{I,min} - V_Q) + V_Q + V_D]}{(V_0 + V_D)}\left[a^2 + \frac{1}{3a^2}\right]}$$

$$\Delta = \left\{1 + \frac{12\,F_{w,max}\,F_c\,d_{wr}}{d_m}\right\}^{1/2} - 1$$

and the expression for the minimum reactor mass is

$$m_{T,min} = \frac{2\,\pi^{1/4}}{3^{1/2}\,\Delta^{1/2}}\left\{\frac{c_1 c_2}{F_{w,max}}\right\}^{3/4}\left\{\left(\Delta + \frac{\Delta^2}{6}\right) d_m + 6\,F_{w,max}\,F_c\,d_{wr}\right\}$$

$$= K_1\left\{\frac{P_{0,max}}{f_s}\right\}^{3/4}$$