The University of Tennessee
Department of Electrical Engineering
Knoxville, Tennessee 37916

A STUDY OF
UNIVERSAL MODULATION TECHNIQUES
APPLIED TO SATELLITE DATA COLLECTION

Final Report

December 1980

Contract No. NAS5-24250

Prepared for

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

Abstract

A scheme for a universal modulation and frequency control system for use with data-collection platform (DCP) transmitters is examined. The final design discussed can, under software/firmwave control, generate all of the specific digital data modulation formats currently used in the NASA satellite data-collection service and can simultaneously synthesize the proper RF carrier frequencies employed.

A novel technique for DCP time and frequency control is presented. The emissions of NBS radio station WWV/WWVH are received, detected, and finally decoded in microcomputer software to generate a highly accurate time base for the platform; with the assistance of external hardware, the microcomputer also directs the recalibration of all DCP oscillators to achieve very high frequency accuracies and low drift rates versus temperature, supply voltage, and time.

The final programmable DCP design also employs direct microcomputer control of data acquisition, data reduction, formatting, transmitter switching, and system power management. The system hardware and software was described in detail. Finally, future techniques for PDCP design, projected tasks for PDCP field units, and the anticipated capabilities of new units to handle these jobs are presented.

CONTENTS

CONTENTS (continued)

CONTENTS (continued)

LIST OF FIGURES

LIST OF FIGURES (cont.)

LIST OF TABLES

1. INTRODUCTION

1.1 BACKGROUND AND PURPOSE

The major impetus for this project was the desire of NASA personnel at Goddard Space Flight Center, particularly Mr. J. Earle Painter, to develop a universally applicable data-collection platform (DCP) which would be capable of acquiring various types of analog and digital data, formatting and storing this information, and then through a standard RF transmitter relaying the digital data stream to an overhead satellite for transmission to a central data receiving station[1].

Perhaps the major difficulty in implementing such a universal data-collection system is the considerable variation from satellite to satellite in their requirements for data bit rates, transmission burst lengths, data formats, modulation parameters, modulation types, and final RF frequencies employed in the DCP-to-satellite uplinks. For this reason DCP's have been implemented for specific satellites only; only through substantial hardware and/or crystal changes (normally done at the depot or factory level) could a platform for a specific satellite be converted for use with another [2].. In addition, the DCPs available at present are quite costly for the data-collection end-user to purchase, thus precluding many potential DCP users from getting into the field. As a result, satellites are frequently underutilized and their capacity for public service is curtailed. NASA personnel have therefore greatly encouraged the development of a system which will not only fulfill the operational requirements of a universal DCP but which will be moderate in cost, highly reliable, and simple for the end-user to operate successfully in the field.

The system developed by the Electrical Engineering Department at the University of Tennessee meets these requirements by utilizing the vast flexibility of a microprocessor-controlled DCP developed by U-T for NASA under Contract No. NAS5-22495 [3] and augmenting this concept with several new and cost-effective techniques for modulation and frequency control. The net result should provide unprecedented DCP performance and versatility at quite moderate cost, thus enabling many more agencies and groups to acquire the benefits of NASA's satellite data-collection facilities.

1.2 DESIGN PHILOSOPHY

The specific intent of the project, as designated by the contract title, was to develop a "universal modulator" system which could receive a previously-encoded data bit stream and translate it into the proper RF modulation format and frequency for use with any NASA data-collection satellite either currently in use or to be employed in the foreseeable future. A fundamental property of the universal modulator was that it should accomplish all the desired modulation and frequency-control tasks as much as possible via microprocessor software/firmware and with an absolute minimum of external hardware. The output waveform was to be stored in digital form in a high-speed read-only memory to facilitate generation of the desired output signal by microprocessor control.[4].

An additional requisite for the "universal modulator" approach was that it be compatible with the format of the previously developed U-T PDCP system, in order to retain the technological advantages of that implementation. The universal modulator system was therefore designed to interface with the PDCP setup as directly as possible by use of standard I/O -

port devices controlled by the PDCP microprocessor. The extensive array of U-T software was retained with only minor modifications to accomodate the added control algorithms necessary to handle the universal modulator functions.

The basic U-T software package has been rearranged within the program-storage ROMs in the form of blocks of code which as either primary or secondary subroutines can be called by the main operating program in any combination or order desired by the user. The principal advantage of this concept is that the data-collection end-user is free to select only those data-processing routines which are pertinent to his own project; additionally, he can readily add his own special-purpose routines to those already provided in the general data collection package in order to meet his specific requirements. The main operating program is largely transparent to the user; it is necessary to specify only that portion of the control program which determines the desired sequence of subroutines to be employed in the data collection/data processing task. All platform programs are stored in low-power CMOS EPROM arrays which can readily be erased and reprogrammed if the user's requirements for the DCP change.

In addition to the explicit requirements mentioned previously, there were several other basic factors included in the total system design which had considerable bearing on the final form of the implementation. First, since the vast majority of DCPs are deployed at remote sites which cannot be easily serviced, it is normally necessary to power the units with storage batteries, solar panels, or a combination of the two. It therefore becomes imperative to keep overall DCP power consumption to an absolute minimum if the system is to operate unattended for extended periods of time (e.g., up to a year). The DCP microprocessor

system and related components must employ very low-power chips whenever possible, or else perform power management functions to turn off the power except when absolutely necessary to those circuits which have substantial power drains in normal operation (e.g., the RF transmitter). The control microprocessor implements the power-management function by incorporating into the normal sequence of instructions additional program steps which through auxiliary I/O ports turn on and off the various sections of DCP circuitory in a predetermined order to minimize the overall system energy drain while simultaneously providing proper system transmission lengths and intervals.

The second basic area of consideration in the system design procedure was that of economics. The components selected had to be relatively inexpensive; exotic and costly components were to be avoided whenever possible. In the course of component selection for the oscillator circuits it was discovered that although high-quality oscillator modules were available from several vendors, the typical price of three to four hundred dollars each made use of these assemblies economically unfeasible for the DCP systems, especially since the overall system required three of the high-stability oscillators but was to have a final cost of no more than $1500 to $2000. Thus it was a simple matter of expense that prompted the decision to develop the WWV dynamic frequency-correction scheme in order to employ much cheaper oscillators which could be satisfactorily corrected to the high degree of accuracy required by the DCP.

A third concern was that of reliability. Obviously, a data-collection system in a remote location must be able to perform unattended for long periods and should be able to do so with little or no periodic or

emergency maintenance if it is to be attractive to end-users. The high cost of electronic maintenance precludes placing units which drift or otherwise malfunction and therefore require expensive field service. In addition, conversations with personnel from NASA's National Space Testing Laboratory at Bay St. Louis, Mississippi revealed an undesirably high incidence of currently deployed DCPs which in the course of a few months to a year of unattended service drift out of their assigned frequency bands and into adjacent ones, causing harmful interference to other DCPs on nearby channels. Still other DCPs drift out of their assigned time slots and thereby interfere with other co-channel units. The control scheme employed on the U-T system provides for standard-frequency acquisition from WWV which will enable the system clocks to stay well within tolerances sufficient to guarantee on-channel operation of the DCP; standard WWV time code is also decoded to facilitate proper timing of system functions, typically to better than $\pm$15 milliseconds.

The final consideration was that of ease of use; the data-collection customer must be able to program and set up the platform with a minimum of special training and/or effort. To that end, the U-T unit has been designed to be simple to install and, once set up, to be essentially automatic in operation for the life of the power source. Considerable effort has been expended to make the system control features transparent to the user and to ensure that the programming procedure is as straightforward as possible.

For these reasons the U-T DCP system should represent a commercially feasible system of high quality which offers the potential user a higher performance/price ratio than is available currently. It is therefore

hoped that the system can be of substantial benefit to NASA and the public in general by expanding the applications and usefulness of satellite data-collection to many new areas.

REFERENCES

1. Request for Proposal, NASA-Goddard Space Flight Center, RFP Number 5-45587-254, January, 1977.

2. Instruction Manual for the Convertible Data Collection Platform (CDCP) and Related Equipment. LaBarge, Incorporated, Tulsa, Oklahoma, 1976, p. 2-5.

3. Programmable Data Collection Platform System, Phase II. University of Tennessee, NASA Contract NAS5-22495, May, 1978.

4. Document for Contract NAS5-24250, NASA-Goddard Space Flight Center, Greenbelt, Maryland, July 14, 1977.

2. DIGITAL OSCILLATOR SYSTEM

2.1 SYSTEM CONCEPTS

The basic intent of the digital oscillator concept, first demonstrated for NASA by Texas Instruments, Incorporated, was the synthesis of a digitally-controlled FSK waveform with special characteristics for use in satellite communication systems.[1]. In order to more efficiently utilize available RF spectrum space it is always desirable to restrict signal bandwidths, commensurate, obviously, with very low to negligible bit-error rates. Narrow-bandwidth signals, when employing some form of angle modulation such as FSK or PSK, are extremely useful in relatively low signal-to-noise reception conditions such as normally occur in satellite data transmission systems. In addition, these angle-modulated signals are relatively simple to generate, are capable of being amplified without distortion by high-efficiency class-C transmitting stages, and can be efficiently demodulated using such devices as feedback detectors, phase-locked loops, and pulse-counting discriminators. The overall usefulness and superiority of FSK and PSK modulation for digital RF transmission has been well established for many years; indeed, these forms of modulation are the worldwide standards for digital communications via satellite.

Newer, more refined forms of FSK and PSK have emerged as a result of the desire to minimize spectral bandwidth requirements, average bit errors, interference to adjacent communication channels, and transmitter power levels required to overcome channel noise.[2]. Although Manchester-encoded, biphase PSK is currently the most popular modulation scheme in use with satellite data-collection systems, NASA has been keenly interested in the

particular type of FSK known as MSK (minimum-shift keying), which is a special form of CPFSK (continuous-phase frequency-shift keying). CPFSK is notable in that its frequency transitions are generated with continuous-phase zero-crossings; i.e., no discontinuities in phase are allowed to occur. It can be demonstrated mathematically that any fast phase transitions or discontinuities in the RF signal waveform give rise to sideband components of considerable amplitude which lie at integral multiples of the basic data bit rate away from the RF center frequency. If these fast shifts in frequency (and phase) are eliminated, a useful improvement in average occupied signal bandwidth (for a given data bit stream) can be realized; moreover, a substantial reduction in instantaneous peak frequency deviations results. Significantly, it is these occasional wideband bursts which contribute to the majority of bit errors encountered in units receiving on channels adjacent to the one in question. This crosstalk therefore is a significant consideration in the selection of any modulation format which is to be utilized in a tightly-packed frequency-multiplexed system such as a data-collection satellite setup, particularly when the costs of system equipment and the relative economic value of collected data are so high. With narrower effective channel bandwidths, a given satellite transponder is capable of handling more channels of data with the same error rates or else reducing the bit error rates due to crosstalk on the existing number of channels.

2.2 DIGITAL OSCILLATOR THEORY

The basic digital oscillator system, as developed by Texas Instruments for NASA, is pictured in block diagram form in Figure 2.2.1.

In the drawing, the heavy lines represent a multi-bit parallel

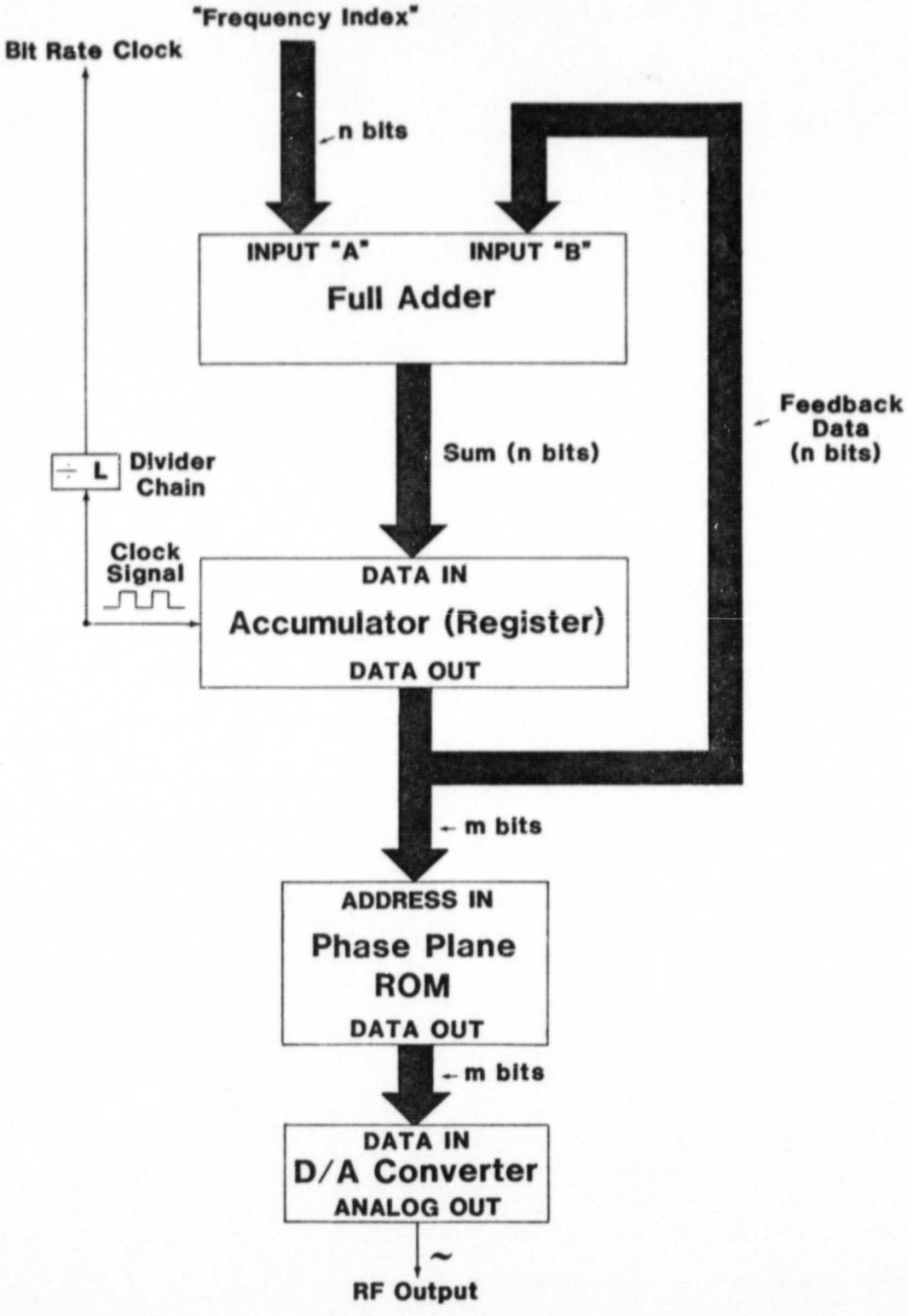

Figure 2.2.1. Basic Digital Oscillator-Block Diagram.

digital data bus; all of the indicated data bus paths are either n bits wide (inputs to the adder and accumulator) or m bits (inputs to the phase plane ROM and D/A converter). As can be seen, the two inputs to the full adder block are n-bit data words which represent the frequency number (into input "A") and the accumulator output (into adder input "B"). The sum of "A" and "B" (without the carry bit) is generated at the adder output and is fed into the accumulator. On each positive transition of the clock signal, the register inputs are transferred to the outputs and thus to the address inputs of the phase plane ROM and back to the "B" inputs of the full adder.

The overall operation of the system is as follows: on command from the system clock, the accumulator gates data from the full adder circuits into its registers. This output digital word then (after progation delays) is presented to the full adder, along with the "frequency index" (F.I.). The adder, after its propagation delays, generates the sum of F.I. and the register output word, which immediately appears at the accumulator inputs. Upon the next system clock pulse, the entire process repeats itself. The net effect of all this is that, assuming an initial count of zero and F.I. equal to one, the register outputs count up from a value of all zeros to a value of all ones. The count increments by one each clock pulse, until with the register output word = 11111 ... 111 the next clock pulse causes the adder result to overflow to 000 ... 000. In this circuit the highest carry (overflow) bit is ignored, and only a certain number of bits are retained. Since the count progresses linearly (with clock pulses) from all zeroes to all ones and then suddenly changes to all zeros, it numerically represents a ramp function with a periodic reset to zero. The length of

time required for one complete cycle of this function is simply the clock period times 2^n, where n is the number of bits (width) of the accumulator. In addition, if F.I. is chosen to be some number of ($\leq$ n binary bits) other than one, the output period will also change. For instance, if F.I. is set to two (...00010), then the result will increment to all 1's twice as fast (since on each clock pulse the result will increase by two) and thus the output frequency will be double that of the original case. The output frequency (f_{OUT}) can therefore be related to the clock frequency (f_{CLK}), the frequency index (F.I.), and the register size of n bits by the equation

$$f_{OUT} = \frac{(f_{CLK})(F.I.)}{2^n} , \qquad \text{(Eqn.2.2.1)}$$

Thus by varying either n, F.I., or f_{CLK} one can change the output frequency. The minimum frequency change attainable with the digital oscillator is given by

$$\Delta f_{min} = \frac{f_{CLK}}{2^n} , \qquad \text{(Eqn.2.2.2)}$$

where Δf_{min} represents the frequency resolution or frequency step size of the system. In a multichannel communications setup, Δf_{min} may be set equal to the desired unipolar CPFSK frequency deviation (or a submultiple thereof) or perhaps equal to the desired interchannel spacing when the digital oscillator is used as a frequency synthesizer. By changing the value of F.I. one may therefore digitally select either the FSK deviation and/or the center channel frequency. The minimum frequency increment, as can be seen from Equation 2.2.2, is directly proportional to the clock frequency but varies inversely with 2^n, where n is the number of accumulator

bits. Thus a higher clock rate produces a higher output frequency and larger step frequency increment, whereas increasing the register width has the opposite effect.

Another constraint of the MSK-generation process is that the data bit transitions must be synchronous with the system clock. This ensures that no glitches or races in the logic will occur, as might happen for a non-synchronous data change; more specifically, the reference clock must be an integral multiple of the effective bit rate frequency in order to produce the desired continuous-phase zero crossings of the final analog output waveform. Also, since MSK has been defined as the special case of CPFSK with the modulation index (β) of 0.25, the effective unipolar final carrier frequency shift $|\Delta f|$ must be exactly one-half the bit rate frequency. This condition also places constraints on the following system RF circuitry, as will be discussed later.

There are two other fundamental constraints in the digital oscillator proper which govern its timing. The first is the ratio of the reference clock frequency to the generated output frequency. The higher this ratio is, the finer the level of quantization in time of the output waveform occurs; this determines the effective number of samples per cycle of the output wave. A reasonable level of accuracy is provided when the clock is roughly an order of magnitude higher in frequency than the output; this yields about ten samples per cycle, or one sample every 36° in phase. This waveform in itself is not very "clean", i.e., there is considerable energy near the sample (clock) frequency and its harmonics, but normally this undesired energy is removed in a bandpass filter immediately following the output D/A converter.

The second basic limitation is the maximum bit rate. As mentioned previously, the effective bit rate must be exactly an integral submultiple of the clock frequency. Furthermore, since the principal advantage of MSK is its relatively small effective bandwidth, it is reasonable to assume that the effective deviation is quite small compared with the center frequency of interest. Thus, the modulating (bit rate) frequency must also be much less than the carrier frequency. A practical limit for narrowband signal bandwidth is roughly one per cent of carrier frequency, so if the bit rate is set at no greater than one-hundreth of the output frequency for the digital oscillator, the output frequency-modulation index will be <1.0 and the narrowband requirement is thus satisfied.

The digital oscillator may also be used indirectly as a phase modulator for digital input signals. This ability of the circuit to generate PSK was developed at The University of Tennessee as part of the effort to minimize the hardware requirements for the "Universal Modulator" system. The circuit is basically an enhancement of the original digital oscillator concept, in which an additional full adder block is inserted between the accumulator output and the address inputs of the phase plane ROM, as shown in Figure 2.2.2. The phase shift is produced by adding a fixed number (designated the "Phase Index", P.I.), to the m highest output bits of the accumulator in accordance with the data bit to be transmitted. The actual value of the P.I. will depend on the desired phase shift needed from the digital oscillator. For instance, if the phase-plane ROM has 256 words, then each phase step will represent $\frac{360°}{256} = 1.40625°$. Thus, if a $\pm$ 1 radian phase shift (approx. $\pm$ 56.25°) is desired at the digital oscillator carrier output frequency, then the P.I. would be $\frac{\pm 56.2500°}{1.40625} = \pm 40_D$. If the rest phase is arbitrarily assigned a P.I. of zero, then P.I.

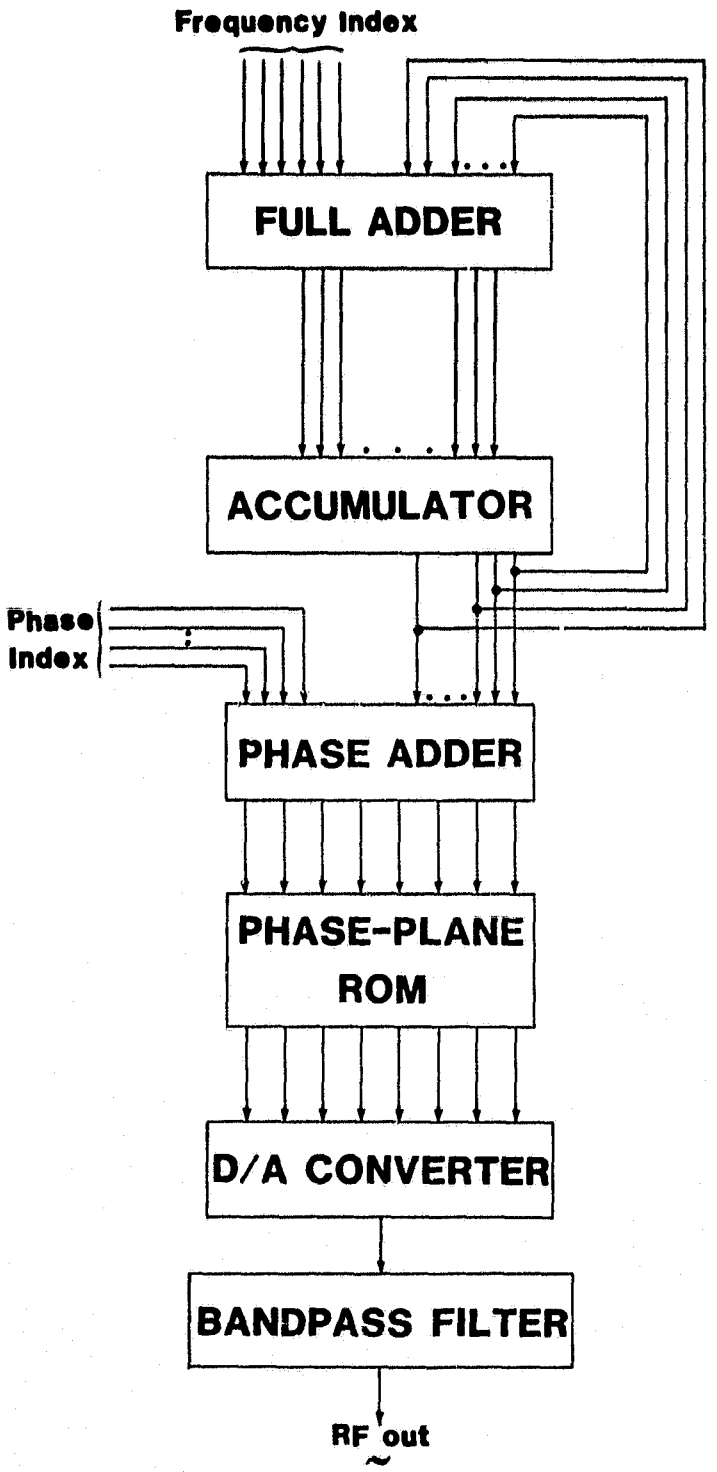

Figure 2.2.2. Enhanced Digital Oscillator System-Block Diagram.

would be 40_D (28_H) for a data bit 1 and the two's complement of 40_D ($D8_H$) for a data bit 0. When the P.I. is changed, the result is a jump in the phase plane address (by the specified amount) which in turn causes a phase shift in the analog signal emerging from the D/A converter output. The following bandpass filter removes extraneous high frequency (e.g., clock-rate) and low-frequency (e.g., bit-rate) signals from the carrier output to ensure the spectral purity of the transmitted RF signal. The positive P.I. causes the phase of the output waveform to advance, while the two's complement form produces a retarded-phase output, thus producing the desired PSK modulation. The phase deviation may be defined as any integral multiple of $\pm$ 1.40625° up to $\pm$ 180°, simply by specifying the positive and negative (two's complement) values of the P.I.

As with MSK, the digital oscillator configuration experiences certain limitations with respect to the generation of PSK. Due to the digitization of both the output amplitude and phase, there are quantizing errors associated with the output RF waveform. Since amplitude errors are inherently not a significant consideration in angle-modulated communication systems, the use of an 8-bit data word in the phase plane and the resultant 8-bit resolution from the D/A converter presents no real problem to the accurate transmission of digital data. However, the discrete time intervals at which values for the output waveform are defined are significant in determining the ultimate time or phase accuracy of the output. Specifically, the zero-crossing points should be very accurate, or else phase jitter will be the apparent result. Appendix I gives a detailed consideration of this effect, which is perhaps the most confining limitation of the digital oscillator concept.

The 8-bit ROM phase plane data essentially represents one complete cycle of a sine wave, with an added dc offset. The offset is added to allow a continuous, unipolar analog signal to be produced by the following D/A converter. Although in some applications it has proven feasible to represent the sinusoid as a single quadrant and employ count-up/count-down addressing and analog output phase-inversion switching to generate an accurate waveform with a smaller ROM requirement, in the digital oscillator setup this leads to several difficulties. First, the phase-switching circuitry can cause timing errors in the critical region around the zero-axis crossings of the wave. Secondly, with the digital oscillator it is difficult to implement both count-up and count-down functions simultaneously. Therefore it is both more convenient and more accurate (phase-wise) to store the entire cycle. In addition, the algorithm used employs a dynamic range of 255 rather than the full 256 capability of the ROM. The purpose of this is to guarantee a symmetrical range of values for the output wave, thus minimizing the generation of even-order harmonics of the desired RF signal. The actual algorithm is given by

$$V(\phi) \cong [\ 128_D + 127_D \sin n\alpha\ ]_H,\ \alpha = 1.40625^\circ \quad \text{(Eqn.2.2.3)}$$

In the formula, $V(\phi)$ represents the equivalent hexadecimal value, rounded to the nearest whole number, of the bracketed expression. The phase increment α is simply $360^\circ/2^8$, or $\frac{360^\circ}{256\ \text{steps}}$; n is any integral value from 0 to 255, inclusive. The maximum value (corresponding to 90°) is 255; the minimum (at 270°) is one. Note that the values at 0° and 180° are precisely 128, which is the equivalent dc offset; thus the output wave zero-crossings are explicitly specified, thereby reducing the effects of

amplitude round-off error on the final phase jitter of the RF output signal.

The digital oscillator system when used as a frequency synthesizer has very good inherent frequency stability (normally same as the clock-frequency source); the integrated phase jitter over a long period is zero, since the average value of the jitter error signal is zero. As seen from Eqn. 2.2.2, the size of the minimum frequency step is dependent solely on f_{CLK} and the overflow value of the accumulator, namely 2^n. The relationship between the attainable frequency resolution Δf_{min} and the number of parallel accumulator bits n is given by

$$\Delta f_{min} \propto 2^{-n} . \qquad \text{(Eqn. 2.2.4)}$$

It can thus be seen that there is a fixed relationship between bit rate, resolution, and accumulator width.

The essential design equations for the digital oscillator system are powerful tools for the analysis of system performance and facilitate the necessary trade-off studies of attainable bit rates, output frequencies, deviations, and phase performance. The analysis in Appendix I relates system phase jitter and frequency resolution to the basic system parameters and provides an index of system performance for a wide variety of hardware and/or software configurations.

2.3 SOFTWARE IMPLEMENTATIONS

The basic digital oscillator scheme previously described can also be implemented via software programs in a standard microprocessor. In fact, the technique utilized in the digital oscillator could be useful in a wide variety of frequency-synthesis and waveform-generation applications.

The only major limitation of the method when used in microprocessor-based systems is the ultimate output frequency attainable, and that in turn is dependent upon the instruction cycle time of the particular machine under consideration.

As an example, the digital oscillator system, including the phase plane, was implemented in software for an 1802-based microcomputer system to determine the feasibility at this point in time for direct software implementation of the MSK/PSK generation technique. The basic program loop consists of a 16-bit add cycle (which is comprised of one 8-bit straight addition and one 8-bit add with carry) and a simple 8-bit add instruction. The 16-bit add routine takes the desired Frequency Index and adds it to the 16-bit number stored in the accumulating register. The second add utilizes the high-order 8 bit portion of the accumulator and adds to it the 8-bit Phase Index. The sum of this operation, neglecting the carry bit, is then used to address the previously-stored phase plane data; this data is then outputted to a D/A converter which produces the actual MSK/PSK modulated carrier.

This basic program was written for several types of microprocessors to ascertain the maximum output frequencies available. Bit-slice units were considered, as was a 16-bit NMOS unit, and the various speeds and power dissipations compared. The condensed results are found in Table 2.3.1. Included for comparison purposes are the parameters for various hardware-type implementations with the standard 16-bit accumulator width. The test conditions assume a standard +5V supply for the LSTTL, I^2L, and NMOS chips and a V_{DD} supply of +10V for the CMOS units. It is also assumed that $f_{CLK} \approx 10 f_{OUT} \approx 1000\ f_{BR}$.

Table 2.3.1.

Microprocessor Speed Comparisons

LOGIC TYPE	CHIP TYPES	CHIP NOS.	APPROX. POWER DISSIPATION	APPROX. MAX. ADD RATE (f_{CLK})	APPROX. MAX. f_{OUT}	APPROX. MAX. BIT RATE
CMOS	Adders/Registers	45181 45182 74C174	225mW	1.5MHz	150kHz	1500Hz
LSTTL	Adders/Registers	74LS283 74LS174	800mW	15MHz	1.5MHz	15kHz
LSTTL	Bit-slice µP	2901 2902 2909	4.0W	6MHz	600kHz	6kHz
ECL	4-Bit-slice µP	10800	6.0W	10MHz	1.0MHz	10kHz
I^2L	4-Bit-slice µP	SBP0400A SBP401	800mW	2MHz	200kHz	2kHz
NMOS	16-bit µP	9900	500mW	140kHz	14kHz	140Hz
CMOS	8-bit µP	1802	20mW	20kHz	2kHz	20Hz

From the results in Table 2.3.1 it is evident that in general, except for the bipolar units, the microprocessors are much too slow to produce the desired 300kHz-1MHz carrier output frequency. Since in currently operational satellite DCP systems (e.g., LANDSAT) the bit rate may be as high as 5kHz, the bipolar bit-slice units are sufficiently fast but will in operation consume roughly as much power as the entire RF transmitter assembly. Obviously, this is unsatisfactory for battery-powered systems since this fact alone would double the required battery capacity for the DCP system. Thus at this juncture, the LSTTL hardware approach offers the most useful balance between power consumption and speed for implementation of the complete digital oscillator system.

Nevertheless, for demonstration purposes, digital oscillator simulation programs have been written for the 1802 and the 8080A microprocessors. These programs take a prestored array of data bits, convert them to a serial data stream, and then (by means of changing the "Frequency Index" number) alter the output frequency being sent from an 8-bit parallel port which is then translated to a continuous audio-frequency sinusoid by a final D/A converter.

2.3.1 Demonstration Software for 1802

The 1802 demonstration program utilizes the register-oriented structure of the machine to efficiently address the prestored Frequency Index number, use it with the 16-bit accumulated value to perform the digital oscillator-type add function, and then perform the appropriate 8-bit phase-control addition. This result is then used to address a byte in the phase-plane array stored in RAM; the byte is then loaded into an output port which feeds the D/A converter. The basic flow diagram for the

1802 demonstration program is shown in Fig. 2.3.1.

The flag inputs $\overline{EF1}$, $\overline{EF2}$, and $\overline{EF3}$ are used by the program to determine the desired modulation parameters. Flag $\overline{EF1}$ selects the modulation type (PSK or MSK); flag $\overline{EF2}$ determines when the carrier is modulated by the data stream; and $\overline{EF3}$ is sampled in order to determine the output center frequency, to simulate how a microprocessor under software or firmware control could select different transmitting channels. The digital output is converted to a nearly sinusoidal wave by the action of the phase plane and D/A converter and its associated bandpass filter. The output audio-frequency signal is monitored through a small loudspeaker. The technique allows the nontechnical personnel witnessing the demonstration to readily perceive the effects of frequency shift, sideband structure, and bit rates on the MSK and PSK signals. In addition, this audio tone (roughly 600-700Hz) may be recorded on a standard cassette or transmitted via telephone for dissemination of these modulation techniques to a wide range of satellite data-collection system users and potential users.

The first major task of the demonstration program, after register initialization and data storage, is to sample the three external flag ($\overline{EF}$) inputs to determine which set of modulation conditions is desired by the operator. The flag decoding routine shown at the top of Figure 2.3.1. sequentially determines the flag states and then branches to one of eight subroutines, A through H, according to the frequency, operation, and modulation type desired. The MSK function is implemented as CPFSK with a modulation index of exactly 0.25; the PSK is synthesized by causing a jump of $\pm$60.47° ($\pm$43 steps) in the phase plane. The effects of the two modulation forms are easily detected by ear and serve to underscore the

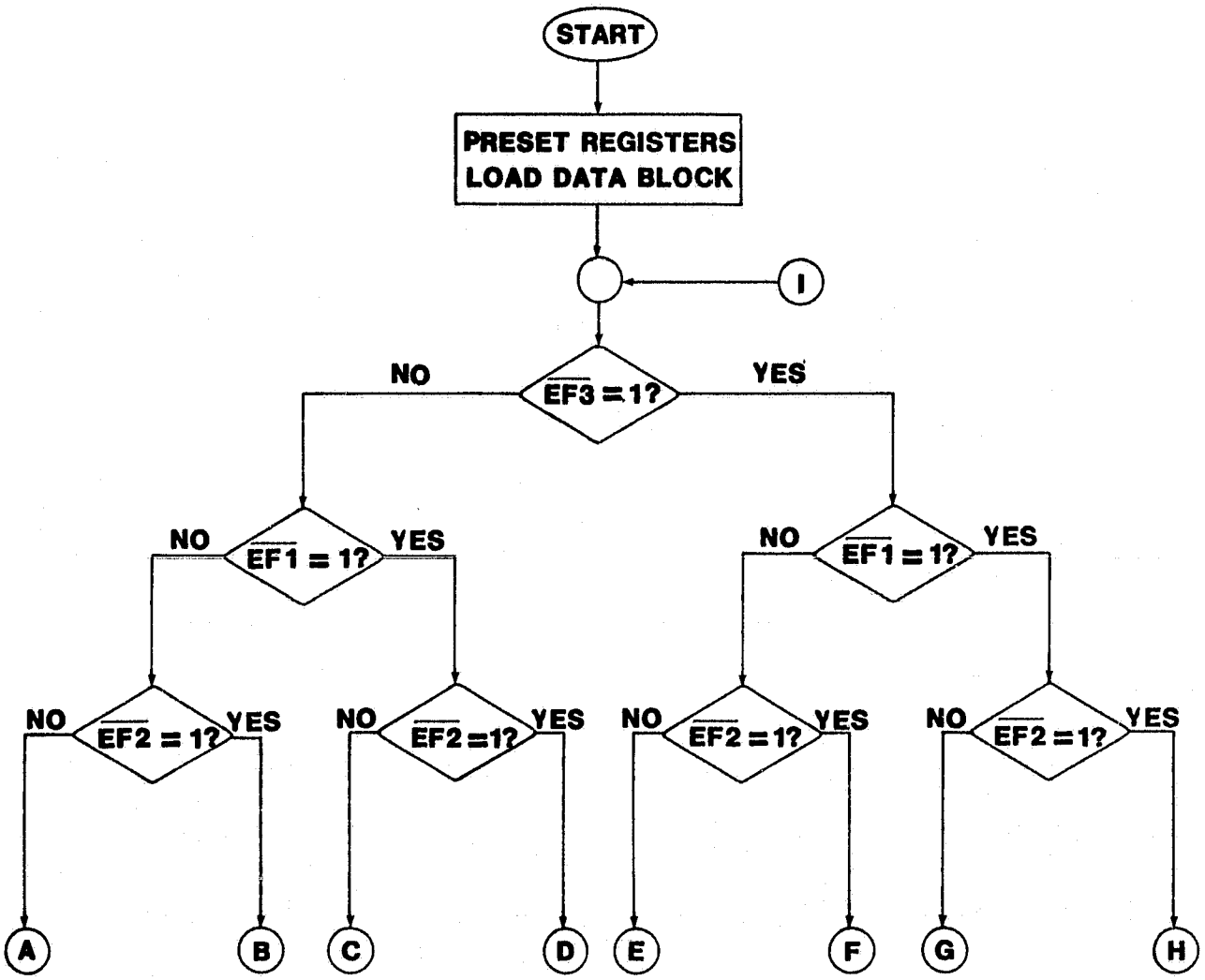

Figure 2.3.1. Basic Flow Chart for 1802 MSK/PSK Demonstration Program.

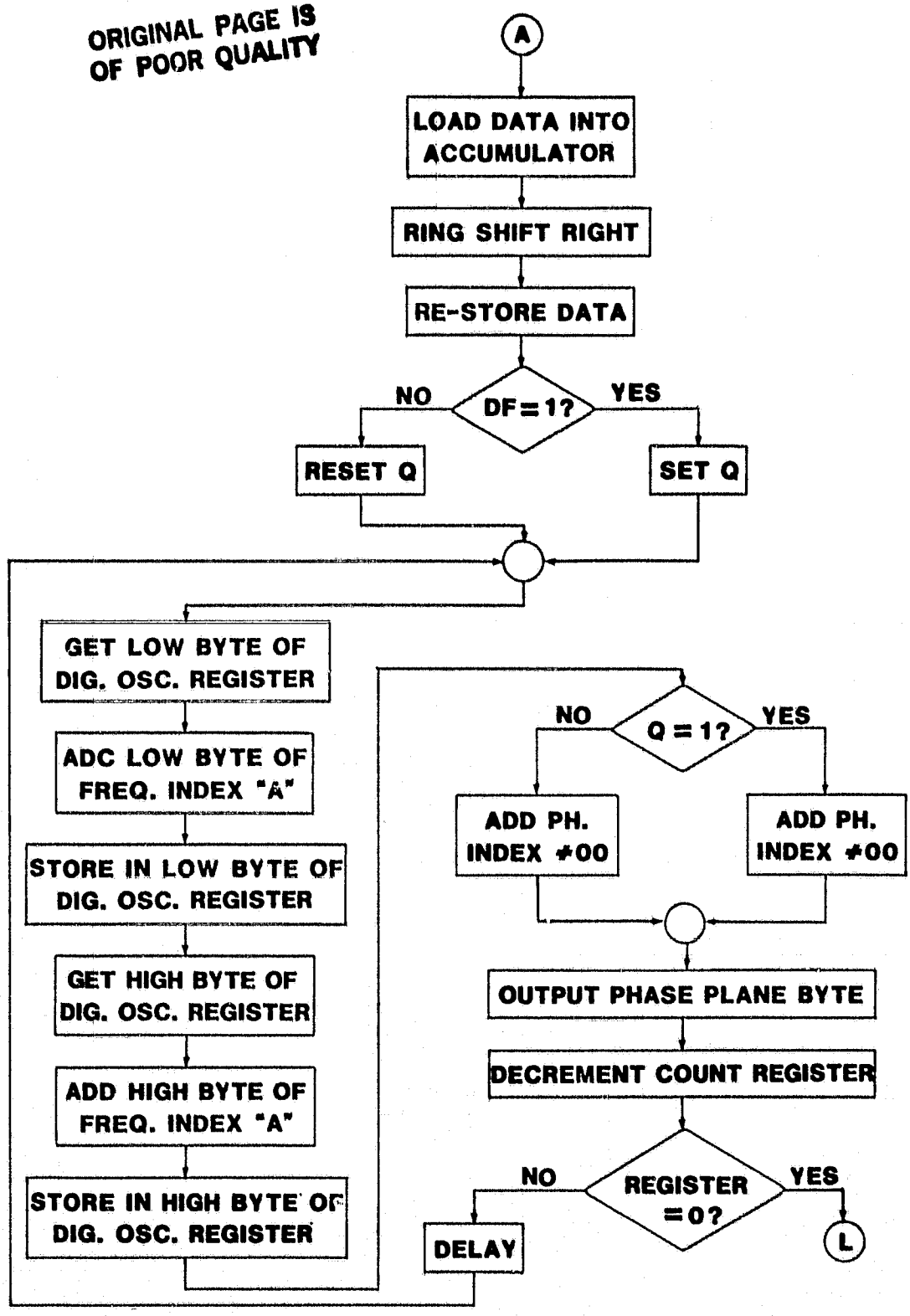

Figure 2.3.1. Continued.

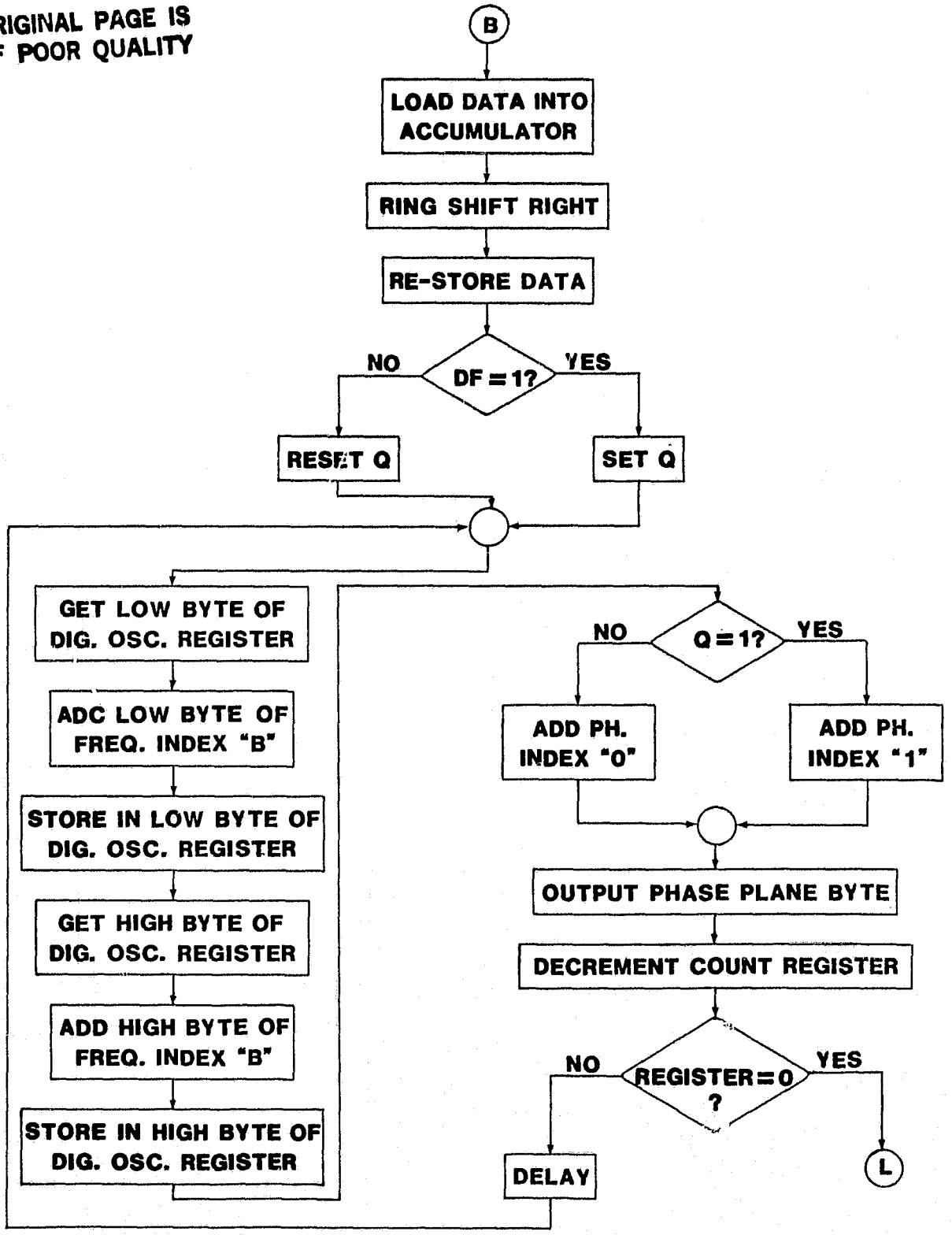

Figure 2.3.1. Continued.

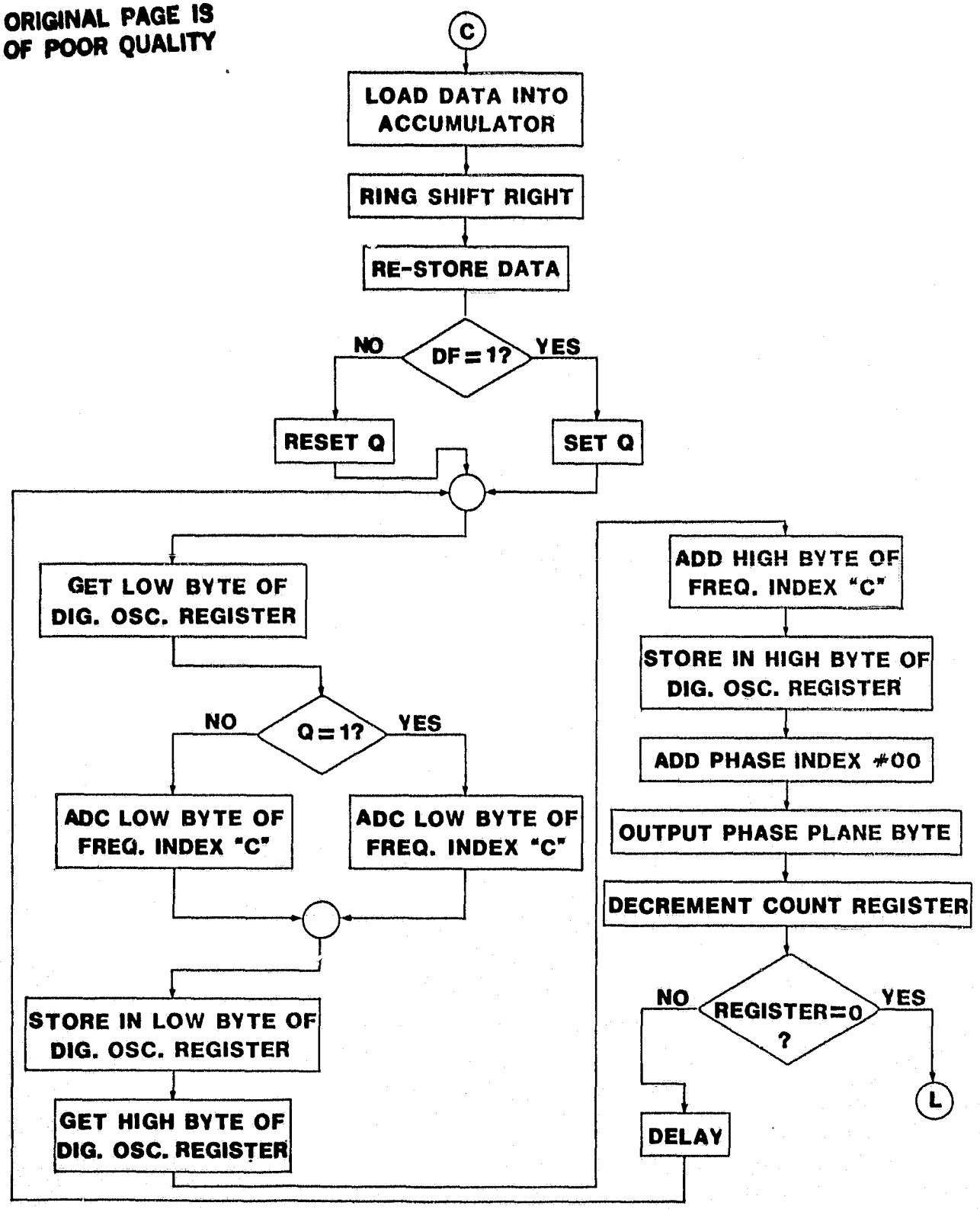

Figure 2.3.1. Continued.

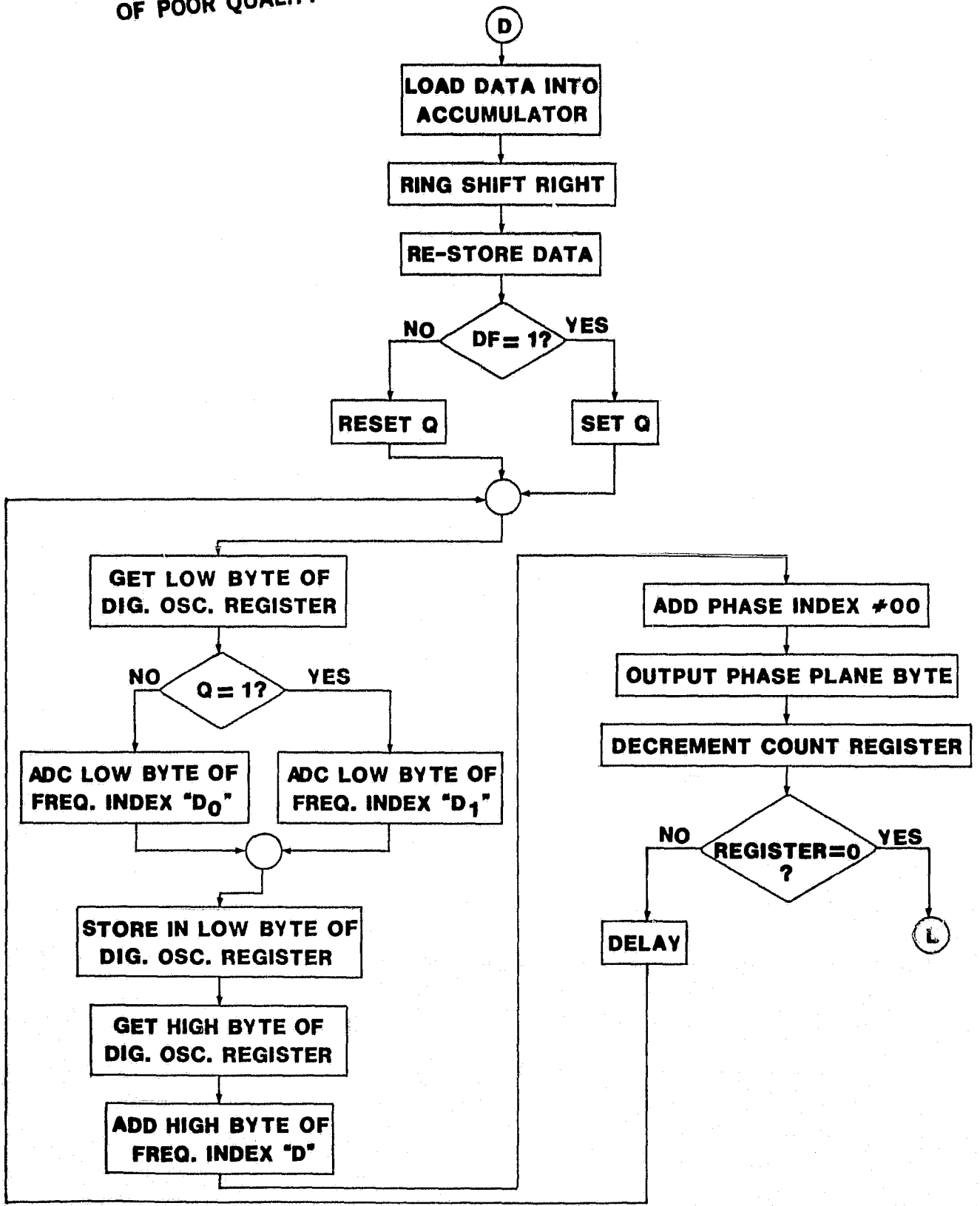

Figure 2.3.1. Continued.

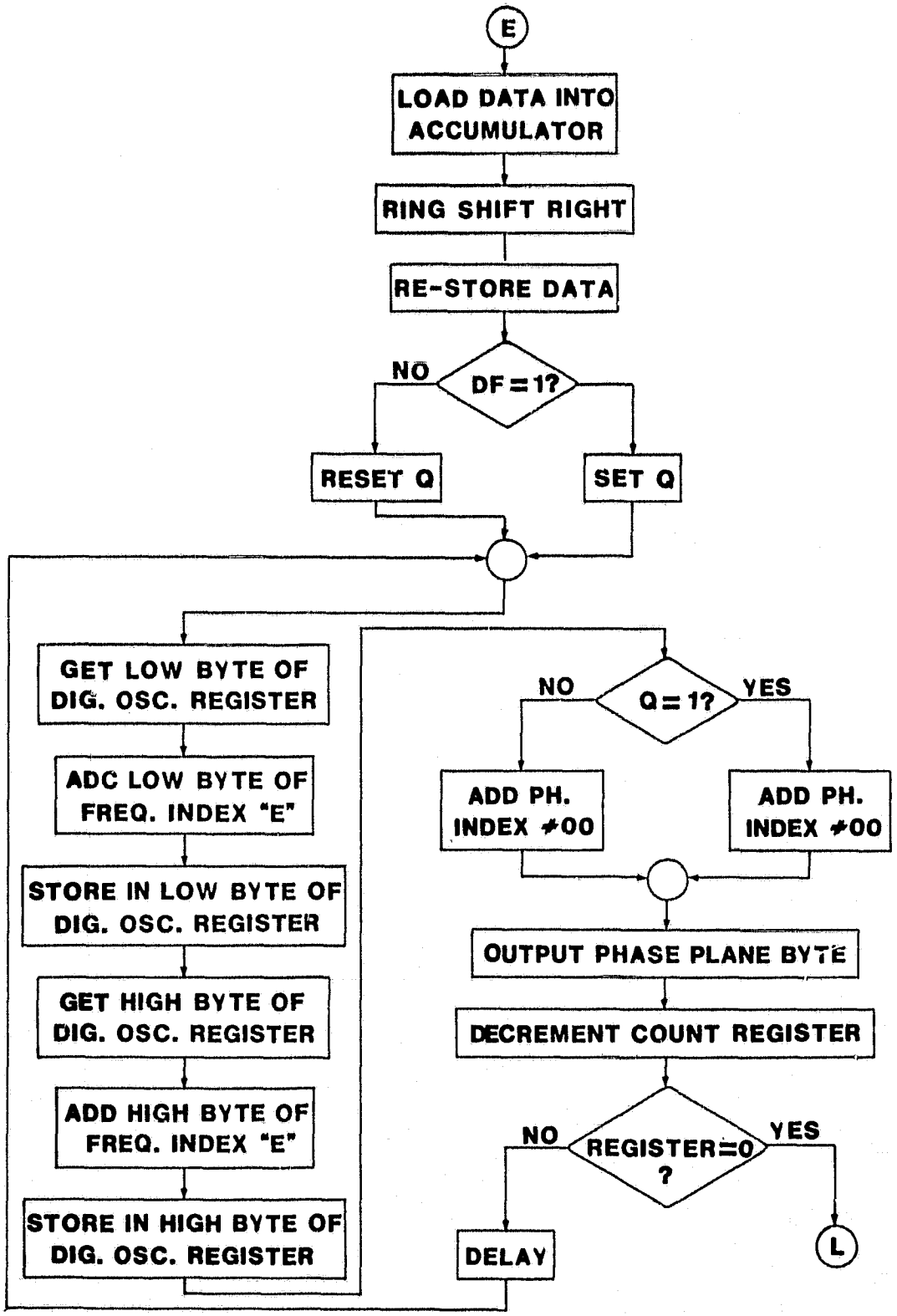

Figure 2.3.1. Continued.

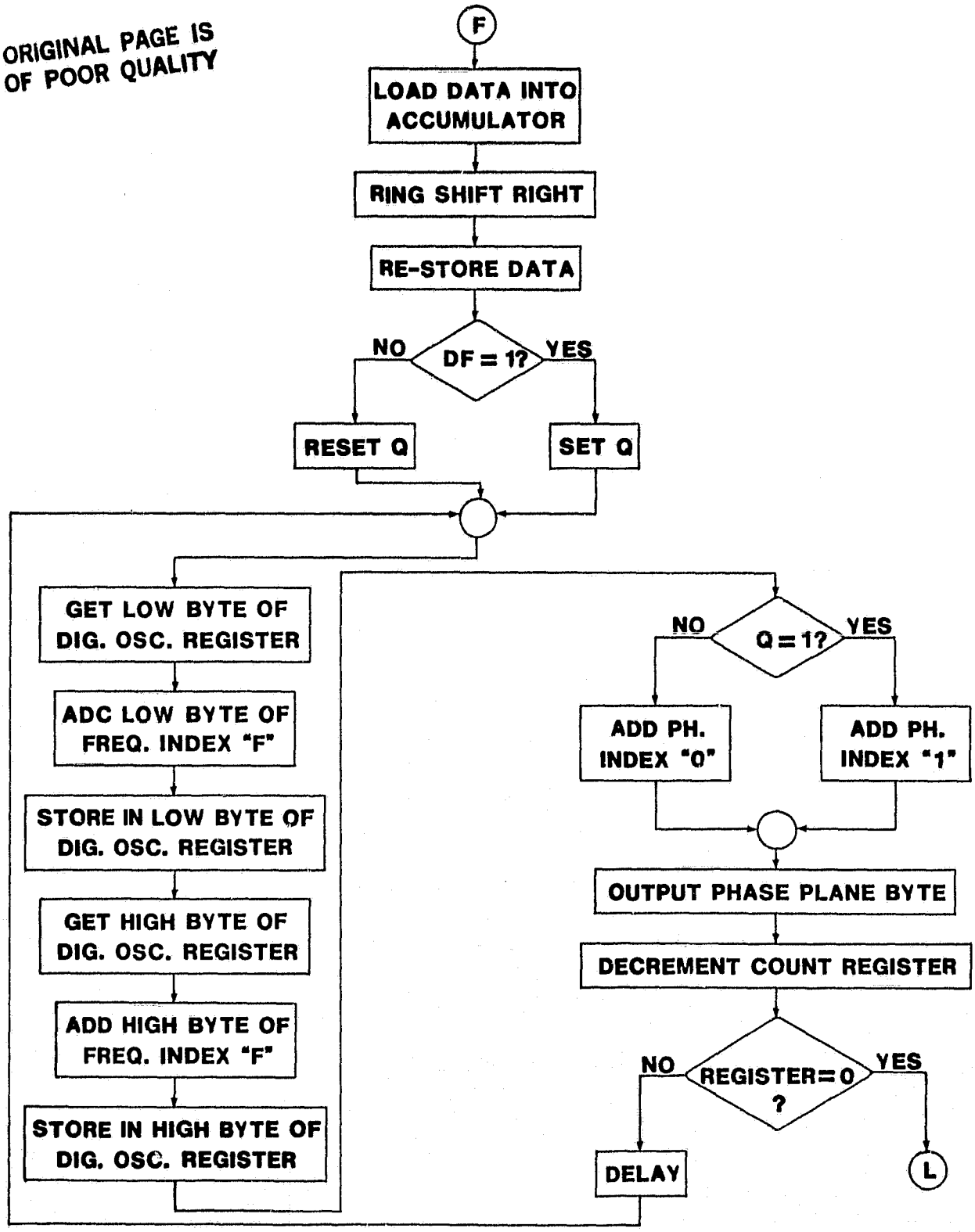

Figure 2.3.1. Continued.

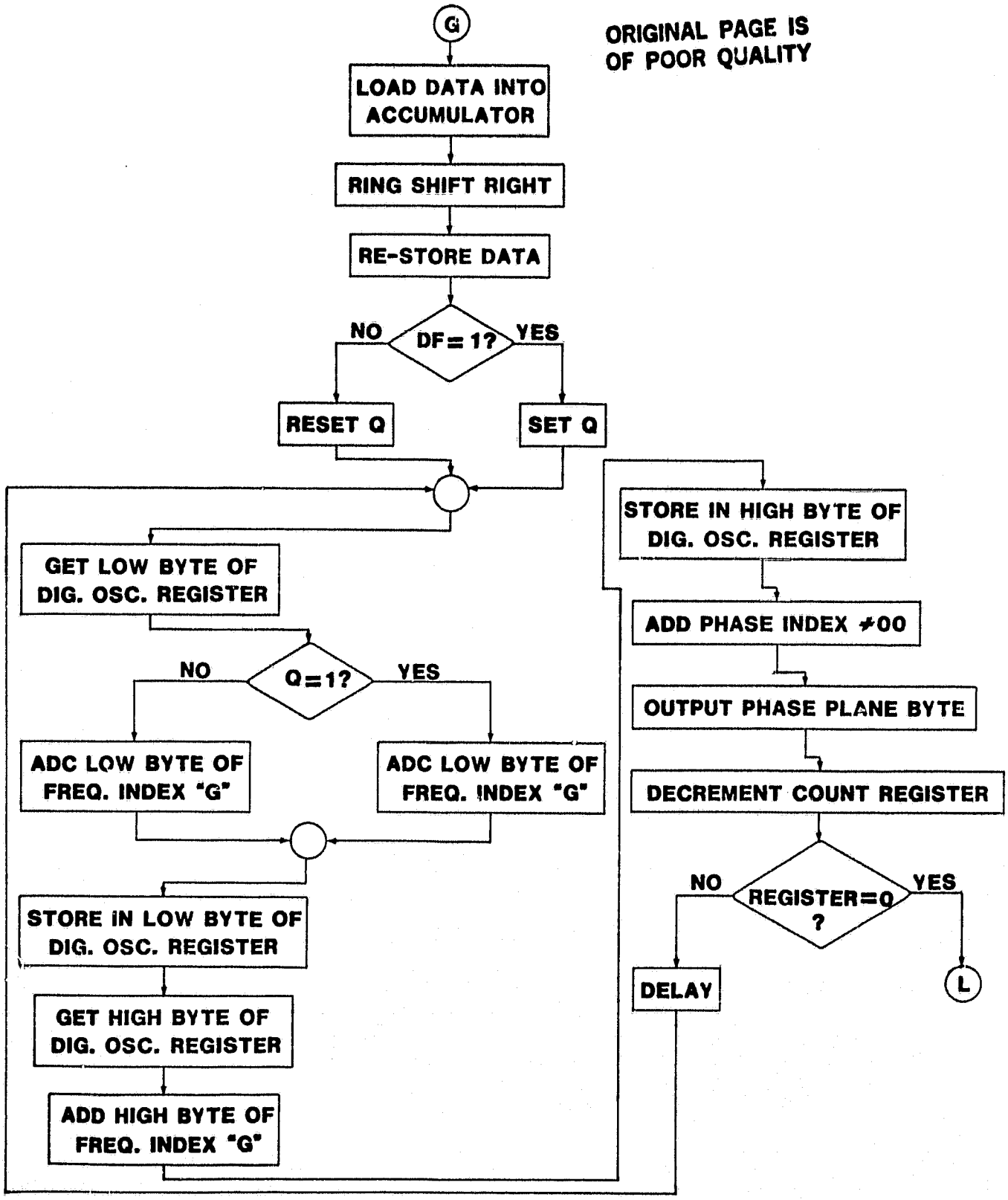

Figure 2.3.1. Continued.

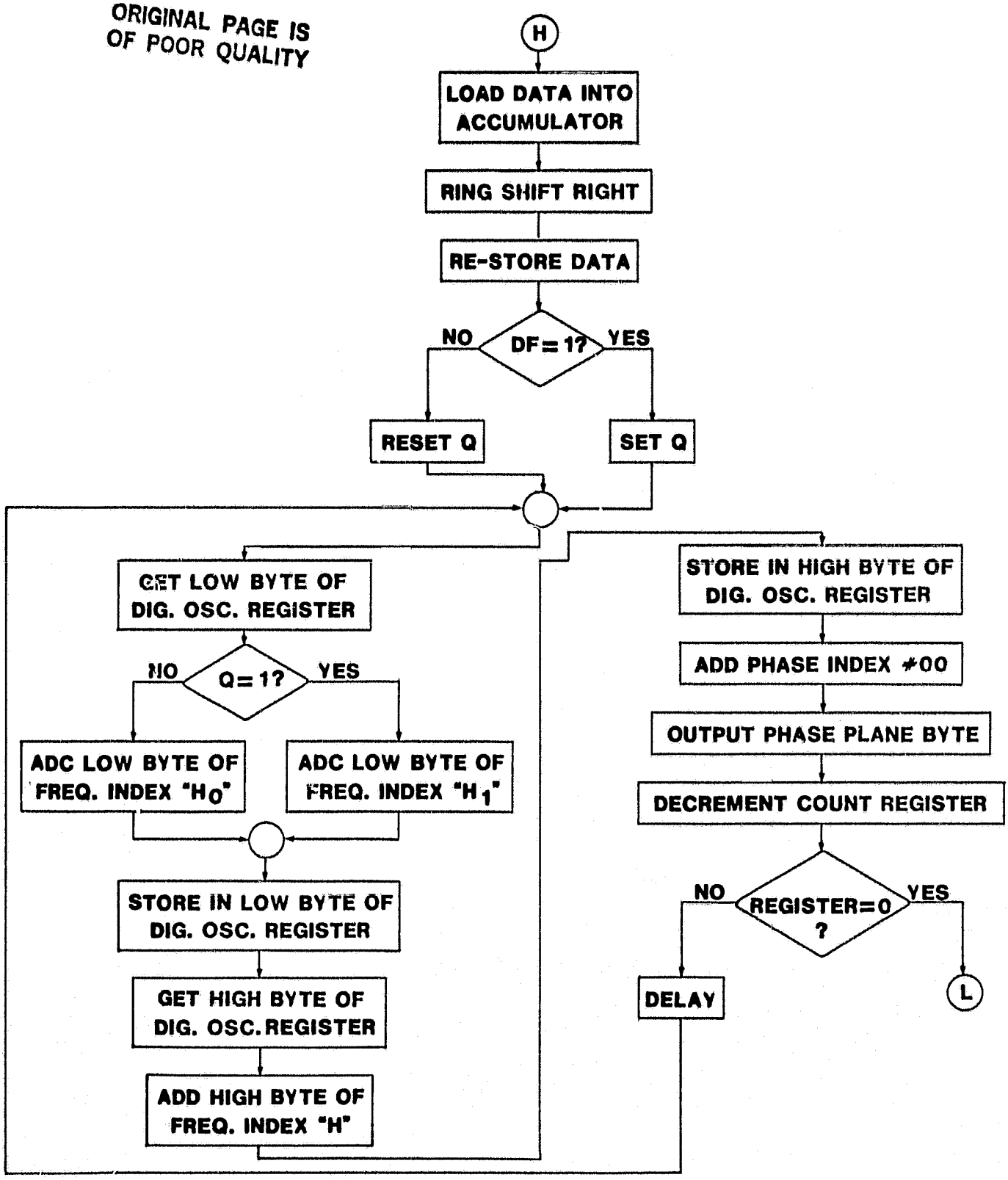

Figure 2.3.1. Continued.

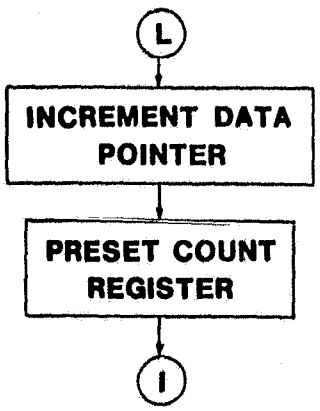

Figure 2.3.1. Continued.

fundamental bandwidth superiority of MSK over PSK for a given bit rate.

The total digital oscillator subroutine loop requires 60 machine cycles, or 150μS; this results in an effective f_{CLK} of 6.667kHz for the 16-bit wide simulated digital oscillator. The output carrier frequency is roughly one decade lower, or 665Hz. The output frequency is determined by the position of the $\overline{EF3}$ switch (f_{LO}/f_{HI} select) and the $\overline{EF2}$ width (rest/operate select); in the "operate" mode the $\overline{EF3}$ function selects a "low" (approx. 651 Hz) or "high" (682Hz) carrier frequency. Furthermore, in the MSK mode the output frequency is shifted with continuous phase to a higher or lower value, depending on the data bit just read from the data block in RAM. The MSK deviation number represents 64 steps in frequency; 1024 add cycles of the digital oscillator function occur per data bit period. All frequency-and phase-control loops (A through H) are timed to cause synchronous transitions of data and oscillator clock signals to ensure that all transitions are continuous-phase and glitch-free. The Q flip-flop output from the microprocessor is available for monitoring the actual data bit train, although its transitions are slightly advanced in time compared with the changes in phase-plane output bytes.

As can be seen from Figure 2.3.1, subroutines A through H are each very similar in format. The only differences are in the actual values of Frequency Index and Phase Index numbers entered in each case. Also, routines A, B, E, and F switch the Phase Index according to the data bit value and thereby generate PSK; analogously, routines C, D, G, and H vary the Frequency Index according to the data bit and thus create MSK modulation.

In the main program, R0 is the program counter; R6 serves as the digital oscillator clock loop counter. The data block pointer is R7; R8

is used as the 16-bit digital oscillator accumulator; and R9 is the phase plane pointer [3].

2.3.2. Demonstration Software for 8080A

To facilitate demonstration of the Universal Modulator functions on commonly available hardware, a routine to simulate the digital oscillator technique of MSK/PSK generation has been developed for use on the 8080A microprocessor. The program has been written specifically for the Intel Intellec MDS-800 system, but it may be run (with minor modifications to accomodate system hardware implementation differences) on any 8080A/Z-80 based system [4]. The basic flow charts are shown in Figure 2.3.2.

The basic program functions are similar to the previously mentioned 1802 routines. The data is retrieved from a block stored in RAM, shifted to convert the parallel-formatted storage to a serial stream, and finally used to select the appropriate Frequency Index and Phase Index numbers for the digital oscillator routine.

The 8080A register pairs are used in several modes to produce as efficient a code as possible. The D&E register pair serve as the pointer for the phase plane RAM block; B&C serve as the digital oscillator accumulator; and H&L combine functions as the data pointer and as a clock loop counter. Since the 8080A does not have external flag inputs comparable to $\overline{EF1}$ through $\overline{EF4}$ on the 1802, the various routines are selected by front-panel interrupt switches (0-7) on the Intellec system. Each interrupt switch via hardware causes a vectored restart to one of eight locations (#00, #08, #10, #18, #20, #28, #30, or #38) which in turn force an unconditional jump to one of eight control subroutines. Each of these subroutines, although similar to the others, has unique Frequency Index

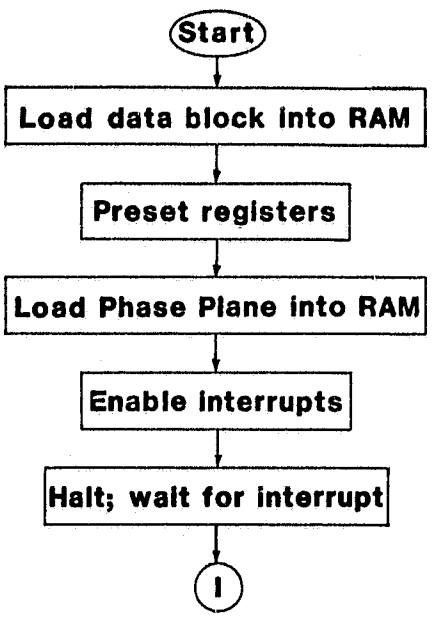

Figure 2.3.2. Basic Flow Chart for 8080A MSK/PSK Demonstration Program.

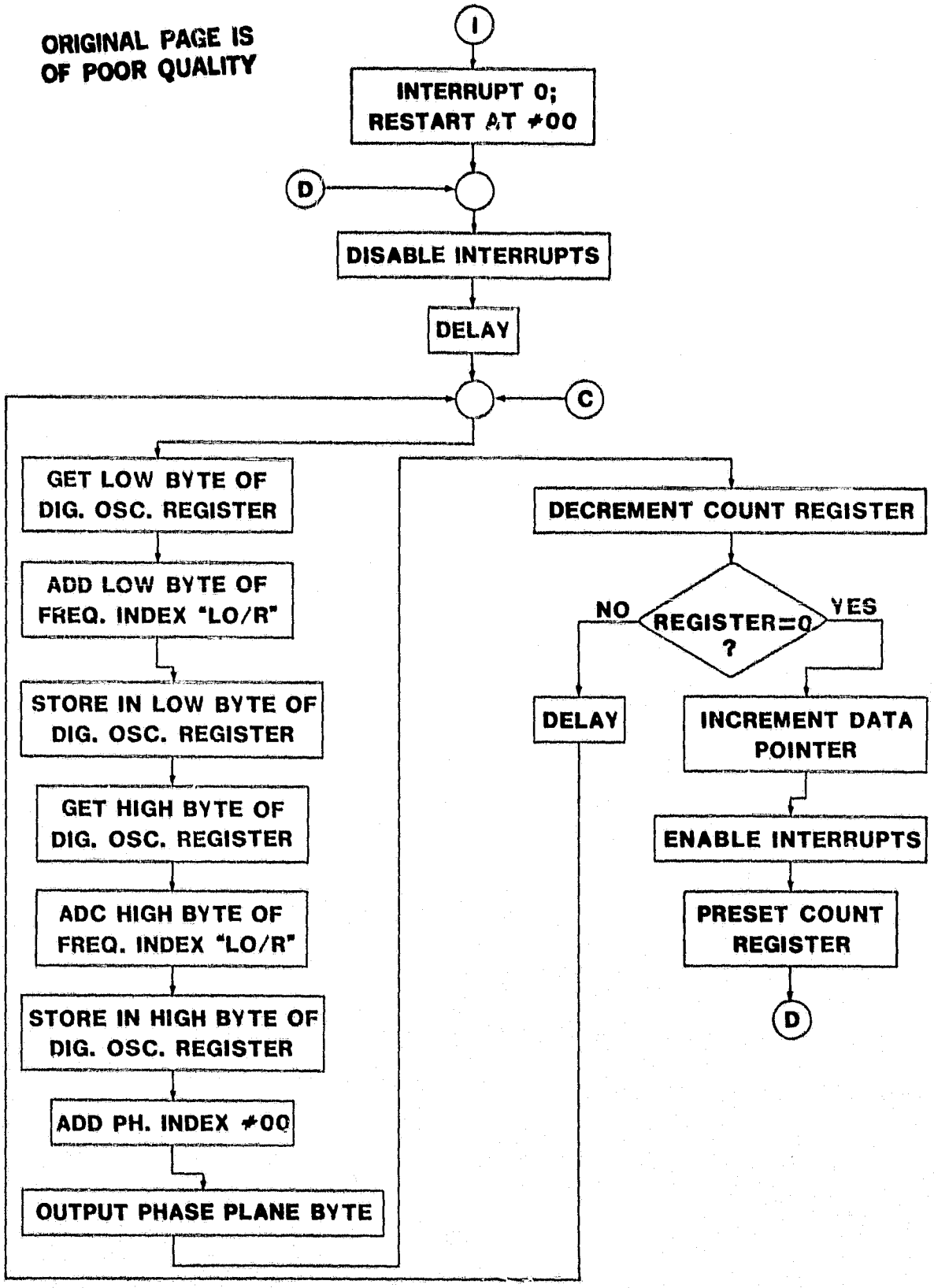

Figure 2.3.2. Continued.

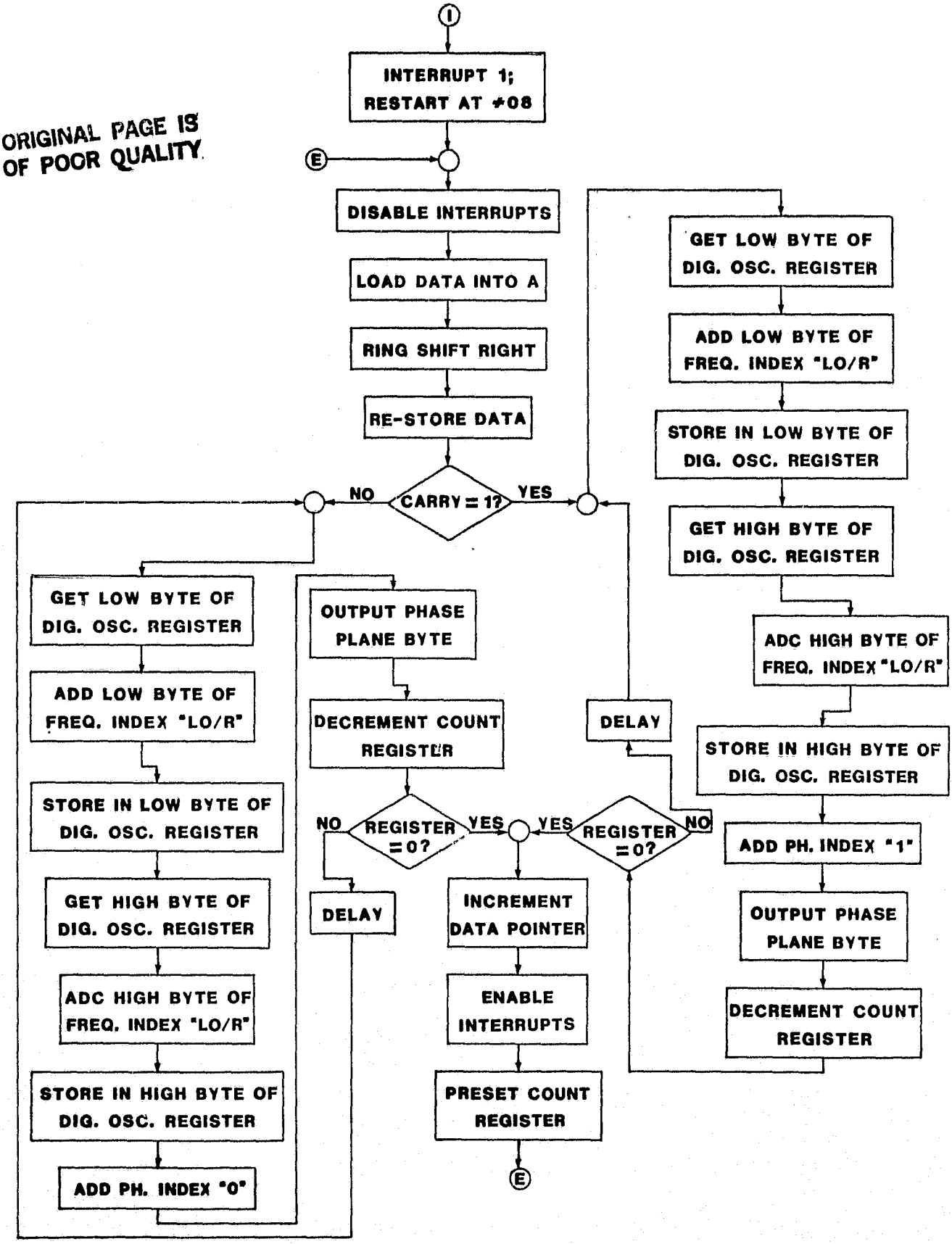

Figure 2.3.2. Continued.

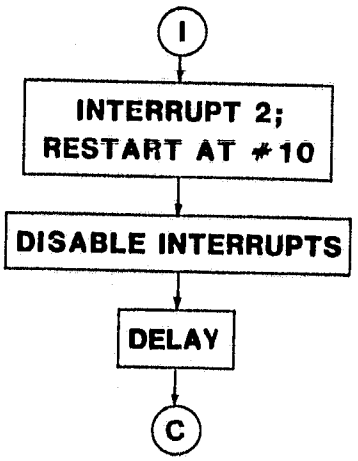

Figure 2.3.2. Continued.

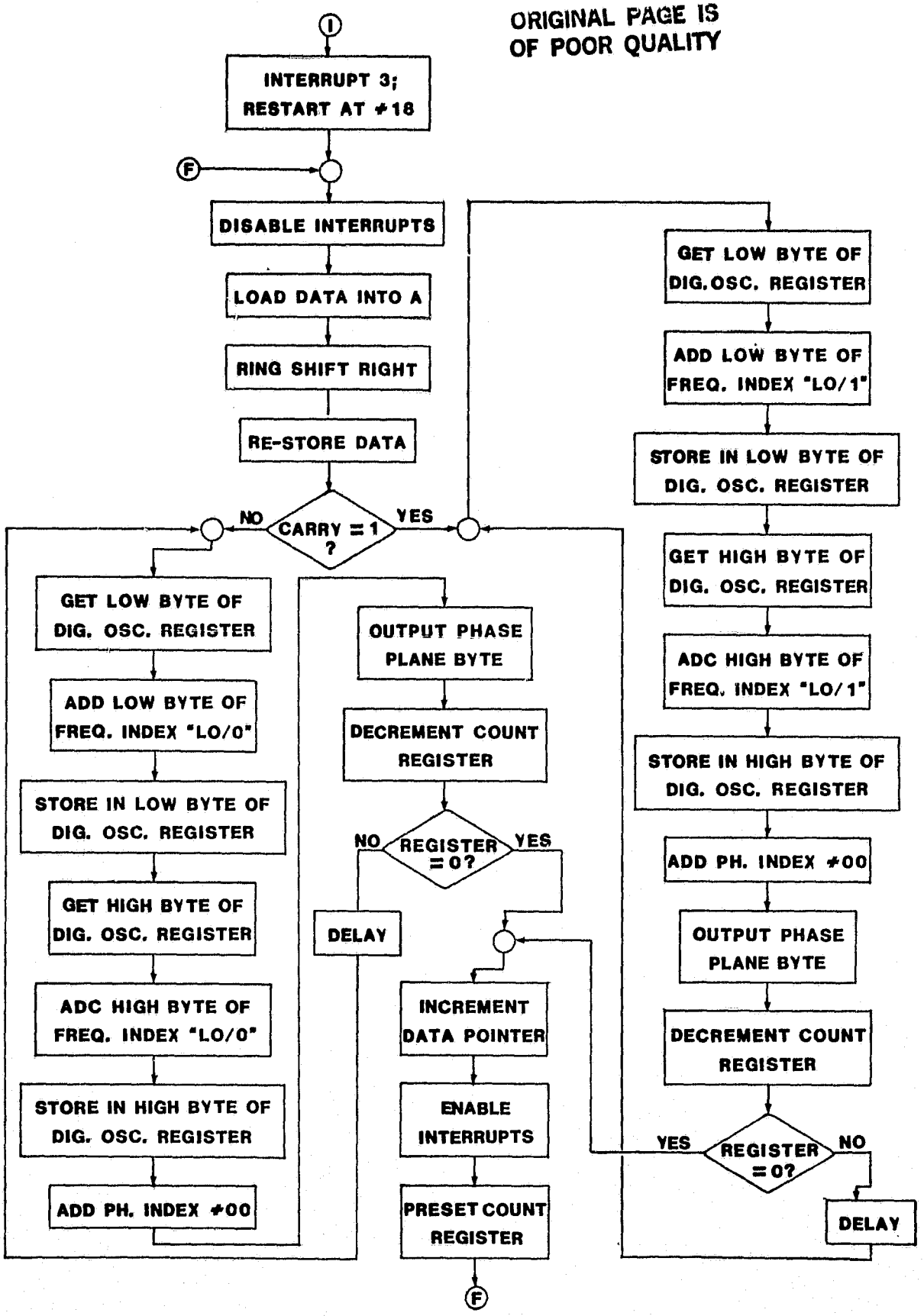

Figure 2.3.2. Continued.

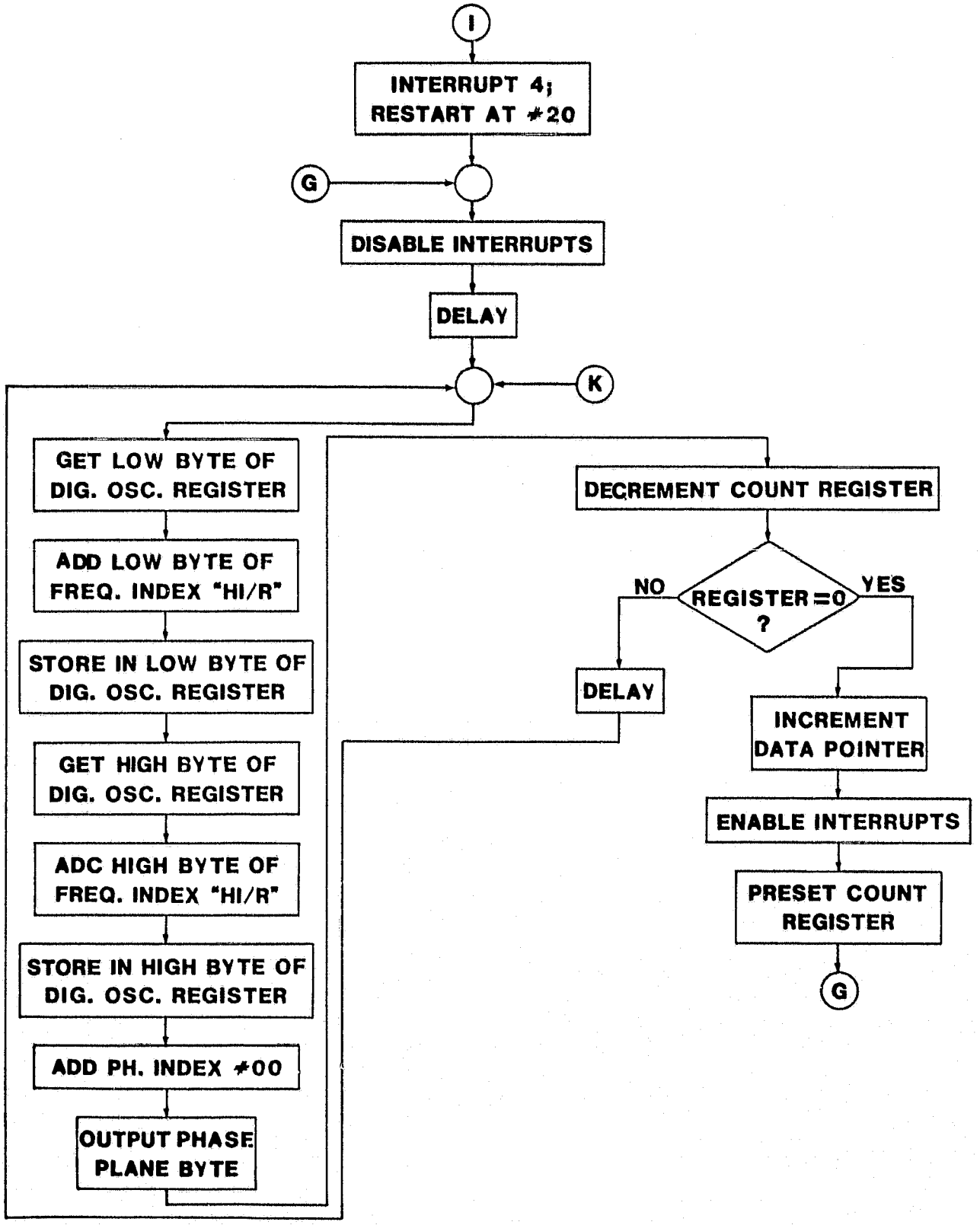

Figure 2.3.2. Continued.

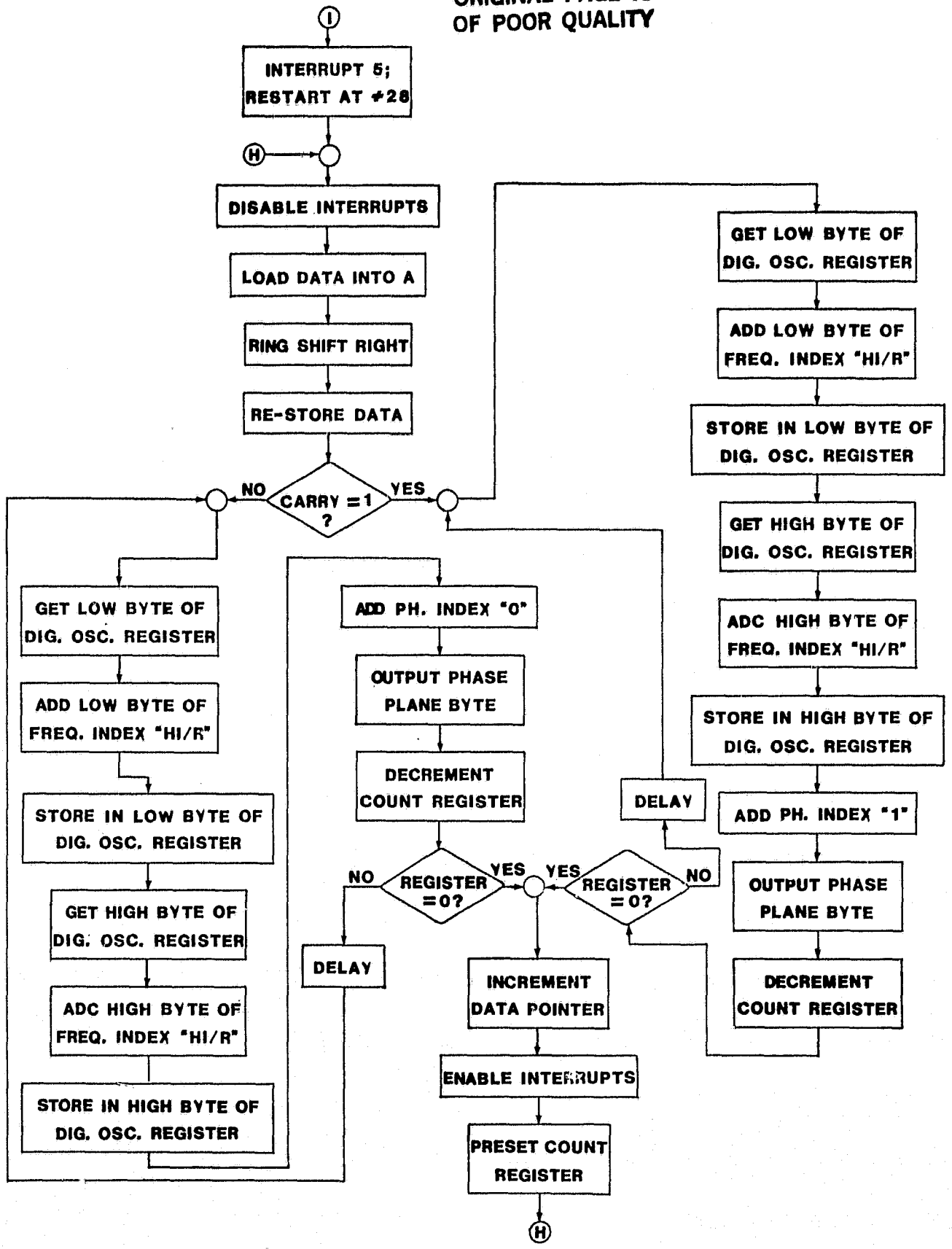

Figure 2.3.2. Continued.

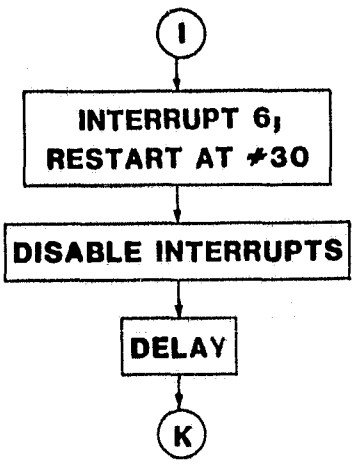

Figure 2.3.2. Continued.

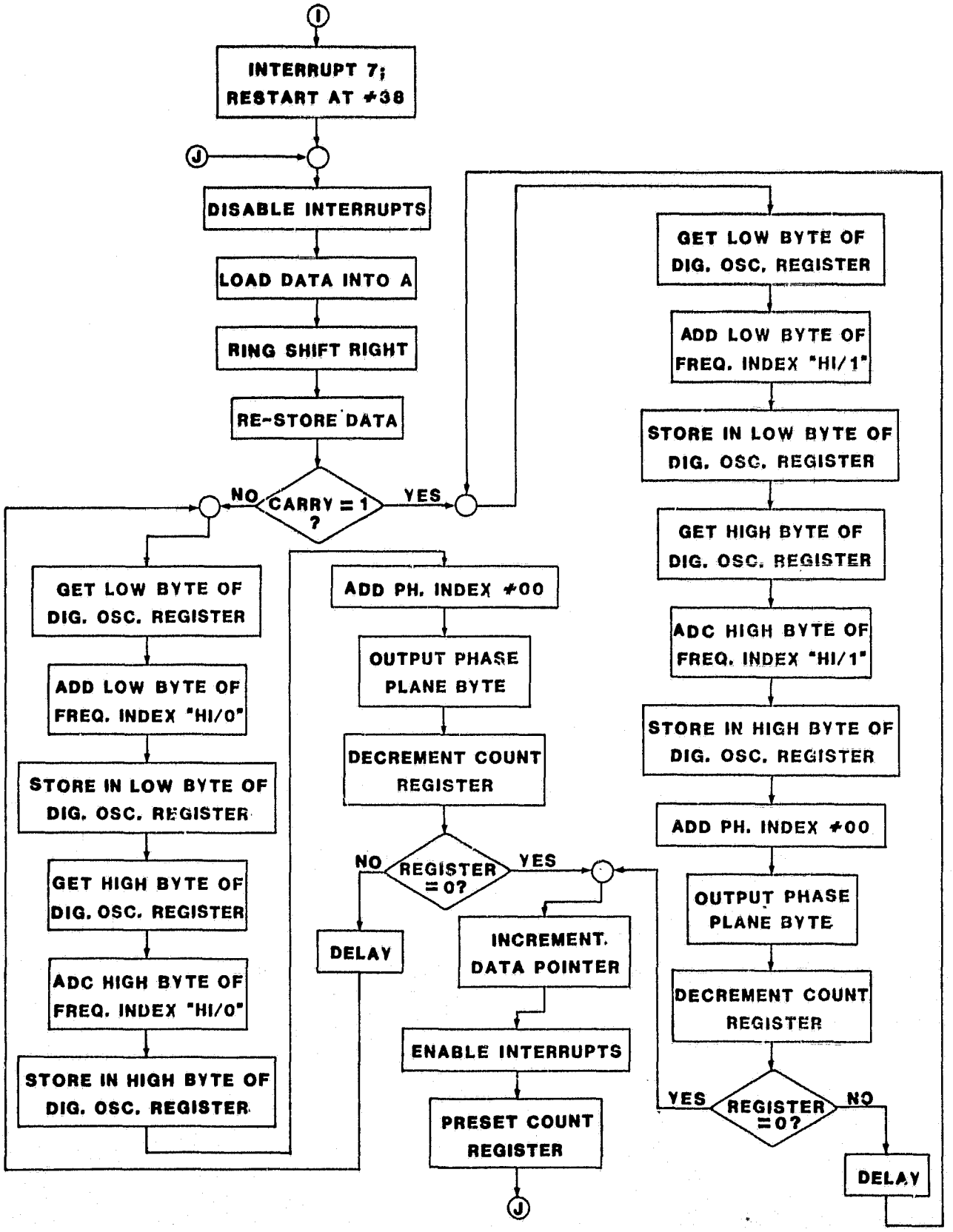

Figure 2.3.2. Continued.

and Phase Index constants which specify the mode of modulation, operating frequency, and the rest/operate state of the system. As with the 1802 demonstration package, the 8080A routine outputs the phase plane values to an 8-bit parallel output port which feeds a digital-to-analog converter that produces the desired analog output. For demonstration of the MSK/PSK generation technique this analog output may be amplified and applied to a loudspeaker in the same manner as with the 1802 setup.

As noted in Table 2.3.2, routines 0 through 3 operate at a lower carrier output frequency than routines 4 through 7. The even-numbered routines are standby programs which produce a clear (unmodulated) carrier, whereas the odd-numbered ones provide for MSK or PSK modulation. Routines 1 and 5 generate PSK; MSK is produced by branching to subroutines 3 and 7. Each subroutine is structured to provide a constant execution time for each program loop; in addition, all the subroutines have identical overall execution times since the effective bit rate must remain constant. Each routine samples for interrupts once per bit period; if no interrupt is detected, the routine in control continues. The delays inserted at various positions in the flow diagrams are used to equalize the loop times to meet the constant bit-rate requirement.

2.4 HARDWARE DESIGN CONSIDERATIONS

The actual clock frequencies, register lengths, and bit rates required from the digital oscillator system are functions of the specific applications of the DCP. In particular, the four principal satellites currently in service have specific RF frequencies, data formats, modulation forms, and bit rates which must be accomodated by the overall PDCP/UM unit. The task of synthesizing the proper data bit streams via the 1802

Interrupt	Function	Restart Location
0	f_{LO}/PSK/Rest	#00
1	f_{LO}/PSK/Operate	#08
2	f_{LO}/MSK/Rest	#10
3	f_{LO}/MSK/Operate	#18
4	f_{HI}/PSK/Rest	#20
5	f_{HI}/PSK/Operate	#28
6	f_{HI}/MSK/Rest	#30
7	f_{HI}/MSK/Operate	#38

Table 2.3.2. Restart Locations and Parameters for 8080A Demonstration Software.

microprocessor has been successfully achieved at the University of Tennessee [5]. The major impetus for the "Universal Modulator" task was to utilize the 1802 in the generation of the several useful forms of data modulation as well as control by microprocessor of the final RF transmitting frequencies.

At the outset of this contract NASA personnel offered a list of basic features or specifications which were desirable for the satellite data collection service. Table 2.4 summarizes these requirements, which represent systems used currently as well as in the forseeable future. As can be seen, MSK is anticipated to be the dominant form of modulation in future DCP systems, followed by PSK. Since the Landsat satellite has no apparent successor, it seems that the narrowband, low-bit-rate systems are destined to dominate the data-collection field. In addition, personnel from the National Space Testing Laboratory at Bay St. Louis, Mississippi have suggested that MSK may be tried on the GOES satellite in the near future, which further strengthens the position that MSK is the wave of the future.

2.4.1 Original PDCP/UM Design Parameters

The original hardware requirements for the PDCP/UM system were based on the current group of operational data-collection satellites (TIROS-N, GOES, LANDSAT, and NIMBUS-F) and on the projected availability of a snap-diode frequency multiplier which could convert a 50MHz signal to roughly 400MHz for use in the satellite band. Table 2.4.1.1 gives the satellites, types of modulation, and RF frequencies required. On the basis of the snap-diode unit's frequency multiplication factor of eight, the

System Parameter	Current Specification	Future Specifications
(1) Output frequency	401.2 - 401.85MHz	400 - 403MHz
(2) Output power	2 - 5 Watts	2 - 5 Watts
(3) Modulation types	FSK, PSK	MSK,PSK,FSK,CW
(4) Modulated bit rates	200Hz - 5kHZ	100Hz - 10kHz
(5) Number of channels	1 - 99 per satellite	approx. 100 max. per sat.
(6) Operational life	$\frac{1}{2}$ - 1 year	1 - 2 years min.
(7) Dominant modulation mode	PSK	MSK
(8) Power consumption	∿ 100mW avg.	< 100mW avg.
(9) Frequency control	hardware (xtal)	software (μP)
(10) Modulation control	hardware system	software (μP)
(11) Automatic frequency control	none	via WWV
(12) Programmable operation	no	yes
(13) Automatic emergency operation	no	yes
(14) Overall cost ($K)	approx. 5-10	approx. 2-4
(15) Reliability (overall)	good	excellent

Table 2.4. Basic Requirements for PDCP/UM System

Satellite	Frequency	Modulation Format	Effective Bit Rate	Approx. Trans. Power
NIMBUS-F (TWERLE)	401.20MHz	PSK, ±60°	200Hz	600mW
TIROS-N (ARGOS)	401.65MHz	PSK, ±60°	800Hz	3W
LANDSAT (ERTS)	401.55MHz	FSK, ±5kHz	5kHz	5W
GOES (SMS)	401.70-401.85MHz	PSK, ±60°	200Hz	5W

Table 2.4.1.1. Current Satellite Standards for DCPs.

desired system parameters were calculated from Equations 2.2.1 and 2.2.2 to give the final output frequencies and deviations.

As noted from Equation 2.2.2, the minimum frequency increment is given by

$$\Delta f_{min} = \frac{f_{CLK}}{2^n},$$

where n is the number of digital oscillator accumulator bits. For a 16-bit-wide accumulator, $2^n = 65{,}536$. Now the clock frequency can be determined from the output frequency constraints:

$$\Delta f_{RF} = 8 \cdot \Delta f_{OUT} \qquad \text{(Eqn. 2.4.1.1)}$$

$$\Delta f_{RF} \cong 1499\text{Hz (GOES)} \qquad \text{(Eqn. 2.4.1.2)}$$

$$\Delta f_{RF} = 5000\text{Hz (LANDSAT)} \qquad \text{(Eqn. 2.4.1.3)}$$

$$\Delta f_{OUT} = \frac{1}{8} \cdot \Delta f_{RF} \qquad \text{(Eqn. 2.4.1.4)}$$

The average interchannel frequency spacing for the GOES satellite is 1499.97143Hz; this becomes a constraint on the step size Δf_{OUT} and thus the clock frequency f_{CLK}. Another requirement is that the CPFSK frequency deviation for the LANDSAT system is 5kHz. Obviously, these two constraints cannot be satisfied accurately by a single clock frequency, so two different clocks must be employed - one for GOES, NIMBUS-F, and TIROS-N, and the other for LANDSAT. For the former,

$$\Delta f_{OUT_1} = \frac{1}{8} \cdot 1499.07143\text{Hz} = 187.38393\text{Hz} \qquad \text{(Eqn. 2.4.1.5)}$$

$$f_{CLK_1} = \Delta f_{OUT_1} \cdot 2^{16} = \qquad \text{(Eqn. 2.4.1.6)}$$

$$(187.38393)(65{,}536) \cong 12.280393\text{MHz}$$

CHANNEL NUMBER	OUTPUT FREQUENCY MHZ
1	401.700,996
2	401.702,495
3	401.703,994
4	401.705,493
5	401.706,992
6	401.708,491
7	401.709,990
8	401.711,489
9	401.712,989
10	401.714,448
11	401.715,987
12	401.717,486
13	401.718,985
14	401.720,484
15	401.721,983
16	401.723,482
17	401.724,981
18	401.726,480
19	401.727,979
20	401.729,478
21	401.730,977
22	401.732,476
23	401.733,976
24	401.735,475
25	401.736,974
26	401.738,473
27	401.739,972
28	401.741,471
29	401.742,970
30	401.744,469
31	401.745,968
32	401.747,467
33	401.748,966
34	401.750,465
35	401.751,964
36	401.753,463
37	401.754,962
38	401.756,462
39	401.757,961
40	401.759,460
41	401.760,959
42	401.762,458
43	401.763,957
44	401.765,456
45	401.766,955
46	401.768,454
47	401.769,953
48	401.771,452
49	401.772,951
50	401.774,450

CHANNEL NUMBER	OUTPUT FREQUENCY MHZ
51	401.775,949
52	401.777,449
53	401.778,948
54	401.780,447
55	401.781,946
56	401.783,445
57	401.784,944
58	401.785,443
59	401.787,942
60	401.789,441
61	401.790,940
62	401.792,430
63	401.793,938
64	401.795,437
65	401.796,935
66	401.798,435
67	401.799,935
68	401.801,434
69	401.802,933
70	401.804,432
71	401.805,931
72	401.807,430
73	401.808,929
74	401.810,428
75	401.811,927
76	401.813,426
77	401.814,925
78	401.816,424
79	401.817,923
80	401.819,422
81	401.820,922
82	401.822,421
83	401.823,920
84	401.825,419
85	401.826,918
86	401.828,417
87	401.829,916
88	401.831,415
89	401.832,914
90	401.834,413
91	401.835,912
92	401.837,411
93	401.838,910
94	401.840,409
95	401.841,908
96	401.843,408
97	401.844,907
98	401.846,406
99	401.847,905

Table 2.4.1.2 GOES Satellite Channel Frequencies

For the latter,

$$\Delta f_{OUT_2} = \frac{1}{8} \cdot 5000Hz = 625Hz \qquad \text{(Eqn. 2.4.1.7)}$$

$$f_{CLK_2} = \Delta f_{OUT_2} \cdot 2^{16} = 40.96MHz \qquad \text{(Eqn. 2.4.1.8)}$$

In the first calculation, Δf_{OUT_1} has been assumed to be one step and the resultant f_{CLK_1} is a reasonable value. However, f_{CLK_2} is too high a frequency to be handled by low-power hardware, so Δf_{OUT_2} is now assumed to be four steps in digital oscillator frequency. The new clock frequency is:

$$\Delta f_{OUT_2} = \frac{1}{8} \cdot \frac{1}{4} \cdot 5000Hz = 156.25Hz \qquad \text{(Eqn. 2.4.1.9)}$$

$$f_{CLK_2} = \Delta f_{OUT_2} \cdot 2^{16} = 10.24MHz \qquad \text{(Eqn. 2.4.1.10)}$$

which is more suitable. Note that both clock frequencies satisfy the general constraints of Section 2.2 in that both are roughly 1000 times greater than the highest desired data rate ($\approx$ 10kHz) and about an order of magnitude greater than the desired digital oscillator output frequency of roughly 1MHz. This figure was chosen principally as a compromise between ease of generation and the need to ensure that any image frequencies generated by the translation/multiplication process following the digital oscillator will not fall within the satellite band of interest. Since the digital oscillator produces a roughly 1MHz output with channel spacings of one-eighth the desired final RF frequency steps, the D/A output must be mixed with a local oscillator signal before being multiplied up to the 401MHz band. Using the above values for f_{CLK_1} and a typical GOES transmitting frequency from Table 2.4.2, the local oscillator frequency will be:

$$\text{GOES channel \#50} = 401.774450\text{MHz} \qquad \text{(Eqn. 2.4.1.11)}$$

$$\text{Input to X8 Multiplier} = 50.22180625\text{MHz} \qquad \text{(Eqn. 2.4.1.12)}$$

$$f_{OUT} = \frac{(F.I.)(f_{CLK_1})}{2^{16}} = \frac{(5503)(12.28039315\text{MHZ})}{65{,}536} \approx 1.03117376\text{MHz} \qquad \text{(Eqn. 2.4.1.13)}$$

$$f_{L.O.} = 50.22180625 - 1.03117376 = 49.19063249\text{MHz} \qquad \text{(Eqn. 2.4.1.14)}$$

The local oscillator is simply used to translate the digital oscillator signal up to the 50.22180625MHz frequency which feeds the X8 multiplier system. This multiplier may be implemented by either exotic methods such as microwave snap diodes or may simply be three cascaded frequency-doubler stages using standard UHF biolar or field-effect transistors.

A basic constraint of this approach to generating the operating frequency is that of the image frequencies produced in the mixing process. From Equation 2.4.14 it is evident that the sum-frequency output of the mixer is the desired signal (at 50.22180625MHz), but the difference (image) frequency at 48.15945873MHz is also present and is applied to the multiplier block just as the desired signal is. The final result will be a spurious signal, somewhat attenuated by the RF selectivity of the transmitter, which lies at 385.2756698MHz, some 16.49878MHz below the desired signal on GOES channel 50.

Four benefits are obtained from this separation in frequency of the main and image signals. First, the image lies outside the standard satellite DCP transmitting band and thus presents no danger of interference to other DCPs. Second, the image is sufficiently removed from the main channel that a simple transmission-line trap may be applied if necessary

to effectively notch out the image. Third, since the signal is aimed essentially upward from the ground, there would be little possibility of harmful interference to land-based communications. Finally, there is probably no need for an expensive high-selectivity filter following the mixer stage; this would help keep system costs low.

Using the previously determined values for the various system oscillator frequencies, the system parameters for several satellite channels can be enumerated and are presented in Table 2.4.1.3. Included are data for the LANDSAT, TIROS-N, NIMBUS-F frequencies and three typical channels on the GOES system.

From a quick examination of the table it is evident that the local oscillator and clock frequencies have been tailored to the requirements of the GOES satellite, since due to its 99 channels it is the most sensitive of the four systems to transmitter frequency errors. The other units, being somewhat more forgiving in this respect, are still served with frequency errors of no more than 0.75ppm. In addition, the CPFSK produced for LANDSAT use yields previsely the ±500OHz frequency deviation required by the satellite; in addition, the +60Hz offset in center frequency is negligible compared with the Doppler shifts present with LANDSAT. Interestingly enough, by using one-fourth the normal deviation, MSK can be directly synthesized for use on LANDSAT with absolutely no change in hardware.

The F.I. and P.I. figures indicate the decimal values and the actual equivalent hexadecimal numbers gated into the digital oscillator by the data-handling microprocessor to effect the modulation- and frequency-control functions. The phase increments of ±5 units generate ±7.03125° phase shifts at the digital oscillator output; this phase deviation is then multiplied by eight in the succeeding RF circuitry to generate ±56.25° of phase shift at the final RF carrier frequency, which is within 6.25% of the nominal ±60° deviation and is well within the specification limits of current DCP transmitters.

f_{CLK_1} = 12.28039315MHz (GOES/TIROS-N/NIMBUS-F)

f_{CLK_2} = 10.2400000MHz (LANDSAT)

$f_{L.O.}$ = 49.19063249MHz

Multiplication factor = 8

SATELLITE	OUTPUT FREQ(MHz)	FREQ. ERROR	DIG. OSC. FREQ.(MHz)	F.I.(DECIMAL/HEX)	P.I.(DECIMAL/HEX)
TIROS-N(Rest)	401.650027	+27Hz	1.01562089	5420/152C	0/00
(Bit=0)	401.650027	+27Hz	1.01562089	5420/152C	-5/FB
(Bit=1)	401.650027	+27Hz	1.01562089	5420/152C	+5/05
NIMBUS-F(Rest)	401.200306	+306Hz	0.95940571	5120/1400	0/00
(Bit=0)	401.200306	+306Hz	0.95940571	5120/1400	-5/FB
(Bit=1)	401.200306	+306Hz	0.95940571	5120/1400	+5/05
LANDSAT(Rest)	401.550060	+60Hz	1.00321500	6420/1914	0/00
(Bit=0)	401.545060	+60Hz	1.00250000	6416/1910	0/00
(Bit=1)	401.555060	+60Hz	1.00375000	6424/1918	0/00
GOES#1(Rest)	401.700996	0Hz	1.02199195	5454/154E	0/00
(Bit=0)	401.700996	0Hz	1.02199195	5454/154E	-5/FB
(Bit=1)	401.700996	0Hz	1.02199195	5454/154E	+5/05
GOES#50(Rest)	401.774450	0Hz	1.03117376	5503/157F	0/00
(Bit=0)	401.774450	0Hz	1.03117376	5503/157F	-5/FB
(Bit=1)	401.774450	0Hz	1.03117376	5503/157F	+5/05
GOES#99(Rest)	401.847905	0Hz	1.04035557	5552/15B0	0/00
(Bit=0)	401.847905	0Hz	1.04035557	5552/15B0	-5/FB
(Bit=1)	401.847905	0Hz	1.04035557	5552/15B0	+5/05

Table 2.4.1.3 Parameters for Original PDCP/UM Configuration.

2.4.2 Modified Hardware Configuration

At the request of Goddard personnel, the previously discussed design was modified in order to utilize a currently available NIMBUS-F DCP transmitter manufactured by Handar[6]. This unit is configured as a chain of RF amplifier/multiplier stages which takes a master oscillator input signal of a few milliwatts at 10.03MHz and multiplies the frequency by a factor of 40 to get to the 401.2MHz satellite channel. Phase-shift control inputs for $\pm 60°$ deviation are provided to allow the DCP to modulate the RF outputs; application of +12 volts to the appropriate terminals will produce RF with -60°, 0°, or +60° phase, respectively[7].

With the overall RF frequency multiplication ratio set to 40, the digital oscillator clock and local oscillator frequencies must be altered to provide the desired output frequencies and deviations from the PDCP/UM system. Analogously to Equations 2.4.1.5 - 2.4.1.14, the resulting calculations are:

$$\Delta f_{OUT_1} = \frac{1}{40} \cdot 1499.07143\text{Hz} = 37.47678575\text{Hz} \qquad \text{(Eqn. 2.4.2.1)}$$

$$f_{CLK_1} = \Delta f_{OUT_1} \cdot 2^{18} = 9.824314524\text{MHz} \qquad \text{(Eqn. 2.4.2.2)}$$

$$f_{CLK_2} = 10.240000\text{MHz} \qquad \text{(Eqn. 2.4.2.3)}$$

$$\text{GOES channel \#50} = 401.774450\text{MHz} \qquad \text{(Eqn. 2.4.2.4)}$$

$$\text{Input to X40 Multiplier} = 10.04436125\text{MHz} \qquad \text{(Eqn. 2.4.2.5)}$$

$$f_{OUT} = \frac{(F.I.)(f_{CLK_1})}{2^{18}} = \frac{(26{,}635)(9.824314524\text{MHz})}{262{,}144} \approx 0.998194188\text{MHz} \qquad \text{(Eqn. 2.4.2.6)}$$

$$f_{L.O.} = 10.04435125 - 0.998194188 = 9.046167062\text{MHz} \qquad \text{(Eqn. 2.4.2.7)}$$

Thus as in the original setup a single translation of the digital oscillator output frequency is accomplished with a UHF - type mixer and a heterodyning local oscillator. The result of this mixing process, namely signals at 10.04436125MHz (the desired frequency) and 8.047972874MHz (the image), is applied to the X40 multiplier chain to produce the final RF signal at 401.774450MHz and an attenuated spurious component at 321.918915MHz. As before, this spurious signal lies outside the satellite band and is unlikely to cause harmful interference to other communications.

Since the required frequency step size at the output of the digital oscillator system is only one-fifth the step size the original configuration, it became necessary to modify both of the oscillator frequencies and to increase the resolution of the digital oscillator itself. This was accomplished by adding another 4-bit full adder block and lengthening the accumulator register. The resultant 18-bit digital oscillator has 2^2, or 4 times the frequency resolution of its 16-bit counterpart. The rest of the required resolution increase was obtained by reducing the digital oscillator clock frequency to exactly 4/5 of its original value. Table 2.4.2.1 gives the calculated output frequencies and frequency/phase indices for several satellite channels.

A potential drawback to the use of this specific system configuration involves the rather high frequency multiplication factor of the RF amplifier chain in the Handar transmitter. Because the output phase deviation at the final carrier frequency is 40 times greater than the input phase deviation, the digital oscillator must be limited to only

f_{CLK_1} = 0.824314524MHz (GOES/TIROS-N/NIMBUS-F)

f_{CLK_2} = 10.2400000MHz (LANDSAT)

$f_{L.O.}$ = 9.046167062MHz

Multiplication factor = 40

SATELLITE	OUTPUT FREQ.(MHz)	FREQ. ERROR	DIG. OSC. FREQ.(MHz)	F.I.(DECIMAL/HEX)	P.I.(DECIMAL/HEX)
TIROS-N(Rest)	401.650027	+27Hz	0.99508362	26,552/67B8	0/00
(Bit=0)	401.650027	+27Hz	0.99508362	26,552/67B8	-1/FF
(Bit=1)	401.650027	+27Hz	0.99508362	26,552/67B8	+1/01
MINBUS-F(Rest)	401.200306	+306Hz	0.98384058	26,252/668C	0/00
(Bit=0)	401.200306	+306Hz	0.98384058	26,252/668C	-1/FF
(Bit=1)	401.200306	+306Hz	0.93484058	26,252/668C	+1/01
LANDSAT(Rest)	401.5498076	-192Hz	0.99257813	25,410/6342	0/00
(Bit=0)	401.5451200	+120Hz	0.99246094	25,407/633F	0/00
(Bit=1)	401.5544948	-505Hz	0.99269531	25,413/6345	0/00
GOES#1(Rest)	401.700996	0Hz	0.99635783	26,586/67DA	0/00
(Bit=0)	401.700996	0Hz	0.99635783	26,586/67DA	-1/FF
(Bit=1)	401.700996	0Hz	0.99635783	26,586/67DA	+1/01
GOES#50(Rest)	401.774450	0Hz	0.99819419	26,635/680B	0/00
(Bit=0)	401.774450	0Hz	0.99819419	26,635/680B	-1/FF
(Bit=1)	401.774450	0Hz	0.99819419	26,635/680B	+1/01
GOES#99(Rest)	401.847904	-1Hz	1.00003055	26,684/683C	0/00
(Bit=0)	401.847904	-1Hz	1.00003055	26,684/683C	-1/FF
(Bit=1)	401.847904	-1Hz	1.00003055	26,684/683C	+1/01

Table 2.4.2.1. Parameters for Modified PDCP/UM Configuration.

±1.5° shift to produce the nominal ±60° shift at carrier. Due to the digitization of amplitude and phase of the output from the phase plane ROM, there is a finite amount of phase jitter produced by the digital oscillator, on the order of 1/4° RMS. This jitter will be multiplied by the RF chain to produce approximately 10° of jitter at carrier, which is excessive for high-quality data transmission. It was therefore decided to utilize the PSK capabilities of the Handar transmitter to ensure clean phase-modulated signals and reserve the frequency-synthesis functions for the digital oscillator.

The basic hardware configuration utilizes low-power Schottky TTL chips to simultaneously provide the low propagation delay times and the moderate power consumption levels necessary for a practical field model digital oscillator system. The adders are 54/74LS283 types, and 54/74LS174 hex "D" flip-flops are used for the accumulator register. The phase plane is an 82S114 which has an output data latch to reduce output data bit skew; the D/A converter is a high-speed current-output bipolar type to give sufficiently fast settling times to accurately represent the output waveform changes which occur at the roughly 10MHz clock rate. All clock signals are controlled externally by the 1802 microprocessor and are generated on another system board. The 1852 8-bit I/O ports and their associated 1853 decoder are used to load the 8-bit "Phase Index" and 16-bit "Frequency Index" and "Frequency Number" constants utilized with the 1802 software to control all PDCP oscillator frequencies. The complete schematic diagram for the digital oscillator subassembly may be found in Appendix II.

REFERENCES

1. Final Report Addendum for the Design and Demonstration of An Advanced Data Collection/Position Locating System. Texas Instruments, Incorporated, NASA Contract NAS5-23599, May, 1978.

2. Pasupathy, S., "Minimum Shift Keying: A Spectrally Efficient Modulation", IEEE Communications Magazine, July, 1979, pp. 14-22.

3. RCA Solid State Division, User Manual for the CDP1802 COSMAC Microprocessor. RCA Corporation, Somerville, New Jersey, 1977.

4. Intellec Microcomputer Development System Reference Manual. Intel Corporation, Santa Clara, California, 1976, pp. 3-37 through 3-41.

5. Programmable Data Collection Platform System, Phase II. University of Tennessee, NASA Contract NAS5-22495, May, 1978.

6. Letter from J. Earle Painter to Dr. Robert W. Rochelle, NASA-Goddard Space Flight Center, Greenbelt, Maryland, file 10344, April 26, 1978.

3. MICROPROCESSOR BOARDS

3.1 INTRODUCTION

The heart of the PDCP/UM system is the hardware used to implement the microcomputer functions. The basic unit for the U-T PDCP system is the CDP1802 microprocessor, along with its associated RAM, ROM, I/O, and decoding circuits. For the field PDCP/UM application, it was desirable to utilize CMOS technology, in order to keep the system power consumption at an absolute minimum; thus the 1802 was selected. Its power drain at bias levels of $V_{DD} = V_{CC} = 5$ volts is only 10mW during program execution and 5mW standby ("idle" mode); for the alternate bias of $V_{DD} = 10V$ and $V_{CC} = 5V$, the levels are 30mW and 15mW, respectively.

As the list of functions required of the overall PDCP/UM system grew, it became evident that using a single CPU, although theoretically feasible, placed severe constraints on system software structure and timing. Although the original PDCP data-reduction and formatting routines could be combined with the necessary frequency-and modulation-control algorithms without a significant loss in PDCP calculation and/or data analysis capability, the new timekeeping routines caused too many complications for the software design of the system. Specifically, the real-time clock and its companion WWV-decoding program had to be precisely timed in order to keep the platform on a consistently accurate chronological base. Since each segment of these new programs required exact matching of loop execution times in order to maintain synchronization with the WWV time-code transitions, and since a major goal of the present PDCP development effort is to allow simple, flexible software control of all significant DCP functions in order to ease the end-user's task of

programming, it was decided to utilize a second 1802 microprocessor to perform the WWV-based timekeeping and cueing functions.

The second 1802 (μP_0) by virtue of its hardware interconnections is able to initiate an unconditional jump to any location in the main (μP_1) memory by causing a main-unit interrupt and then supplying a one-byte table address which may point to any 16-bit address in the μP_1 memory. A simple interrupt routine stored in ROM then causes transfer within the μP_1 memory to the subroutine desired by the programmer. The above control mechanism is thus transparent to the user and the complex timing contained in the μP_0 WWV-decode and real-time clock programs does not exhibit any interaction with user routines. The significance of this feature is even greater when considering the applicability of higher-level languages such as BASIC or PASCAL to the PDCP data-analysis tasks likely to be required as the field develops further.

The basic function, then, of μP_0 is to continuously decode the 100-Hz digital BCD time code information supplied by the WWV receiver and its ancillary filter/detector and to use this information to continually update the data produced by a specialized real-time clock routine which produces a running count of actual time in days, hours, minutes, and seconds, accurate to within 15 milliseconds of actual WWV time. In addition, the clock program samples a block of data in PROM which contains the start time for any user-selected event (also in days, hours, minutes, and seconds), the interval between successive occurrences of the event (also in days, hours, minutes, and seconds), and the one-byte restart address for the event routine in μP_1 memory. The clock program then compares the desired event time with real time data and, if the two times match, executes the specified routine through μP_1 and simultaneously

updates the next event execution time by adding the interval data to it. The net result of all this is to provide the PDCP/UM system with the ability to start any desired data-handling routine contained in μP_1 memory at any desired time, without forcing the user to develop his own timekeeping software. Thus the end user can simply specify which routines he desires (and the time and order of their execution) in μP_0 PROM and then the routines themselves in μP_1 PROM; the preprogrammed supervisory routines do the rest. Under this arrangement, any convenient types of software languages may be employed by the user without regard for system timing, so long as sufficient time is allowed for a given event to complete execution before the next one is initiated.

Another significant advantage of this system implementation is that the PDCP does not have to have its first transmission set manually with the resultant time error in event execution. Instead, this operation is fully automatic; a front-panel LED will indicate to the technician setting up the PDCP in the field when proper lock with the WWV carrier frequency and time code has been established. It is therefore simply a matter of setting up the PDCP unit and transmitting antenna, turning the unit on, and waiting until the LED indicates synchronization with WWV. The prestored programs in ROM or EPROM do the rest and prevent any PDCP transmissions from occurring until all system oscillators are properly corrected to the WWV frequency standard and the BCD time code is acquired without error over a one-minute period. This ensures that no spurious transmission of improper frequency and/or timing will occur from the PDCP even under transient or fault conditions. If an error in timekeeping

occurs, the unit will not allow transmissions until the entire WWV-acquisition procedure is properly executed.

A further and quite powerful advantage of the two-microprocessor implementation is the versatility offered to system users. One might program the PDCP/UM to transmit to one satellite every 15 minutes (e.g., at 14, 29, 44, and 59 minutes past the hour) and alternately send to a second satellite on a different schedule (perhaps on every half-hour). Thus one PDCP could perform the functions of two or more conventional DCPs and simultaneously retain the capability to switch to still another satellite or channel for emergency functions (e.g., a seismic pickup, floodwater alarm, etc.).

3.2 CPU Board-μP_0

The function of the μP_0 CPU board is to perform the PDCP executive timekeeping functions. Figure 3.2. shows the basic block diagram of the card. The 1024x8 read-only memory system is comprised of two Intersil IM6554 512x8 CMOS EPROMs, each of which has a maximum access time of 450nS and a maximum dissipation of 100μW at $V_{DD} = V_{CC} = +5$ volts. These chips are used for the main program storage and also contain the user-defined functions such as event times and subroutine locations. The internal program code is partitioned so that for large-volume production of the PDCP system the low-order chip could be replaced with a 512x8 mask-programmed CMOS ROM such as the CDP1832 for lower cost. The program code occupies the low-order chip, and the user data is reserved for the top locations of the higher-order EPROM, thus allowing the custom programming of only one chip for this board. The timing signal ($\overline{E}_1$) for the onboard latches on the 6654s is derived from a Fairchild 4027 flip-flop

which is clocked by the TPA signal from the microprocessor. This chip is fabricated with the Isoplanar process, which produces a propagation delay roughly half that of conventional CMOS; this increased speed is necessary for reliable system timing.

The remainder of the system memory is embodied in two RCA CDP1822 256x4 RAMs which are operated in parallel to produce the desired 256x8 array. Latching and decoding of the 1802 memory address lines are accomplished in a CD4042 quad "D" latch and an associated CD4011 quad NAND gate chip, which provide the necessary enable and chip-select signals to the EPROMs as well as the RAMs. The 6654s occupy hex memory locations 0000 through 03FF; the 1822s are vectored between 0400 and 04FF, inclusive. The decoder block also provides a signal to the system interrupt indicator driver, as shown in the diagram.

The microprocessor itself has four external flag ($\overline{EF}$) inputs from other sections of the PDCP/UM system and is also tied to the master reset line for proper initialization at turn-on. There is also a single analog control line from the RF board which feeds a d-c control voltage to a varactor diode placed in the crystal-controlled frequency-determining network for the 1802 clock oscillator. This control voltage varies the varactor capacitance and thereby effects a small but finite shift in the 1802 clock frequency in order to exactly (within one part in 10^7) synchronize the 1802 output frequencies to the WWV standard. This accuracy is especially important in the MSK mode of operation, since the 10.24MHz digital oscillator clock reference frequency is phase-locked to the 3.2MHz microporcessor clock. The input to $\overline{EF3}$ is the squared-off waveform representing the BCD time-code modulation from the WWV receiver.

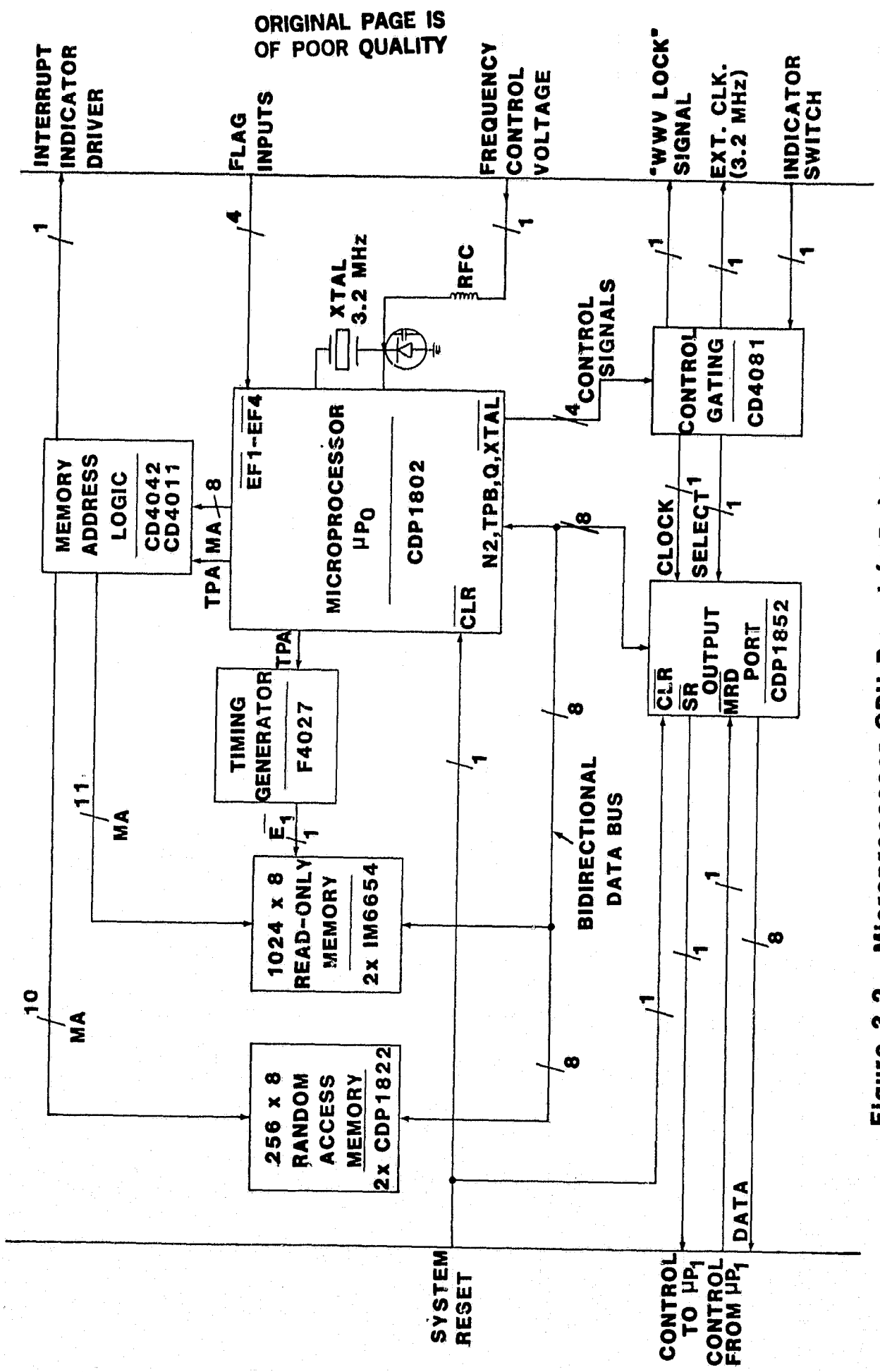

Figure 3.2. Microprocessor CPU Board (μP_0) Block Diagram.

The RF amplifier chip used in the WWV processor chain also has a squelch output, which is fed to $\overline{EF4}$ on the 1802 as an indicator of adequate WWV signal strength; if the received carrier level drops below the threshold of hard limiting, the microprocessor software will ignore the $\overline{EF3}$ data and revert to internal timekeeping routines.

The final major functional block on the μP_0 board consists of the CDP1852 I/O port and its associated control gating within the CD4081. It is the duty of the 1852 to present the address byte from μP_0 to the μP_1 bus during the system interrupt interval in order to effect the desired jump to a new routine in μP_1 memory as specified by the table data stored in μP_0 EPROM. The service request ($\overline{SR}$) line of the 1852 is connected directly to the $\overline{INT}$ input on μP_1. When the 1852 is loaded by μP_0 the internal service request flip-flop is set, causing $\overline{SR}$ to go low, thus forcing μP_1 to interrupt. An interrupt service routine then reads in the data word through the port and places it in the low-order byte of a 16-bit register. This register is subsequently used as a pointer to a table in ROM in which is stored the 16-bit starting address of the desired routine. This address is then loaded into another register, which is then designated the program counter, thus causing an unconditional jump to the location contained in the register.

3.3 CPU Board-μP_1

The CPU board for the main processor (μP_1) is very similar to the previously described μP_0 board. As before, the EPROM consists of two IM6654s, configured as a 1024x8 block of permanent storage and strobed from a high-speed Fairchild F4027 flip-flop driven by the TPA signal from the microprocessor. The RAM is comprised of two paralleled

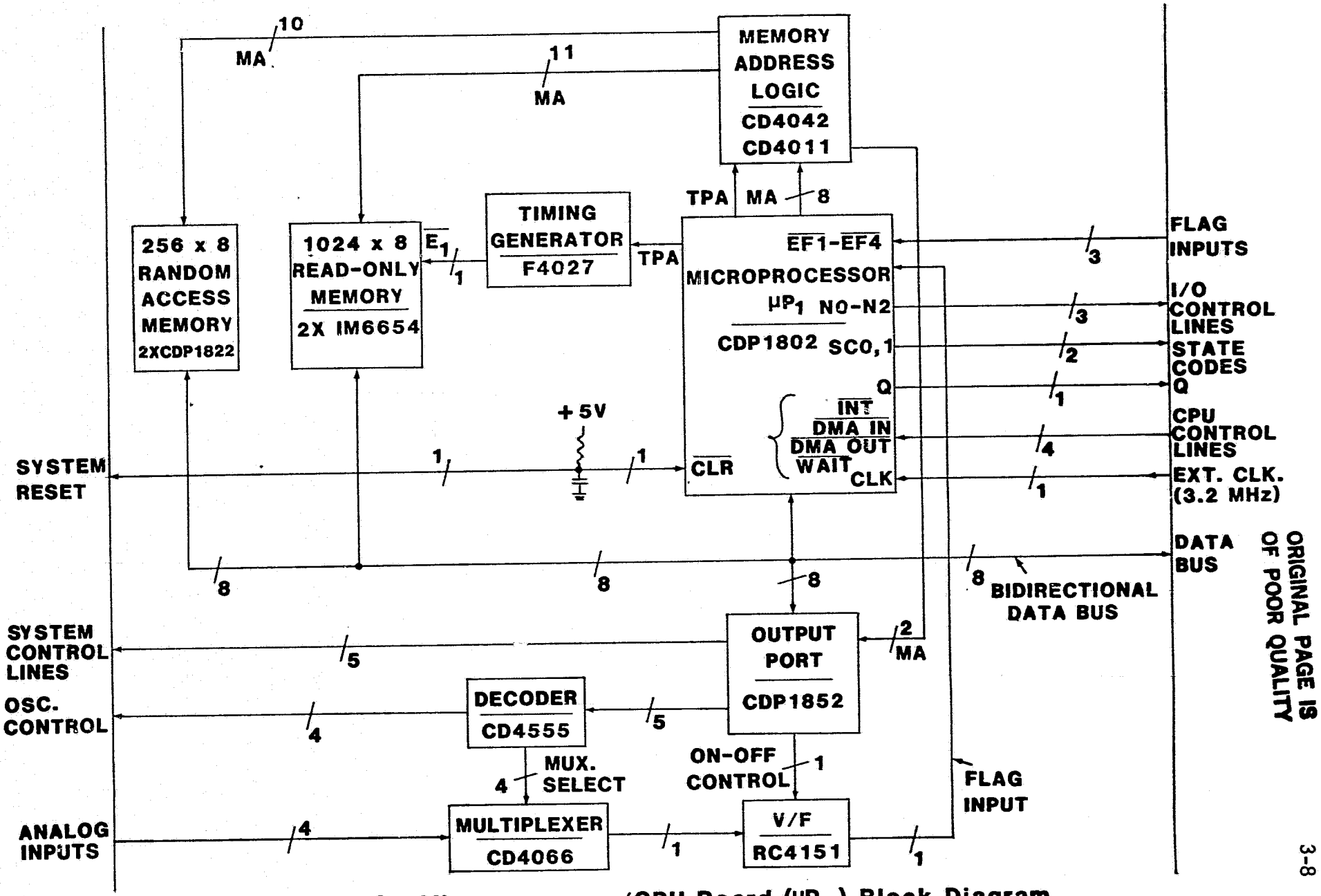

Figure 3.3. Microprocessor/CPU Board (μP_1) Block Diagram.

CDP1822s operating as a 256x8 read/write array, identical to the μP_0 setup.

As can be seen from Figure 3.3. , the memory address high-order byte is latched using TPA in a CD4042; the true/complement outputs of the chip are used to furnish several of the necessary address inputs to the 6654s. The remainder of the address decoding is done in the CD4011 quad NAND gate; the EPROMs as before occupy the hex memory locations from 0000 through 03FF and the RAM from 0400 through 04FF. Unlike the μP_0 setup, however, the 1852 I/O port is directly accessed by the CPU as a memory location (0600 hex).

The 1852 on this board is essentially used as a control output port. Five of its output bits are used to address a CD4555 dual 1-of-4 decoder, which in turn with one decoder selects which one of four analog inputs to the CD4066 multiplexer is to be routed to the RC4151 voltage-to-frequency converter. This V/F feeds an external flag input on the 1802 and in conjunction with a software routine provides analog-to-digital conversion of the signals presented to the CD4066. The second decoder in the 4555 is used to provide control signals for the frequency-correction circuitry on the system RF board. In addition, bits 3 and 4 of the 1852 output are used directly to control the digital oscillator clock source multiplexer; bits 5 and 6 direct the PDCP power-switching functions.

The microprocessor is equipped to generate its own crystal-controlled clock signal, but in the PDCP/UM setup it will normally be fed the 3.2MHz clock generated by μP_0, as selected by a jumper on the board. The master reset signal for the system is generated by an RC network in the $\overline{\text{CLEAR}}$ circuit of the 1802; this signal resets numerous system components to

known states when platform power is initially applied.

Also provided on the board are memory-select inputs which may be used to address the 6654s and 1822s when an external memory board is added to the μP_1 configuration. The normal decoding scheme for the add-on memory selects blocks of 1024 words (1K) each; when the EPROMs on the CPU board are allocated to block #0 and the RAMs to block #1, the hex memory addresses of the on-board memory are unchanged from the original implementation; this thereby simplifies new user-software design.

3.4 EXPANSION MEMORY BOARD

The basic philosophy of this setup is to allow the PDCP user to simply "stack" routines sequentially in PROM without special consideration for routine locations. By utilizing an additional memory board, considerably more complex data collection and analysis tasks can be performed by the PDCP and the usefulness of the platform vastly increased.

One example of this flexibility is in the basic memory configuration; any combination of RAM or EPROM, in 1Kx4 increments, can be utilized within the basic 4K add-on memory space. Recently, Intensil, Inc. and Harris Semiconductor introduced the IM6514, a 1Kx4 CMOS RAM which with a 5-volt supply has a typical access time of 170nS and a standby power requirement of only 1μW. The companion EPROM is the IM6653, also configured as 1Kx4. A CD4515 latch/4-to-16 decoder chip handles the address selection; the user may by means of jumpers specify which of the sixteen 1K memory blocks are to be occupied.

A further benefit of the add-on memory board is that of spare slots which may be employed for high-density CMOS mask-programmable ROMs such as the IM6316 (2Kx8) or the IM6364 (8Kx8) or for such special-purpose

devices as the CDP1855 hardware multiply/divide unit which is designed for use with the 1802 microprocessor. The implications of these ROMs for higher-level languages and of the 1855 for number-crunching tasks are considerable. The IM6364 could easily be programmed with a full-sized BASIC or a somewhat simplified PASCAL to enhance user programming speed and convenience; even the smaller IM6316 could be masked with an effective version of TINY BASIC which has already been written in well under 2000 bytes of memory. Furthermore, use of the 1855 would in great measure alleviate the major shortcoming of the 1802; i.e., its comparatively slow speed in complex arthmetic tasks.

A block diagram of an add-on memory board for the μP_1 system which includes the above features is shown in Figure 3.4.

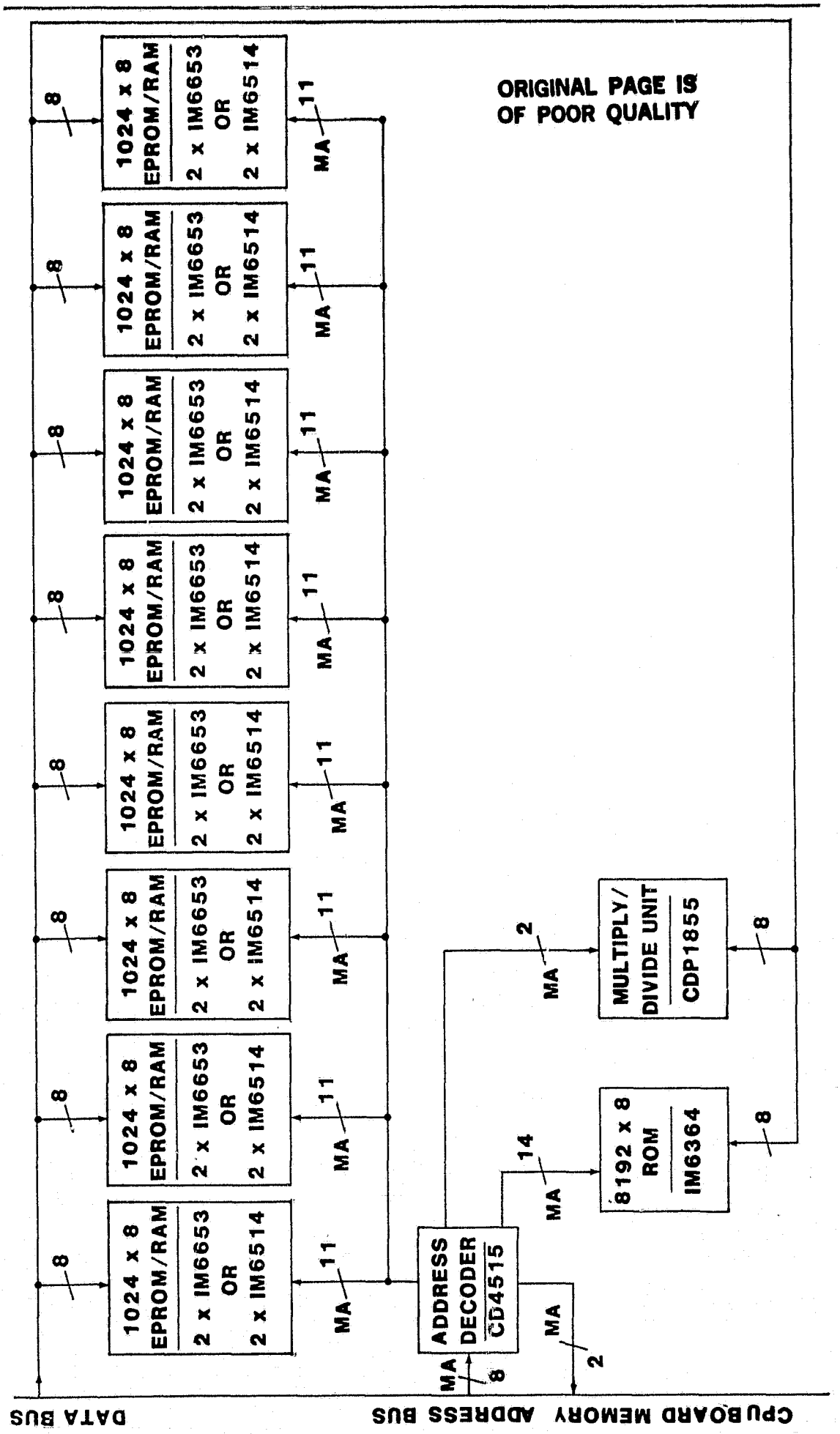

Figure 3.4. Typical Add-on Memory Board Block Diagram.

4. RF BOARD

4.1 INTRODUCTION

The RF board contains all the low-level radio frequency circuitry necessary for operation of the PDCP system. As shown in Figure 4.1. , one chain consists of the RF filter/frequency translator which handles the roughly 1MHz output of the digital oscillator board and converts it to the 10MHz range to drive the transmitter system. The signal from the digital oscillator is first applied to a 1MHz bandpass filter of fairly high selectivity, which rejects both low frequency noise and high-frequency spikes and clock glitches from the oscillator. In addition, the stairstepped output wave from the digital oscillator is smoothed by the filter and is rendered spectrally clean enough to be applied to the wideband hot-carrier diode balanced-mixer module. Here the 1MHz signal is mixed with the output of a crystal-controlled MOSFET oscillator stage operating at approximately 9.046MHz. The sum and difference frequencies from the balanced mixer are amplified by an RF buffer stage which simultaneously boosts the sum frequency (10.03MHz) to a power level of 1 to 10 milliwatts average and attenuates the spurious difference frequency (roughly 8.06MHz). The 50Ω output of this stage then feeds the transmitter board for final frequency multiplication and amplification to the desired 3-to 5-watt level in the 401-402MHz satellite band.

A second signal system is the RF oscillator setup with its associated frequency-correction circuitry. Each of the two oscillator stages consists of a VHF-type MOSFET transistor in a Pierce oscillator configuration. The frequency is determined principally by an AT-cut quartz crystal which is temperature-compensated (to a first order) by means of the surrounding

ORIGINAL PAGE IS
OF POOR QUALITY

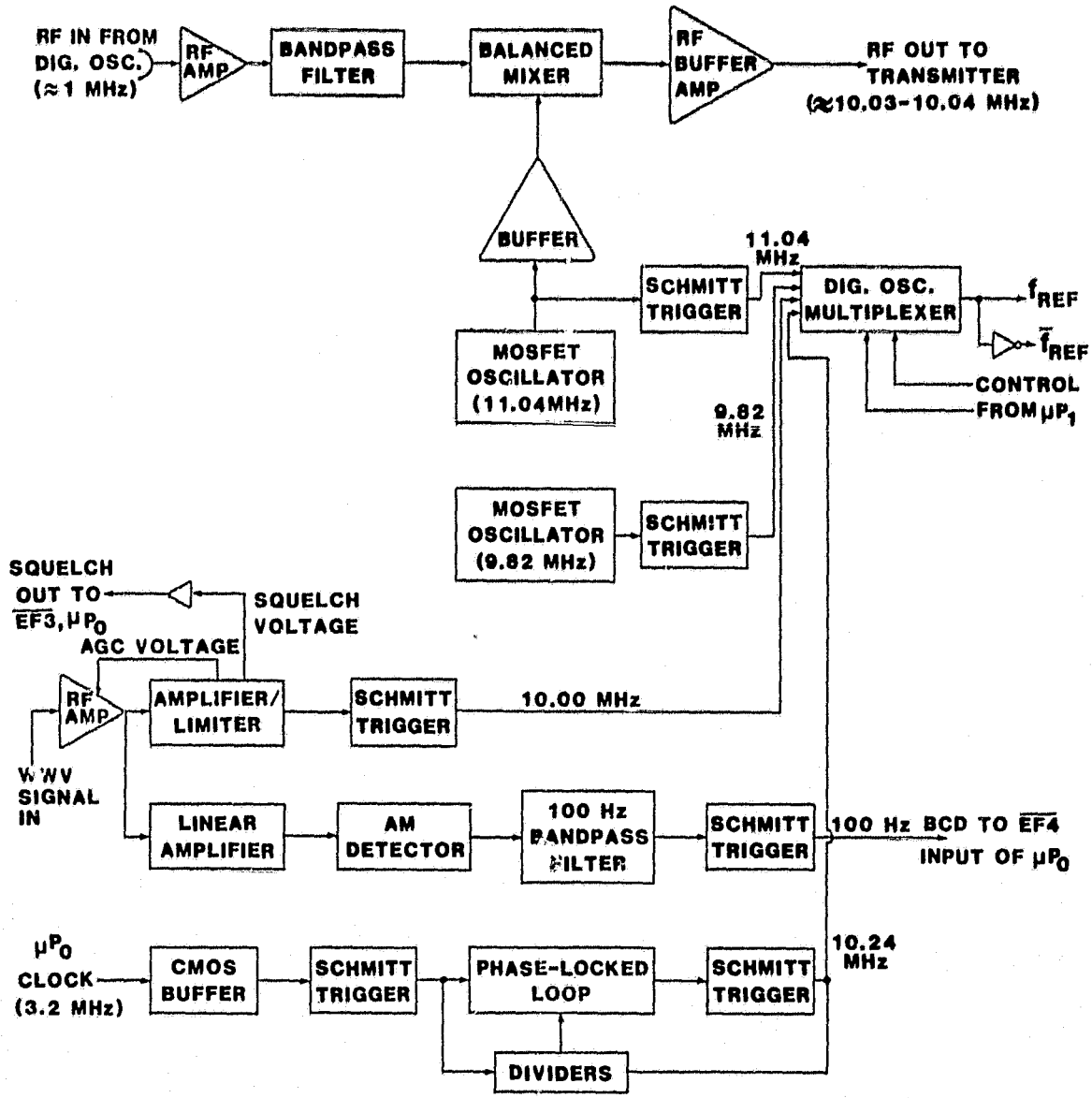

Figure 4.1. Block Diagram of RF Board.

capacitors. In addition, each oscillator is supplied with a highly linear 16-bit-equivalent CMOS D/A converter stage which feeds a d-c correction voltage to a varactor diode in the crystal oscillator circuit. By means of external hardware and a software routine, the main microprocessor (μP_1) generates numbers related to the oscillator frequency error relative to WWV at 10MHz and inputs these data words to the latches whose outputs feed the DACs. A low-speed independent AFC loop is thereby generated for each oscillator and allows greatly enhanced long-term frequency stability for the RF system.

The third signal system on the card is the WWV-based standards generation unit. This consists of a specialized high-sensitivity receiver for 10MHz WWV which has a front-end RF amplifier and two IF amps. The first IF amplifier chip is a high-gain amplifier/limiter system which recovers the WWV carrier frequency in a square-wave form; this signal is amplified and applied to a Schmitt trigger for translation to standard TTL logic levels. The second IF strip is a linear amplifier with a wide-range AGC and an AM detector. This IC detects the tones which are amplitude-modulated on the WWV carrier; the resultant audio output is fed to a high-Q bandpass filter centered at 100Hz which retrieves the BCD time-code information derived from the NBS master clock in Boulder, Colorado. This 100Hz sinusoid is squared up by another Schmitt trigger and is routed to a flag input on μP_0 for software-directed decoding of the time code.

The final signal system is the 10.24MHz generator. This unit consists of a CMOS buffer to provide an isolated 3.2MHz clock signal from μP_0, a Schmitt trigger for shaping, and a phase-locked frequency multiplier to generate the required frequency-and phase-locked 10.24MHz clock signal

needed by the digital oscillator when generating MSK modulation. A final low-power Schottky TTL multiplexer performs the digital oscillator clock selection function under control from μP_1.

4.2 RF FILTER/FREQUENCY TRANSLATOR-CHAIN

As mentioned above, the task of the RF Filter/Frequency-Translator Chain is to convert the RF output of the Digital Oscillator board to a frequency and power level suitable for driving a conventional DCP RF transmitter module. The transmitter in its standard form employs a high-quality temperature-compensated crystal oscillator module which has an output frequency of 10.03MHz. This signal is subsequently buffered and amplified by a chain of class-C RF stages which are configured as frequency multipliers. The total frequency multiplication factor for the transmitter in question is forty, which produces the desired 401.20MHz output for TWERLE service.

From the frequency calculation procedure discussed in Chapter 2, the MOSFET local oscillator mixing frequency, assuming the use of the sum-frequency output from the mixer stage, is 9.046167062MHz. This local oscillator signal is fed into one port of a double-balanced mixer at a level of roughly +7dBm referred to 50 ohms, or about 1.12 volts. The other port of the mixer is fed by a high-speed LM318 op-amp/emitter follower stage which performs multiple functions. The current output from the D/A converter on the digital oscillator board is converted to a voltage by the stage and the impedance level is reduced to 50 ohms to match the mixer input. In addition, the signal is filtered by a series-resonant LC network of moderately high Q which is tuned to 1MHz; this bandpass filtering serves to remove both low-frequency noise such as bit rate energy and dc offsets

and high-frequency components such as glitches, thermal noise, clock-rate signals and their associated intermodulation products, plus any harmonics of the desired RF output signal. It is necessary to remove the dc component from the desired output since any offset appearing at the input of the mixer can cause unbalances in the network which would result in increased production of even-order harmonics and other spurious signals. The LM318 device is a fairly low-power, high-slew-rate general-purpose op amp which has very good dc characteristics (e.g., low bias currents and offset voltage) and a gain-bandwidth product of 15-20MHz. Its guaranteed slew rate of better than 50V/μS enables it to easily handle the desired maximum output level of 1V peak at 1MHz. The actual slew rate required is given by Equation 4.2.1

$$S_r = 2\pi f_s V_p, \qquad \text{(Eqn. 4.2.1)}$$

where S_r is the slew rate, f_s is the frequency of the sinusoidal signal, and V_p is the peak amplitude (in volts) of the maximum desired output level. Substituting the above values in the equation yields:

$$S_r = (2)(3.1416)(1x10^6)(1.0)\frac{V}{S} = 6.28x10^6 V/S = 6.28V/\mu S,$$

which is almost an order of magnitude below the capabilities of the chip. The complementary emitter-follower stage boosts the output current available from the LM318 and serves to buffer the op-amp from the 50Ω mixer input impedance. The normal output signal is roughly 0.22V RMS.

The mixer itself is a hermetically-sealed unit which is fully shielded for RFI protection. It is internally double-balanced and employs a matched hot-carrier diode bridge and wideband coupling transformers to perform

the mixing function. The mixer is quite linear to better than +10dBm out with only 1dB of compression. The isolation from the local oscillator port to the output is over 50dB in this application; conversion loss is roughly 7dB. All spurious intermodulation products are on the order of 50dB below the 10.03-10.04MHz RF output.

The final stage in the RF amplifier/translator chain is the output buffer amplifier/filter. This wideband, direct-coupled microwave-type unit is a hybrid integrated-circuit power amplifier capable of greater than 100mW output into a 50-ohm load. The unit, packaged in a standard TO-3 case for ease of heat-sinking, is internally protected against overloads and high VSWR conditions. Its overall power gain is at least 19dB; to produce the desired maximum output power level of +20dB the mixer output is roughly +1dBm, or about 0.25V across 50ohms. The difference-frequency output of the mixer at 8.05-8.06MHz is attenuated at the power amp input by a fairly high-Q LC notch filter in order to ensure adequate out-of-band signal rejection to eliminate possible interference by the PDCP to other VHF systems when transmitting data to the satellite.

4.3 RF OSCILLATORS

The two crystal oscillators used to generate the necessary reference frequencies for operation of the RF board are both MOSFET units designed for high frequency stability versus time, temperature, and supply-voltage variations. The units also have a very low power requirement and are relatively inexpensive. To meet these needs, each oscillator utilizes two VHF-type 40468A MOSFET devices in a two-stage setup. The first transistor serves as the oscillator. A parallel resonant AT-cut crystal is used as the frequency-controlling element, and is stable to better than ±5 parts

per million in frequency over a temperature range of -30°C to +85°C. The oscillator feedback and padding capacitors are all high-stability silver-mica types, except for one air-variable trimmer used to initially adjust the frequency to exactly the desired value. A 470μH RF choke isolates the oscillator RF from the B+ line; a 0.01μF ceramic capacitor bypasses any residual RF from the supply lead. For maximum bias stability a 2.7KΩ source resistor supplies local negative dc feedback to the stage; the parallel bypass capacitor allows the stage gain to increase at RF frequencies in order to maintain stable oscillations with temperature, time, and component variations. The square-law characteristic of the MOSFET devices minimizes the production of harmonic frequencies in the oscillator output as compared with a bipolar transistor; in addition, the MOSFET transconductance increases with decreasing temperature, thus enabling the circuit to function properly at very low temperatures (e.g., -50°C).

The oscillator stage is buffered by the second MOSFET stage which is configured as a source follower. This arrangement provides excellent isolation of the oscillator from load impedance variations and simultaneously provides adequate drive capability for the following stages. The extremely high and constant load impedance presented to the oscillator proper allows very good inherent oscillating-frequency stability under normal operating conditions.

Unfortunately, the exacting demands of the satellite data collection service required even better stability with temperature, supply-voltage variations, and time than could be achieved at reasonable economic cost with conventional circuitry. It was therefore necessary to develop a more sophisticated approach which could hold the PDCP oscillators to a

short-and long-term stability on the order of one part in 10^7.

Since only oven-type TCXO systems are capable of this level of stability, a brief investigation was made into this type of frequency control. Unfortunately, no currently-available commercial units with the desired order of accuracy could be found which did not require prohibitively large amounts of oven heater power. One possible solution to this problem would be an integrated-circuit oscillator using hybrid and/or monolithic technology which would enclose a monolithic crystal, appropriate active devices, temperature-compensating circuitry, and an integrated chip heater system in a single thermally-insulated package. (This concept is discussed in detail in Chapter 7.) A comprehensive scheme such as this would virtually eliminate the short-term drift effects of temperature, supply voltage, and oscillator loading but would still fall short in fully compensating for long-term errors such as crystal aging, although "clean" IC processing could make a substantial improvement in this regard.

The approach chosen for use in the PDCP/UM system is a very general technique which could be applied to greatly enhance the frequency stability of virtually any type of oscillator, but its use here is especially desirable in the context of the satellite data-collection platform application with its attendant long-term oscillator stability requirements. Basically, the microprocessor and associated hardware comprise the comparison and filtering blocks of multiple sampled-data, discrete-time automatic frequency control loops which enclose the three crystal oscillators within the PDCP system. All three loops are referenced to the recovered 10.00MHz carrier frequency from WWV which is processed in the WWV receiving system, divided down by the digital oscillator, and applied to the microprocessor

μP_1. The 16-bit number read from the digital oscillator buffer register is converted in a software routine to another 16-bit quantity which is fed to one of three CMOS multiplying D/A converters with integral data latches. The latched data in each D/A specifies the magnitude of a dc current injected into the summing junction of an offset-nulled low-power op-amp, which serves as a current-to-voltage converter. The output voltage controls the bias on a high-frequency, high-Q varactor diode which is placed in the crystal-padding network of the associated MOSFET oscillator stage and thereby shifts the crystal frequency as needed to maintain the desired accuracy.

To implement this function with a usefully large range and adequate frequency resolution, two eight-bit buffered converters are used to form a 16-bit resolution unit. Since ultimate linearity is not required, the two 8-bit units may be combined in a weighting ratio of 256:1 to produce the desired 16-bit resolution; the higher-order unit is linear to better than $\pm 1/8$ LSB while the lower-order converter has a relaxed $\pm 1/2$ LSB specification. This implementation is satisfactory since the remaining system components are in general nonlinear and to a small degree undefined with respect to their exact responses to a given AFC voltage. Due to component tolerances, thermal drift, crystal aging, and other factors, the calculated AFC voltage level may not give precisely the desired correction; therefore μP_1, under control of the software algorithm, repeats the measurement/correction cycle until the desired accuracy is achieved. Figure 4.3. shows a functional hardware diagram of the μP-based AFC system.

The function of the AFC loop is a sequence of steps. First, the pro-

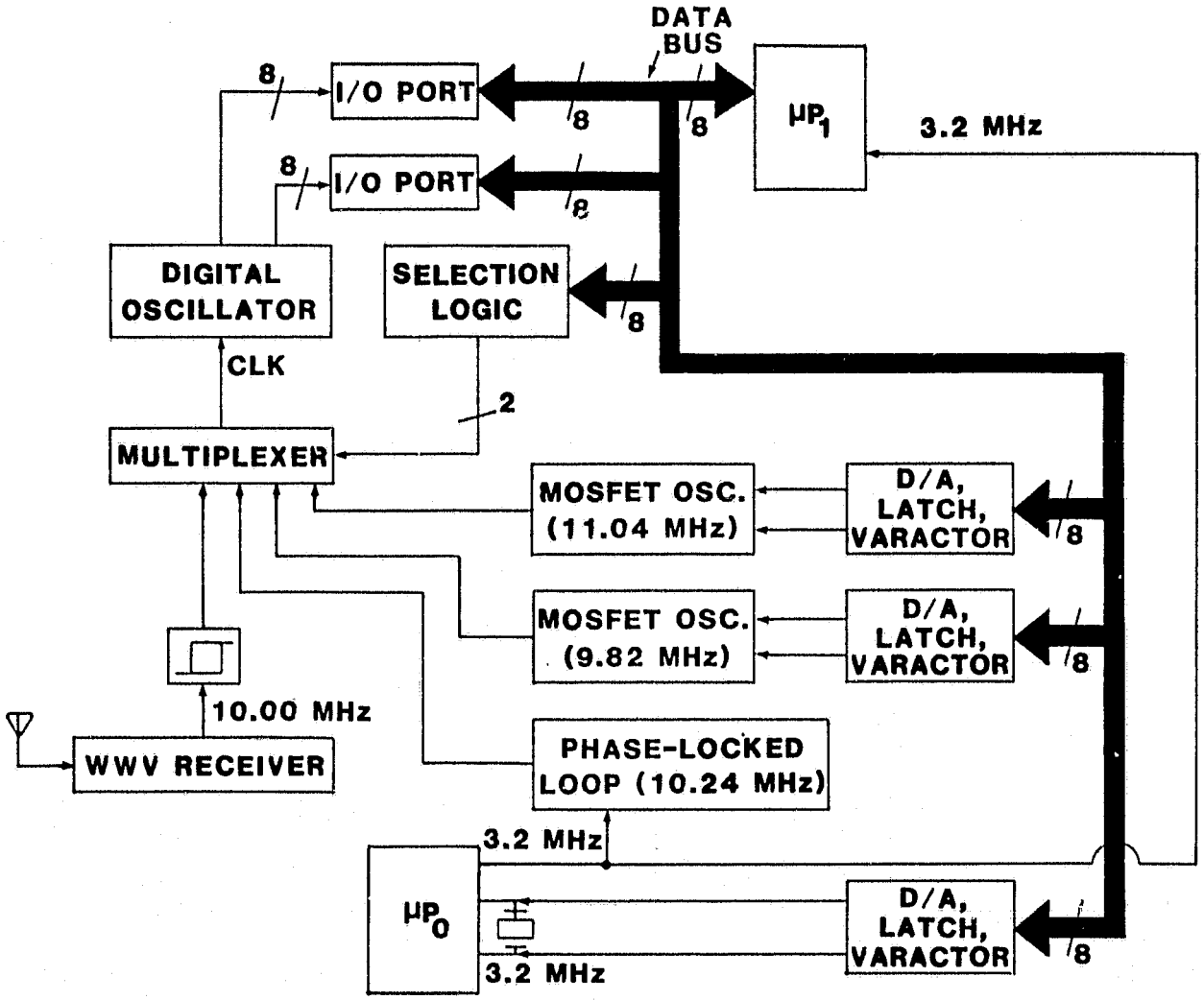

Figure 4.3. Microprocessor-Based Oscillator AFC System.

gram causes μP_1 to input a specified "Frequency Index" to the digital oscillator data input and through the "Selection Logic" block to gate the 10.00MHz carrier frequency from the WWV receiver to the digital oscillator clock input. The 10.00MHz signal is allowed to clock the digital oscillator for exactly one second, or 200,000 instruction cycles. At the end of that time the number stored in the digital oscillator accumulator is loaded onto the μP_1 data bus and is subsequently compared to the contents of the digital oscillator register immediately prior to the one-second interval. If the difference between the numbers is equal to zero, then the 3.2MHz clock driving both μP_0 and μP_1 is accurate within one part in 10^7 (one count in 10 million). If the number differs by $\pm n$, then the microprocessors clock is within $\pm(n+1)$ parts in 10^7 of 3.2MHz and the μP will load a new correction number into the D/A converter associated with the 3.2MHz clock. The procedure will be repeated until n decreases to zero and remains at zero for three successive cycles.

The second step is to calibrate the 9.82MHz digital oscillator clock frequency. Now that the 3.2MHz clock has been corrected (if necessary) it remains only to input a new Frequency Index and allow the digital oscillator to count up for one second, as before. The resulting 16-bit number is analyzed by the software program and a 16-bit frequency-correction number generated; this number is written into the D/A latches associated with the 9.82MHz MOSFET oscillator. This oscillator is then allowed to clock the digital oscillator again for one second, and the correction number is calculated from the result; the cycle, as in the first step, repeats until the oscillator is fully corrected. In like manner, the 9.046MHz local oscillator is corrected to within 0.1 part per million. The AFC procedure is then complete and the PDCP is now prepared to

transmit. The 10,24MHz phase-locked oscillator is not corrected separately, since it is referenced to the 3,2MHz microprocessor system clock. The WWV correction software is discussed in greater detail in Section 6.3.3.

4.4 WWV RECEIVING SYSTEM

The function of the WWV Receiving System block is to amplify, condition, and detect the signal from the National Bureau of Standards standard frequency and time station at 10.00MHz for use by the PDCP reference circuitry. The first stage of the receiver is an MC1590G RF amplifier chip which is transformer-coupled to the antenna input. This unit, which has tuned input and output circuits, provides a maximum voltage gain of 42dB and has an AGC range with low distortion of better than 60dB. The amplifier drives an RF transformer tuned to 10.00MHz, whose secondary windings feed two intermediate-frequency amplifier chips.

The two IF chips are for two different functions: the first, a CA3089, processes the WWV carrier while the second, an LM373, amplifies the AM envelope and detects the WWV audio modulation. The CA3089 is a unit designed for 10.7MHz IF applications in standard FM broadcast tuners and receivers. It consists of a series of amplifier/limiter stages which has a typical sensitivity of 12μV for 3dB limiting and includes facilities for muting control and delayed AGC for the RF amplifier. The output level is roughly 300mV peak-to-peak at 10MHz; a following discrete transistor amplifier stage increases the swing to 5 volts peak-to-peak and provides sufficient drive to feed one section of a 74LS14 hex Schmitt trigger chip. From the 74LS14 the 10,00MHz signal is routed to the digital oscillator clock multiplexer. The WWV signal strength may be as low as 5μV and still be properly processed by the receiving chain. If the signal drops below

that level, the RF tuning meter output on the CA3089 drops to less than 2.5 volts and thus switches a CMOS buffer on the RF board to the low state, thus signalling μP_0 via flag input $\overline{EF4}$ and causing a software action to inhibit further frequency and time acquisition from WWV until the signal level is restored.

The second IF processing system, the LM373 and its associated circuitry, performs the task of amplification and linear synchronous detection of the audio information which amplitude-modulates the WWV RF carrier. The LM373 is a general-purpose device intended for AM/FM/SSB applications in the HF range. It contains two high-gain linear amplifier stages (32dB and 37dB, respectively) which boast an overall sensitivity of 15μV RMS for 10dB S+N/N ratio at 10MHz. The AM signal-to-noise ratio is 38dB for a 30mV input. The detector produces between 50mV and 100mV RMS audio output for chip RF input levels from 50μV to 100mV. Interstage filtering is accomplished by high-Q LC networks to enhance selectivity and noise rejection. The audio output of the device feeds a two-stage active bandpass filter comprised of two amplifiers within an LM358 chip and the associated feedback components. The filter has a gain of roughly 15, a Q of approximately 25, and a center frequency of 100Hz. The sinusoidal filter output signal is squared up in a Schmitt trigger and is sent to the $\overline{EF3}$ flag input on μP_0 for software - controlled decoding of the 100Hz-rate serial BCD time code data; this information is utilized to maintain the PDCP system time to within ±15mS of the WWV standard.

4.5 PHASE-LOCKED OSCILLATOR SYSTEM

The final system on the RF board is the 10.24MHz phase-locked oscillator setup which is used to clock the digital oscillator during MSK transmissions.

To ensure proper glitch-free operation of the digital oscillator system in the generation of MSK modulation, the digital oscillator clock must be synchronous with the bit-rate clock; i.e., a bit must not change during or near a positive clock transition to avoid bit errors and spurious frequency outputs. To effect this condition, the 10.24MHz source must be phase-locked to the 3.2MHz microprocessor system clock. A block diagram of the system is shown in Figure 4.5.

The reference for the phase-locked oscillator is derived from the crystal-controlled, WWV-corrected μP_0 clock output. To avoid loading the 1802, the 3.2MHz clock output is fed to a CD4050 noninventing CMOS buffer which provides the desired isolation and in addition shapes the nearly-sinusoidal clock waveform into a square wave. This is suitable for driving a 74LS90 biquinary/decade counter configured to divide the 3.2MHz input by five. The resulting 0.64MHz output is fed to the signal input port of an MC1496 balanced-modulator IC which serves as a phase comparator. The other input port of the MC1496 receives the output signal from a 74LS93 4-bit binary counter which divides the phase-locked oscillator frequency by sixteen, thus producing an output frequency of 0.64MHz, same as from the μP_0 clock divider. The phase comparator output is low-pass filtered and the resultant dc component is applied to a varactor-diode network which is in the LC tank network of a MOSFET oscillator similar to the crystal-controlled oscillators discussed previously. The buffered output of the MOSFET VCO is squared up in a Schmitt-trigger inverter; the output 10.24MHz square wave is sent to the digital oscillator clock input multiplexer and to the input of the divide-by-sixteen counter, which closes the frequency/phase control loop. Thus the 10.24MHz signal is locked to

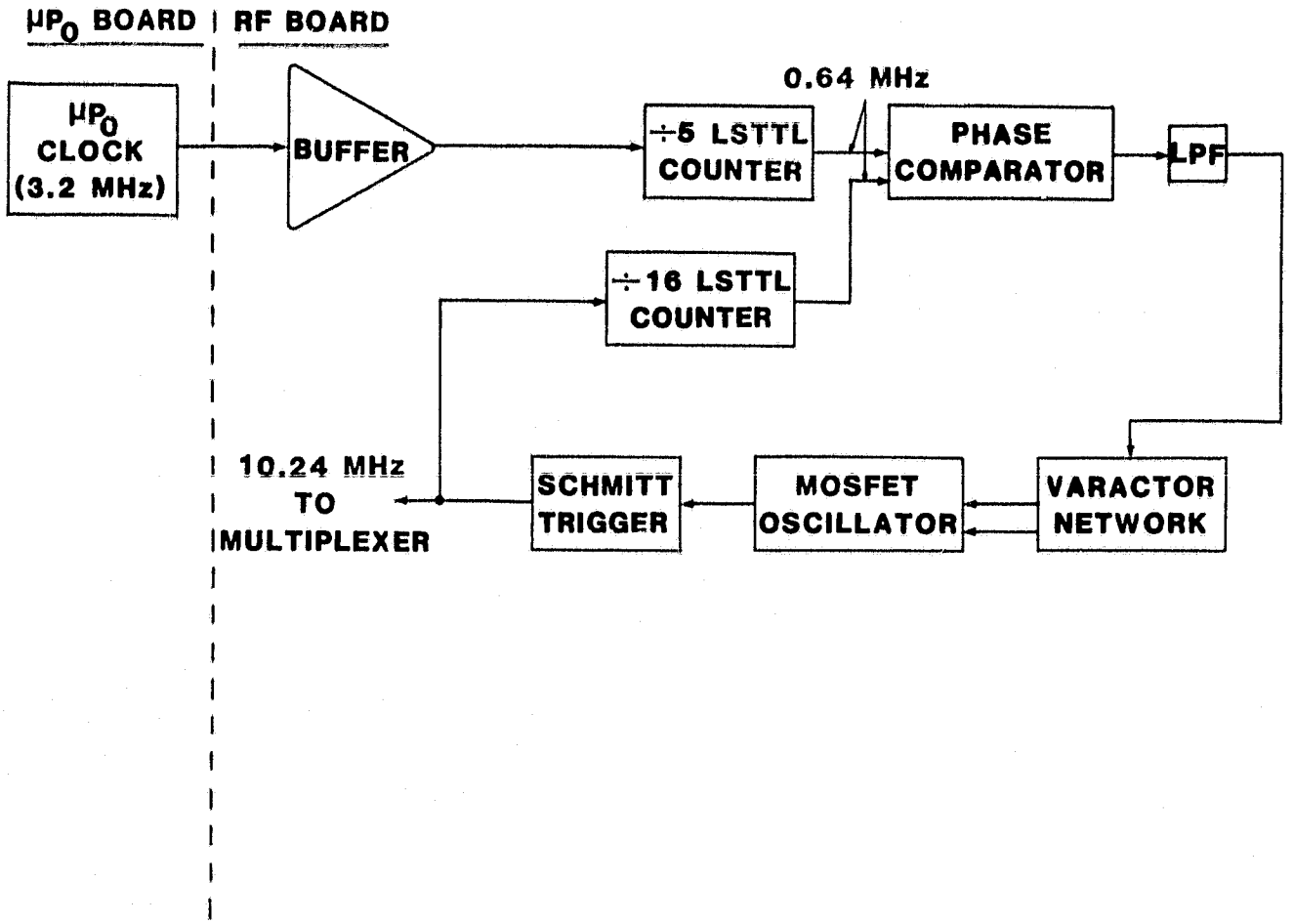

Figure 4.5. Block Diagram of Phase-Locked Oscillator System.

the 3.2MHz clock for use in the generation of MSK; the frequency multiplication ratio is $\frac{16}{5}$, or 3.2.

To avoid excessive standby power consumption in the PDCP system, all systems on the RF board are normally powered down by the executive program in the μP_1 microprocessor. The RF oscillators are generally turned on several seconds before the AFC routine begins, in order to minimize drift, but the other systems are activated only as they are actually needed. Power management considerations for the PDCP unit are discussed more completely in Chapter 6.

5. POWER SUPPLY/INTERFACE BOARD

5.1 GENERAL

The function of the Power Supply/Interface board is to provide the PDCP system with all necessary power supply voltages, to accomplish the desired power management switching tasks, and to provide the appropriate user front-panel, external, and transmitter interface facilities. The system is designed for maximum power efficiency and for a high degree of flexibility in coupling to special and conventional DCP RF transmitter units. Integrated circuit techniques are fully utilized in order to reduce complexity, size, and costs while maintaining high reliability and electrical performance characteristics.

5.2 POWER SUPPLIES

The PDCP/UM system concept requires that a wide variety of analog and digital signal processing devices be powered from a single 12-volt nominal rechargeable battery system with an absolute minimum conversion loss. In addition, the on-off control for various systems within the PDCP must be implemented under control of microprocessor μP_1 to keep overall system power consumption as low as possible; any system not in active use is powered down in accordance with the power management software. The supply voltages required are +5 and +10 volts for the microcomputer systems (μP_0, μP_1, and their associated memory chips); +5 volts for the digital oscillator board; $\pm$15 volts, +12 volts, and +5 volts for the RF board, and +12 volts for the RF transmitter module. All the voltage-conversion tasks except the generation of +10 volts are handled by switching voltage regulators which have typical power efficiencies of

better than 80%, good regulating properties, moderately low noise, and short-circuit protection. Figure 5.2 shows the block diagram of the power supply/power switching setup.

5.2.1. Digital Oscillator Power Supply

The +5V supply for the Digital Oscillator board is derived from the battery voltage by means of a Fairchild 78S40 high-efficiency IC-type switching regulator system. The input power to the regulator is filtered by an L-C pi network to isolate the switching spikes from the remainder of the power supply system; this noise decoupling is essential to ensure minimal degradation of RF receiver performance as well as to maintain negligibly low digital system data bit errors. The supply for the Digital Oscillator system is switched on and off via a saturating bipolar transistor in series with the regulator +12 volt input; control is effected by a buffered, level-shifted data bit signal from a μP_1 output port.

The digital oscillator requires roughly 600mA at +5V; this is supplied at roughly 80% overall efficiency from the single 78S40 chip. The approximate switching "on" time of the regulator is 56μS; the "off" time is about 60μS. The overall switching frequency is typically 8.5kHz, which allows low switching losses in the regulator circuitry. The audibility of the supply is probably not a significant disadvantage since the PDCP unit is almost always unattended in operation. The +5 volt output of the regulator is applied to another L-C pi-type filter to attenuate switching spikes, noise, and ripple on the supply line before it goes to the Digital Oscillator proper. The power drain from the battery for this regulator is roughly 375mW when energized, but the average is much lower since the software power-management routines limit the on-time of this system to only the

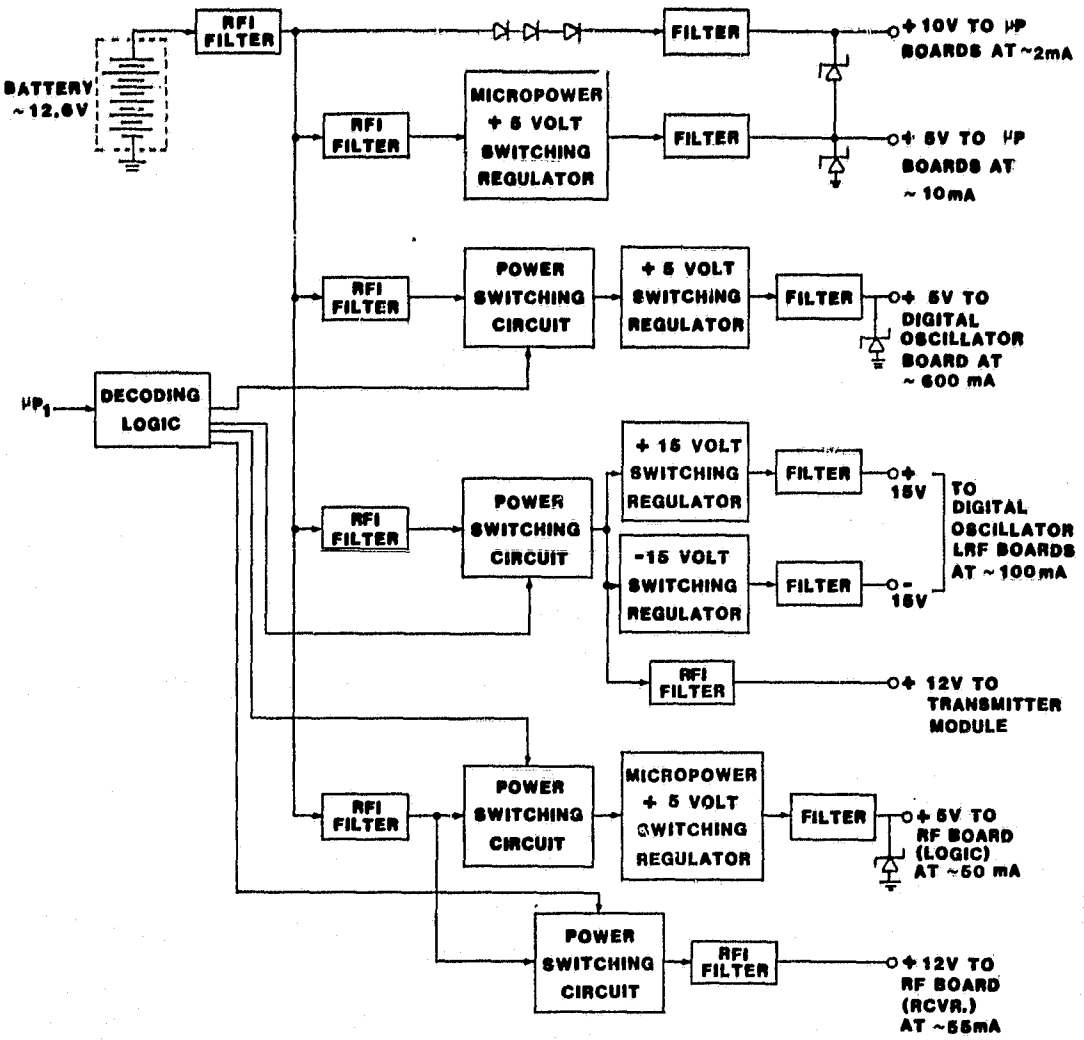

Figure 5.2. Block Diagram of Power Supply System.

C-2

intervals required for the frequency-correcting and actual transmitting functions of the PDCP system.

5.2.2 Dual-Polarity 15-Volt Power Supply and Power Switch

The ±15 volt supply needed to operate the high-speed D/A converter on the Digital Oscillator board and the following buffer amplifier on the RF board is obtained from two 78S40 chips, along with a few external components. In the negative supply, a single MPS-U52 PNP power transistor performs the actual switching function; base drive for the device is obtained from the 78S40. An external high-speed catch diode conducts the negative current pulses from the 470μH inductor and produces the -15 volt output across the 500μF electrolytic capacitor. This output voltage is converted to a current via a 150KΩ resistor and is inverted by the internal op-amp on the 78S40 chip. The op-amp output is compared by the chip with the 1.3V reference to control the switching "on" time of the system.

The positive supply is slightly simpler; the only external components needed are the current-limiting resistor, the timing capacitor, and the inductor. The 0.022μF timing capacitor produces an "off" time of 60μS, and the required "on" time is on the order of 20μS. The overall switching rate is 12.5kHz. To provide complementary tracking ±15V supplies, the divided-down output of the regulator is compared with the 1.3V reference on the negative regulator chip; this setup references both supplies to the same voltage, thus ensuring tracking of the output voltages with time, load, and temperature. For this supply the internal 78S40 catch diode is used, but the op-amp is not needed since the output voltage is the same polarity as the +1.3V reference; efficiency at an output current of 100mA is about 81%.

Both ±15V supply busses are filtered by hash-choke/capacitor networks to reduce the switching noise and are subsequently routed to the Digital Oscillator and RF boards; the typical currents are 90mA from the +15V line and 30mA from the - 15V side. The composite efficiency is about 85% for both supplies; output ripple on each line is less than 20 millivolts peak-to-peak.

The power control switch is comprised of another μP_1 - controlled NPN power transistor which is in series with the battery supply bus. The device controls not only the input power to the ±15V regulators but also directly gates the +12V power to the RF transmitter module through still another RFI filter network. The use of this configuration allows a single data bit from μP_1 to control not only the transmitter unit itself but also the preceding driver stages (including the D/A converter) which are needed only during actual RF transmission intervals. A special feature of this switching unit is an RC network in the base circuit of the power-switching transistor which provides soft turn-on and turn-off functions to minimize high-current transients in these higher-power circuits.

5.2.3. Microprocessor Power Supplies

The 1802 microprocessors and their associated memory, decoding, and I/O circuitry require very little operating power due to their CMOS fabrication but since these systems are always operational, their total power consumption must be carefully considered in developing an effective power management scheme for the overall PDCP system. In order to hold power consumption to an absolute minimum consistent with reliable system operation over supply voltage and temperature variations, a novel micro-power-dissipation switching regulator system is utilized to generate the

required +5 volts for the microcomputer systems.

The typical current drain for an 1802 microprocessor with a 3.2MHz clock is in the range of 18 to 25 milliwatts, depending on the temperature, instruction, and the individual chip. In the "idle" state the 1802 dissipates roughly one-half as much power as in normal operation; this fact is utilized in the PDCP operating program by terminating each μP_1 routine in software with the "IDL" instruction, thus forcing the microprocessor to idle until the next command interrupt occurs. Nevertheless, it was still desirable to reduce the regulator dissipation as much as possible consistent with high reliability and low parts count.

The circuit employed includes two IC chips, a low-power NPN switching transistor, an inductor, and a few resistors plus a timing capacitor. The setup consists of an Intersil ICL8211 micropower voltage detector plus a standard CD4093 CMOS quad 2-input Schmitt-trigger NAND gate. The ICL8211 consists of a highly stable voltage reference, a comparator, and a pair of output buffer/drivers. In operation, a divided-down voltage derived from the +5 volt output of the regulator system is compared with the ICL8211's 1.15 volt internal reference source. The comparator output is buffered and subsequently becomes one input to a NAND gate (on the CD4093 chip) which controls the "on" time of an astable multivibrator formed by a second Schmitt-type NAND gate and its accompanying RC timing network. The outputs of both NAND gates drive inputs of the two other NAND gates on the chip, which form a negative-trigger R-S flip-flop. One output of this flip-flop drives the base of a 2N2222A transistor, which switches current on and off through the inductor. The output voltage is filtered by a 10μF tantalum electrolytic capacitor; a parallel 0.1μF mylar unit provides bypassing for

high-frequency noise components. Figure 5.2.3 is a block diagram of the micropower regulator system.

The average maximum load current is typically 10mA in normal operation, though the regulator can easily handle 50mA. The efficiency at the more probable level of 10mA is better than 95%; the two chips typically draw a total of only 27μA from the +12-volt supply. Total regulator dissipation is roughly 1 to 2 milliwatts and is principally dependent on the switching characteristics of the 2N2222A transistor. The output of the regulator is shunted to ground by a 5.6V avalanche diode; this provides overvoltage protection with very low standby power dissipation.

The +10V supply for the V_{DD} inputs of the 1802s is derived from the battery voltage by a series string of three silicon diodes; this provides the desired output voltage with roughly 79% efficiency, which is adequate in light of the low current requirements for this supply. An additional advantage of this method of generating the +10 volts is that the power supply sequencing requirement for the 1802s ($V_{DD} \geq V_{CC}$ at all times) is automatically met during turn-on or battery connection; for the case of power-down or disconnection, a Schottky diode connected between the +5V and +10V lines serves to protect the microprocessors from any reverse-voltage transients.

5.2.4. RF Board Power Supplies

The power for the RF board is derived from the battery with the same types of hardware as previously discussed. The receiver circuits, which require +12 volts at roughly 55mA for normal operation, are fed through a power switching circuit and two RFI filters to provide on-off control and noise decoupling. To supply the MOSFET crystal oscillators and buffers

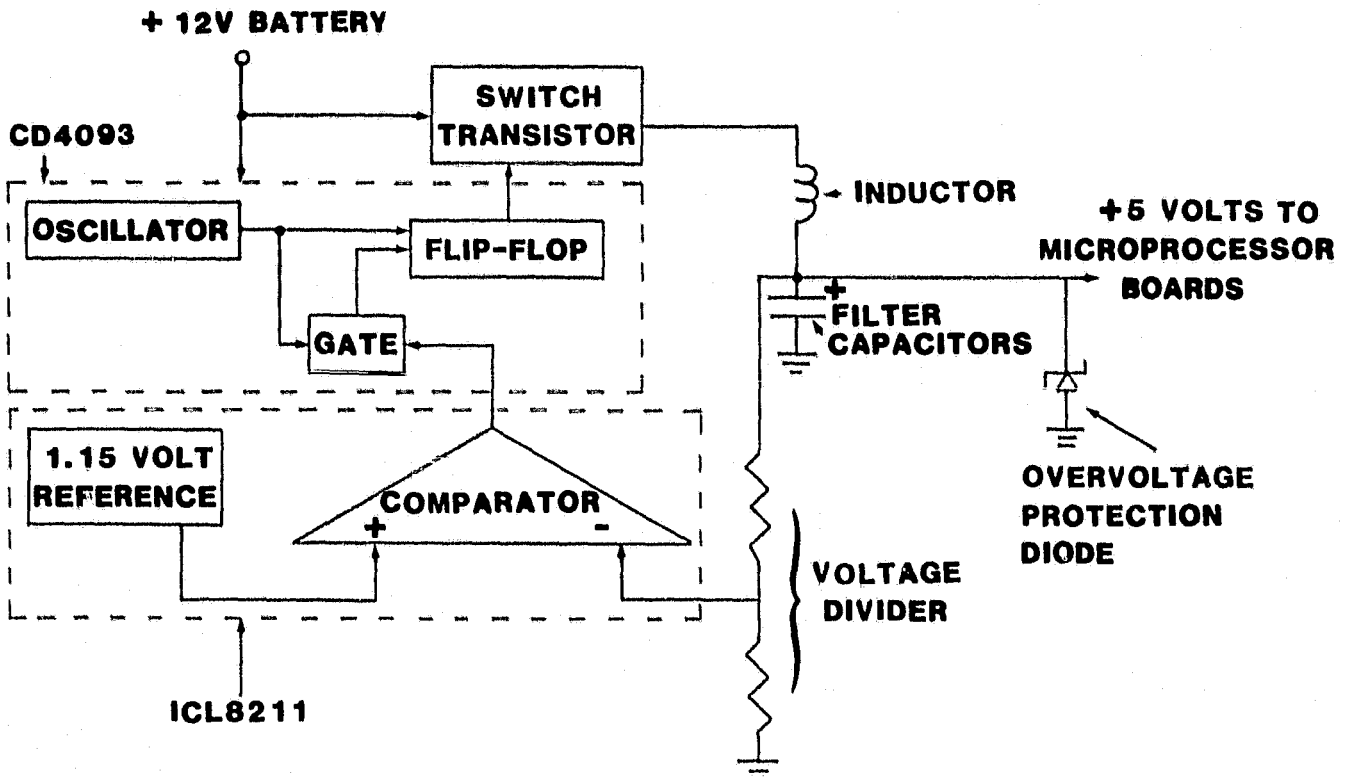

Figure 5.2.3. Block Diagram of Micropower + 5 Volt Switching Regulator.

and the LSTTL logic with +5 volts at about 50mA, another power switch and micropower switching regulator system are employed to provide on/off control and to keep the supply efficiency as high as possible (about 90%). Following the regulator is another pi-network filter to remove switching noise and another 5.6V avalanche diode for overvoltage transient protection. This +5 volt bus is RFI filtered once again on the RF board to ensure a noise-free supply for the oscillator stages. Switching control signals for these supply lines are also generated from control bits derived from the μP_1 output port and optically coupled into the power supply system.

5.3 INTERFACE CIRCUITS

There are two data interface systems on the Power Supply/Interface board. These provide output data from the μP_1 system to an external DCP transmitter module and/or a standard telephone line. The transmitter interface provides switched +12 volt signals used by RF transmitter modules manufactured by Handar and others which have three PSK control inputs, designated 0°, +60°, and -60°. The input to this setup is a +5-volt logic signal from the Q output of μP_1; the output is a set of three decoded +12 volt outputs which represent "clear carrier","data=0", and "data=1" states. The telephone-line interface system takes the Q data bit stream and converts it to midband audio tones suitable for sending on standard dedicated or switched telephone transmission circuits.

5.3.1 Standard DCP Transmitter Interface

The data required to be transmitted is obtained directly from the "Q" output of μP_1. This signal is buffered by a noninverting CMOS gate, then level-shifted by a combination of an open-drain buffer in a 74C906 chip which drives a 2N3906 PNP transistor. The collector of the 2N3906

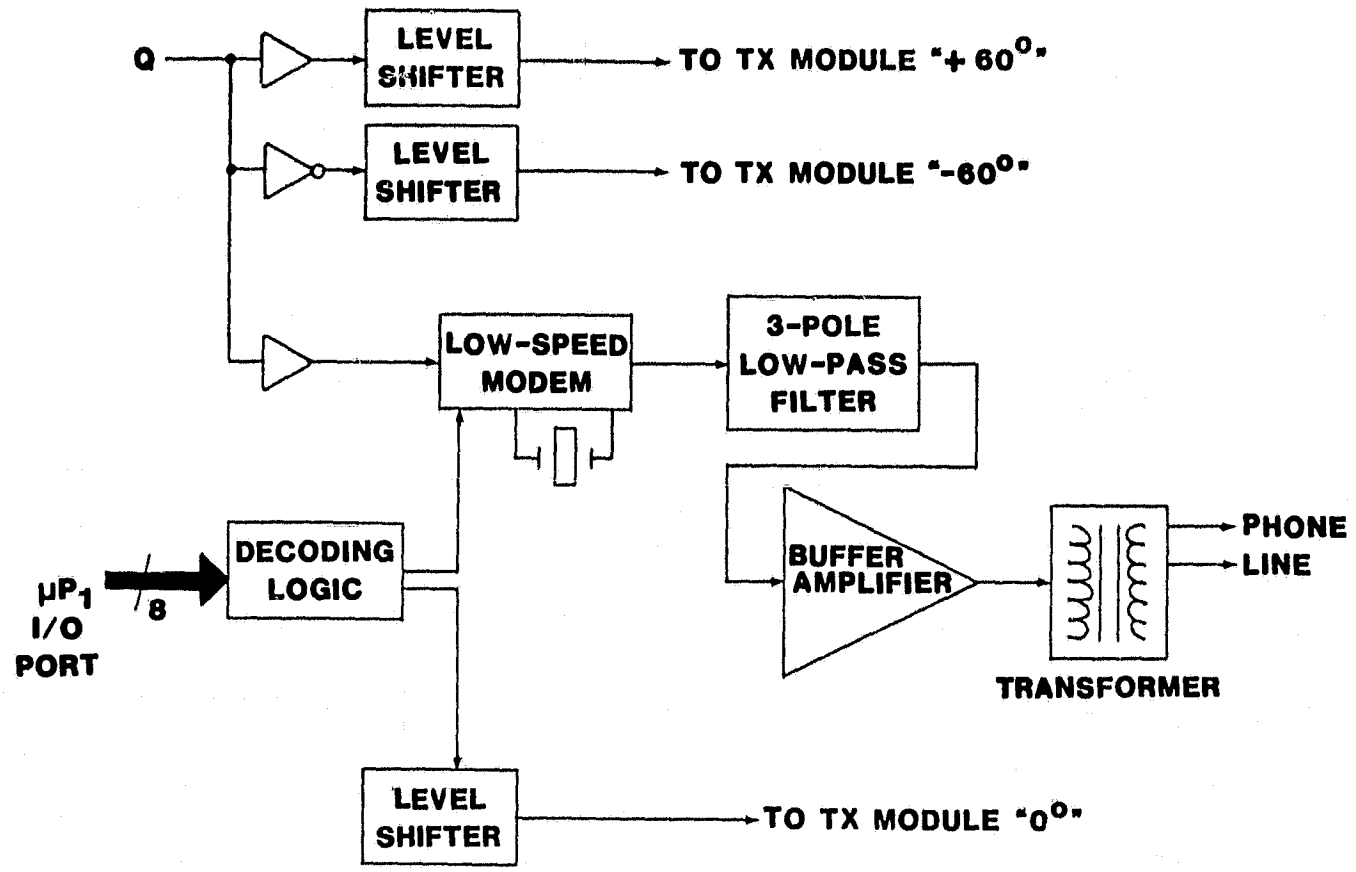

Figure 5.3. Block Diagram of Interface Circuitry.

is grounded through a 10KΩ pull-down resistor and is the drive point for the RF transmitter "+60°" control input. An identical setup, except with an inverting gate at the input, drives the transmitter's "-60°" input. The "0°" pin, representing clear-carrier operation (no PSK modulation), is driven by still another buffer/transistor circuit controlled by an output bit from an 1852 I/O port device. This unit receives eight input bits from μP_1 and generates control signals for the Power Supply/Interface card as listed in Table 5.3.1. Bits 1 and 2, which control substantially higher-power circuits, use external NPN transistors to drive the power switching devices. The software in the μP_1 system directs the power supply and interface switching by outputting the appropriate control word into the 1852 output port #7, which is designated the "Command Out" port.

BIT NO.	FUNCTION
0	RF Board +12V on/off
1	Digital Oscillator on/off
2	Transmitter Power on/off
3	"Clear-Carrier" on/off
4	Telephone Interface on/off
5	Echo Send on/off
6	RF Board +5V on/off
7	I/O System Power on/off

Table 5.3.1. Power Supply/Interface Control Function Decoding

5.3.2. Telephone Audio Interface

The final system on this card is the telephone interface unit. This setup consists of an MC14412 low-speed modem CMOS/LSI chip, a dual low-power operational amplifier, and a line-matching audio transformer. As shown in Figure 5.3, the "Q" output of μP_1 is buffered by a noninverting section of a CD4041 true/complement buffer chip and then applied to the "Transmit Data" input of the 4412. The modem generates (according to the frequency-select inputs) the U.S. standard data originating-mode frequencies of 1270Hz (data=1) and 1070 (data=0). These output tones are digitally synthesized from a 1.0MHz crystal-controlled clock within the 4412 system and are thus extremely frequency-stable and accurate. The stepwise-sinusoidal transmit-carrier output waveform is low-pass filtered by a third-order Butterworth network incorporating one unit of the dual op-amp. The other unit serves to amplify the smoothed output of the filter up to a level suitable to drive the line-matching transformer. The typical audio output level into a 600Ω balanced line is 0dBm, roughly 775mV RMS. The MC14412 is limited to data rates of 600 bits per second and is configured to transmit only. For more complex ground communication schemes, especially those involving two-way data transfer and/or remote control or programming of the PDCP unit, a modem/UART package could be implemented on a separate card which would plug into one of the spare slots on the PDCP/UM motherboard.

One bit from the CDP1852 is used to control the +5 volt power to the telephone interface system, in order to keep the system on only when necessary and thereby conserve power.

6. SYSTEM SOFTWARE

6.1 SYSTEM PERSPECTIVE

A major feature of the system configuration is its intrinsic software compatibility with the UT Model PDCP implementation previously described in Contract NAS5-22495 [1]. The current hardware allows the program package of arithmetic, data-handling, and data-formatting routines to be executed with only minor modifications to accomodate the enhanced I/O capabilities of the present setup. The overall software design of the combined PDCP/UM system provides for program "modules" to be stored in memory and randomly addressed as specified by the real-time clock/control program executed by control microprocessor μP_0. This modularity of the transmission software package permits the end user to select only the routines he needs from the PDCP library and thereby minimizes programming effort as well as PDCP memory storage requirements.

The partitioning of PDCP software tasks between μP_0 and μP_1 permits virtually all of the software previously developed by UT to be efficiently executed by the enhanced PDCP dual-microprocessor implementation. Basically, the task of timing and sequencing all PDCP events is handled exclusively by μP_0, whereas the actual job of acquiring, processing, formatting, and transmitting data is reserved for μP_1. As previously stated, the μP_0 system via the SR-bit on the 1852 output port is configured to initiate an interrupt within the μP_1 system. The interrupt service routine stored in μP_1 memory then directs an indirect jump to the new subroutine address via a table-lookup containing the new two-byte starting address of the desired routine. Although a bit more complex than a straightforward two-byte address exchange between μPs, this scheme (similar to the ATCAR

technique described in the Final Report for Contract NAS5-22495) allows for enhanced PDCP software modularity by reducing the software interaction between μP_0 and μP_1. If changes in the data processing, formatting, or transmitting routines are required, then the EPROMs associated with μP_0 need not be changed unless the transmitting intervals are also to be altered. This feature allows easier accomodation of changes in sensor characteristics, data processing and compaction algorithms, and transmitting formats or channels, since only the event number is stored in μP_0 memory along with the desired start-times and intervals. In addition, the single-byte identification scheme saves memory space and allows a total of 40 events to be controlled by μP_0 (rather than the maximum of 34 with the two-byte approach). This implementation permits extensive programming changes within the μP_1 system to be quickly accomplished without regard for the critical timing requirements of the μP_0 software. Obviously, this partitioning of the system software enhances overall reliability and further eases the programming burden for the DCP end user.

6.2. EXECUTIVE CONTROL PROGRAMS FOR μP_0

6.2.1 OVERVIEW

The overall operation of the PDCP/UM system is directed by firmware stored in the 6654 EPROM chips on the μP_0 processor board. There are four basic tasks performed by μP_0 which permit the platform to function with a high degree of temporal accuracy. These are (1) initialization; (2) the real-time clock routine; (3) the WWV-based time decode program; and (4) the DCP event timing/selection routine.

The essential task of the Real-Time Clock code is to implement in software an accurate clock/calendar function which provides a running calculation of actual time in days, hours, minutes, and seconds. All PDCP operations are keyed to the times calculated in this routine, which is as accurate as the μP_0 clock frequency. The WWV-based Time Decode software provides a means of continually updating the PDCP system time reference generated by the Real-Time Clock. To accomplish this, the 100Hz BCD-encoded time data transmitted by WWV or WWVH is first extracted from the 10MHz signal by an amplitude detector. The resultant audio-frequency signal is bandpass-filtered at 100Hz to remove the 1000/1200Hz marker pulses (which occur each second) and subsequently shaped by a Schmitt-trigger gate. The resultant pulse train is introduced to the $\overline{EF3}$ flag input of μP_0, as previously described in section 4.4. The Time Decode routine then decodes this train to retrieve the WWV time data, which is periodically jammed into the Real-Time Clock registers to update them to the NBS reference.

The Event Timing/Selection routine provides the interface between the Real-Time Clock and the μP_1 system and is responsible for the initiation of all PDCP events. Briefly, the Event Timing/Selection software compares the actual time with the time calculated for the next initiation of each specific PDCP event. When the actual time and a next-event time coincide, the associated task identification byte (stored in EPROM along with the next-event time for the task) is loaded into the 1852 8-bit port on the μP_0 board. The loading process causes the "service-request" flip-flop internal to the port to be set, pulling down the $\overline{INT}$ (interrupt request) line on μP_1 and initiating an interrupt. Normally,

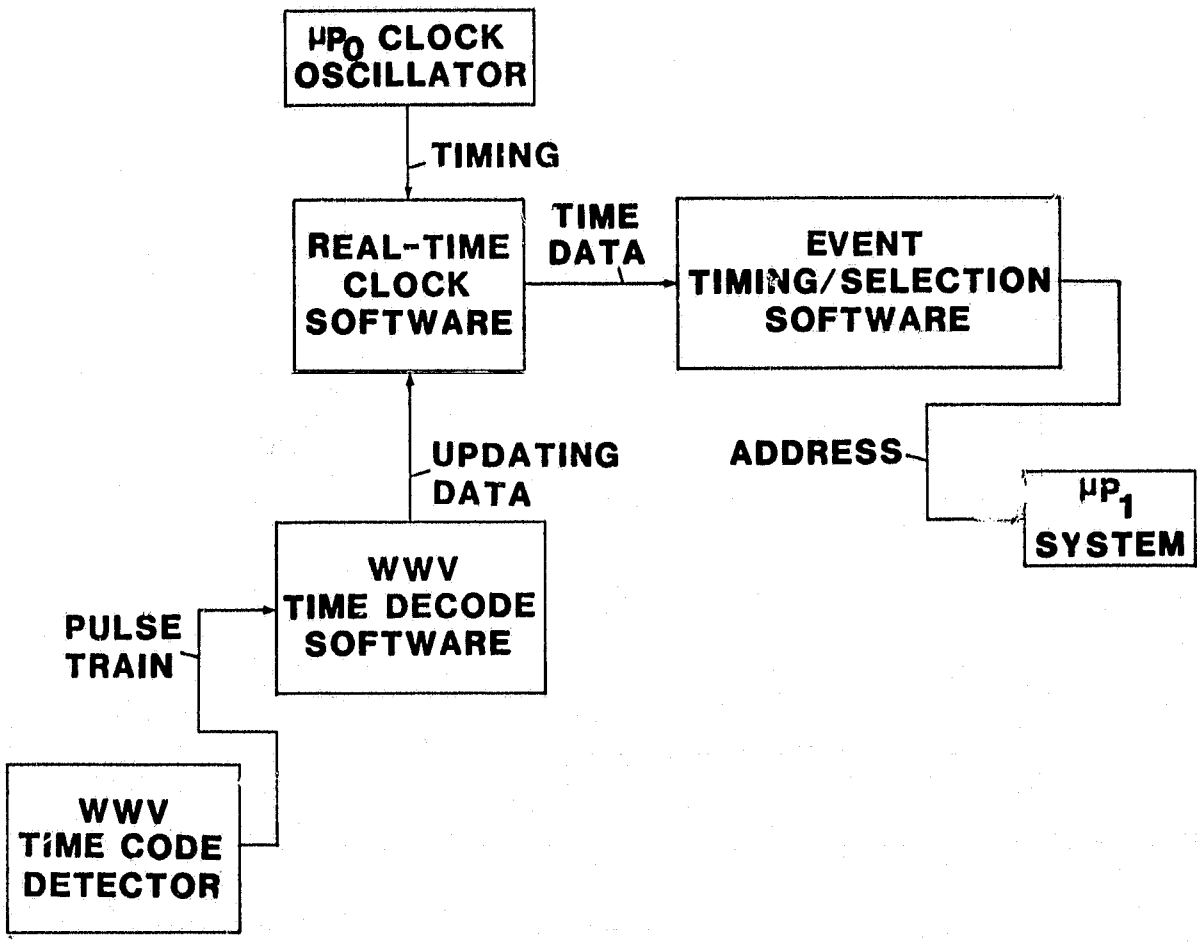

Figure 6.2.1. Program Information Flow.

μP_1 will have already been placed in the IDLE state at the conclusion of the previous task and will therefore immediately acknowledge the request and begin execution of the interrupt service routine. The data byte contained in the port is loaded into μP_1 register R2 and used as the low-order part of an address vector which points to the table location containing the starting address for the next event's software code. This address is then loaded into another CPU register which becomes the new program counter for the execution of the event routine. The final task of the Event Timing/Selection program in μP_0 is to calculate the next event time for the just-initiated task and return the results to RAM for future use. The interaction of the three basic blocks of μP_0 software is depicted in Figure 6.2.1., along with the information flow to and from each program module.

6.2.2. Main/Real-Time Clock Program

The Real-Time Clock software implements the real-time clock/calendar function with the μP_0 onboard registers and a complex chain of precisely-timed loops. The time stored is in days, hours, minutes, and seconds; the routine provides the special BCD-based modulo-60, modulo-24 and modulo-365/366 addition functions to correctly advance the clock in the absence of WWV time information. Since the worst-case increment (at 365/366 days, 23 hours, 59 minutes, and 59 seconds) involves a rollover in all units (to 1 day, 0 hours, 0 minutes, and 0 seconds), the routine must of necessity examine each denomination and digit to perform the incrementation function. The digits are all stored in BCD format to enhance compatibility with the WWV-based data received from the Time Decode program and to allow the end-user to program his event times with decimal numbers. The μP_0 register assignments are summarized in Table 6.2.2. After the Initialization routine

Table 6.2.2. Register Assignments for μP_0

Register No. (Hex)	Use
0	Main program counter
1	"Data-load/skip" S/R counter
2	"Time-update" S/R counter
3.0,3.1	Loop counters
4	"Increment" location
5	Pointer for "Data" bytes (coded time)
6.0	Shift storage
6.1	"Error" register
7.0,7.1	Loop counters
8.0	"Seconds" storage
8.1	Scratchpad
9.0	"Minutes" storage
9.1	Scratchpad
A.0	"Hours" storage
A.1	Scratchpad
B.0	"Days" storage
B.1	"Year Number" storage
C.0	"Hundred-days" storage
C.1	"Last-hundred-days" storage
D	"Next Time/Event" location
E	"Real-Time" location
F	"Zero/One counter" delay register

presets the CPU registers and certain RAM locations to their desired initial values, the WWV Time Code is demodulated and the BCD time data stored in RAM with RE serving as pointer to the time-data stack. At this point the Real-Time Clock code begins execution. To preserve the exact timing needed for the PDCP system, the overall second-by-second execution time of this routine must be held at precisely 400,000 machine cycles for the 3.2000MHz microprocessor clock.

Temporally, the Time Decode and Event Timing/Selection routines are interleaved into the Real-Time Clock program since functions of all three codes must operate concurrently. Basically, once each second the Real-Time

Clock performs an incrementation of the real-time data stored in RAM (and duplicated in registers 8,0, 9,0, A,0, B,0, and C,0 within the CPU). A special subroutine designated "Time Update" is called upon to perform the specialized addition functions necessary to properly calculate the new real-time data values. Register R4 is utilized as a pointer to the formatted data stored in EPROM which comprises the value of the increment (0 days, 0 hours, 0 minutes, and 1 second) which is added in the "Time Update" subroutine to the previously-stored numbers to produce the current values of the real-time data bytes. These bytes are (subsequently to the addition process) returned to the same stack locations in RAM for use during the next second. In addition, these values are at this time compared with the values in the Event Timing/Selection table to determine whether a PDCP event should be executed at the beginning of the next one-second interval. Figure 6.2.2.1 depicts the conceptual flow diagram for the main μP_0 software activity.

The "Load WWV Time Data" block in Figure 6.2.2.1 is executed near the beginning of each second in normal operation and occupies roughly 80% of the CPU time per second. The routine is responsible for decoding the bit stream received from the 100Hz bandpass filter/detector/shaper on the RF board. The serial BCD data stream is introduced to flag input $\overline{EF3}$ of the 1802 μP and is sensed by a branch-on-$\overline{EF3}$ instruction in the software, as shown in Figure 6.2.2.2.

Initially, registers 5,6,0, and 7,1 are reset and register 7,0 is set to #08. The serial-to-parallel data conversion begins by sensing the $\overline{EF3}$ line as mentioned above and shifting the resultant bits using R6,0. At the beginning of each loop flag $\overline{EF4}$ is tested to verify that a sufficient-strength WWV carrier is being received. If not, an error bit in the R6,1

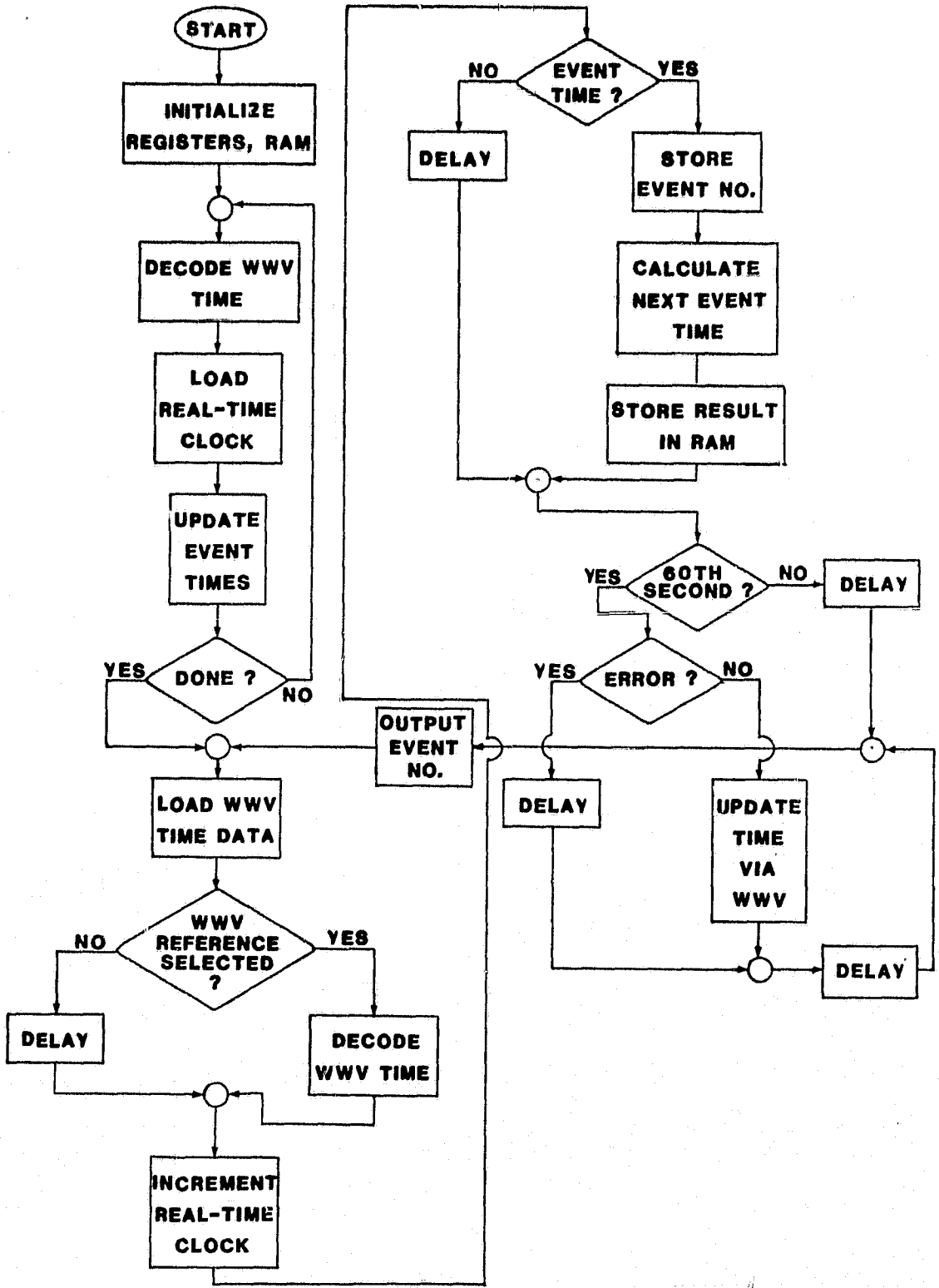

Figure 6.2.2.1. Flow Diagram for μP_0 Main Program/Real-Time Clock Routine.

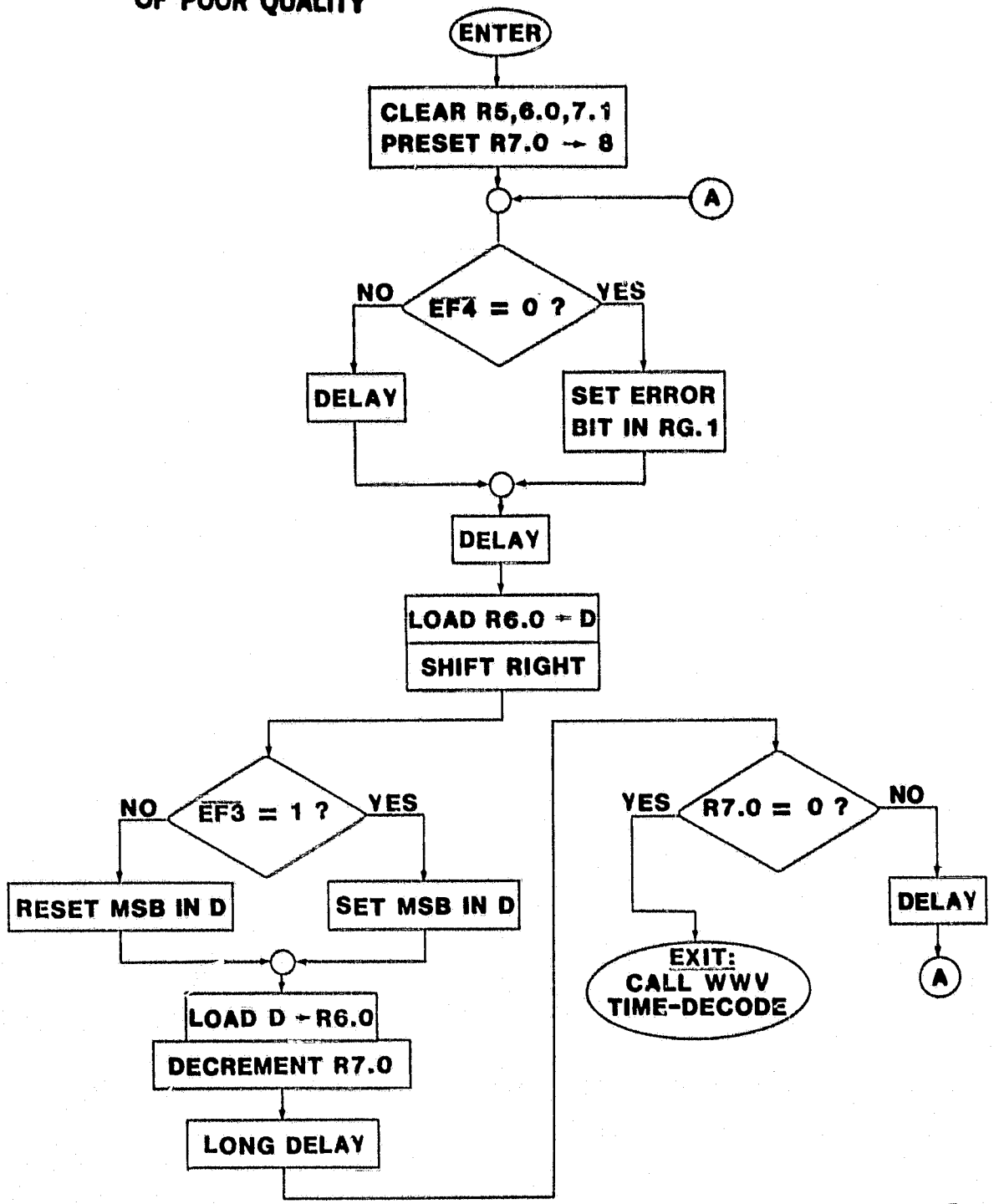

Figure 6.2.2.2. Flow Diagram for "Load WWV Time Data" Software.

Error Register is set for future reference. After a delay of roughly 50 ms, the data in R6,0 is right-shifted and a bit corresponding to the state of the $\overline{EF3}$ flag input is loaded into the MSB position. This cycle is repeated a total of eight times, until R6,0 is full. The interval for bit samples of approximately 130 ms is generated by the "Long Delay" block. After the eight samples have been acquired, the routine exits with a SET P call to the WWV Time-Decode routine, which is described in Section 6,2,3.

Depending on the operational mode, the Real-Time Clock can either be updated at the end of each minute by the data from the WWV-based Time Decode routine, or else run on its own internal software-based timing, which is ultimately dependent on the accuracy of the 3,2MHz microprocessor clock. It is desirable to provide both options, since many existing DCPs use a simple crystal-oscillator/divider network to provide timing intervals and thereby do not respond to the periodic updating (by means of leap seconds) of the NBS time standard which is broadcast by WWV and WWVH. In order not to lose time-synchronization with respect to these older DCP's, the leap seconds must be ignored by the PDCP system; of course, the PDCP will still possess a highly-accurate time base due to the periodic tweaking of the 3,2MHz system clock frequency by the WWV-based Frequency-Correction software contained in the μP_1 system. Additionally, it is necessary to skip the updating process for the Real-Time Clock data after a low-signal condition of the WWV RF carrier has been detected, since the decoded data would be of questionable accuracy. These conditions are handled in the Flow Diagram of Figure 6,2,2,1 by the delay loops associated with the "WWV Reference Selected?" and the "Error?" decision blocks. If the WWV time reference is not selected, the Real-Time Clock will not call the

WWV Time-Decode subroutine. Similarly, the block labelled "Update Time Via WWV", which simply implements the loading of decoded WWV time from RAM into the registers (R8.0, 9.0, A.0, B.0, and C.0) and RAM locations reserved for the Real-Time data, is replaced by a suitable delay, and the Real-Time Clock routine continues.

The block designated "Increment Real-Time Clock" is responsible for the second-by-second updating of the clock data. As previously mentioned, the actual time increment (0 days, 0 hours, 0 minutes, and 1 second) is added via the "Time Update" subroutine to the existing real-time data; the result is returned to the previously-mentioned registers and RAM locations, for use by the following Event Timing/Selection routine.

The "Time Update" subroutine is utilized within the Initialization, Real-Time Clock, and Event Timing/Selection routines. In addition to its use in the "Update Event Times" portion of the initializing software, the subroutine is executed at least once each second to keep the real and next-event times current. A flow diagram for the subroutine is shown in Figure 6.2.2.3.

Upon entering the subroutine, the data pointer "X" is set to 4, and the Unit Seconds (U.S.) digit contained in R8.0 is tested to determine if its value is greater than or equal to seven. If so, the U.S. increment in RAM (pointed to by R4) is added and the result is tested to see if it is ≥ 4. If so, the data is corrected to the true BCD value by adding the hexadecimal number six (#06); if not, the routine delays the length of the last addition and proceeds to test the sum. If in the initial test the U.S. digit is < 7, then a simple delay followed by addition of the U.S. increment from RAM precedes the sum test. If the sum, as indicated in the decision block (third from the top), is greater than nine, the Ten Seconds

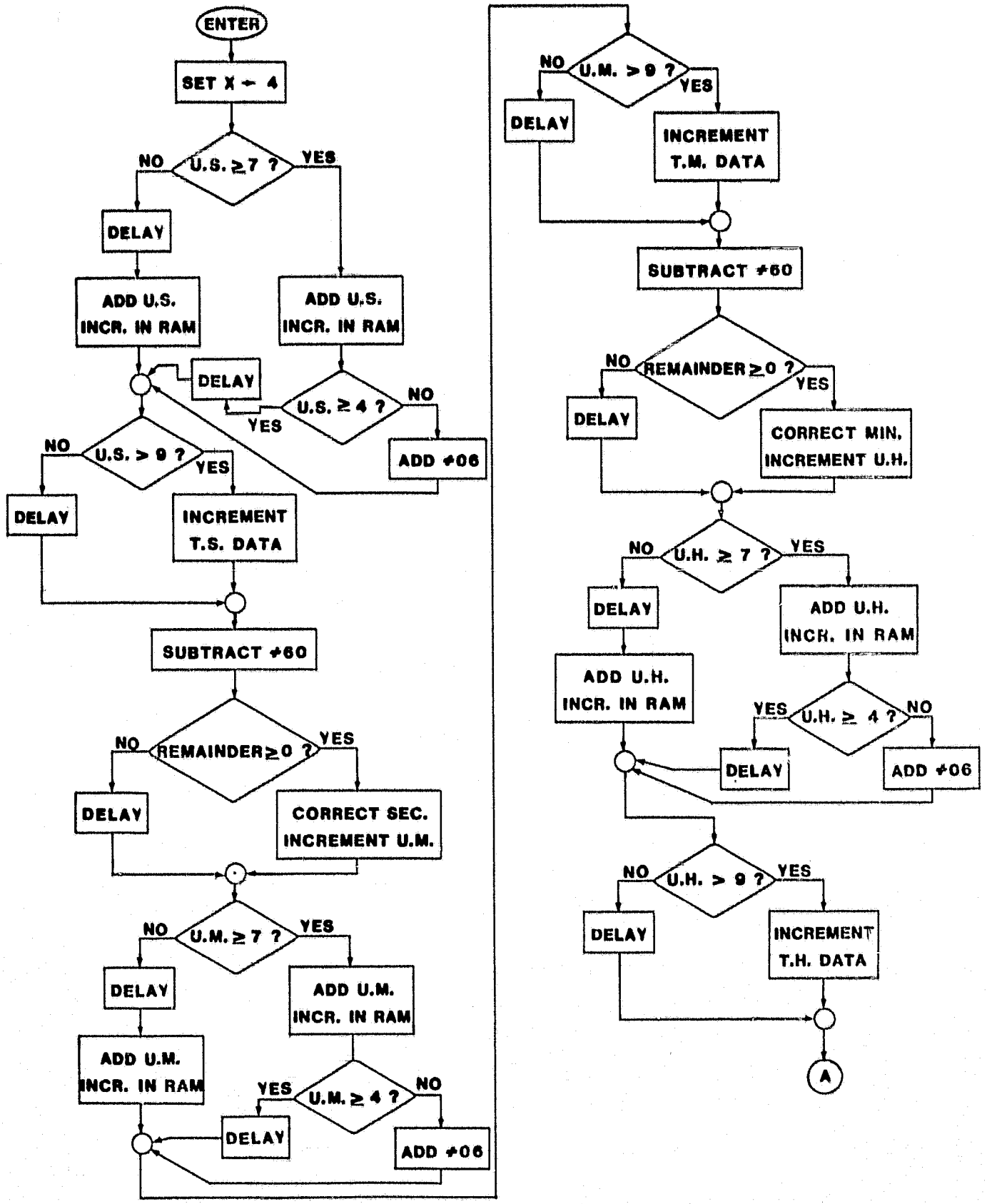

Figure 6.2.2.3. Flow Diagram for Time-Update Subroutine.

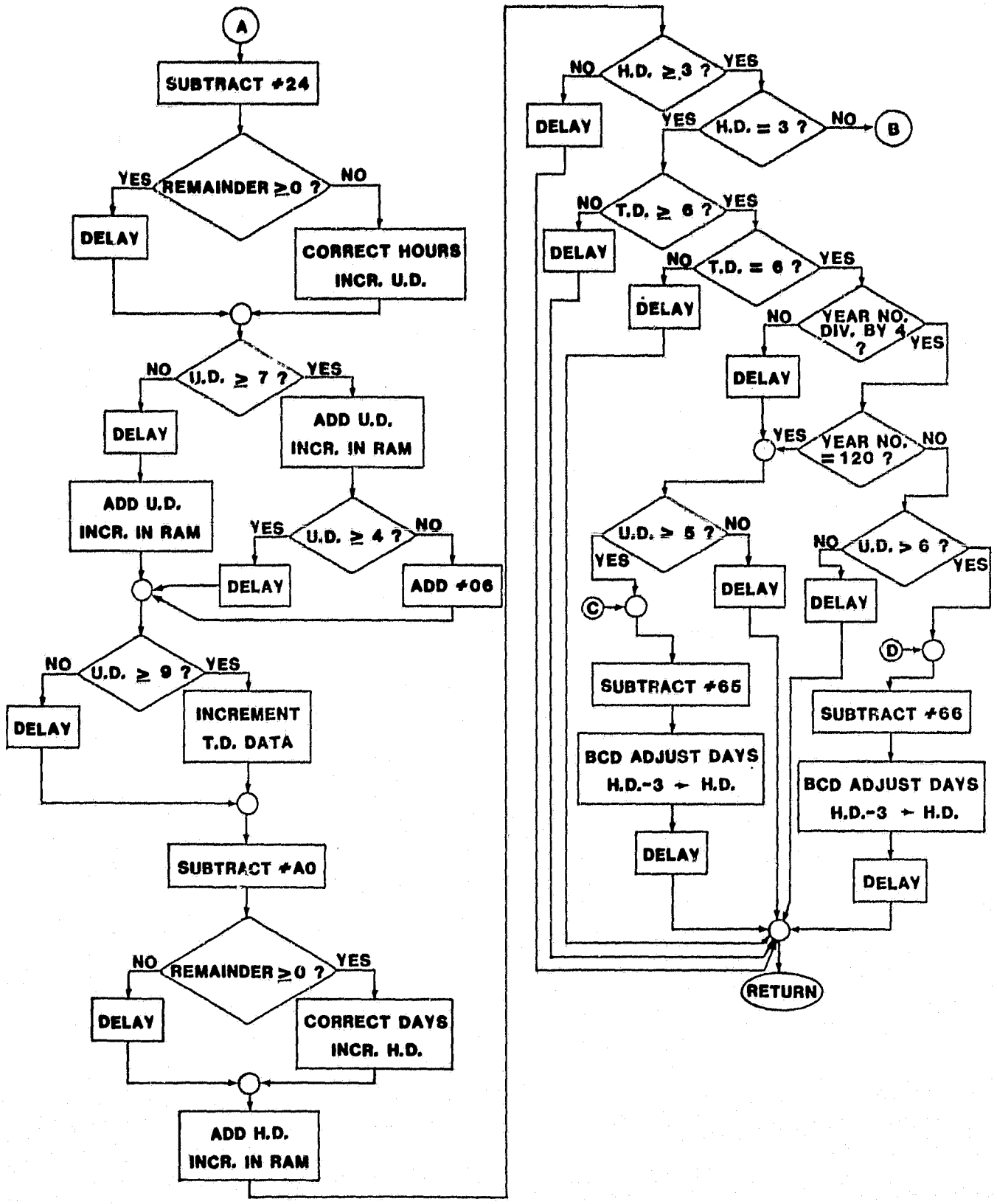

Figure 6.2.2.3. Continued.

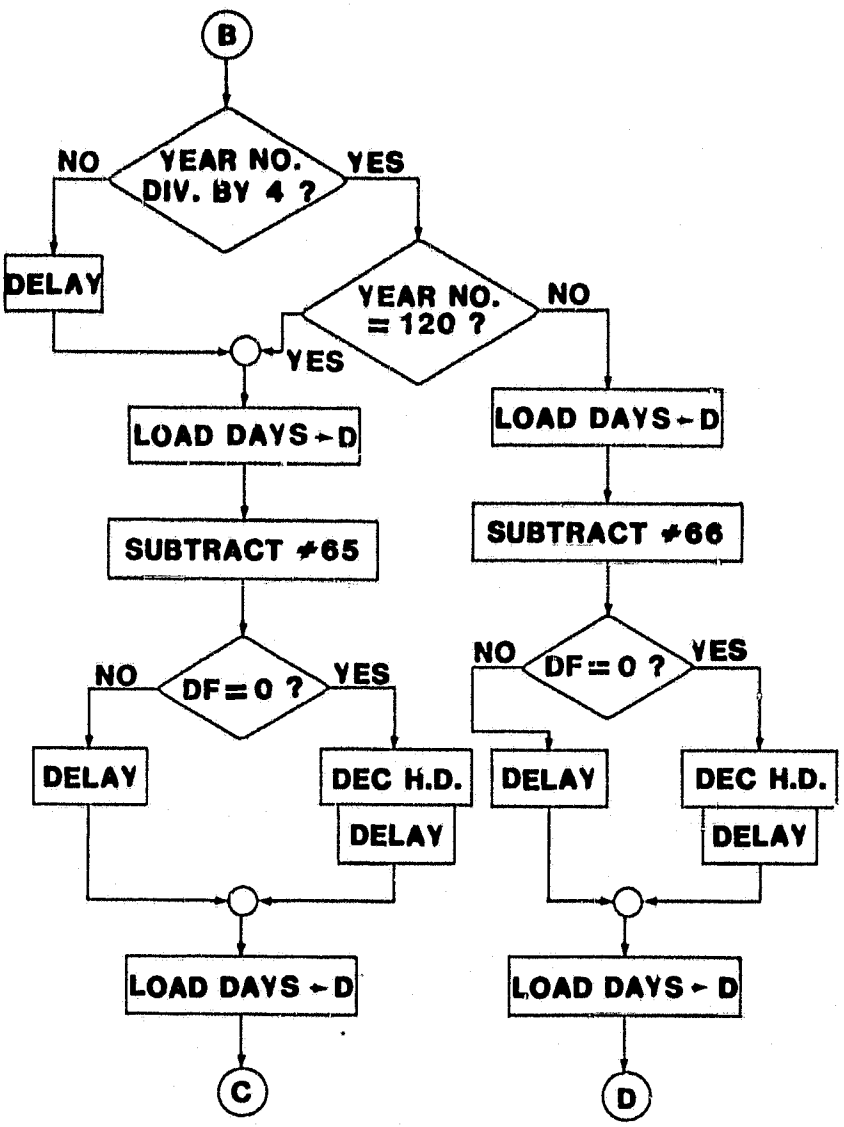

Figure 6.2.2.3. Flow Diagram for Time-Update Subroutine (cont.).

(T.S.) digit is incremented; if not, a corresponding delay is executed. Now the result has #60 subtracted from it and the remainder is tested; if it is positive or zero, the seconds (T.S./U.S.) byte is BCD-adjusted and the Unit Minutes (U.M.) digit is incremented. If the remainder is negative (indicating no carry), the routine delays to maintain the desired loop timing. The substantial number of delays inserted here and throughout most of the μP_0 software (and many of the μP_1 routines) are indicative of the exact timing required by the programs to maintain precise synchronization and accurate interval generation. All possible program paths must have identical execution times; furthermore, the entire program cycle must in this case be exactly 400,000 machine cycles (one second) long. Hence, the delays in the program both equalize parallel branch times and adjust the entire routine to the desired length.

Now that the Seconds data has been calculated, the identical process is applied to the Minutes data, generating a possible carry into the Unit Hours (U.H.) digit. Likewise, the Hours data is added and BCD-adjusted, except that the modulus used in testing for the carry information is 24, rather than 60. If the Hours sum equals or exceeds 24, the Unit Days (U.D.) digit is incremented and #24 subtracted from the Hours figure. The correction algorithm leaves the true BCD representation of the Hours data in RA.0, and calculation of the Days value begins.

The processing of the Days data is significantly more complex than that for Seconds, Minutes, and Hours. Not only must the modulo-100 addition be performed on the T.D. and U.D. digits to determine the Hundred Days (H.D.) value, but the entire figure must be corrected to a modulo-365 or -366 format, depending on whether or not the given year is a leap year. The process for calculating the Days digits is very similar to the basic

system used to calculate Seconds and Minutes, except that the carry is generated only when the Days sum (after adding the increment) is at least equivalent to #A0. If the remainder is zero, or positive, the Days value is corrected and the H.D. digit is increased by one. Next the H.D. value is tested to see if it is ≥ 3. If not, then no possibility of rollover to the next year exists and the routine causes a delay before returning to the calling program. If, however, the H.D. digit is at least three, the data must be tested further. If H.D. = 3, then the T.D. value is analyzed; if T.D. < 6, then no carry exists and the necessary delay is executed. For T.D. = 6 the possibility exists for a carry, if U.D. > 5 (or U.D. > 6 for a leap year). The leap year status is determined by first ascertaining if the year number is divisible by four; this is quickly implemented by testing the last two bits of the hexadecimal number for zeros. (The test for year number = 120 is implemented primarily for illustrative purposes; the first year divisible by four which is not a leap year (in the Gregorian calendar system) is 2100 A.D., which is year 120 from 1980 (assumed to be year zero). Thus the Real-Time Clock should theoretically provide an accurate calendar function until 2200 A.D.) Depending on whether or not the given year is a leap year, either #65 (for 365 days) or #66 (for 366) is subtracted from the U.D. digit, if the value of U.D. exceeds 5 (common year) or 6 (leap year). The remainder is then BCD-adjusted and three subtracted from H.D. If U.D. is not greater than the index, the routine simply implements an appropriate delay and then returns to the calling program. The last possible branch in this routine occurs if H.D. > 3; the program decisions are essentially identical to those in the previous routine, except that if after the subtraction of #65/#66 there is a borrow, then the H.D. digit is decremented once. The code then branches back to the

H.D. = 3 path to BCD-adjust the Days data and subtract 3 ; from H.D. before returning to the original routine which called "Time Update."

6.2.3. WWV Time-Decode Routine

When activated, the WWV Time-Decode software provides a stable, accurate means of analyzing the BCD time-of-year code which (along with other signals) amplitude-modulates the WWV and WWVH carrier signals. The data is presented as a specific sequence of selective-length bursts of a 100Hz tone which modulates the main carrier to a depth of 25%. The format is a modified IRIG-H code which consists of a 1.03-second "hole" (necessary due to the lengthened minute-marker pulses); a string of eight zeros; a position identifier pulse; and seven sets of BCD digits corresponding to the time. The marker pulses consist of 80 cycles of 100Hz; binary ones are 50 cycles and binary zeros are 20 cycles of the 100Hz subcarrier frequency.[2] Since these binary pulses are time-multiplexed with the more familiar 1000Hz (WWV) or 1200Hz (WWVH) seconds-marker "ticks", the leading edges of all the 100Hz bursts are delayed 30ms from actual time; this offset is compensated for in the Time-Decode software. Figure 6.2.3.1. provides a chart of the time code and its various features.

Referring to Figure 6.2.3.1. and to Figure 6.2.3.2, the flow chart for the WWV Time-Decode routine, it is evident that the code characteristics require that the decoding software be executed in segments corresponding to the distribution of time-code information during the entire one-minute span. Once each second the main program effects a call to the Time-Decode routine, whose program counter is R1, by a simple SET P=1 instruction. Most of the time available each second is spent in the analysis of the serial bit patterns to enable decoding of the data bits by the WWV Data

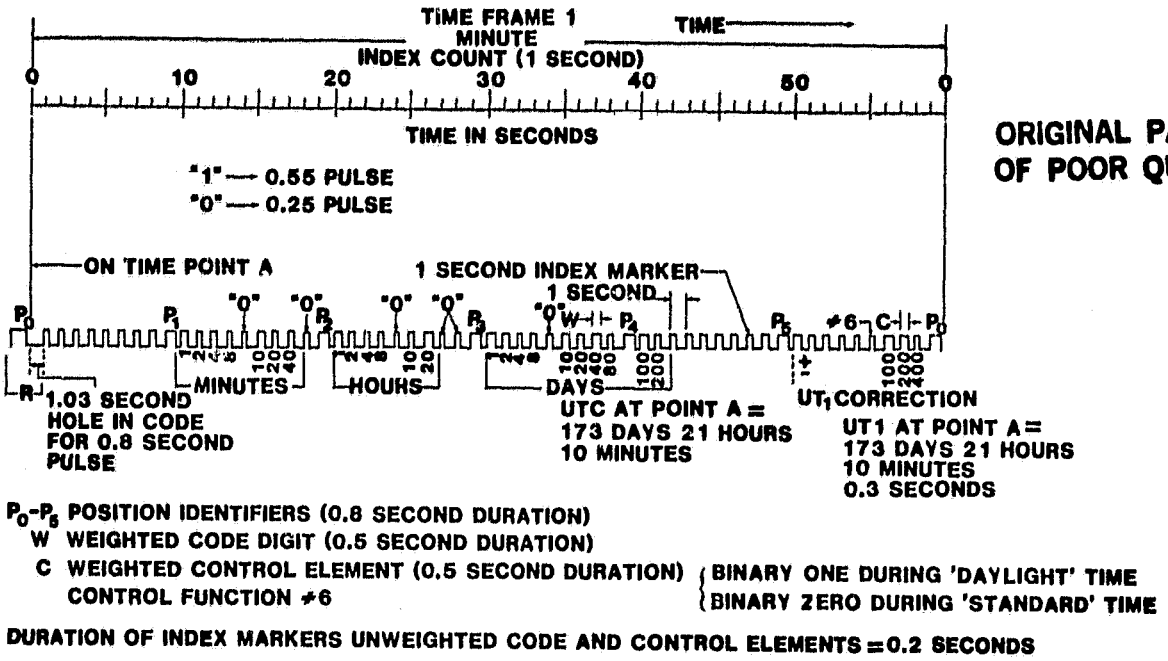

Figure 6.2.3.1. Chart of time code transmissions from NBS radio stations WWV and WWVH.

Figure 6.2.3.1. Chart of time code transmissions from NBS radio stations WWV and WWVH.

Load section of the Main program; the Time-Decode routine then sorts these bits into the compacted BCD-oriented format used by the PDCP operating software to store the time data in RAM. Since the code characteristics also require numerous synchronizing and marker pulses in addition to the actual time data, the Time-Decode software (to minimize dynamic RAM storage size requirements) must discard these auxiliary bits while performing the data-word decoding in real-time.

After recognizing (and subsequently ignoring) the "hole" in the code (second 1) and the following string of eight zeros (seconds 2-9) plus the P_1 marker pulse (second 10), the software starts the actual time-code acquisition during second 11, when the LSB of the Unit Minutes data is

being transmitted. As can be seen from Figure 6.2.2.2, the processing during the data intervals (seconds 11-14, 16-19, 21-24, 26-29, 31-34, 36-39, and 41-44) is almost identical; the only differences are in the states of the nested loop counters, R3.0 and R7.0. At the conclusion of each group of four bits (i.e., one BCD digit), the program steps to a delay routine which occupies the time slots within seconds 15, 20, 25, 30, 35, and 40, thus skipping over these zero and marker bits. Seconds 45-59 also contain filler or superfluous bits and are similarly skipped, since the UT1 correction and Daylight/Standard time information bits contained therein are not used by the PDCP software.

During second 60 the presence of the P_0 marker pulse is detected; if the pulse does not occur, the bit pattern in R6.0 is tested for a bit 0. If the bit is a zero, the second is assumed to be a leap second and a delay of roughly one second is invoked before the routine proceeds. If the bit is not a zero, a bit error is noted and execution continues in a normal fashion. The routine at this point returns to the main program and the entire one-minute cycle repeats.

The time-decoding operation actually occurs in the block (in Figure 6.2.3.2) designated "Decode/Load Data". Here the bit patterns loaded into R6.0 each second are deciphered into binary bits and the bits then grouped into sets of two BCD digits for the Minutes, Hours, Days, and Hundred Days entries subsequently stored in RAM. Upon entering the routine, the byte in R6.0 is decoded to determine if the represented data bit is a zero or a one. According to the result, the MSB of the RAM byte is either reset or set, and the data stored in scratchpad register R8.1. On the last digit (for Hundred Days) the top six bits of the RAM byte are arbitrarily reset; the completed data array is then stored in RAM using R5 as a data pointer.

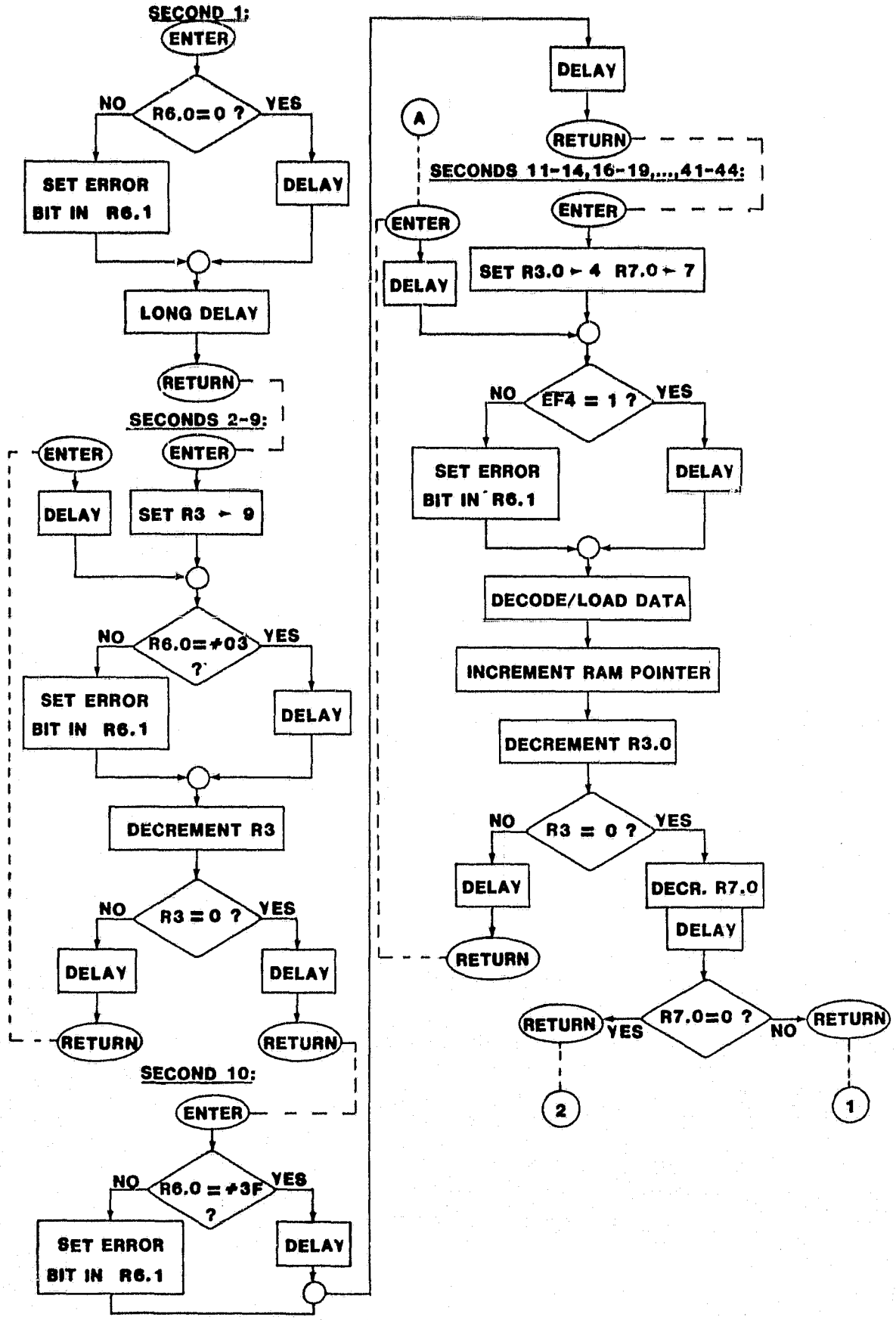

Figure 6.2.3.2. Flow Diagram for WWV Time-Decode Routine.

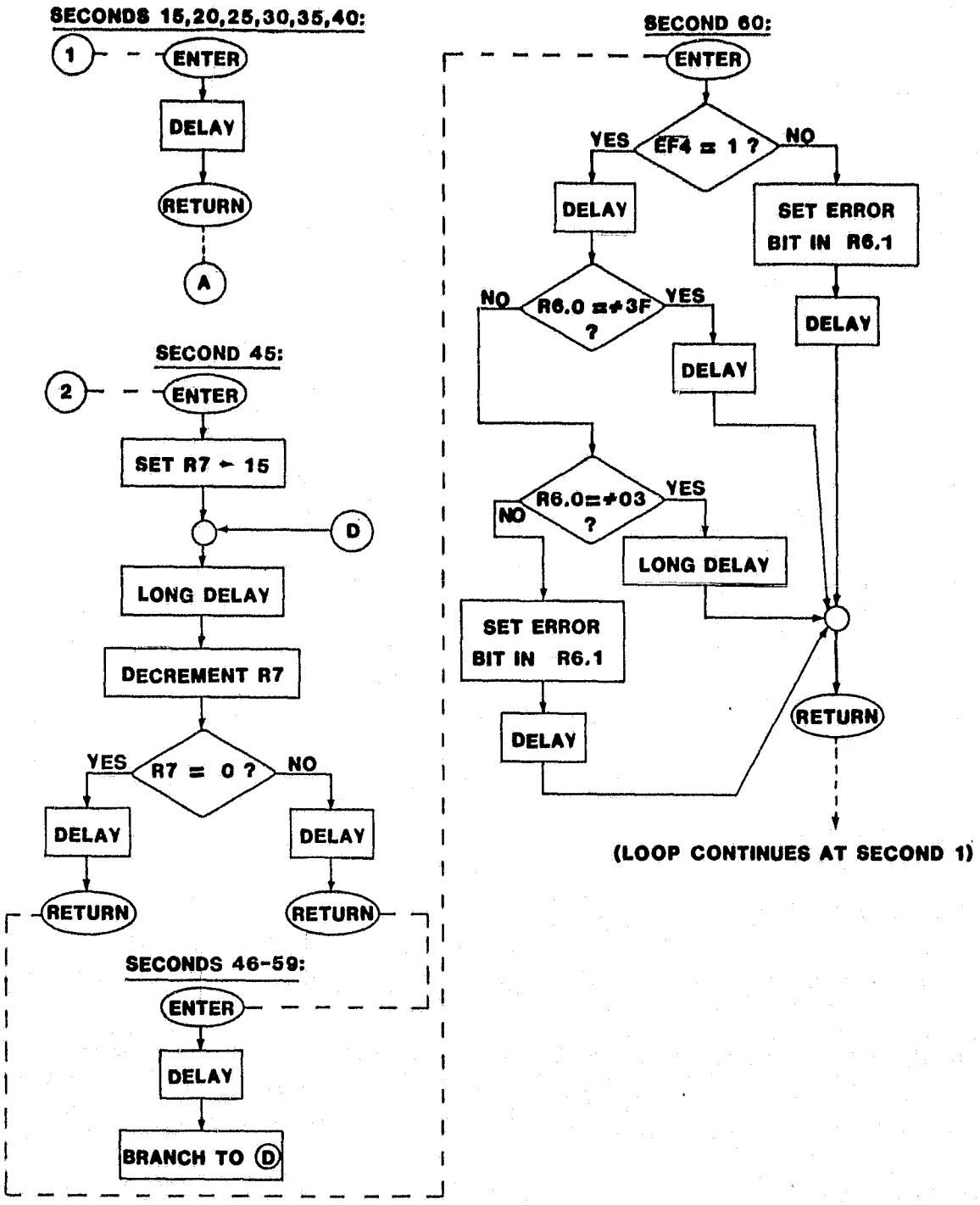

Figure 6.2.3.2. Continued.

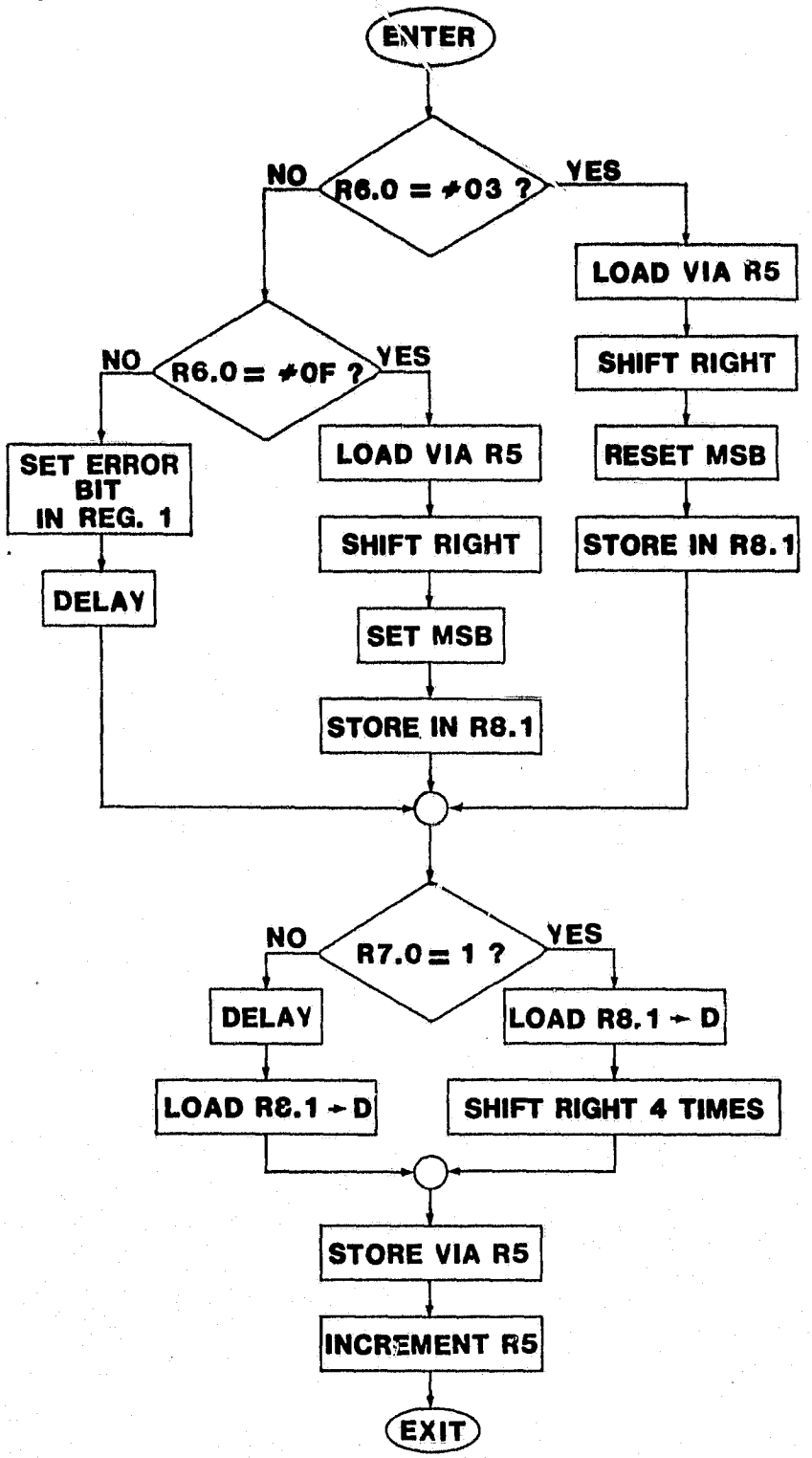

Figure 6.2.3.3. Flow Diagram for "Decode/Load Data" Routine.

The data is thus placed into RAM in the final desired BCD/units format and is now available for use by the "Update Time via WWV" routine.

6.2.4. Event Timing/Selection Routine

Once the system is operating properly on the Real-Time Clock software, the timing for the various desired PDCP events can be specified. The Event Timing/Selection software first transfers the Real-Time Clock data from registers R8,0, 9,0, A,0, B,0, and C,0 to a stack in RAM designated by RE. The total number of events is loaded into R7,1 to provide indices for both the data comparison and the "Long Variable Delay" functions. Each event is scanned every second (primarily to equalize the loop execution times), but only one event is permitted to be triggered each second. If a proper match between the next-event time and the real-time data is detected, the one-byte event number is stored in a RAM location (to be outputted to μP_1 at the end of the current second). The routine now calls the "Time-Update" subroutine and returns with the new data for the next time the specified event is scheduled to occur. Finally, if a rollover in the Hundred Days digit is noted, the "year number" index is incremented and the routine returns to the Main program.

The "Long Variable Delay" block is used to compensate for the varying number of user-programmed events desired; as different numbers of PDCP functions are needed, the code inserts a calculated amount of delay to ensure that the overall loop execution times will remain constant. The pertinent details of the routine are given in Figure 6.2.4.

Programming the EPROM associated with this routine is the only task necessary for the PDCP user, and the simple format of BCD event-time data followed by a seven-bit event number (MSB=0 for the stored byte) allows

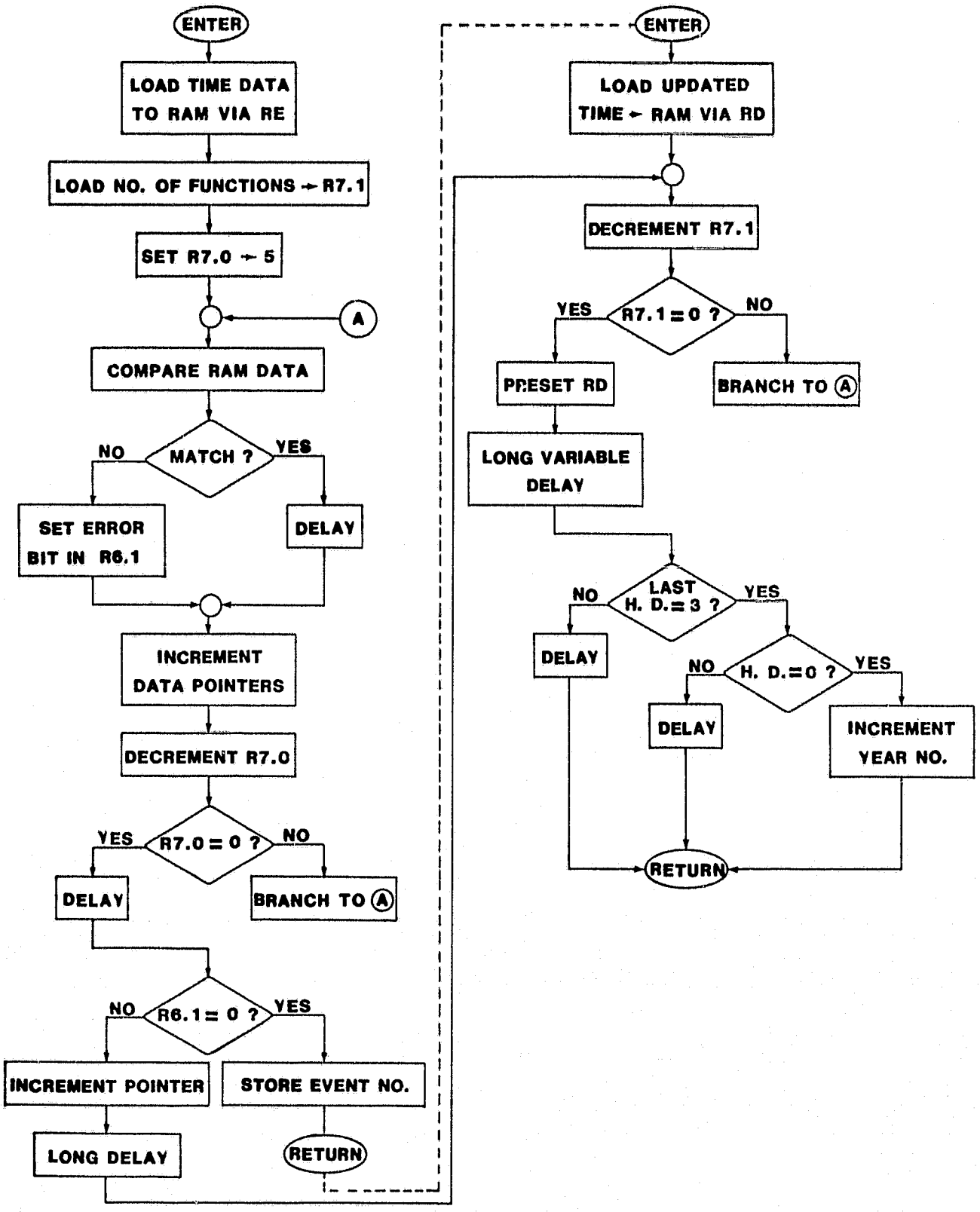

Figure 6.2.4. Flow Diagram for Event Timing/Selection Routine.

easy setup of the PDCP system even when complex sequences of events are desired.

6.2.5. Overall μP_0 Software Timing

The sequencing of the interleaved routines is accomplished primarily by a complex series of subroutine calls implemented with the unique SET P instructions available on the 1802 microprocessor. The critical nature of the program requires that each loop be precisely timed, though the uniform instruction lengths (2 or 3 machine cycles) of the 1802 drastically ease the program timing burden. [3] The overall timing cycle for a given second (referred to the WWV specification) is shown in Figure 6.2.5.

Obviously, the Main/Real-Time Clock routine occupies the vast majority of the total time; the relative execution times of the called routines comprise only about 15% of the typical second. The speed with which microprocessors can perform DCP-related tasks can be appreciated more fully by realizing that delay loops actually consume over 80% of the total second with the 5μS/7.5μS instruction times specified by the 3.2MHz system clock.

6.2.6. System Initialization Program

The final aspect of μP_0 software to be examined is the power-up Initialization routine, which takes the system from the reset condition and configures all register and RAM locations to their desired initial values prior to the startup of the Main/Real-Time Clock loop. First, the various registers serving as program counters, data pointers, and loop counters are preset to the necessary values. Next, the PDCP software is synchronized to the WWV time code and the Main Loop executed until the WWV time is properly acquired and the real-time clock updated. Now that the time base is established, the Event Timing/Selection routine (with

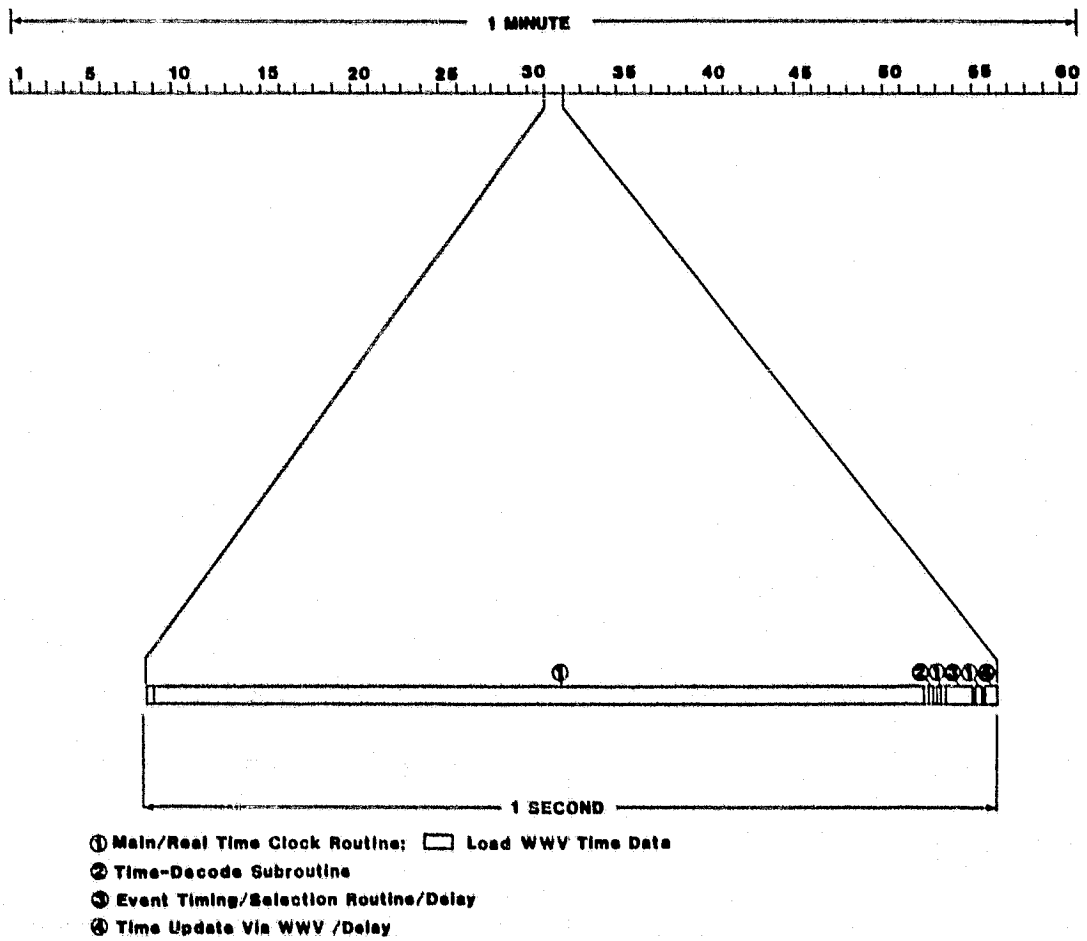

Figure 6.2.5. Diagram of Relative μP_0 Software Timing.

output inhibited) is called and each entry in RAM updated. The procedure involves adding the basic start-time for the desired event and the specified interval time to get the next desired incidence of the specific function. The result of the addition is compared with the recently-established real-time data; if the calculated next event time number is less (i.e., an earlier time), the event time is incremented repeatedly until the final result is greater than the real-time figure. The data pointer then advances,allowing the algorithm to update each event in turn until all are preset to values corresponding to future time. To facilitate updating of short-interval events such as TIROS-N satellite transmission tasks, the program can upon user request bypass the days/hours additions by jamming in the desired next-event days/hours values directly from the real-time registers, thereby drastically shortening the initial updating process. The absence of delays in this routine is due to the lack of any need to rigidly time these operations; in fact, it is desirable for this portion of the code to execute as quickly as possible so that PDCP setup time for the field technician may be minimized. Once the updating process is completed, the routine jumps to the Main/Real-Time Clock code and normal PDCP operation begins. A flow diagram for the Initialization Program is provided in Figure 6.2.6.

6.3 DATA PROCESSING/TRANSMITTING ROUTINES FOR μP_1

6.3.1 OVERVIEW

One of the salient features of the PDCP/UM system is the nearly-transparent compatibility with previously developed routines described in the Final Report document for Contract NAS5-22495,[4] All the programs for arithmetic computation, data acquisition, and data reduction can be directly

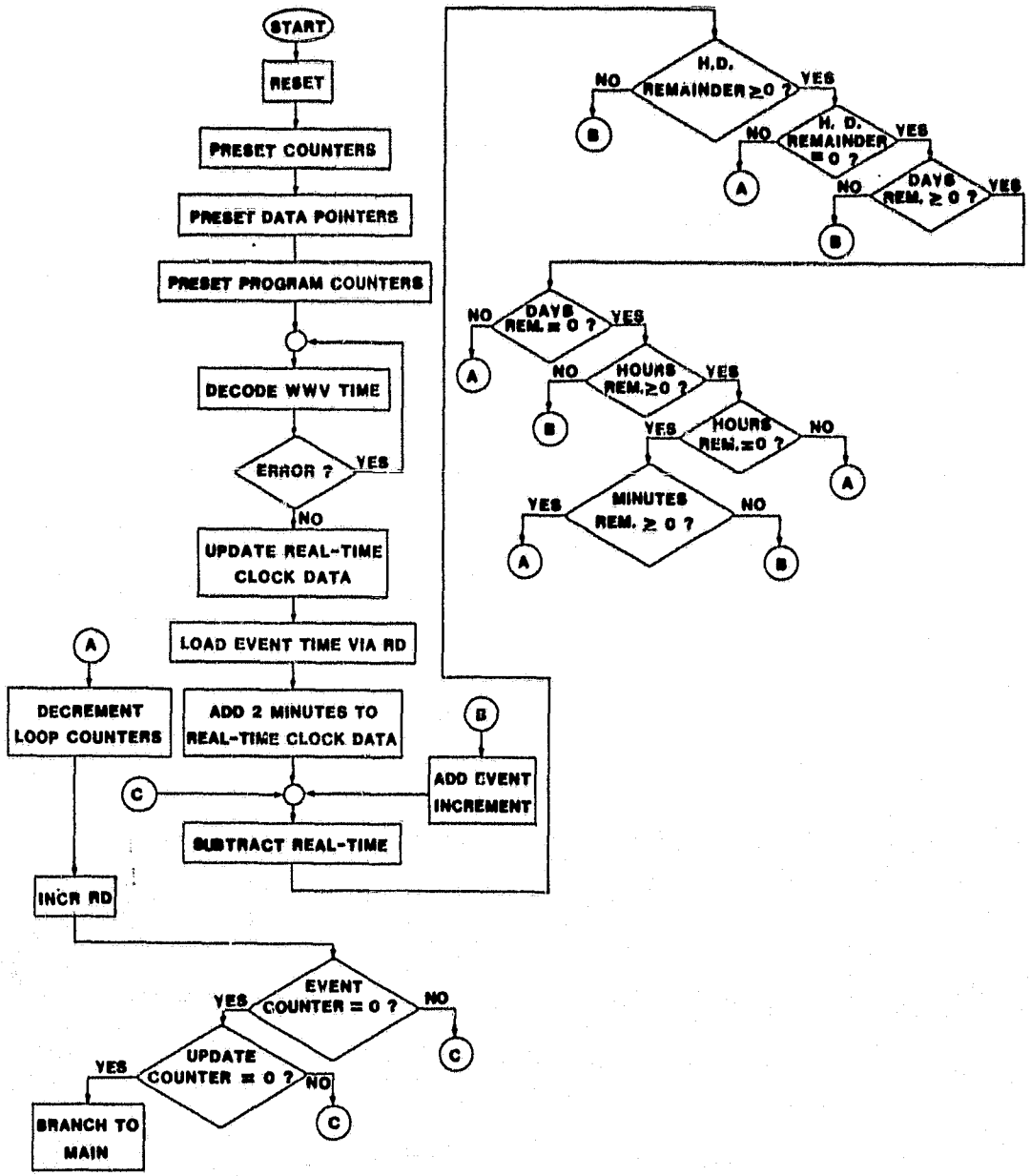

Figure 6.2.6. Flow Diagram for Initialization Program.

utilized by simply providing the appropriate starting vectors in the ATCAR address table contained in EPROM. Thus the complete data-handling package developed for the UT Model PDCP can be utilized with the PDCP/UM system without modification. The data transmitting routines, however, do require slight changes to accomodate the addition of the digital oscillator hardware to the system; these differences are discussed in the following section.

The second significant aspect of the software programming for the PDCP/UM implementation is the total modularity of the μP_1 software. Since μP_0 has the task of triggering all system functions and maintaining proper timing, it is left to the user only to specify the actual routines he needs for acquiring and transmitting data through the PDCP facilities. The desired programs may be stacked into the EPROM μP_1 memory, separated only by a single IDLE instruction (op code #00). Each routine is called by μP_0 software through a hardware-driven interrupt scheme which permits completely random accessing of all μP_1 subprograms. Additionally, each μP_1 program is free to call any others using SET P, ATCAR, SCRT, or other linkage techniques; thus great flexibility is retained along with the advantages of software modularity. (For complete documentation of the data acquisition, arithmetic, and data-reduction PDCP software, the reader is referred to the NAS5-22495 Final Report). The utility of modular software blocks can be extended even further by the use of a memory-efficient high-level language such as FORTH. With FORTH (and particularly the more advanced forms of the language) the complex routines needed for computations and even data formatting can be easily and quickly accomplished with very little penalty in RAM size, while reserving the actual data-transmission tasks to machine code to facilitate timing. Thus the user could easily develop his own efficient data-analysis software with little regard

for RAM space limitations or interactions with preprogrammed machine-language modules.

6.3.2 PDCP Transmitting Routines

The data transmission software performs the tasks of data formatting and transmitter control necessary for DCP activity. In the PDCP/UM system the transmitter control functions include not only switching the RF excitation and +12 volt power but also specifying the operating carrier frequency, modulation form (MSK/FSK/PSK), and deviation. The latter three parameters are determined by the control bytes sent to the digital oscillator; the two-byte Frequency Index (F.I.) and single-byte Phase Index (P.I.) fully specify the modulation format of the RF signal. (A complete discussion of digital oscillator system operation is contained in Chapter 2).

The specifications for data transmission to three currently-used satellites, along with flow diagrams for the respective transmitting routines, are given in the following tables and figures. [5] The only significant changes between these routines and the corresponding ones in the NAS5-22495 report are the additions to handle the F.I. and P.I. output data and changes in certain loop-counter constants to maintain the proper data bit rates. Note that the software control of the Q flip-flop, although not necessary for a digital oscillator-equipped transmitter, is retained to facilitate control of older transmitter modules and to provide serial data for use through a telephone-line modem or other similar device. Also, the power-up/power-down instructions to control the digital oscillator board as well as the transmitter are included to reduce the overall operating PDCP/UM system power requirements.

Table 6.3.2.1. and Figure 6.3.2.1. provide specifications and program

flow for the NIMBUS-F (TWERLE) system; Table and Figure 6,3,2,2 describe TIROS-N transmissions; and Table and Figure 6,3,2,3, deal with the GOES requirements and software.

Table 6.3.2.1.

NIMBUS-F (TWERLE) DATA TRANSMISSION

SEQUENCE SPECIFICATIONS

Transmission Interval:	64 seconds nominal
Transmission Length:	1 second nominal
Transmission Rate:	100 bits per second
Coding:	Manchester encoded with a 0 → 1 transition representing a 1
Modulation:	PSK, ± 60°

Transmission Sequence:

1. Transmitter power-up followed by a 1 second warm-up delay
2. Clear carrier transmission for 0.32 to 0.36 seconds
3. Data transmission
   - a. Bit synchronization code (1Ø1Ø1Ø1Ø) (8 bits)
   - b. Frame synchronization code (11Ø1Ø11ØØØØØ) (12 bits)
   - c. Address code (assigned to user) (10 bits)
   - d. Mode bits (2 MSB's of radio altimeter data, LSB first) (2 bits)
   - e. Data bits (32 bits, LSB first)
     1) Radio altimeter data (8 bits)
     2) Air temperature data (8 bits)
     3) Air pressure data (8 bits)
     4) Pressure/temperature data (8 bits)
4. Transmitter power-down

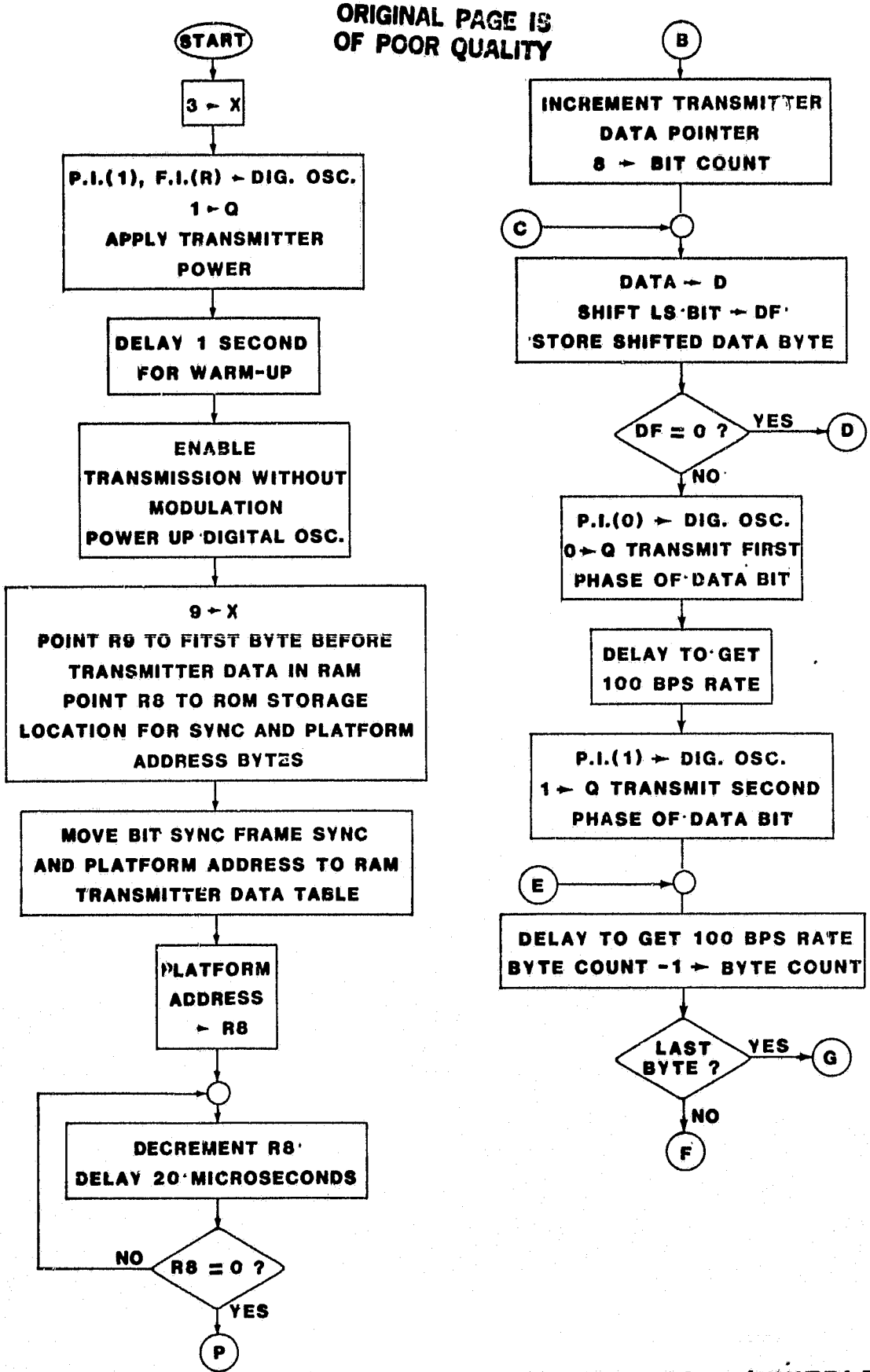

Figure 6.3.2.1. A Flow Chart for the NIMBUS-F (TWERLE) Data Transmission Subroutine.

ORIGINAL PAGE IS
OF POOR QUALITY

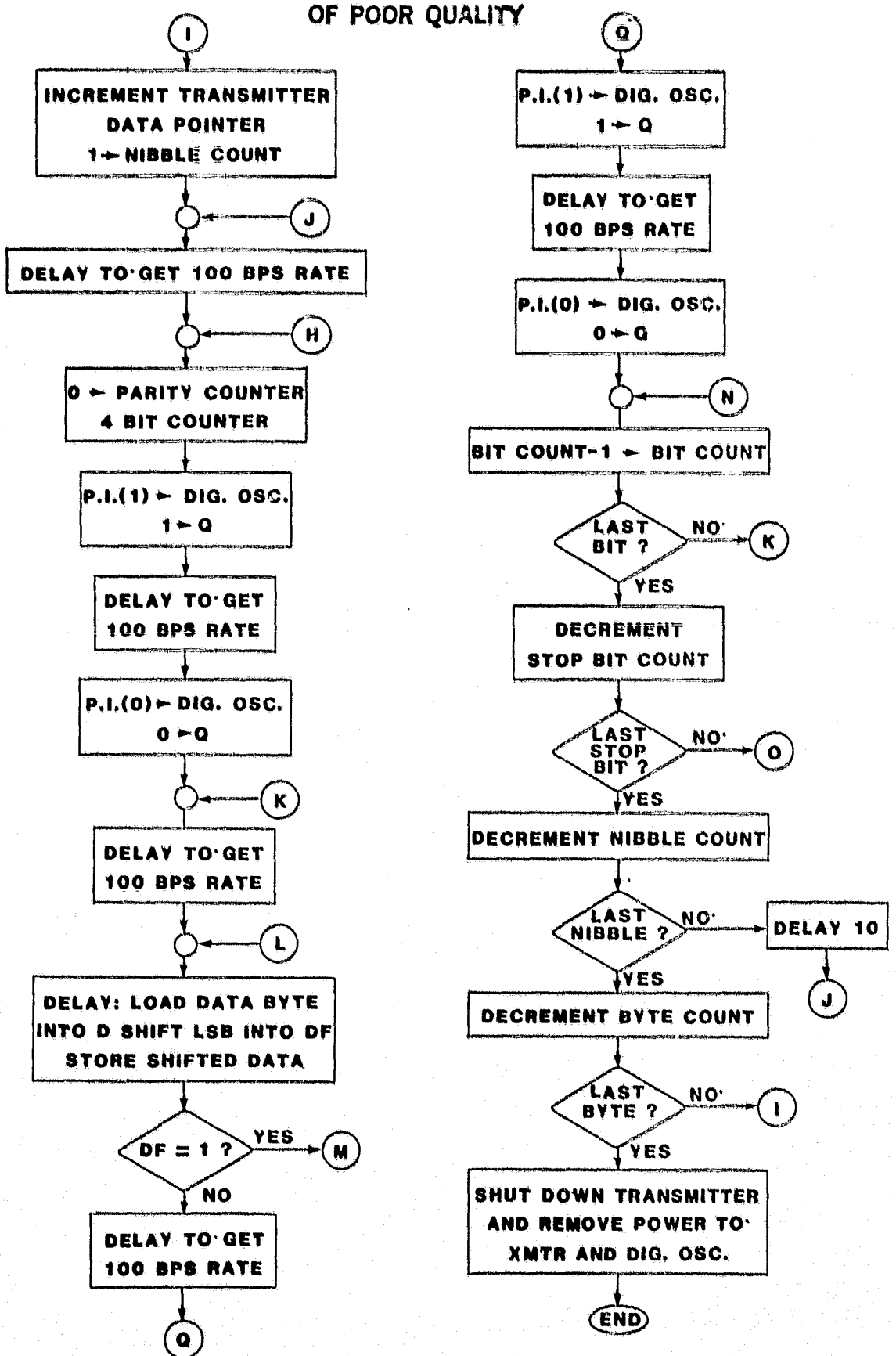

Figure 6.3.2.1. Continued.

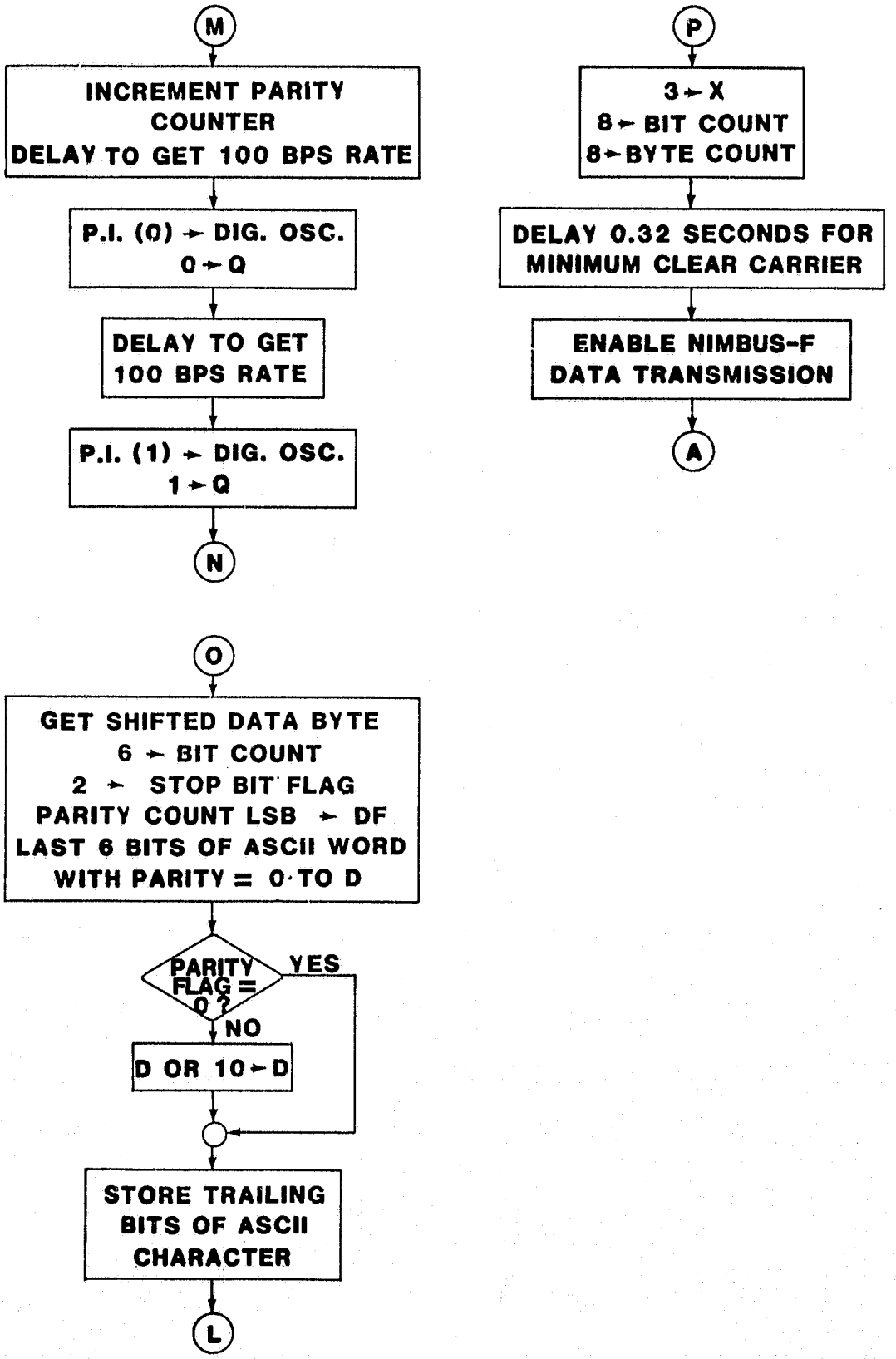

Figure 6.3.2.1. Continued.

Table 6.3.2.2

TIROS-N DATA TRANSMISSION
SEQUENCE SPECIFICATIONS

Transmission Interval:	Variable 40, 60 or 80 seconds
Transmission Length:	360 milliseconds nomial
Transmission Rate:	400 bits per second
Coding:	Manchester encoded with a 0 → 1 transition representing a 1
Modulation:	PSK, ± 60°

Trnamission Sequence:

1. Transmitter power-up followed by a 1 second warm-up delay
2. Clear carrier transmission for 160 ± 2.5 milliseconds
3. Preamble transmission
   a. Bit synchronization clock (15 bits)
   b. Frame synchronization code (ØØØ1Ø1111) (9 bits)
   c. Address code (assigned to user) (24 bits)
4. Data transmission - four bytes (32 bits)
5. Transmitter power-down

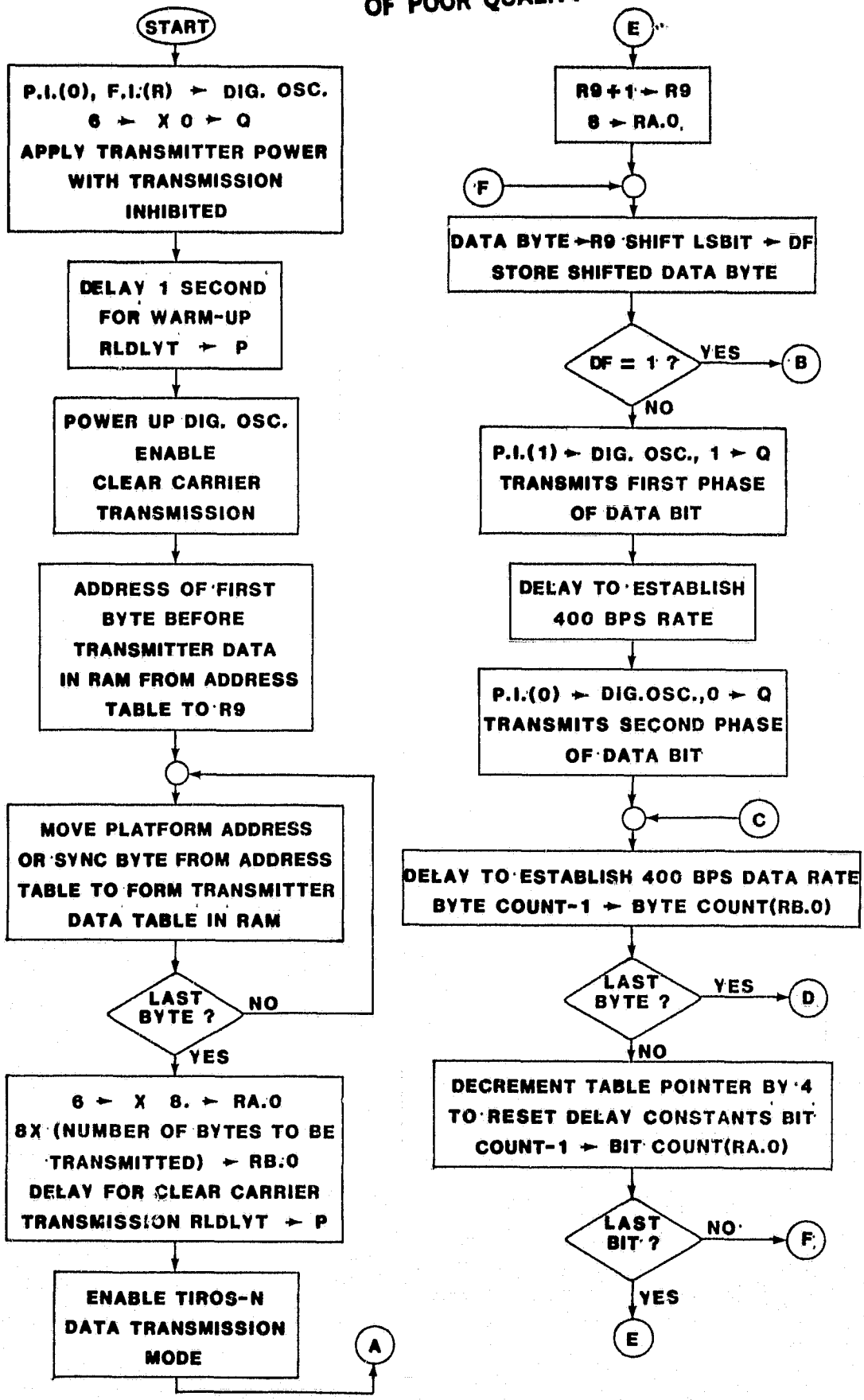

Figure 6.3.2.2. A Flow Chart for the TIROS-N Transmission Subroutine.

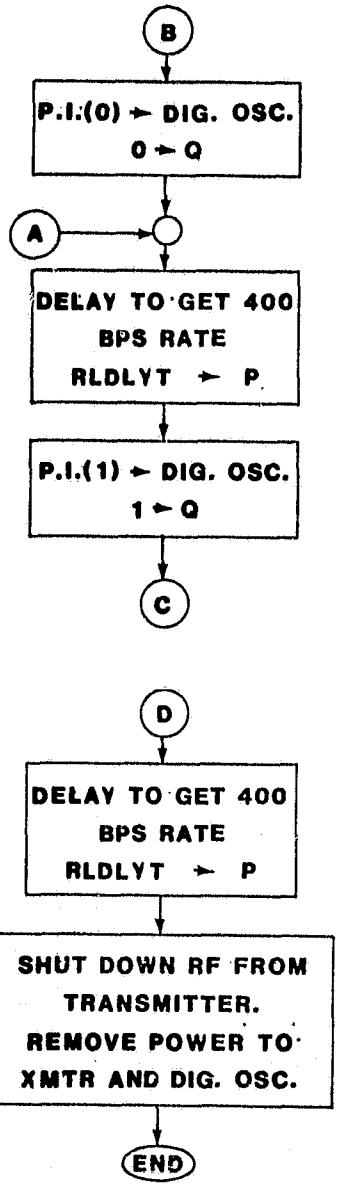

Figure 6.3.2.2. Continued.

Table 6.3.2.3.

GOES Data Transmission Sequence Specifications

Transmission Interval:	Selectable up to 24.75 hours in 0.25 hour increments
Transmission Length:	5 to 25 seconds (approximately)
Transmission Rate:	100 bits per second
Coding:	Preamble - Manchester encoded with a 0 → 1 transition representing a 1
	Data and EOT characters - ASCII encoded then Manchester encoded as above
Modulation:	PSK, ± 60°

Transmission Sequence:

1. Transmitter power-up followed by a 1-second warm-up delay
2. Clear carrier transmission for a minimum of 5 seconds
3. Preamble transmission
   a. Bit synchronization clock (250 bits minimum)
   b. Frame synchronization code (1ØØØ1ØØ11Ø1Ø111) (15 bits)
   c. Address code (assigned to user) (31 bits)
4. Data transmission (up to 2000 bits)
5. EOT code transmission - three ASCII end-of-transmission characters (33 bits)
6. Transmitter power-down

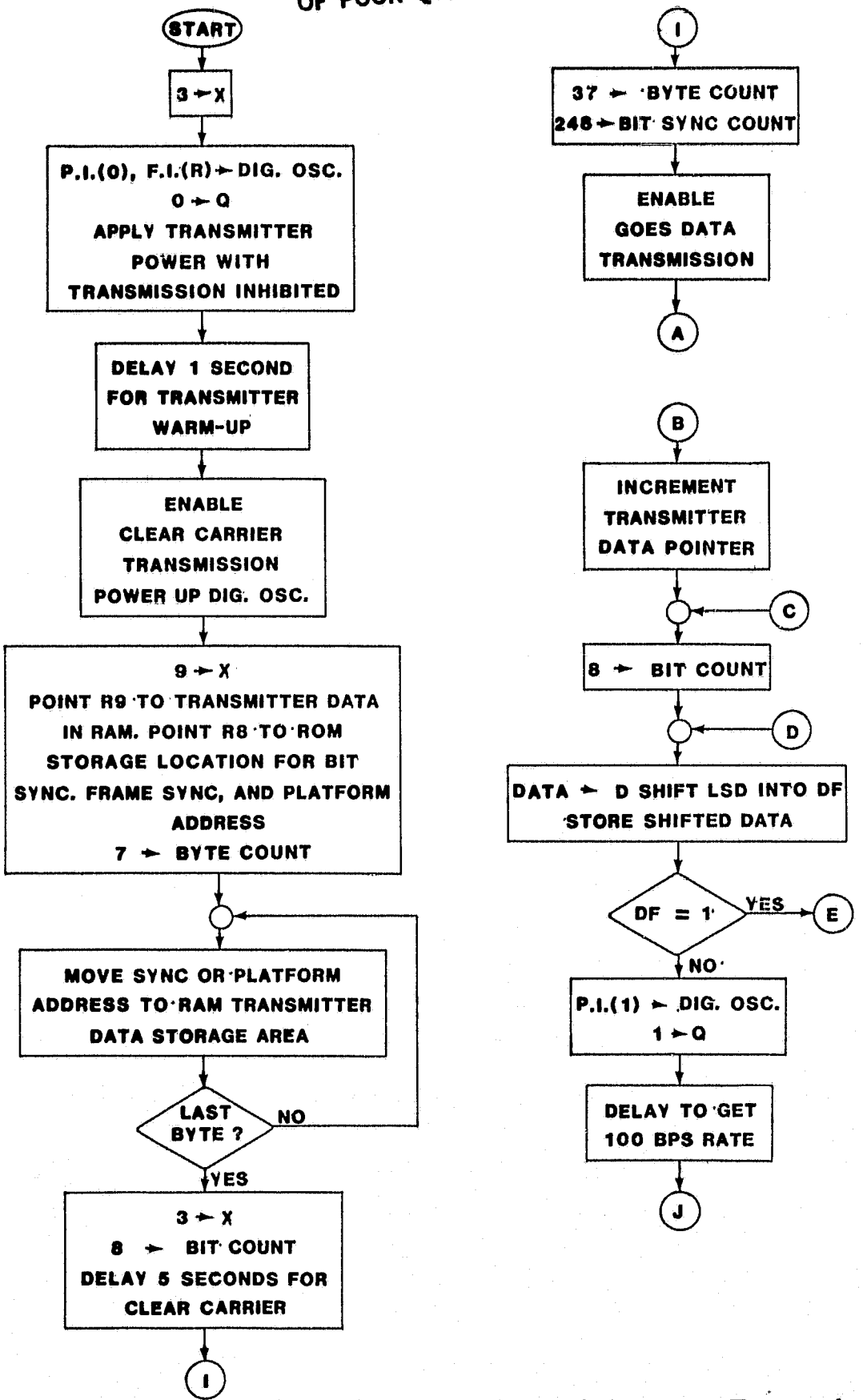

Figure 6.3.2.3. A Flow Chart for the GOES Data Transmission Subroutine.

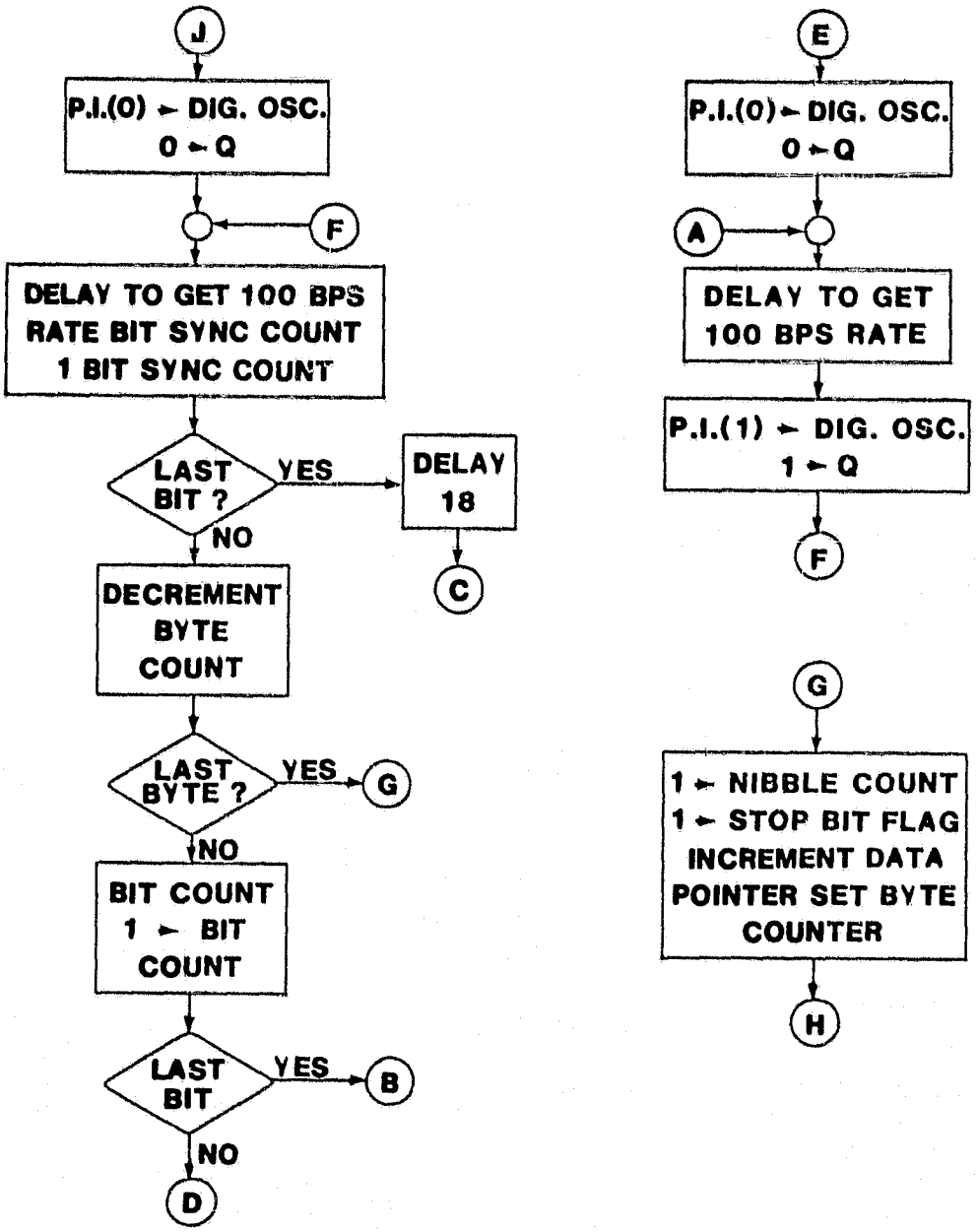

Figure 6.3.2.3. Continued.

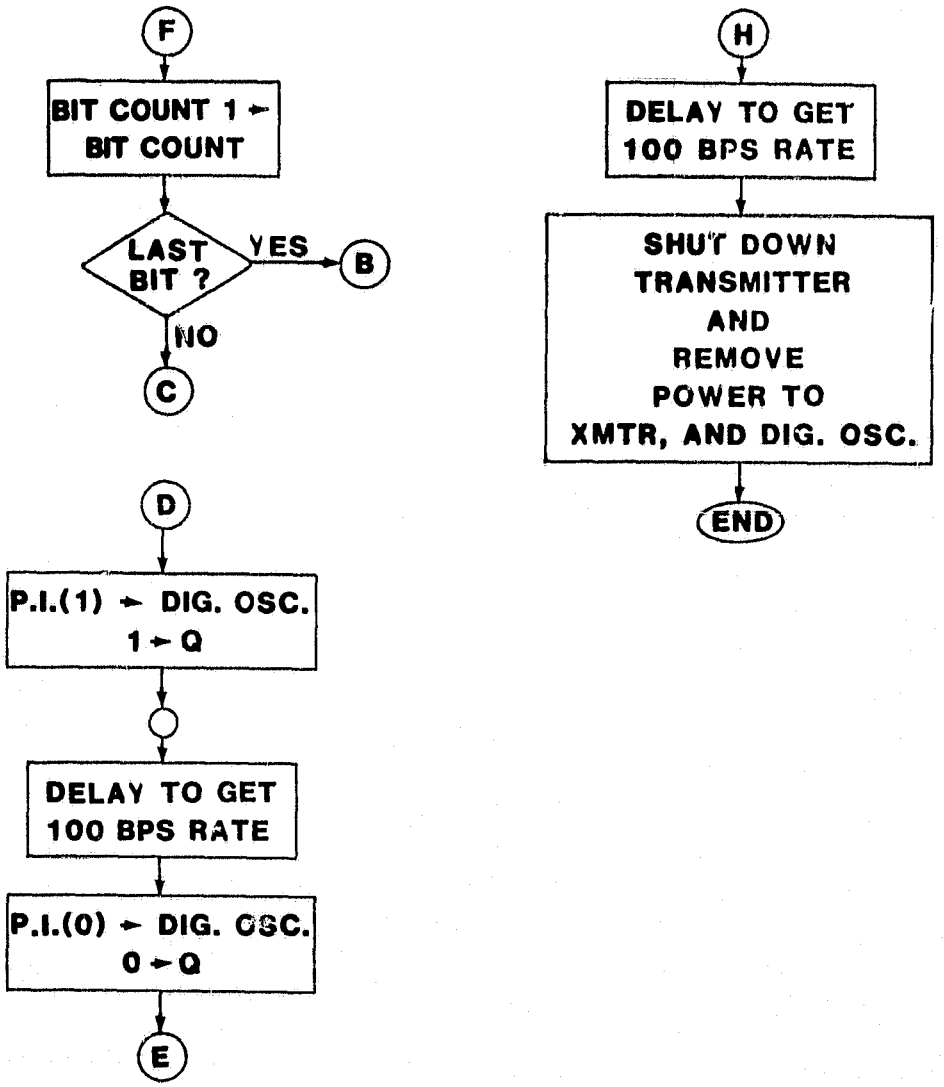

Figure 6.3.2.3. Continued.

6.3.3. WWV FREQUENCY-CORRECTION SOFTWARE

The software directing the WWV-based frequency-correction routines is contained in a program module within μP_1 memory. Periodically the μP_0 Event Timing/Selection routine will call the WWV Frequency-Correction program to "tweak in" the RF system oscillators using the highly accurate 10.00MHz WWV carrier frequency as a reference. Normally the routine will be invoked following data-acquisition activity but prior to a scheduled transmission to the chosen satellite. Thus the RF frequencies will be very close to their intended values, since the drift during the short interval between correction and transmission will be quite small.

The frequency-correction process begins by recalibrating the 3.2MHz microprocessor system oscillator using the WWV standard. This is accomplished by first clocking the digital oscillator with the recovered 10.00MHz carrier frequency from the WWV signal. The digital oscillator clock mux is gated on for exactly 400,000 μP machine cycles and the latched 16-bit result retrieved and held by a pair of 1852 chips configured as input ports. The 16-bit number is double-precision subtracted from a constant which represents zero frequency-error for the 3.2MHz clock, assuming the preset F.I. is used to load the digital oscillator input registers. The remainder of the 16-bit subtraction is adjusted via a normalizing constant which accounts for the approximate voltage-versus-frequency characteristics of the varactor-oscillator circuit. The resultant 16-bit word is transferred to the D/A converter to complete the correction loop. If very high accuracy is required (as in the PDCP case) or if the voltage-versus-frequency control characteristic of the oscillator is nonlinear or drift-prone (as could occur with an inexpensive oscillator),

the loop is repeated as often as necessary to provide the desired degree of accuracy. The 3.2MHz correction routine has an inherent negative response (i.e., if there is a positive frequency deviation, the numerical result from the digital oscillator divider scheme will be less than the ideal value), whereas the 9.82 and 9.046MHz correction routines exhibit positive responses. In all cases the software thus must account for the polarity of the correction to ensure stable operation. Figure 6.3.3 provides a functional flow diagram of the frequency-correction software. The routine is configured so that if for some reason an oscillator frequency cannot be corrected to within the desired tolerance within a fixed number of loops, the PDCP/UM system will inhibit transmission to ensure that no off-frequency operation occurs.

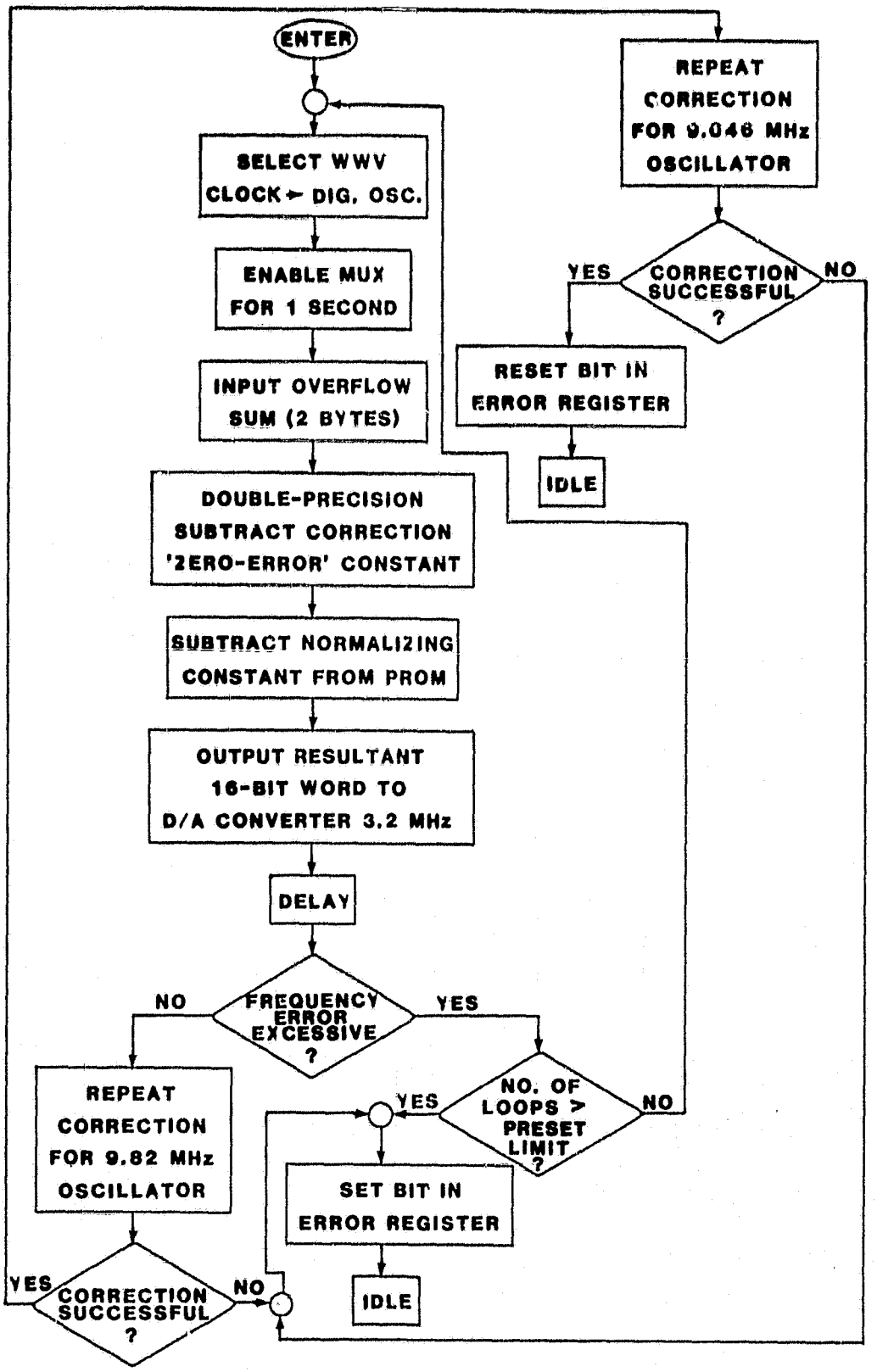

Figure 6.3.3. Flow Diagram for WWV Frequency-Correction Software.

REFERENCES

1. Programmable Data Collection Platform System, Phase II. University of Tennessee, NASA Contract NAS5-22495, May, 1978, pp. 25-81.

2. Bartlett, George W., Ed., NAB Engineering Handbook, 6th Edition. National Association of Broadcasters, Washington, D.C., 1975, pp. 110-115.

3. RCA Solid State Division, User Manual for the CDP1802 COSMAC Microprocessor. RCA Corporation, Somerville, New Jersey, 1977, p. 13.

4. Programmable Data Collection Platform System, Phase II. University of Tennessee, NASA Contract NAS5-22495, May, 1978, pp. 43-53.

5. op. cit., pp. 53-72.

7. FUTURE DCP TECHNIQUES

7.1 DCP DESIGN TRENDS

From the inception of the satellite data collection service in 1967, the basic DCP has been implemented as a stand-alone device capable of transmitting to one specific satellite. The early units were implemented exclusively with discrete logic chips to handle the digital data processing and a fixed crystal-controlled oscillator to serve as both the master clock and as the principal RF frequency source. The RF stages were wholly comprised of discrete transistor amplifiers and were all fixed-tuned to the frequencies dictated by the satellite being serviced.

Early DCPs such as those used with the ATS-1, Nimbus-3, and the later GOES satellites employed ordered transmissions, in which either an RF command signal receiver or an internal clock provided a positive time reference for initating the RF transmitting function. Although an ordered system allows more efficient time-multiplexing of all extant DCPs on a particular channel than the random-transmission system, the presence of an on-board receiver (as in the earlier types) normally leads to a higher overall DCP cost.[1] On the other hand, units employing an on-board timing reference derived from the master oscillator have exhibited in field use sufficient long-term drift to allow the devices to wander into the time slots of other co-channel DCPs and thereby cause the loss of data from both units. Thus it seems that the receiver-directed platform, although slightly costlier, has an inherent reliability advantage over its internally-referenced counterpart and would thus be preferable in the highly-utilized channels characteristic of future satellite data-collection systems.

The inclusion of the WWV receiving setup into the DCP system de-

scribed in this report allows a substantial improvement over conventional techniques in both the time and frequency stability of the RF transmissions to the satellite. The degree of frequency stability (roughly 0.1ppm), heretofore unattainable in low-power oscillator designs, permits maximum utilization of multiple closely-spaced channel configurations without the fear of significant interference among DCPs on adjacent channels. Furthermore, the use of the WWV time-code signal can provide a temporal reference consistently within better than 15 milliseconds of the NBS standard. This not only allows significantly "tighter" time-division multiplexing of the available channels but also drastically simplifies the initial setup procedure required before placing each DCP system into operation in the field.

The advent of the microprocessor has already had a significant impact on DCP design, allowing substantially enhanced data processing and formatting capabilities while simultaneously permitting reductions in the overall size, weight, and complexity of system hardware. As early as May of 1976, researchers at The University of Tennessee demonstrated the viability of a programmable data collection platform and developed a complete sample package of data formatting, data reduction, and transmitter control routines suitable for DCP use, using the Intel 8080A microprocessor.[2] Subsequent work (1977-78) on Contract NAS5-22495 produced a programmable DCP unit based on the ultra-low-power CMOS 1802 microprocessor first manufactured by RCA.[3] About the same point in time (1976), Lebarge, Inc. of Tulsa, Oklahoma introduced the Convertible Data Collection Platform (CDCP) which could by simple hardware changes be configured to transmit either to the Landsat satellite or (on a single specified channel) to the GOES system. The Lebarge unit was significant in that it utilized along with standard digital hardware a single Intel 4040 4-bit NMOS microprocessor to handle much of the data

manipulation tasks.[4] More recently, the University of Tennessee development work employing the 1802 microprocessor has been incorporated into a new PDCP design marketed by Handar Corporation of California.

Future DCP designs must have enhanced price/performance characteristics in order to encourage growth in both the number and the types of end users participating in the satellite data collection program, particularly in an inflationary economic situation. The spectral efficiency of DCP RF transmissions must be optimized while simultaneously reducing hardware costs for both transmitting systems and antennas. Competition among DCP hardware/software vendors should be strongly encouraged and end-user demand stimulated to enlarge the overall DCP market. New technologies such as CMOS microcomputers, low-power, high-speed logic chips, and novel packaging techniques must be fully exploited to provide the necessary advances in DCP state-of-the-art implementations. Future DCP designs must address a wide range of system hardware and software requirements which the end-users (as consumers) will place on them, primarily directed toward ease and simplicity of platform programming, setup, and operation.

The following list provides the salient features and incentives for the characteristics of an ideal (for the end-user) DCP system.

(1) Tight operating frequency and timing tolerances. The DCP must remain precisely on its assigned transmitting channel(s) and must transmit within its designated time slot to avoid interference to other DCPs. These parameters must not drift with temperature or time.

(2) Extremely low power consumption. The DCP should draw as little power as possible, both in transmitting and standby modes. The unit should be capable of greater than a year's operation without replacing batteries.

A secondary benefit of low power drain is the reduced initial cost of batteries (or other power sources) due to the lighter load requirements.

(3) High inherent reliability. The DCP, since it is frequently located at a remote site, should have a large MTBF for its component parts. To this end, the design should be as conservative as possible, consistent with reasonable cost. Reliability should be maintained over wide ambient temperature/humidity excursions and repeated thermal cycling.

(4) Modular design. The basic DCP should be easily customized to meet specific user requirements. A multicard, bus-oriented structure should be employed to facilitate the addition of special-purpose data-acquisition, memory, or processor boards to accomodate user needs, yet provide a minimal-cost system for small DCP implementations. The modular design should also enhance maintenance of the system.

(5) Software control of data processing and transmitting functions. To provide flexibility in application and nonobsolescence when new satellites are launched, all operating DCP functions should be defined by microcomputer programs stored in ROMs or EPROMs. The user can then change DCP tasks, channels, and times by merely inserting a new chip. Diagnostic programs may also be executed via EPROM to facilitate DCP maintenance.

(6) Power control/management software. To accomplish low overall power consumption, the DCP should be programmed to power-down all subsystems not in active use. Additionally, power-control software should monitor battery conditions and if desired provide the capability to handle an auxiliary power source.

(7) Effective power sources. The DCP system should include the capability of operating from batteries, solar cells, thermoelectric generators, or any other cost-effective energy source. The user should be

provided with adequate support and documentation to simplify the selection and setup of an effective, reliable source for DCP power.

(8) User software support. The end-user should have at his disposal an extensive library of software data processing, acquisition, and transmission routines, all available in ROMs or EPROMs. In addition, cross-assemblers or interpreters should be provided to allow users to translate routines in BASIC, FORTRAN, or programmable-calculator codes to DCP instructions. Special DCP-oriented MACROs would also be desirable, as would detailed simulator programs for use on larger computer systems.

(9) Easy DCP field setup/maintenance. All DCP-related hardware should be designed to simplify installation. This includes antenna structures, mounting pedestals, and interconnecting assemblies. As previously mentioned, the DCP should be modular and allow the execution of diagnostic programs to enhance the maintenance/troubleshooting tasks. The need for initial system frequency or time setup should be eliminated via internal software routines.

(10) Multitasking/multiuser capabilities. The DCP software should permit multiple data collection/transmission tasks to be performed on a timesharing basis. Provision should also be made for execution of special emergency transmissions upon detection of dangerous conditions by DCP sensors. Multiuser implementations should be facilitated by program memory partitioning; this would allow one user to reprogram his DCP tasks independently of other users of the same platform.

(11) Applications programming and engineering assistance. The user should be fully supported by the vendor to enable specialized DCP tasks to be successfully defined and implemented. This should encourage the development of novel uses for the DCP/satellite link.

(12) Secure data communications capability. Special coding and/or encryption for confidential user data should be enabled by add-on software and/or hardware packages from the vendor. This capability should enhance the use of DCPs by military and law-enforcement agencies.

(13) Low cost. Perhaps the single most important DCP parameter to the end-user is the cost of the system. The cost of a complete DCP package must be low enough to allow colleges, municipalities, private firms, and tightly-budgeted state and federal government agencies to acquire large numbers of the units to support their activities. This is perhaps the single most important factor in determining the success of the DCP/satellite data-collection service.

7.2 TECHNOLOGICAL TRENDS IN DCP DESIGN

To meet the requirements of future DCP users, the semiconductor industry must provide devices capable of higher performance with lower power consumption and lower prices. Newer technologies are emerging which are yielding significantly improved speed-versus-power products for both digital and analog circuits.

7.2.1. Digital Integrated Circuit Technology

The maturing of the bipolar TTL process has led in the past two years to three new digital logic forms: the Texas Instruments AS (Advanced Schottky) and ALS (Advanced Low-power Schottky) and the Fairchild FAST (Fairchild Advanced Shottky Technology) series. Figure 7.2.1 shows the relationships between these state-of-the-art forms and the established TTL, STTL, and LSTTL processes. [5] A dramatic improvement in the speed-power characteristics can be obtained in these new series of pin-compatible devices. A substantial effort in reducing chip and device geometries

and in dielectric isolation has resulted in faster gates with lower power consumption, decreased parasitic capacitance, and increased logic density in the same standard configurations and packages.

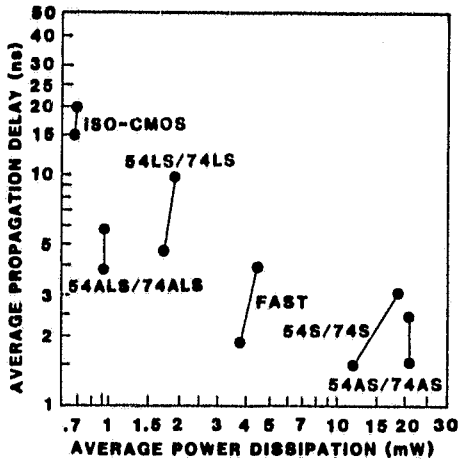

Figure 7.2.1. Comparison of Digital IC Technologies.

Another contender in the field of medium-speed, low-power logic is the new ISO-CMOS technology currently being developed by Mitel Semiconductor of Canada. Although these devices are not as fast as TTL or LSTTL, they are surprisingly close (typically 15 ns delay versus 10 ns per gate) and have markedly smaller dissipation figures.

For moderate-speed versions ($f_{CLK} \approx$ 3MHz) of the digital oscillator, these devices will probably be the optimum choice since in addition to their speed-power capabilities they can operate over a wide -40° C to +85°C temperature range with plastic packages and the full military range (-55°C to +125°C) in ceramic. Already octal latches are available; within a year or two the adders should be out. These devices could allow significant operational advantages in future DCP digital oscillator implementations.

7.2.2. Microcomputer Component Technology

New CMOS processes to produce microprocessors, RAMs, ROMs, EPROMs, and even EEPROMs and one-chip microcomputers are rapidly being developed and marketed by various semiconductor manufacturers to meet the ever-increasing demand for high-performance, low-power microcomputer systems. New SOS/CMOS (RCA), P^2CMOS (National) and SELOX-C (Intersil) processes are permitting a wide variety of CMOS devices to be produced.

The 1800 series, originally produced by RCA (and now second-sourced by Hughes and Solid State Scientific), includes the lowest-power microprocessors available and the widest range of CMOS support devices. The time-tested 1802, which was the first one-chip 8-bit CMOS microprocessor, can with a 5-volt supply operate with typically 6mW dissipation at a clock frequency of 3.2MHz; it sells for about eight dollars in lots of 100. Its bigger brother, the 1804, is a one-chip 8-bit microcomputer with onboard 2Kx8 ROM, 64x8 RAM, clock logic, and an 8-bit presettable, prescalable down-counter/timer. The SOS/CMOS device has a much larger (upward-compatible) instruction set than the 1802 plus hardware subroutine execution and yet requires only 8mW for the entire μC chip. Besides the standard PIA and UART devices, ROMs, RAMs, and EPROMs, the 1800 series includes a high-speed hardware multiply-divide unit, the 1855. This chip drastically enhances the number-crunching capabilities of the 1802 and 1804 and may thus overcome the greatest single shortcoming of the μPs. Interestingly, up to four 1855s may be cascaded to provide for operands up to 32 bits wide; the possibilities for FFT units and the like are intriguing, particularly since the 1855 can multiply or divide in 5μs with only 10mW power drain from a 5-volt supply.

National Semiconductor has fielded a major entry into the CMOS microprocessor race with the NSC800, a CMOS version of the popular and powerful

Z-80 device. The NSC800 dissipates about one-tenth as much as the NMOS Z-80A (50mW versus 500mW), yet operates at the same speed (4MHz) and executes the same instruction set. For high-level languages and complex programs this device is undoubtedly the most powerful CMOS device currently available; a family of sophisticated support chips is also forthcoming. Perhaps the only drawback to the use of the NSC800 in DCP applications is the 50mW power consumption, which is still an order of magnitude higher than that of the 1802.

Intersil, Inc. has developed a wide variety of CMOS devices, both analog and digital. Its microprocessor components include: the 6100, a 12-bit CPU which dissipates only 10mW and which executes the well-known PDP-8E instruction set; support devices for the 6100, including ROM, RAM, and I/O; the 80C49 and 87C48 CMOS versions of the popular Intel 8049 and 8748 one-chip 8-bit microcomputers; several types of CMOS RAMs, from 256x1 bits to 4Kx1 bits; 4K bit CMOS EPROMs, the 6653 (1024x4) and the 6654 (512x8); and CMOS ROMs ranging in size from 1024x12 bits (the 6312) to 8192x8 (the 6364). All these devices are low power; the microcomputers require about 50mW, while the memory devices consume typically 10mW in operation and less than 500μW in standby.

At this writing, close to two dozen other different CMOS μPs and μCs are being offered by manufacturers such as National, Texas Instruments, Motorola, NEC, Panasonic, Toshiba, Fujitsu, OKI, and Hitachi, although all but five of these (the Motorola MC146805, the NEC μCOM-87LC and μPD80c48, and the Hitachi HD6301 and HD6305) are 4-bit units. CMOS versions of the popular NMOS 8049 and 8051 devices are being developed by Intel; Mitel Semiconductor is currently preparing a CMOS 6802. In addition, Hewlett-Packard has for several years manufactured the MC2, a 16-bit CMOS/SOS

unit, but the device itself has not been marketed commercially; two Japanese firms have exhibited their own 16-bit CMOS units, but as of yet none have been available for sale. Obviously, a wealth of modern low-power microprocessor products is rapidly becoming available for DCP designs. Undoubtedly, the computing power of future DCPs will be drastically increased over current designs and will assist in reducing the amount of information required to be sent through the satellite as more sophisticated data preprocessing is utilized prior to final encoding for RF transmission. This fact will in turn allow more total data to be sent through the same satellite link and will thus facilitate more intensive use of the data-collection service by a greater number of DCPs.

7.2.3. Proposed DCP Simplifications

In the next few years, the satellite data-collection service should experience several operational changes to enhance the quality and simultaneously reduce the cost of acquiring remote data. As previously mentioned, new DCPs will be able to perform far more data-handling tasks yet should cost less than current designs. It is also foreseen that to minimize RF spectral bandwidth requirements there will be a gradual but steady conversion to the use of MSK modulation for all DCP transmissions. The application of MSK in preference to FSK or PSK, plus the enhanced RF frequency accuracy of modern DCP transmitters, should permit the full utilization of the tightly-spaced GOES channels and a simultaneous reduction in channel-to-channel crosstalk and carrier frequency drift problems. The scheduled phase-out of the use of LANDSAT should also simplify the hardware requirements of a universal modulator in implementing all the necessary modulation formats required for DCP transmissions, since the high data

rate and FSK deviation (5kHz) demanded by LANDSAT is at odds with the high-resolution requirements of the more modern GOES system. In addition, the low bit rates (100 or 400 Hz bipolar) used by GOES, TIROS-N, and NIMBUS-F permit substantially more real-time data preprocessing and formatting than with LANDSAT and can thus allow a reduction in DCP microcomputer RAM size requirements.

In order to simplify the digital oscillator hardware requirements and minimize the multiplication of quantization phase noise produced by the digitally-implemented universal modulator scheme, a frequency multiplication factor of no greater than eight should be used in the RF transmitting amplifier chain. A factor of eight can be easily generated by three cascaded frequency-doubler stages or by the state-of-the-art snap-diode unit, and a corresponding local heterodyning oscillator frequency selected which will permit the digital oscillator to produce the desired RF frequencies using the microprocessor clock frequency instead of a separate high-accuracy crystal oscillator. The impact of this change is substantial: not only is the original 9.82MHz digital oscillator clock source eliminated, but also the 10.24MHz phase-locked oscillator and its related digital dividers and phase detector. Additionally, since by using the 1802 master clock frequency the digital oscillator is inherently synchronized to the µP transitions, MSK or PSK may be generated from the single digital oscillator clock frequency. Furthermore, the WWV-based frequency correction scheme is simplified by the elimination of one of the three D/A converter-varactor circuits on the DCP RF board. The block diagram of the simplified digital oscilator system is shown in Fig. 7.2.3.

The microprocessor, an 1802, provides the Frequency Index (F.I.) and Phase Index (P.I.) data to the three 1852 I/O ports. Since the F.I. is

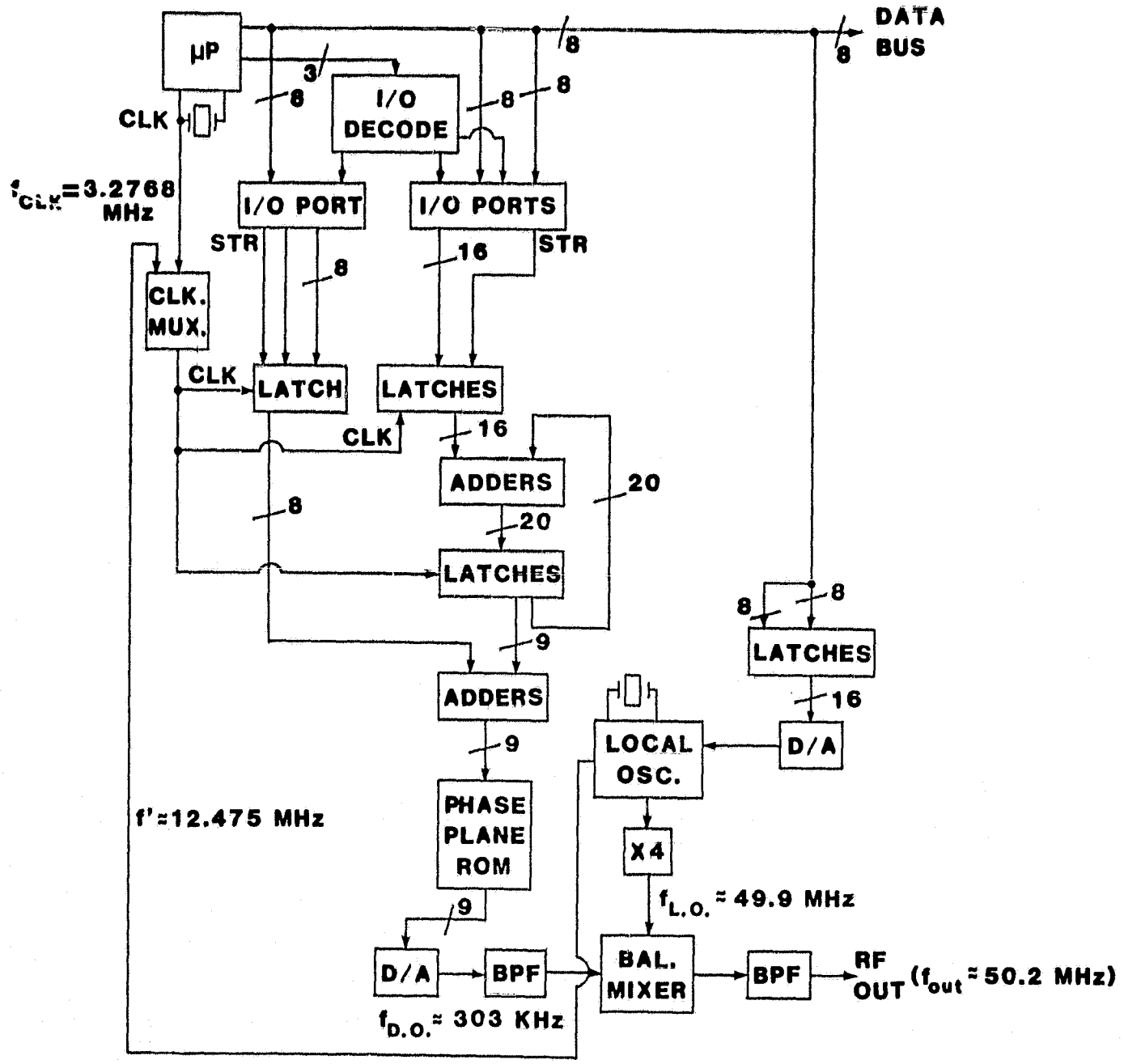

Figure 7.2.3. Simplified Digital Oscillator System Block Diagram.

16-bits, the 1852s must be double-buffered by a pair of 8-bit latches to allow the sequential loading of the two F.I. bytes by the μP. Similarly, the 1852 containing the P.I. data byte is buffered by another 8-bit latch. All three latches are synchronized by the digital oscillator clock to provide glitch-free RF output signal generation and strobed by the respective I/O port service-request lines which signal the arrival of a new P.I. or F.I. data byte. The F.I. latches output their 16-bit data to a 20-bit-wide adder, whose other input data is the final latch output word. The nine high-order bits from the digital oscillator latch are added to the P.I. byte in the second (phase) adder block; the sum is sent to the address inputs on the phase plane ROM array. The output data from the ROM is converted by the D/A to a stepwise sinusoidal signal whose frequency is of the order of 303kHz. The subsequent bandpass filter removes the harmonic and subharmonic energy, leaving a nearby pure sinusoid, which is heterodyned in the balanced mixer with the local oscillator system output at roughly 49.9MHz. The resultant 50.2MHz RF output is then introduced to another bandpass filter (to remove the difference-frequency component at 49.6MHz); the filtered output drives the X8 multiplier chain to produce the final DCP RF carrier output frequency in the neighborhood of 401.6MHz. The 3.2768MHz clock frequency still yields an integral number of μP states for each state of the biphase data stream and actually permits a slight increase in the frequency-correction resolution offered by the WWV frequency-referencing scheme. Eliminating the need for LANDSAT compatibility thus permits this cost-effective digital oscillator configuration to be exploited in future DCP designs. Furthermore, if it is assumed that MSK transmissions replace ±60° PSK as the standard on the GOES, TIROS-N, NIMBUS-F, and later data-collection-oriented satellite systems, the P.I. port, latch,

and adder may be eliminated from the circuit of Figure 7.2.3. The resultant system could be implemented with as few as 15 SSI/MSI chips (including the local oscillator and frequency-correction components) and a few discrete RF transistors. The F.I. values and RF output frequency errors for the latter configuration are presented in Table 7.2.3.

Table 7.2.3 Parameters for Simplified Digital Oscillators (MSK Mode)

f_{CLK} = 3.276800MHz

$f_{L.O.}$ = 49.90930625MHz

N = 20

Multiplication Factor = 8

Δf_c (Carrier-frequency step size) = 25Hz

Frequency Index	ΔF.I.	f_0(MHz)	Dev.(Hz)	Satellite/ch.	f_cError(Hz)
97,060	±2	0.3033125	±50	GOES#1	-46
100,000	±2	0.3125000	±50	GOES#50	0
102,940	±2	0.32168750	±50	GOES#99	+45
77,022	±2	0.24069375	±50	NIMBUS-F	0
95,022	±8	0.29694375	±200	TIROS-N	0

The minimum step size at the final RF carrier frequency is 25Hz, assuming a frequency multiplication factor of eight following the balanced mixer. For MSK, with a modulation index of 0.25, the required frequency deviation at 401MHz is ±50Hz about carrier for GOES and NIMBUS-F and ±200Hz for the TIROS-N satellite. The clock frequency and 20-bit accumulator width permit MSK to be generated for effective bit rates (before biphasing) down

to 50Hz. The output RF carrier center frequency errors are also enumerated: the TIROS-N, NIMBUS-F, and GOES channel #50 frequencies are nominally exact; the GOES channels other than #50 are off by 1Hz per channel number difference from 50, since the 3.276800MHz clock forces the GOES channel spacing to be precisely 1500Hz, whereas the actual spacing is closer to 1499Hz. The worst-case error in any event is less than 50Hz due to this situation; this compares favorably with the maximum error figure of ±40Hz due to the uncertainty of ±1 count associated with the WWV-based frequency-correction algorithm. Thus the overall error would be less than ±90Hz on any GOES channel and no worse than ±40Hz on either TIROS-N or NIMBUS-F.

7.2.4 PROPOSED NEW INTEGRATED CIRCUITS FOR DCP USE

7.2.4.1. Digital Oscillator Chip

Although the simplified digital oscillator setup requires only about 15 IC packages (plus a few discrete transistors for the local oscillator doublers), to be truly cost-effective the heart of the system should be housed in a single hybrid or monolithic analog/digital LSI device or, failing that, at least in one digital LSI chip plus a separate RF transistor array for the oscillator system. The following diagram (Fig. 7.2.4.1.) gives a possible block diagram and pin-outs for such a self-contained device, which would consist of separate digital and high-speed analog chips mounted on a hermetically-sealed ceramic substrate. The 40-pin package itself is quite typical of the high-reliability LSI devices currently manufactured.

The nineteen inputs to the digital oscillator frequency-index buffer register are placed on the same side of the I.C. package to simplify circuit board layout. Input #20 is designated to always be zero, so it is grounded internally. Pin #20 is intended to accept a strobe pulse from

ORIGINAL PAGE IS
OF POOR QUALITY

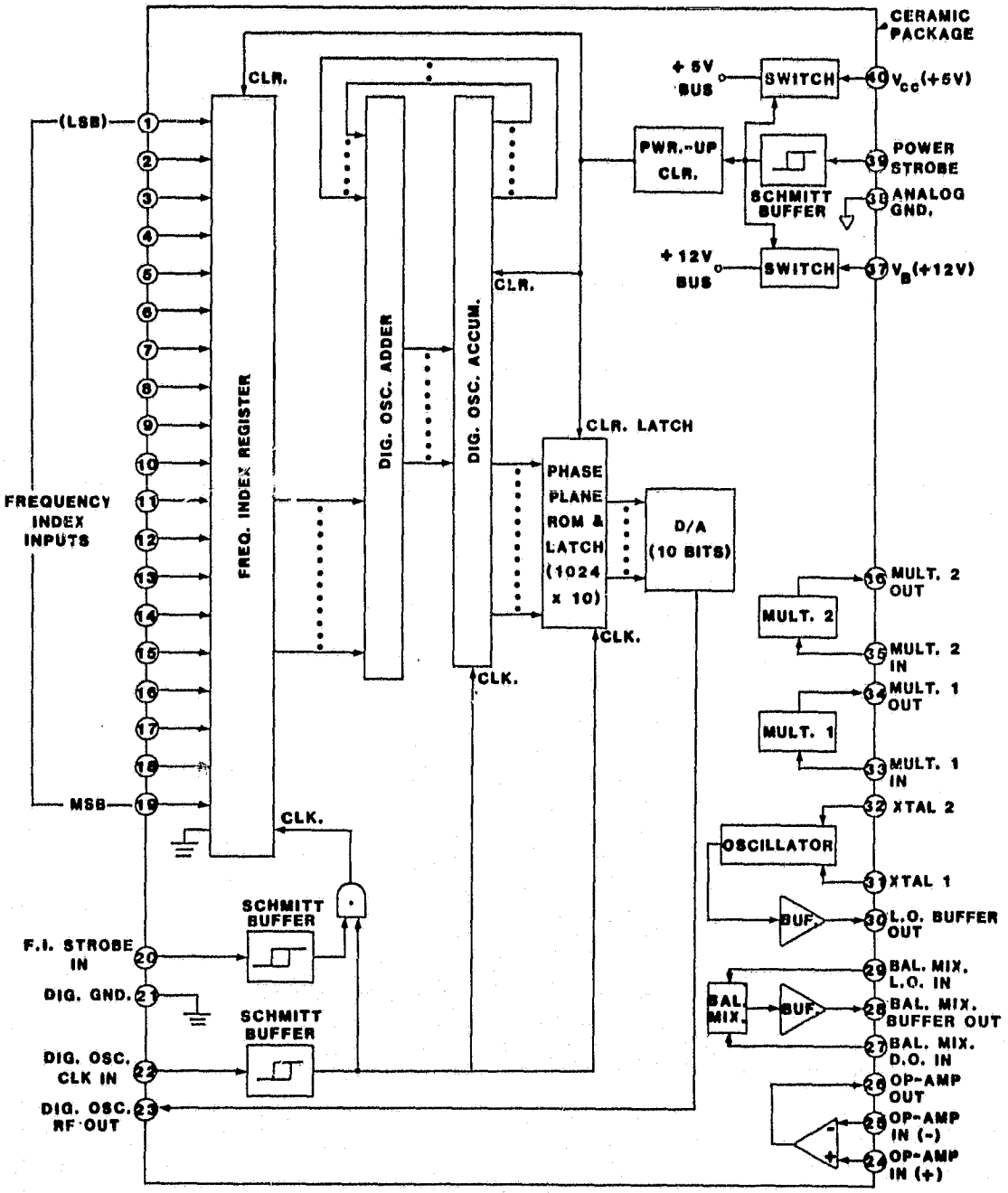

Figure 7.2.4.1. Proposed Digital Oscillator I. C.

the frequency-index data source to indicate that a new F.I. word is ready to be loaded. The loading occurs on the leading edge of the register clock signal, which is the conditioned external strobe ANDed with the digital oscillator clock signal. This feature ensures a synchronous, glitch-free transition of the MSK output signal. The digital oscillator clock also strobes data into the accumulator register and latches data at the output of the phase plane ROM. The 10-bit D/A converter delivers a high-speed current output to pin #23. Pins #24 and #25 are the noninverting and inverting inputs to a wideband, high-speed op-amp such as the LM318 which possesses a high output-drive capability. The monolithic balanced-mixer is configured internally for unbalanced inputs from the digital oscillator system and the local oscillator buffer or multipliers. The output of the mixer is buffered to provide a low source impedance suitable for driving a 50Ω RF load. The RF multipliers are wideband four-quadrant devices wired to perform as low-distortion frequency doublers. In the normal DCP application the two multipliers are cascaded to produce the desired 49.09MHz local oscillator mixing frequency from the crystal oscillator which operates with a fundamental-mode crystal of 12.475MHz. The "Power Strobe" pin provides on/off control of both the +5V digital and +12V analog supply busses and also drives an internal power-up reset circuit which clears all digital registers upon application of the Power Strobe logic signal.

A useful manufacturing approach would be to employ either LS or ALS technology on the digital chip and a high-speed linear process on the analog chip. Standard large-area power transistors could be used as the switch elements; differential pairs with current-source control would be suitable for the RF frequency multiplier/doubler blocks and darlington-type

emitter followers for the RF buffers.

As a whole, the I.C. should dissipate on the order of 1 watt in operation, and no more than a milliwatt or two in the standby (power-down) mode. Interestingly, this I.C. could find application not only in DCPs but in a wide variety of industrial, commercial, military, and government communication systems which feature large numbers of relatively closely-spaced channels and which require accurate, digitally-controlled frequency generation.

7.2.4.2. Proposed Thermally-Stabilized Crystal Oscillator Chip

As originally mentioned in Chapter 2, one means of increasing the precision of the digital oscillator output frequencies in a DCP is to use a high-accuracy, high-stability crystal-controlled oscillator as a frequency source. Obviously, an ovenized unit offers superior accuracy and stability to other oscillator types but consumes far too much power for DCP use. The temperature-compensated crystal oscillator (TCXO) offers good stability with fairly low power dissipation, but it is subject to long-term drifts and crystal aging effects. Although the WWV-based correction scheme is far more effective in reducing temperature-,time-, and voltage-induced frequency errors in crystal-controlled oscillator systems, there are some circumstances where a high-stability isolated TCXO would be advantageous. In auroral regions, near sources of RFI, and during times of intense solar storms the WWV signal at 10MHz may be insufficiently stable to properly synchronize the DCP system TCXOs; in addition, there may be some DCP locations in which it is difficult to erect an effective WWV receiving antenna. In many instances, the WWVB signal at 60kHz (with appropriately longer frequency averaging intervals) would provide satisfactory operation,

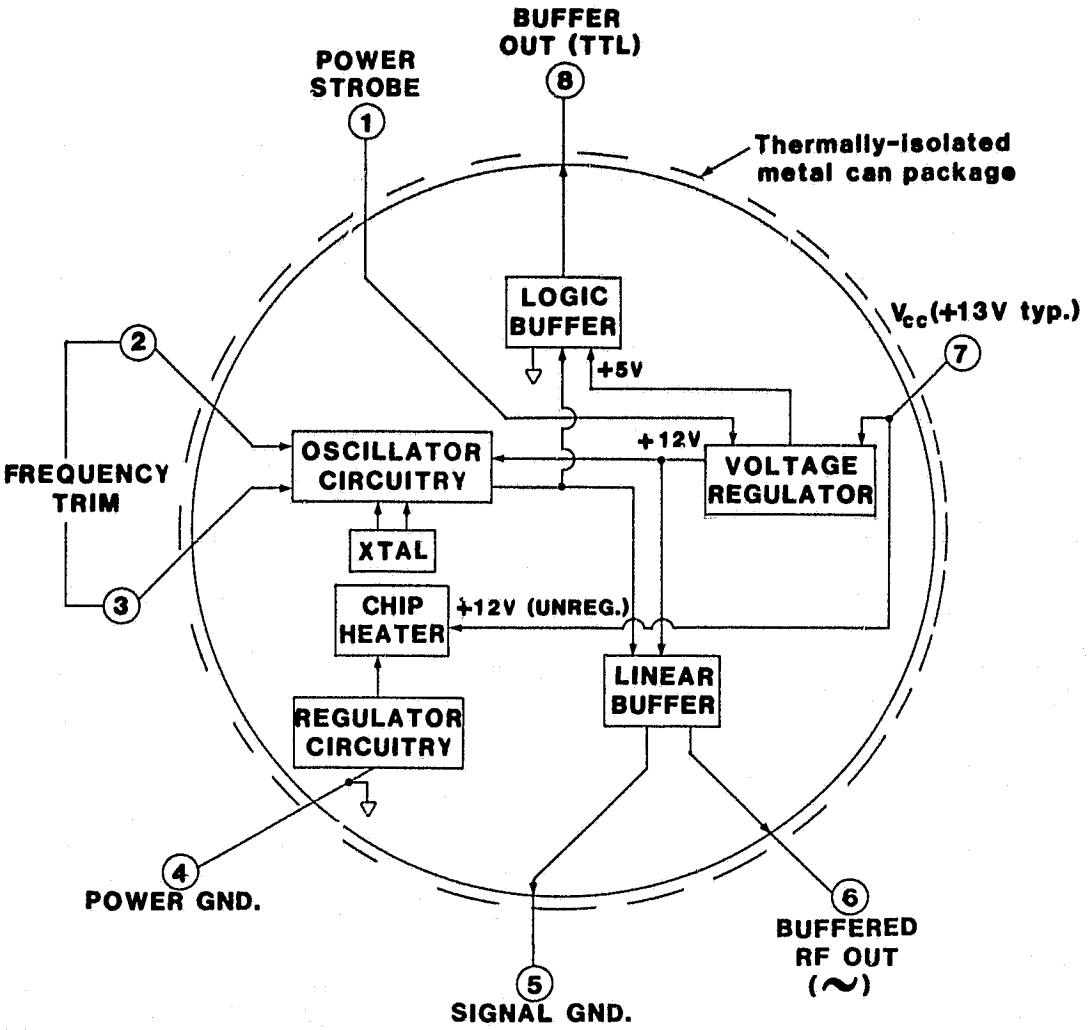

Figure 7.2.4.2.1. Block Diagram of Proposed Crystal Oscillator Chip.

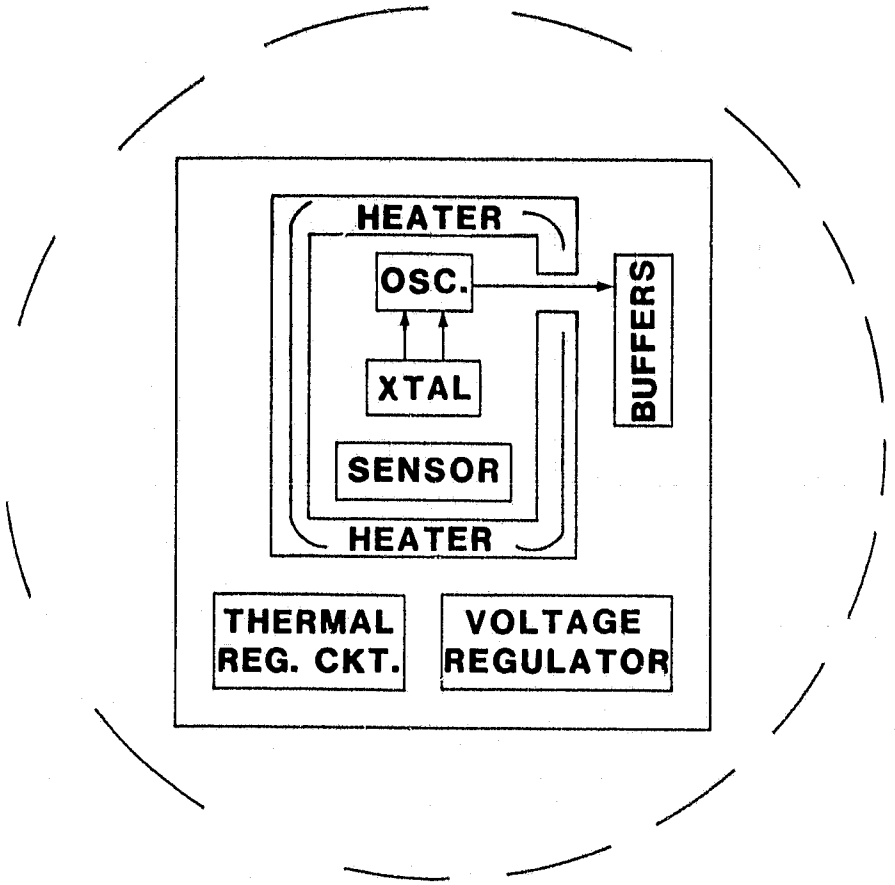

Figure 7.2.4.2.2. General Physical Layout of Proposed Chip.

but there will probably still exist a need for a highly-stable stand-alone TCXO which has low power consumption. In response to this, a new temperature-controlled crystal oscillator I.C. is proposed which should provide oven-type stability but at much lower power. The monolithically-fabricated device would consist of an on-chip crystal (or possibly a discrete crystal mounted against the chip), an appropriate low-power transistor oscillator circuit with integral temperature compensation, a buffer capable of linear or digital (TTL-level) outputs into a 50Ω load, and an integrated chip temperature-control circuit; it would be mounted in a hermetically-sealed, thermally-insulated package similar to that employed by National Semiconductor for the LM199 series voltage-reference devices.

By keeping chip geometries small a die of minimum size could be utilized, thereby keeping the required heater current low. Advanced processing techniques such as ion implantation and dielectric isolation would allow higher speed without the normal penalties in power consumption. Since the heater power is the dominant dissipation mechanism, careful thermal design should be able to produce a unit compatible with DCP system energy requirement. Figure 7.2.4.2.1. gives a block diagram of the proposed chip.

Physically, the heater, sensor, crystal, and oscillator circuitry are in very close proximity to each other to keep thermal gradients between these parts to an absolute minimum. In addition, to avoid thermal disturbances due to changes in buffer power output levels, the layout of Figure 7.2.4.2.2. is suggested.

All the analog circuit blocks and the logic buffer would be configured for minimum quiescent current drain; the "power strobe" input (pin #1) would permit the chip to be shut down during longer intervals between DCP transmissions to conserve power. Eventually the device would be turned on 30 to 60 seconds before it is actually needed to allow the temperature-control system to get the chip back up to operating temperature. The on-board voltage regulator would serve to reduce long-term errors due to gradual declines in DCP battery voltage due to aging or insufficient charge.

7.3 PROJECTIONS ON DCP DESIGNS AND USES FORECASTS

7.3.1. SEMICONDUCTOR TECHNOLOGY

The semiconductor technology will have a profound influence on the character of DCP units. The types of technology available are the dominant factors in determining the speed and energy requirements for the DCP electronics, both digital and analog. With bulk-CMOS and SOS/CMOS currently in the foreground for the implementation of low-power microprocessors and memory systems, it is not anticipated that by 1985 these processes will be displaced; indeed, both should evolve (especially SOS/CMOS) to provide at least twice the speed for the same dissipation level. Thus it is anticipated that for the majority of DCP tasks a one-chip CMOS microcomputer with onboard RAM, ROM/EPROM, and I/O with perhaps some external memory will be adequate. Another very desirable development will involve CMOS-LSI computational chips, which will be able to multiply, divide, average, extract square roots, and provide exponentiation, logarithms, integration, and trig functions. Other useful functions could include correlation FFTs, and chirp-Z algorithms, which would have broad application in the

preprocessing of temperature, wind and water velocity, seismic, and similar signals frequently encountered in DCP-based monitoring systems. Table 7.3.1 summarizes the status of most major types of digital semiconductor technologies, both currently and for the 1985-1990 period. The table is based on a survey conducted by the Lockheed Missile Space Center.

Table 7.3.1. Status of Semiconductor Technology

Period	Current			Future (1985-1990)	
Criteria	NMOS	Bulk CMOS	SOS/CMOS	SOS	GaAs
Relative Process Maturity (1980)	9	8	4	2	1
Packing Density (gates/mm^2)	100 to 200	40 to 90	100 to 200	200 to 500	300 to 1000
Propagation Delay (typical) (nS)	15	20	10	0.3	0.07
Speed-Power Product (pJ)	5 to 50	2 to 40	0.5 to 30	0.1 to 0.2	0.01 to 0.1

Obviously, GaAs will probably be the leading technology of the late 1980's. Already Rockwell Electronics Research Center in California has designed, fabricated, and fully tested a dozen different types of GaAs digital function chips containing up to 96 gates per chip, including a digital FM demodulator circuit; an 8x8 parallel multiplier with 1000 gates is presently in the works. Rockwell scientists project that by 1984 circuits with complexities approaching 10,000 gates will be feasible - on a chip just 200 mils on a side. This is compared with current μP chips, which have about 10,000

gates on a chip 300 mils square.[6] 'A very-high-speed version of the digital oscillator chip could probably be fabricated in GaAs and on the market by the late 1980's; conceivably, a DCP manufactured in that era could contain virtually all of its systems in perhaps seven LSI-type chips: (1) a 16-bit microcomputer, with clock, ROM, RAM, and I/O; (2) a math processor chip; (3) a high-resolution data-acquisition chip with mux and μP-compatible A/D converter; (4) a mass-memory device (perhaps even a bubble chip); (5) the digital oscillator system I.C.; (6) a hybrid TO-3-cased RF amplifier I.C. capable of 5 watts output; and (7) a switching-type power-supply regulator system with perhaps 95% efficiency.

With the support of these chips, the DCPs of the late 1980's will undoubtedly support high-level languages such as FORTRAN, BASIC, FORTH, PASCAL, and ADA and will be able to analyze one to two orders of magnitude more data than can currently-available models. These DCPs will also analyze their own operations and alert the user (through the satellite) to any problems or impending failures.

7.3.2. FUTURE DCP USES

As the inherent "intelligence" of the typical DCP increases, an ever-increasing number of disciplines will find tasks for which the application of a DCP system would be advantageous or even essential. Future DCPs will find use in such diverse fields as: meterology; oceanography; vulcanology; seismology; botany; zoology; traffic control; agricultural R&D; forestry; firefighting; flood control; law enforcement; hydroelectric power management; navigation; air, water, thermal, radiation, and chemical pollution monitoring and law enforcement; military data acquisition and reconnaissance; industrial telemetry; and emergency

locating transmitters (ELTs).

The advanced software capabilities of future DCPs should permit single DCPs to be shared by multiple users, thus enhancing the economic feasibility of employing DCPs for all types of remote (and perhaps not-so-remote) data-acquisition tasks. In addition, DCP software programs could be written to permit split-channel operation of a DCP as well as special functions such as: transmitting emergency data on special channels; transmitting only when data exceeds a preset value; transmitting special strings when abnormal data readings are encountered; and transmitting voice and pictures at sub-real-time rates. Buoy-mounted DCPs could track ocean currents, winds, and water temperatures; balloon-carried units could be utilized in atmospheric scans for jet stream movements, upper-air temperature and humidity profiles, pollutant concentrations, and ultraviolet radiation levels. Geophysical applications include magnetometry-based units to measure variations in the earth's magnetic field, cosmic ray detection, and examination of auroral phenomena.[7] Future DCPs may be powered with batteries, photovoltaic cells, thermoelectric generators, fuel cells, windmills, waterwheels, or geothermal energy, as well as conventional power.

Users should be able to program future DCPs with FORTRAN, BASIC, or other popular languages or download assembly-language routines from microprocessor development systems, time-shared cross-assembler software, or even from pocket calculator output ports with the appropriate adapters. Large numbers of researchers in universities and colleges will for the first time be able to freely utilize DCPs to support a vast array of studies in natural sciences, engineering, and even commerce. Finally, the positive impact of DCPs on society as a whole will be substantially felt as the increased amounts of DCP-acquired data are analyzed and implemented in ways directed toward improving the overall quality of life.

REFERENCES

1. Programmable Data Collection Platform Study. University of Tennessee, NASA Contract NAS5-22495, May, 1976, pp. 1-1, 1-2.

2. op. cit., pp. 3-1 through 6-17.

3. Programmable Data Collection Platform System, Phase II. University of Tennessee, NASA Contract NAS5-22495, May, 1978.

4. Instruction Manual for the Convertible Data Collection Platform (CDCP) and Related Equipment. LaBarge, Incorporated, Tulsa, Oklahoma, 1976, pp. 5-1 through 5-3.

5. Mendelsohn, A., "Second Generation Enhances TTL Logic," Electronic Products 23, October, 1980, pp. 31-36.

6. Bursky, D., "Memory and μP IC/Pack More, Consume Less", Electronic Design 28, June 7, 1980, pp. 75-87.

7. Wolfe, E.A., Cote, C.E., and Painter, J. E., Satellite Data Collection User Requirements Workshop. NASA-Goddard Space Flight Center, Greenbelt, Maryland, May 21, 1975.