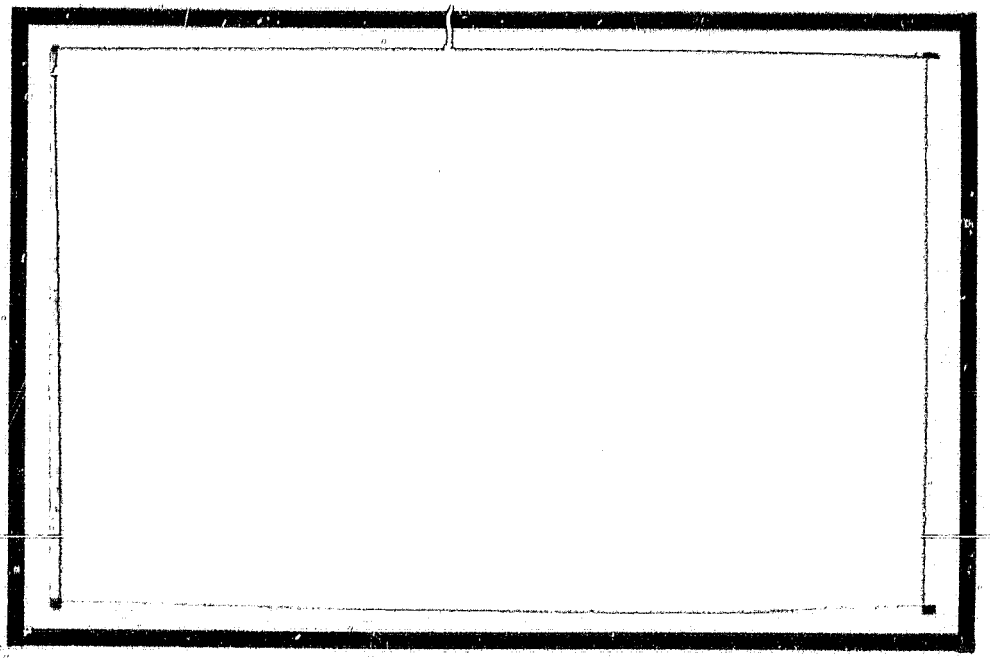

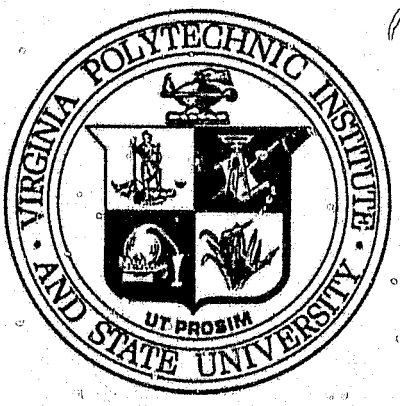

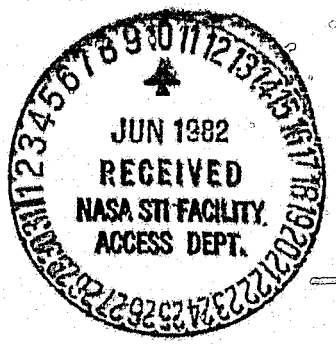

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Final Report

INPUT FILTER COMPENSATION FOR SWITCHING REGULATORS.

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I. INTRODUCTION

An input filter is often required between a switching regulator and its power source. The filter serves to 1) prevent the regulator switching current from being reflected back into the source, and 2) to isolate the source voltage transients so as not to degrade the performance of switching regulators downstream. Thus the filter is required to provide high attenuation at the switching frequency and sufficient damping against line disturbances. Unfortunately there exists a complex interaction between the input filter, the output filter and the control loop [2,3,4,5] which can result in loop instability, degradation of transient response and of the audiosusceptibility characteristic; this makes the input filter design more difficult.

In this report the problems caused by the interaction between the input filter, output filter, and the control loop are first discussed. The input filter design is made more complicated because of the need to avoid performance degradation and also stay within the weight and loss limitations. Conventional input filter design techniques are discussed next. The concept of pole zero cancellation developed earlier [6] is reviewed next; this concept is the basis for an approach to control the peaking of the output impedance of the input filter and thus mitigate some of the problems caused by the input filter. The proposed approach to control the peaking of the output impedance of the input filter is to use a feedforward loop working in conjunction with the feedback loops already developed [6], thus forming a total state control scheme. The design of the feedforward loop for a buck regulator proceeded in three

steps which are presented next. The report ends with a possible implementation of the feedforward loop design.

II. INPUT FILTER RELATED PROBLEMS

A buck type switching regulator with a single stage input filter is shown in Fig. 2.1. The switching regulator has been shown to have a nonlinear negative resistance, Fig. 2.2, [3]. The input current i_r to the switching regulator is related nonlinearly to the input voltage e_r and the input resistance $\frac{di_r}{de_r} = -\frac{1}{r}$. Under certain conditions the input filter-switching regulator combination can become a negative resistance oscillator, producing large amplitude voltage excursions across capacitor C_1. When this happens serious degradation of regulator performance could occur, [3], including loss of stability.

The effect of the input filter is more clearly seen using a small signal model.

The averaging technique [1] can be used to relate the low frequency modulation component of the source voltage and control signal to the corresponding frequency components of the converter output voltage. Using the continuous inductor current buck regulator with input filter of Fig. 2.1, as an example, a small signal model using the dual-input describing function can be developed, as shown in Fig. 2.3, [2]. In this model the effect of the input filter is characterized by the following two parameters: the forward transfer characteristic of the input filter H(s) and the output impedance of the input filter Z(s). In Fig. 2.1 the output filter is made up of R_ℓ, L, R_C and C, R_L is the load resistance, D is the steady state duty cycle ratio $D = T_{on}/T$,

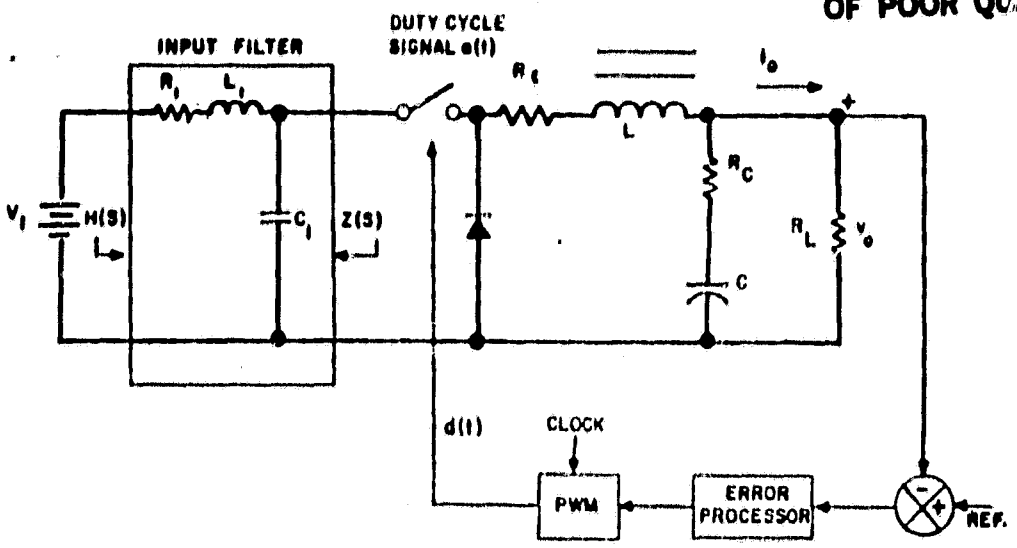


Fig. 2.1. Buck Converter with an input filter.

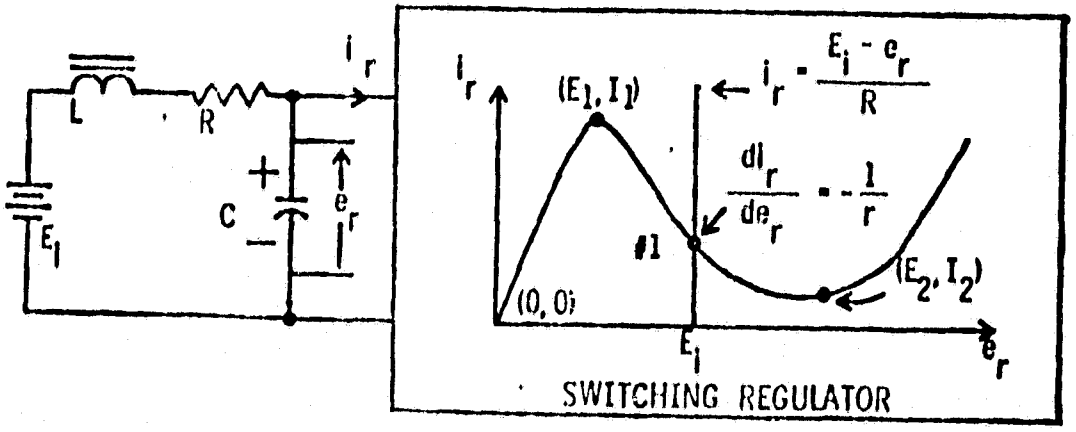


Fig. 2.2. Negative resistance oscillation.

V_I and I_I are the steady state regulator input voltage and current respectively, and the lower case letters with a caret above them denote modulation signals.

The small signal model of Fig. 2.3 can be used to illustrate the complex interaction between the input filter, output filter and the control loop and the problems caused by the interaction, [2].

2.1 Input filter Interaction -- Loop Stability and Transient Response

The stability of a switching regulator can be examined by the open loop gain $G_T(s)$:

$$G_T(s) = F_C(s)F_p(s)F_E(s)F_M(s) \qquad (2\text{-}1)$$

where $F_c(s)F_p(s)$ is the duty cycle-to-output describing function $\hat{v}_o/\hat{d}$, and $F_E(s), F_M(s)$ are the transfer functions of the error processor and pulse modulator respectively. The peaking of the output impedance of the input filter Z(s) has the following effects:

1. The duty-cycle power stage gain $F_C(s)$ includes the output impedance Z(s) -

$$F_C(s) = V_I - Z(s)I_I \text{ or} \qquad (2\text{-}2)$$

$$F_C(s) = I_I\left[\frac{V_I}{I_I} - Z(s)\right] \qquad (2\text{-}3)$$

The first term in the brackets $\frac{V_I}{I_I}$ is the negative input impedance of the regulator. At the input filter resonant frequency, Z(s) reaches a peak value and if this value is large enough the result could be a reduction in loop gain or even worse a negative duty cycle power stage gain $F_C(s)$. Reduction in loop gain could lead to loop instability, whereas a

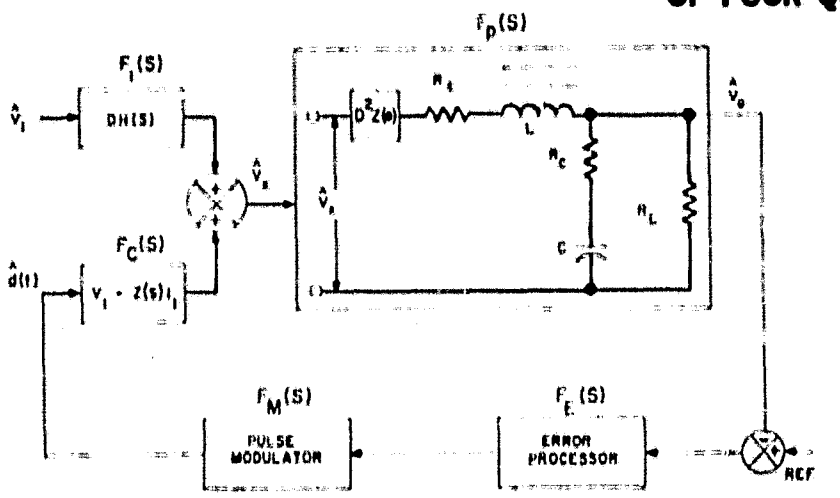


Fig. 2.3. Small-signal model using the dual-input describing function.

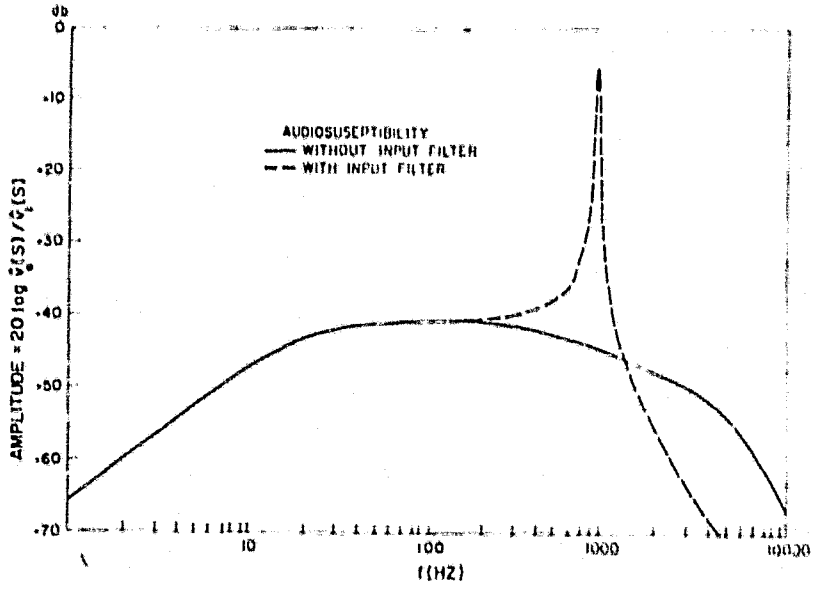


Fig. 2.5. Audiosusceptibility with and without input filter.

negative $F_c(s)$ together with the negative feedback loop will result in a positive feedback unstable system.

2. The power stage transfer function $F_p(s)$ includes the output impedance $Z(s)$ -

$$F_p(s) = \frac{[R_C + 1/sC]//R_L}{D^2 Z(s) + Z_i(s)} \quad \text{where} \tag{2-4}$$

$$Z_i(s) = R_\ell + sL + [R_c + 1/sC]//R_L \tag{2-5}$$

= input impedance of the regulator.

Excessive $Z(s)$ at the input filter resonant frequency can significantly reduce $F_p(s)$, and thus the loop gain.

Figures 2.4(a) and 2.4(b), [2], illustrate the effect of peaking of $Z(s)$ on the duty cycle-to-output transfer function $F_c(s)F_p(s)$ if an improperly designed input filter is employed. At the input filter resonant frequency the peaking of the output impedance $Z(s)$ causes a sharp change in the gain and phase of the duty cycle-to-output transfer function. This results in loop instability and degradation of transient response from a presumably well damped system to an oscillatory one; control of the peaking effect of the output impedance $Z(s)$ is necessary to avoid these problems.

2.2 Input filter Interaction - Audiosusceptibility and Output Impedance

The audiosusceptibility is defined as the closed loop input-to-output transfer function $G_A(s)$; this transfer function indicates how a small audio frequency disturbance on the input voltage affects the regulated output voltage.

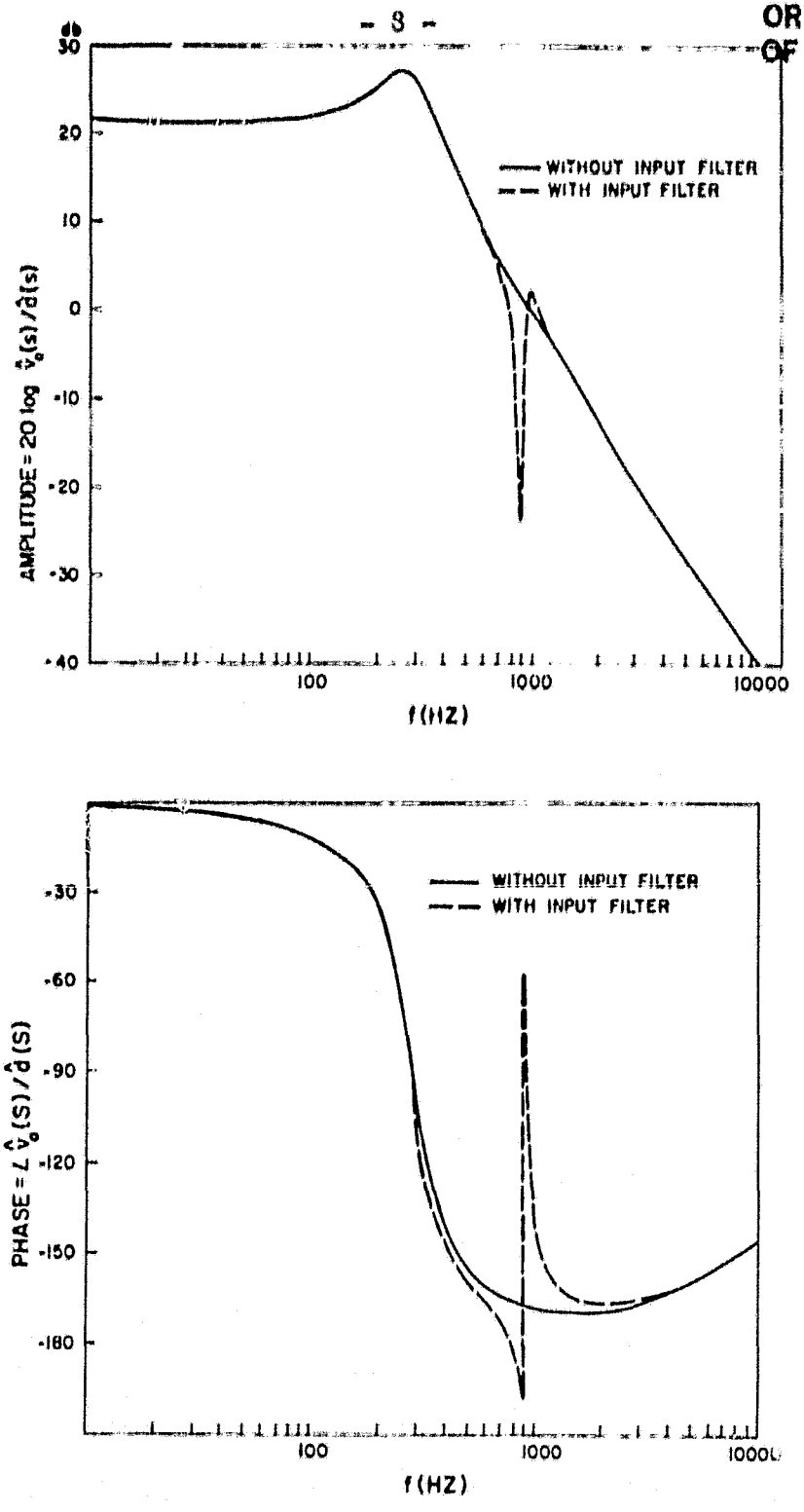


Fig. 2.4. Duty cycle-to-output voltage transfer characteristic with and without input filter (a) gain (b) phase.

$$G_A(s) = \frac{v_o(s)}{v_I(s)} = \frac{F_I(s)F_p(s)}{1+F_C(s)F_p(s)F_E(s)F_M(s)} = \frac{F_I(s)F_p(s)}{1+G_T(s)} \qquad (2\text{-}6)$$

where $F_I(s) = DH(s)$ = input voltage gain of the power stage. $G_A(s)$ and thus the audiosusceptibility are affected by the resonant peaking of the output impedance Z(s) and of the forward transfer function of the input filter with the regulator disconnected H(s), because $F_I(s)$ is a function of H(s) whereas $F_C(s)$ and $F_p(s)$ are functions of Z(s). The reduction of loop gain at the resonant frequency can thus severely degrade the audiosusceptibility. Fig. 2.5, [2], illustrates the audiosusceptibility of the buck regulator with and without an input filter.

The output impedance of the buck regulator is affected at the resonant frequency. The output impedance should be low but at resonance the reduction in loop gain causes an increase in the output impedance.

Control of the peaking of Z(s) and H(s) is thus necessary to avoid serious degradation of audiosusceptibility at the resonant frequency. It is also seen that the reduction in loop gain affects not only stability but also audiosusceptibility, output impedance and transient response.

A buck type switching regulator with a two stage input filter is shown in Fig. 2.6. Fig. 2.7, [2], shows the measured values of open loop gain and phase as a function of the frequency. Significant changes in the open loop gain and phase characteristics at the resonant frequencies of both the first stage and the second stage of the input filter are observed, [2]. Thus it is seen that the peaking of the output impedance at resonant frequency of the two stage input filter can also cause serious performance degradation.

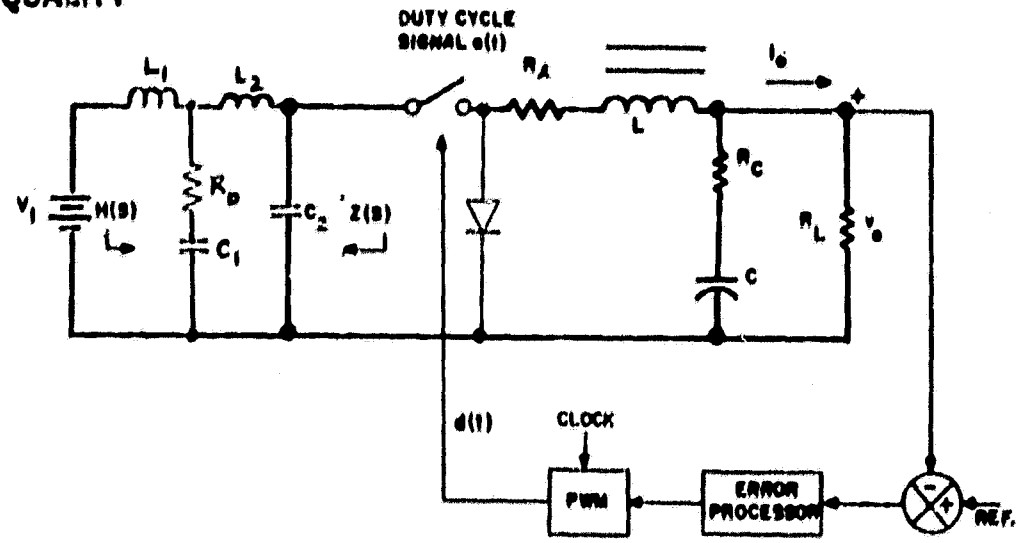


Fig. 2.6. Buck type switching regulator with a two stage input filter.

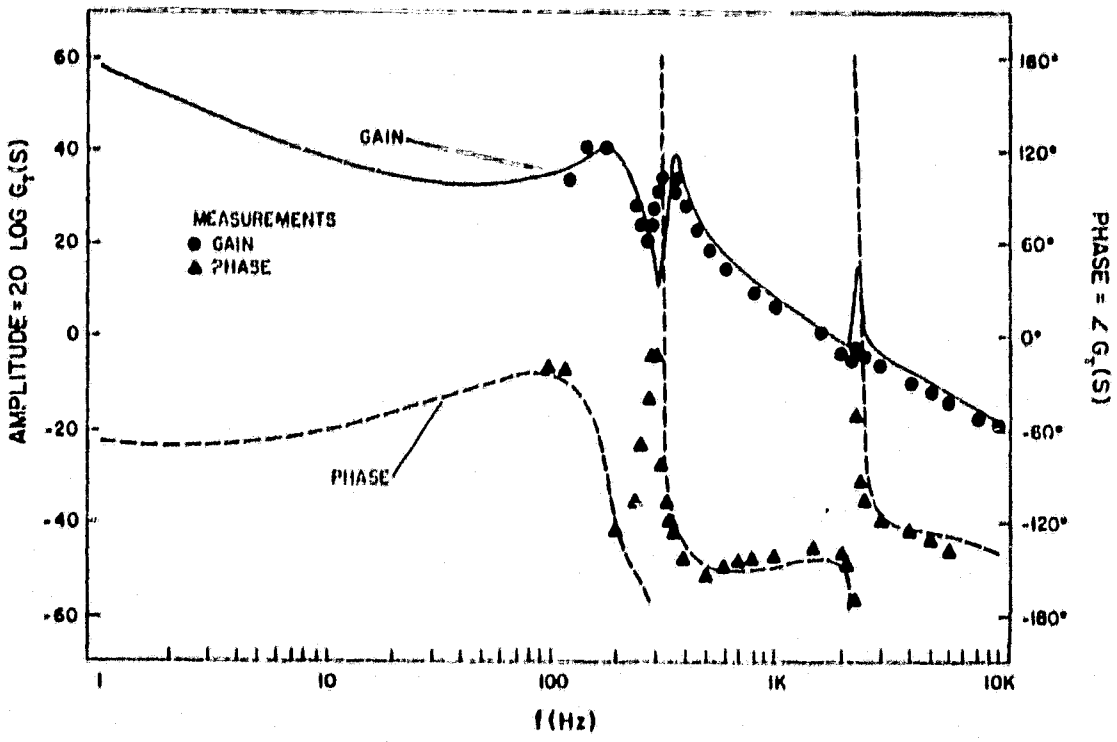


Fig. 2.7. Open loop gain and phase characteristics without the input filter damping resistance R_D.

III. CONVENTIONAL INPUT FILTER DESIGN TECHNIQUES

The design of the input filter is constrained by the following requirements -

1) The amount of regulator switching current reflected back into the source should be limited (conducted interference requirement).
2) The peaking of the output impedance of the input filter Z(s) should be limited to a safe value to avoid loop instability.
3) The peaking of the transfer function of the input filter H(s) should be limited, where H(s) is designed to satisfy the conducted interference requirement, [5].
4) The input filter weight and energy loss are limited.
5) The Nyquist stability criterion has to be satisfied; thus the closed loop poles should be in the left half plane for stable operation -

$$\left|1 + F_C(s)F_p(s)F_E(s)F_M(s)\right| > 0$$

6) The closed-loop input-to-output transfer characteristic (audiosusceptibility) should not be degraded by a noticeable amount.

The input filter design is made more complicated by the necessity of avoiding performance degradation and still stay within the weight and loss limitations. An input filter design that limits performance degradation (degradation of stability, transient response and audiosusceptibility) often penalizes the input filter weight and loss. A satisfactory input filter design thus trades off one or more of the performance degradations for size, weight or loss.

Some of the conventional design techniques are presented.

3.1 The single stage input filter

The single stage input filter can be designed to avoid performance degradation -- but this would result in larger filter L_1 and C_1, thus resulting in weight and size increase. The filter of Fig. 3.1(a), [3], is simple and commonly used but it cannot often satisfy the stringent requirement on audiosusceptibility. Resonant peaking of the filter of Fig. 3.1(b), [3], is lowered by adding resistance R, but this lowers efficiency because the pulse current flowing through C_1 increases losses. Another design uses a resistance R in parallel across C_1, [5], but this results in a large C_1.

The design of a single stage input filter thus is not possible without trade off between performance degradations and the weight and loss limitations.

3.2 Separation of the input and output filter resonant frequencies

The degradation of the power stage transfer function $F_p(s)$ due to peaking of Z(s) can be avoided if there is sufficient separation of the input filter resonance frequency $w_1 = \frac{1}{\sqrt{L_1 C_1}}$ and the output filter resonant frequency $w_0 = \frac{1}{\sqrt{LC}}$, [2,4,5]. Fig. 3.2, [2,4,5], shows three possible combinations of w_1 and w_0. $F_p(s)$ is related to both Z(s) and the input impedance of the regulator $z_i(s)$ thus

$$F_p(s) = \frac{[R_c + 1/sC]//R_L}{D^2 Z(s) + Z_i(s)} \qquad (3\text{-}1)$$

where $$Z_i(s) = R_\ell + sL + [R_c + 1/sC]//R_L \qquad (3\text{-}2)$$

$$= \text{input impedance of the regulator.}$$

Z(s) and $Z_i(s)$ peak at the frequencies w_1 and w_0 respectively. If the two

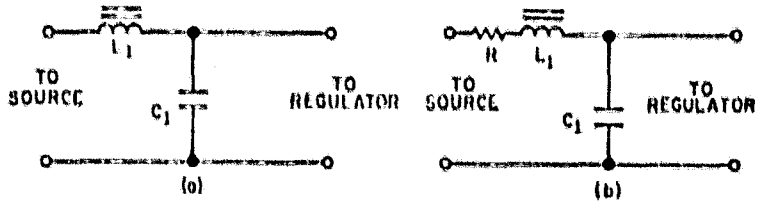


Fig. 3.1. Single-stage input filters.

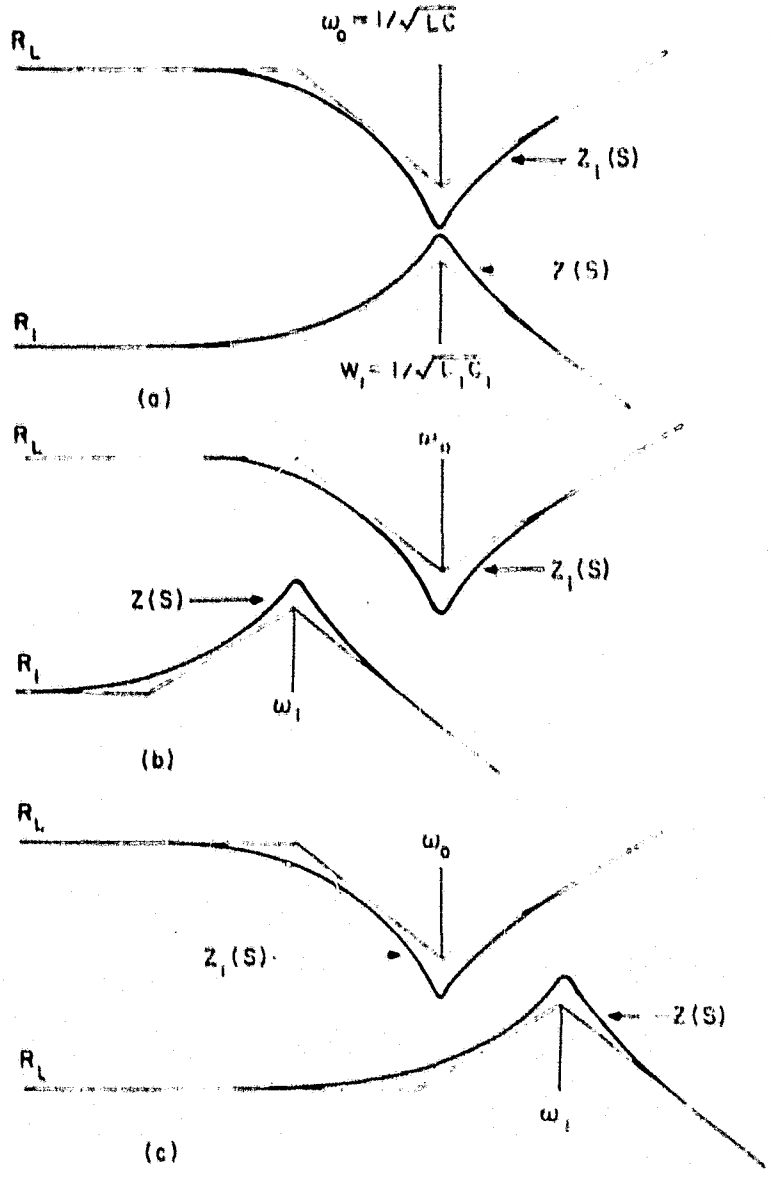


Fig. 3.2. Interaction between output impedance Z(s) of input filter and input impedance $Z_1(s)$ of regulator.

resonance frequencies are the same as in Fig. 3-2(a) then both Z(s) and $Z_1(s)$ peak at the same frequency and thus at that frequency the transfer function $F_p(s)$ would be affected, i.e. reduced, to the maximum possible extent. Shifting the two frequencies w_0 and w_1 apart as shown in Figs. 3.2(b) and (c) will result in reducing the effect of peaking on $F_p(s)$. Reducing w_1 would result in increasing the size of the input filter, thus possibly violating the weight limitation. A high value of w_1 is desirable from the point of view of weight and size reduction but this results in performance degradation -- from Fig. 2.4 it is clear that the gain of the duty cycle-to-output transfer function $F_C(s)F_p(s)$ decreases with increasing frequency and thus the effect of peaking of Z(s) on the gain of $F_C(s)F_p(s)$ would be more pronounced if Z(s) peaks at a higher w_1. The reduction of the loop gain at higher input filter resonant frequency w_1 often results in poor audiosusceptibility, oscillatory transient response or even an unstable system. The choice of w_1 thus involves a trade off.

3.3 The two stage input filter

A two-stage input filter configuration has been described, [2,3] and is shown in Fig. 3.3. The first stage consisting of L_1,C_1,R_3 and R_1 controls the resonant peaking of the filter. The second stage consisting of L_2, C_2 supplies most of the pulse current required by the regulator. As shown in the literature, [2], the two stage input filter is capable of reducing H(s) and Z(s) at resonant frequency without significantly increasing weight and loss, unlike the single-stage input filter. Computer optimization techniques have been utilized to optimally design two-stage filters. It has been shown that the two-stage filter is much lighter than its single-stage counterpart under identical design constraints.

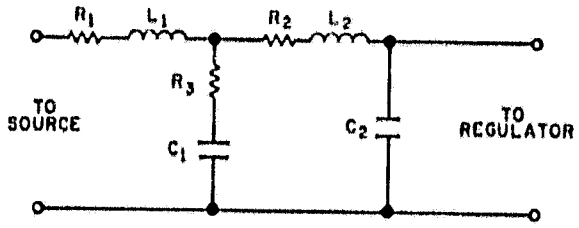


Fig. 3.3. Two-stage input filter.

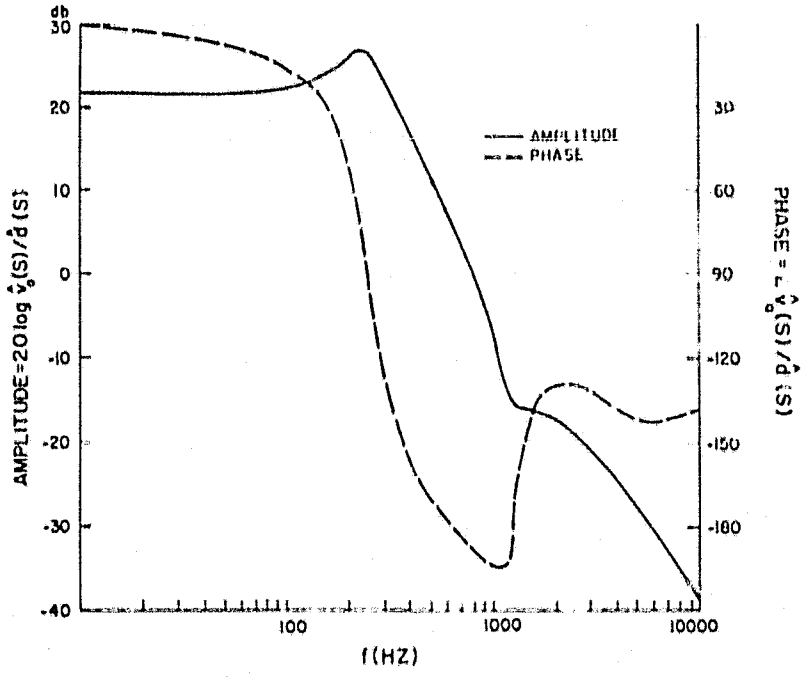


Fig. 3.4. Duty cycle-to-output describing function of power stage with two-stage input filter.

Also it has been shown that for the same filter weight the single stage filter has a significantly higher peaking of H(s) and Z(s). Fig. 3.4 shows the gain and phase of the duty cycle-to-output describing function of a power stage with a two stage input filter, [2]. Fig. 2.4 shows the gain and phase of the duty cycle-to-output describing function of a power stage with a single-stage input filter, and the two-stage filter of Fig. 3.4 was designed to have the same weight as the single-stage input filter of Fig. 2.4. Comparing the two figures the improvement in performance regarding the duty cycle-to-output transfer function is dramatic and obvious.

It can therefore be concluded that the two-stage filter provides the best compromise among the conflicting requirements of an input filter.

IV. CONCEPT OF POLE-ZERO CANCELLATION

A two loop adaptive feedback control implementation was developed earlier, [6]. Fig. 4.1, [6], shows a two-loop controlled switching buck regulator. The dc loop senses the converter output voltage and compares it with the reference voltage to generate a dc error signal for voltage regulation. The ac loop senses the ac voltage across the output filter inductor to generate an ac signal. Both ac and dc signals are processed through an operational amplifier summing junction to provide a total error signal at the output of the operational amplifier integrator. It is apparent that the error signal at the output of the integrator contains information regarding the output filter state variables -- the inductor current and the capacitor voltage. It was shown, [6], that the feedback control loops when properly designed can provide complex zeros to cancel completely the complex poles presented by the low-pass output filter of the power stage. It was also shown that the feedback control loop has the ability to sense filter parameter changes and automatically provide pole-zero cancellation. To examine the adaptive nature of the control loops the open loop regulator transfer function $G_T(s)$ is used

$$G_T(s) = \frac{kZ(jw)}{sP(jw)} \tag{4-1}$$

where K is a constant determined by the power stage and control loop parameters and

$$Z(jw) = 1 + j2e_1\, w/w_{n1} - w^2/w_{n1}^2 \tag{4-2}$$

$$P(jw) = 1 + j2e_2\, w/w_{n2} - w^2/w_{n2}^2 \tag{4-3}$$

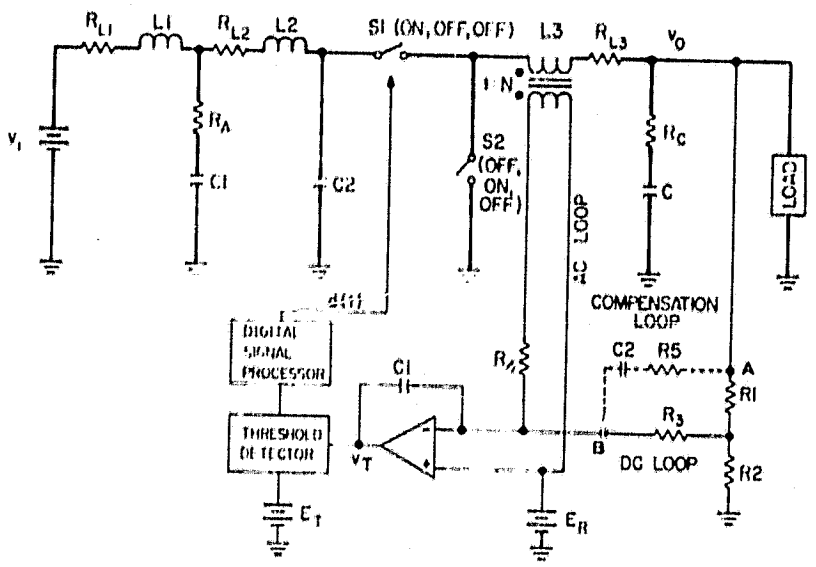


Fig. 4.1. Two loop controlled switching buck regulator.

P(jw) has complex poles corresponding to the output filter and Z(jw) has complex zeros produced by the two loop feedback control.

$$w_{n1} = \sqrt{\frac{\alpha}{LC}} \tag{4-4}$$

$$w_{n2} = \frac{1}{\sqrt{LC}} \tag{4-5}$$

$$e_1 = \frac{w_{n1}}{2}\,\tau_z \tag{4-6}$$

$$e_2 = \frac{w_{n2}}{2}\left(\frac{L}{R_L} + R_C C + R_\ell C\right) \tag{4-7}$$

$$\alpha = \frac{R_4}{NR_Y} \tag{4-8}$$

$$\tau_z = (R_Y + R_5)C_2 + \frac{L}{\alpha R_L} \tag{4-9}$$

$$R_Y = \left[(R_1/R_2) + R_3\right]\frac{(R_1 + R_1)}{R_2} \tag{4-10}$$

L, C, R_ℓ and R_C form the output filter as in Fig. 4.1. The control parameters can be chosen such that

$$w_{n1} = w_{n2} \tag{4-11}$$

$$e_1 = e_2 \tag{4-12}$$

thus resulting in

$$P(jw) = Z(jw) \tag{4-13}$$

and

$$G_T(s) = \frac{K}{S} \tag{4-14}$$

The open loop transfer function is of first order and is completely independent of output filter parameters. The adaptive nature of the control loop is apparent from the fact that the complex zeros imitate

the change in the complex poles due to component tolerance, aging or temperature variations, thus preserving the pole-zero cancellation. This concept of pole-zero cancellation of the output filter characteristics is used to investigate the pole-zero cancellation of the input filter characteristics as well.

V. MODELING OF THE POWER STAGE WITH INPUT FILTER

The first step in the design and analysis of the feedforward loop is to develop the small signal model of the power stage with input filter for the buck-boost, buck and boost type of switching regulators, using the averaging technique, [1]. The modeling is carried out in the continuous conduction operating mode, in which the inductor current is always nonzero. This mode is the prevalent operating mode for most dc-dc converters. The discontinuous conduction operating mode in which the inductor current is zero for some time during the cycle occurs at light loads and is seldom used as the intended design at full load.

The modeling is carried out in the following steps -

1) State space equation formulation during T_{ON} and T_{OFF}
2) State space averaging and perturbation.
3) Linearization and derivation of the small signal equations and the small signal equivalent circuit and state space model.

5.1 Buck-boost converter small signal model derivation

The buck-boost converter is shown in Fig. 5.1. During T_{ON}, the switch S is on and the circuit is as shown in Fig. 5.2

The equations describing the circuit are

$$i_p = \frac{N_P}{L_p}\,\phi \qquad \phi = \text{flux in core} \tag{5-1}$$

$$\frac{di_{L1}}{dt} = \frac{i_{L1}}{L1}\,(-R_{L1} - R_{C1}) + \frac{R_{C1}}{L1}\,\frac{N_P}{L_p}\,\phi - \frac{v_{C1}}{L1} + \frac{v_I}{L1} \tag{5-2}$$

$$\frac{d\phi}{dt} = \frac{v_{C1}}{N_P} + \frac{R_{C1}}{N_P}\,i_{L1} - \frac{\phi}{L_p}\,(R_{C1} + R_p) \tag{5-3}$$

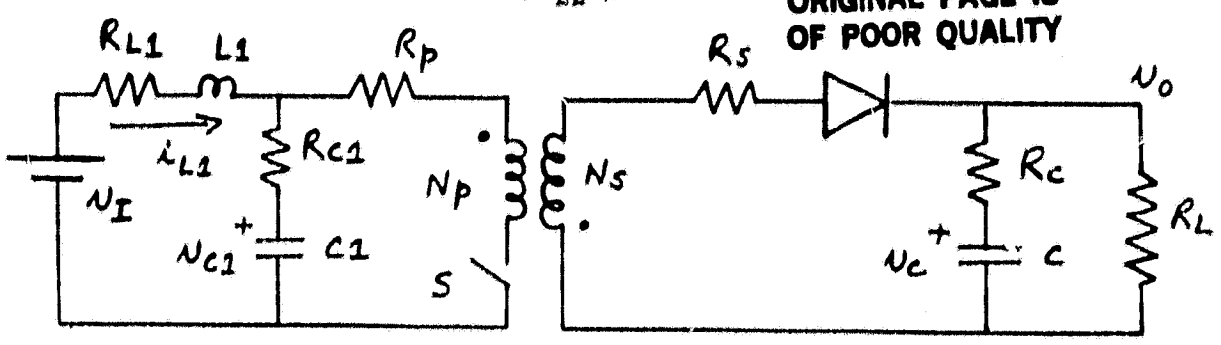


Fig. 5.1. Buck-boost converter power stage.

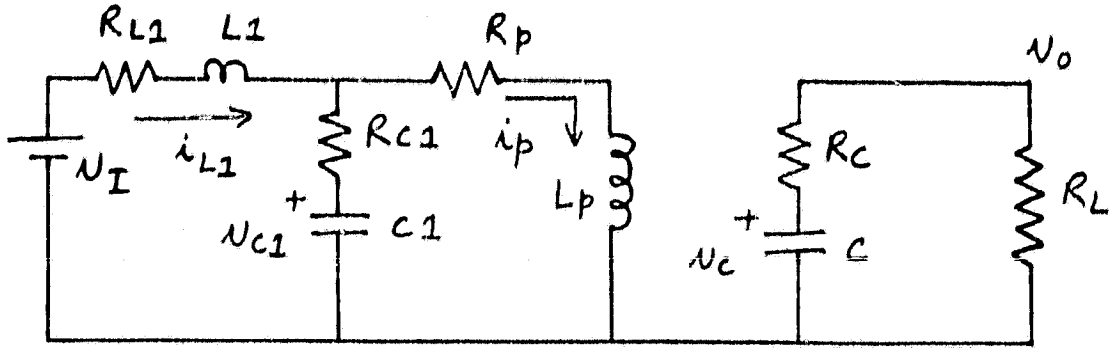


Fig. 5.2. Buck-boost converter power stage model during T_{ON}.

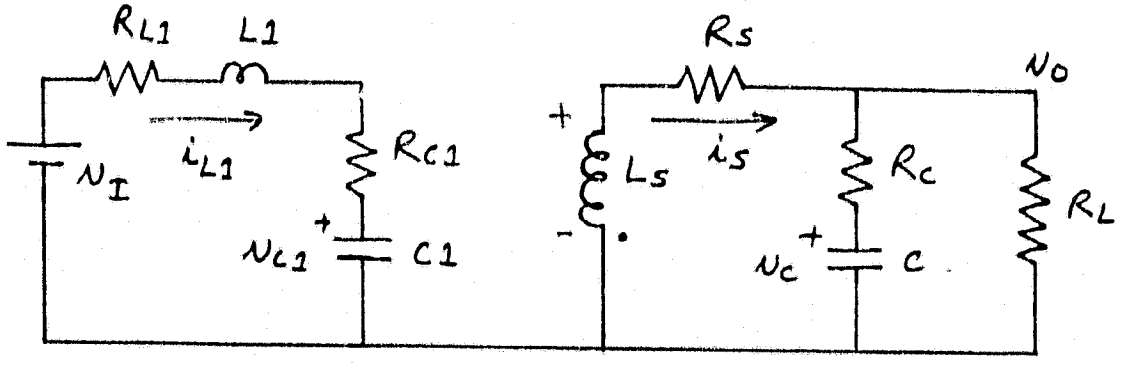


Fig. 5.3. Buck-boost converter power stage model during T_{OFF}.

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C1} - \frac{N_p}{C1L_p}\phi \tag{5-4}$$

$$\frac{dv_C}{dt} = \frac{-v_C}{C(R_L+R_C)} \tag{5-5}$$

$$v_0 = \frac{R_L v_C}{R_C+R_L} \tag{5-6}$$

During T_{OFF} the switch S is off and the circuit is as shown in Fig. 5.3 The equations describing the circuit are

$$i_S = \frac{N_S}{L_S}\phi \tag{5-7}$$

$$\frac{di_{L1}}{dt} = \frac{i_{L1}}{L1}(-R_{L1} - R_{C1}) - \frac{v_{C1}}{L1} + \frac{v_I}{L1} \tag{5-8}$$

$$\frac{d\phi}{dt} = \frac{-(R_S R_C + R_S R_L + R_C R_L)\phi}{L_S(R_C + R_L)} - \frac{R_L v_C}{N_S(R_C + R_L)} \tag{5-9}$$

$$\frac{dv_{C1}}{C1} = \frac{i_{L1}}{C1} \tag{5-10}$$

$$\frac{dv_C}{dt} = \frac{N_S R_L \phi}{CL_S(R_C+R_L)} - \frac{v_C}{C(R_C+R_L)} \tag{5-11}$$

$$v_0 = \frac{R_L v_C}{R_C+R_L} + \frac{R_C R_L N_S \phi}{L_S(R_C+R_L)} \tag{5-12}$$

The following vectors are defined

$$\underline{x} = \begin{bmatrix} i_{L1} \\ \phi \\ v_{C1} \\ v_C \end{bmatrix} \qquad \underline{u} = [v_I] \qquad \underline{y} = [v_0] \tag{5-13}$$

resulting in the following state space equations

T_{ON}	T_{OFF}	
$\dot{\underline{x}} = A_1 \underline{x} + B_1 \underline{u}$	$\dot{\underline{x}} = A_2 \underline{x} + B_2 \underline{u}$	(5-14)
$\underline{y} = C_1 \underline{x}$	$\underline{y} = C_2 \underline{x}$	

where

$$A_1 = \begin{bmatrix} -\frac{(R_{L1}+R_{C1})}{L1} & \frac{R_{C1}N_P}{L1L_P} & \frac{-1}{L1} & 0 \\ \frac{R_{C1}}{N_P} & \frac{-(R_{C1}+R_P)}{L_P} & \frac{1}{N_P} & 0 \\ \frac{1}{C1} & \frac{-N_P}{C1L_P} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C(R_L+R_C)} \end{bmatrix} \tag{5-15}$$

$$A_2 = \begin{bmatrix} -\frac{(R_{L1}+R_{C1})}{L1} & 0 & \frac{-1}{L1} & 0 \\ 0 & \frac{-R_1}{L_S} & 0 & \frac{-R_L}{N_S(R_C+R_L)} \\ \frac{1}{C1} & 0 & 0 & 0 \\ 0 & \frac{N_S R_L}{CL_S(R_C+R_L)} & 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix} \tag{5-16}$$

$$B_1 = \begin{bmatrix} \frac{1}{L1} & 0 & 0 & 0 \end{bmatrix}^T \tag{5-17}$$

$$B_2 = B_1 \tag{5-18}$$

$$C_1 = \begin{bmatrix} 0 & 0 & 0 & \dfrac{R_L}{R_C + R_L} \end{bmatrix} \tag{5-19}$$

$$C_2 = \begin{bmatrix} 0 & \dfrac{R_C R_L N_S}{L_S (R_C + R_L)} & 0 & \dfrac{R_L}{R_C + R_L} \end{bmatrix} \tag{5-20}$$

$$R_1 = \frac{R_S R_C + R_S R_L + R_C R_L}{R_C + R_L} \tag{5-21}$$

The state space averaged model over the entire period T is

$$\dot{\underline{x}} = [dA_1 + d'A_2]\ \underline{x} + [dB_1 + d'B_2]\ \underline{u} \tag{5-22}$$

$$\underline{y} = [dC_1 + d'C_2]\ \underline{x}$$

where d = duty cycle ratio $= \dfrac{T_{ON}}{T_{ON} + T_{OFF}}$ (5-22)

$$d' = 1 - d$$

$$T = T_{ON} + T_{OFF} \tag{5-23}$$

The state space averaged model is perturbed thus –

$$d = D + \hat{d}$$

$$d' = D' - \hat{d}$$

$$\underline{u} = \underline{U} + \hat{\underline{u}} \tag{5-24}$$

$$\underline{y} = \underline{Y} + \hat{\underline{y}}$$

$$\underline{x} = \underline{X} + \hat{\underline{x}}$$

Assuming that the perturbation is small

$\dfrac{\hat{d}}{D} << 1$, $\dfrac{\hat{x}}{X} << 1$ etc. leads to the following small signal linearized model

$$\underline{Q} = [DA_1 + D'A_2]\ \underline{X} + [DB_1 + D'B_2]\ V_I$$

$$V_0 = [DC_1 + D'C_2]\ \underline{X}$$

$$\dot{\underline{\hat{x}}} = [DA_1 + D'A_2]\ \hat{\underline{x}} + [DB_1 + D'B_2]\ \hat{v}_I \qquad (5\text{-}25)$$

$$+ [A_1 - A_2)\ \underline{X} + (B_1 - B_2\ V_I]\ \hat{d}$$

$$\hat{v_0} = [C_1 - C_2]\ X\ \hat{d} + [DC_1 + D'C_2]\ \hat{x}$$

Defining

$$A = DA_1 + D'A_2$$

$$B = DB_1 + D'B_2 \qquad (5\text{-}26)$$

$$C = DC_1 + D'C_2$$

results in

$$\dot{\underline{\hat{x}}} = A\ \underline{\hat{x}} + B\ \hat{v}_I$$

$$+ [A_1 - A_2)\ \underline{X} + (B_1 - B_2)\ V_I]\ \hat{d} \qquad (5\text{-}27)$$

$$\hat{v_0} = [C_1 - C_2]\ \underline{X}\ \hat{d} + C\ \underline{\hat{x}}$$

Using Laplace transforms results in

$$\underline{\hat{x}}(s) = [SI - A]^{-1} B\ \hat{v_I}(s)$$

$$+ [SI - A]^{-1}[(A_1 - A_2)\ X + (B_1 - B_2)\ V_I]\ \hat{d}(s) \qquad (5\text{-}28)$$

$$\hat{v}_0(s) = [C_1 - C_2]\ \underline{X}\ \hat{d}(s) + C\ \underline{\hat{x}}(s)$$

The state space model is derived from the two equations above, and is shown in Fig. 5.4.

To derive the small signal equivalent circuit, it is first necessary to use the equation for $\hat{v_0}$ to substitute for $\hat{v_C}$ in terms of $\hat{v_0}$, in the small signal equations described above. Simplifying the four equations

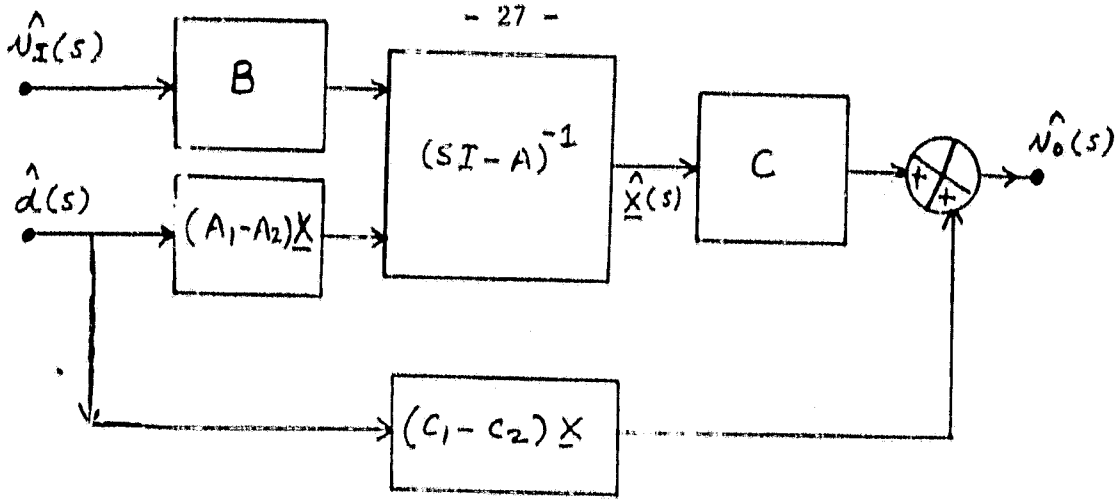
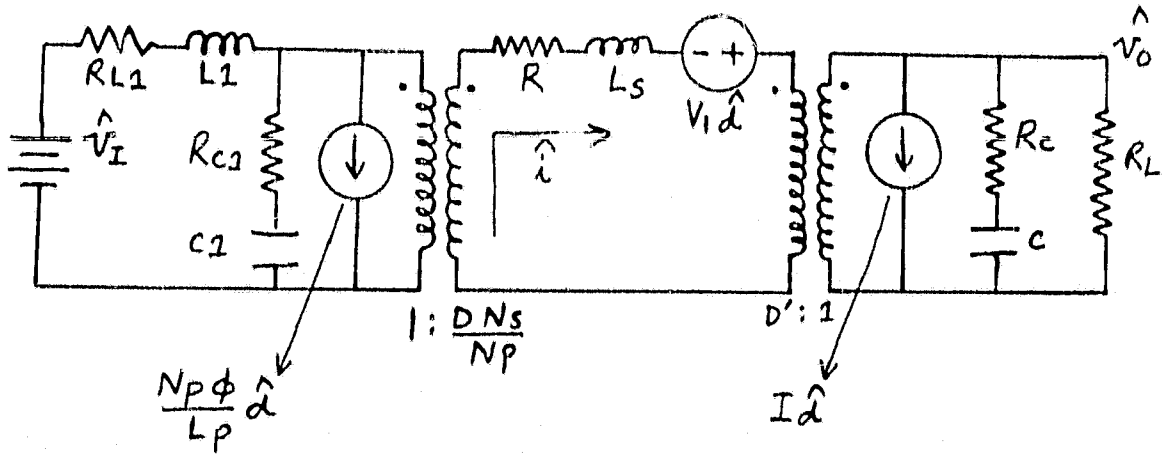


Fig. 5.4. Buck-boost converter power stage small signal state space model.



$$R = \frac{DD'R_{C1}L_S}{L_P} + \frac{DD'R_CR_L}{R_C + R_L} + R_S$$

$$V_1 = \left[\frac{R_{C1}I_{L1}N_S}{N_P} - \frac{R_{C1}IL_S}{L_P} + \frac{R_CR_LI(D-D')}{(R_C + R_L)} + \frac{V_{C1}N_S}{N_P} + V_O \right]$$

Fig. 5.5. Buck-boost converter power stage small signal equivalent circuit.

are obtained

$$\hat{v}_I = (R_{C1} + R_{L1})\hat{i}_{L1} - \frac{R_{C1}N_P D}{L_P}\hat{\phi} + L1\frac{d\hat{i}_{L1}}{dt} + \hat{v}_{C1} - \frac{R_{C1}N_P}{L_P}\phi\,\hat{d} \tag{5-29}$$

$$C1\frac{d\hat{v}_{C1}}{dt} = \hat{i}_{L1} - \frac{DN_P}{L_P}\hat{\phi} - \frac{N_P}{L_P}\phi\,\hat{d} \tag{5-30}$$

$$C\frac{d\hat{v}_C}{dt} = \frac{D'N_S}{L_S}\hat{\phi} - \frac{\hat{v}_O}{R_L} - \frac{N_S}{L_S}\phi\,\hat{d} \tag{5-31}$$

$$D\frac{\hat{v}_{C1}N_S}{N_P} = \frac{N_S d\hat{\phi}}{dt} - \frac{R_{C1}N_S D}{N_P}\hat{i}_{L1} + \frac{DR_{C1}N_S}{L_P}\hat{\phi} + \frac{R_S N_S}{L_S}\hat{\phi} + \frac{DD'R_C R_L N_S}{L_S(R_C+R_L)}\hat{\phi} + D'\hat{v}_O - \frac{R_{C1}I_{L1}N_S}{N_P}\hat{d} + \frac{R_{C1}\hat{d}\phi N_S}{L_P} - \hat{d}\,V_O - \frac{R_C R_L N_S \phi\hat{d}(D-D')}{L_S(R_C+R_L)} - \frac{V_{C1}N_S}{N_P}\hat{d} \tag{5-32}$$

Using a fictitious current i described by

$$L_S i = N_S\phi \tag{5-33}$$

an equivalent circuit can be made up that is described by the four equations given above. This circuit will use the current i flowing through L_S and it is thus the small signal equivalent circuit for the buck-boost converter, as shown in Fig. 5.5.

5.2 Buck converter small signal model derivation

The procedure used in deriving the small signal model for the buck converter is exactly similar to that used for the buck-boost converter. The buck converter is shown in Fig. 5.6.

During T_{ON} the switch S is on and the circuit is as shown in Fig. 5.7.

The equations describing the circuit are

$$\frac{di_{L1}}{dt} = \frac{-(R_{L1} + R_{C1})}{L1} i_{L1} + \frac{R_{C1}}{L1} i_L - \frac{v_{C1}}{L1} + \frac{v_I}{L1} \tag{5-34}$$

$$\frac{di_L}{dt} = \frac{R_{C1}}{L} i_{L1} - \frac{R_1}{L} i_L + \frac{v_{C1}}{L} - \frac{R_L v_C}{L(R_C + R_L)} \tag{5-35}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C1} - \frac{i_L}{C1} \tag{5-36}$$

$$\frac{dv_C}{dt} = \frac{R_L i_L}{C(R_C + R_L)} - \frac{v_C}{C(R_C + R_L)} \tag{5-37}$$

$$v_O = \frac{R_L R_C i_L}{R_L + R_C} + \frac{R_L v_C}{R_L + R_C} \tag{5-38}$$

During T_{OFF}, the switch S is off, and the circuit is shown in Fig. 5.8. The equations describing the circuit are

$$\frac{di_{L1}}{dt} = \frac{-(R_{L1} + R_{C1})}{L1} i_{L1} - \frac{v_{C1}}{L1} + \frac{v_I}{L1} \tag{5-39}$$

$$\frac{di_L}{dt} = \frac{-R_2 i_L}{L} - \frac{R_L v_C}{L(R_L + R_C)} \tag{5-40}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C1} \tag{5-41}$$

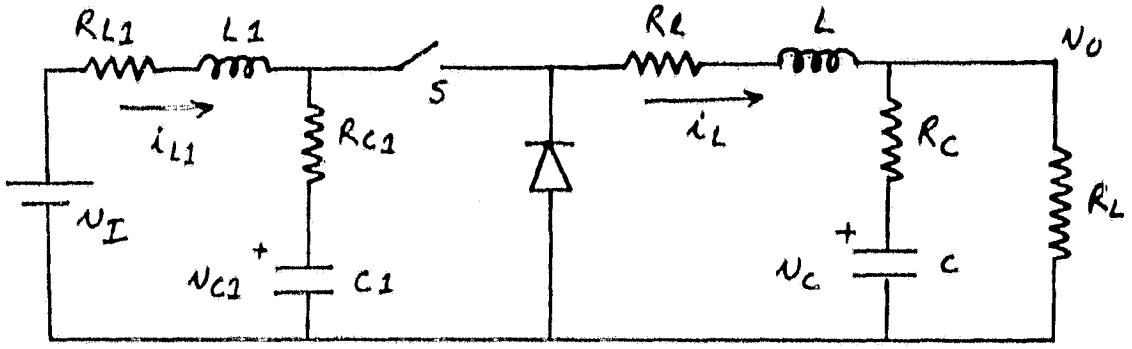


Fig. 5.6. Buck converter power stage.

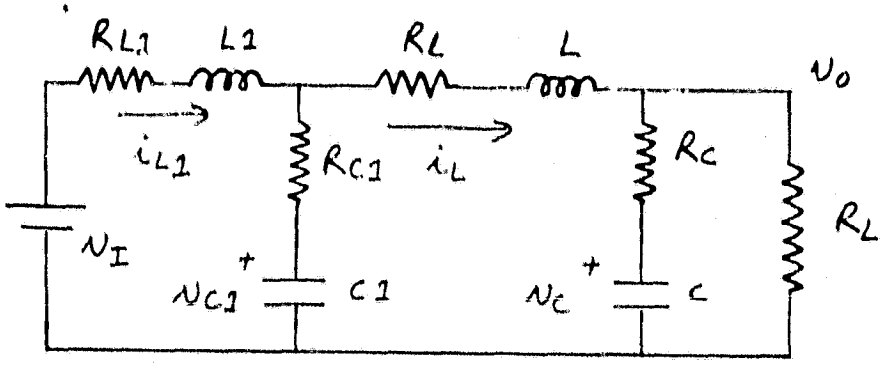


Fig. 5.7. Buck converter power stage model during T_{ON}.

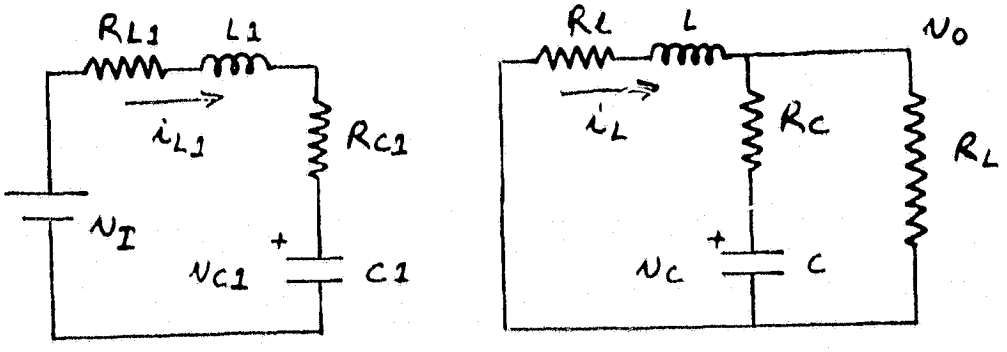


Fig. 5.8. Buck converter power stage model during T_{OFF}.

$$\frac{dv_C}{dt} = \frac{R_L i_L}{C(R_L + R_C)} - \frac{v_C}{C(R_L + R_C)} \tag{5-42}$$

$$v_O = \frac{R_L R_C i_L}{R_L + R_C} + \frac{R_L v_C}{R_L + R_C} \tag{5-43}$$

$$R_2 = R_\ell + \frac{R_C R_L}{R_C + R_L} \tag{5-44}$$

$$R_1 = R_{C1} + R_\ell + \frac{R_C R_L}{R_C + R_L} \tag{5-45}$$

The following vectors are defined

$$\underline{x} = \begin{bmatrix} i_{L1} \\ i_L \\ v_{C1} \\ v_C \end{bmatrix} \qquad \begin{aligned} \underline{u} &= [v_T] \\ \underline{y} &= [v_O] \end{aligned} \tag{5-46}$$

resulting in the following state space equation

T_{ON}	T_{OFF}	
$\dot{\underline{x}} = A_1 \underline{x} + B_1 \underline{u}$	$\dot{\underline{x}} = A_2 \underline{x} + B_2 \underline{u}$	(5-47)
$\underline{y} = C_1 \underline{x}$	$\underline{y} = C_2 \underline{x}$	

where

$$A_1 = \begin{bmatrix} \frac{-(R_{L1} + R_{C1})}{L1} & \frac{R_{C1}}{L1} & \frac{-1}{L1} & 0 \\ \frac{R_{C1}}{L} & \frac{-R_1}{L} & \frac{1}{L} & \frac{-R_L}{L(R_C + R_L)} \\ \frac{1}{C1} & \frac{-1}{C1} & 0 & 0 \\ 0 & \frac{R_L}{C(R_L + R_C)} & 0 & \frac{-1}{C(R_L + R_C)} \end{bmatrix} \tag{5-48}$$

$$A_2 = \begin{bmatrix} \frac{-(R_{L1}+R_{C1})}{L1} & 0 & \frac{-1}{L1} & 0 \\ 0 & \frac{-R_2}{L} & 0 & \frac{-R_L}{L(R_C+R_L)} \\ \frac{1}{C1} & 0 & 0 & 0 \\ 0 & \frac{R_L}{C(R_L+R_C)} & 0 & \frac{-1}{C(R_L+R_C)} \end{bmatrix} \tag{5-49}$$

$$B_1 = \begin{bmatrix} \frac{1}{L1} & 0 & 0 & 0 \end{bmatrix}^T \tag{5-50}$$

$$B_2 = B_1 \tag{5-51}$$

$$C_1 = \begin{bmatrix} 0 & \frac{R_L R_C}{R_L+R_C} & 0 & \frac{R_L}{R_L+R_C} \end{bmatrix} \tag{5-52}$$

$$C_2 = C_1 \tag{5-53}$$

The state space averaged model over the entire period T is

$$\dot{\underline{x}} = [dA_1 + d'A_2]\underline{x} + [dB_1 + d'B_2]\underline{u} \tag{5-54}$$

$$\underline{y} = [dC_1 + d'C_2]\underline{x}$$

where d = duty cycle ratio $= \frac{T_{ON}}{T_{ON} + T_{OFF}}$

$$d' = 1 - d \tag{5-55}$$

$$T = T_{ON} + T_{OFF}$$

The state space averaged model is perturbed and linearized in exactly the same way as for the buck-boost converter. The resulting small signal linearized model is

$$\underline{0} = [DA_1 + D'A_2]\underline{X} + [DB_1 + D'B_2]V_I$$

$$\dot{\underline{\hat{x}}} = [DA_1 + D'A_2]\underline{\hat{x}} + [DB_1 + D'B_2]\hat{v}_I$$

$$+ [(A_1 - A_2)\underline{X} + (B_1 - B_2)V_I]\hat{d} \qquad (5\text{-}56)$$

$$V_0 = [DC_1 + D'C_2]\underline{X}$$

$$\hat{v_0} = [C_1 - C_2]\underline{X}\hat{d} + [DC_1 + D'C_2]\underline{\hat{x}}$$

Defining

$$A = DA_1 + D'A_2$$

$$B = DB_1 + D'B_2 \qquad (5\text{-}57)$$

$$C = DC_1 + D'C_2$$

results in

$$\dot{\underline{\hat{x}}} = A\underline{\hat{x}} + B\hat{v_1}$$

$$+ [(A_1 - A_2)\underline{X} + (B_1 - B_2)V_I]\hat{d} \qquad (5\text{-}58)$$

$$\hat{v_0} = [C_1 - C_2]\underline{X}\hat{d} + C\underline{\hat{x}}$$

Using Laplace transforms gives

$$\underline{\hat{x}}(s) = [SI - A]^{-1}B\ \hat{v_I}(s)$$

$$+ [SI - A]^{-1}[(A_1 - A_2)\underline{X} + B_1 - B_2)V_I]\hat{d}(s) \qquad (5\text{-}59)$$

$$v_0(s) = [C_1 - C_2]\underline{X}\ \hat{d}(s) + C\ \underline{\hat{x}}(s)$$

The state space model is derived from the above two equations and is shown in Fig. 5.9.

The procedure for deriving the small signal equivalent circuit is exactly similar to the one used for the buck-boost converter. The four equations that result are

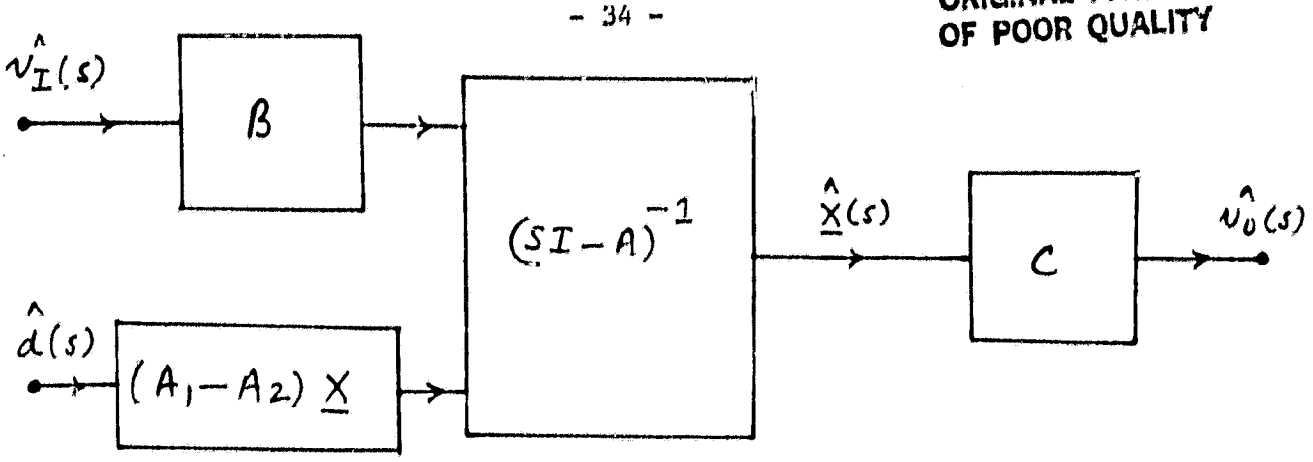
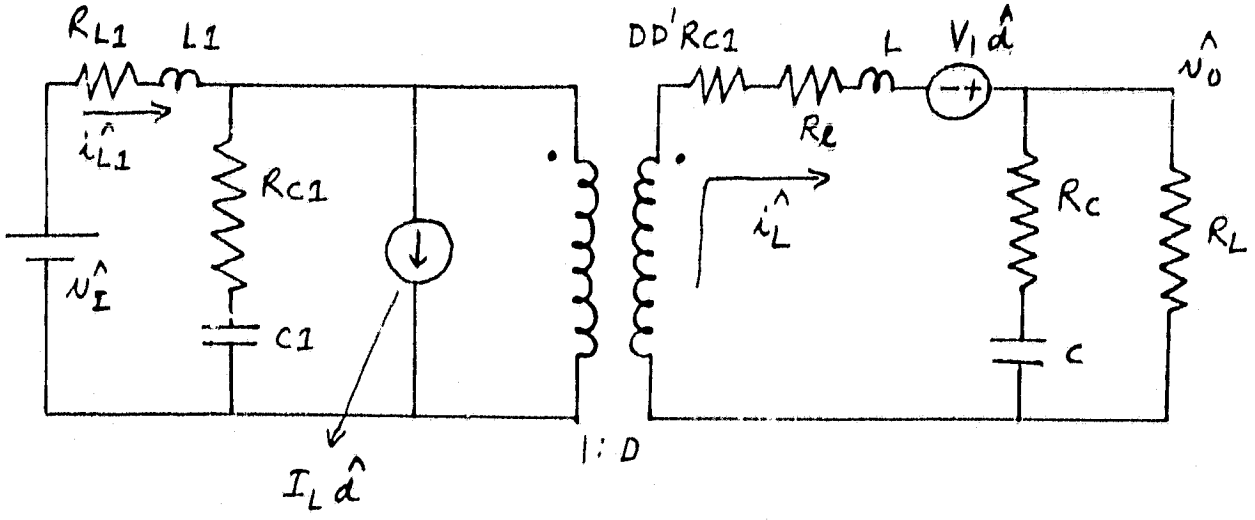


Fig. 5.9. Buck converter power stage small signal state space model.



$$V_1 = V_{C1} - D'R_{C1}I_L + R_{C1}I_{L1}$$

Fig. 5.10. Buck converter power stage small signal equivalent circuit.

$$\hat{v_I} = (R_{L1} + R_{C1})\hat{i_{L1}} - DR_{C1}\,\hat{i_L} + L1\,\frac{d\hat{i_{L1}}}{dt} + \hat{v_{C1}} - R_{C1}I_L\hat{d} \tag{5-60}$$

$$D\hat{v_{C1}} = (DR_{C1} + R_\ell)\hat{i_L} - DR_{C1}\hat{i_{L1}} + \hat{v_O} + L\,\frac{d\hat{i_L}}{dt} - (R_{C1}I_{L1} - R_{C1}I_L + V_{C1})\hat{d} \tag{5-61}$$

$$C1\frac{d\hat{v_{C1}}}{dt} = \hat{i_{L1}} - D\hat{i_L} - \hat{d}I_L \tag{5-62}$$

$$C\,\frac{d\hat{v_C}}{dt} = \hat{i_L} - \frac{\hat{v_O}}{R_L} \tag{5-63}$$

The small signal equivalent circuit is described by the four equations above, as in the buck-boost converter, and is shown in Fig. 5.10.

5.3 Boost converter small signal model derivation

The procedure used in deriving the small signal model for the boost converter is exactly similar to that used for the buck-boost converter. The boost converter is shown in Fig. 5.11.

During T_{ON}, the switch S is on, and the resulting circuit is shown in Fig. 5.12.

The equations describing the circuit are

$$\frac{di_{L1}}{dt} = \frac{-(R_{L1} + R_{C1})}{L1}\,i_{L1} + \frac{R_{C1}}{L1}\,i_L - \frac{v_{C1}}{L1} + \frac{v_I}{L1} \tag{5-64}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C1} - \frac{i_L}{C1} \tag{5-65}$$

$$\frac{di_L}{dt} = \frac{R_{C1}}{L}\,i_{L1} - \frac{(R_{C1} + R_\ell)}{L}\,i_L + \frac{v_{C1}}{L} \tag{5-66}$$

$$\frac{dv_C}{dt} = \frac{-v_C}{C(R_C + R_L)} \tag{5-67}$$

$$v_O = \frac{v_C R_L}{R_C + R_L} \tag{5-68}$$

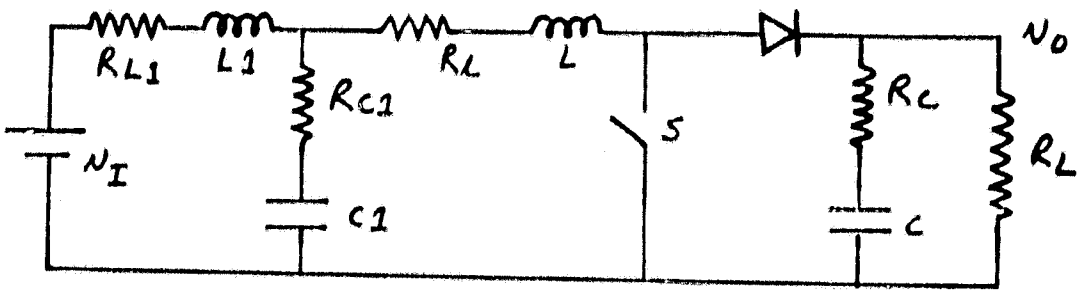


Fig. 5.11. Boost converter power stage.

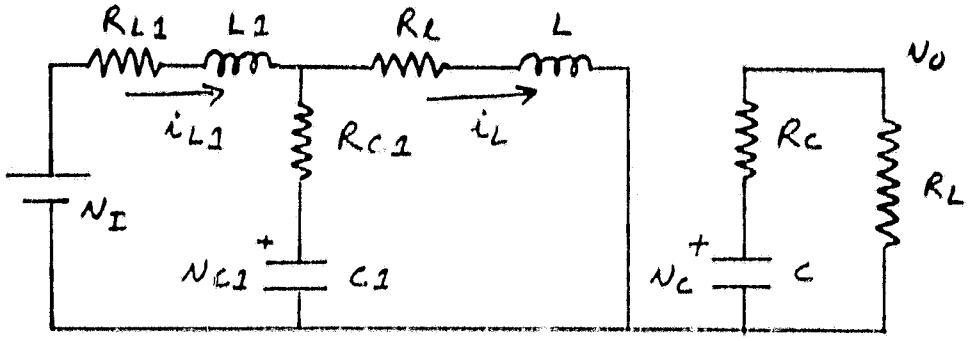


Fig. 5.12. Boost converter power stage model during T_{ON}.

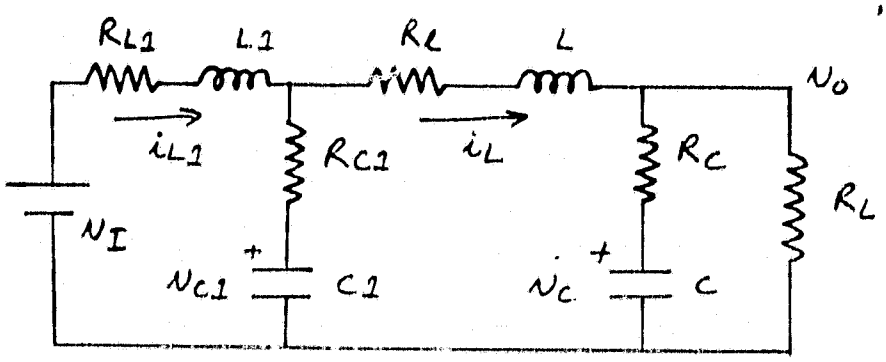


Fig. 5.13. Boost converter power stage model during T_{OFF}.

During T_{OFF} the switch S is off and the resulting circuit is shown in Fig. 5.13.

The equations describing the circuit are

$$\frac{di_{L1}}{dt} = \frac{-(R_{L1} + R_{C1})}{L1} i_{L1} + \frac{R_{C1}}{L1} i_L - \frac{v_{C1}}{L1} + \frac{V_I}{L1} \tag{5-69}$$

$$\frac{dv_{C1}}{dt} = \frac{i_{L1}}{C1} - \frac{i_L}{C1} \tag{5-70}$$

$$\frac{di_L}{dt} = \frac{R_{C1}}{L} i_{L1} - \frac{i_L}{L}\left(R_{C1} + R_\ell + \frac{R_C R_L}{R_C + R_L}\right) - \frac{R_L v_C}{L(R_C + R_L)} + \frac{v_{C1}}{L} \tag{5-71}$$

$$\frac{dv_C}{dt} = \frac{R_L i_L}{C(R_C + R_L)} - \frac{v_C}{C(R_C + R_L)} \tag{5-72}$$

$$v_O = \frac{R_C R_L}{R_C + R_L} i_L + \frac{R_L v_C}{R_C + R_L} \tag{5-73}$$

The following vectors are defined

$$\underline{x} = \begin{bmatrix} i_{L1} \\ i_L \\ v_{C1} \\ v_C \end{bmatrix} \qquad \underline{u} = [v_I] \qquad \underline{y} = [v_O] \tag{5-74}$$

resulting in the following state space equations.

T_{ON}	T_{OFF}	
$\dot{\underline{x}} = A_1\underline{x} + B_1\underline{u}$	$\dot{\underline{x}} = A_2\underline{x} + B_2\underline{u}$	(5-75)
$\underline{y} = C_1\underline{x}$	$\underline{y} = C_2\underline{x}$	

where

$$A_1 = \begin{bmatrix} \frac{-(R_{L1}+R_{C1})}{L1} & \frac{R_{C1}}{L1} & \frac{-1}{L1} & 0 \\ \frac{R_{C1}}{L} & \frac{-(R_{C1}+R_\ell)}{L} & \frac{1}{L} & 0 \\ \frac{1}{C1} & \frac{-1}{C1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix} \tag{5-76}$$

$$A_2 = \begin{bmatrix} \frac{-(R_{L1}+R_{C1})}{L1} & \frac{R_{C1}}{L1} & \frac{-1}{L1} & 0 \\ \frac{R_{C1}}{L} & \frac{-R_1}{L} & \frac{1}{L} & \frac{-R_L}{L(R_C+R_L)} \\ \frac{1}{C1} & \frac{-1}{C1} & 0 & 0 \\ 0 & \frac{R_L}{C(R_C+R_L)} & 0 & \frac{-1}{C(R_C+R_L)} \end{bmatrix} \tag{5-77}$$

$$R_1 = R_{C1} + R_\ell + \frac{R_C R_L}{R_C+R_L} \tag{5-78}$$

$$B_1 = \begin{bmatrix} \frac{1}{L1} & 0 & 0 & 0 \end{bmatrix}^T \tag{5-79}$$

$$B_2 = B_1 \tag{5-80}$$

$$C_1 = \begin{bmatrix} 0 & 0 & 0 & \frac{R_L}{R_C+R_L} \end{bmatrix} \tag{5-81}$$

$$C_2 = \begin{bmatrix} 0 & \frac{R_L R_C}{R_L+R_C} & 0 & \frac{R_L}{R_C+R_L} \end{bmatrix} \tag{5-82}$$

The state space averaged model over the entire period T is

$$\dot{\underline{x}} = [dA_1 + d'A_2]\underline{x} + [dB_1 + d'B_2]\underline{u} \tag{5-83}$$

$$\underline{y} = [dC_1 + d'C_2]\underline{x}$$

where d = duty cycle ratio $= \dfrac{T_{ON}}{T_{OFF} + T_{ON}}$

$$d' = 1 - d \tag{5-84}$$

$$T = T_{ON} + T_{OFF}$$

The state space averaged model is perturbed and linearized in exactly the same way as for the buck-boost converter. The resulting small signal linearized model is

$$\underline{0} = A\,\underline{X} + B\,V_I$$

$$\dot{\hat{\underline{x}}} = A\,\hat{\underline{x}} + B\,\hat{v_I} + [(A_1 - A_2)\,\underline{X} + (B_1 - B_2)V_I]\hat{d} \tag{5-85}$$

$$V_0 = C\,\underline{X} \tag{5-86}$$

$$\hat{v_0} = [C_1 - C_2]\,\underline{X}\,\hat{d} + C\,\hat{\underline{x}} \tag{5-87}$$

where $A = DA_1 + D'A_2$

$$B = DB_1 + D'B_2 \tag{5-88}$$

$$C = DC_1 + D'C_2$$

Using Laplace transforms gives

$$\hat{\underline{x}}(s) = [SI - A]^{-1}\,B\,\hat{v_I}(s) + [SI - A]^{-1}[(A_1 - A_2)\underline{X} + (B_1 - B_2)V_I]\hat{d}(s) \tag{5-89}$$

$$\hat{v_0}(s) = [C_1 - C_2]\underline{X}\,\hat{d}(s) + C\hat{\underline{x}}(s)$$

The state space model is derived from the above two equations and is shown in Fig. 5.14.

The procedure for deriving the small signal equivalent circuit is exactly similar to the one used for the buck-boost converter. The four equations that result are -

$$L1\frac{d\hat{i}_{L1}}{dt} = -(R_{L1}+R_{C1})\hat{i}_{L1} + R_{C1}\hat{i}_L - \hat{v}_{C1} + \hat{v}_I \tag{5-90}$$

$$L\frac{d\hat{i}_L}{dt} = R_{C1}\hat{i}_{L1} - (R_{C1}+R_\ell)\hat{i}_L - DD'\frac{R_C R_L}{R_C+R_L}\hat{i}_L \tag{5-91}$$

$$+ \hat{v}_{C1} - D'\hat{v}_0 + \frac{R_C R_L I_L \hat{d}(D-D')}{R_C+R_L} + V_0\hat{d}$$

$$C_1\frac{d\hat{v}_{C1}}{dt} = \hat{i}_{L1} - \hat{i}_L \tag{5-92}$$

$$C\frac{d\hat{v}_C}{dt} = D'\hat{i}_L - \frac{\hat{v}_0}{R_L} - I_L\hat{d} \tag{5-93}$$

The small signal equivalent circuit is described by the four equations above as in the buck-boost converter, and is shown in Fig. 5.15.

The power stage small signal models developed include the input filter state variables, whereas earlier models [2,4,5] had treated the input filter only in terms of its output impedance and transfer function. The models developed in this chapter are used to analyze and design a feedforward loop that includes the input filter state variables.

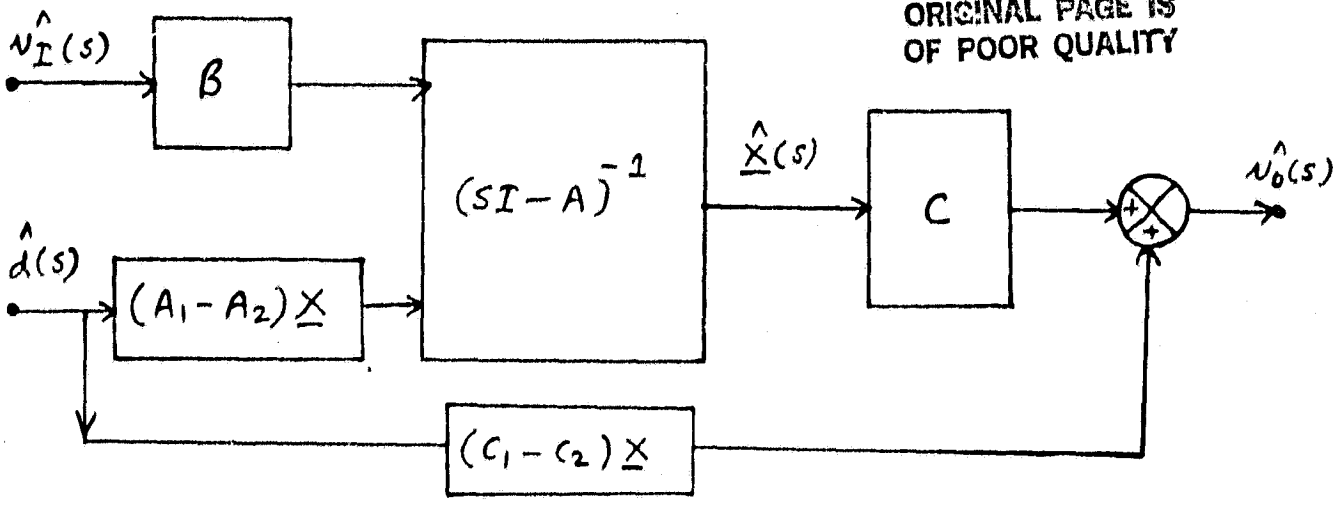
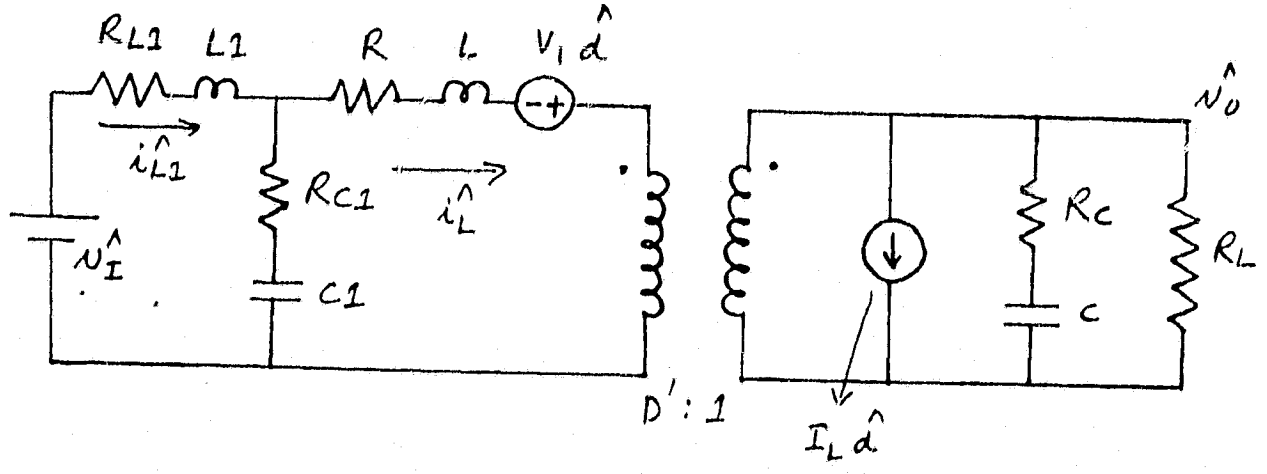


Fig. 5.14. Boost converter power stage small signal state space model.



$$R = R_\ell + \frac{DD'R_CR_L}{R_C + R_L}$$

$$V_L = V_O + \frac{R_CR_LI_L(D-D')}{R_C + R_L}$$

Fig. 5.15. Boost converter power stage small signal equivalent circuit.

VI. ANALYSIS OF FEEDFORWARD LOOPS LEADING TO A DESIGN OF THE FEEDFORWARD LOOPS FOR A BUCK REGULATOR.

This chapter presents an analysis that leads to a design of the feedforward loops for a buck regulator. A small signal model that includes the feedforward loops is developed; analysis of the model leads to a design of the feedforward loops. The buck regulator is treated in this chapter, but the analysis and design procedure would be similar for the boost and the buck-boost converters.

6.1 Development of a small signal model that includes the feedforward loops.

The small signal model to study the behavior of the feedforward loops was developed in two steps - in the first step and output voltage to duty cycle transfer function was developed, and in the second step the above transfer function was used to develop a model that includes the feedforward loops.

The small signal equivalent circuit model of the buck converter described earlier was used to relate $\hat{d}(s)$ to $\hat{v_0}(s)$, with the input $\hat{v_I}(s)$ set equal to zero. Fig. 6.1 shows the circuit used. Expressions for $\hat{i_1}(s)$ and $\hat{v_2}(s)$ were written and used to relate $\hat{d}(s)$ to $\hat{v_0}(s)$. The transfer function developed is -

$$\frac{\hat{v_0}(s)}{\hat{d}(s)} = \frac{V_0}{D} \frac{(R_L - D^2Z)(1+SCR_C)}{D^2Z(1+SCR_L)+LCR_L(s^2+aS+b)} \qquad (6\text{-}1)$$

where

$$a = \frac{1}{CR_L} + \frac{DD'R_{C1}+R_\ell+R_C}{L} \qquad (6\text{-}2)$$

$$b = \frac{1}{LC} \qquad (6\text{-}3)$$

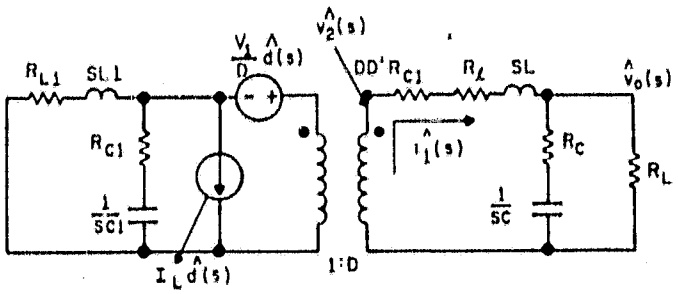


Fig. 6.1. Small signal equivalent circuit of the buck converter power stage with $\hat{v_I}(s) = 0$

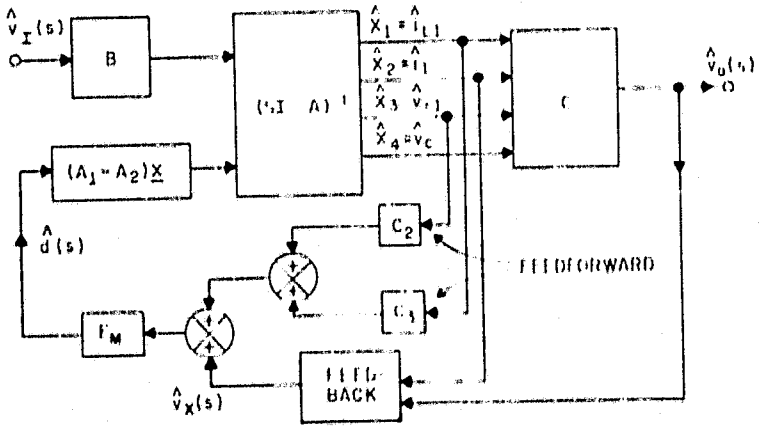


Fig. 6.2. Buck converter model with feedforward and feedback loops.

$$Z = (R_{L1} + SL1)//(R_{C1} + \frac{1}{SC1}) \quad (6\text{-}4)$$

= output impedance of input filter

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = F_p(s)$$ where $F_p(s)$ is the output voltage to duty cycle transfer function. (6-5)

The state space model for the complete buck converter including the feedforward and feedback loops is shown in Fig. 6.2, where $C_2(s)$ and $C_3(s)$ are the gains of the feedforward loops. The design of the feedforward consists of choosing appropriate gain expressions.

To examine the behavior of the feedforward loops $\hat{v}_I(s)$ is set equal to 0 and $\hat{v}_x(s)$ is related to $\hat{v}_0(s)$. F_M is the transfer function of the pulse modulator.

$F_M(s) = (2R_4C_1/n)(1/M)$ as developed in (6).

The equations needed are

$$[\hat{v}_x(s) + C_3(s)\hat{i}_{L1}(s) + C_2(s)\hat{v}_{C1}(s)]F_M = \hat{d}(s) \quad (6\text{-}6)$$

$$F_p(s)\hat{d}(s) = \hat{v}_0(s) \quad (6\text{-}7)$$

where it is assumed that the feedforward signal made available to the pulse modulator is $C_3(s)\hat{i}_{L1}(s) + C_2(s)\hat{v}_{C1}(s)$ and $F_p(s)$ is the output voltage to duty cycle transfer function developed above.

Using the equation

$$(SI - A)\hat{x}(s) = (A_1 - A_2)\underline{X}\hat{d}(s) \quad (6\text{-}8)$$

it is possible to relate $\hat{i}_{L1}(s)$ and $\hat{v}_{C1}(s)$ to $\hat{d}(s)$.

The result is

$$C_3(s)\hat{i}_{L1}(s) + C_2(s)\hat{v}_{C1}(s) = F_F(s)\hat{d}(s) \quad (6\text{-}9)$$

where

$$F_F(s) = \frac{V_0\{[(1+SCR_L)(SL+R_L)+R_L][C_3(S)+SC1R_{C1}C_3(S)-C_2(S)SL1-C_2(S)R_{L1}]\}}{R_L[a_1(s)b_1(s) + D^2(1+SCR_L)(SL1+R_{L1})]} \quad (6\text{-}10)$$

and $$a_1(s) = R_L(S^2LC + SCR_\ell + SCR_C + 1) + SL \quad (6\text{-}11)$$

$$b_1(s) = S^2L1C1 + SC1(R_{C1}+R_{L1}) + 1 \quad (6\text{-}12)$$

substitution gives the following

$$[\hat{v_x}(s) + F_F(s)\hat{d}(s)]F_M = \hat{d}(s)$$

$$\hat{v_x}(s)F_M = \hat{d}(s)[1 - F_F(s)F_M] \quad (6\text{-}13)$$

$$= \frac{\hat{v_0}(s)}{F_P(s)}[1 - F_F(s)F_M]$$

$$\frac{\hat{v_0}(s)}{\hat{v_x}(s)} = \frac{F_P(s)F_M}{1 - F_F(s)F_M} . \quad (6\text{-}14)$$

The small signal model developed, equation (6-14), includes the effect of the feedforward loops as is seen clearly in (6-10).

It is easier to analyze the effect of feedforward if the following assumption is made -

$$R_{C1} = 0 \quad (6\text{-}15)$$

This is not an unrealistic assumption since the ESR of the input filter capacitor can be assumed negligibly small compared with the other resistances. Assumption (6-15) lends to the following simplified expressions -

$$F_p(s) = \frac{V_0(R_L - D^2Z)(1+SCR_C)}{D\left\{\frac{D^2(1+SCR_L)(SL1+RL1)}{b_1(s)} + a_1(s)\right\}} \quad (6\text{-}16)$$

$$Z = \frac{SL1 + R_{L1}}{b_1(s)} = \text{Output impedance of input filter} \quad (6\text{-}17)$$

$$a_1(s) = R_L(S^2LC + SCR_\ell + SCR_C + 1) + SL \qquad (6\text{-}18)$$

$$b_1(s) = S^2L_1C_1 + SC_1R_{L1} + 1 \qquad (6\text{-}19)$$

Substitution of (6-16), (6-17), (6-18) and (6-19) into (6-14) leads to the following simplified small signal model -

$$\frac{\hat{v_0}(s)}{\hat{v_x}(s)} = \frac{V_0F_Mb_1(s)(R_L - D^2Z)(1+SCR_C)R_L}{DN_1(s)} \qquad (6\text{-}20)$$

where

$$N_1(s) = R_L[\{a_1(s)b_1(s) + D^2(1+SCR_L)(SL1+RL1)\}] -$$

$$V_0F_M[\{(1+SCR_L)(SL+R_L) + R_L\}\{C_3(s) - C_2(s)R_{L1} - C_2(s)SL1\}] \qquad (6\text{-}21)$$

The simplified small signal model of equation (6-20) and (6-21) reveals, using equation (6-17), that the output impedance of the input filter Z(s) affects both the numerator and denominator of the simplified model. In equation (6-21) the gains of the feedforward loops are $C_2(s)$ and $C_3(s)$ and it is seen that if appropriate gain expressions are chosen such that the numberator and denominator terms containing Z(s) in (6-20) are cancelled, then the addition of feedforward effectively results in eliminating the peaking effect of Z(s) on the loop gain and phase.

6.2 Design of the feedforward loops

The design of the feedforward loops thus reduces to choosing appropriate gain expressions for the gain blocks in the feedforward loops.

It is seen that choosing

$$C_3(s) = 0 \qquad (6\text{-}22)$$

and

$$C_2(s) = \frac{-D^2}{V_0 F_M} \tag{6-23}$$

leads to

$$\frac{\hat{v_0}(s)}{\hat{v_x}(s)} = \frac{V_0 F_M b_1(s)(R_L - D^2 Z)(1 + SCR_C)R_L}{Da_1(s)b_1(s)(R_L - D^2 Z)} \tag{6-24}$$

Simplifying leads to

$$\frac{\hat{v_0}(s)}{\hat{v_x}(s)} = \frac{V_0 F_M R_L (1 + SCR_C)}{Da_1(s)} \tag{6-25}$$

Equation (6-25) reveals that for the case of a buck regulator operating in the continuous conduction mode, only one feedforward loop is necessary and that the gain of the feedforward loop is a constant. The peaking effect of the output impedance of the input filter Z(s) is completely eliminated as is evident from a comparison of equations (6-25) and (6-20). The transfer function of equation (6-25) is exactly the one obtained if there is no input filter in the power stage; thus the effect of the input filter is completely eliminated.

VII. POSSIBLE IMPLEMENTATION OF THE PROPOSED FEEDFORWARD LOOP DESIGN

The proposed feedforward loop design is to be implemented for constant volt-sec control. As developed in the last section, the feedforward loop need only sense the input filter capacitor voltage and the gain of the feedforward circuit is

$$C_2(s) = \frac{-D^2}{V_0 F_M} \tag{7-1}$$

With constant volt-sec control the product of input voltage and the on time of the converter is constant. The gain of the feedforward circuit will therefore be a constant.
Substituting for F_M from [2] and for D leads to

$$C_2(s) = \frac{-V_0 n\, T_{ON}}{2V_I\, R_4 C_1'} \tag{7-2}$$

or
$$C_2(s) = \frac{-V_0\, n\, M}{2V_I^{\,2}\, R_4 C_1'} \tag{7-3}$$

where $M = V_I\, T_{ON}$ is constant.

and V_0 = output voltage

V_I = input voltage

R_4, C_1' = control circuit parameters

n = turns ratio of the inductor current sensing transformer

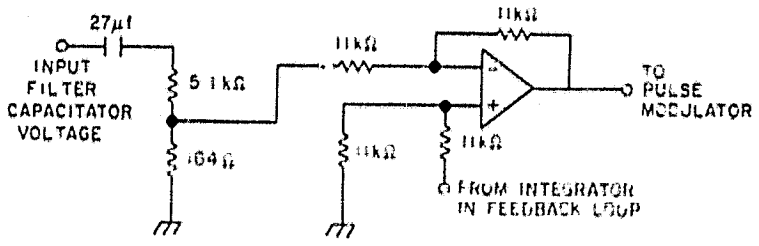


Fig. 7.1. Feedforward circuit for a buck converter with constant input voltage.

As an example a feedforward circuit is designed for the following values:

$V_0 = 20$ V

$V_I = 30$ V

$n = 0.65$

$R_4 = 40.7$ KΩ

$C_1' = 5600$ pf

$M = 0.88 \times 10^{-3}$ V-sec

The gain of the feedforward loop is calculated as $G_2(s) = -0.03$. Figure 7.1 is a possible implementation of the feedforward gain. The input to the circuit is the input filter capacitor voltage and a series capacitor of 27 μF is necessary to filter out the dc component of the capacitor voltage. The gain of 0.03 is implemented by the potential divider made up of the 5.1 KΩ and 164 Ω resistances. The input voltage to the circuit is multiplied by the gain and then subtracted from the feedback signal generated at the output of the integrator in the feedback loop.

VIII. CONCLUSIONS AND FUTURE WORK

In switching regulators the peaking of the output impedance of the input filter interacts with the regulator control loop, and this in turn could result in degradation of regulator performances and possible loop instability. An approach based on pole-zero cancellation is proposed to mitigate these detrimental effects. It is shown analytically that a feedforward loop can be designed that eliminates the peaking effect of the output impedance.

The design of the proposed feedforward loop for a buck regulator proceeded in three steps. First the small signal model of a buck regulator power stage with continuous inductor current operation is derived. Similar small signal models for the boost and buck-boost regulator power stages are also derived. These models preserve the original properties of the input-filter/output filter state variables. The next step is to develop a small signal model for the buck regulator including the feedforward and feedback loops; this is done using the power stage models derived earlier. The model includes the effect of feedforward loops and is examined next to see if pole-zero cancellation to control the peaking effect of the input filter output impedance is possible. It is shown in this report that a simple choice of feedforward loop gains results in complete cancellation of the peaking effect. The transfer function obtained with feedforward compensation is exactly the one that would be obtained if there is no input filter used; thus the feedforward results in cancelling the

interaction between the output impedance of the input filter and the regulator control loop. A possible implementation of the proposed feedforward is presented.

Future work will involve implementation of the proposed feedforward compensation and measurement of the open loop gain and phase of the buck regulator to confirm the analytical prediction and design. The closed loop input-to-output transfer function will also be examined to check the effect of feedforward on audiosusceptibility.

The implementation of input filter compensation scheme is currently under investigation under NASA contract NAS 3-220 by investigators Fred C. Lee and S. S. Kelkar of Virginia Polytechnic Institute and State University.

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