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EVALUATION AND VERIFICATION OF EPITAXIAL PROCESS SEQUENCE FOR SILICON SOLAR-CELL PRODUCTION

D. Redfield
RCA Laboratories
Princeton, New Jersey 08540

FINAL PROGRAM SUMMARY REPORT

NOVEMBER 1981

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The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low cost solar arrays.

Prepared under Contract No. 955825 for

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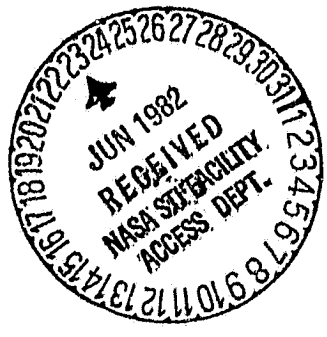
Pasadena, California 91103



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PREFACE

This Final Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from January 29, 1981 to August 5, 1981 in the Energy Systems Research Laboratory, Dr. B. F Williams, Acting Director. The Project Scientist was Dr. D. Redfield, and the Project Supervisor was Dr. A. H. Firester, Head, Process and Applications Research. Dr. R. V. D'Aiello also participated in the research (cell processing) for this report.

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SECTION I

GOALS AND OBJECTIVES

The goal of this program was to evaluate the applicability of previously developed solar-cell and module-processing sequences developed for single-crystal silicon under the sponsorship of the LSA Project for use on lower-cost epitaxial silicon wafers. These process sequences have been shown to be of potentially low cost and to perform effectively when applied to the high-quality silicon crystals for which they were developed. The present program was intended to verify the extent to which such process sequences can also perform effectively when applied to lower-cost thin-film solar cells formed by epitaxial deposition of Si on potentially inexpensive substrates of upgraded-metallurgical grade (UMG) Si. Therefore, maximum use was made of process steps developed under the LSA Project, and of epitaxial Si wafer development being performed at RCA Laboratories under the concurrent SERI Exploratory Development program.

Because of the premature termination of this contract, the goals were not accomplished.

SECTION II

INTRODUCTION

To achieve the program goals, 28 minimodules were to have been fabricated and tested, using 600 cells made from three-inch-diameter wafers processed by the sequence chosen for this purpose. Of these 600 cells, half were to be made from epitaxially grown layers on potentially low-cost substrates. The other half were to be made from commercial semiconductor-grade (SG), single-crystal silicon wafers that served as controls. Cell processing was normally performed on mixed lots containing significant numbers of each of these two types of wafers. After evaluation of the performance of all cells, they were separated by types for incorporation into modules that were to be tested for electrical performance and response to environmental stress. A simplified flow chart displaying this scheme, for quantities representing half of the planned total to be processed, is shown in Fig. 1.

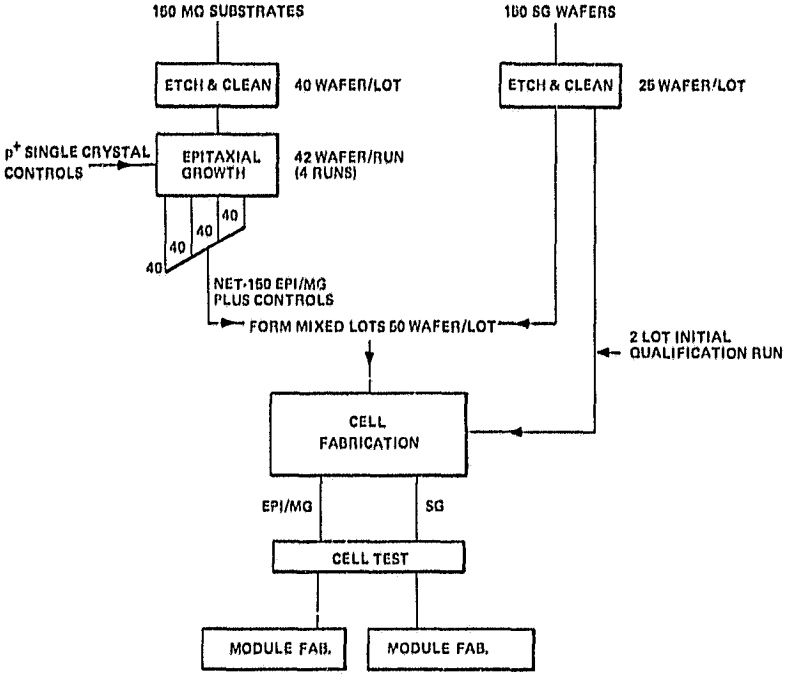

Figure 1. Processing flow chart.

Documentation of the specifications and procedures of all process steps chosen for this program, and detailed SAMICS cost analyses have been provided in separate reports bearing those titles. As with all R&D projects, however, there are unavoidable differences between some of the laboratory processes used to fabricate cells and modules for the present evaluations and the analogous processes as they would take place in a factory at high production rates. In all cases where uncertainties may exist in specific process steps, the materials or procedures used were consistent with developments occurring under either the LSA program or the Exploratory Development (ED) contract that RCA was conducting for SERI [1]. In this report, some information is provided on relevant work under the ED program.

1. "Exploratory Development of Thin-Film Polycrystalline Photovoltaic Devices," Solar Energy Research Institute Contract XS-09100-3.

SECTION III

DATA AND RESULTS

Progress, present status, and data are presented by tasks defined in the contract.

A. TASK 1: SILICON SUBSTRATE MATERIALS

1. Epitaxial Substrates

Because low-cost substrates for epitaxial growth of Si are still under development, their properties are not yet thoroughly established. Indeed, there are substantial variations in the properties of substrate materials from different suppliers. RCA has used a variety of such substrates and has chosen for its epitaxial programs materials that are basically UMG-Si (all p-type) as being most promising for meeting both the cost and performance goals of the Exploratory Development contract [1]. The specific type that seemed most promising was the heat-exchanger-method (HEM) Si that is made in large ingots by Crystal Systems, Inc. Therefore, use of that material was planned in this program as well.

Extensive chemical analysis of HEM material has shown that its purity benefits substantially from segregation of impurities during the slow directional solidification. For aluminum, which is always a high-concentration impurity, the results indicate that the quantitative amount of purification is close to that which would be expected from the value of the equilibrium segregation coefficient. If that were also true of the transition metals, which have very low segregation coefficients, it would lead to exceedingly low concentrations of them in the HEM wafers. That would explain the success of these wafers as epitaxial substrates, in that the epi layers are quite free of lifetime killers. However, present evidence is that carbon does not segregate in HEM at the equilibrium rate. That could be because carbon in Si is rather special, or it may be that a number of elements do not follow their equilibrium behavior in the HEM process.

For several reasons, it was decided to use two types of substrate materials in this program. One reason was uncertainty regarding the timely availability of enough HEM substrates. A second reason was the continuing difficulty that had been experienced in the early portion SERI Exploratory Development program

with particulate inclusions in HEM material. Inclusions occurred commonly in those wafers and have been identified as the cause of low fill factors in large-area cells that cannot exclude them.

Recent evaluation of various HEM materials by the ED epitaxial program [1], however, produced two major findings: (1) that the use of well-selected MG feedstock can provide substantial improvement in solar-cell properties; and (2) that double solidification can improve the material further, provided much of the particle-containing top is removed after the first solidification. The performance of epitaxial solar cells made on substrates of these improved HEM wafers has been quite good.

Chemical analyses show that the particles in HEM material that cause poor solar-cell properties seem to be of two types: predominantly iron or predominantly carbon. Regardless of type, however, recent experiments by Crystal Systems, Inc. have shown that the number of harmful particles can be greatly reduced by simply increasing the lateral dimensions of the ingot. This result further improves the prospects for use of HEM substrates in epitaxial solar cells.

A number of cells of various sizes were made on epitaxial wafers whose HEM substrates were solidified twice by the use of South African metallurgical-grade-silicon (MG-Si) feedstock. The numbers of particulate inclusions in these substrates are much lower than in previous HEM substrates, for which other feedstocks were used, and the cell performances are correspondingly better. For 20-cm^2 cells with evaporated metals, efficiencies of more than 10% have been obtained with good yields. Also on these substrates, cells of 4.5-cm^2 area with screen-printed metals displayed equally good efficiencies. Cells of larger sizes are now being processed on these materials. There appear to be good prospects for finding alternative sources of better-quality MG-Si in the United States and for avoiding the need for a second HEM solidification.

The second material chosen for substrates was UMG from Hemlock Semiconductor Corp. (a subsidiary of Dow-Corning Co.). Considerable experience at RCA with such substrates had shown these to be satisfactory for the present purposes, and they were available to us immediately in sufficient quantity (viz., 150). However, analyses of results described under Task 2 showed that there is reason to suspect the presence of a few harmful inclusions in some of these wafers as well. Close visual examination has indeed revealed some particles that had not previously been found. Thus, this may be a generic problem to UMG materials.

Spectroscopic analysis of the impurity content of these Dow-Corning wafers and the electrical resistivities had previously been measured [2]. Although the impurity content is somewhat variable, the resistivities are quite uniform at 0.01 Ω·cm.

Also purchased for this program were 50 three-inch-diameter wafers of p^+ CZ silicon for use as control substrates for epitaxial growth. These were to be employed in the as-sawed condition to resemble the UMG wafers, which were unpolished. The same etching treatment was used for these controls and UMG materials in preparation for epi growth.

2. Epitaxial Growth

Preparation of as-sawed wafers for use as epi substrates consisted only of etching 2 mils off each side of all wafers in batches of 25 in an NBK Model SW-100 Etching Apparatus that had just been tested and put into use here for the first time. The etch takes two minutes in a solution of buffered HF/HNO_3. Following rinsing, the wafers are subjected to a Megasonic cleaning just before placement in the epi reactor. Later experience, described below, caused a switch to NaOH.

All epi growths for this program were done in RCA's high-throughput reactor (HTR) which can process a batch of about 40 wafers at a time with quite good uniformity. On the basis of considerable experience with epitaxially made solar cells, a doping profile such as shown in Fig. 2 was chosen. Not only does such a profile make economical use of the high-quality Si in the epi layer (since that layer is only about 20 μm thick), but it also produces naturally a "back-surface field." This field exists as a consequence of the difference in resistivity between the front and the substrate. It can also be easily tailored to provide a wide range of doping gradients in the transition region. Moreover, the high conductivity of the substrates eases problems of making good electrical contact to the back of the cell. Another factor of major importance is that epi growth (at about 1100°C) can produce a layer whose carrier lifetimes are adequate. Thus, there is not a serious problem of contamination by the UMG substrate.

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2. R. V. D'Aiello and P. H. Robinson, "Low-Cost Epitaxial Techniques for Solar-Cell Fabrication," Final Report, SERI/PR-0-8274-4, November 1980, Subcontract No. XS-9-8274.

The HTR received several improvements before this program began. The entire gas-handling system was revised with improved components, and the hydrogen gas that is used in quantity as a carrier gas is now supplied from a liquid-hydrogen tank rather than from ordinary cylinders. This enhances the hydrogen purity.

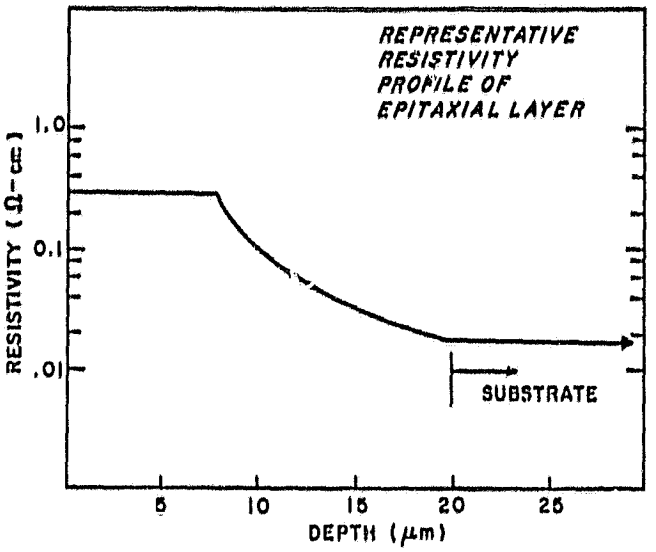

Figure 2. Representative resistivity of epitaxial layer.

In three epitaxial-growth runs performed in the high-throughput reactor, 52 Dow-Corning UMG wafers and seven single-crystal CZ control wafers had epi layers grown. The resistivity profiles all were similar to that shown in Fig. 2; the layer thicknesses were 28 μm for run 39, 19 μm for run 40, and 24 μm for run 41.

All substrates were etched before growth in the manner described above. However, on the basis of subsequent results, there is reason to doubt that the amount of material removed in this way was as great as desired. This etching is intended to remove saw damage on the UMG wafers, which are neither lapped nor polished. Because saw damage can propagate through an epi layer, this removal is essential for the production of good solar cells. Experience has shown that 2 mils should be removed this way from each sawn surface to achieve the necessary quality. The use of the new batch etching machine and imprecise

thickness measurements may have resulted in uncertain values for the thickness removed.

As part of the effort to check on the possible presence of residual saw damage at the surfaces of UMG substrates, a series of x-ray topographs were made. These reveal strain patterns in the Si, whether they are caused by isolated dislocations, misfit at epitaxial interfaces, or saw damage. Figure 3 shows three portions of a section topograph of an epi/UMG wafer from epi run 40. The dark band on the right side is the epi layer that contains many misfit dislocations caused by nonuniform doping; their presence is verified by projection topographs. The dots throughout the thickness of the substrate are dislocations and other strain-inducing defects. Along the left surface are numerous dark regions -- more than the bulk density can explain -- that appear to be remnants of saw damage. Therefore, it appears fair to infer that similar damage existed on the other surface where the epi layer is grown. If insufficient removal of saw damage did occur, then we should expect that all of the properties (J_{sc}, V_{oc}, FF) of the eventual cells would be harmed. As discussed in the next section, another closely related effect may be simultaneously affecting the FF.

B. TASK 2: PROCESS SEQUENCE DETERMINATION

The process sequence chosen for this program is characterized in broad terms by $POCl_3$ junction diffusion, thick-film screen-printed Ag front grid, thick-film aluminum back contact, and sprayed-on antireflection coating. Details have been presented in the "Process Development Plan" submitted as a separate report. A graphical summary of this sequence appears in Fig. 4.

Of particular importance in this sequence are the screen-printed metallizations. Although promising for cost reduction, this technology is still under development. It is also desirable to eliminate the use of silver eventually, so future changes in this process are possible. The epitaxial cells provide a useful advantage for the back contact, regardless of contacting procedure, because of the high conductivity of all UMG epi substrates. It is generally easier to make good electrical contact to silicon of high conductivity than of low conductivity. This property of epi substrates was exploited by use of a simple aluminum ink that is fired briefly into the back of epi cells. A final pattern of screen-printed silver covers the Al (after thorough cleaning).

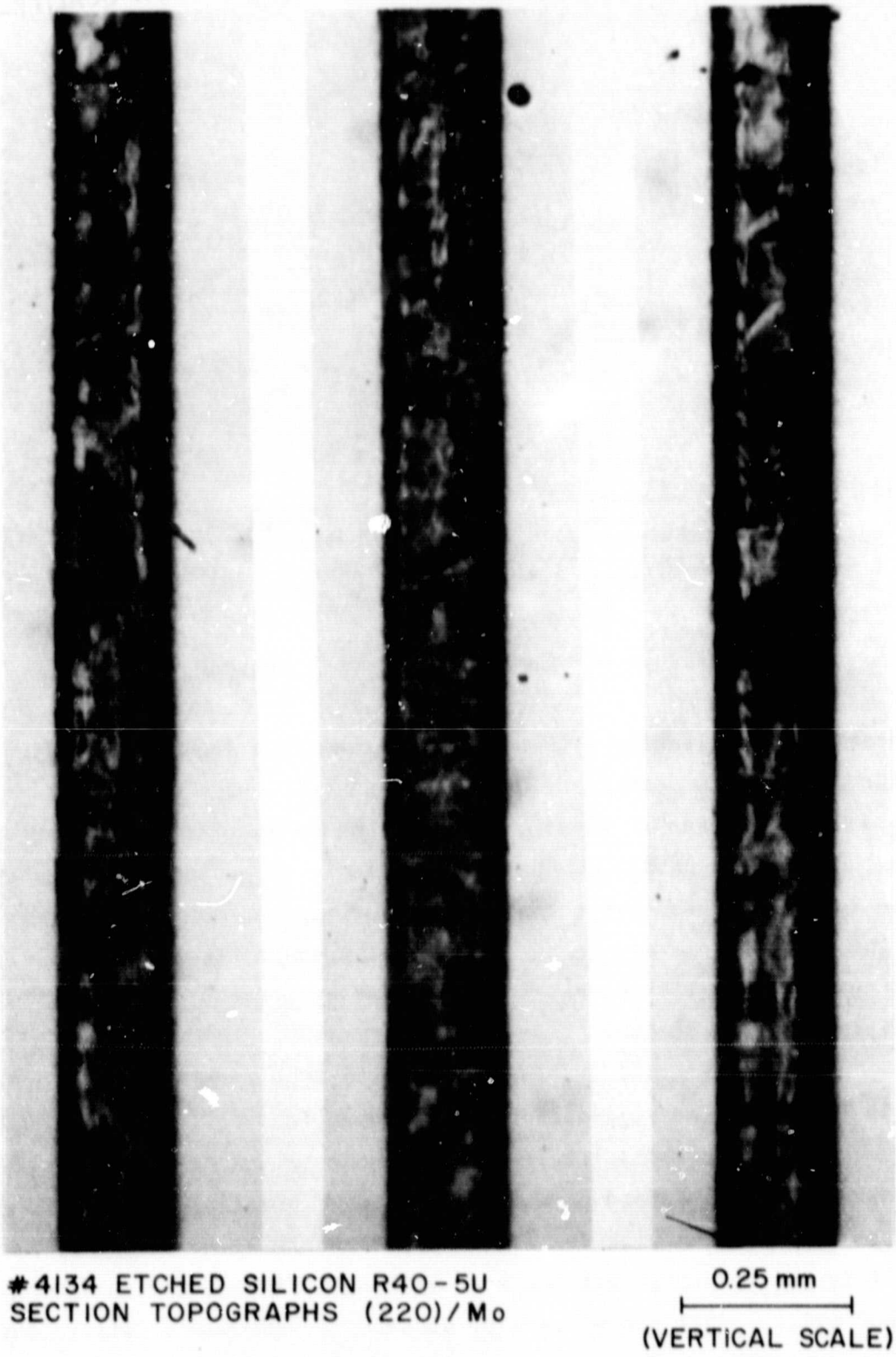

Figure 3. Section x-ray topographs of a Dow-Corning UMG wafer with an epitaxial layer about 20μm thick on the right-hand face. Dark regions are strained.

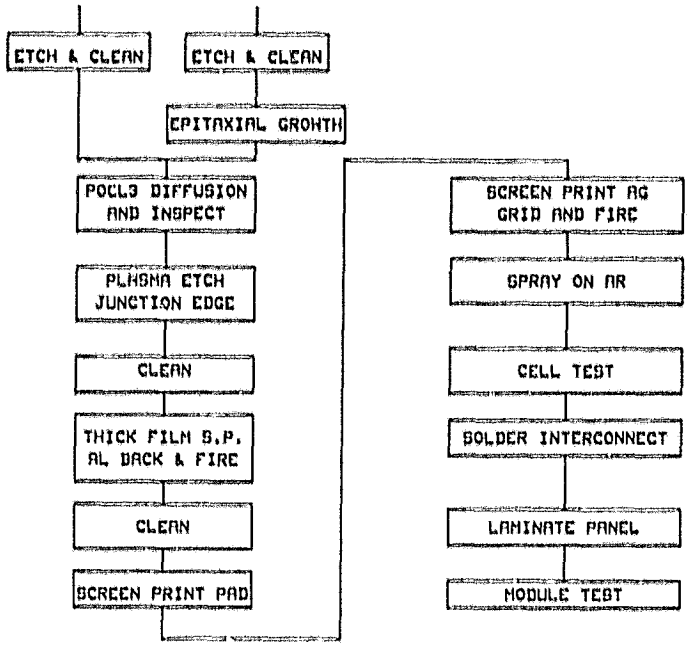

Figure 4. Summary of process sequence.

To develop familiarity with this cell-processing sequence in batches of full size, three lots containing only semiconductor-grade (SG) wafers (25 in each lot) were processed. These are designated by process lot numbers 1, 2 and 3, even though they contain no epi wafers. The cell-processing sequence was complete for these lots except that the AR coating was not applied. There is enough information to evaluate the electrical properties of such cells since a good AR coating normally increases the current by a factor of about 1.35, and the efficiency by about 1.4.

Values of V_{oc} and J_{sc} for the cells of the first two lots are presented in Table 1. Two significant facts emerge from Table 1: the currents are very good, and there is little spread in the values of both V_{oc} and J_{sc}. The mean values and standard deviations for these quantities are given in Table 2. There were problems with the fill factors that will be described next. First, it is worth noting that the mean values of Table 2 are characteristic of quite good cells. That can be seen by assuming a reasonable fill factor of 0.75 for use with V_{oc} = 0.56 and J_{sc} = 32 mA/cm^2 (including the factor of 1.35 for the effect of an AR coating). Together, these values lead to a mean efficiency of η = 13.4% (at 100 mW/cm^2 irradiance).

TABLE 1. CURRENTS AND VOLTAGES FOR PROCESS LOTS 1 AND 2

Cell No.	V_{oc} (Volt)	J_{sc} (mA/cm^2)
01P01S	0.559	23.64
01P02S	0.567	24.19
01P05S	0.560	24.34
01P06S	0.567	24.29
01P07S	0.563	23.02
01P08S	0.571	21.22
01P09S	0.563	{21.97 {22.29
01P11S	0.561	23.82
01P12S	0.558	24.42
01P13S	0.558	23.19
01P14S	0.567	21.69
01P15S	0.552	24.35
01P16S	0.562	22.09
01P17S	0.560	24.25
01P18S	0.562	23.67
01P19S	0.557	24.02
01P21S	0.555	24.33
01P22S	0.557	24.08
01P23S	0.553	22.69
01P24S	0.558	22.03
01P25S	0.557	23.42
02P01S	0.565	23.52
02P02S	0.562	24.34
02P03S	0.561	24.67
02P04S	0.561	24.89
02P07S	0.555	24.61
02P08S	0.559	24.65
02P09S	0.559	24.79
02P10S	0.559	24.58
02P11S	0.559	24.86
02P12S	0.562	24.35
02P13S	0.558	24.25
02P14S	0.558	23.78
02P15S	0.570	24.60
02P16S	0.554	24.86
02P17S	0.558	24.10
02P18S	0.561	23.92
02P20S	0.557	24.42
02P21S	0.554	23.49
02P22S	0.547	23.87
02P23S	0.556	22.84

TABLE 2. MEAN VALUES AND STANDARD DEVIATIONS σ FOR V_{oc} AND J_{sc} IN LOTS 01 AND 02

Parameter	Lot 1	Lot 2
V_{oc}	0.560 V	0.559 V
σ_V	0.005	0.005
J_{sc}	23.3 mA/cm^2	24.3 mA/cm^2
σ_J	1.0	0.55
$1.35 \times J_{sc}$ [(a)]	31.5 mA/cm^2	32.8 mA/cm^2

(a) The normal effect of an AR coating is to increase J_{sc} by this factor.

The measured fill factors and, therefore, the efficiencies of all cells in lots 1 and 2 were very poor. Additional measurements showed resistive effects in the screen-printed metal contacts.

The third process lot of 25 SG wafers was processed, with several subgroups given slightly different treatments in an effort to diagnose the cause of the poor fill factors in the first two lots. These variations and subsequent work led to the conclusions that (i) the poor FFs were due to inadequate metal-semiconductor contact by the screen-printed metal on the front of the cells (not the back); (ii) the surface texture of the Si substrate affects the quality of the contact; and (iii) the surface conductivity of the diffused layer is high enough to make fairly good contact with the screen-printed silver.

The first of these conclusions was reached by several different etching treatments of the metals that consisted of dipping the cells into 2% HF solution. This type of treatment is known to improve the contact properties of poor screen-printed Ag on Si, although it causes other problems, as described below. By masking the backs of some wafers and the fronts of others before this etch, we demonstrated that the effect occurred only when the HF dip acted on the metal of the front of the cells.

The role of surface texture in determining the quality of the metal-Si contact has been established in other places, and was confirmed here by direct comparisons of the properties of cells that were nearly identical except for the nature of the initial surface. The central result is that a highly polished Si surface makes poor contact to screen-printed silver. This result is not

understood, and the limits of its validity are not known. Specifically, will a variety of crystallographic orientations in the surface due to polycrystallinity create problems in the surface preparation for this purpose?

One complication that is not fully resolved is the close relation between the improper surface texture and the possible presence of saw damage at the surface. There is clear evidence that each of these can harm cell performance, but it is difficult to distinguish between them at present.

The conclusion that the surface conductivities used here are not the primary source of the poor FFs was reached by modifying the diffusion schedule for some wafers to produce a higher conductivity (~25 Ω/□) without a significant increase in junction depth. At this level of conductivity, it is well established that the silver ink used here can make a good electrical contact. But this increase in conductivity (the former value was ~40 Ω/□) did not succeed in eliminating the problem with poor FFs.

The first epitaxial wafers to be processed into solar cells were 14 wafers from epi runs 39 and 40, which were processed simultaneously with 11 SG single-crystal wafers as process lot 4. One of the 14 epi wafers consisted of an epi layer grown on a substrate of p^+ single-crystal CZ Si as a control for evaluating the epitaxial growth. The FFs for these cells before and after the HF dip are shown in Fig. 5 as a function of the wafer position in the group of 25 as they stood in the diffusion furnace. It is obvious that in their initial condition the cells made on UMG substrates had much worse FFs than the others. (There is evidence, shown later, that cell Nos. 24 and 25 at the end of the furnace had lower FFs because of lower surface conductivity.) The fact that cell No. 10, which was the epi control, had a much better FF than all the other epi cells makes it clear that the responsibility for poor FFs is not with the epi growth.

The effects of an HF dip on the FFs of the UMG cell are dramatic; also, most of the SG cells have improved FFs. There is, unfortunately, insufficient understanding of the cause of this improvement to allow its use to diagnose the original trouble with the FFs. There may be two contributions to the limitation in FF: one due to nonoptimum surface textures and one due to some remnant saw damage at the front surface. One further observation in Fig. 5 is that even after the HF dip the FFs are not quite as good as they should be for good cells (~0.75).

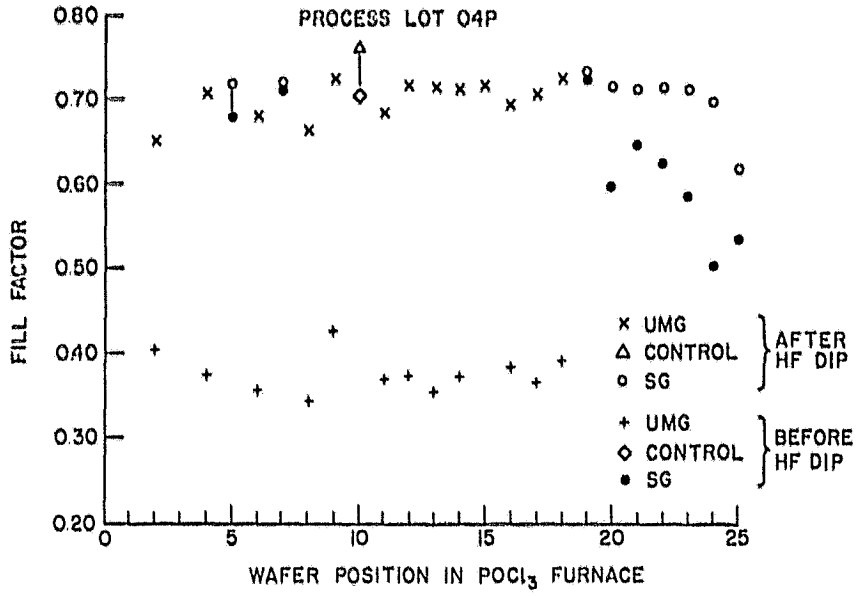

Figure 5. Fill factors of cells in process lot 4 in their original condition and after HF treatment to improve the metal equalization. The wafer position number is its location in the boat during diffusion, with the lowest numbers at the end near the gas entrance.

That is not the only problem with the use of HF to improve the metal contact. There has been evidence in the past that contacts that need the HF dip become sensitive to moisture after the treatment. In the case of process lot 4, this effect appeared prominently upon subsequent application of an AR coating as shown in Fig. 6. The FFs dropped back to values comparable to their initial values. The AR coating used here -- a sprayed-on suspension of TiO_2-based particles -- contains a great deal of water when it is applied.

Also shown in Fig. 6 are the measured values of the sheet resistivity of the diffused layers in all of these cells. These data were obtained by 4-point-probe measurements on the front surfaces after diffusion, and before further processing. It can be seen that this diffusion process results in layers with somewhat higher resistivities near the end of the boat, i.e., at the downstream end as determined by the direction of flow of the gases. Among the SG cells, some correlation apparently exists between low resistivity and higher FF. However, this cannot explain the very poor FFs of the UMG cells, many of which have quite low resistivities.

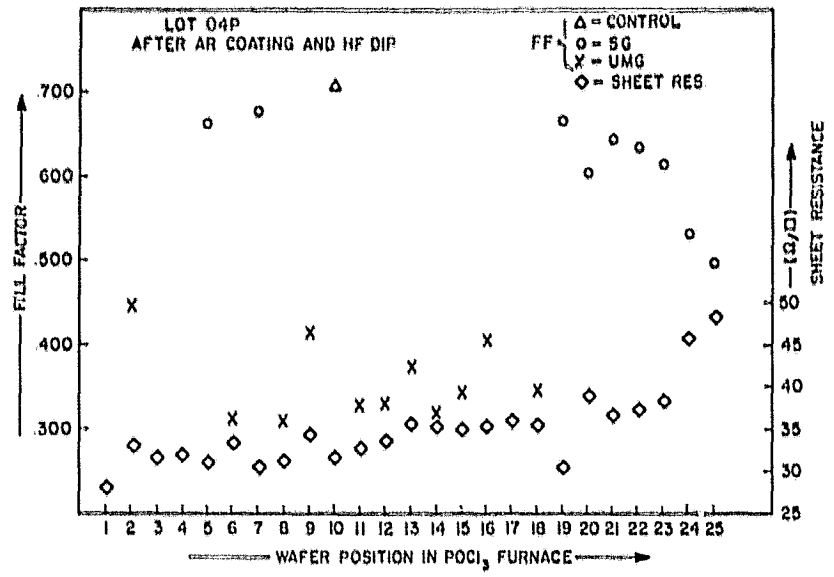

Figure 6. Fill factors of cells in process lot 4 after application of a sprayed-on AR coating, and sheet resistances of the diffused layers.

Subsequent measurement of the solar-cell properties of the cells of lot 4 showed still further degradation of their FFs, presumably due to the action of humidity in the air. This effect is shown schematically for two epi/UMG cells and one SG cell in Fig. 7. Without any further pursuit of this type of observation, it becomes quite clear that the improvement caused by HF on the FF of poor contacts of screen-printed Ag is illusory: it will eventually be lost to natural degradation. On the other hand, contacts that are initially good appear likely to stay that way.

As part of the evaluation of substrates of HEM/South African MG-Si, epitaxial solar cells were processed by the use of both evaporated and screen-printed metals. At the same time, two 4.5-cm^2 cells were processed on the wafers from epitaxial/Dow-Corning UMG growth, run 39. These cells had the same screen-printed metals as were used in process lot 4. In this small size the two cells, even without any treatment, had FFs of 0.78 and 0.79, both better than any seen in lot 4. The present conjecture is that occasional particulate inclusions may spoil a large-area cell in which they are unavoidable, whereas small cells might well be free of such scarce inclusions.

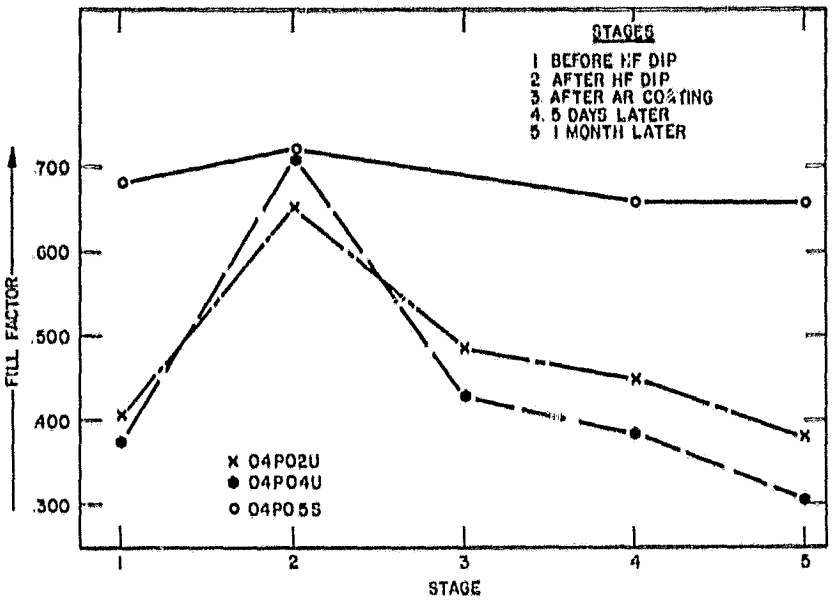

Figure 7. Representation of the variations in fill factors of three cells of process lot 4 at three different stages of their processing and at two subsequent times.

One other significant result of this group of cells was the marked difference in FF between cells that had epi layers grown on polished wafers (average FF = 0.56) or on etched wafers (average FF = 0.77). This confirms other observations of the importance of surface finish. This finish is influenced by both the initial amount of saw damage and the surface treatments.

In further efforts to diagnose the source of the poor fill factors, two exploratory series of cells were made by having a different operator perform the etching and epi growth. These both used 2-inch square wafers, and growths took place in a horizontal epitaxial reactor. One set contained Dow-Corning UMG substrates and p^+ CZ substrates, all getting the same epi layers. The second set contained twice-solidified HEM substrates. Of all the resulting cells, none had good fill factors, although those of the CZ substrates were better than the others. After measurement, two of the HEM cells were cut into smaller pieces to look for possible local variations in their properties. The subcells from cell 19, whose FF was 0.52, had FFs that ranged from 0.42 to 0.72. Thus, there seems to be clear evidence for problems in the surface finish that affects the screen-printed Ag contacts used on all cells, and in inhomogeneities in the UMG substrates from both Dow-Corning and Crystal Systems.

Because of continuing problems in the FF of single-crystal cells with screen-printed Ag contacts, and the mounting evidence of the importance of surface finish to the quality of those contacts, we have introduced a different Si etch to our processing. The purpose of the change is to reliably produce a slightly roughened surface that is known to be desirable for good screen-printed contacts. To achieve this, we chose NaOH, an etch that has been widely used within the LSA program. It is less expensive than the acid etch we have been using, and is known to be capable of producing "textured" surfaces under the right conditions. Since the present need is different from the texturing process (removal of saw damage is a major requirement here), we used a procedure developed by Spectrolab (under JPL sponsorship) for this purpose.

A series of etching experiments was performed on semiconductor-grade single-crystal wafers using 30% NaOH solution at 85°C for times of 5-20 min. The criterion used to qualify this process was a surface texture (observed under a microscope) that appeared to match a previously acid-etched wafer which had formed a good contact to screen-printed Ag. All the cells etched this way had good fill factors as well as good V_{oc} and J_{sc}, as shown in Table 3. With this encouraging result, a group of wafers has been prepared in this way for use as epi substrates. This group includes wafers of HEM, Dow-Corning UMG, and single-crystal materials. The premature termination of this contract prevented completion of the experiment.

TABLE 3. SOLAR-CELL DATA ON NaOH-ETCHED SINGLE-CRYSTAL DEVICES

Cell No.	V_{oc} (Volt)	J_{sc} (mA/cm^2)	FF	Eff. (%) (No AR)
5-A	0.59	23.0	0.69	9.3
5-3	0.59	22.5	0.69	9.1
10-A	0.59	22.5	0.71	9.4
10-B	0.59	22.4	0.72	9.4
15-A	0.59	21.8	0.73	9.4
15-B	0.59	21.9	0.75	9.6
20-A	0.584	21.600	0.736	9.3
20-B	0.586	21.120	0.700	8.7

C. TASK 3: PROCESS SPECIFICATION

The preliminary set of cell process specifications and procedures has been prepared and submitted in a separate report entitled "Preliminary Process Specifications and Procedures" (April 1981). These specifications represent the detailed descriptions of the various processes, materials, and procedures for the sequence that is outlined in Fig. 3. The change to NaOH etchant is not incorporated in that report. All of the specifications are consistent with either the epitaxial cell development by RCA under the ED contract [1] or the various LSA processes that were developed under JPL sponsorship. Because of certain unavoidable differences between laboratory processing as performed in the fabrication of cells under this contract and eventual factory production at high rates, these specifications differ in some details from the currently used processes. One example is the provision of specifications for epitaxial wafers that are 4-inch squares rather than the present 3-inch circles. In addition, recent advances in technology dictated specifications for the projected use of EVA encapsulant rather than the PVB now being used.

Planned revisions of these specifications were not completed at the time of the premature termination of this contract.

D. TASK 4: MINIMODULE DESIGN

Design of the minimodules to be fabricated is complete, and is to be glass/PVB/cell/PVB/Tedlar,* all laminated. For compatibility with JPL testing mounts, the modules have external dimensions to comply with JPL Dwg. No.10087506, Rev. A as provided to us by JPL. The cells were to be series-connected, as called for in that drawing, but no half-cells were planned for use.

E. TASK 5: PROCESS AND DESIGN VERIFICATION

Verification tests and measurements on cells were reported under Task 2. Because of the problems with performance of the epi/UMG cells reported under Task 2, the fabrication of operating modules containing such cells had been postponed. In the meantime, however, a group of non-epi cells of 3-in.-diameter was obtained and used in the fabrication of a complete trial module.

*Tedlar is a registered trademark for PVF film made by E. I. du Pont de Nemours & Co., Inc., Wilmington, DE.

This procedure has established the various steps in cell interconnect, module assembly, and lamination. These processes appear to be well in hand so as to be ready when useful epi/UMG cells will be available.

F. TASK 6: COST EVALUATION AND PROJECTIONS

An initial SAMICS cost analysis has been prepared and submitted as a separate report entitled, "Initial SAMICS Cost Analysis" (April 1981). As with the process specifications in Task 3, this analysis is based on the projected factory operation which is, of course, not identical to the present laboratory processes. A brief summary of the principal process steps and their projected costs are presented in Table 4. It can be seen that the projected module price is far below the $700/kWp that was the 1986 goal of this contract. The reason is that the associated Exploratory Development program of SERI has a target date of 1990, by which time it is expected that this epitaxial technology can produce modules at less than $500/kWp.

Planned revisions of this SAMICS Cost Analysis were not complete at the time of the premature termination of this contract.

TABLE 4. SAMICS COST SUMMARY (from Initial SAMICS Cost Analysis)

Process Step	$/Wp
HEM Solidification	0.032
Sectioning	0.015
FAST Slice	0.047
Wafer Etch	0.038
Megasonic Clean - 1	0.014
HTR Epi	0.085
$POCl_3$ Deposition	0.007
Junction Plasma Etch	0.007
Megasonic Clean - 2	0.014
Screen Print Al Back	0.008
Screen Print Cu Pad	0.004
Screen Print Ag Grid	0.076
Spray AR	0.007
Cell Test	0.004
Cell Interconnect	0.039
Encapsulation (Springborn)	0.072
Module Test (Motorola)	0.002
Total	0.491