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A LORAN-C PROTOTYPE NAVIGATION RECEIVER FOR GENERAL AVIATION

by

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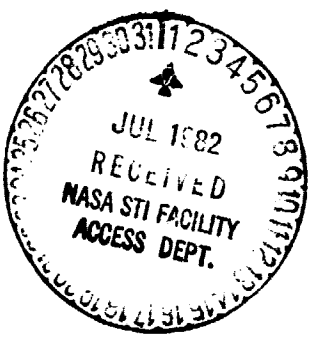

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I. INTRODUCTION

The Avionics Engineering Center, Ohio University Department of Electrical Engineering, has pursued the techniques required for Loran-C navigation with application to the general-aviation pilot. The goal has been to produce prototype equipment for flight evaluation which will provide enroute navigation in both latitude-longitude and rho-theta coordinates and to evaluate the non-precision approach capabilities of such equipment.

For this prototype project, single-chain, master-dependent operation was chosen as a demonstration mode, with three stations tracked. The prototype hardware design will, however, permit cross-chain, master-independent navigation. The number of stations tracked simultaneously can be expanded. These extended operating modes are implemented through programming utilizing existing shared tracking-loop hardware as described below.

The prototype Loran-C receiver has been flight-tested using a variety of flight paths, with and without simultaneous ground radar position data collection. Results are presented later in this paper; further flight evaluation is planned, and will be reported separately.

The following sections describe major receiver elements, drawing upon the work and publications of project team members who contributed to the design.

II. RECEIVER OVERVIEW

As configured for laboratory and flight evaluation (Figure 1), the prototype Loran-C receiver utilizes an aircraft ADF sense antenna or similar unit, connected directly to the wide-band preamplifier/coupler. Signal levels for the linear RF processor are stabilized by a commutated, sampled AGC element, under control of the receiver computer.

The RF unit performs analog signal processing and conversion to TTL-compatible output pulses corresponding to Loran-C envelope events. For the prototype receiver, a commercially-available microcomputer is utilized for both sensor and navigation processing, plus AGC control. Computer control and data recording for experimentation are provided by a hand-held ASCII terminal and either analog or digital cassette units.

Pilot control of receiver functions is effected through the panel-mounted keyboard and video display unit, supported by a video processor board with independent memory. The receiver computer is, in this prototype implementation, supported by a mathematical function processor chip, aiding in the coordinate conversion from Loran-C to geodetic coordinates, and for rho-theta conversions.

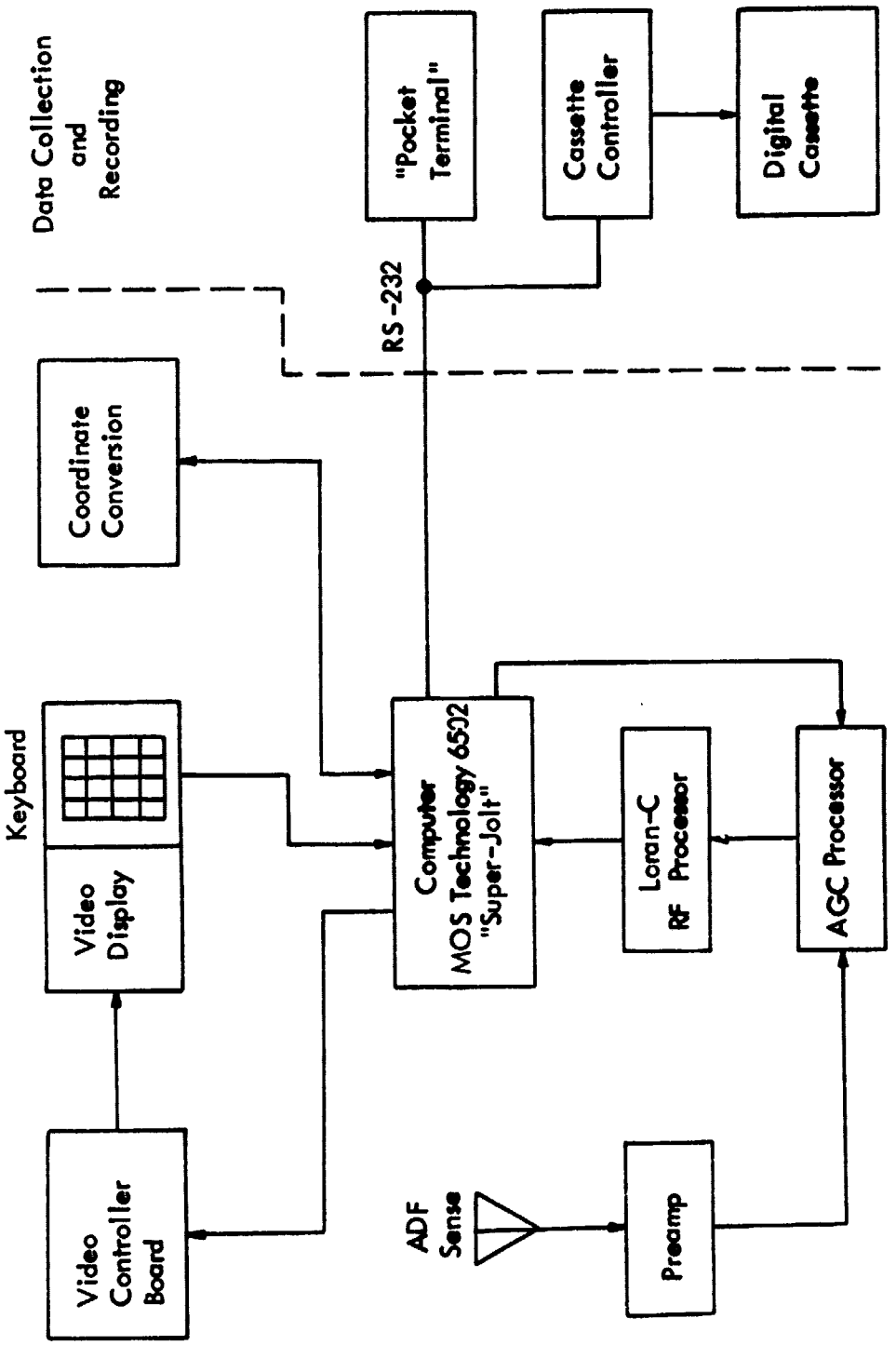


Figure 1. Prototype Loran-C Receiver - Block Diagram.

III. ANTENNA PREAMPLIFIER/COUPLER

The Loran-C prototype utilizes the wide-band preamplifier of the type reported by Burhans [1, 2, 3] for connection to either a 1-meter (or larger) whip antenna for laboratory tests or to the existing ADF sense antenna aboard the test aircraft. This preamplifier, illustrated in Figure 2, provides -4.9 dB voltage gain at 100 Khz., matching a High-Z antenna to a 1000 Ω receiver input impedance, and a dynamic range from 0.2 to 10,000 microvolts rms at the input terminal. Preamplifier 3 db points occur at 10 Hz and 8 MHz.

The preamplifier schematic is shown as Figure 3. Input surge protection is provided by the NE-2 bulb at the input terminal. The low-noise JFET drives an open-collector output stage, the load resistor for which is contained in the receiver RF module. Both DC power and signal use the signal coaxial cable connecting the preamplifier to the receiver RF section, eliminating power-supply ground-loop problems.

IV. LORAN-C RF PROCESSOR

The Loran-C receiver RF processor is based on an auto-correlation envelope detector. The unit is driven by the low-impedence output of the broadband, unity-gain antenna preamplifier. See Figures 4, 5 and 6.

The input circuit is a broad-tuned transformer with a 40kHz bandwidth, centered at 100kHz. The output of this transformer is placed across a 1K ohm potentiometer, the wiper of which controls the amount of signal provided to the trap circuitry. Note that this voltage-divider circuit has created a passive RF gain control, to which the operator has access in the prototype design.

To improve signal-to-noise ratio (with respect to interfering frequencies) of the Loran-C signal, it is desirable to eliminate strong signals close to the 100 kHz region before the RF is actively amplified. This is accomplished by passing the RF through a pair of notch filters. These narrowband filters are centered at 88 kHz and 119 kHz, to eliminate the 88 kHz, 116 kHz, and 122 kHz interfering frequencies affecting the 99600 U.S. Northeast Chain. These interfering frequencies are listed in the May 1980 edition of the Loran-C User Handbook by the U.S. Coast Guard [4].

Current work is underway to investigate distortion products from multiple RF signals and harmonic mixing or multiplying to produce new frequencies that interfere with Loran-C. Research results and documentation of this work will be available from the Avionics Engineering Center through the NASA Joint University Program.

Once the interfering frequencies are minimized, the RF signal is amplified by a tuned RF amplifier. This TL072 operational

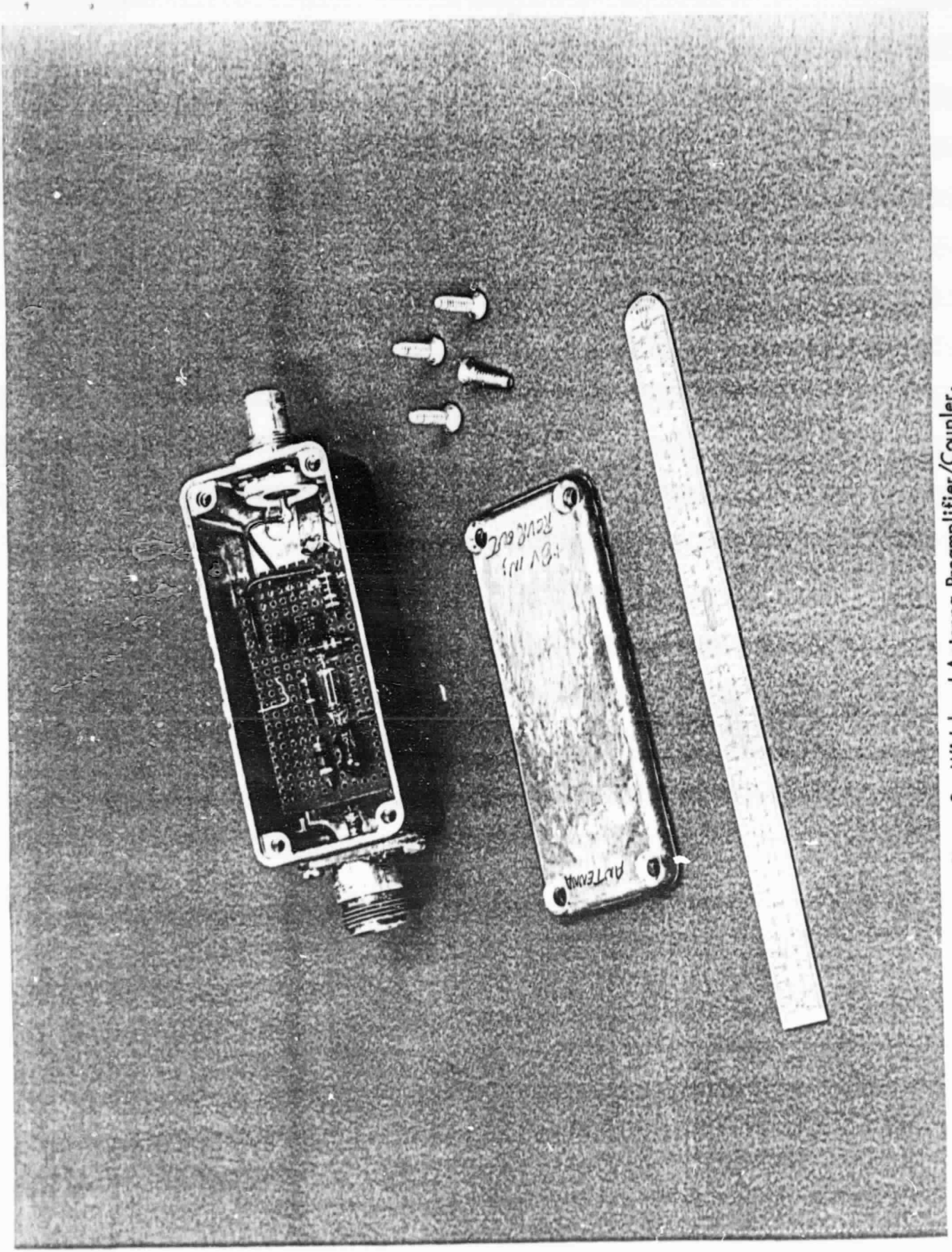


Figure 2. Wideband Antenna Preamplifier/Coupler.

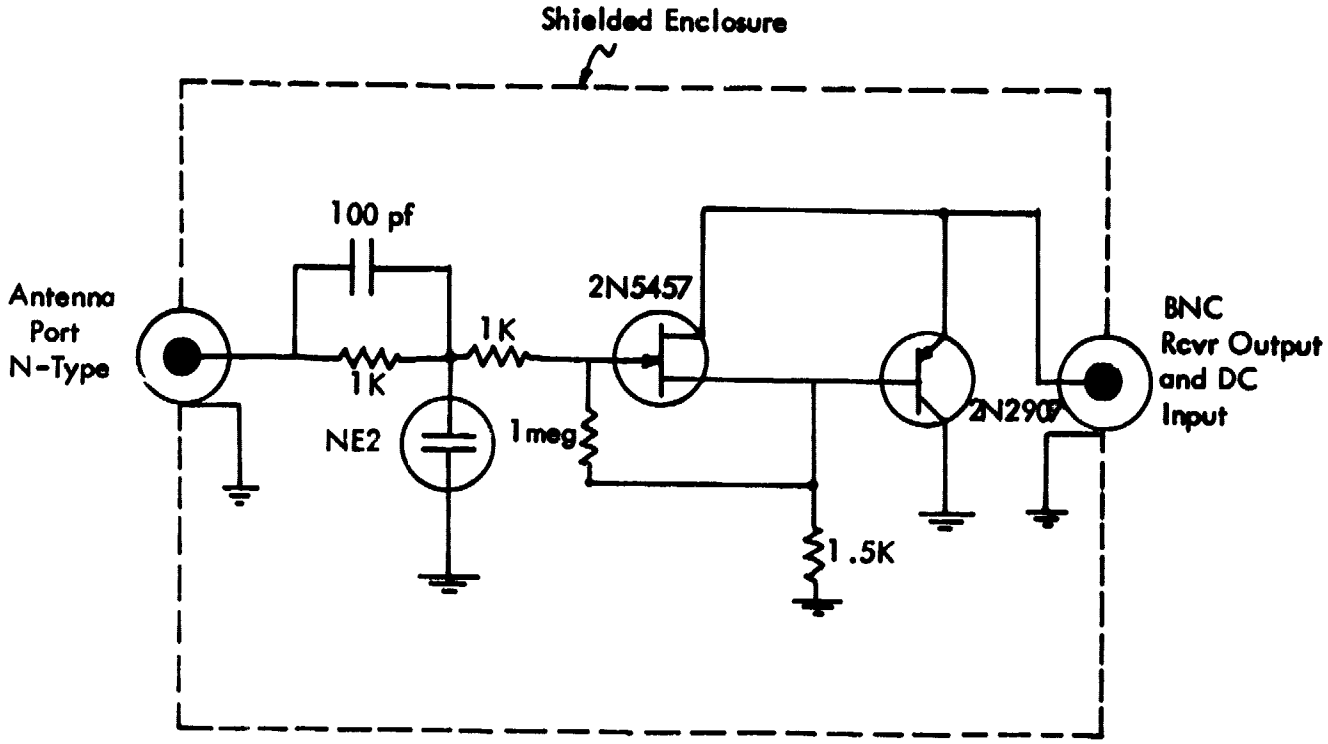


Figure 3. Preamplifier Schematic.

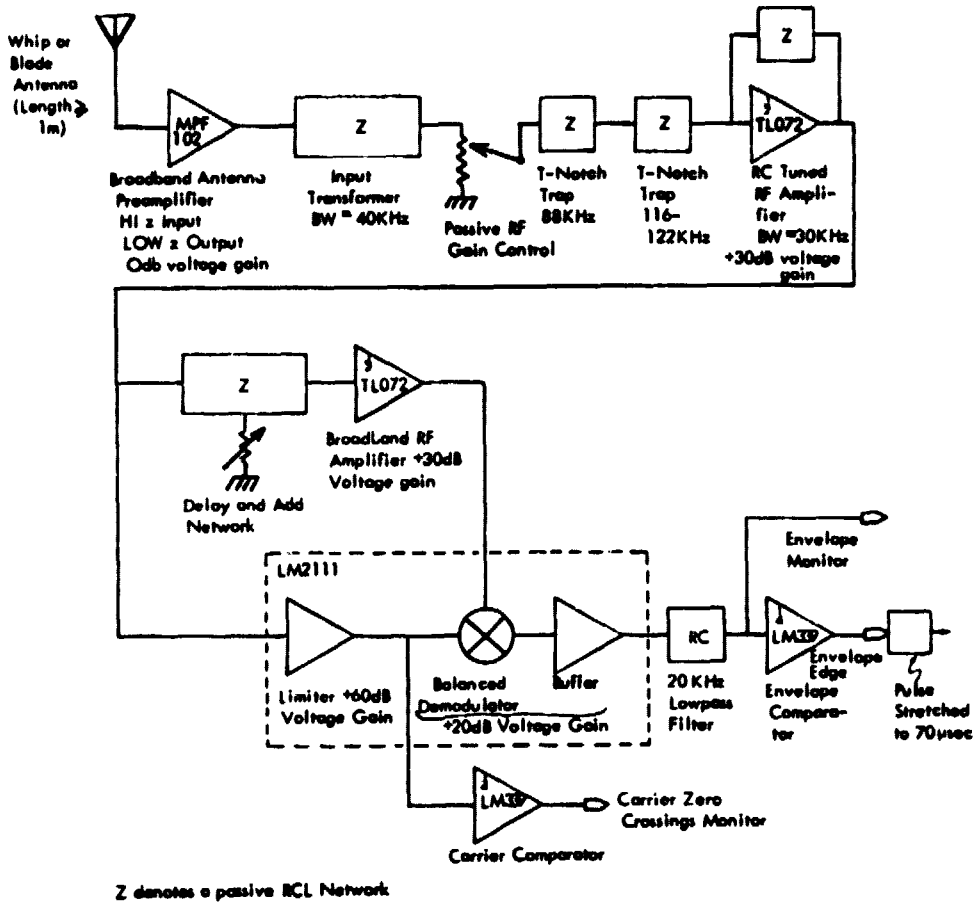


Figure 4. Loran-C Autocorrelation Envelope Detector.

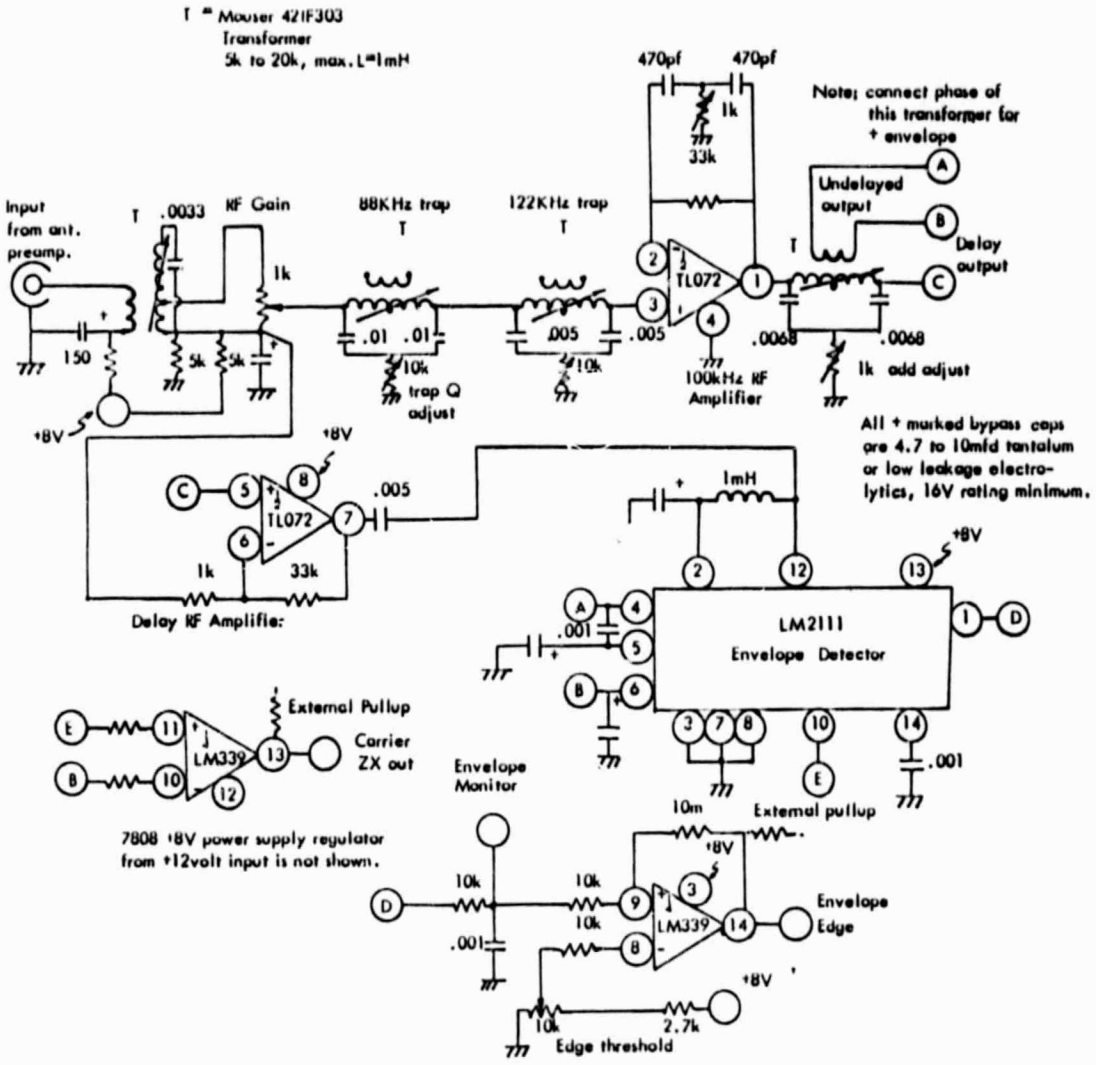


Figure 5. Mini-L80, Loran-C RF Detector Circuit.

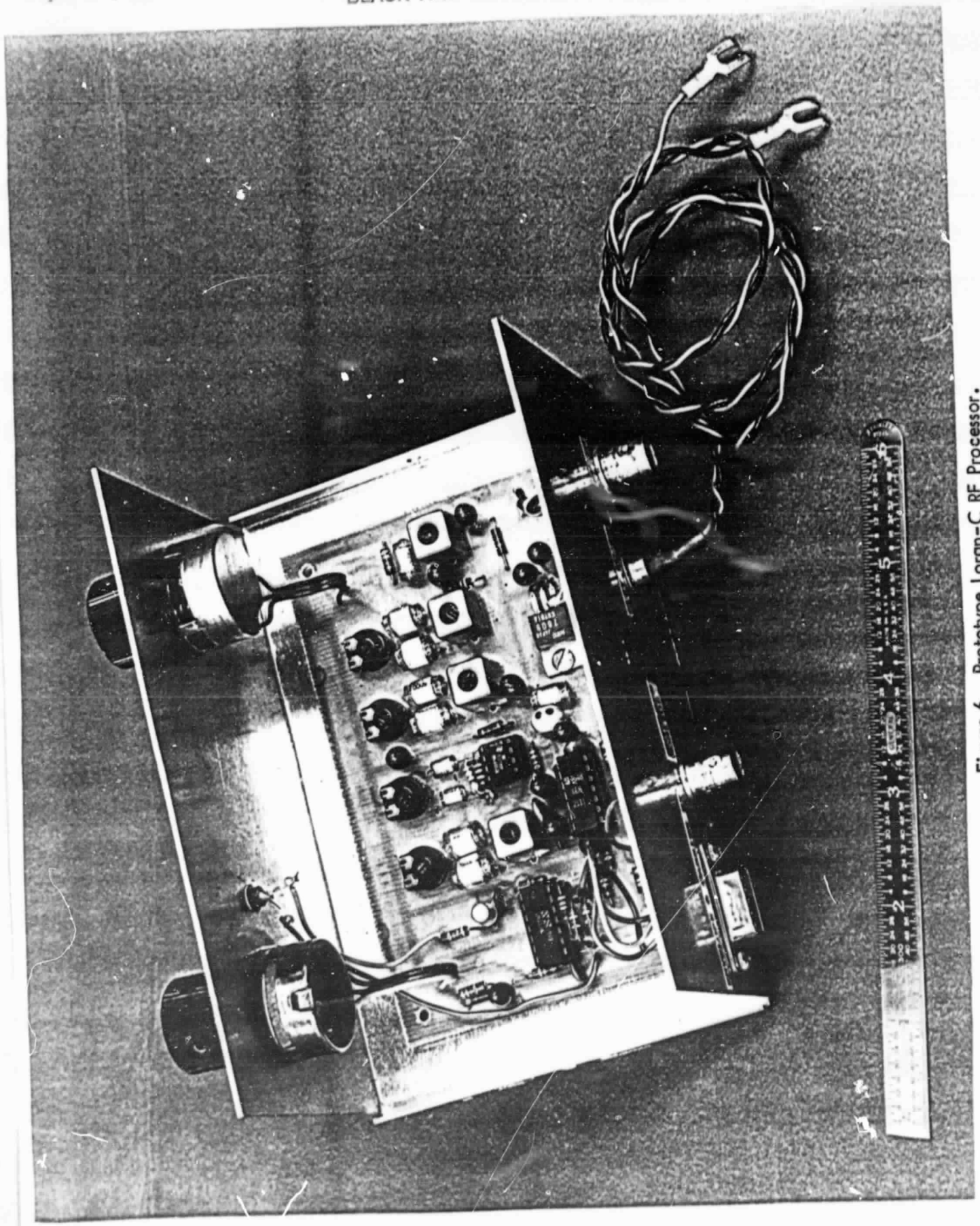


Figure 6. Prototype Loran-C RF Processor.

amplifier circuit offers +30 dB gain with a 30 kHz bandwidth, centered at 100 kHz. The RF signal flow now branches into two separate paths, to be manipulated separately to create the RF signals required for the LM2111 FM Detector and Limiter. One path drives a T-notch filter tuned tc 100 kHz which delays the RF signal and adds the delayed reproduction to the actual incoming RF (delay-and-add). The delayed-and-added signal is then amplified by a broadband, +30 dB gain TL072. This signal path is terminated at one of the RF inputs to the balanced demodulator of the LM2111. The second path drives the RF limiter of the LM2111 (the limiter has +60 dB gain), which in turn provides the signal for the second RF input of the balanced demodulator and the carrier zero-crossing detector.

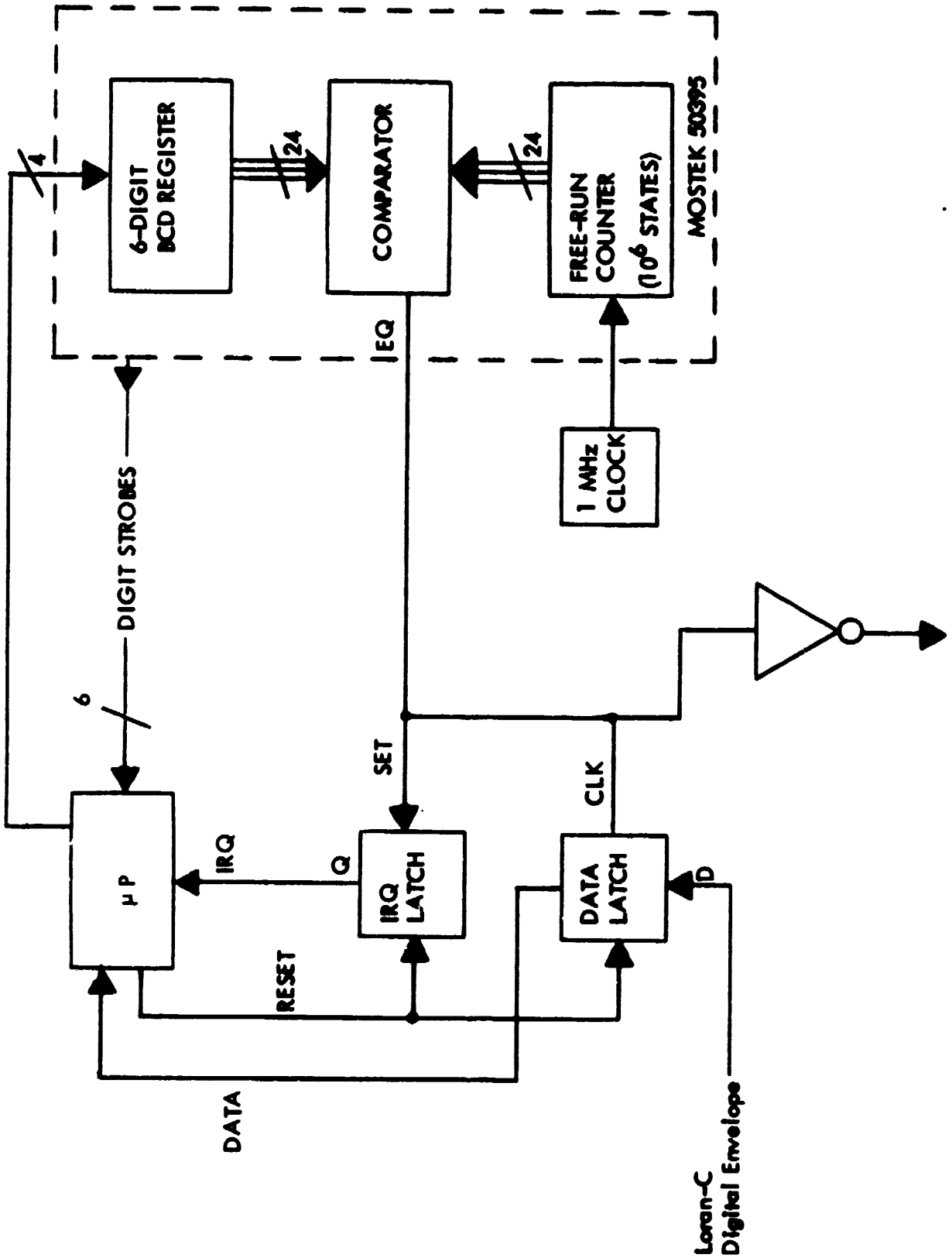
The LM2111 IC provides a double-balanced active multiplier used as an envelope detector. The demodulated signal is fed to a lowpass RC filter (20 kHz bandwidth), creating the Loran-C envelope, from which the digital output is derived. An envelope level detector produces a digital pulse at the zero crossing of the rising edge of the Loran-C envelope. This pulse, correlated with the zero crossings of the RF carrier (from the output of the LM2111 limiter) produces the digital pulses to be used for signal processing. These pulses are stretched to 70 µsec. to permit the tracking loop search routines to operate efficiently.

V. TRACKING LOOP HARDWARE

The Loran-C prototype receiver achieves time-difference measurement by use of a software-controlled, shared, digital loop. The block diagram for this loop circuit is shown in Figure 7, and its schematic in Figure 8. A 1 MHz clock drives the 6-digit BCD free-running counter portion of the MOSTEK 50395 integrated circuit, providing the receiver time base. The 6-digit comparator produces an EQ pulse each time the counter and the 6-digit register are identical.

In operation, the microcomputer loads the register with the count corresponding to the desired sample time for loop operation, while the counter continues to run. Equality of counter and register produces an EQ pulse, which is latched as an interrupt request (IRQ) for the microcomputer. At the time the EQ pulse is received, the Loran-C digital envelope signal is also latched, and its value made available to the microcomputer. The microcomputer may then reload the register for the next sample point, a process which has been measured to require 450 µsec. The loop, therefore, is able to detect each envelope pulse, at the 1 msec. Loran-C interval, with sufficient guard time to insure correct operation.

The schematic shows interconnection between the tracking loop and the Super-Jolt (TM) microcomputer, which is used in the prototype receiver for evaluation. Pinouts are detailed in Figure 9. This 8-bit microcomputer is based upon the MOS Technology 6502 CPU chip, running at a 1 MHz clock rate. In the prototype receiver, the computer and loop clocks are obtained from the same TCXO for convenience, but computer software is entirely asynchronous, interrupt-driven code.



TIME SYNCHRONIZATION WITH IRIG-B

Figure 7. Tracking Loop Block Diagram.

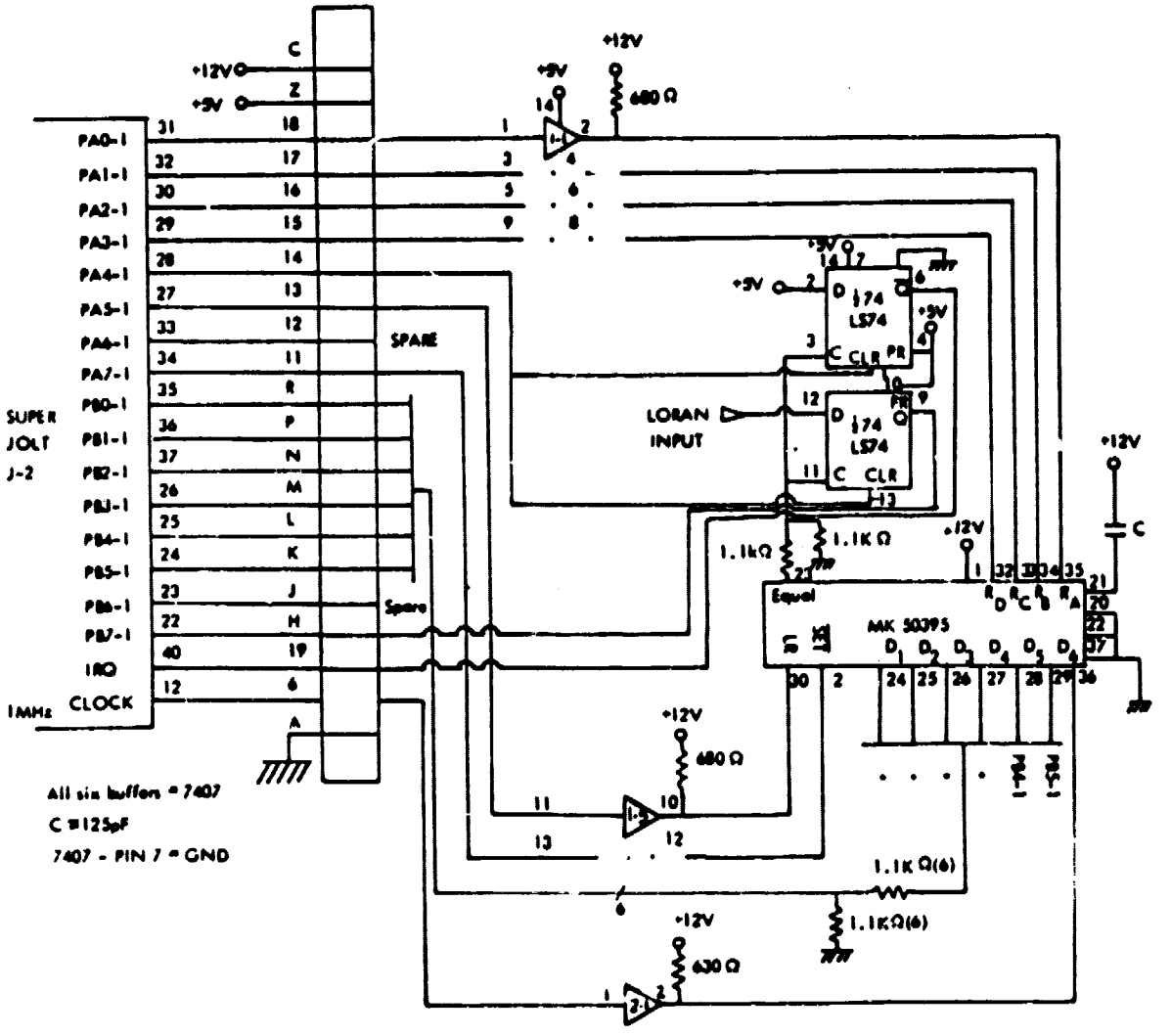


Figure 8. Tracking Loop Schematic.

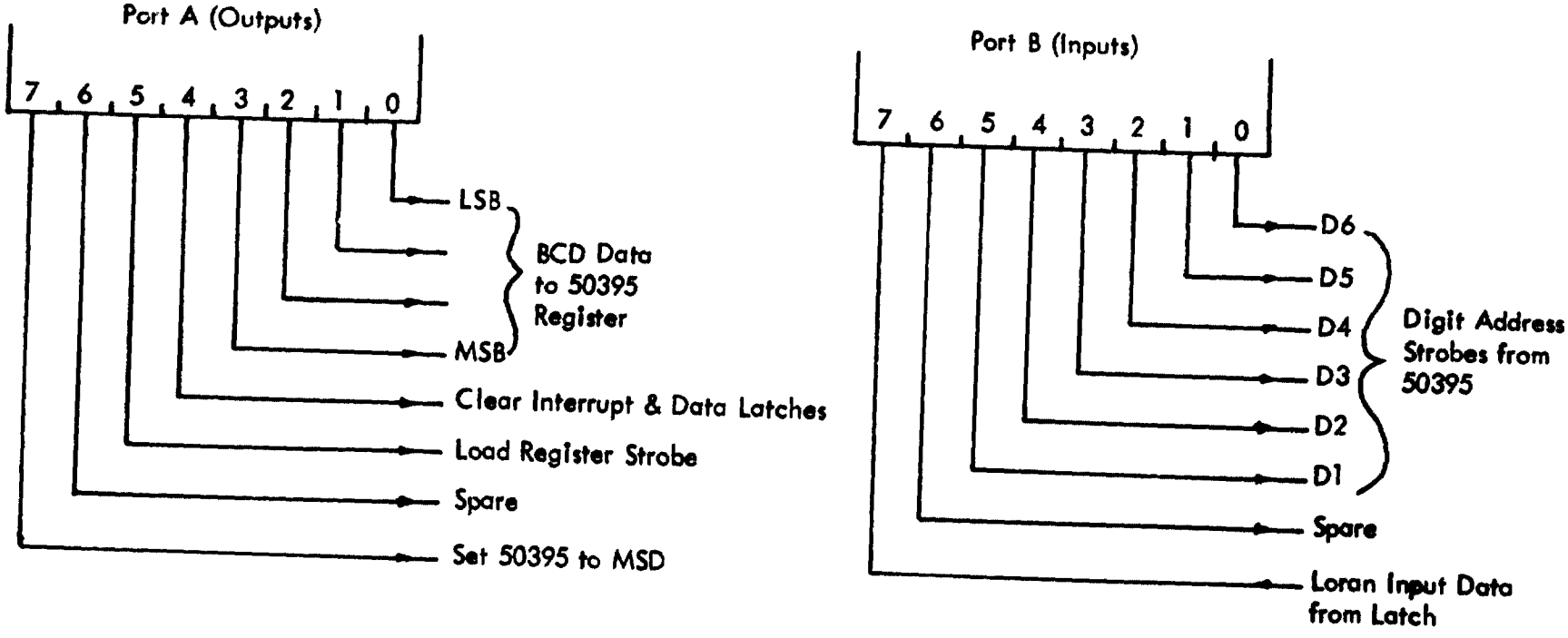


Figure 9. Tracking Loop PIA Assignment.

The digital loop circuit board is shown in Figure 10. The MOS Technology 50395 is visible as the 40-pin chip, supported by a 7474 latch for IRQ and Loran-C input latching, and one monostable multivibrator, 74123, to stretch the Loran-C digital RF processor outputs to 70 μsec. for loop use. The remaining circuitry provides level shift services, to interface the MOS loop chip to TTL input/output lines for the microcomputer.

The entire loop circuit is operated by one 6520 PIA interface, which is an integral part of the Super-Jolt microcomputer.

VI. TRACKING LOOP PROGRAMMING

Initially, tracking loop software has been developed to demonstrate correct hardware operation and to provide a basis from which coordinate-conversion and area-navigation routines could be developed. This sensor processor software consists of signal acquisition, tracking and time-difference generation segments, operating on a single Loran-C chain. In the current implementation, three stations are tracked, one of which must be the master station.

Loop routines are initiated at receiver start-up, by user choice of Loran-C chain. This selection, made by entering the group repetition interval (GRI), causes the loop routine to add the GRI, in microseconds, to the loop register upon receipt of each loop interrupt request (IRQ). The result is a series of interrupts, at the GRI rate, with samples of Loran-C input data occurring with each interrupt. Loop arithmetic is continuous; that is, the counter is allowed to overflow at 10^6 counts, with no resulting effect on sample rate.

Each IRQ causes loop software to read the state of the Loran-C latch and to clear the Loran-C and IRQ latches. While in this acquisition mode, the goal of the loop routines is to find correlated signals at the Loran-C latch, compared with the GRI samples. If no occurrence of five contiguous Loran-C ones in 32 GRI frames is found, the acquisition segment modifies the sample time by adding 6,500 μsec. to the register. This addition effectively delays the sample comb by 6,500 μsec., and the test for Loran-C signals is repeated. After an unsuccessful test at the 6,500 μsec. increment, the test is repeated for 36 mini-increments of 33 μsec. each.

With each Loran-C pulse stretched to 70 μsec., acquisition is generally accomplished in less than ten seconds. Once one Loran-C pulse is found, acquisition code passes control to station-track code, which immediately subtracts 2,000 μsec. from the original register contents and repeats the acquisition test. If no pulse is found, the register is increased by 1,000 μsec., and the test repeated. If a pulse is found, 2,000 μsec. is subtracted again. In this manner, the first pulse of each Loran-C station is acquired.

Fine tracking begins at this point, with the station-track routine subtracting one microsecond when the Loran-C data is high, and

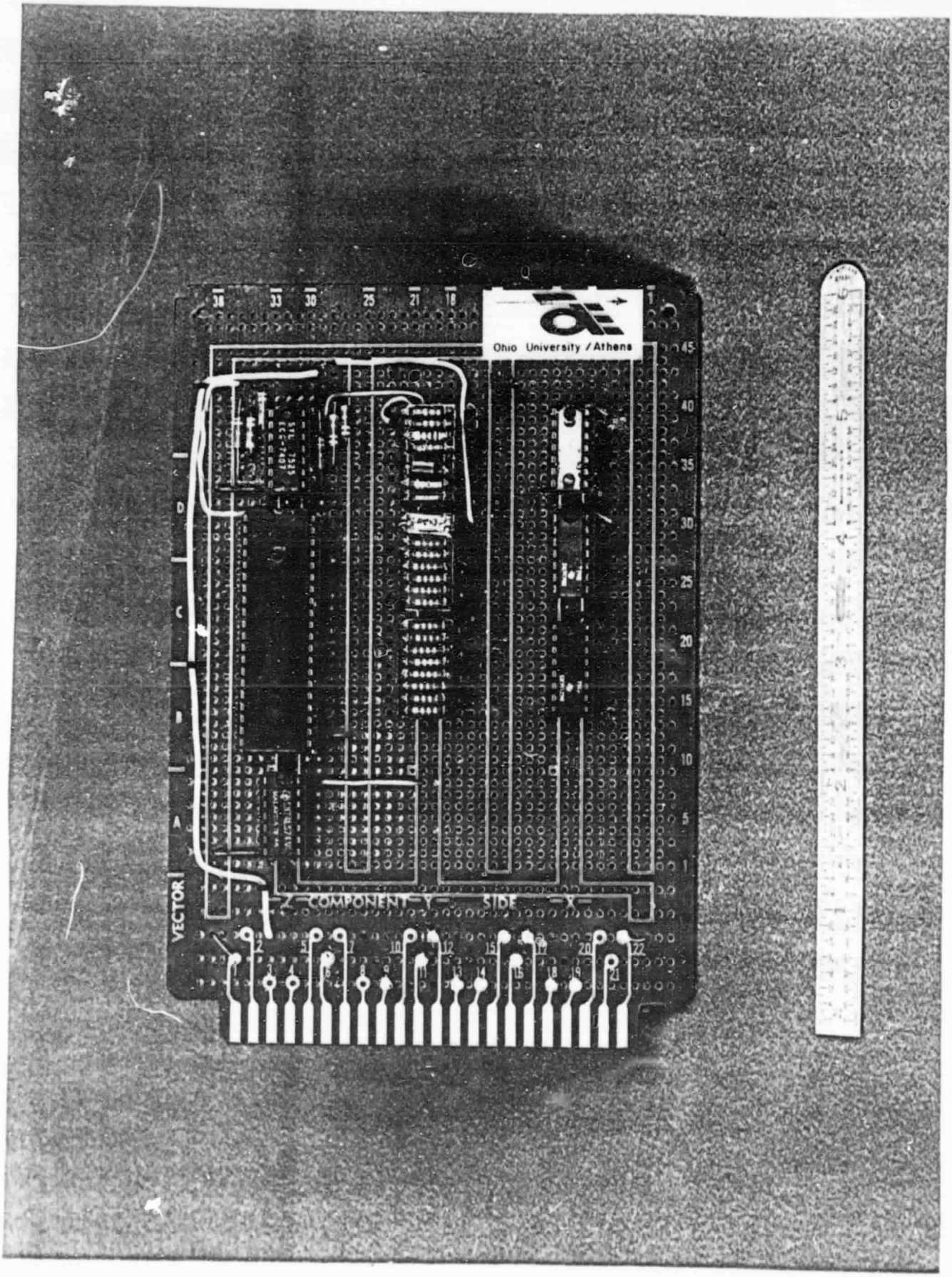


Figure 10. Tracking Loop Implementation.

adding one microsecond when the Loran-C data is low. A loop filter is inserted at this point, in the form of an up-down software counter, to provide for optimum loop characteristics. Filter parameters are taken from previous theoretical [5] and experimental [6] work, and were chosen as a 5-bit register. When this register overflows, one microsecond is added to the loop register. Upon filter register underflow, one microsecond is subtracted. The result is a low-pass loop filter, with time constant of 4 GRI time periods. Using the first-pulse position in the loop register, determined by the search/track process just described, the station-track segment then generates eight sample pulses, by 1,000 μsec. increments of the loop register, spaced one millisecond apart, and permits correction of the loop register value at each of the eight pulses.

After successful lock to the station, the loop register is incremented by 9035 μsec., and the master 9th pulse is sought by the acquisition test. If found, the current station is labeled as the master, for use by background routines in computing time differences. The register content, representing the time of occurrence of the station first-pulse, is stored for retrieval at the next occurrence of the station's signal.

The loop software then generates a search pulse immediately after the last pulse for the current station, and the search/track process is repeated. The third station is located in the same manner.

In addition to the basic pulse-tracking function, the loop routines also produce a signal-quality number, useful in generating user warnings and assessing receiver operation. A software counter is incremented by one, for each station, when the loop routines must subtract one microsecond to retain lock. This counter is then cleared by background routines after display. In the current implementation, the counter is active for ten GRIs, resulting in a total pulse count opportunity of 80. In ideal conditions, with no noise present on the Loran-C input, the counter should reach one-half the total pulse count, since alternate additions and subtractions of one microsecond would be required to retain lock, on each of the station pulses. Significant deviations from this value indicate the potential for loss of lock, and may be used to trigger re-acquisition of the station.

The background routines, which operate with IRQ enabled, execute when the signal-processing software just described is completed for each Loran-C pulse. A BCD buffer for each Loran-C station contains the loop register value generated in the previous GRI; these values are averaged over ten GRI periods, and the slave values subtracted from the master after averaging. The results are displayed as the time differences. The signal quality numbers are displayed also. Time difference data is placed in buffers for use by the latitude-longitude conversion routines.

The initial implementation of tracking loop programs has met the desired objective. The receiver logic has been demonstrated, and

loop parameters measured. It has been determined that the single microprocessor receiver will be capable of five-station tracking plus coordinate conversion, and that ample guard time exists between Loran-C envelope pulses for signal processing to take place, with the microcomputer operating at 1 MHz.

A counter/comparator IC offering faster digit-strobe operation would be a definite aid, as the scan oscillator on this IC is the limiting factor in register loading by the microcomputer.

The software-controlled tracking loop implementation has demonstrated some interesting by-products, in that the loop has applications in time synchronization and navigation audio processing not contemplated at its inception. Use of the loop in IRIG-B time synchronization, for example, has been accomplished with complete success. [7]

VII. VIDEO OUTPUT

A prototype video interface [8], designed specifically for large-character output for cockpit use, has been used throughout the receiver development and evaluation program. Figure 11 shows this video circuit board. With the forthcoming addition of rho-theta area-navigation software, this video interface will be exchanged for a smaller circuit board, able to display both character and graphics data.

Two-page output permits display of Loran-C time-difference data, signal quality and housekeeping data on one video page, and the latitude-longitude and range-bearing waypoint data on the other. With the graphics interface available, CDI information will be displayed on both pages, driven by the bearing-distance coordinate conversion routines.

Figure 12 shows the receiver package, with video monitor and keyboard installed. The Loran-C RF processor will be enclosed under the chassis for isolation from the digital circuitry and the video monitor oscillator, and the digital circuit boards will surround the monitor chassis. The package is standard general-aviation width, for mounting in the vertical stack. The power transformer visible at the rear of the unit is installed for bench testing only, and is not part of the final prototype, which will operate on 14VDC.

VIII. LABORATORY AND FLIGHT EVALUATION

Receiver tests run with a Loran-C simulator have consistently provided receiver time differences within ± 1 μsec. of simulator outputs. These tests have also defined the need for receiver AGC applied station-by-station, due to TD offsets observed for variations in relative signal strength among stations. This AGC circuitry is currently under test.

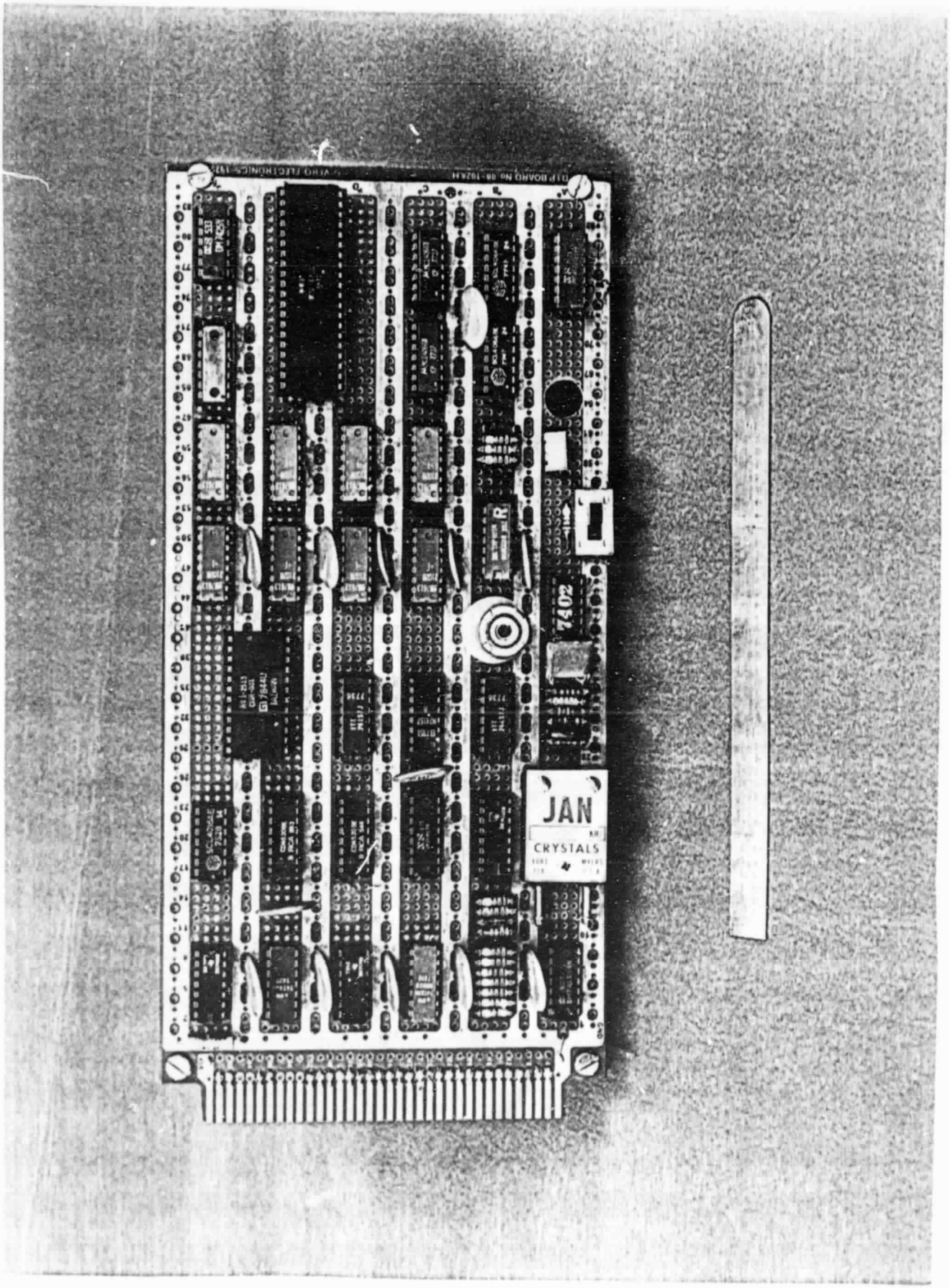


Figure 11. Video Interface Circuit Board.

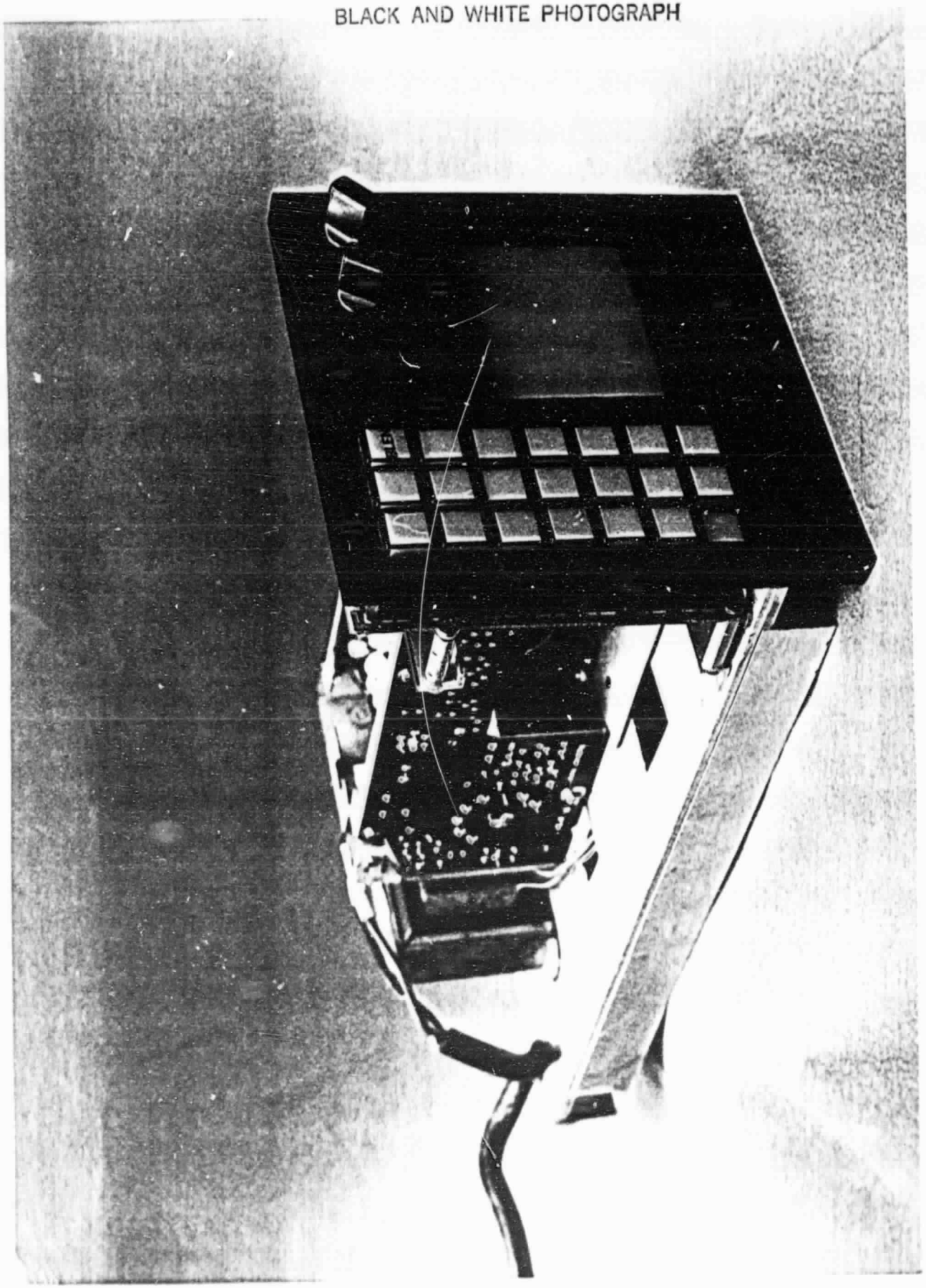


Figure 12. Receiver Enclosure.

Flight evaluations, made without AGC circuitry at Ohio University Airport, Athens, Ohio on March 9, 1981 are illustrated in Figures 13 and 14. These graphs are plots of receiver latitude/longitude outputs, converted to range and bearing from a waypoint.

For Figure 13, the waypoint is the calculated latitude and longitude of the runway center point. The flight path begins at point (1), on takeoff roll over the waypoint. The path proceeds on climbout, heading 240° and through pattern turns at 800 feet AGL to crosswind and downwind legs. Downwind is extended to seven miles northeast of the airport, where the aircraft is turned inbound, across the UNI non-directional beacon, 5.3 nautical miles from threshold. A normal low approach is then executed, heading 243, flying visually along the runway centerline.

Following the low approach, a tight turn is made to a close downwind leg, followed by an outbound segment (2) approximately 30° south of centerline. A perpendicular cut across the UNI beacon (3) is then executed, followed by a turn (4) back to the beacon, and a left 270° turn to the inbound approach course. A second low approach along runway centerline is then executed, followed by landing and taxi operations.

The data presented is averaged by the receiver over a ten-GRI time period; approximately one second on the 99600 chain. Positioning repeatability over the UNI NDB, and along the approach track are observed to be excellent. Long-term variations along the approach course tend to be well-correlated, with a peak variation of less than 600 feet. Note, however, the offset to the north, resulting in a track parallel to the desired runway centerline track, of approximately one-half mile. This offset has been determined using the laboratory simulator to be due to signal-strength characteristics among Loran-C stations in the local area.

Figure 14 shows Loran-C data, with one-second TD averaging and subsequent latitude/longitude conversion, presented as distance and bearing from the runway. For this flight, a receiver waypoint was determined by placing the aircraft stationary at the runway center point, and entering the resulting receiver latitude and longitude value as the waypoint. The flight then consists of a takeoff and climbout to 1000 feet AGL, on runway heading. Variations noted on this plot are a maximum of 0.4 nmi south of course, and 0.3 nmi to the north.

It should be noted that these flight evaluations were local, short flights to assess basic receiver operation and raw data stability. Current plans call for documented flights, including ground radar tracking for position reference, as soon as AGC circuitry is fully tested.

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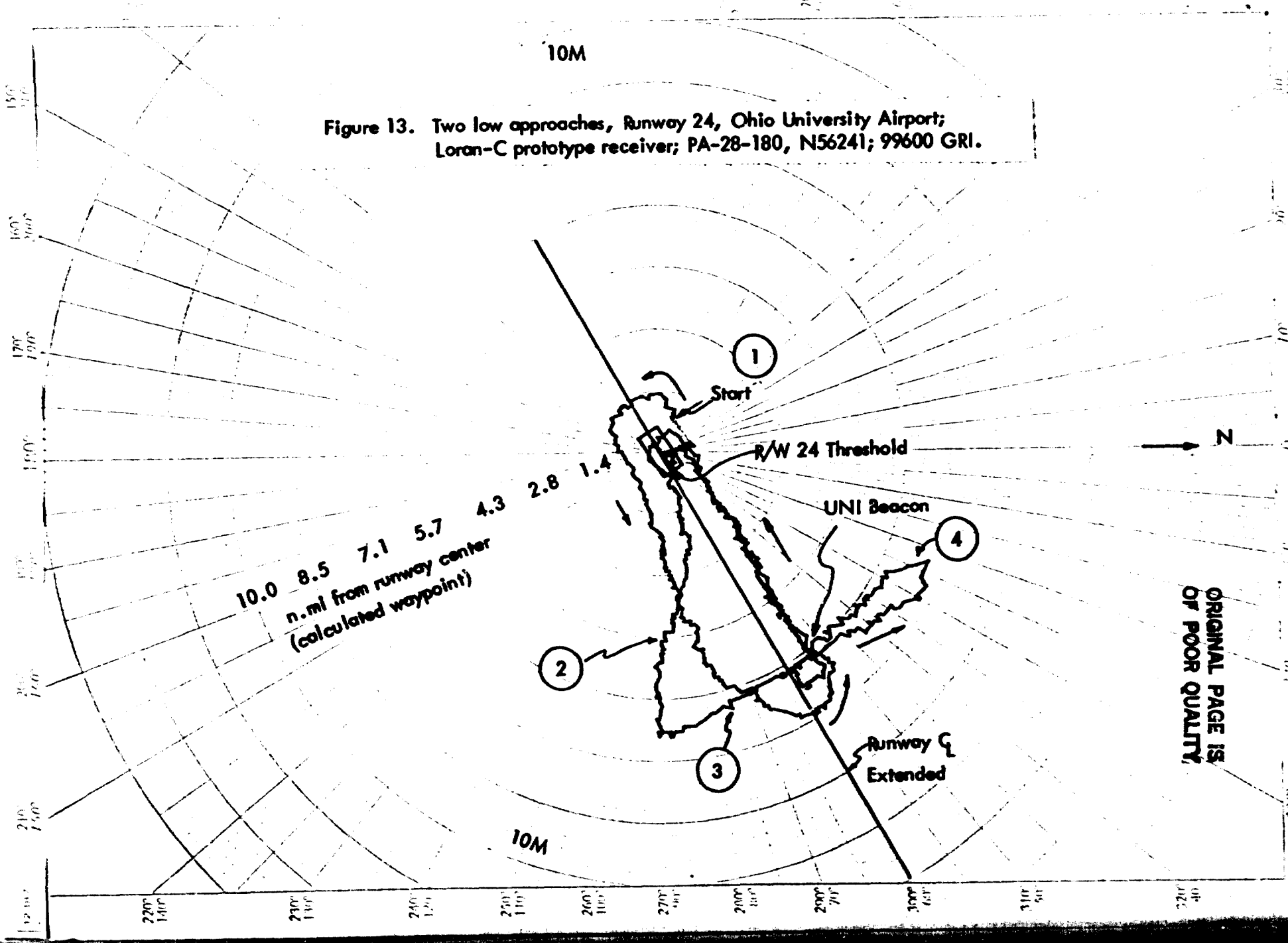
Figure 13. Two low approaches, Runway 24, Ohio University Airport; Loran-C prototype receiver; PA-28-180, N56241; 99600 GRI.



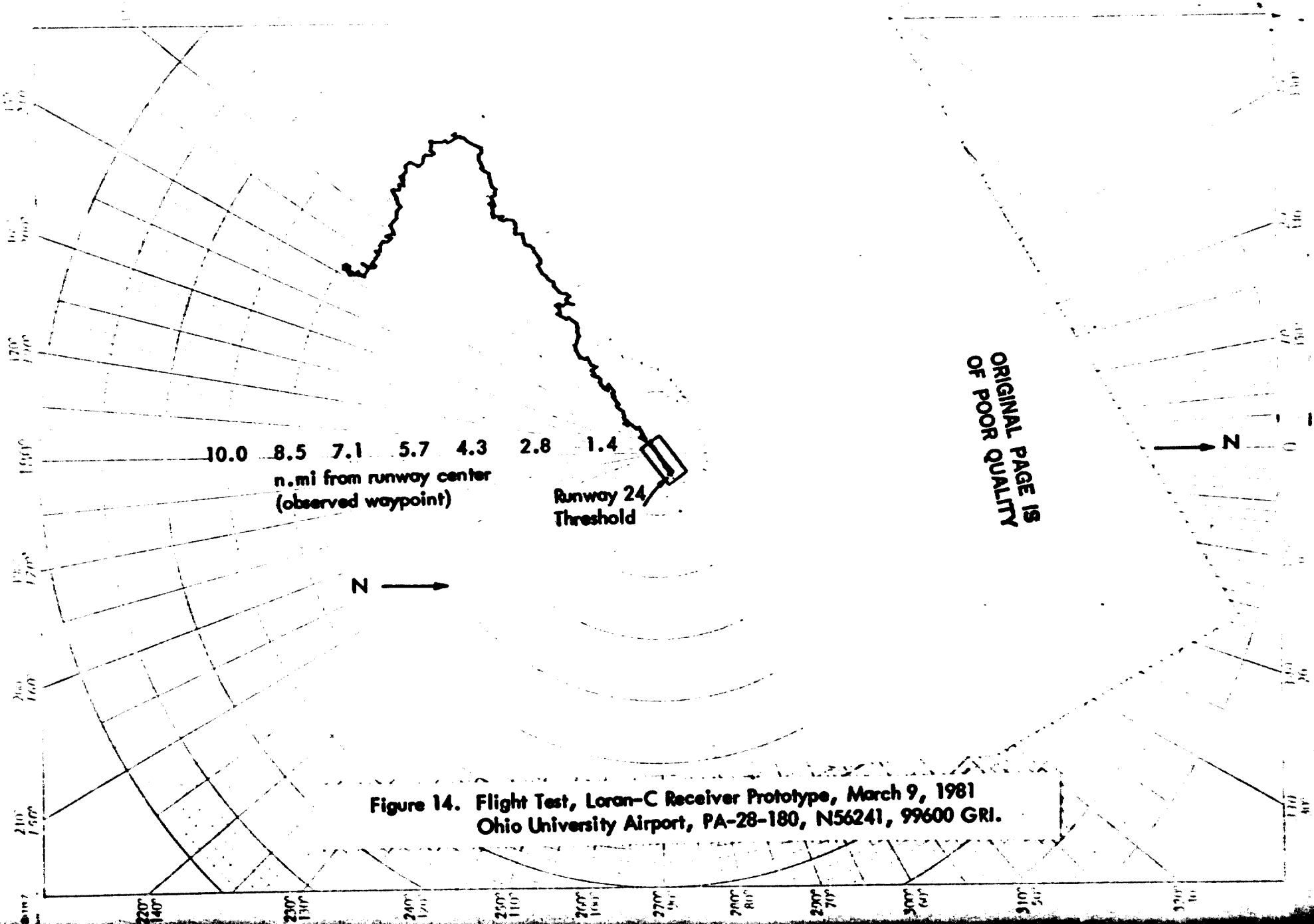


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Figure 14. Flight Test, Loran-C Receiver Prototype, March 9, 1981
Ohio University Airport, PA-28-180, N56241, 99600 GRI.

IX. CURRENT WORK IN PROGRESS

Tracking loop software changes are contemplated for five-station tracking with master independence. Decoded warning messages will be provided when the master 9th-pulse blink code is available. All valid time differences will be made available to the coordinate-conversion and area-navigation software, so that composite position fixes will be possible.

Initial flight evaluations have shown encouraging results, especially with regard to repeatability. Absolute accuracy in the first field tests suffered due to variations in signal strength among stations. A computer-controlled AGC, acting on each Loran-C envelope pulse and commutated among active stations, has been designed and is under test as of this writing. Initial results show marked improvement, with receiver bias reduced over 75% from operation without AGC, on the 9960 chain in southeastern Ohio.

The latitude/longitude and range/bearing coordinate conversion circuitry and software have been used routinely in receiver evaluation; the documentation for this portion of the receiver will appear [9] as a M.S. thesis in the near future.

Additional flight evaluations are planned, using ground-based radar for position reference data. Techniques and procedures for differential Loran-C are also under study, to determine whether receiver cost may be minimized by permitting a differential setting periodically during a flight, or prior to an approach.

X. ACKNOWLEDGEMENTS

The prototype Loran-C receiver is being developed under Grant NGR-36-009-017, supported by NASA Langley Research Center. Ralph W. Burhans, Project Engineer, developed receiver antenna preamplifier and RF processor units, with support from student intern James Roman. Tracking loop software development, and keyboard interface were supported by intern Stan Novacki. M. S. Candidate Joe Fischer contributed the time-difference to latitude-longitude conversion hardware and software, and intern Steve Yost developed power supply and commutated AGC circuitry.

Personnel are members of the NASA Joint University Program in Air Transportation Systems at Ohio University; the program is carried out in cooperation with similar teams operating at MIT and Princeton University. [10]

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