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SPECIAL REPORT

entitled

POST HEAT TREATMENT EFFECTS ON DOUBLE LAYER METAL STRUCTURES FOR VLSI APPLICATIONS

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

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I. INTRODUCTION

The increasing demands toward greater packing densities in LSI and VLSI make it imperative that multilevel metallization systems be developed. Although several reviews have been written [1-7], the realization of reproducible and reliable results have yet to be forthcoming. The most common problem associated with double layer metal has been the inability to make electrical contacts between metal layers through via holes etched in the dielectric to provide electrical communication between metals. The problem is more acute when the number of vias is large (>500) and are relatively small in size ($\leq$0.2 mil square). Another, less important problem is associated with shorts between metal layers due to pinholes in the dielectric film, thin spots, or poor coverage of hillocks in the first level metal. An example of the use of double layer metal for circuit application [8] is given in Figure 1.

In order to study the effects associated with double layer metal structures having a large number of small vias, a test pattern was generated consisting of a string of 560 vias. The via size was varied from 0.5 mil square to 0.2 mil square per string. Electrical measurements were made on the test pattern after initial sintering and subsequent heat treatments in order to monitor contact resistance behavior and variations in yield. Metal interconnects between vias were typically 0.7 mils wide although samples were also prepared and tested having interconnects of 0.4, 0.5, and 0.6 mil wide Al, with little or no variation in results.

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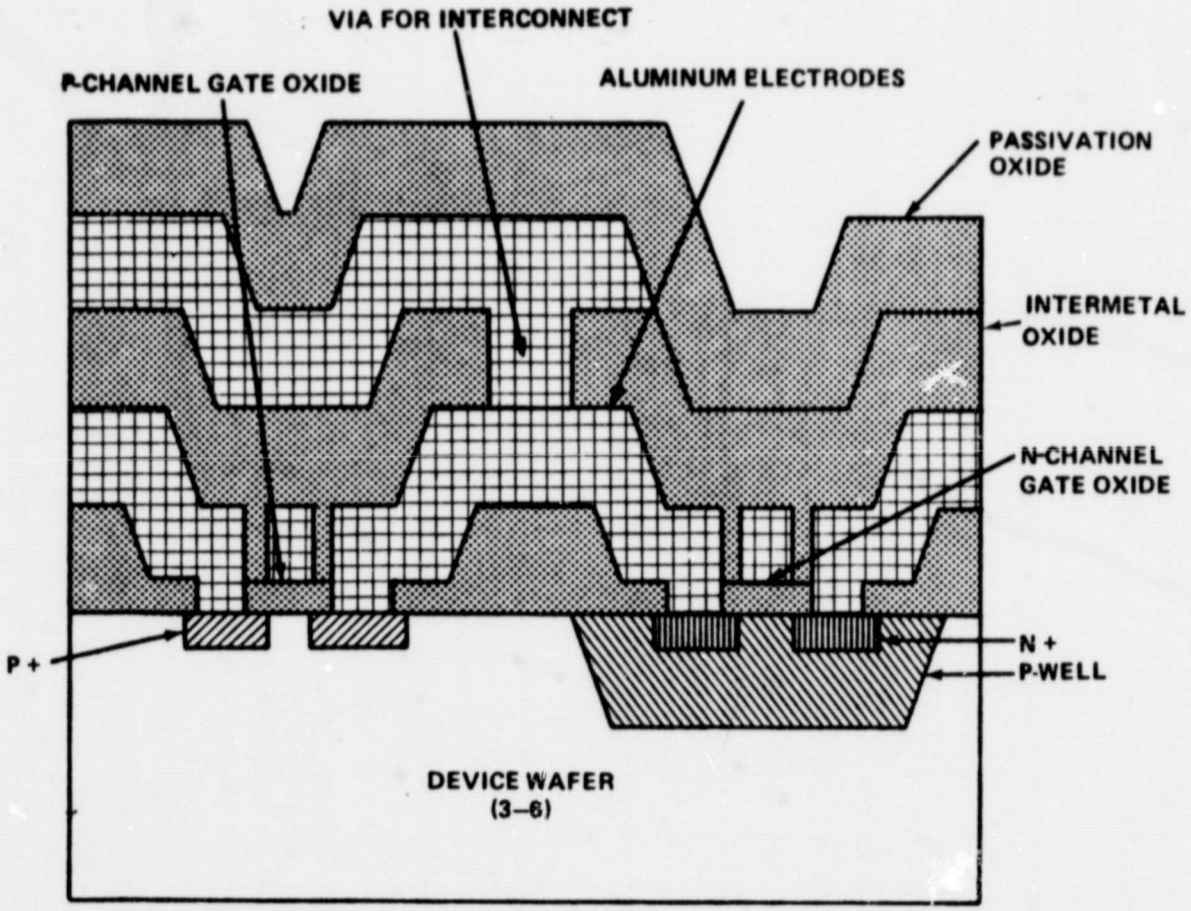

Figure 1. An example of the use of double layer metal in the realization of an aluminum gate C-MOSFET structure.

II. PREPARATION OF TEST VEHICLE

The steps involved in preparing the test vehicle consist of the following. The starting material was 3-8 ohm-cm, (100) oriented, n-type phosphorous doped silicon wafers. A field oxide was thermally grown in dry O_2 for 5 minutes, boiling H_2O for 60 minutes and then dry O_2 for an additional 15 minutes at 900°C resulting in an oxide thickness of 14^{K}Å . Prior to depositing the first layer metal, a cleaning step was performed, this consisted of a one-minute dip in dilute HF: H_2O (1:10) at room temperature and a 10 minute rinse in deionized water. The wafer was then dehydrated at 900°C in an N_2 ambient for 10 minutes. The first metal layer was d.c. sputtered structural grade Al alloy 6061 of 0.5μm thickness. The metal was patterned using conventional photolithographic techniques with Waycoat-31 negative photoresist.

Prior to depositing the dielectric, scribe lines (0.7 mils wide) were etched around the test patterns through the thermally grown field oxide down to the silicon substrate. These lines were used as an etch end-point monitor in etching vias in the intermetal dielectric.

The intermetal oxide was next deposited at 400°C using CVD of SiH_4 (4% in Ar) and O_2 (and later P_2O_5 of approximately 3 mole percent) to a thickness of 8^{K}Å . Dielectric thickness was measured with an (laser) ellipsometer. Vias were etched in this dielectric film with buffered HF using standard photolithographic masking. This etching was done first by dipping the wafers in a stirred

solution of etchant, using the scribe lines as reference to determine when etching was completely through the dielectric film. In later processes, this etching was done ultrasonically in a totally enclosed container.

The second layer metal was also deposited using dc sputtering of the same target used in the first layer metal and patterned. Typically a 15 minute aluminum sintering process at 470°C preceded the first testing of the completed test vehicle.

III. EXPERIMENTAL RESULTS

Approximately 50 wafers were processed. Each wafer had 200-220 test patterns with via sizes ranging from 0.2 mils square to 0.5 mils square. Table I represents a summary of results in terms of percent yield obtained for each via size as a function of fabrication process. Process A through L are explained below. Among other variables it will be noted that each process is characterized by an etch time associated with etching the vias in the intermetal dielectric film. The scribe lines were used as reference. When all dielectric was etched from these scribe lines, this was defined as the 'break' time. Any additional etching beyond this break time is measured in seconds.

Process Definitions:

A. Wafers were processed as described in section II. The width of the first level metal interconnect of 0.4, 0.5, 0.6 and 0.7 mils corresponded to test patterns having square vias of 0.2, 0.3, 0.4 and 0.5 mils, respectively. The width of the second metal

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	Percentage Yield Via Resistance for 560 Vias < 20 Meg Ohm Process Identification											
Via Size	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	81	76	95	98	99	98	94	84	94	98	98	98
0.4 mils	70	56	88	94	97	98	92	82	89	90	97	97
0.3 mils	61	53	64	85	93	94	92	83	87	80	100	100
0.2 mils	40	13	64	82	91	94	93	89	72	67	98	98

Table I-A

	Percentage Yield Via Resistance for 560 Vias < 10 Kil Ohms Process Identification											
Via Size	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	17	59	86	97	97	94	84	61	92	93	98	98
0.4 mils	8	48	73	89	94	96	88	64	82	90	97	97
0.3 mils	0	30	45	64	89	92	88	74	85	80	100	100
0.2 mils	0	14	13	26	44	59	64	52	38	67	98	98

Table I-B

	Percentage Yield Via Resistance for 560 Vias < 1 Kil Ohm Process Identification											
Via Size	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	0	59	78	85	86	82	74	56	92	92	98	98
0.4 mils	0	46	47	66	72	72	68	54	82	90	97	97
0.3 mils	0	28	85	36	47	55	58	56	85	80	100	100
0.2 mils	0	8	10	15	22	27	30	30	32	67	75	98

Table I-C

Table I Percentage yield as a function of processing with via size as a parameter for contact resistance of 560 vias less than 20 Megohm, 10 Kilohm, and 1 Kilohm for tables I-A, I-B, and I-C, respectively.

was 0.7 mils. Via etch time was break plus 10 seconds.

B. Wafers were processed as described in section II. The metal interconnects on both levels were 0.7 mils wide. (This is true for all processes B through H). Via etch time was break plus 10 seconds.

C. Wafers processed as described in section II with via etch time in stirred dielectric etchant extended 20 seconds beyond break time.

D. thru H. correspond to wafers processed as described in section II but with via etch time in stirred dielectric etchant extended 40, 60, 80, 100 and 120 seconds beyond break, respectively. (Note that the values given for processes A through H represent an average of five different process runs of eight wafers for each run.)

I. Wafers processed as described in section II but having a phosphorous doped intermetal dielectric of 3.1 mole percent (as determined by Auger spectroscopy) and with vias etched in stirred dielectric etchant for 20 seconds beyond break.

J. Wafers processed as described in I above except via etching was done ultrasonically in a closed container for 20 seconds beyond break.

K. Wafers processed as described in J above with the addition of a first level metal cleaning step through the vias prior to depositing the second level metal. The metal cleaning solution consisted of an ethylene glycol-buffered $HF-H_2O$ solution for the removal of Al_2O_3 from the first level metal prior to deposition of second level metal[10].

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L. Wafers processed as described in K above but having undergone a one-half hour post heat (sintering) treatment at 490°C.

The results of processes C through H are displayed graphically in Figure 2. The data are shown in Tables IA, B, and C which give the percent yield for via contact resistances less than 20 meg-ohms, 10 kil-ohms and 1 kil-ohm. It is desirable to have minimum contact resistance (i.e. less than 250 ohms) since as the number of vias increase from 600 to approximately 3000 for a VLSI circuit, the resistance will increase proportionately. Any pattern having a contact resistance greater than 20 meg-ohm is assumed to be an open-circuit in Table I.

Wafers processed as described in D in Table I were used for an Auger surface analysis of the first level metal through a 0.5 mil via just prior to depositing the second level metal. The purpose of the Auger analysis was to determine what insulating materials reside on the surface of the first level metal which prevented good low resistance ohmic contact between metal levels. The results of this analysis indicated the following materials were present with an accuracy of ± 5%:

Al_2O_3	64%
C	31%
N	1.8%
Mg	1.3%
Si	0.6%
F	0.6%
S	0.7%
O (other than Al_2O_3)	<0.1%

For this contact, the amounts of Mg and Si were about the same as

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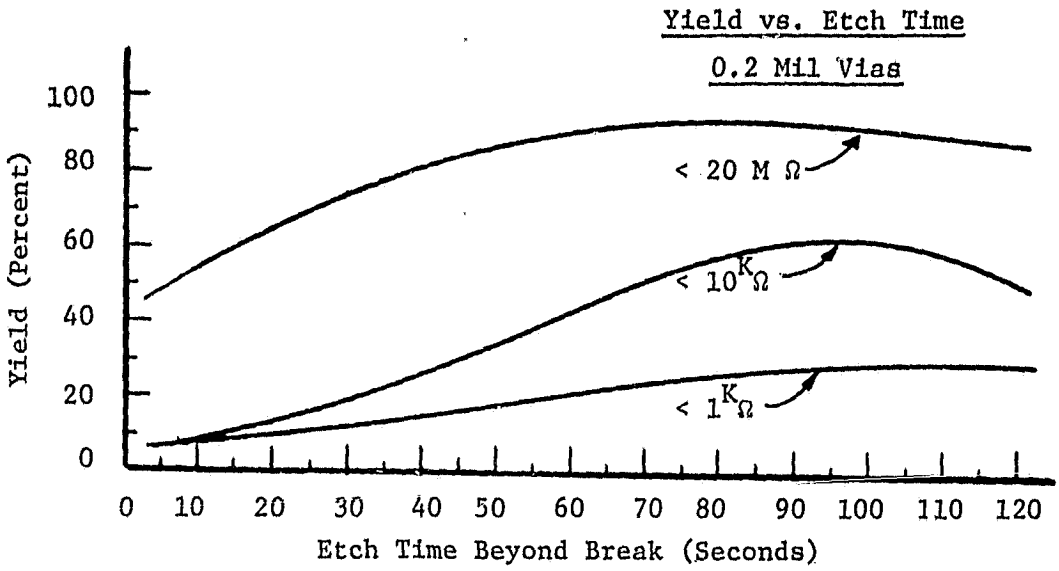

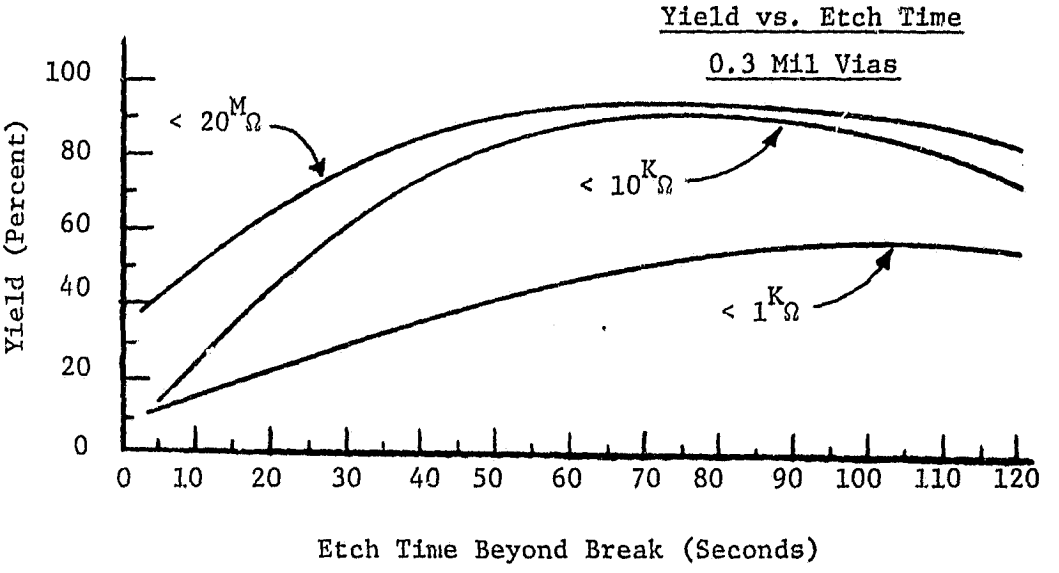

Figure 2. Percent yield as a function of etch time beyond break with via size as a parameter. Intermetal dielectric etch accomplished with stirred B.O.E.

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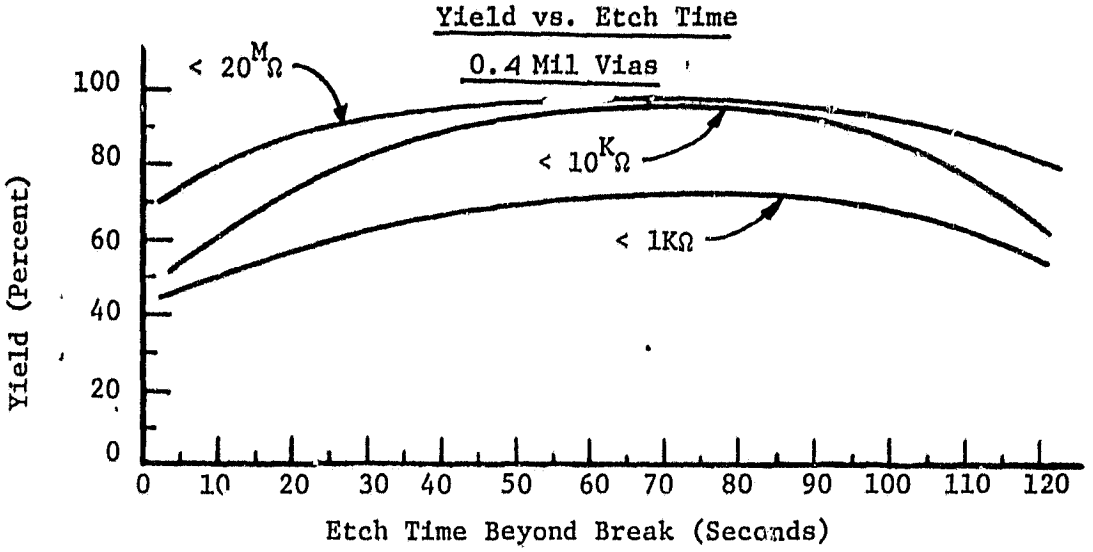

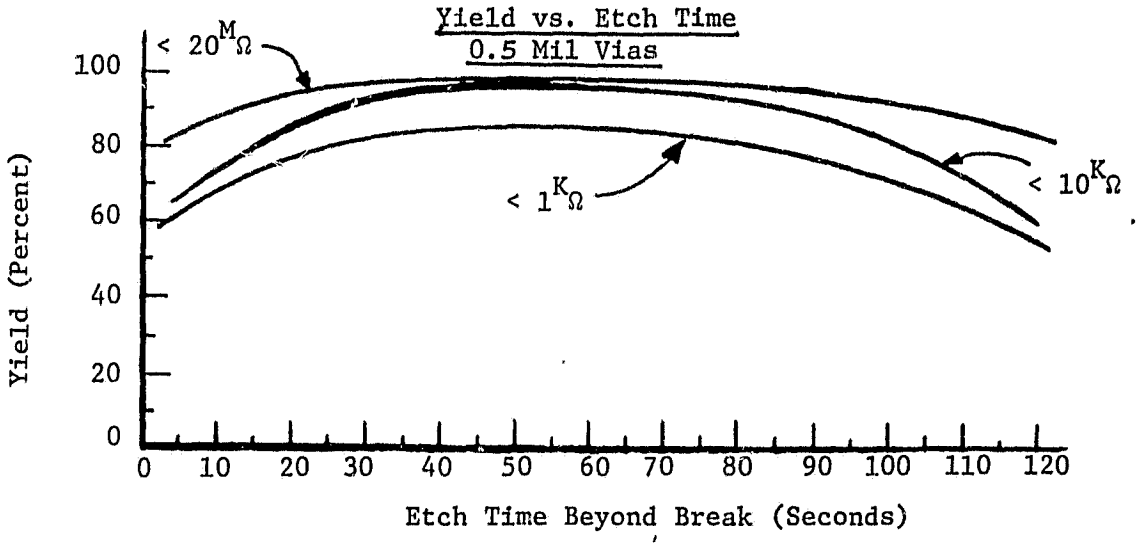

Figure 2. (continued). Percent yield as a function of etch time beyond break with via size as a parameter. Intermetal dielectric etch accomplished with stirred B. O. E.

the bulk Al alloy so there did not seem to be any surface enrichment of Mg_2Si which was suspected as a source of the high resistance. When about 100Å of this surface was removed by ion etching, the N,S,F, and C were greatly reduced, which suggested that they may be a source of interfacial contamination.

The large percentage of carbon measured (31%) is believed to be a result of the photoresist leaving a carbon residue on the wafer. The composition of this photoresist could not be obtained from the manufacturer.

It should be noted that the composition of the structural grade Al 6061 consist of the following impurities:

Si	0.4 - 0.8%
Cu	0.15 - 0.4%
Fe	0.7%
Mg	0.8 - 1.2%
Mn	0.15%
Cr	0.15 - 0.35%
Zn	0.25%
Ti	0.15%

The primary reason for using this Al alloy was for the prevention of hillock formation.

Post heat treatment or sintering of a wafer exhibiting an initial poor yield (i.e. less than one kil-ohm for a chain of 560 vias in series) can increase the effective yield by 500 to 700% as illustrated in Figure 3 for wafers 10H and 2W. These wafers were processed as in 'C' above, having only a 15 minute 470°C sintering before initial testing.. All addition sintering was done at 490°C in a nitrogen ambient.

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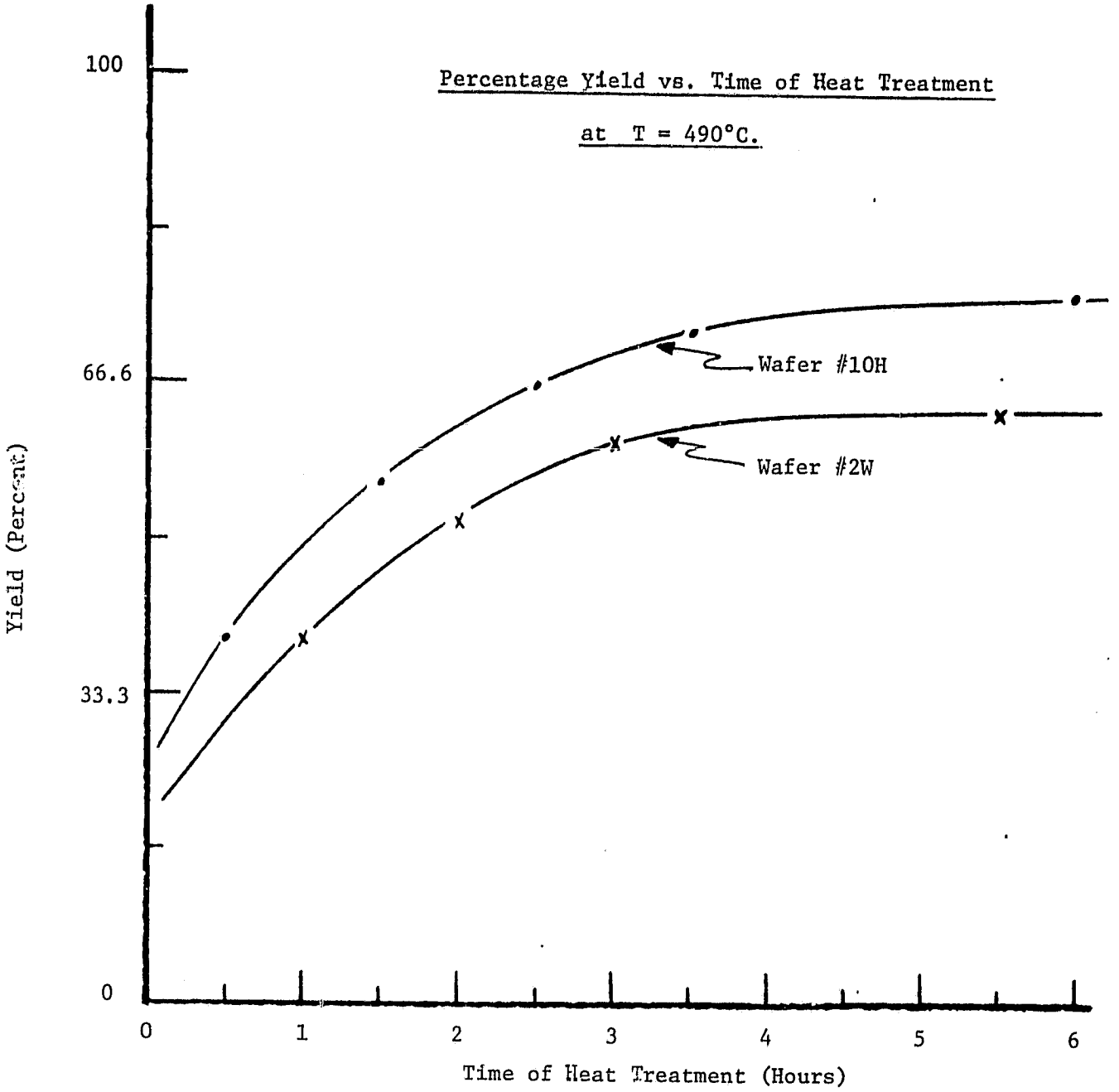

Figure 3. Percentage yield of number of chips less than 1 kil ohm as a function time of heat treatment at 490°C for wafers with undoped intermetal dielectric.

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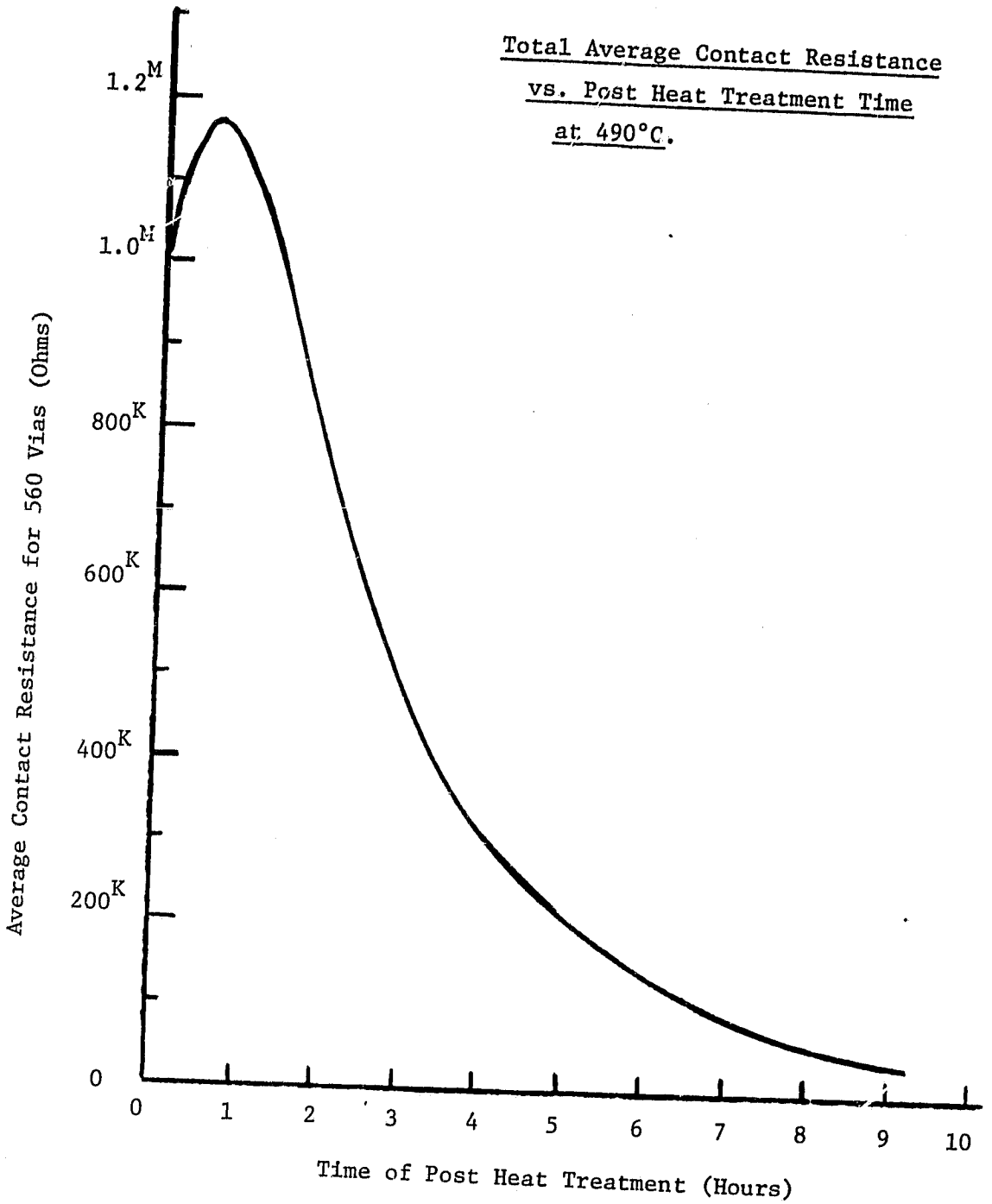

Figure 4. Average contact resistance for 560 vias of all 0.5 mil square chips as a function of post heat treatment time for wafer #2W. (Total number of chips = 55)

The primary reason for this increase in yield with post heat treatment is due to the fact that the Al-to-Al contact resistance decreases with sintering, as demonstrated in Figure 4. Here, the average resistance for all test patterns having 0.5 mil square vias (approximately 55 of the total 212 chips) is plotted as a function of sintering time. As the time of sintering increases, the number of test patterns having a contact resistance < 1 kil-ohm increases, hence the yield increases.

On an individual chip basis, the contact resistance for 560 vias per chip behaved as shown in Figure 5. For a given wafer which initially exhibits a relatively poor yield, the number of chips behaving in the manner shown for chips #10C and 10W was approximately 51%, those behaving like chip #10R was 27% and those like chip #10T was 10%. The remaining chips either exhibited low initial contact resistance (<300 ohms) or were open-circuited (>20 meg-ohms). Those chips initially exhibiting a low contact resistance generally had their resistance lowered with increasing heat treatment, however a few chips showed a gradual increase in resistance with increased heat treatment time as shown in Figure 6. It is believed that this increase in resistance is due primarily to the consumption of Al by SiO_2 to lessen the Al thickness. Since at 490°C Al reacts chemically with SiO_2 to form Al_2O_3 and free Si, Al is consumed at a rate of 210Å/hr. [15]

The most predominant trend found in sintering of double level metal test patterns is demonstrated in Figure 7. As inferred

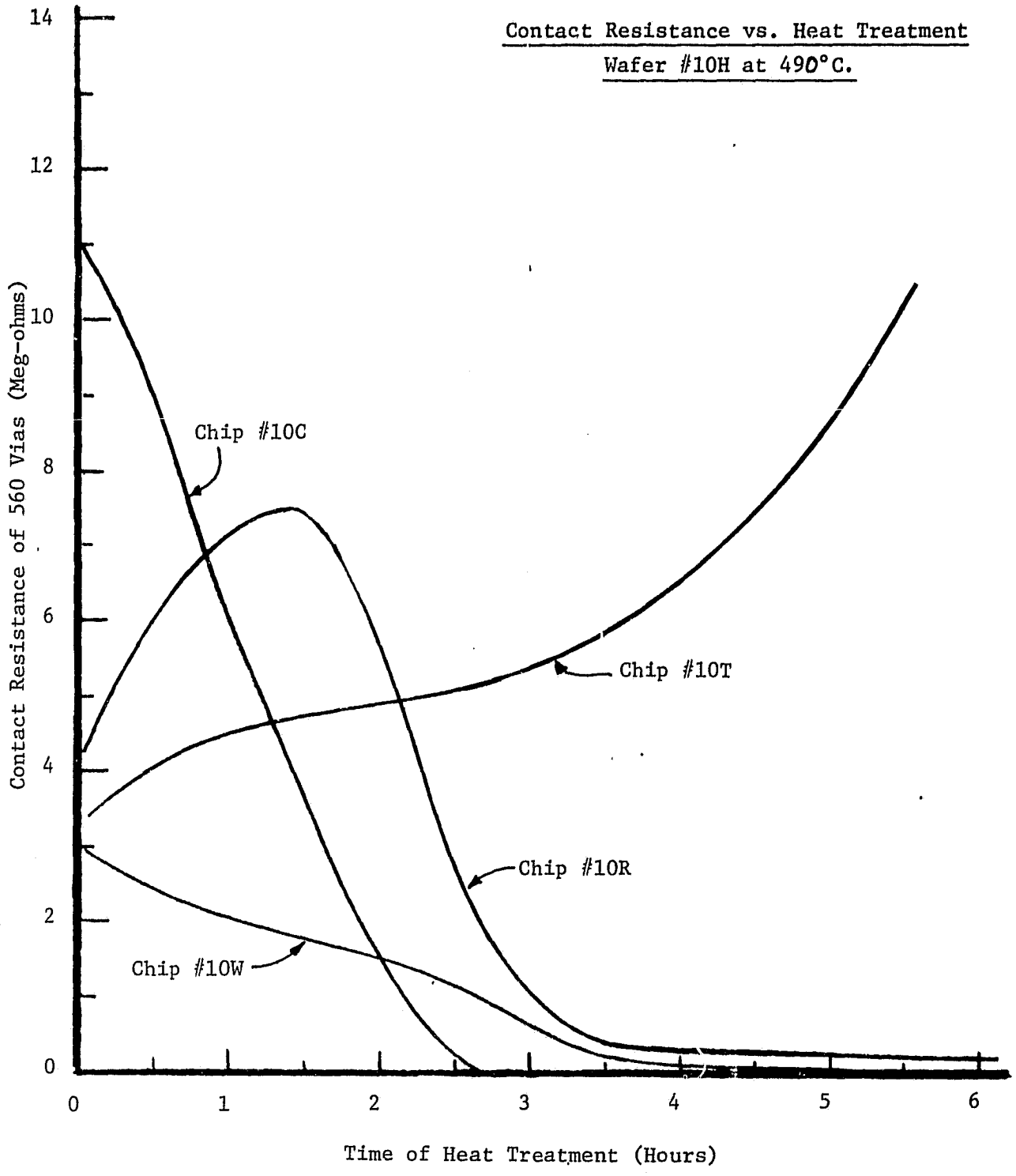

Figure 5. Contact resistance of 560 vias as a function of heat treatment time for several different chips of wafer #10H at a temperature of 490°C.

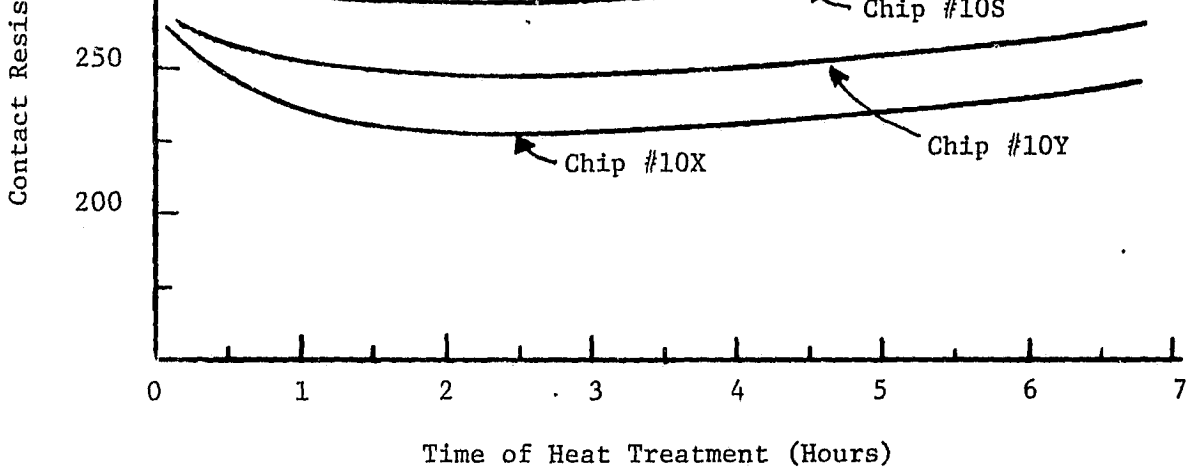

Figure 6. Contact resistance of 560 vias as a function of heat treatment time for wafer #10H showing slight increase in resistance with time of heat treatment for ~6% of the chips on the wafer.

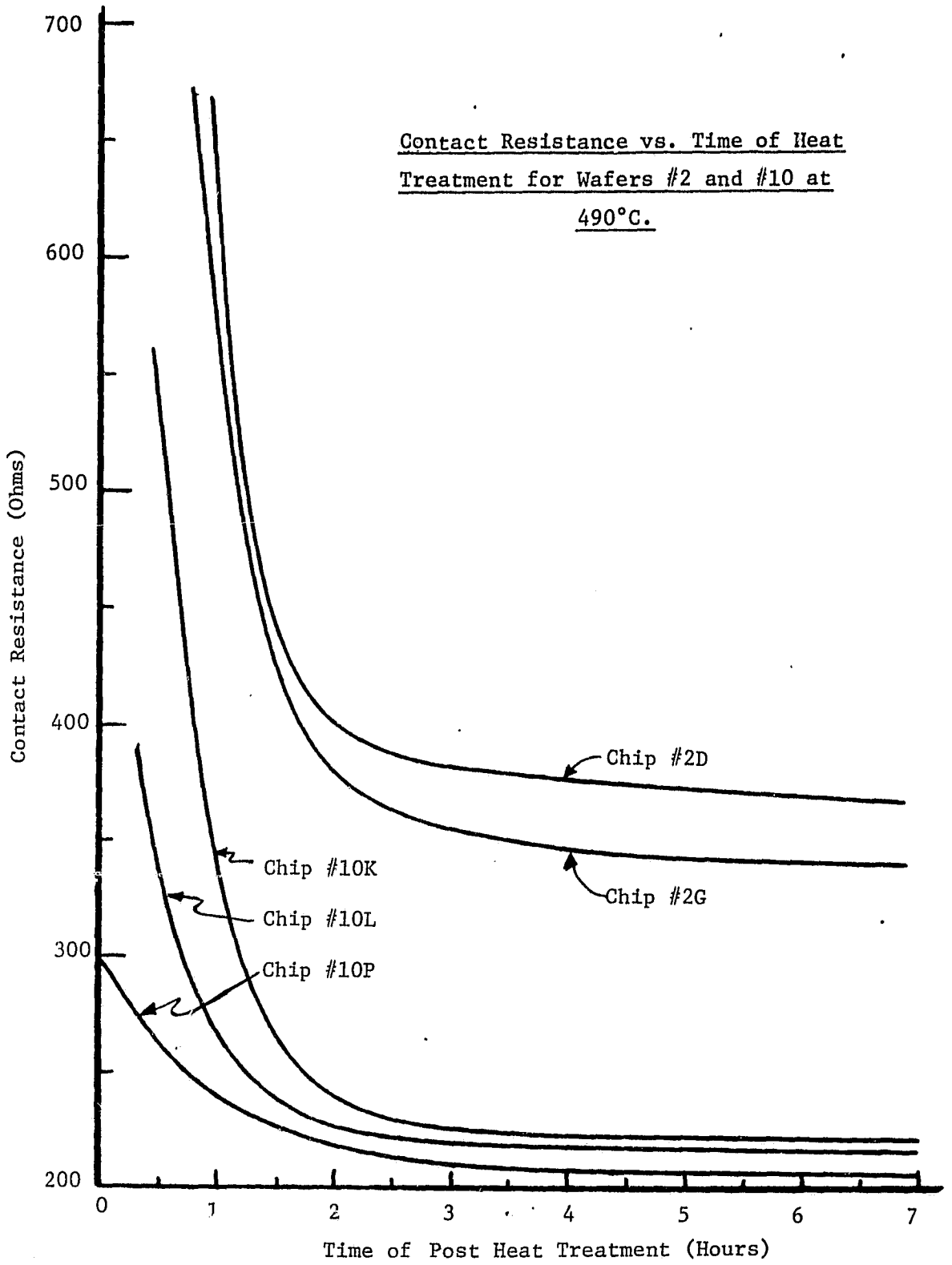

Figure 7. Contact resistance trends as a function of heat treatment time for wafers #2 and #10.

from this plot of contact resistance as a function of post-heat treatment for these two wafers, the average contact resistance decreases drastically for the first few hours of sintering. Because of this feature, the realization of multiple level metal LSI having a large number of vias (>2000) is a distinct possiblity.

One major problem involved in post heat treatment of double layer metal structures is that the dielectric (C.V.D. - SiO_2) has a tendency to crack or "craze" at elevated temperatures (>500°C). This cracking, as illustrated in Figure 8, is due to excess stress on the insulating layer[9]. One method to lessen, if not-alleviate this problem, is to use a phosphorous doped dielectric of 3 to 5 mole percent. This increases the effective temperature for which sintering can be done before cracking is observed[9].

Using this phosphorous doped dielectric (also called phosphosilicate glass or PSG) resulted in a much higher yield as shown in Table I and also a considerable less contact resistance as shown in Figure 9. Here the average contact resistance as a function of via size is plotted for a test pattern with a doped dielectric layer for no heat treatment (curve B) and with 30 minutes post heat treatment at 490°C (curve A). These results are compared to the best results obtained for the undoped case (curve C), even after many hours of heat treatment. The table in the figure indicates resistance and percent yield for each case presented.

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A resistance map of the wafer shown in curve B is given below:

			173	159	154	217	161	143	158	196	176						
		170	171	∞	157	231	158	161	159	183	171	158					
	166	163	168	158	166	226	162	162	162	171	167	161	164				
	164	164	167	161	158	208	164	159	161	172	170	163	165	173			
	168	170	170	160	159	212	163	161	163	228	169	164	∞	172	164		
157	168	169	170	165	158	219	162	161	160	234	168	163	163	170	160		
164	170	170	171	164	156	213	161	163	159	221	173	159	163	170	165		
112	173	201	176	164	151	143	173	∞	163	192	174	162	162	170	171		
164	175	375	181	167	159	405	172	162	158	181	167	161	164	167	165		
	177	202	182	169	159	211	164	161	154	176	164	160	156	166			
	176	216	184	171	161	228	169	158	154	∞	162	156	154	165			
	44	198	179	171	162	228	164	158	153	173	160	157	151				
		260	181	171	163	231	166	159	154	172	160	153					
				177	166	200	167	159	151	167	157						

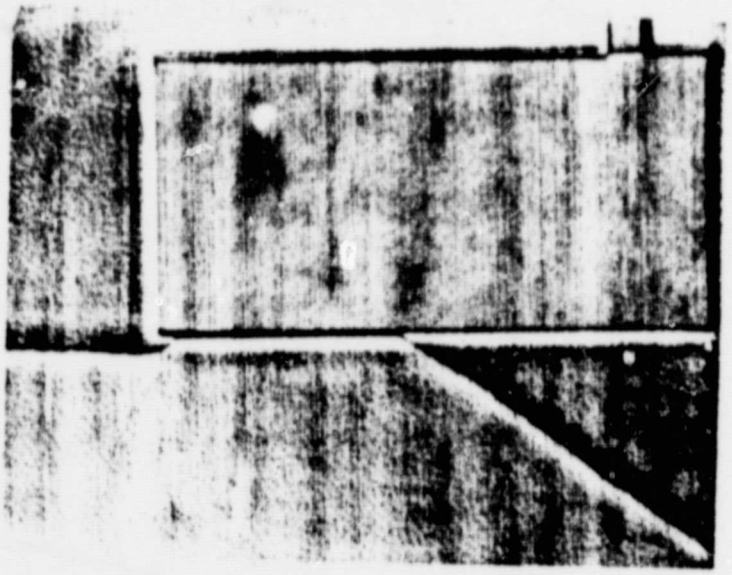
Via size	.4	.5	.2	.3	.4	.5	.2	.3	.4	.5	.2	.3	.4	.5	.2	.3	.4	

IV. ANALYSIS AND CONCLUSIONS

The following comments and conclusions may be derived from this investigation.

1.) The variation in width of the metal interconnects between vias had little influence on yield, as expected. It may have had a slight effect on total resistance, especially for the 0.4 mil compared to 0.7 mil wide interconnect, but this was not detectable. The major difficulty came in mask alignment of the smaller interconnects.

2.) The extension of the via etch time of the dielectric film for both the dipped (stirred) etching and the ultrasonic etching



Photomicrograph (A)

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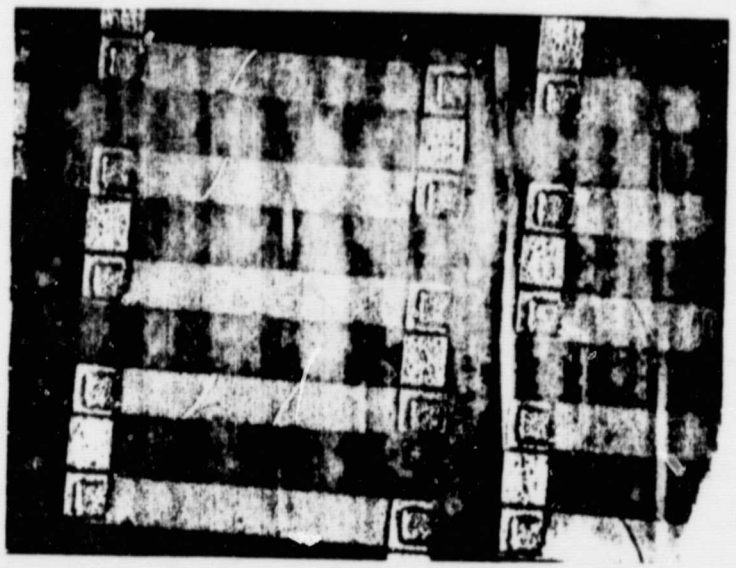

Photomicrograph (B)

Figure 8. Photomicrograph of test pattern at 300X magnification illustrating crazing tendency at temperatures >500°C and for fast pull from the furnace. Photomicrograph (A) shows crazing around a test pad whereas (B) shows crazing in the test pattern itself.

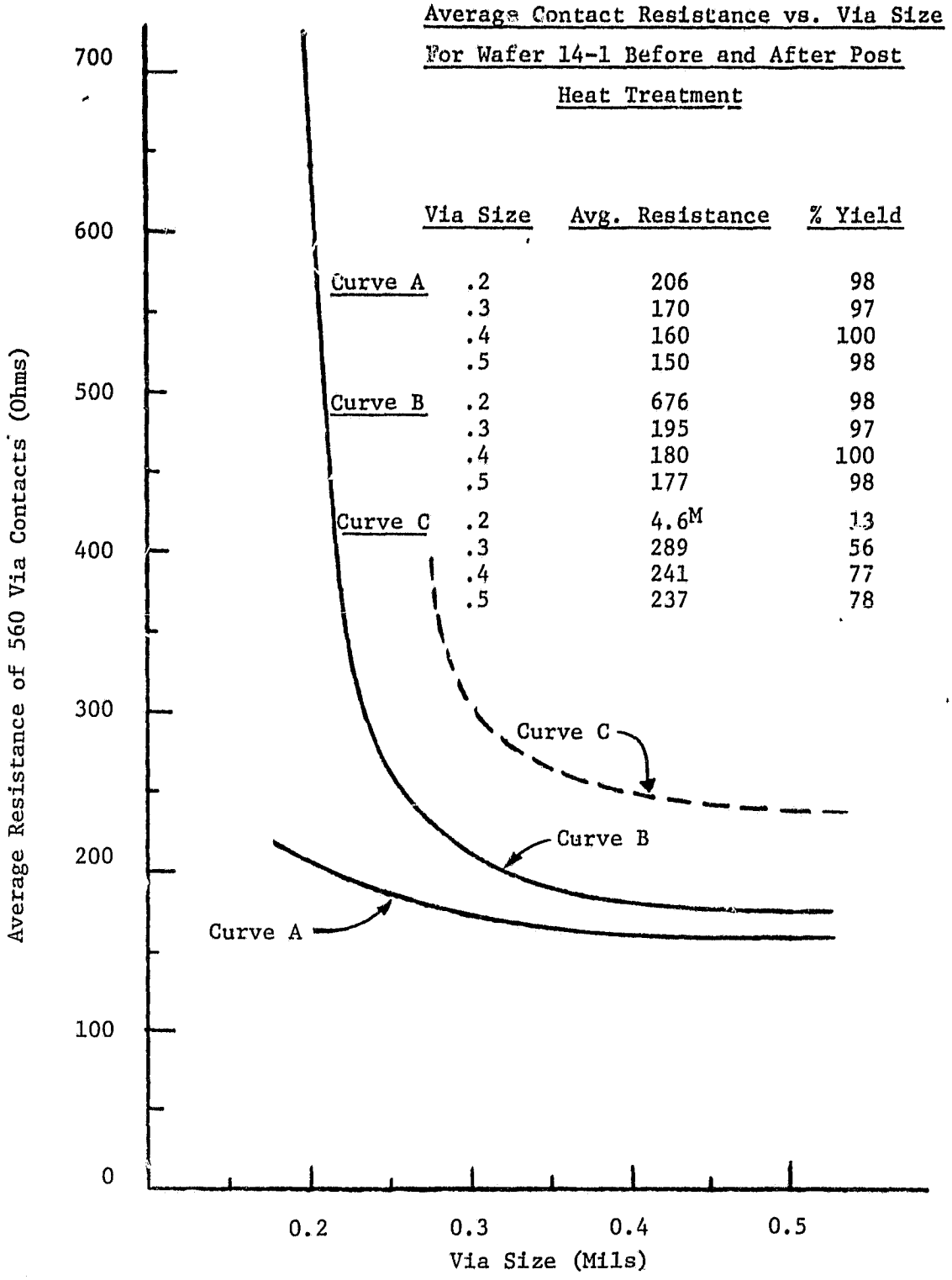

Figure 9. Average contact resistance vs. via size for wafer #14-1 having phosphorous doped intermetal dielectric before post heat treatment (curve B) and after 30 minutes at 490°C (curve A). For comparison with a wafer having an undoped dielectric, curve C represents such a wafer after undergone 8 hours of post heat treatment at 490°C. (Note contact resistance for 0.5 mil via of wafer in curve C prior to post heat treatment was 90 kilohms.)

indicated a substantial improvement in yield with only a slight undercutting for extended times below 90 seconds. (As expected, the doped dielectric etched faster than the undoped.) For etch times beyond break in excess of 110 seconds; the yield decreased. This is believed to be attributed to an increase in contact resistance- and thus a decrease in yield - due to a chemical reaction between the dielectric etchant and the alloys of the sputtered aluminum to form an insulating layer at the surface of the first level metal prior to depositing the second layer.

As indicated in Figure 2, the optimum etch time is dependent on the size via being etched.

3.) The addition of phosphorous doping to the oxide eliminated the possibility of intermetal dielectric cracking for post heat treatment temperatures below 500°C. A considerable increase in yield was also realized, having total average contact resistances slightly over 200 ohms for 0.5 mil vias and 250 ohms for 0.2 mil as per Figure 9. (A slow pull of the wafer from the furnace was also practiced to eliminate cracking.)

4.) The use of an ultrasonic etching bath for etching vias gives a much better probability of etching small vias (<0.2 mils). This etching was accomplished in a completely enclosed container.

5.) The chemical cleaning of the first level metal through the vias prior to depositing the second level metal also increased yield. The first layer Al develops a thin oxide coating as soon as it is exposed to the atmosphere and this oxide skin creates a high resistance upon depositing the second layer. This coupled with the

difficulty of removing all of the dielectric film from the via and the formation of oxides of the alloys contained within the Al all tend toward low yield, high resistance contacts. There are actually two approaches for solving this problem, back sputtering and chemical etching. Back sputtering has the advantage that the oxide thickness can in principle be reduced to zero if the subsequent metallization is applied without exposure to air. The disadvantages include: possiblity of radiation induced MOS damage; potential for contamination of the sputtering system; redeposition of previously sputtered materials especially from the substrate table; etc. The chemical etch procedure does not have these disadvantages, but the oxide thickness can never be reduced to zero.[14]

The use of a 1:1:1 ethylene glycol: buffered -HF : H_2O etch removes all but 30-50 Å of oxide[10] without attacking the Al. (The second layer sputtered Al can easily penetrate this oxide thickness to form good ohmic contacts.) This etch was done just prior to second level metallization.

6.) The application of post heat treatments can drastically increase yield by lowering total via contact resistance. There are several possible reactions which could occur to cause this temperature effect.[11] Aluminum could react with aluminum oxide in the film between the layers to form various aluminum suboxides and thus break up the continuous layer of dielectric. Alternately, the recrystallization of aluminum in both of the levels could mechanically disrupt the thin native oxide layer, therefore forming aluminum-to-aluminum contact. As yet, there is no evidence for this

speculation.

Figures 4 and 5 indicate that in some cases the contact resistance increases with post heat treatment time prior to the "diffusion" through this 'interfacial contamination' by the two layers of aluminum. If this contamination were SiO_2, then it could be said that there exists excess ionic silicon in the oxide which becomes tied-up upon the application of post heat treatments[12]. Since the contamination is probably Al_2O_3, one might say there exist excess ionized Al in the oxide which reacts with the oxidizing species during the sintering process, thus decreasing the total ionic charge in the oxide layer causing the net resistance to increase.

7.) Testing the via test pattern can be tedious. For high resistance vias the measured resistance was seen to be both light sensitive and current sensitive. As a result, all testing was accomplished in the dark. Ideally, very low testing potentials are applied in order not to break down a barrier layer thus turning a defective via into a good one. Also, theoretically, vias should not be tested in series, since the entire applied voltage will be dropped across a defective via, probably causing it to break down and appear good. However, in our testing, all vias were measured at once in series using a digital voltmeter.

8). Recently, a new planar multilevel interconnection technology was introduced [13] using polyimide films. Although this procedure appears to be very promising for future applications if taken at face value, it is felt there is still many facets of "magic"

associated with it.

V. ACKNOWLEDGEMENT

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