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CHARACTERIZATION OF SILICON-GATE CMOS/SOS INTEGRATED CIRCUITS PROCESSED WITH ION IMPLANTATION

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16. Abstract

This final report describes the double-layer metallization technology applied on p-type silicon-gate CMOS/SOS integrated circuits. A smooth metal surface was obtained by using the 2% Si-sputtered Al. More than 10% probe yield was achieved on Solar-Cell Controller Circuit TCS136 (or MSFC-SC101).

Reliability tests were performed on 15 arrays at 150°C. Only three arrays failed during the burn-in, and 18 arrays out of 22 functioning arrays maintained the leakage current below 100 μA. Analysis indicates that this technology will be a viable process if the metal short-circuit problem between the two metals can be reduced.

17. Key Words (Selected by Author(s))

Double-Layer Metallization
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SUMMARY

Double-layer metallization technology was applied on P-Gate CMOS/SOS integrated circuits, Solar-Cell Controller TCS136 or (MSFC-SC101). Prior to the metallization, the wafers were fabricated using the all-ion-implantation process developed in the previous year under the same contract. The first-layer metal is 2% Si Al (S-gun) alloy, and the second-layer metal is a filament-evaporated pure Al. The interlayer oxide is low-temperature (450°C) silane-oxide.

The wafers produced showed $V_{tn} = 0.76 \pm 0.23$ V, and $V_{tp} = 0.87 \pm 0.11$ V, both measured at $I_d = 10$ μA. Optical and SEM measurements indicate that the first-layer metal is very smooth which is an essential quality for this technology in reducing electrical short circuits between the two metal layers. The second-layer metal is continuous over the step of the first-layer metal. Contact resistance between two metals through 7.6 μm x 7.6 μm via-hole openings is 1.5 to 4.0 Ω. This is 20 to 50% of poly-to-metal contact resistance. However, this is somewhat higher than expected and could be reduced by employing better technology such as an in situ back-sputter Al etch prior to the deposition of the second-layer metal.

The probe yield on the two lots was 10%. Ninety-six of the 132 packaged arrays passed final tests. Of these, 25 arrays with less than 100-μA leakage current were selected for burn-in life tests.

The burn-in tests consisted of three bias cycles: (1) 168 h at 125°C, (2) 72 h at 150°C, and (3) 168 h at 150°C.

Only three arrays failed the burn-in tests, probably due to a metal-1 to metal-2 short through the interlayer oxide. The remaining 22 arrays functioned very well, and 18 of these maintained leakage current below 100 μA.

I. INTRODUCTION

The objective of this work is to study the implementation of all-ion-implantation technology in processing the Marshall Space Flight Center (MSFC) double-layer metal Standard Transistor Array Radix (STAR) circuits on both silicon-on-sapphire and aluminum-gate bulk-silicon substrates. A major advantage of this process is in the reduction of interconnect resistance (no poly with high resistance) which improves circuit performance. Chip density can also be measured by as much as a factor of 1.5 to 2.0, because less real estate is necessary for routing the metal lines.

The Solar-Cell Controller Circuit TCS136 (or MSFC-SC101) is used as a demonstration vehicle for the study of a double-layer aluminum metallization system and the reliability of the resulting circuit. This demonstration vehicle was designed by NASA using their STAR design. The STAR design is similar to RCA's Universal Array concept, and the same mask sets are used for both silicon-gate CMOS/SOS or aluminum-gate bulk-silicon technology.

The TCS136 (MSFC-SC101) mask set was designed and fabricated at MSFC's facility and then delivered to RCA. Wafers were fabricated at RCA to a point of metallization and then shipped to MSFC for the processing of the multilayer metal system. Some were fabricated at RCA. The results presented in this report are based on the data taken from wafers fabricated at RCA. After wafer fabrication the wafers were circuit-probed and inked at MSFC using a Macrodata tester. The marked wafers were returned to RCA for laser scribe and packaging.

The procedures for testing TCS136 were developed at RCA using the Datatron tester, and these procedures were used to evaluate reliability during the burn-in test. The circuit probe yield of the TCS136 was over 10% on two lots. The life tests indicate that the weak area of this technology is the possibility of an electrical short circuit between the two metal layers; however, 88% of total arrays passed the 168-h burn-in at 150°C.

This technical report covers the work performed by RCA Solid State Technology Center, Somerville, New Jersey, under Contract NAS8-31986 from July 1, 1977 to June 30, 1979. The contract was administered under the technical direction of John Gould and Donald Routh, Marshall Space Flight Center, AL 35812.

Contributors to this report are J. S. Mack for silicon film deposition, S. G. Policastro for wafer processing, and D. Brown for the life test. Appreciation is also due to J. J. Di Piazza for monitoring various processing steps, and K. Phelps for writing the Datatron Test Program and assisting in the test and analysis of test data.

II. ALL-ION-IMPLANTATION PROCESS

A. Process Description

Initially, a silicon film is grown on $(1\bar{1}02)$ sapphire substrate in the standard manner with no intentional doping. Phosphorus is then implanted at a dose of 1.8×10^{11} cm^{-2} at E = 150 keV. A thin oxide (500 Å) is grown and etched with the both-islands mask to delineate both NMOS and PMOS transistors. This thermal oxide is then used as the etch mask for the silicon etch. The PMOS islands are shielded with photoresist and boron is implanted to control the NMOS threshold voltage. The photoresist and mask-oxide are then stripped.

A 110 ±5-nm-thick thermal oxide is next grown in HCl steam at 940°C, and a 500-nm-thick polysilicon layer is deposited and doped with a heavy boron implant. Oxide is deposited, patterned, and the polysilicon is etched by means of a plasma processing operation. A 1-μm-thick aluminum shield film is deposited and etched by the use of the n^+ mask. After stripping of the photoresist, a thin aluminum (20 ±5-nm-thick) film is deposited. This is to discharge the surface ions during implantation to protect the silicon film and sapphire substrates from damage. Source-drain implantation is then performed. The PMOS islands are shielded during the above implantation process. Similarly, the PMOS source-drain implantation is performed by using the p^+ mask. After stripping off the shield film, a 800-nm-thick field oxide is deposited. All of the implanted impurities are activated simultaneously for 15 min at 1050°C; also, the oxides are densified and the surface states are annealed. This completes the five implantation steps, and the schedules are summarized in Table 1.

The first-layer aluminum, deposited after contacts are opened in the normal manner, is 0.8 μm thick. Two percent Si-Al deposited by using a S-Gun and is patterned with a Metal-1 mask. Low-temperature SiH_4 oxide is deposited at 450°C as an interlayer insulator, and then via-holes are

TABLE 1. ION IMPLANTATION SCHEDULE USED ON LOT S1998 AND LOT S2010 OF TCS136 (MSFC-SC101)

IMPLANTATION		ION SOURCE	DOSE (cm^{-2})	ENERGY (keV)
Substrate $2I^2$(NP/N)	P/N - Well	Phosphorus	$1.8x10^{11}$	150
	P - Well	Boron	$2.0x10^{11}$	100
Polysilicon-Gate	P^{++}	Boron	$5.0x10^{15}$	50
Source-Drain	N^+	Phosphorus	$1.0x10^{15}$ $1.0x10^{15}$	170 70
	P^+	Boron	$3.0x10^{15}$	70

etched using the normal bond-pad etch to avoid attack on the aluminum. The quality of this oxide film is very important because any pinhole may cause an electrical short circuit. A second-layer aluminum is then deposited, and extreme care is required at this step to maintain low resistance contacts between these two metal layers. The second-level aluminum is deposited by filament evaporation; however, it is preferable to use sputtered aluminum with a slight in situ aluminum sputter-etch prior to deposition for better ohmic contact between the two layers. The top-layer aluminum is patterned with a Metal-2 mask. A protective oxide is deposited and then etched by using the bond-pad mask. The process is completed after alloying, and the wafers are ready for evaluation. The various thicknesses in the double-layer metal structure are shown below:

Metal-1	0.8 μm	2% Si-Al (S-Gun)
Interlayer Oxide	0.6 μm	Low-temperature Oxide
Metal-2	1.2 μm	Pure Aluminum (Filament)
Protective Oxide	0.6 μm	Low-temperature Oxide

B. Experiments

Experiments were performed on Lots S1998 and S2010 which are the double-layer metallization. The first-layer metallization was split into a three-way experiment: (1) the in situ-doped p^{++} polysilicon film which was deposited at RCA; (2) the 2% Si-sputtered Al which was deposited at RCA; and (3) the sputtered Al layer deposited at MSFC.

The details of the experimental matrix are summarized in Table 2. As shown in the table, six wafers (Group A and Group B) were completed at RCA, and another six wafers (Group C) were sent to MSFC for the various metallization experiments.

TABLE 2. DOUBLE-LAYER METAL EXPERIMENTS

Group	Wafer No.	Metal 1	Metal 2
A	1 2 ③	In situ-doped p^{++} Si at RCA	Filament Al RCA
B	4 5 ⑥	Sputtered Al (2% Si) at RCA	Filament Al at RCA
C	7 8 ⑨ ⑩ 11 12	Sputtered Al	Al at MSFC

○ 200 Å Al and the high-beam-current Extrion ion implanter* (Model 200-1000) were used for n^+ and p^+ implantation

C. Wafer Acceptance Test

After completion of the processing, the Insert Test Chip (MSFC-C017) was used to determine the device characteristics and to evaluate the double-layer metallization. A microphotograph of MSFC-C017 Insert Test Chip is shown in Fig. 1.

*Varian-Extrion Division, Blackburn Industrial Park, Gloucester, MA.

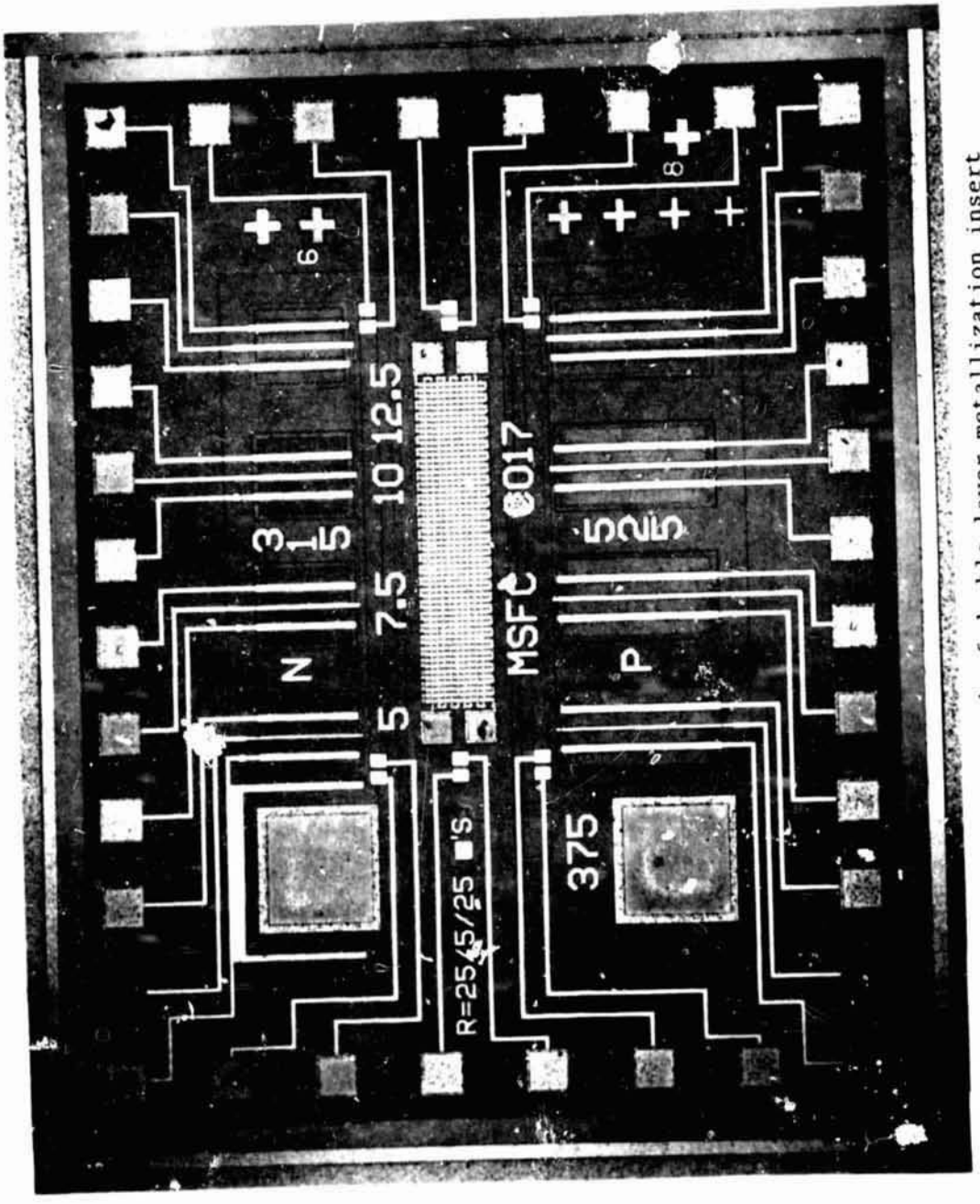


Figure 1. Microphotograph of double-layer metallization insert test chip TCS136 (MSFC-C017).

Wafer Group-A, with p^{++} polysilicon as the first layer conductor, exhibited ohmic contact problems in the source-drain of the NMOS transistors. Device characteristics of the Group-B wafers were normal and the results are presented in Table 3. The threshold voltages measured at I_d = 10 μA are V_{tn} = 0.76 ± 0.23 V, and V_{tp} = 0.87 ± 0.11 V. Leakage currents are I_{dssn} = 2.5 to 50 nA, and I_{dssp} = 1.5 to 15 nA.

TABLE 3. WAFER ACCEPTANCE TEST ON TEST TRANSISTORS (L = 7.5 μm) FOR GROUP B WAFERS OF LOTS S1998 AND S2010

Lot No.	Wafer No.	N - MOS				P - MOS			
		I_{dss} (nA) 10 V	V_t (V) 10 μA	V_t (V) 40 μA	BV_{ds} (V) 10 μA	I_{dss} (nA) 10 V	V_t (V) 10 μA	V_t (V) 40 μA	BV_{ds} (V) 10 μA
S1998	6	28	0.75	1.05	18	15	0.83	1.07	25
S2010	4	32	0.67	1.00	18	5	0.83	1.15	27
	5	50	0.53	0.90	14	10	0.80	1.15	26
	6	2.5	1.07	1.39	23	1.5	1.03	1.38	27

The Group C wafers were processed at MSFC and were not returned to RCA.

The test results on the double-layer metallization systems indicate that the second-layer metal is continuous over the step of the first-layer metal, and there are no short-circuiting problems between the two metal layers. Contact between the two metal layers through the via-holes is excellent. The measured results are presented in Table 4.

TABLE 4. RESISTIVITY MEASUREMENT FOR SECOND-LAYER METAL

Lot No. and Wafer No.	Continuity of 2nd Metal (ohm)	Pinhole Test (ohm)	Via-hole (110 holes) Test 1st Metal and 2nd Metal (ohm)
S1998-6	27.5	∞	400
S2010-4	27.5	∞	450
S2010-5	28.0	∞	180
S2010-6	24.0	∞	380

III. CIRCUIT PROBE

A. Design Verification

Solar-Cell Controller (TCS136 or MSFC-SC101) wafers were shipped to MSFC after a preliminary wafer acceptance test (WAT) for design verification and circuit probe. A schematic diagram and microphotograph are shown in Figs. 2 and 3.

Two wafers (S1998-6 and S2010-6) which were probed and inked were returned by MSFC to RCA with test patterns and procedures (see Table 5). The circuit probe yield of these two wafers are above 10%, and details of the results are summarized in Table 6.

B. Assembly

The wafers were laser-scribed and wire-bonded in a 22-lead dual in-line ceramic (DIC) package according to the bonding diagram shown in Fig. 4.

Of the 132 packaged arrays which were shipped to MSFC for final testing, 95 passed the test. Of the number that passed, 78 good packaged arrays were returned to RCA for life tests.

The details are summarized in Table 7.

C. Test Procedure

The TCS136 (MSFC-SC101) test program was coded for the Datatron Tester* at RCA acccording to the test pattern supplied by MSFC. This test is done immediately after burn-in, because some failure mode or defects may recover at room temperature. The truth table used in the

*Datatron Inc., Santa Ana, CA.

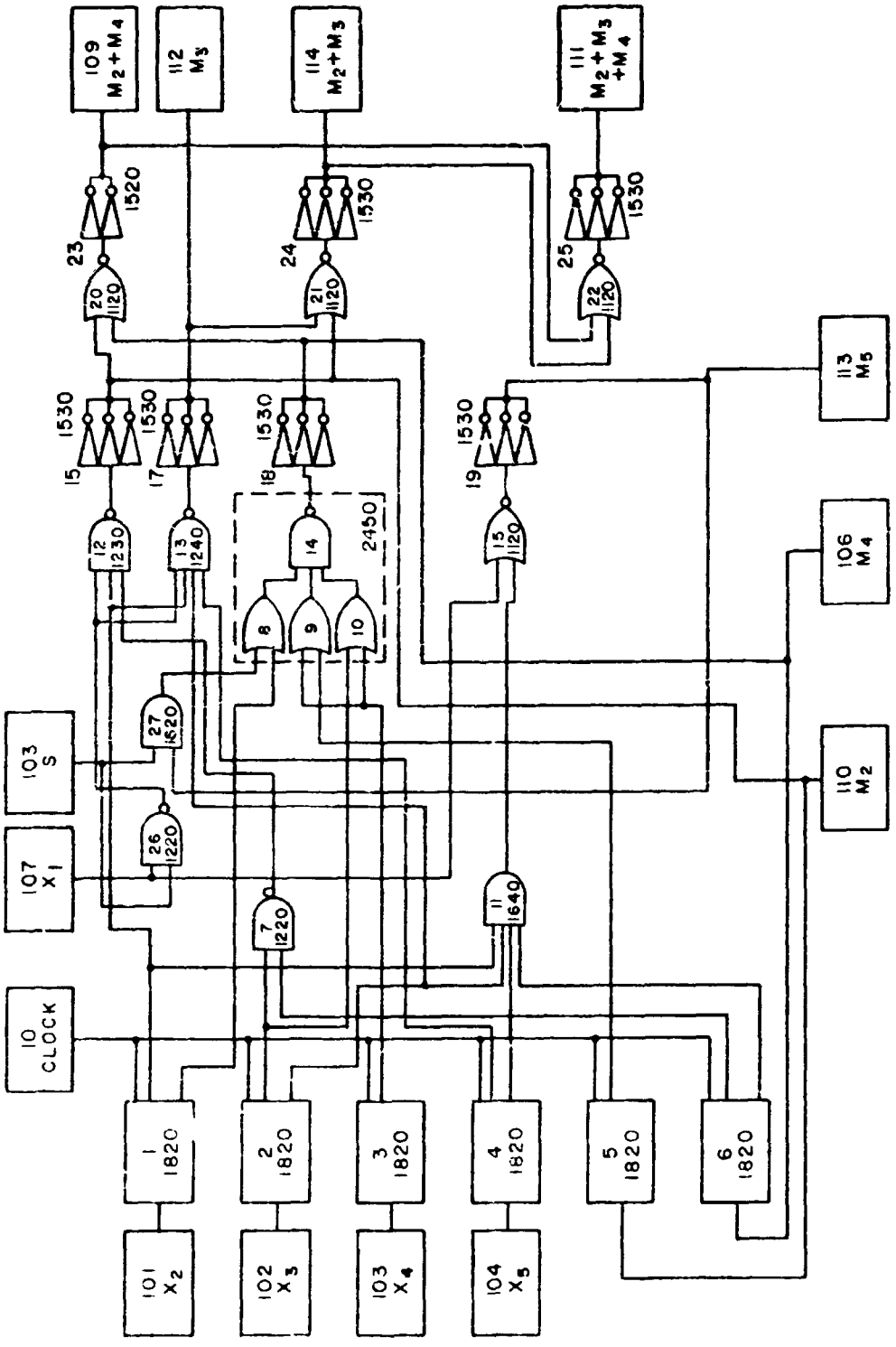


Figure 2. Schematic diagram of Solar-Cell Controller Circuit, TCS136 (MSFC-SC101).

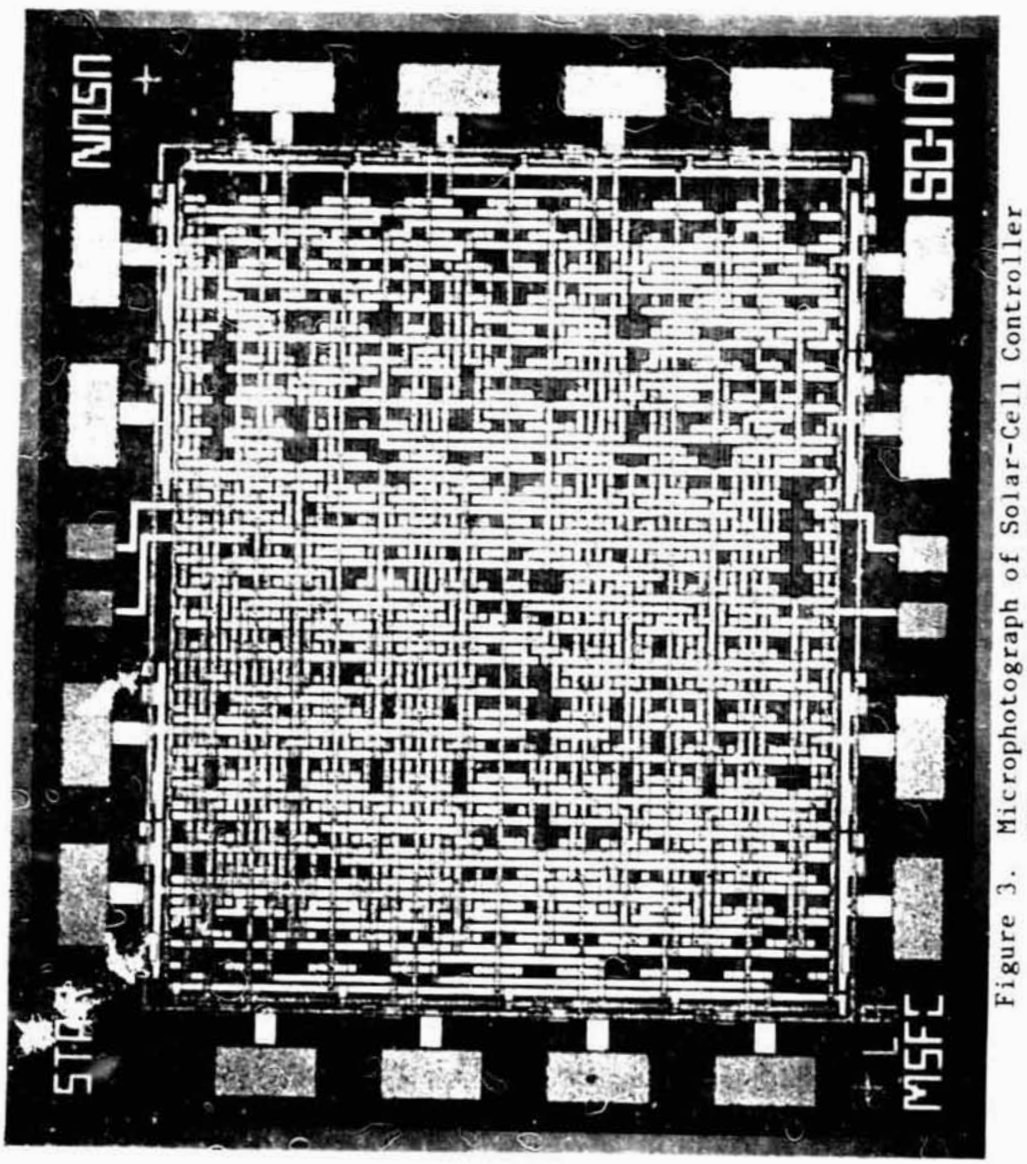
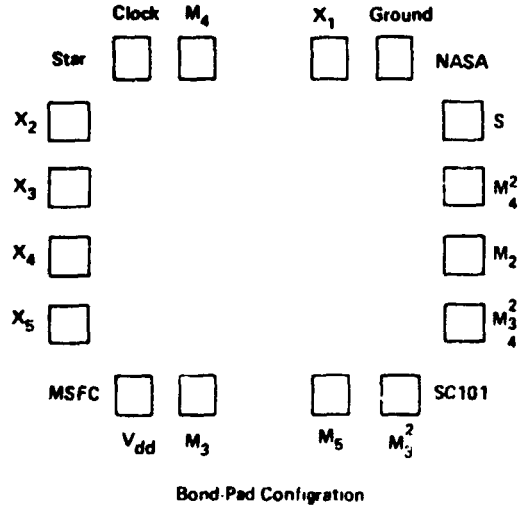


Figure 3. Microphotograph of Solar-Cell Controller Circuit, TCS136 (MSFC-SC101).The first-layer aluminum runs vertical and the second layer runs horizontal.

TABLE 5. TCS136 (MSFC-SC101) TEST PATTERN AND TEST PROCEDURE

Test Step	Input Pattern							Output Pattern							
	Octal	S	X_1	X_2	X_3	X_4	X_5	Octal	M_2	M_3	M_4	M_4^2	M_3^2	M_4^2	M_5
1	26	0	1	0	1	1	0	033	0	0	1	1	0	1	1
2	27	0	1	0	1	1	1	033	0	0	1	1	0	1	1
3	50	1	0	1	0	0	0	000	0	0	0	0	0	0	0
4	51	1	0	1	0	0	1	000	0	0	0	0	0	0	0
5	76	1	1	1	1	1	0	033	0	0	1	1	0	1	1
6	26	0	1	0	1	1	0	033	0	0	1	1	0	1	1
7	37	0	1	1	1	1	1	117	1	0	0	1	1	1	1
8	41	1	0	0	0	0	1	032	0	0	1	1	0	1	0
9	36	0	1	1	1	1	0	047	0	1	0	0	1	1	1
10	75	1	1	1	1	0	1	001	0	0	0	0	0	0	1
11	02	0	0	0	0	1	0	032	0	0	1	1	0	1	0
12	51	1	0	1	0	0	1	116	1	0	0	1	1	1	0
13	50	1	0	1	0	0	0	001	0	0	0	0	0	0	1
14	56	1	0	1	1	1	0	046	0	1	0	0	1	1	0



Bond-Pad Configration

TEST PROCEDURE
(Inverted Gate)

1. Setup Input Pattern
2. Clock Circuit (⌐¬└)
3. Compare with expected output

TABLE 6. PROBE DATA OF LOT S1998-6
AND LOT S2020-6

Lot - Wafer	# Good Chips	Yield (%)
S1998-6	93	10.9
S2010-6	109	12.8

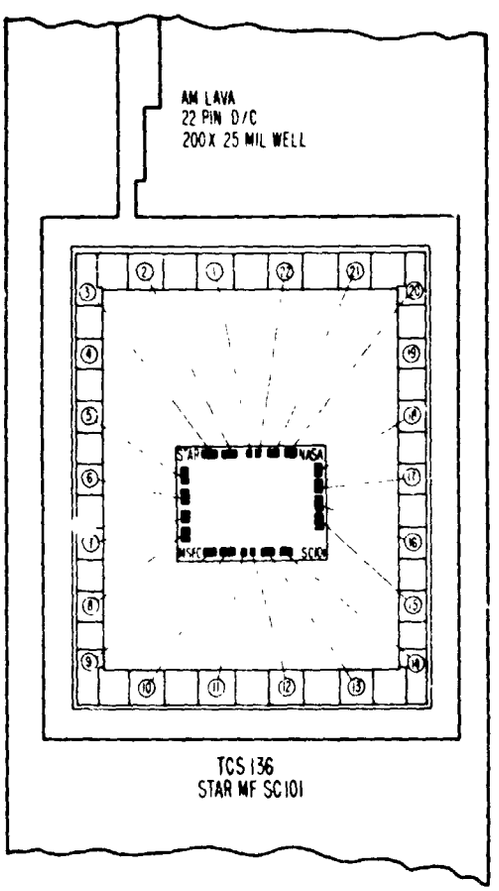


Figure 4. TCS136 (MSFC-SC101) bonding diagram.

TABLE 7. FINAL TEST RESULT OF PACKAGED ARRAYS

Lot No.	Date Code	No. Arrays to NASA	No. Arrays Passed	No. Arrays to RCA
S1998	7842J	70	44	38
S2010	7842S	62	51	40
	Total	132	95	78

Datatron Tester is presented in Table 8. Three types of leakage currents were measured on these devices after functionality testing:

(1) Terminal Leakage

Input terminals S, Clock, X1, X2, X3, X4, X5 are exercised by Truth Table 3 (TT-3) which checks Input with ONE (V = + 10 V) or ZERO (V = 0 V) and records the leakage current.

(2) Total Leakage of Total Steps

All inputs are connected and exercised according to the Truth Table (TT-1) supplied by NASA. Three tests are provided for I_{dd} values in three ranges of 1 mA, 500 μA, and 25 μA.

(3) Total Leakage of Selected Steps

Steps 2 and 3 were selected in TT-1, and the corresponding total leakage current (I_{dd}) were datalogged on both hard copy and Cartrifile Tape. The I_{dd} currents were measured in 3 ranges (1 mA, 500 μA, and 25 μA) to maintain better accuracy. One sample (Chip #97) of test results is presented in Table 9.

TABLE 8. TRUTH TABLE FOR DATATRON TESTER TO TEST TCS136 (MSFC-SC101)

TRUTH TABLE 0001
GROUP 0001

LINE	8	16	
0001	10101100	01101100	000010
0002	10101110	01101100	000010
0003	11010000	00000000	000010
0004	11010010	00000000	000010
0005	11111100	01101100	000010
0006	10101100	01101100	000010
0007	10111111	00111100	000010
0008	11000010	01101000	000010
0009	10111100	10011100	000010
0010	11111010	00000100	000010
0011	10000100	01101000	000010
0012	11010011	00111000	000010
0013	11010000	00000100	000010
0014	11011100	10011000	000010

TRUTH TABLE 0002
GROUP 0001

LINE	8	16	
0001	00000000	00000000	000010
0002	11111111	11111100	000010

TRUTH TABLE 0003
GROUP 0001

LINE	8	16	
0001	10000000	00000000	000000
0002	01000000	00000000	000000
0003	00100000	00000000	000000
0004	00010000	00000000	000000
0005	00001000	00000000	000000
0006	00000100	00000000	000000
0007	00000010	00000000	000000
0008	01111110	00000000	000000
0009	10111110	00000000	000000
0010	11011110	00000000	000000
0011	11101110	00000000	000000
0012	11110110	00000000	000000
0013	11111010	00000000	000000
0014	11111100	00000000	000000

TABLE 9. DATATRON OUTPUT SAMPLE OF ARRAY #97 FOR TCS136 TEST RESULTS

```
PROG 0358       STA    ID # 13600097
TOTAL TESTS 0059

ADDR. 0046  STEP 0001  GROUP 0001
                                          Input Terminal Leakage, TT-3, Step 1
PIN
001V   +9.985  -00.01U  002V   +J 000  -00 09U  003V   -0.006  +00.07U
004V   -0.010  -00.02U  005V   +0.002  +00.05U  006V   -0.007  +00.04U
007V   -0 014  -00.04U

ADDR. 0046  STEP 0008  GROUP 0001   Input Terminal Leakage TT-3, Step 8

PIN
001V   -0.006  +00.01U  002V   +9.983  -00.30U  003V   +9.978  +00.00U
004V   +9.986  -00.03U  005V   +9.984  +00.09U  006V   +9.972  -00.04U
007V   +9.974  -00.07U

ADDR. 0070  STEP 0002  GROUP 0001

PIN
022V   -0.010  +0.001M

ADDR. 0070  STEP 0003  GROUP 0001

PIN
022V   -0.007  -0.003M

ADDR. 0077  STEP 0002  GROUP 0001

PIN
022V   -0.009  -004.2U

ADDR. 0077  STEP 0003  GROUP 0001

PIN
022V   -0.012  -007 5U

ADDR. 0084  STEP 0002  GROUP 0010

PIN
022V   -0 006  -0  69U

ADDR. 0084  STEP 0003  GROUP 0010

PIN
022V   -0 016  -02 64U
```

Leakage Current, TT-1, Steps 2 & 3
Current Range: 1 mA

Leakage Current, TT-1, Steps 2 & 3
Current Range: 500 uA

Leakage Current, TT-1, Steps 2 & 3
Current Range: 25 uA

IV. LIFE TEST

A. Initial Test

Total leakage current (I_{dd}) of TCS136 (MSFC-SC101) was tested selecting steps 2 and 3 in Truth Table 1.

TRUTH TABLE 1

	INPUT							OUTPUT							
Step	Octal	S	X_1	X_2	X_5	X_4	X_3	Octal	M_2	M_3	M_4	M_4^2	M_3^2	$M_4^2 M_3^2$	M_5
2	27	C	1	0	1	1	1	033	0	0	1	1	0	1	1
3	50	1	0	1	0	0	0	000	0	0	0	0	0	0	0

The I_{dd} currents measured were datalogged and the results of all 80 chips are presented in Table 10. Leakage currents vary from 1 μA to a few mA. Twenty-five arrays with lower leakage current (1 μA $\leq I_{dd} \leq$ 100 μA) were selected for burn-in test.

B. Burn-In Board

The burn-in board was wired to provide the bias for the configuration of step-2 in TT-1, and the pin-out and its supply voltage is shown in Table 11.

C. Burn-In Test

Twenty-five TCS136 (MSFC-SC101) have been burned-in at 125° to determine reliability. When the burn-in boards were first hooked up, the stress voltage supply indicated an input current of 180 mA at V_{dd} = 10 V for the 25 packaged arrays. The devices were stressed at the above condition for about 10 minutes. This excessively high current level was due to the turn-on of the PMOS test transistors because of the wrong

TABLE 10. TOTAL LEAKAGE CURRENT OF TCS 136 AT INITIAL TEST

Array #	Step 2		Step 3		Array #	Step 2		Step 3	
10	3.162	mA	64.07	µA	80	3.030	mA	4.112	mA
12	42.08	µA	04.75	µA	81	03.02	µA	02.87	µA
13	1.963	mA	572.06	µA	87	25.31	µA	13.55	µA
15	120.0	µA	408.5	µA	88	03.39	µA	07 24	µA
16	1.294	mA	2.809	mA	89	01.00	µA	5.240	mA
21	510.2	µA	458.8	µA	90	00.83	µA	01.16	µA
22	510.2	µA	545.8	µA	93	04.15	µA	03.29	µA
24	29.22	µA	53.18	µA	95	01.59	µA	01.06	µA
25	27.61	µA	1.511	mA	96	25.72	µA	07.45	µA
26	367.4	µA	05.39	µA	97	3.69	µA	2.64	µA
27	45.24	µA	145.9	µA	98	01.46	µA	00.94	µA
28	1.139	mA	1.090	mA	99	26.74	µA	53.63	µA
29	207.8	µA	152.8	µA	100	01.30	µA	01.05	µA
31	230.5	µA	20.66	µA	101	216.5	µA	03.04	µA
32	230.5	µA	8.706	mA	103	26.21	µA	23.28	µA
34	235.7	µA	8.393	mA	105	345.0	µA	17.20	µA
35	423.9	µA	74.53	µA	106	196.4	µA	01.51	µA
36	3.651	mA	3 071	mA	107	01.54	µA	02.28	µA
38	05.75	µA	12.24	µA	111	46.82	µA	01.49	µA
43	05.80	µA	11.77	µA	112	600.2	µA	01.15	µA
46	28.71	µA	27.51	µA	113	00.69	µA	01.04	µA
47	28.86	µA	27.65	µA	115	34.00	µA	43.66	µA
49	13 70	µA	13.48	µA	116	00.97	µA	01.41	µA
51	1.095	mA	08.45	µA	117	10.09	µA	04.41	µA
53	1.174	mA	2.545	mA	118	01.68	µA	01.80	µA
54	110.4	µA	111.0	µA	119	215.2	µA	411.2	µA
55	705.9	µA	541.6	µA	120	17.63	µA	429.4	µA
56	572.0	µA	619.8	µA	121	01.33	µA	01.61	µA
57	572.0	µA	4.262	mA	122	01.58	µA	01.41	µA
58	11.09	µA	29.55	µA	123	07 69	µA	21.70	µA
62	171.4	µA	734.7	µA	124	1.206	mA	01.63	µA
63	870.1	µA	1.307	mA	125	07.03	µA	03.25	µA
64	47.91	µA	45.48	µA	126	1.376	mA	01.29	µA
65	323.4	µA	113.6	µA	127	00.69	µA	118.5	µA
66	419.7	µA	34.23	µA	128	01.35	µA	01.53	µA
67	3 244	mA	3.262	mA	129	00.98	µA	01.04	µA
69	3.612	mA	3.070	mA	131	00.84	µA	01.72	µA
70	73.68	µA	73.08	µA	132	04.95	µA	00.82	µA
79	01.21	µA	01.29	µA					

TABLE 11. BURN-IN CONFIGURATION OF TCS135 (MSFC-SC101)

Pin		Voltage
1	PD	0
2	M_4	open
3	Clock	0
4	Not Connected	0
5	X_2	-
6	X_3	0
7	X_4	10
8	X_5	10
9	V_{dd}	10
10	M_3	open
11	ND	0
12	NG	10
13	M_5	open
14	M_3^2	open
15	M_3^2	open
16	M_2^4	open
17	M_4^2	open
18	S	0
19	Not Connected	-
20	GND (SN)	0
21	X_1	10
22	PG	10

bias configuration of the burn-in board. Approximately 7.5 mA flowed through the PMOS device. This, however, should not have caused any damage to the circuits.

The wiring error on the burn-in boards was corrected and the 25 packaged arrays were burned-in for 168 h at 125°C. When the burn-in was completed, the packages were allowed to cool to room temperature (25°C) with stress-bias on. These devices were then retested using the Datatron tester. One array (Array #38) failed the functionality test after the 168-h burn-in at 125°C, and tests show that it shorted ($I_{dd} \geq 10$ mA) at step-2 configuration test. All of the 25 arrays were burned-in for an additional 72 h at 150°C. One more array (Array #12) failed during the second burn-in period. After testing was complete, all of the 25 arrays were burned-in additionally for 168 h at 150°C. At this time, Array #79 failed to function. The burn-in results are summarized in Table 12.

TABLE 12. BURN-IN RESULT OF TCS136 (MSFC-SC101)

	Step 2		Step 3	
Burn-In Conditions	Number of Arrays Passed	Failed Array Number (#)	Number of Arrays Passed	Failed Array Number (#)
Initial Test	25	-	25	-
168-h @ 125°C	24	#38	25	-
72-h @ 150°C	23	#12,#38	24	#12
168-h @ 150°C	22	#12,#38,#79	23	#12,#38

D. Results

The burn-in results (see Table 12) indicate that a total of three arrays failed at step-2 input configuration and two arrays failed at step-3 configuration. It was also noted that the failure was of a permanent nature and that none of the arrays recovered by the subsequent

bias temperature step. This failure may be due to the metal-1 to metal-2 short through the interlayer oxide or channel oxide rupture during the high-temperature bias cycle.

Histograms of the total leakage current at step-2 and step-3 input configuration with various burn-in cycles are plotted in Figs. 5 and 6. The leakage current increases during the initial burn-in (168-h at 125°C); however, the leakage current of some arrays is reduced during the higher temperature (T = 150°C) burn-in cycle.

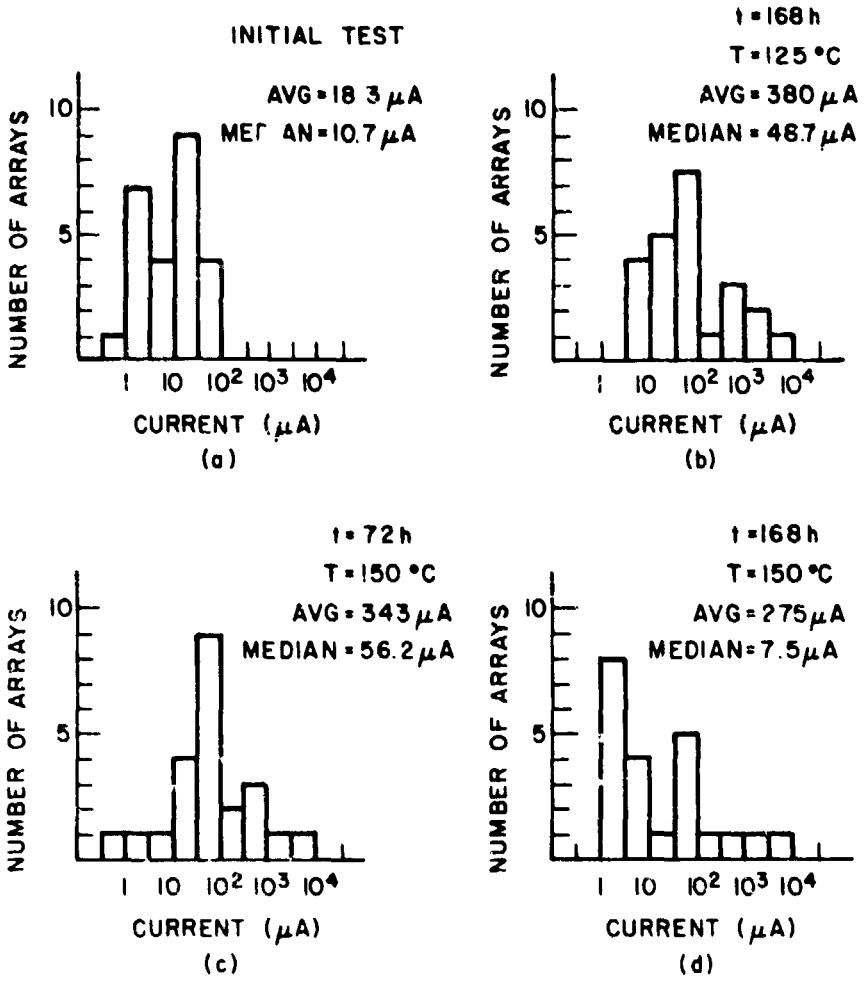


Figure 5. Total leakage current at step-2 input configuration of TCS136 (MSF C101).

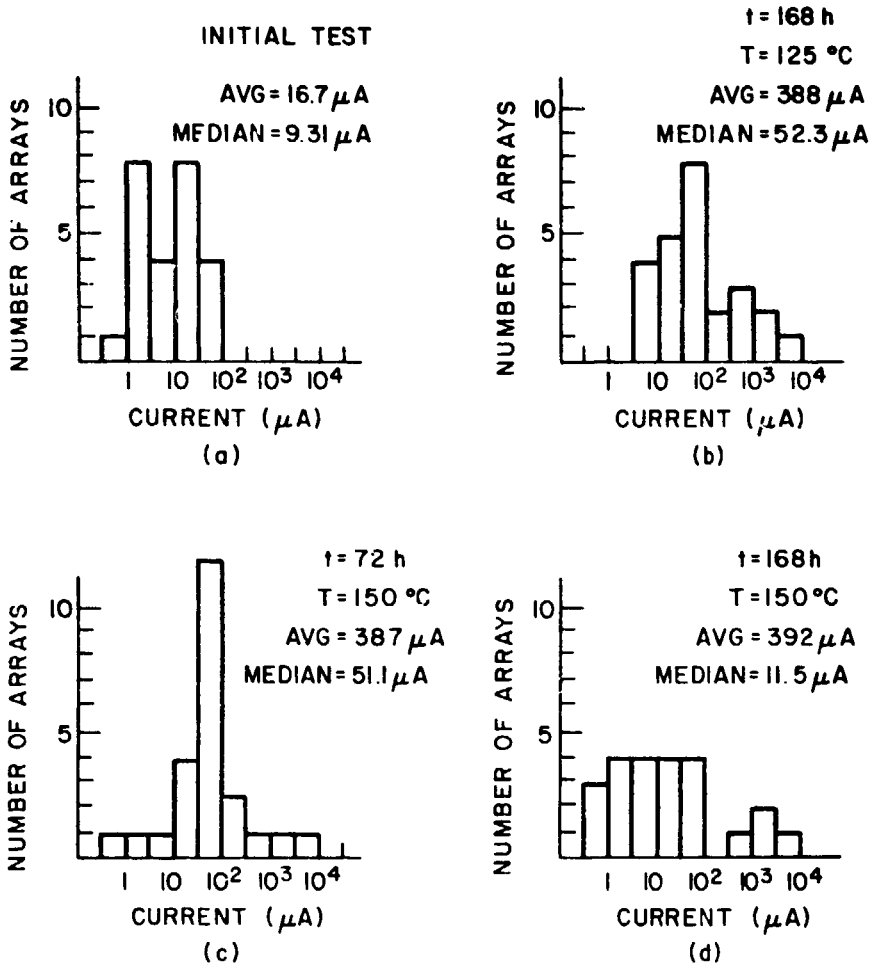


Figure 6. Total leakage current at step-3 input configuration of TCS136 (MSFC-SC101).