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# A System for Measuring Thermal Activation Energy Levels in Silicon by Thermally Stimulated Capacitance

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# ACKNOWLEDGMENTS

# ABSTRACT

One method being used to determine energy levels(s) and electrical activity of impurities in silicon is described. The method is called Capacitance Transient Spectroscopy (CTS). It can be classified into three basic categories: the thermally stimulated capacitance method (TSCAP), the voltage-stimulated capacitance method (VSCAP), and the light-stimulated capacitance method (LSCAP); the first two categories are discussed. From the total change in capacitance and the time constant of the capacitance response emission rates, energy levels, and trap concentrations can be determined. A major advantage of using CTS is its ability to detect the presence of electrically active impurities that are invisible to other techniques, such as Zeeman effect atomic absorption, and the ability to detect more than one electrically active impurity in a sample. Examples of detection of majority and minority carrier traps from gold donor and acceptor centers in silicon using the capacitance transient spectrometer are given to illustrate the method and its sensitivity. Experimental examples are given to illustrate the trap parameters that can be determined from capacitance transients, and the experimental test procedure and equipment used are described.

# GLOSSARY

| | |
|---|---|
| Å | Angstrom |
| $^{\circ}C$ | Degrees Celsius |
| C | Capacitance |
| C(t) | Capacitance with respect to time |
| $c_n$ | Capture rate of electrons |
| $c_p$ | Capture rate of holes |
| $C_\infty$ | Final capacitance |
| $C_0$ | Initial capacitance |
| CTS | Capacitance transient spectroscopy |
| $\Delta C$ | Change in capacitance |
| dc | Direct current |
| DI | Deionized |
| $e_r$ | Emission rate |
| $e_n$ | Emission rate of electrons |
| $e_p$ | Emission rate of holes |
| $E_n$ | Electron energy change during transition |
| $E_p$ | Hole energy change during transition |
| $E_c$ | Electron energy at conduction band edge |
| $E_v$ | Electron energy at valence band edge |
| $\mathcal{E}$ | Electric field |
| $e_o$ | Permittivity of free space |
| $\Delta E$ | Energy level with respect to band edge |
| I-V | Current-voltage |
| $^{\circ}K$ | Degrees Kelvin |
| k | Boltzmann's constant |
| $K_s$ | Dielectric constant of semiconductor |
| $LN_2$ | Liquid nitrogen |
| MHz | Megahertz |
| MOS | Metal-oxide semiconductor |
| $N_{DD}$ | Dopant impurity concentration |
| $N_{TT}$ | Total trap concentration in $cm^{-3}$ |
| $n_T$ | Trapped electron concentration |
| $N_{TOTAL}$ | Total number of traps |
| pf | Picofarad |
| q | Electron charge |
| $\rho$ | Space-charge density |
| S/N | Signal-to-noise ratio |
| T | Temperature |
| TSCAP | Thermally stimulated capacitance |
| TC | Thermocouple |
| $T_{TTA}$ | Thermal activation temperature |
| | Capacitance time constant |
| $t_f$ | Filling (charging) time |
| V | Voltage |
| VSCAP | Voltage-stimulated capacitance |
| W | Depletion width |

## CONTENTS

### Figures

Tables

# SECTION I

## INTRODUCTION

In the development of new techniques to produce silicon for solar cells, an understanding of the effects of impurities on semiconductor performance is necessary. Impurities can be introduced into silicon in many ways, intentionally and unintentionally. Dopant impurities such as phosphorus and boron are intentionally introduced into silicon; their behavior has been studied for many years (References 1 and 2). Unwanted impurities such as iron, copper, molybdenum and others are the subject of current studies, since they have adverse effects on solar cells. Unwanted impurities introduce deep-level trapping centers into silicon that affect carrier lifetimes adversely. The trap energy level or levels that an impurity introduces depend on how well it fits into the silicon lattice. With some impurities, the tendency to form compounds or precipitates on cooling, or their presence in different lattice sites, may result in varying proportions of electrical activity; the electrically active sites have the greatest effect on carrier lifetimes.

This report describes one method being used to determine energy level(s) and electrical activity of impurities in silicon. CTS was first suggested by C. T. Sah in 1965; its effect was first observed in 1967 by Sah et al (Reference 3), and was first disclosed in a technical journal in 1971 (Reference 4). CTS is classified into three basic methods: the thermally stimulated capacitance method (TSCAP), the voltage-stimulated capacitance method (VSCAP), and the light-stimulated capacitance method (LSCAP). From the total change in capacitance during a thermally stimulated transient and the time constant of the capacitance response, emission rates of trapped majority and minority carriers, the energy level from the nearest band edge, the capture rate of the majority and minority carriers, trap concentration, and a trap concentration profile can be determined. A major advantage of using CTS is its ability to detect the presence of electrically active impurities that are invisible to other techniques, such as Zeeman-effect atomic absorption, and the ability to detect more than one impurity in a sample. Another advantage is its sensitivity; CTS can detect impurities as low as $10^{10}$ atoms/cm$^3$ in silicon doped with $10^{14}$ atoms of phosphorus or boron per cm$^3$ (Reference 3).

In the present study, silicon wafers with secondary intentionally added impurities were investigated. Primary impurities in all samples were either phosphorus or boron. Secondary impurities included gold, copper, iron, molybdenum and titanium. The theory behind this measurement is developed in Section II; the experimental procedure and a description of the samples are given in Section III; measurement data, calculations, and results are presented in Section IV. Section V contains a discussion of results, and a summary is presented in Section VI.
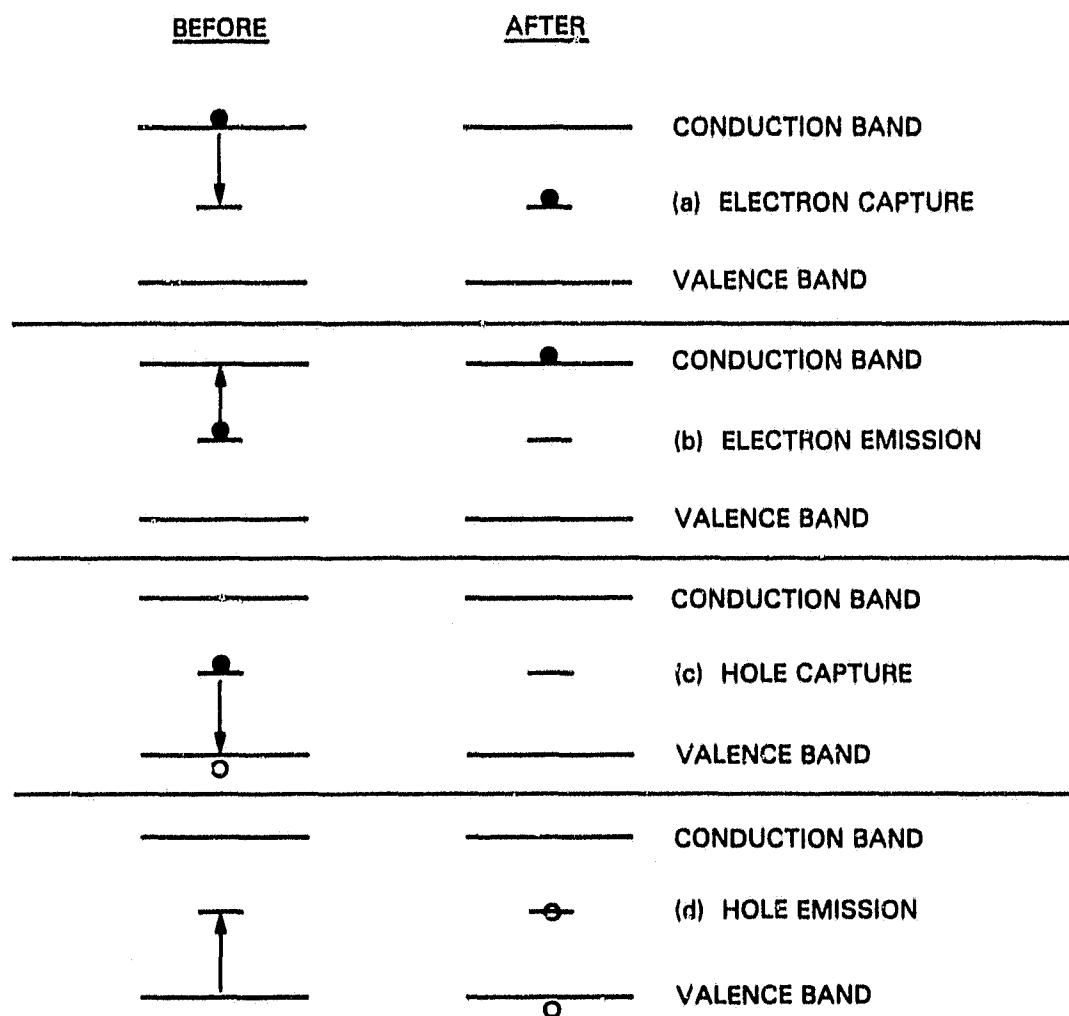
1

Figure 1. Recombination and Generation through Intermediate Centers
(Arrows Designate Direction of Electron Transition)
(After Grove, Reference 1)

# SECTION II

## THEORY

Theoretical analysis of deep-level impurity centers is based on the recombination kinetics of electrons and holes described by Shockley, Read, and Hall (References 5 and 6). The Shockley-Read-Hall (SRH) model relates the kinetics of the deep-level impurity centers in terms of the activation energy level of the centers and the four basic processes of capture and emission of holes and electrons (Figure 1). Sah and Shockley (Reference 7) extended the SRH model to include centers with multiple energy levels. Each energy level has six parameters ($e_n$, $e_p$, $c_n$, $c_p$, $E_n$, $E_p$), which must be defined to characterize the carrier generation-recombination trapping processes (Figure 2). The total rate coefficients are the sum of thermal, optical, and Auger-impact rates, i.e.,

$$e_p = e_p^t + e_p^o + e_p^p \cdot p + e_p^n \cdot n$$

where

$e^t$ = thermal rate

$e^o$ = optical rate

$e^{p,n}$ = Auger-impact rate

It is assumed that the thermal rates dominate; therefore $e_p \approx e_p^t$. In general, only three of the six parameters are needed to characterize the processes of recombination, generation, and trapping in semiconductors. This assumption is only valid at thermal equilibrium (References 8 and 9). For devices operated under non-equilibrium conditions, all six parameters must be known. Sah (Reference 8) points out that the mass action law used to compute capture rates can only be used for very rough estimates. Due to the large transition energy, the experimental thermal emission rates are not sufficiently accurate for calculating capture rates. The calculated results could be orders of magnitude in error.

In this analysis the kinetic process coefficients are determined using the capacitance transient method.

The analysis of the capacitance transient method begins with the rate equation for a single-energy-level acceptor like an SRH center (Reference 6). The rate equation is:

$$\frac{\delta n_T}{\delta t} = - (c_n n + e_n + c_p p + e_p) \, n_T + (c_n n + e_p) N_{TT} \tag{1}$$
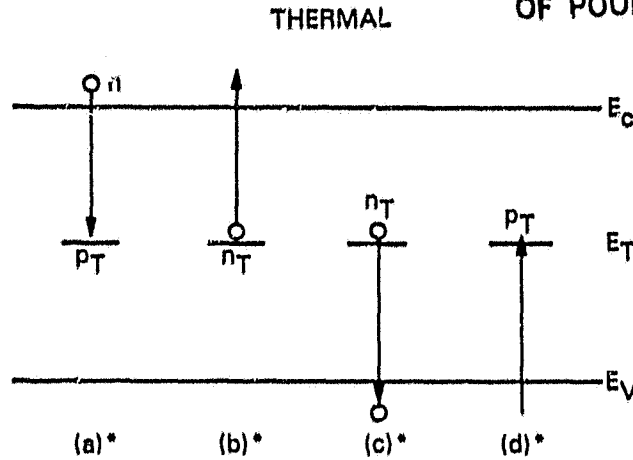
THERMAL



*a: ELECTRON THERMAL CAPTURE $\quad c_n^t n p_T$

b: ELECTRON THERMAL EMISSION $\quad e_n^t n_T$

c: HOLE THERMAL CAPTURE $\quad c_p^t p n_T$

d: HOLE THERMAL EMISSION $\quad e_p^t p_T$

Figure 2. The Four Kinetic Coefficients (After Sah, Reference 7)

where

$n_T$ = number of filled traps

$N_{TT}$ = total number of traps

$n, p$ = carrier concentrations

$c_n, e_n, c_p, e_p$ = capture and emission rates

Equation 1 is non-linear, and for a reverse-biased diode the space charge region is depleted, so $n = p = 0$. Therefore, Equation 1 can be simplified to

$$\frac{\delta n_T}{\delta t} = -(e_n + e_p) n_T + e_p N_{TT} \tag{2}$$

Considering states in the top half of the band gap only, then $e_n \gg e_p$ and Equation 2 reduces to

$$\frac{\delta n_T}{\delta t} = -e_n n_T \tag{3}$$

where Equation 3 is a solution of

$$n_T(t) = N_{TT} \, \epsilon^{(-e_n t)} \tag{4}$$

4

Now, looking at the capacitance of an abrupt p-n junction

$$C^2 = K_s \mathcal{E}_0 \rho / 2(V_R + V_D) \tag{5}$$

where

$\rho = q(N_{DD} - N_{AA} - n_T)$

$V_R$ = reverse bias voltage

$V_D$ = built-in voltage on metallurgical p-n junction

If the abrupt p-n junction has an n-type substrate, Equation 5 becomes

$$C^2(t) = \frac{qK_s \mathcal{E}_0}{2(V_R + V_D)} [N_{DD} - n_T(t)] \tag{6}$$

If the capacitance is calculated at different values of time, a change in capacitance is obtained

$$C(t) = C(\infty) - C(t)$$

$$= C(\infty) \frac{N_{TT}}{2N_{DD}} \epsilon^{-e_n t}$$

$$= C(t) = A\epsilon^{-e_n t} \tag{7}$$

where A is constant if $N_{TT}$ and $N_{DD}$ are constants.

If a reverse-bias voltage ($V_R$) is applied to a previously zero-biased p-n junction, a change in capacitance can be seen. This transient response is exponential if $e_n$ is independent of an electric field.

If a p-n junction is zero biased, then pulsed with a reverse-bias voltage $V_R$, some or all the of traps will be filled, depending on the duration of the reverse-bias pulse, which is referred to as "filling time" of the traps.

For $p^+$-n junction, considering only states above the middle of the gap, the rate equation is

$$\frac{-\delta n_T}{\delta t} = c_n N (N_{TT} - n_T) + e_n n_T \tag{8}$$

This is a solution of

$$n_T(t) = \frac{c_n N N_{TT}}{e_n + c_n N} [1 - \epsilon^{-t(e_n + c_n N)}] \tag{9}$$

5

If the carrier density N is spatially constant and the junction is reverse biased, so that the space charge region is depleted, traps will be filled during the filling time, because $e_n \ll c_n N$. Equation 9 becomes

$$n_T(t_F) = N_{TT}[1 - \epsilon^{(-c_n N t_F)}] \tag{10}$$

where $t_F$ is the filling time.

The capacitance change becomes

$$C(t) = C(\infty) - C(t)$$

$$= C(\infty) \frac{N_{TT}}{2N_{DD}} -e_n t[1 - \epsilon^{(-c_n N t_F)}] \tag{11}$$

and at $t = 0$

$$C = C(\infty) \frac{N_{TT}}{2N_{DD}} [1 - \epsilon^{(-c_n N t_F)}]$$

$$C = B[1 - \epsilon^{(c_n N t_F)}] \tag{12}$$

where

$$B = C(\infty) N_{TT}/2N_{DD}$$

It can be seen that, by fitting C at various filling times, the capture rate ($c_n N$) of electrons can be obtained, and from Equation 7 the thermal emission rate $e_n$ of electrons can be obtained.

The theory presented above proposes that both the emission rates and capture rates can be obtained from a capacitance transient response of a p-n junction diode.

# SECTION III

## EXPERIMENT

In the present study, silicon wafers with intentionally added secondary impurities were used as test samples (materials other than silicon can also be used). All silicon wafers were cut from ingots grown using the Czochralski method and had a primary impurity of either phosphorus or boron. The secondary impurities added in this experiment were gold, iron or titanium. All wafers were approximately 15 mils thick before chemical polishing. Resistivity measurements were performed on all wafers using a four-point probe system (Reference 10) to determine approximately the electrically active impurity concentrations (this measurement sees both primary and secondary impurities together). All wafers were chemically polished using 95% $HNO_3$, 5% HF solution with the sample attached to a Teflon holder and rotated in the solution until the surface of the wafer appeared shiny, then were rinsed in deionized water until the rinse-water resistivity was above 10 megohm. Wafers with phosphorus as the primary impurity (n-type silicon) were made into aluminum-silicon Schottky barrier diodes about 30 mils in diameter (Figure 3). Wafers with boron as the primary impurity (p-type silicon) were made into $n^+p$ junction diodes (Figure 4). Before metallizing with aluminum or diffusing the p-n junction, all wafers were cleaned using a procedure designed to minimize operator handling and to reduce possible contamination by contact with multiple chemicals:

> Immerse wafers in $H_2SO_4$ (70:30) for 10 min.
> Rinse under running DI $H_2O$ for 10 min.
> Etch wafers in $H_2O$, HF (10:1) for 10 sec.
> Rinse under running DI $H_2O$ for 10 min.
> Rinse in DI $H_2O$ until rinse-water resistivity reaches 14 megohms
> Blow-dry wafer with dry $N_2$

All wafers were metallized with 10-Angstrom aluminum. The aluminum was then sintered at 450°C for about 30 minutes in dry nitrogen. After sintering, all diodes were checked on an I-V curve tracer to ensure that they were working properly. Wafers were then cut into individual diodes and packaged. I-V curves were taken on completed Schottky diodes to determine their breakdown voltages and to verify their operation after packaging. The diode breakdown voltage is needed in determining the maximum voltage per unit of bias voltage used during TSCAP and VSCAP measurements. A Tektronix 575 curve tracer was used to measure diode characteristic curves. Diodes are mounted on TO-5 headers, and metal caps are mounted on the headers and soldered in place (Figure 3) to protect the diodes.

The first capacitance transient measurement performed on the completed diode is the TSCAP measurement. This determines how many trapping levels exist in the sample and at what temperature the trap is activated. The total concentration of a trap can also be determined from this measurement. Two TSCAP methods are described, manual and automated:

The manual method test setup is shown in Figure 5. This setup consists of five blocks: (1) a dc power supply used to supply the bias voltage to the
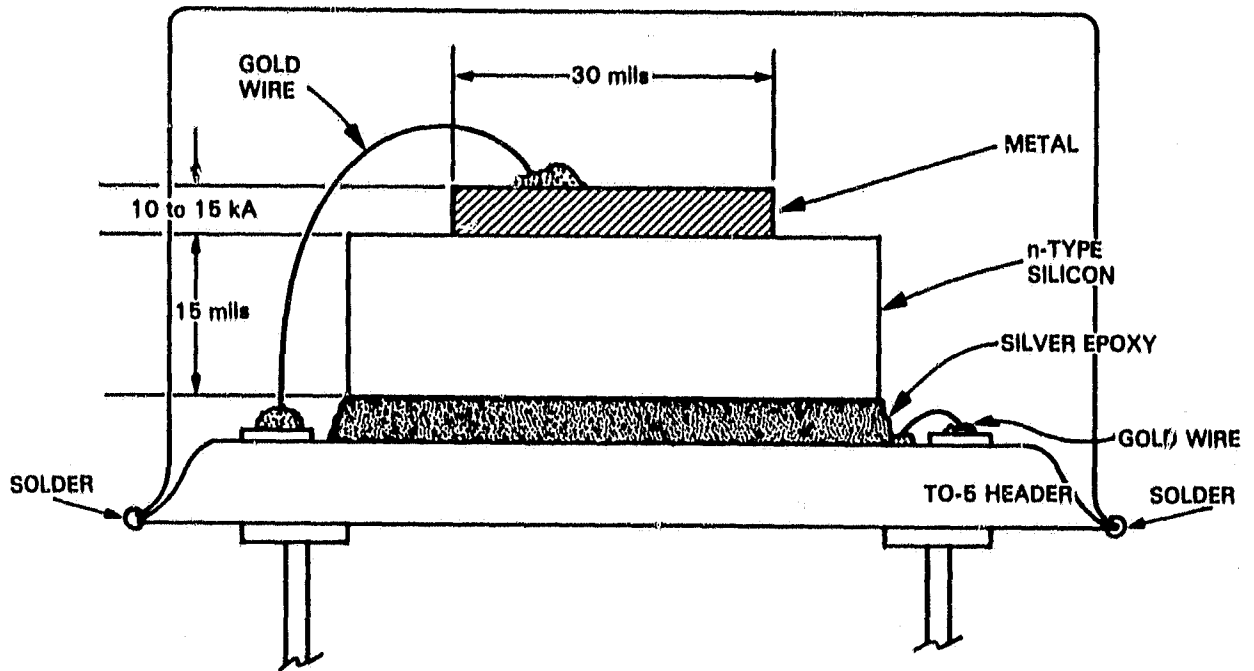
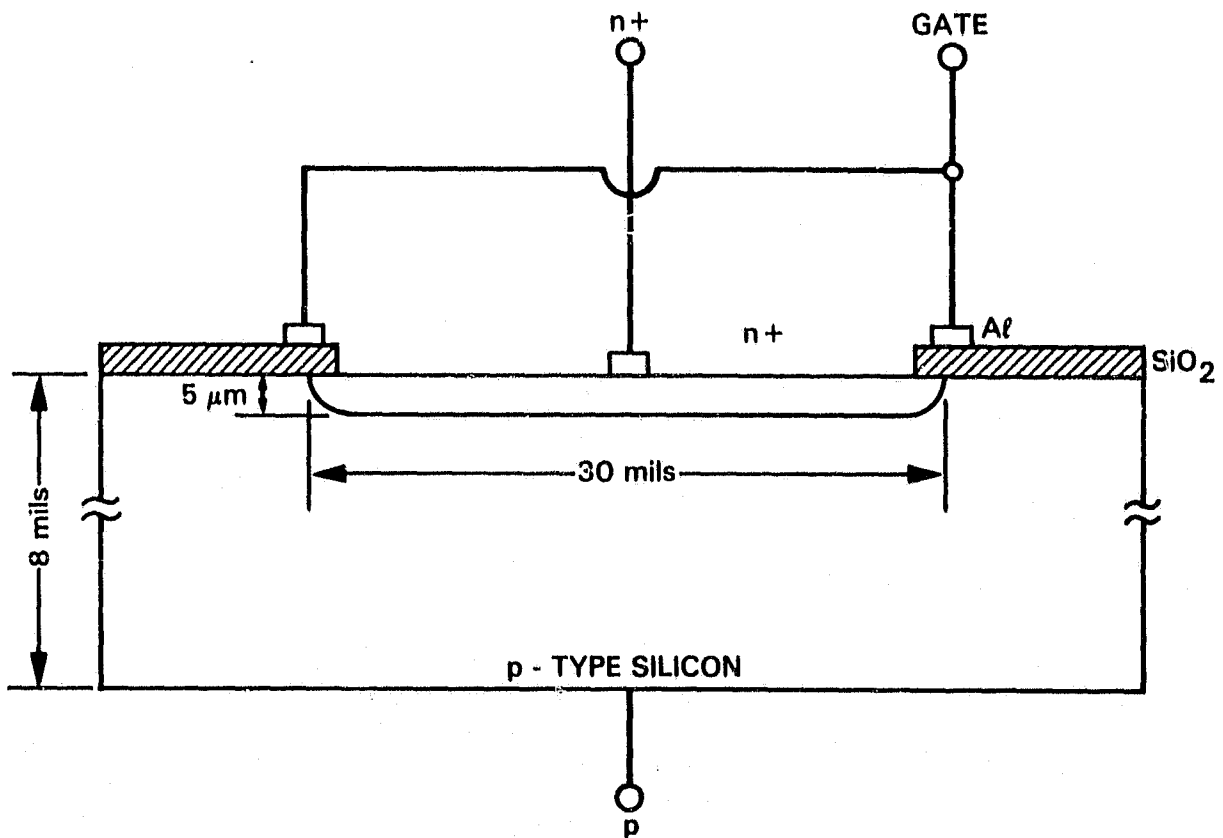Figure 3. TSCAP Test Device Using n-Type Silicon Substrate



Figure 4. TSCAP Test Device Using p-Type Silicon Substrate $n^+p$ Junction
Diode With MOS Gate

8

```
                    ┌──────────────┐
                    │  PRECISION   │
                    │  DECADE      │
                    │  CAPACITOR   │
                    └──────┬───────┘
                           │
                           ▼
┌──────────┐   ┌──────────────┐   ┌──────────────────┐   ┌──────────────────┐
│   DC     │   │ CAPACITANCE  │   │ TEMPERATURE STAGE│   │  TEMPERATURE     │
│   BIAS   │◄─►│ METER        │◄─►│ (DESIGNED BY     │◄─►│  SENSOR AND      │
│(HP-6116A)│   │ (BOONTON 72B)│   │ C.T. SAH)        │   │  CONTROLLER      │
└──────────┘   └──────┬───────┘   └──────────────────┘   │(HP-6224B, HP-419A)│
                      │                                   └──────────────────┘
                      ▲
                      │         ┌──────────────┐
                      └─────────│   x-y-t      │
                                │   PLOTTER    │
                                │  (HP-7100B)  │
                                └──────────────┘
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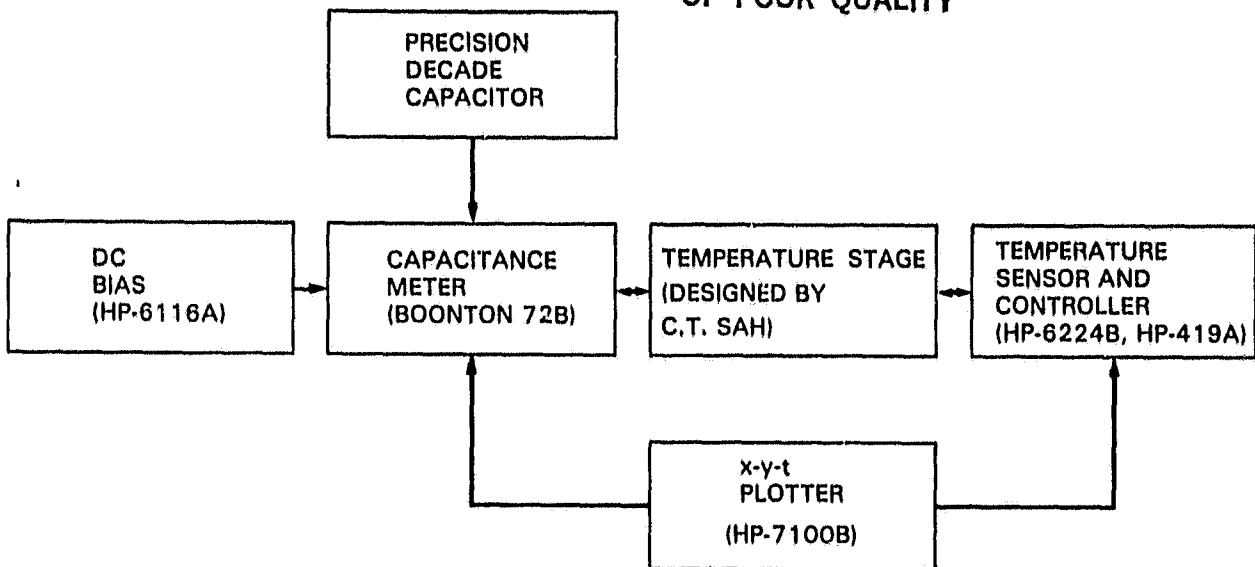
Figure 5.  Manual TSCAP Method

test diode; (2) a 1.0 MHz capacitance meter with precision decade capacitor, Boonton Model 76-3A (the precision capacitor is used to null out the majority of the junction capacitance so that capacitance changes of 0.1 pf or less can be seen easily); (3) a temperature stage, used to lower the temperature of the test device, then raise the temperature again (Figures 6 and 7); (4) a temperature controller circuit used to control temperature at one point or increase it linearly (Figures 8 and 9); (5) an x-y-t plotter, used to record the data.  The manual-method setup is shown in Figure 10.  The procedure is:

(1)    Zero-bias the diode (to fill the recombination centers with electrons in n-type substrate or to fill them with holes in p-type substrate) and lower the temperature to $77^\circ K$ with $LN_2$.

(2)    Switch to reverse bias, as determined from the I-V curve, and record the capacitance or current transients.

(3)    Allow the temperature of the test diode to rise linearly with time.

A manual TSCAP plot is shown in Figure 11.  This plot shows one capacitance transient for a sample containing iron when a temperature scan over the range of $80^\circ K$ to $200^\circ K$ was made.  One of the problems related to the manual method is achieving a truly linear temperature rise so that an accurate value of C can be obtained.  When the temperature rises, so does the capacitance, whether a trap is present or not; the trap just adds to the capacitance change, causing a lump in the curve.  If the temperature is not linear, many lumps will appear in the curve that are not caused by traps.  In order to eliminate the problem of differentiating between a change in capacitance and a trap or temperature fluctuation, a VSCAP measurement can be made instead.  VSCAP is best performed using an automated technique, so an automated test system has been developed (References 11 and 12) (Figure 12). In this method, the basic building blocks used in the manual TSCAP are still
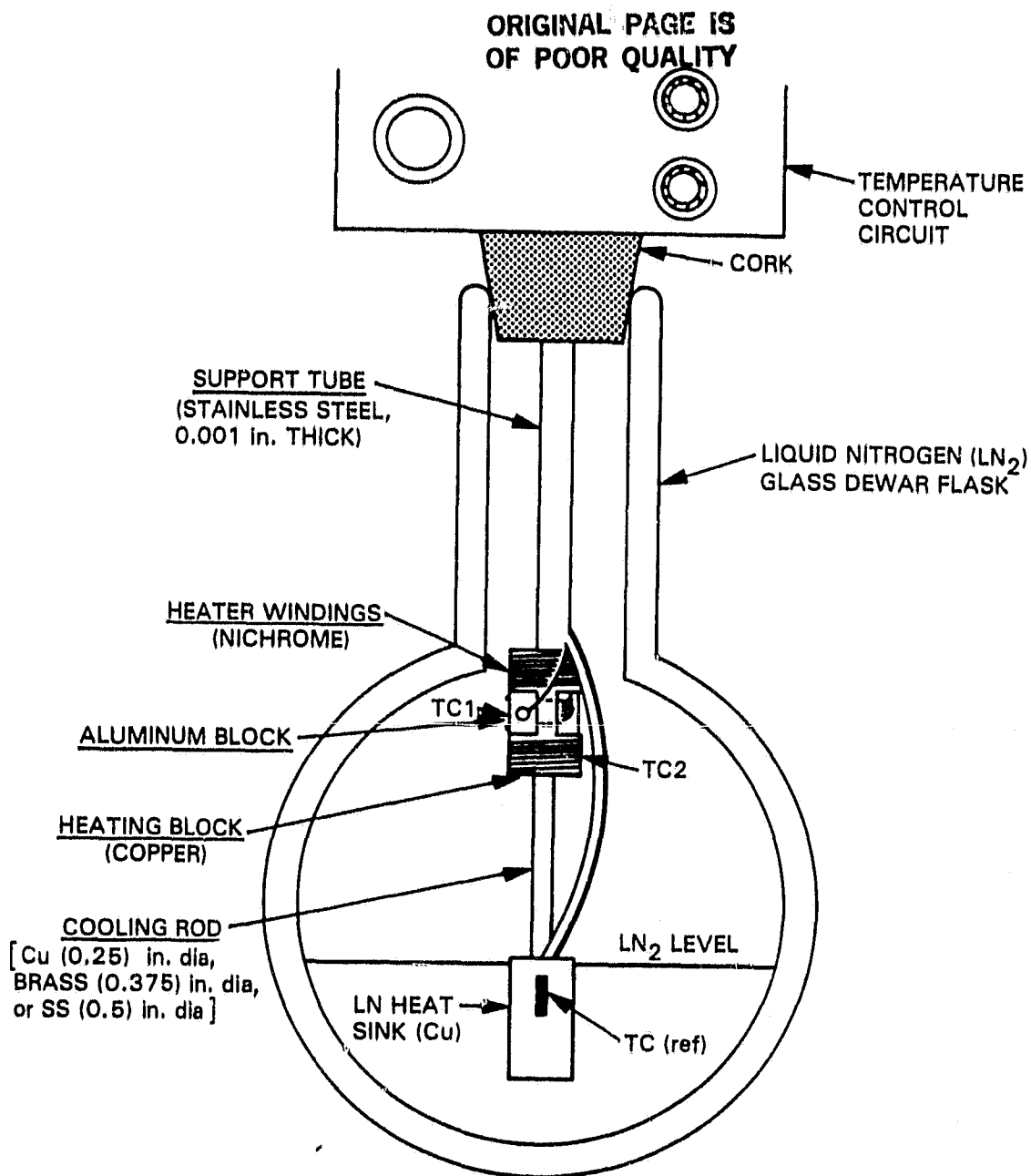
9

Figure 6.   Low-Temperature Chamber (After Sah, Reference 3)

Figure 7. Sample Holder (After Sah, Reference 3)
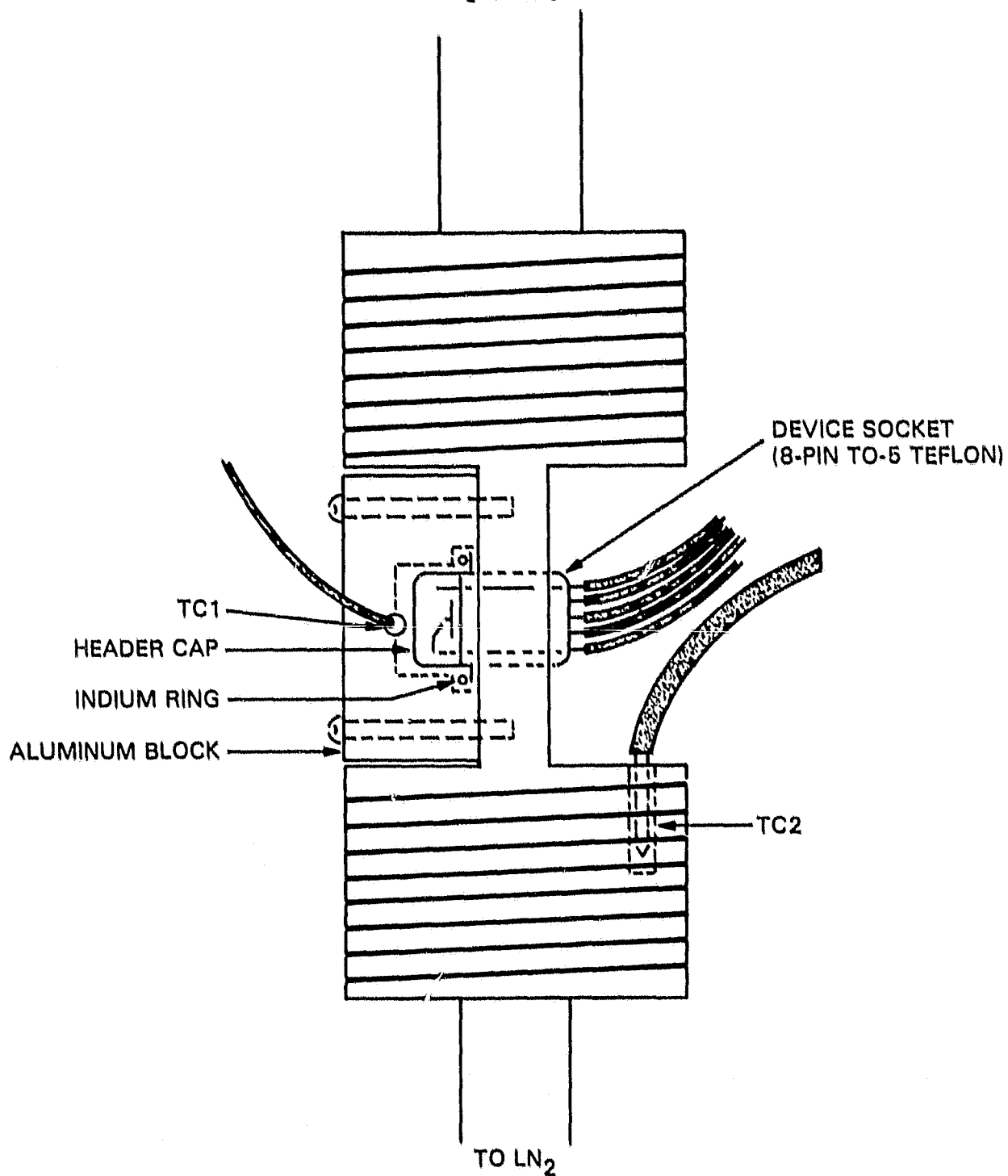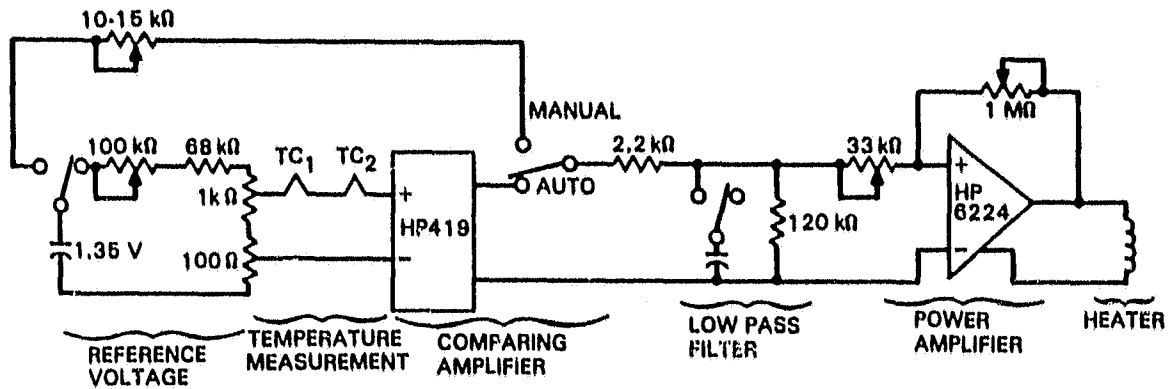
Figure 8. TSCAP Temperature-Control Circuit (C. T. Sah)
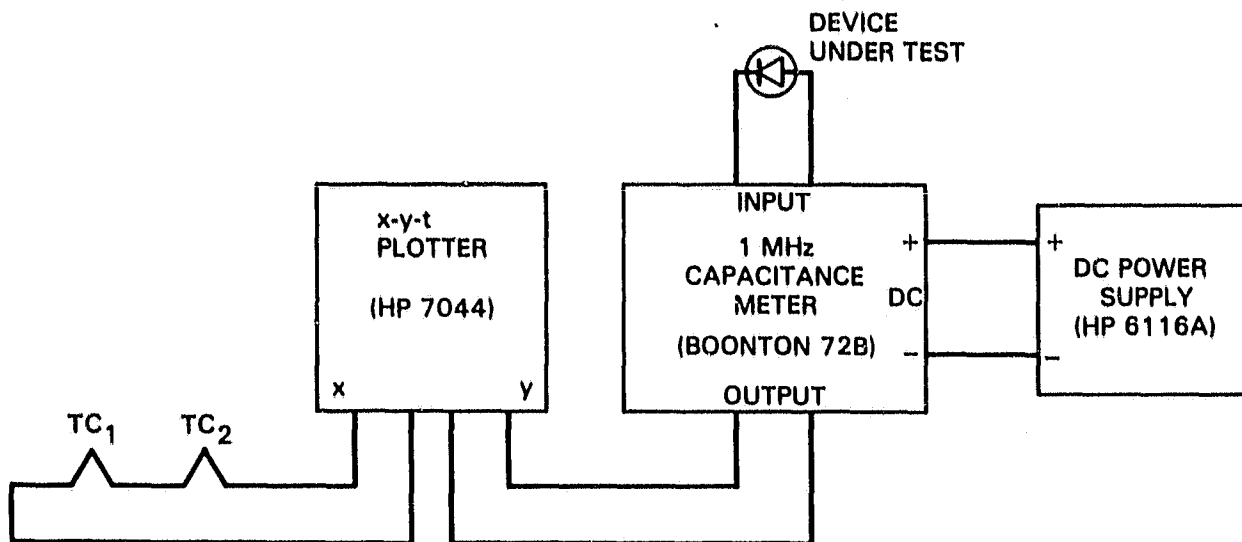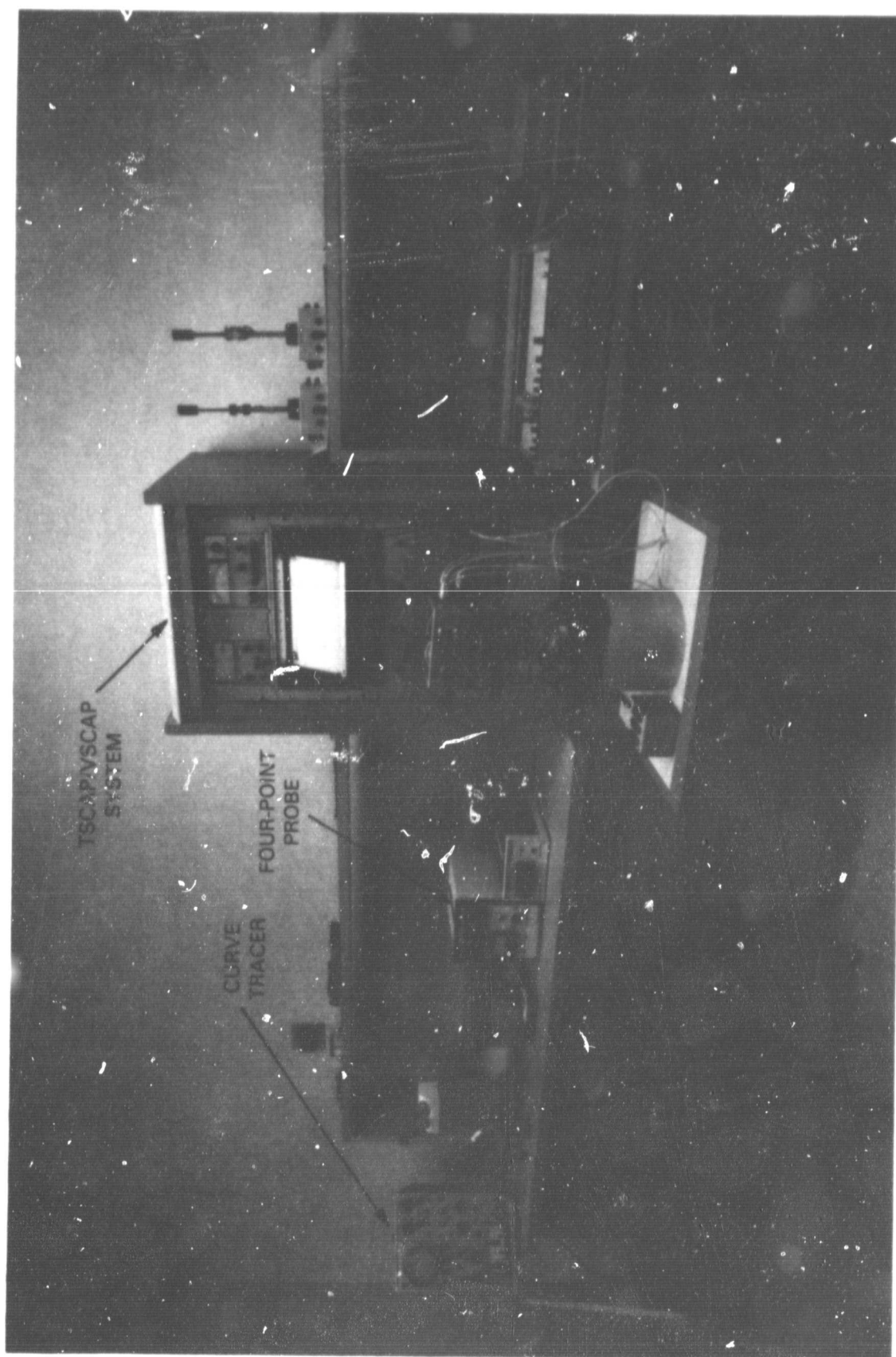


Figure 9. TSCAP Circuit

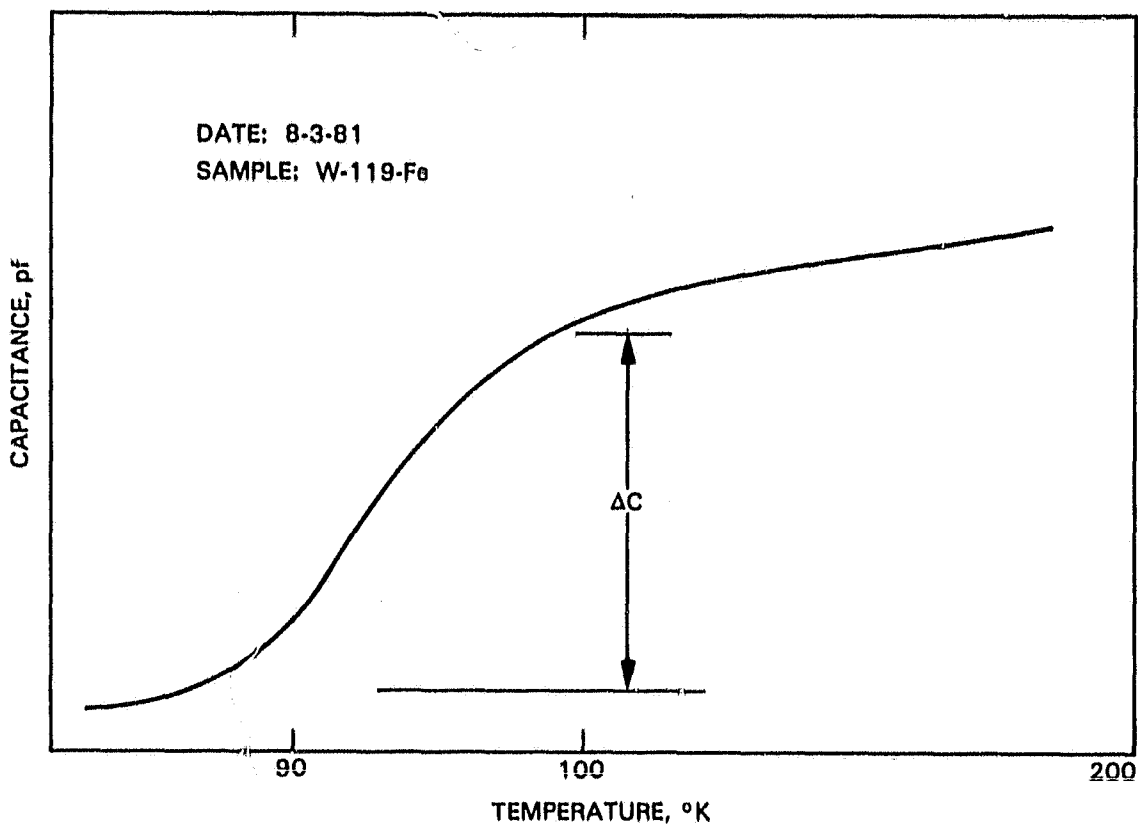Figure 10. Manual TSCAP Method Setup

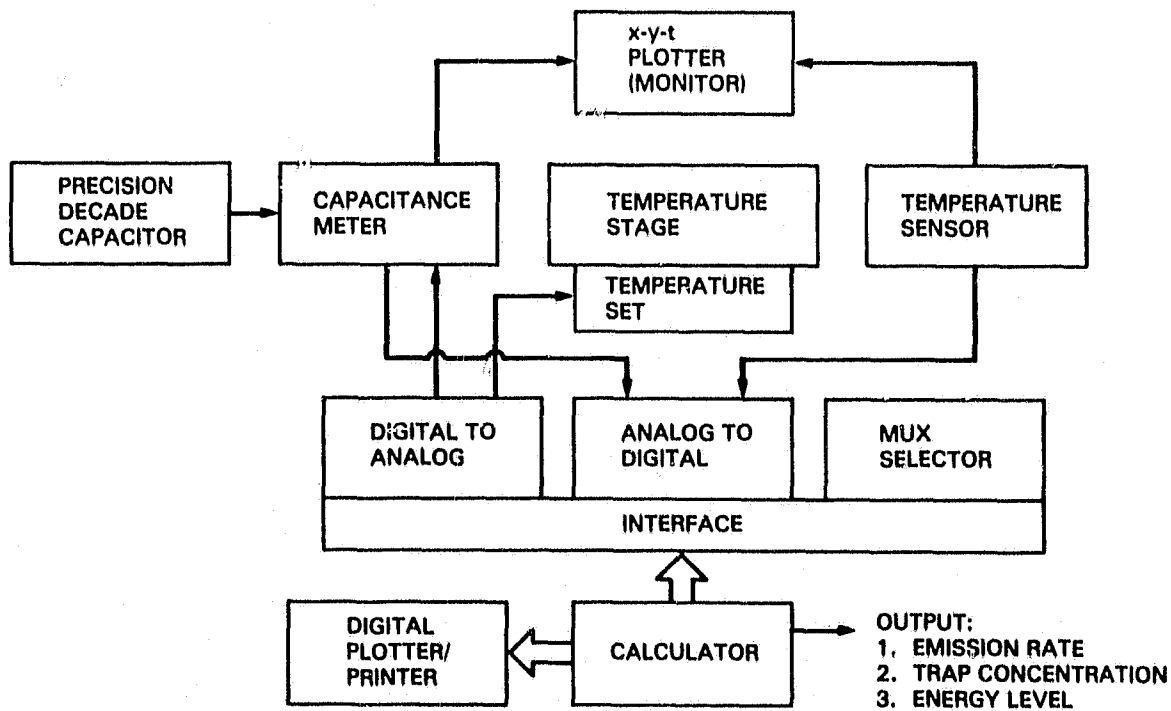Figure 11. A Manual TSCAP Method Curve



Figure 12. Automated VSCAP

used, except that a programmable calculator is used to gather data and set the bias voltage. Change is also made in the test procedure: as the temperature rises, the bias voltage is cycled from zero bias to reverse bias and back again. This step increases the space-charge density, decreases the space-charge layer, and increases the capacitance of the diode junction. This voltage pulsing creates a capacitance transient (Figure 13 a, b, c). For the non-trap capacitance rise the capacitance transient is small, but if a trap is present it is identified clearly by a more definite transient. A different output data format is shown in Figure 14; the computer plots the change in capacitance during a transient in bar-graph form. Figure 14 shows a VSCAP measurement on a test sample containing gold. In each of the procedures described above, temperature was measured using T-type thermocouples. From these TSCAP and VSCAP curves the positions on the curve (in terms of temperature) are obtained for each trap element present, making this technique ideal for scanning samples to determine if electrically active traps are present or not.

The VSCAP test technique also offers additional data about the trap, such as emission rate of carriers from the traps as a function of temperature, the energy level that the trap occupies (from the nearest band edge), the capture rate of carriers, and the concentration of traps as a function of temperature.

The emission rate of carriers is obtained from the capacitance transient curves where the slope gives the emission rate (Figure 15). From a set of emission rates versus temperature the Arrhenius equation is solved giving the energy level of the trap as a result (Figure 16).

The concentration of traps is obtained from the change in capacitance during a transient response. The trap concentration profile is obtained by measuring the total capacitance change as a function of applied reverse bias (Reference 12) (Figure 17).

The capture rate of the majority carriers is determined by measuring the total capacitance change as a function of zero-bias time (Figure 18).

To review briefly, the procedure for VSCAP is:

(1)  Zero-bias the diode and reduce the temperature to the lowest point where a transient occurs.

(2)  Allow capacitance and temperature to stabilize. This may take several minutes. This time can be varied to determine capture rate.

(3)  Switch to reverse bias. Measure capacitance as a function of time.

(4)  Calculate emission rate $e_r$ from capacitance transient.

(5)  Raise the temperature and repeat Steps 2, 3 and 4 for as many data points as are needed.

(6)  From the set of $e_r$'s, calculated  E.

(7)  From the capacitance data, calculate $N_{TT}$.
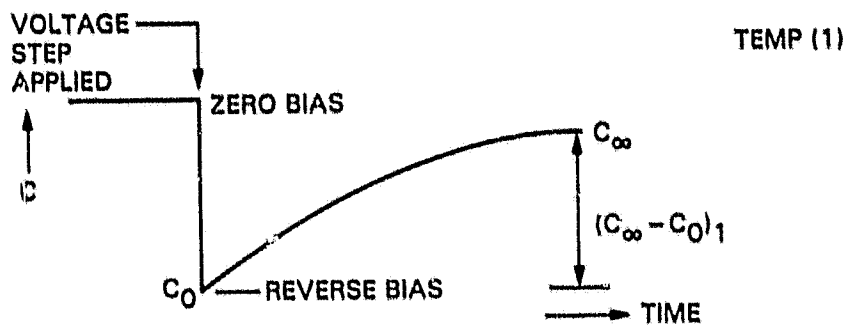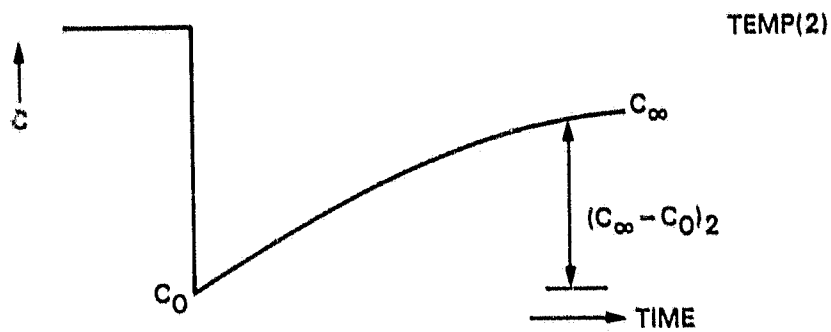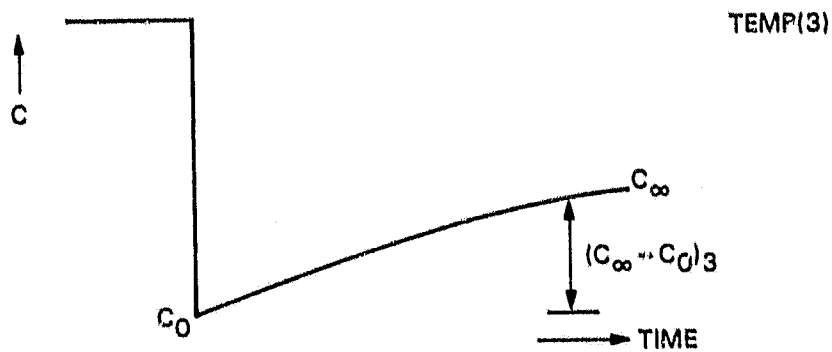
Figure 13. Capacitance Transient Curves

$C_\infty$-$C_0$ MEASUREMENT  PROGRAM NO. 11503-11427



SAMPLE NO. EC-3-AU
DATE: 5-20-82
V1 - 0 x $10^0$
V2 - 0 x $10^0$
V3 - -5.0 x $10^0$
T1 - +1.0 x $10^0$
T2 - +8.3 x $10^1$
T3 - +8.3 x $10^1$
$N_{DD}$ - +2.0 x $10^{15}$
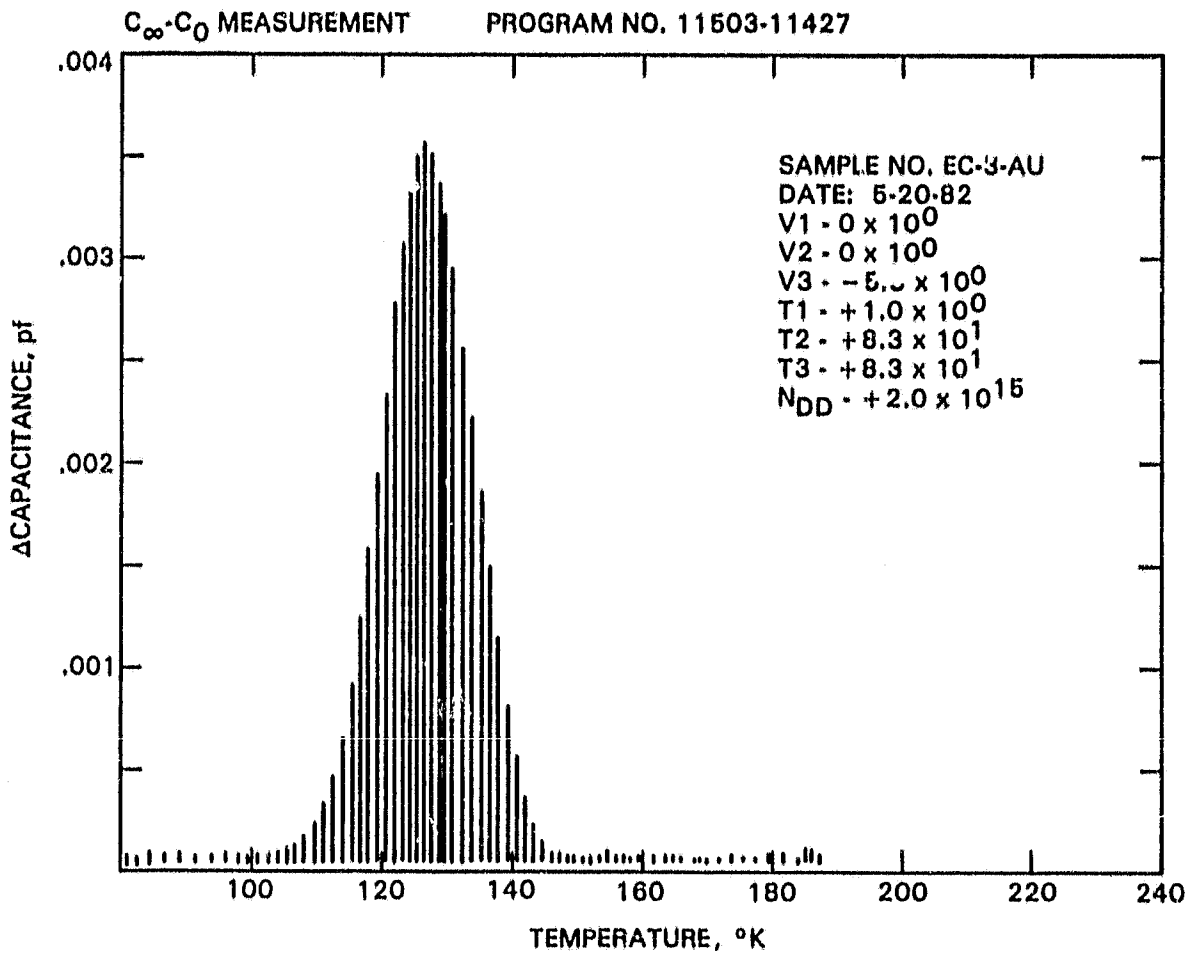
Figure 14.  Automated TSCAP Printout
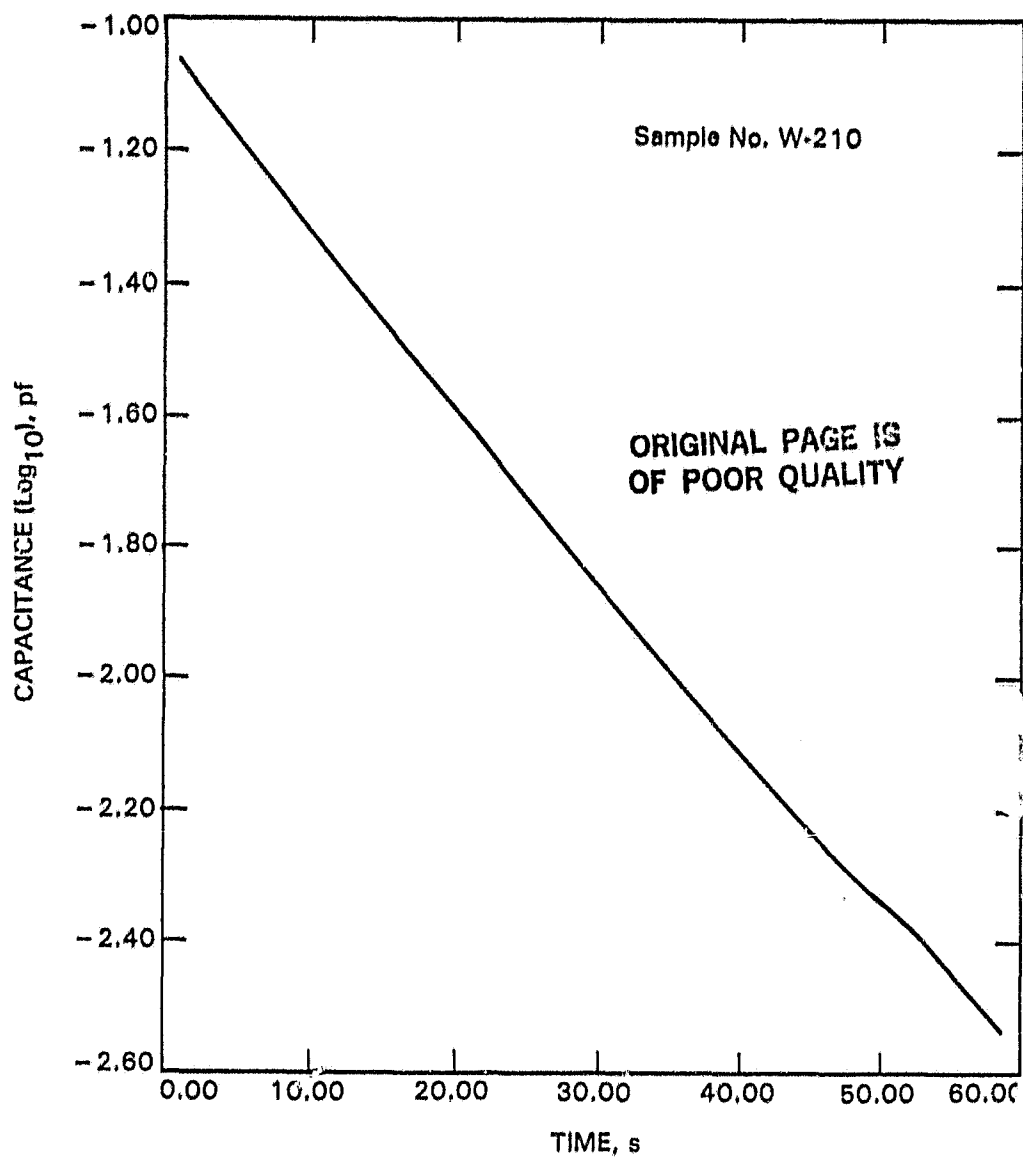
**Figure 15.** Semilog Plot of Capacitance Transient of Titanium-Doped Aluminum/n-Si Schottky Barrier Diode (After Sah, Reference 3)

18
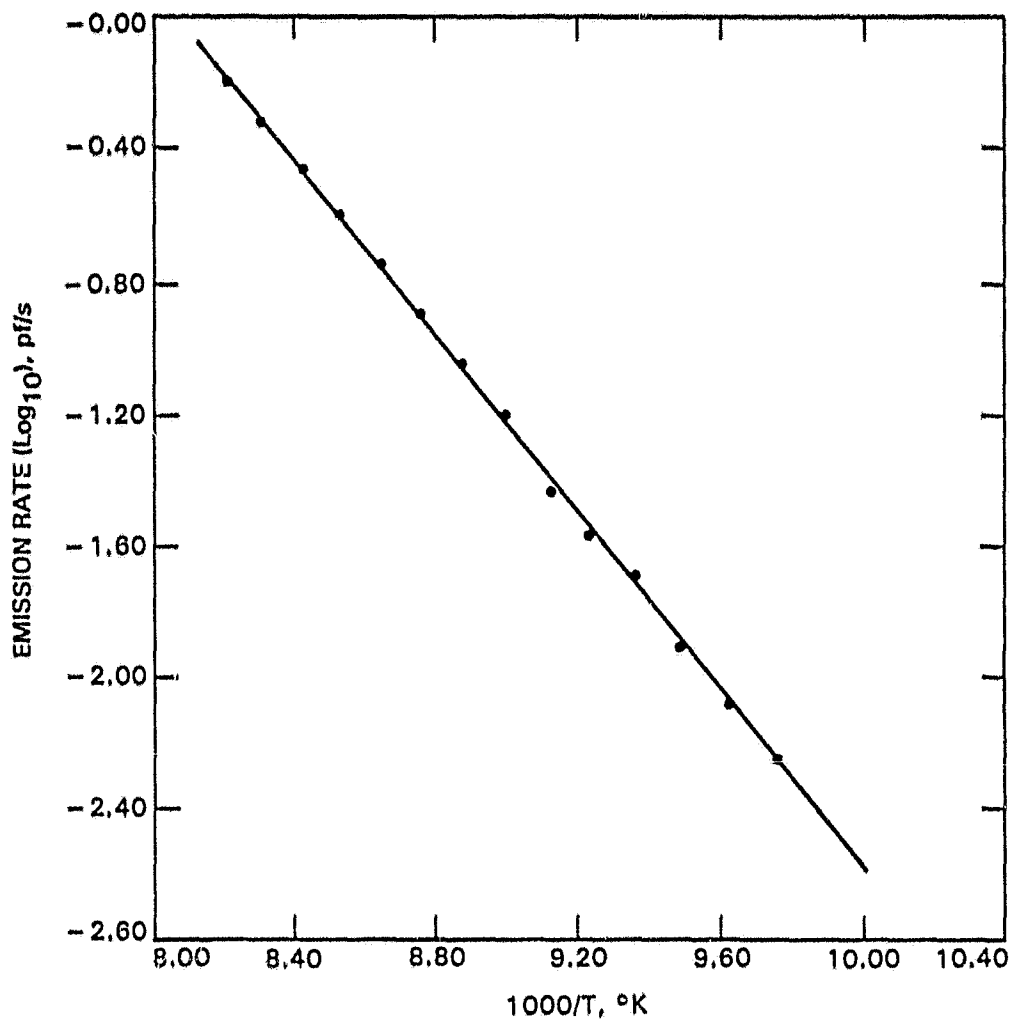
Figure 16. Arrhenius Plot of Thermal Emission Rate of Electrons
(Slope Gives the Thermal Activation Energy) (After Sah,
Reference 3)

19
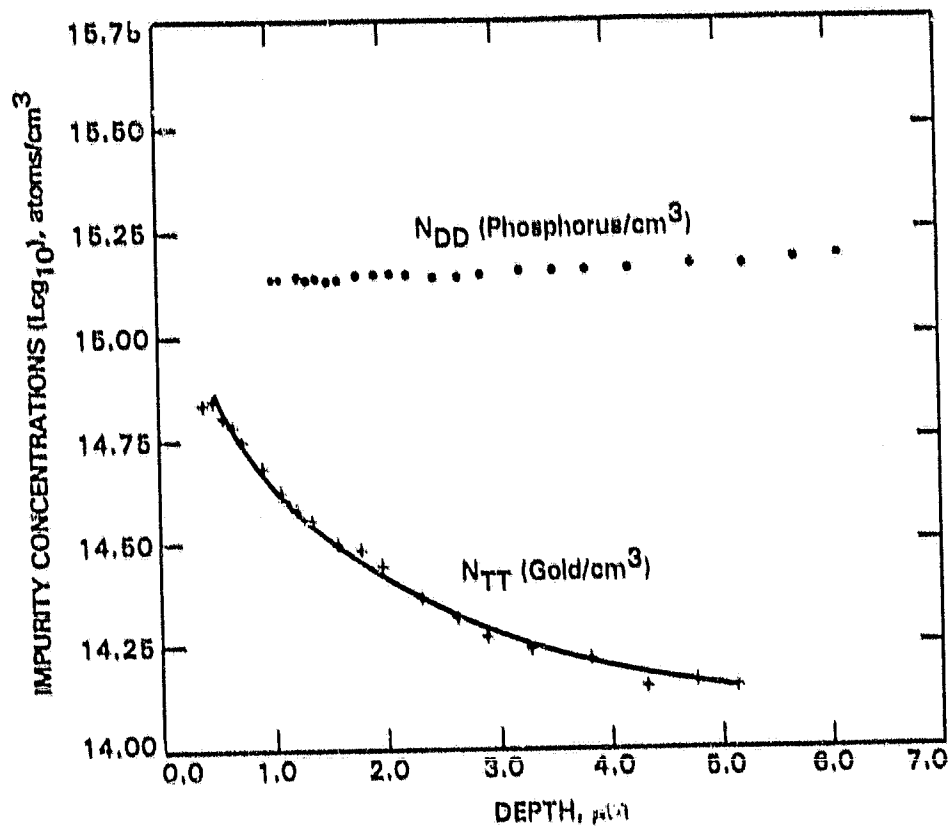
Figure 17.   Concentration Profile of Gold Diffused Into n-Type Silicon
(Reference 3)
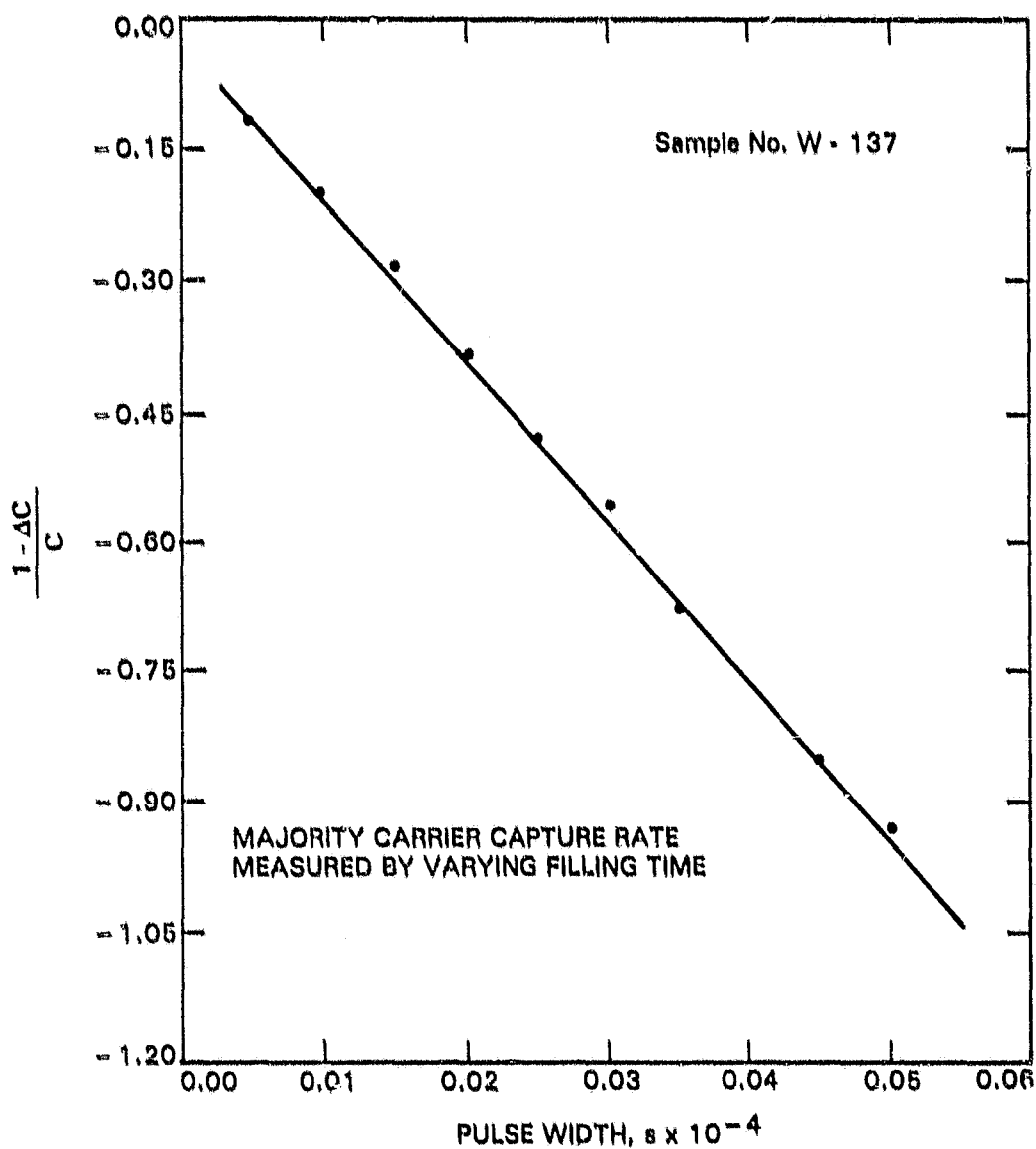
Figure 18.   Total Capacitance Change During Thermal Emission Transient (Slope Gives Majority Carrier Capture Rate) (After Sah, Reference 3)

CALCULATIONS AND RESULTS

When a capacitance transient occurs, if that transient is truly exponential with only one time constant it will follow that

$$C(t) = C_0 + (C_\infty - C_0)(1 - \epsilon^{-t/\tau}) \qquad (13)$$

where

$C(t)$ = Capacitance at any time t

$C_0$ = Capacitance at start of transient

$C_\infty$ = Capacitance at end of transient

$\tau$ = Capacitance time constant (an exponential function)

If a least-square fit (Reference 14) of the capacitance transient data is made and that data proves to be in good correlation with an exponential function as described in Equation 13, the emission rate of carriers can be obtained. For the data shown in Figure 15 the emission rate $e_r$ was calculated as 0.062 carriers per second at 111.24°K.

A set of emission rates is taken over the temperature range of 104°K to 122°K, as shown in Figure 16. Emission rate is related to thermal activation energy level by the Arrhenius equation

$$e_r = AT^n \quad (-\Delta E/kT) \qquad (14)$$

where $AT^n$ is known as the pre-exponential factor. The pre-exponential factor obtained from the capacitance transient method assumes that the emission cross section is independent of temperature, so n = 2. Applying a least-squares fit to a set of emission rates versus reciprocal temperature (the Arrhenius plot) gives the thermal activation energy level, E. From the exponential curve fit calculation b, the slope of the Arrhenius plot is obtained. Applying an exponential curve fit (Figure 16):

$$b = -3.0445$$

The activation energy level is found from

$$E = \frac{b \cdot k \cdot 1000}{q} \qquad (15)$$

where

$k$ = Boltzmann's constant = $1.38 \times 10^{-23}$ joules/molecule-°K

$q$ = Electron charge = $1.6 \times 10^{-19}$ coulombs

and if

$$b = -3.0445$$

$$\Delta E = -262 \text{ meV}$$

Thermal activation energy levels and thermal activation temperatures for selected elements are presented in Tables 1 and 2 respectively.

The majority carrier capture rate can be calculated assuming that the emission cross section is independent of temperature (n = 2) and of electric field. The time constant of the capacitance rise is given by the reciprocal of the thermal capture rate times the electron (or hole) density. Therefore,

$$\tau \approx \frac{1}{c_x} \tag{16}$$

where

$\tau$ = capacitance time constant (an exponential function)

x = n or p

Rewriting the equation, the emission rate is found from

$$c_x \approx \frac{1}{\tau}$$

Now the concentration of the recombination or trapping centers and the sensitivity of the CTS method is determined.

The junction space-charge layer width

$$W \propto \frac{1}{\sqrt{\rho}} \propto \frac{1}{\sqrt{N_{DD} - n_T(t)}} \tag{17}$$

and the high-frequency capacitance of the junction

$$C \propto \sqrt{\rho} \propto \sqrt{N_{DD} - n_T(t)}$$

are combined to calculate the total trap concentration, $N_{TT}$. The fractional capacitance change is then equal to 1/2 of the fractional space-charge density change

$$\frac{\Delta C}{C} = \frac{\Delta \rho}{2\rho} = \frac{N_{TT}}{2N_{DD}} \tag{18}$$

or

$$N_{TT} = \frac{2\Delta C \cdot N_{DD}}{C} \tag{19}$$

24

The change in space-charge concentration comes from the thermal release of trapped charge in the space charge region.

For the capacitance transient shown in Figure 19,

$$\frac{\Delta C}{C} = \frac{N_{TT}}{2N_{DD}} \tag{20}$$

where

$N_{DD} = 10^{14}$ atoms/cm$^3$

$\Delta C = 5 \times 10^{-4}$ pf

$C = 0.345$ pf

then

$N_{TT} = 2.89 \times 10^{11}$ atoms Au/cm$^3$

Experimentally it was determined that the capacitance meter has a noise level of about .0001 pf. If the measured capacitance is 5 times the noise level, then the method sensitivity is

$$N_{TT}/N_{DD} = \frac{2\Delta C}{C}$$

$$= \frac{5 \times 10^{-4}}{10}$$

$$= 10^{-4}$$

where

$C$ = the maximum capacitance that the meter is set for (10 pf)

$\Delta C$ = S/N · noise

This sensitivity means that 1 trap in 10,000 dopant impurity atoms can be detected if a S/N of 5 can be obtained. For a typical sample with $2 \times 10^{15}$ phosphorus atoms/cm$^3$, $2 \times 10^{11}$ traps/cm$^3$ can be detected.

If the sensitivity is measured as $10^{-4}$ times the dopant impurity, then the total number of traps can be obtained from

$$N_{TOTAL} = N_{TT} \, A \cdot W \tag{21}$$

$$= N_{DD} \frac{2 \, (\Delta C)}{C} A \cdot W$$

$$= 2N_{DD} \frac{(\Delta C)}{\mathcal{E}A} A \cdot W^2$$

$$= 2N_{DD}(\Delta C)(2\mathcal{E}V/qN_{DD})/\mathcal{E}$$

$$= \frac{4\Delta CV}{q} \tag{22}$$
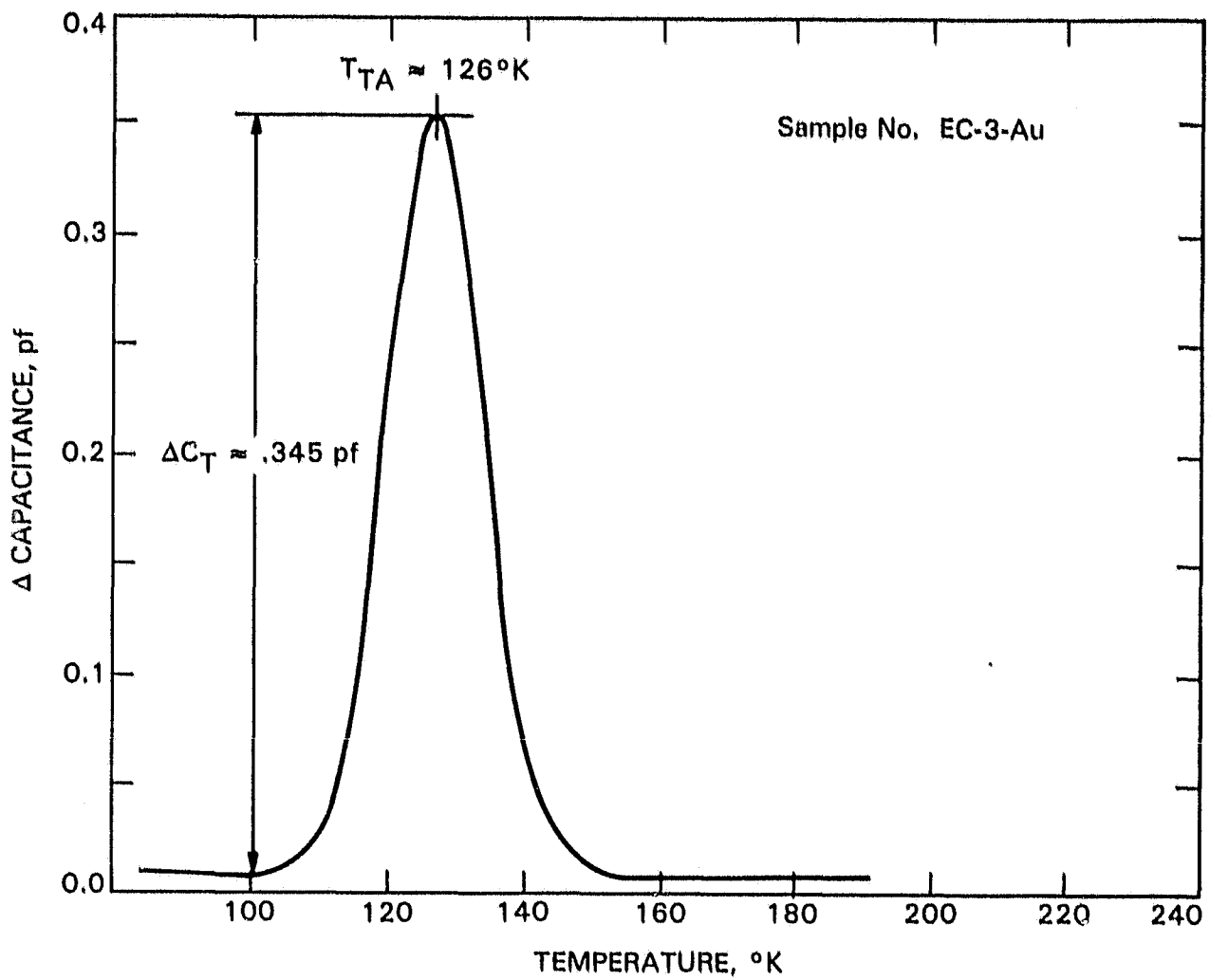
Figure 19. TSCAP Showing Gold Center

where $V = V_D + V_R$, the barrier height of the junction.

This equation is only valid for an abrupt junction with a spatially constant concentration of recombination and dopant impurities. Then, if $C = \text{noise} = 10^{-4}$ pf

$$N_{TOTAL} = \frac{4(\Delta c)V}{q}$$

$$= 2500V \text{ traps}$$

if

$$V = 4$$

$$N_{TOTAL} = 10,000 \text{ traps}$$

In performing each of the previous calculations, accurate temperature data is essential. In order to obtain accurate temperature values a 14th-order polynomial approximation for the T-type thermocouple is solved. The polynomial equation (Reference 15) is

$$V = V_0 + V_T T + V_2 T^2 + V_3 T^3 + V_4 T^4 + V_5 T^5 + V_6 T^6$$

$$+ V_7 T^7 + V_8 T^8 + V_9 T^9 + V_{10} T^{10} + V_{11} T^{11}$$

$$+ V_{12} T^{12} + V_{13} T^{13} + V_{14} T^{14} \tag{23}$$

where

$$V_0 = 5.536 \times 10^3$$
$$V_1 = 3.874 \times 10^1$$
$$V_2 = 4.412 \times 10^{-2}$$
$$V_3 = 1.141 \times 10^{-4}$$
$$V_4 = 1.997 \times 10^{-5}$$
$$V_5 = 9.045 \times 10^{-7}$$
$$V_6 = 2.277 \times 10^{-8}$$
$$V_7 = 3.625 \times 10^{-10}$$
$$V_8 = 3.865 \times 10^{-12}$$
$$V_9 = 2.830 \times 10^{-14}$$
$$V_{10} = 1.428 \times 10^{-16}$$
$$V_{11} = 4.883 \times 10^{-19}$$
$$V_{12} = 1.080 \times 10^{-21}$$
$$V_{13} = 1.395 \times 10^{-24}$$
$$V_{14} = 7.980 \times 10^{-28}$$

It should be noted that Equation 23 is valid only for temperatures below 0°C. A different polynomial is used for temperatures above 0°C.

Table 1.  Thermal Activation Energy Levels From CTS for n = 2
         (References 2, 3, 4, 7, 16)

| Secondary Impurity | Energy Level(s) |
|---|---|
| Gold | $E_V + 0.590$ |
| | $E_V + 0.345$ |
| | $E_C - 0.588$ |
| Silver | $E_V + 0.359$ |
| | $E_C - 0.578$ |
| Aluminum | $E_V + 0.214$ |
| | $E_V + 0.312$ |
| | $E_V + 0.402$ |
| | $E_C - 0.389$ |
| Sulfur | $E_C - 0.276$ |
| | $E_C - 0.528$ |
| Oxygen | $E_C - 0.186$ |

Table 2.  Selected Thermal Activation Temperature Ranges From CTS (Reference 3)

| | |
|---|---|
| Vanadium | 220 to 260°K |
| Titanium | 130 to 200°K |
| Molybdenum | 150 to 180°K |
| (Aluminum) | 150 to 200°K |
| (Aluminum) | 220 to 260°K |
| Niobium | 85 to 100°K |
| (Gold) | 125 to 128°K |

Parentheses indicate that more than one trapping level exists for that element and more than one transient will be seen.

28

# SECTION V

## DISCUSSION

TSCAP and VSCAP limitations can be divided into four categories; with an understanding of them, and with careful experimental techniques, most of these limitations can be overcome.

The first limitation is resolution of measurement data. Great care must be taken to ensure that capacitance and temperature data are accurate (an error in temperature reading of as little as $0.1^\circ K$ can result in an error in $\Delta E$ of 3 meV).

The second limitation is surface channel leakage. New peaks can result from any signal leakage away from the diode junction. This can be eliminated by the addition of a metal-oxide semiconductor (MOS) guard ring around the diode (see Figure 4).

The third limitation is leakage current or interface irregularity of the Schottky barrier diode. A poor metal-to-silicon interface gives rise to high leakage current, which increases the measurement noise level and decreases sensitivity.

The fourth limitation is resolution of overlapping signals. If the thermal activation temperatures of two adjacent trapping levels are separated by only a few degrees, then the bell-shaped capacitance curve (Figure 14) can become a two-peak bell-shaped curve or a one-wide-peak curve. A rough estimate can still be made as long as two peaks can be identified.

Even with these limitations, it is evident that CTS is a useful technique.

# SECTION VI

## SUMMARY

Automated and manual techniques for performing TSCAP to determine an impurity's thermal activation temperature and electrically active concentration are presented. An automated technique for performing VSCAP to determine impurity activation energy level(s), capture rate, and electrically active concentration is also presented. Experimental results on silicon samples demonstrate the usefulness of these techniques in evaluating semiconductor materials. Formulae used to calculate all TSCAP and VSCAP results and an experimental procedure are presented. Block diagrams are provided for both the manual and automated techniques, with identification of the equipment used in each block. These techniques can be used to detect electrically active impurity concentrations of as little as $10^{10}$ atoms/cm$^{-3}$ in a substrate with $10^{14}$ atoms/cm$^{-3}$ of primary impurity concentration.

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