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INVESTIGATION OF RELIABILITY ATTRIBUTES AND ACCELERATED STRESS FACTORS ON TERRESTRIAL SOLAR CELLS

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1981 SUMMARY REPORT

Department of Electrical and Computer Engineering

CLEMSON UNIVERSITY

Clemson, SC 29631

Report Date: June 1982

Principal Investigator: J.W. Lathrop

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Pasadena, California 91103

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ENGINEERING AREA

INVESTIGATION OF RELIABILITY ATTRIBUTES AND ACCELERATED STRESS FACTORS OF TERRESTRIAL SOLAR CELLS

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Principal Investigator: J.W. Lathrop

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The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory California, Institute of Technology by agreement between NASA and DOE.

ACKNOWLEDGEMENTS

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The Jet Propulsion Laboratory Technical Manager for this work was Mr. Edward L. Royal. His numerous contributions to the program are gratefully acknowledged.

ABSTRACT

The 1981 Summary Report on Clemson University's program to investigate the reliability attributes of terrestrial solar cells summarizes the accelerated stress test results obtained on all cells since the inception of the program, as well as describes specific results obtained during the fourth year's effort. Tested cells were grouped according to the method used to form the conductive metallization layer: solder dipped, vacuum deposited, screen printed, and copper plated. Although metallization systems within each group were quite similar, they differed in numerous details according to the procedures employed by each manufacturer. Test results were summarized for all cells according to both electrical degradation and catastrophic methanical changes. These results indicated a variability within each metallization category which was dependent on the manufacturer. Only one manufacturer was represented in the copper plated category and, although these showed no signs of detrimental copper diffusion during high temperature testing, their metallization was removed easily during high humidity pressure cooker testing. Preliminary testing of encapsulated cells showed no major differences between encapsulated and unencapsulated cells when subjected to accelerated testing. While further work must be performed, this seems to indicate the major role of encapsulation to be mechanical protection. An appendix is presented which gives an overview of the data collection and analysis procedures developed on the contract.

SUMMARY

The fourth year of Clemson University's accelerated reliability testing program involved both the continued testing of older cells as well as a number of newer types more recently introduced into the program. A primary goal of this report is to summarize the attributes of all tested cell types prior to initiating a new round of tests. In addition, some preliminary investigations were conducted on encapsulated cells in an effort to determine the direction of future work in this area.

Because metallization appears to be the most vulnerable aspect of a solar cell when subjected to accelerated testing, the twelve cell types that have undergone testing in the program were grouped for comparison purposes according to the method used to form the conductive layers: solder dipped, vacuum deposited, screen printed, and copper plated. The results of accelerated testing were then compared in regard to the amount of electrical degradation measured and the seriousness of the mechanical changes observed. Within the solder, vacuum, and screen categories certain cell types were observed which showed great sensitivity. Tables are presented in the report showing test-by-test comparisons for the cells. These results would imply that it is possible to form reliable contacts with any of these three metallization systems, but that not all manufacturers are achieving satisfactory results. Only one manufacturer submitted cell types with copper plated metallization, so that no comparisons between manufacturing techniques could be made. However, while no detrimental effects of copper diffusion were observed on high temperature B-T testing, these cell types showed up very poorly on high temperature humidity testing. The copper plated metallization lifted off the cell after only a

relatively short exposure.

A relatively few samples of encapsulated single cell minimodules were subjected to essentially the same test schedule developed for unencapsulated cells. The minimodules were of two types: rigid substrate with plastic surface protection and rigid glass superstrate with plastic backing. The upper temperatures of the B-T test schedule (125°C and 150°C) were too high for the plastic materials involved. In the remaining tests similar amounts of electrical degradation were observed for both types of minimodules and the unencapsulated control cells. Although the minimodules were not edge protected and further testing should be performed, the result would seem to indicate that the major roll of encapsulation is mechanical protection and that its presence will retard, but not prevent moisture penetration. Further work is in order to determine the seriousness of this moisture penetration and to establish correlation with tests on unencapsulated cells.

A key factor is the ability to determine the effect of testing is rapid and accurate data collection and analysis. An appendix to the report presents an overview of the sophisticated computer based system which has been developed over the years on this contract.

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1.0 INTRODUCTION

This is the 1981 Summary Report on the Investigation of Reliability Attributes and Accelerated Stress Factors on Terrestrial Solar Cells, a program which has been conducted by Clemson University for the Flat-Plate Solar Array Project of the Jet Propulsion Laboratory. The objective of the study has been to develop test specifications and techniques which could be used to ensure an adequate level of reliability for flat plate silicon terrestrial cells. The approach was to design laboratory test schedules which would accelerate anticipated field failure modes, and then to evaluate these test schedules by subjecting to them quantities of commercially available cells. Examination of test results over an extended period of time on many different types of cells has led to a suggested accelerated schedule for unencapsulated cells which Clemson University feels could be used to give the desired early indications of operational reliability problems. The program was initiated in December of 1977 and earlier reports [1,2,3] have discussed in detail the experimental and analytical methods employed, the data collected, and some preliminary conclusions. It is the purpose of the 1981 Summary Report to present recently obtained data on previously unreported cells, to report preliminary results on the application of accelerated stress testing to encapsulated cells, and to qualitatively summarize the results for the total program.

Reliability is a key factor in the implementation and acceptance of photovoltaic energy generation on a national scale. Somewhat arbitrarily a useable life goal of 20 years for terrestrial photovoltaic arrays has been set, and preliminary economic planning and justification have been based on this figure. Such a goal appears achievable since reliability of this magnitude or greater has indeed been demonstrated by solar cells employed in

the space program. However, the driving factor in the terrestrial photovoltaic program is cost. Reductions in the cost of cells are expected, in part, to be brought about through automation, the use of new and less expensive materials, and design modifications. With the great emphasis on designing to cost, these changes may well affect reliability adversely. It is therefore important, as the photovoltaics program progresses down the economic learning curve, that the degradation mechanisms associated with each new design be understood and their impact on reliability be anticipated in order to avoid consumer dissatisfaction, such as occurred when the early heat pumps were introduced in the 60's or as is occurring now with solar thermal systems.

Photovoltaic reliability depends on many diverse factors, involving both design and fabrication all the way from the system and array level through the module to the basic cell. As in electronic systems, where the basic component (e.g. integrated circuit) is the foundation on which system reliability is built, so the solar cell establishes the basic reliability level for the photovoltaic power system. Because, like the integrated circuit, the solar cell is a highly reliable device with a low failure rate, it is also not possible to determine its mean time to failure, or other meaningful statistical reliability measures, in real time. Accelerated laboratory testing, whereby cells are subjected to higher than normal levels of stress designed to accelerate particular failure mechanisms that are anticipated in the field, offer the only hope of obtaining meaningful reliability measures within a reasonable time. The program therefore undertook:

1. to determine accelerated stress tests which, when applied to unencapsulated cells, could be used to compare the relative sensitivity of different designs to environmental stress, and

2. to establish base line data on the sensitivity to these accelerated tests of conventional state-of-the-art cells for later comparison purposes with advanced-type future cells.

It should be noted, however, that a significant difference exists between the solar cell and its reliability counterpart, the integrated circuit. The IC is manufactured to well defined specifications and if its performance were to degrade below one of these specified limits there is a good chance the system would fail. In the limit, if a bond were to open up making the IC inoperable the system would also be inoperable since it is not likely to incorporate circuit redundancy. The solar cell on the other hand is not manufactured to such rigorous specifications. Furthermore, because a typical system, of kilowatt or greater size, is made up of thousands of identical cells, there will be a great deal of circuit redundancy and failure of a single cell, even an open circuit, will not cause system failure.[4] The important aspect of solar cell failure is therefore not so much the identification of isolated failures as it is characterization of the average amount of degredation as a function of time and the determination of the frequency of catastrophic open circuits.

Whereas previous reports have discussed in detail the accelerated test methods that were used in the program and presented the data that was obtained, both graphically and in tabular form, this report takes a broader view by assessing the significance of the results and offering possible explanations for the observed behavior. Consequently much of the data is presented in the form of "best fit" curves without showing specific data points which tend to make the plots busy and confusing.

2.0 TEST SCHEDULE DEVELOPMENT

At the start of the Clemson program little was known concerning the degradation modes of terrestrial solar cells. In order to develop a meaningful test schedule it was first necessary to decide what types of accelerated tests should be included and then, through experimentation, to select appropriate stress levels, test times, and sample sizes. At the same time, a vast body of information existed concerning integrated circuit time-dependent failure mechanisms, and corresponding accelerating factors, which could be used as a starting point. Examination of this information indicated that there were four basic physical aspects of integrated circuits affected by various time dependent failure mechanisms: surface, metalization, bonds, and hermeticity. The surface effects of solar cells might be expected to be minimal compared to those of MOS, or even bypolar, IC's. There is, however, a surface termination of the p-n junction, which may or may not be covered with a protective oxide, and which can experience the shunting effects of contamination. The susceptible area of a solar cell, however, represents only a small fraction of the total device area as compared to the same fraction for an integrated circuit. One surface condition that is specific to solar cells involves the thin transparent antireflecting (AR) film whose thickness is optimized to provide an optical impedance match between the different media in contact with each other at the surface. This coating is subject to environmental degradation, resulting in discoloration and/or delamination, which may affect the cell's electrical output. It should be noted that while cell performance may be improved only a few percent by the application of an AR coating, it could be degraded by a greater amount, as the result of a mismatched coating, so that this

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potential degradation mode may not be as negligible as first might appear. In addition, while not strictly a surface phenomenon, there is the possibility of metallization from the surface diffusing along grain boundaries and resulting in increased junction leakage. Thus the surface effects of solar cells, instead of being influenced by processes such as charge accumulation, dielectric breakdown, and charge injection, should be affected by contamination, corrosion (AR coating), and diffusion. Consequently the anticipated accelerating parameters are humidity and temperature. (See listing in Table 1).

Degradation processes affecting metallization should result in the predominant solar cell failure modes observed in the field and should be much more analogous to those affecting IC's: electromigration, corrosion, and contact degradation, with accelerating parameters involving humidity, temperature, and voltage. The degree of sensitivity, however, might be expected to be less than IC's because of greater dimensions (mils instead of micrometers), greater contact area per contact, and a fewer number of critical contacts.

Similarly, the sensitivity of solar cells to bond degradation could be expected to be less than for IC's because of bond redundancy and the larger contact areas involved. Nevertheless, the accelerating factors should be temperature and rate of change of temperature with time. Finally, solar cells are not completely hermetically encapsulated and therefore will be subject to moisture penetration which should be accelerated by increasing pressure. Initial stress testing was done using unencapsulated cells where hermeticity was not a factor, but ultimately it is necessary to relate this testing to interconnected operational cells in the module environment. Results of a preliminary investigation of techniques for accelerating degradation in encapsu-

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PHYSICAL REGION	DEGRADATION PROCESS	RELEVANT FACTORS	ACCELERATING PARAMETERS
SURFACE	JUNCTION LEAKAGE	MOBIL IONS CONTAMINATION DIFFUSION	V, T
	AR COATING	H, T	H, T
METALIZATION	ELECTROMIGRATON PLATING	T, J GRADIENTS OF T AND J, GRAIN SIZE	T, J
	CORROSION CHEMICAL GALVANIC ELECTROLYTIC	CONTAMINATION V, T, H	V, T, H
	CONTACT DEGRADATION	T, METALS IMPURITIES	T
BONDS	INTERMETALLIC GROWTH	T, IMPURITIES, BOND STRENGTH	T
	FATIGUE	TEMP CYCLE BOND STRENGTH	T EXTREMES CYCLING
SUBSTRATE	FRACTURE	TEMP CYCLE EXPANSION COEFFICIENTS	T EXTREMES CYCLING

T=TEMPERATURE
H=HUMIDITY
J=CURRENT DENSITY
V=VOLTAGE

TABLE 1. Time-Dependent Failure Mechanisms Anticipated in Silicon Solar Cells.

lated cells, which is expected to become the basis for a later more complete study, is described in this report.

An additional failure mode anticipated for solar cells, but not experienced with IC's, is fracturing due to differential thermal expansion between the metalization and the silicon. This is a consequence of the large area (commonly 3" to 4" diameter) cells. Fracturing, as with bond degradation, should be accelerated both by temperature and by the rate of change of temperature with time.

The four physical regions of cells subject to failure, the anticipated degradation processes affecting each, the factors which could cause this degradation, and the appropriate accelerating factors are summarized in Table 1. It is thus seen that despite the variety of different mechanisms involved, only five accelerating parameters need be considered: voltage, current density, temperature, humidity, and the rate of change of temperature with time. Furthermore, it should be noted that in a given device, voltage and current density will be related.

Based on this type of reasoning, plus consideration of likely use condition stresses, categories of accelerated stress tests were selected for investigation and a test program initiated. These were bias-temperature tests, bias-temperature-humidity tests, temperature-humidity tests, thermal cycle and thermal shock, and a power cycle test. The experimental approach was to subject a number of different state-of-the-art designs to specific test schedules within these stress categories. Based on the electrical and visual changes that were observed, the tests, test time, and the number of cells could then be modified and the process repeated. From such iterations a suitable accelerated test schedule for terrestrial cells, one in which the user had confidence, should eventually evolve. The resulting schedule should be one which

permits comparative data to be obtained in a minimum period of time, using a minimum number of cells, and ideally be correlatable with field performance.

Conventional reliability methodology, as shown in Figure 1, was used. The cells were initially electrically measured and visually inspected, then subjected to a particular stress condition for a period of time, and then remeasured and reinspected. This sequence of measure-stress-measure was repeated many times for each stress condition. A computerized electrical measurement system was developed,[5] with a repeatability of 1%, in order to detect the stress induced changes. This measurement system in turn was part of a sophisticated data handling and analysis system whose operation is described in detail in Appendix A. Since it has repeatedly been observed that the most common time to failure distribution of semiconductor devices, under both use stress and accelerated stress, is the lognormal distribution the cumulative stress time was doubled for each down time. Initial down times were selected on the basis of estimated test severity and later adjusted as data became available. In addition to electrical measurements and visual observations, metal adherence measurements were attempted early in the program.[6] These were found to be difficult to conduct, however, and yielded inconclusive evidence with the result that these measurements were discontinued until better techniques could be developed.

Accelerated testing may result in a gradual and consistant decrease in the maximum electrical power output of a cell as a function of test time and/or a discontinuous and perhaps catastrophic mechanical change. Gradual degradation could occur, for example, as a result of an increase in series resistance due to corrosion at the metal semiconductor interface, while examples of catastrophic change would be a cell cracking or loss of a lead.

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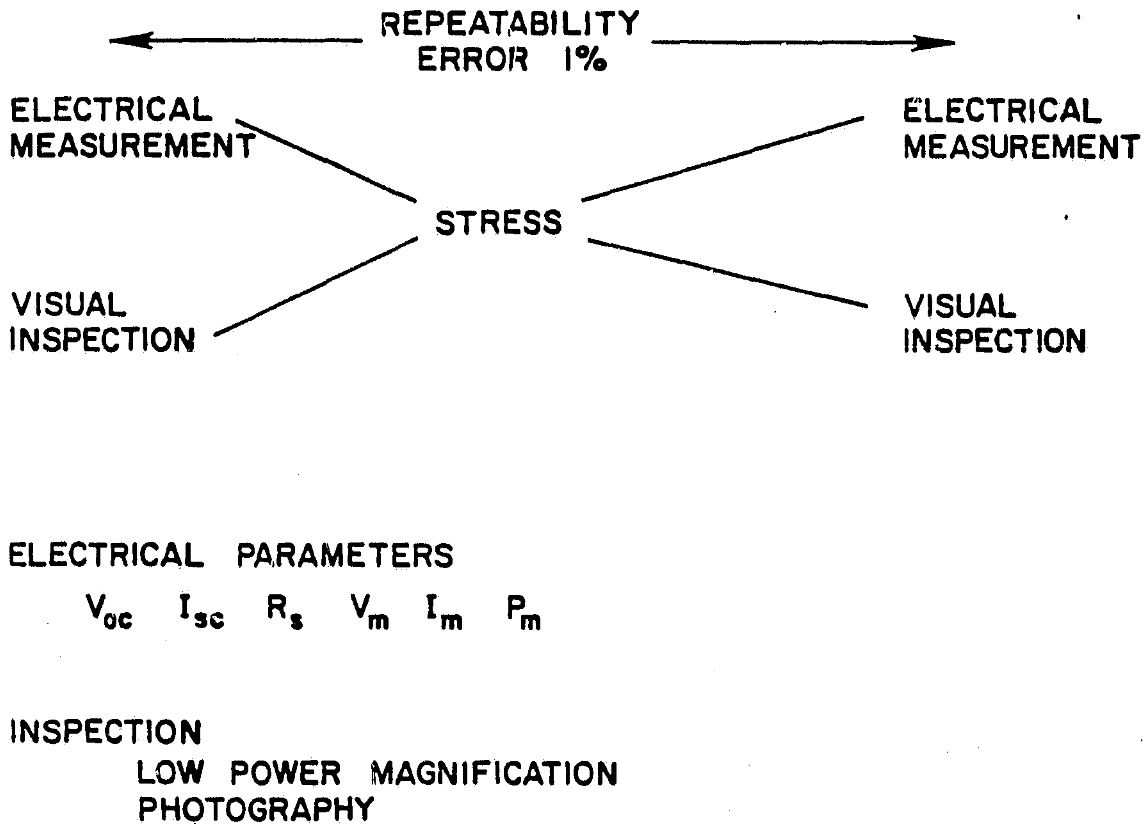

Figure 1. Reliability Methodology used in the Clemson Accelerated Test Program

Since it is not possible to define the point at which a cell becomes a "failure" in the same sense as other electronic components, the electrical data generated through accelerated testing was analyzed in terms of parametric degradation rather than in terms of device failure. Although a number of parameters (see Figure 1) were routinely measured for each cell before and after testing, the most meaningful of these was felt to be the maximum cell power, P_m.

The average decrease in P_m for a group of cells subjected to a particular stress is not necessarily a good indication of discontinuous or catastrophic behavior. At the same time, a catastrophic failure in the field, such as a cell becoming open circuited, can have a potentially serious effect on a photovoltaic array since it may lead to over-stress conditions in other parts of the system and result in a domino-like reduction in power. Thus the occurence of individual catastrophic cell changes could be far more significant than a gradual degradation which might result in an average power loss of only 5 to 10% over the life of the installation. It should also be noted that, in contrast to an electronic system, a cell short circuit is not a particularly serious event, and by itself will only result in the loss of output of the single short circuited cell.

Visual inspection was used to quantify catastrophic cell behavior. Early in the program each cell was inspected in great detail before and after stressing, and diagrams were drawn showing the location and number of observed anomalies such as bumps, spots, and color changes. Photographs were also taken to record these changes. As the number of cells in the program increased, however, it was found that the truly significant changes were being masked by the sheer mass of collected data making analysis by a limited number

of personnel virtually impossible. To avoid this problem a simplified inspection procedure was instituted whereby defects were classified according to four categories which could lead to the open circuit condition: back contact, grid contact, lead contact, or silicon fracture. Notice that other factors such as leaching of the A/R coating, which do not lead to catastrophic failure, are not included in this list, but a separate notation is made of such conditions. The severity of the four types of defects was quantified as: 0--negligible, 1--moderate, 2--catastrophic. A severity 2 condition is meant to imply a virtually inoperable cell--one that would be removed from further accelerated testing--while a severity 1 condition is intended to signal the observable onset of significant physical change. Quantification of visual defects in this fashion was still somewhat subjective, but by restricting the system to only three numerical categories it was possible for relatively inexperienced persons to quickly become proficient inspectors.

By the nature of the applied stress, different tests will tend to induce a different relative percentage of catastrophic changes and electrical degradation. A qualitative representation of the effectiveness of the tests in introducing either gradual degradation or catastrophic change is given in Figure 2. The intent of this figure is to illustrate that bias-temperature is not an effective method of accelerating catastrophic changes while thermal cycle and thermal shock testing are not effective methods of accelerating gradual electrical changes. The pressure cooker test, on the other hand, seems to accelerate both types of effects.

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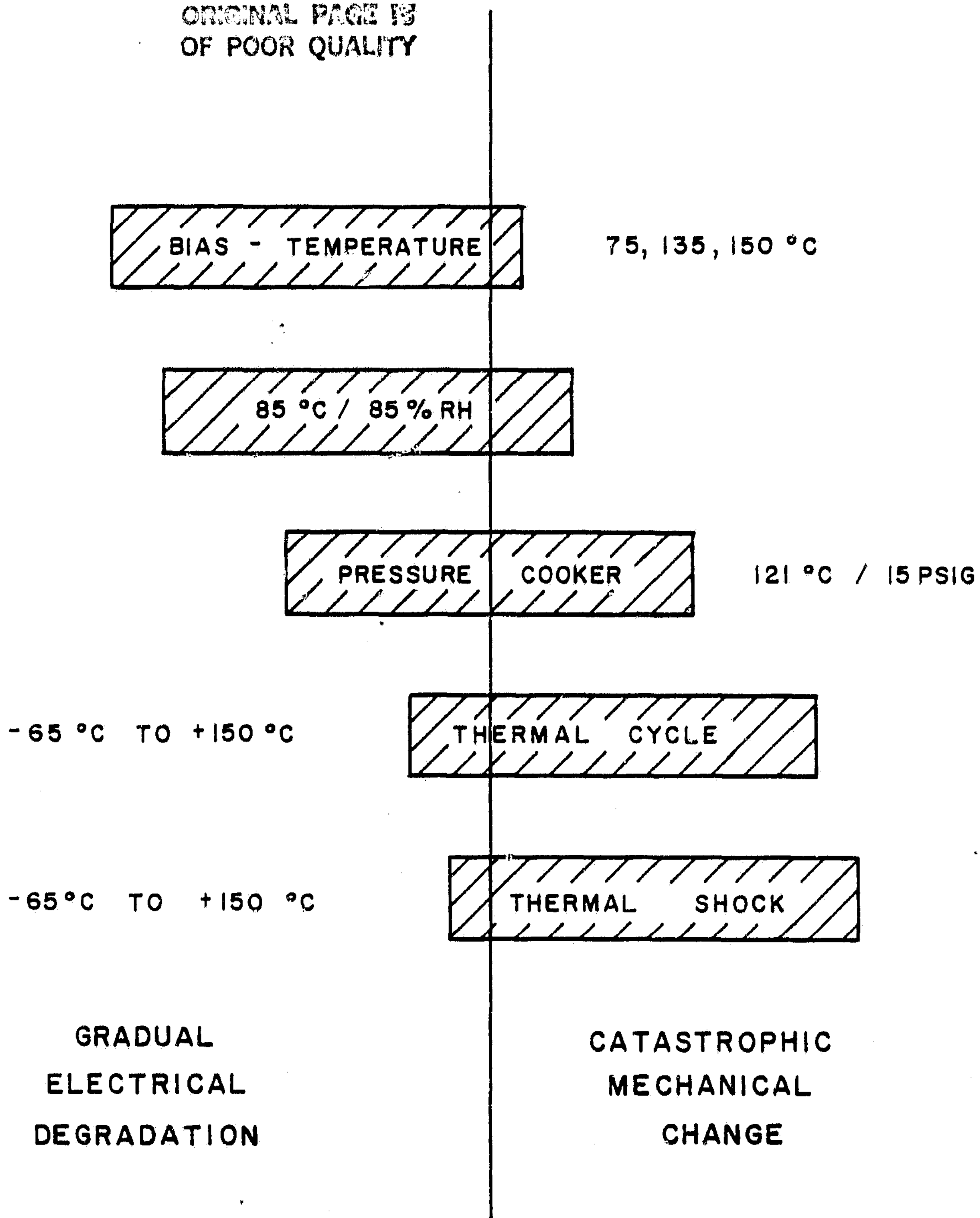

Figure 2. Relative Effectiveness of Accelerated Stress Tests in Causing Electrical Degradation and Mechanical Changes

3.0 ACCELERATED TEST RESULTS (Unencapsulated Cells)

Twelve different types of unencapsulated terrestrial solar cells and two varieties of encapsulated cells have undergone some degree of testing in the program. Table 2 summarizes the twelve types according to their metallization deposition method. The first 4 types, A-E, constitute the first group (Group I) of cells received for testing. The next 4 types, F-I, represent the second group (Group II) and were subjected to a similar test schedule, although somewhat modified as a result of the first group's testing. The final 4 types, J-M, represent the most recent group (Group III) to be entered into the test program and were subjected to what has now become the standard test schedule. The first group of cells were of conventional construction, but with a variety of metallization techniques employed. The second group involved more advanced construction techniques, including EFG and poly crystalline material and ion implanted junction formation, but still with the same basic metallization systems as employed in the first group. These first two groups were therefore used to develop the accelerated test schedule and to establish base line data on state-of-the-art cells, while the third group, which included for the first time low cost plated metallization, represented the first of a series of advanced designs aimed at meeting DOE cost goals.

For ease of notation the metallization system technology for cells tested in the program were classified according to the deposition method used for the primary conductive layer: vacuum, plated, printed, and solder dipped. Figure 3 illustrates these four categories, with the thick conductive layer shown approximately to scale. Except for printed silver frit metallization the systems also contain one or more thin ($\leq$100A°) barrier layers whose thickness and composition vary with the manufacturer. The purpose of these layers, which are not to scale in Figure 3, include preventing diffusion of the conductive metal into the silicon, making good low resistance ohmic contact to the silicon, ensuring good adhesion of the metal to the silicon surface, and providing a surface which will accept further plating uniformly. These barrier/strike layers are usually formed by techniques such as immersion

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		THICKNESS (MILS)	SURFACE	METAL DEPOSITION METHOD
I	A	24		SOLDER
	B	19	AR	VACUUM
	C	20	AR	SOLDER
	E	15	TEXT	PRINTED
II	F	13	AR	SOLDER
	G	12	AR TEXT	SOLDER
	H	12	AR	VACUUM
	I	12	AR TEXT	SOLDER
III	J	12	AR	PRINTED
	K	12	AR	PLATED
	L	13	AR	PLATED
	M	12	AR	PLATED

AR = Antireflective Coating
TEXT = Texturized Surface

TABLE 2. CELL PHYSICAL CHARACTERISTICS

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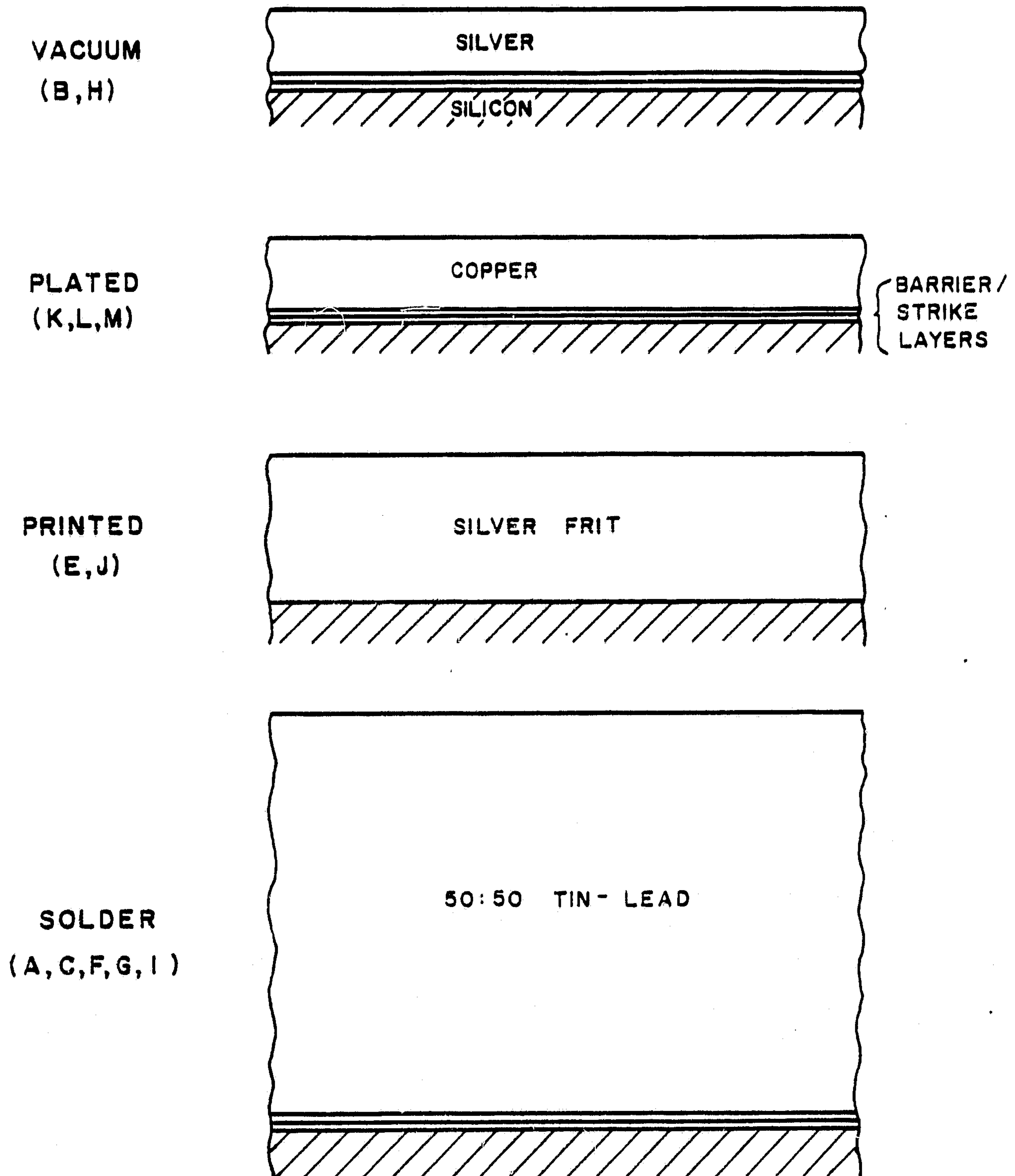

Figure 3. Solar Cell Metallizations Tested. (conductive layers shown approximately to scale)

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providing a surface which will accept further plating uniformly. These barrier/strike layers are usually formed by techniques such as immersion plating, electroless plating, electro plating, ion plating, chemical vapor deposition, and vacuum deposition. In an economic study of metallization systems performed by the University of Pennsylvania for JPL[7], systems of the type shown in Figure 2 were analyzed. On the basis of this analysis it can be concluded that of the four categories shown, only the copper plated system qualifies as a low cost approach to metallzation. Since this system therefore represents the direction future cells are expected to follow, particular attention should be directed towards interpreting the results of K-, L-, and M-cell testing.

Table 3 depicts the evolution of the accelerated test schedule in terms of types of tests and sample sizes per test, while Figure 3 lists the downtimes selected for the present schedule. Originally B-T testing was performed at 165°C, but this proved to be too near the solder melting temperature of 170°C and rather than risk introducing new failure modes this test was discontinued. A power cycle test designed to accelerate electromigration and thermomechanical effects on the metalization such as creep, fatigue and delamination was also originally scheduled. It involved forward biasing the cells with a current in excess of the shortcircuit current for an ON-period and then zero-biasing the cells for an OFF-period to allow them to cool. This resulted in repeated shallow (5°-10°C) thermal cycles accompanied by forward current flow. A standard test, similar in intent and implementation is "Intermittent Life", Method 1006, MIL-STD-883A. Since essentially no changes were observed in either the electrical or physical characteristics of cells subjected to this test to 30,000 cycles, this test was also discontinued.

Temperature-humidity testing in the form of pressure cooker and 85/85 stress was performed with and without forward biasing. The application of a

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STRESS TEST		Number of Cells in Each Test		
		Group 1 Cells (A, B, C, E)	Group 2 Cells (F, G, H, I)	Group 3 Cells (J, K, L, M)[1]
Bias-Temperature	75°C	50	30	25
Bias-Temperature	135°C	50	25	20
Bias-Temperature	150°C	40	25	20
Bias-Temperature	165°C	40	*	*
Bias-Temp-Humidity	121°C/15 psig	20	20	*
Temp-Humidity	121°C/15 psig	—	15	10
Bias-Temp-Humidity	85°C/85% RH	25	20	15
Temp-Humidity	85°C/85% RH	—	15	*
Power Cycle		25	*	*
Thermal Cycle		20	15	10
Thermal Shock		20	15	10
		290	180	110

* test deemed unnecessary

1. Recommended schedule. Some quantities were less because sample sizes were small.

Table 3. Evolution of the Accelerated Test Schedule

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forward bias was found to increase power degradation during 85/85 testing, but to have no effect during pressure cooker testing. Consequently all pressure cooker testing is now being performed without bias, considerably simplifying the environmental chamber construction.*

Finally, as the testing procedures evolved, it was found that the observed degradation effects were sufficient to permit a reduction in the number of samples. This has resulted in the recommended schedule of Figure 4 with a total sample requirement of 110 cells, down from the 290 originally used. On the other hand it is doubtful this should be reduced much further since 10 cells represents statistically desirable lower limit for any given test. On the other hand, the number of cells to be tested depends on availability and the desired quantity of cells may simply not be available. This was the case in this program for the K, L, and M developmental copper plated cells. In this instance, in order to maintain a sufficient number of cells per test, and because all 3 cell types had similar metallization, some tests were simply omitted on some types. Nevertheless, it should be understood that testing fewer than 110 cells per type can seriously reduce confidence in the statistical significance of the test results.

* It should be noted that biased pressure cooker testing of components can be dangerous due to potentially explosive hydrogen evolution occurring as a result of the dissociation of water. In this case, however, with the cells connected in parallel, the applied voltage was kept well below 1.23 volts, the dissociation voltage of water.

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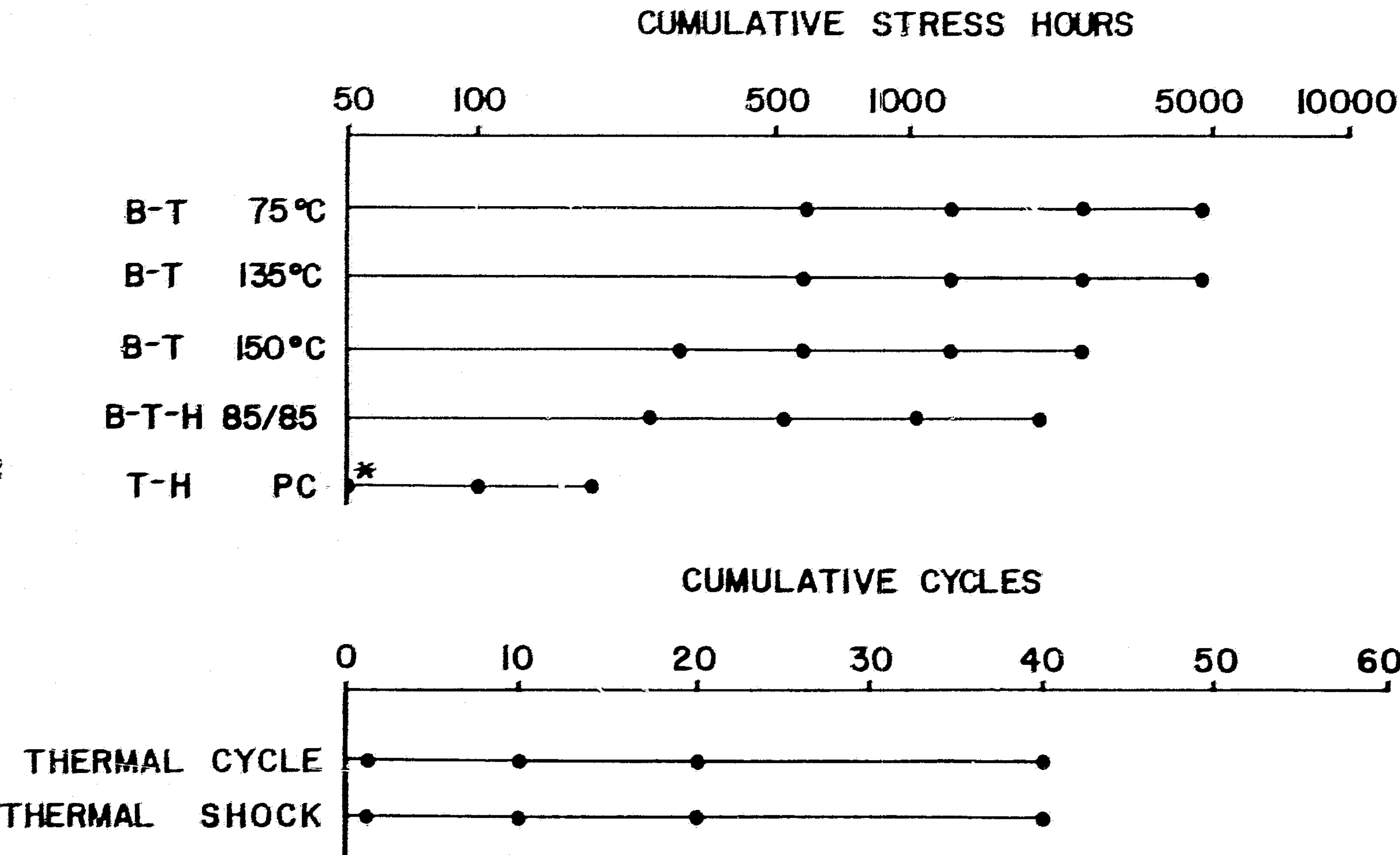

Figure 4. Present Clemson Accelerated Test Schedule for Unencapsulated Cells, Showing Points at which Electrical Measurement and Visual Inspection are made.

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3.1 Accelerated Test Results--Degradation

Bias-Temperature Testing. Bias-temperature stress testing is designed to accelerate mechanisms sensitive to current flow, or temperature, or both. Among other effects this would include penetration of the junction by metalization resulting in low shunt resistance, electromigration, and segregation effects or voiding in the metalization leading to high series resistance and/or possible poor metal or tab adherence. Bias-temperature testing should result primarily in gradual electrical degradation. Because of the wide variety of possible mechanisms this was considered a key stress test and the only one which should allow mathematical extrapolation back to use conditions.

Figure 5 shows the average change of P_m with time for A-cells subjected to 75°C, 135°C, and 150°C B-T testing. These curves can also be thought of as illustrating the change in P_m of a typical cell from each group. Of course not all the cells in a group behave identically and Figure 6 shows the change in the A-cell distribution with test time. In this case, two percent of the A-cells showed no change in 9000 hours while three percent would produce only 40% of their normal output. A-cell B-T test results are a classical example of the acceleration of a mechanism leading to gradual degradation. The nature of the mechanism is not yet understood, however. The decrease in P_m is a consequence a rise in the series resistance[8] which appears to correlate with the diffusion of a gold in silicon. A-cell metallization consists of a gold strike layer, a nickel barrier layer, and a conductive solder layer. Theories currently under investigation are that the gold in the barrier layer next to the silicon diffuses into the silicon resulting in a high resistivity layer or that oxygen diffuses to the interface resulting in formulation of a Schottky barrier. Small quantities of gold in silicon are known to result in high resistivity,[9] but when the time to 10% degradation is plotted versus the inverse absolute stress temperature for type A cells, an activation energy of

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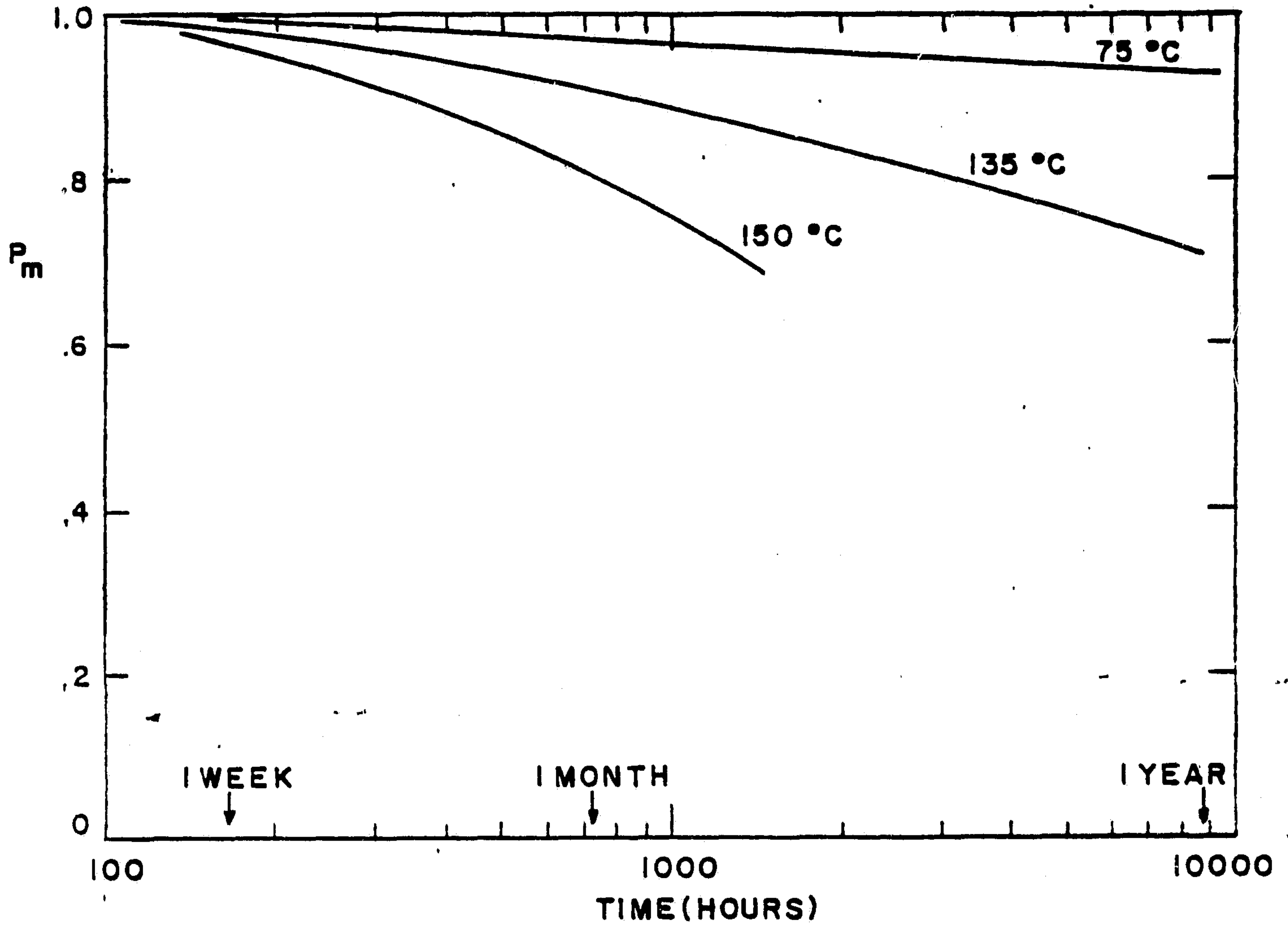

Figure 5. Average Normalized Pm as a Function of B-T Stress Time for A-Cells (Au/Ni/Solder)

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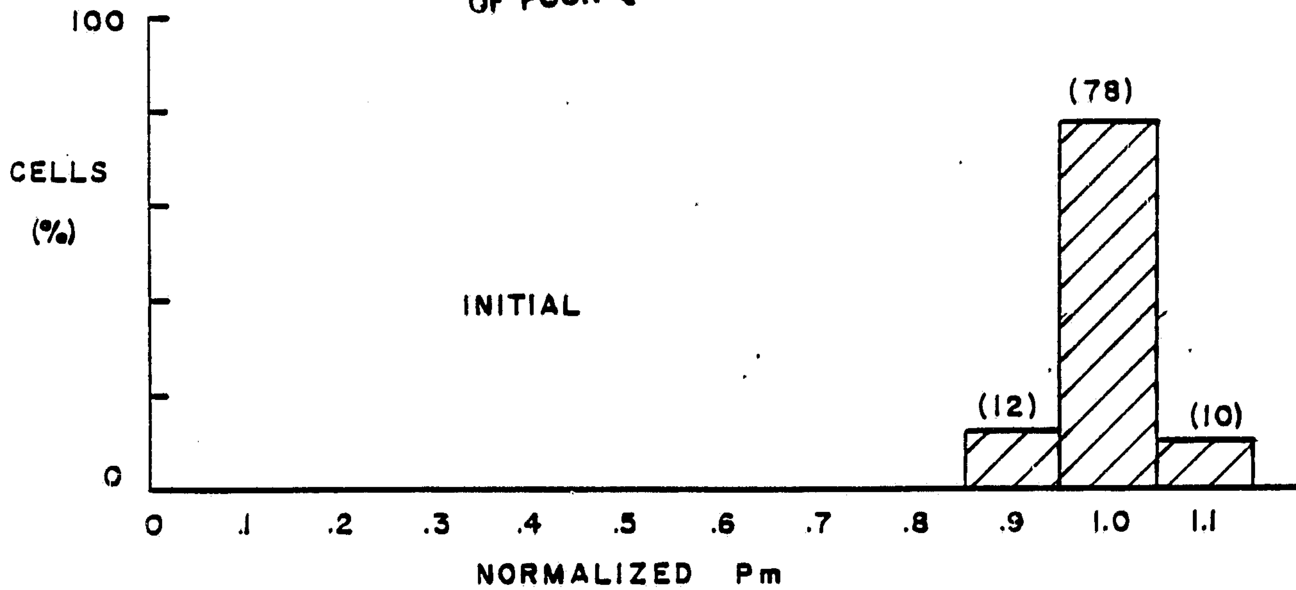

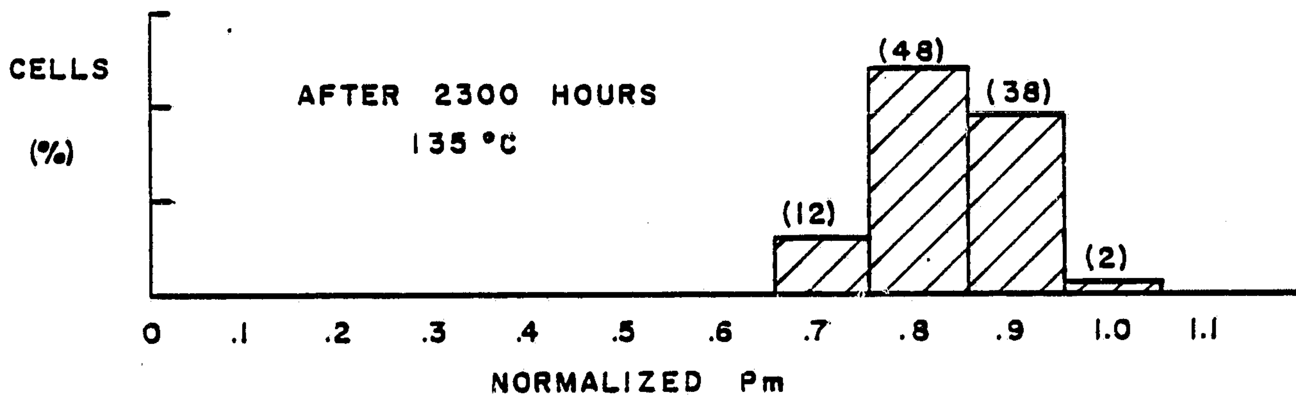

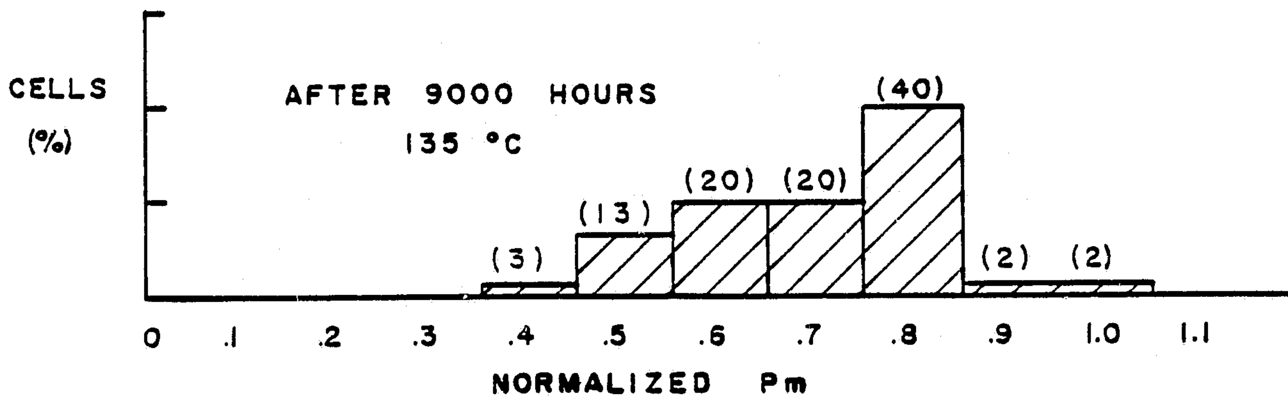

Figure 6. Change in the Pm Distribution of A-Cells as a Function of Time Stressed at 135 C.

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about 0.5eV is found[10] which is about a factor of two lower than the activation energy for gold diffusion in silicon at temperatures in the 800°C to 1200°C range. While the regularity of the phonomenon, as well as its temperature dependence, would suggest a diffusion mechanism, the exact nature of this mechanism is not yet understood.

Extrapolation to 50°C (approximate use condition) resulted in between 2 and 10 years for the time required for A-cells to degrade to 90% of their initial power output (10% power loss). Such an extrapolated degradation rate is of course only due to current and temperature, and other use-condition stress would be additive.

While the A-cells are a textbook example of a gradual degradation phenomonon, other cell types behaved differently. The B-cells, with barrier layers of titanium and palladium and a conductive layer of silver, showed essentially no decrease in P_m whatsoever with test time. The E-cells, which are screen printed with a silver frit, on the other hand, showed a threshold phenomenon, as can be seen from Figure 7. At 135°C essentially no change was observed in P_m up to 4000 hours, but then P_m decreased quite markedly with time. This same behavior was observed at 165°C, but sooner. Examination of the data indicated that the electrical manifestation was the same as for the A-cells, i.e., an increase in the series resistance, but the onset of the effect was much more sudden as can be seen from the distributions of Figure 8. No change was observed after 2300 hours, but a rectangular shaped distribution had occurred after 9000 hours compared with the more nearly normal distribution of the A-cells. This sort of behavior suggests the occurrence of either a chemical reaction or a solubility effect. It is well known, for example, that solder can leach silver and special solder compositions with a percent or two

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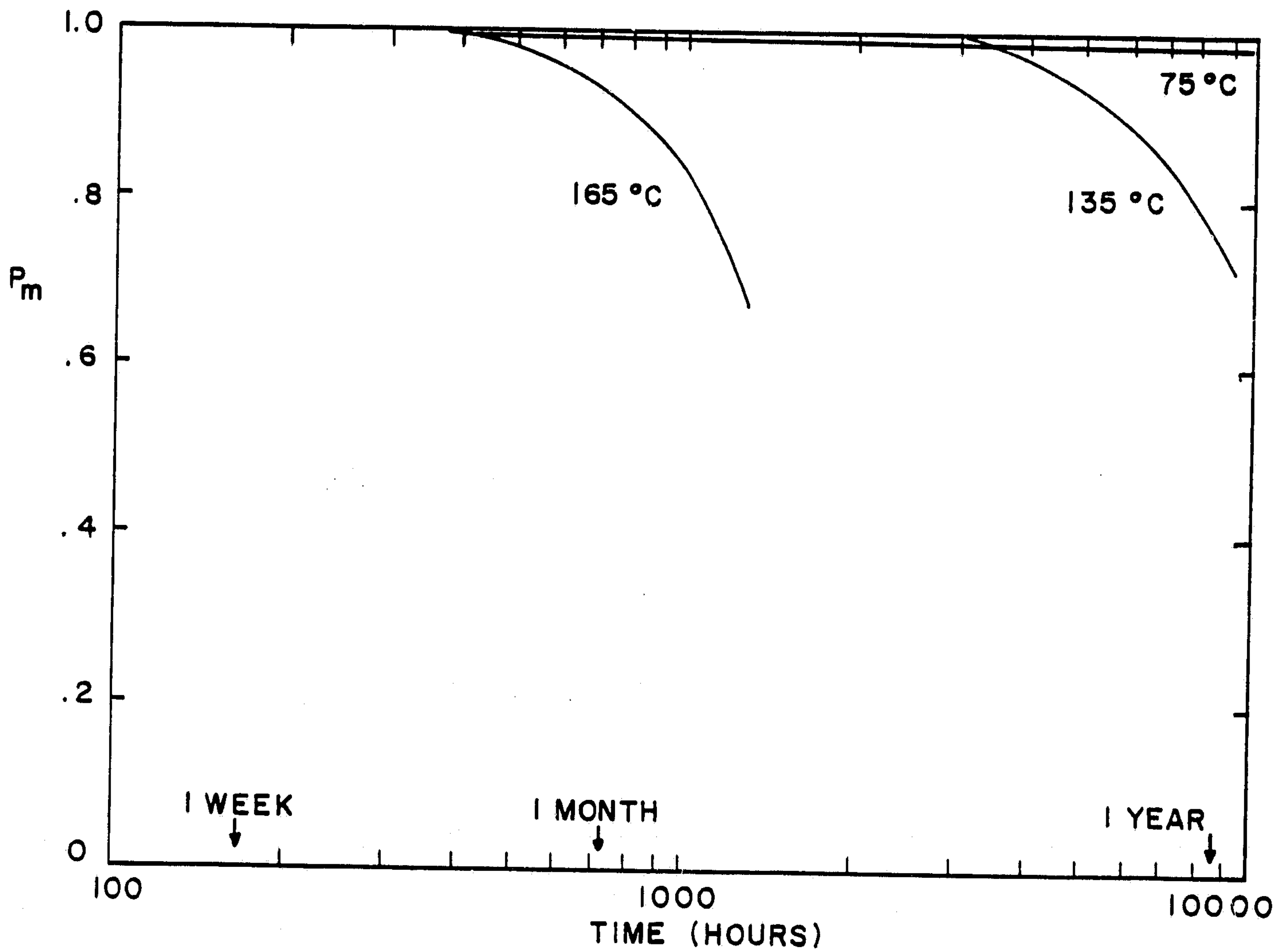
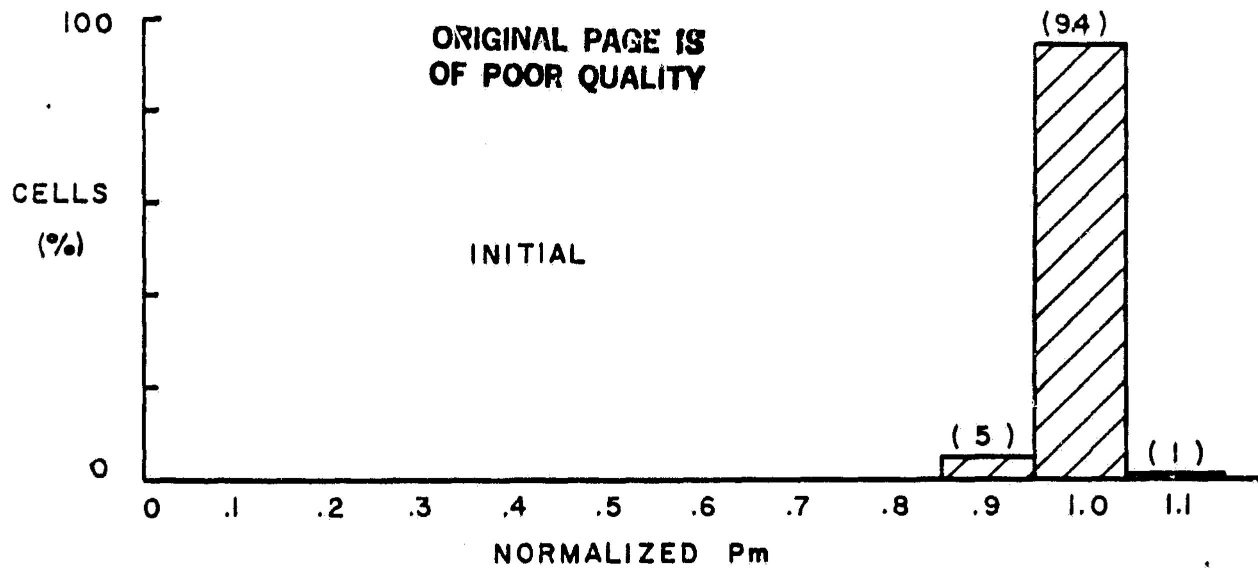
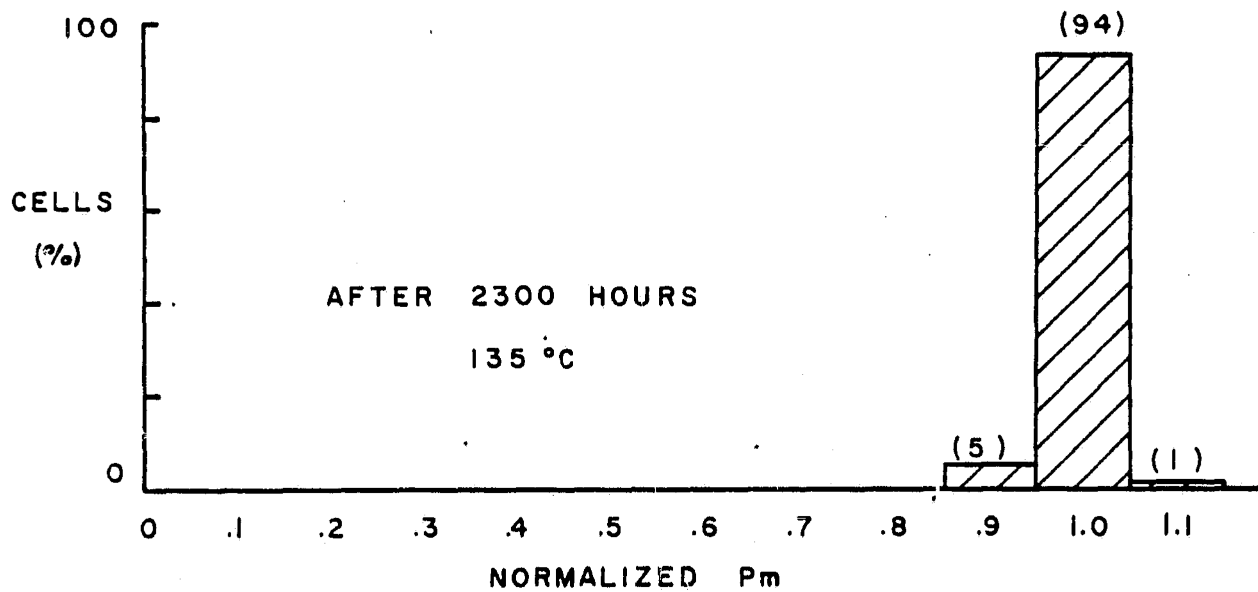


Figure 7. Average Normalized Pm as a Function of B-T Stress Time for E-Cells (Printed Ag)





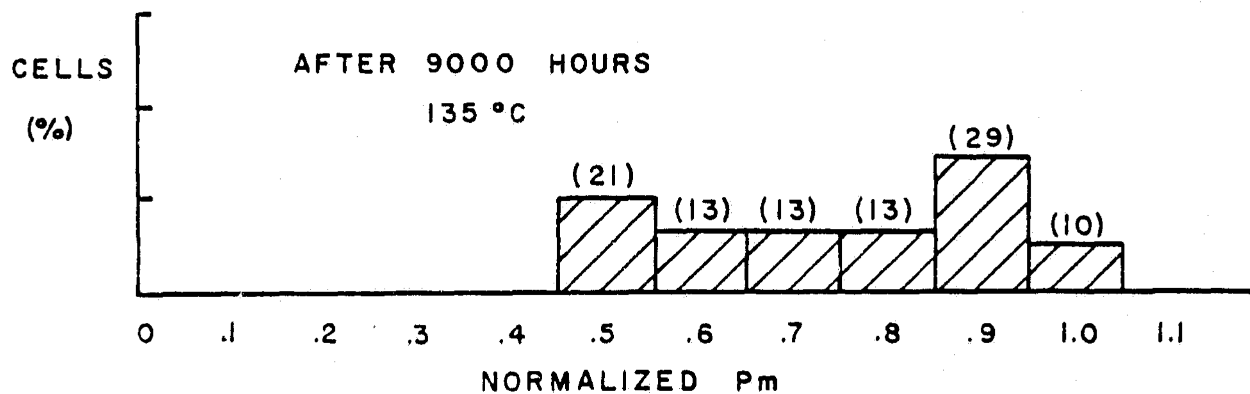


Figure 8. Change in the Pm Distribution of E-Cells as a Function of Time Stressed at 135°C.

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of silver added are often used to minimize this effect. Special attention must be paid therefor, to the metallurgy of the system when soldering to silver, as on the B- and E-cells. If such leaching action were to occur the tab adherence strength should be appreciably weakened after stressing. Despite the somewhat inconclusive results of the pull test studies mentioned earlier[6] there did appear to be a significant weakening of tab adherence for B- and E-cells after B-T testing compared to A- and C-cells. On the other hand, the vacuum deposited B-cells showed no electrical threshold effect for P_m degradation.

The copper plated K-, L- and M-cells behaved very much like the vacuum deposited cells in that they showed essentially no change. This has been confirmed independently on similar cells made by a different manufacturer.[11] There was concern that copper, which is a fast diffuser like gold, would diffuse into the silicon and degrade the cell's performance. Apparently the barrier/strike layers used in the plating process have sufficient integrity that this effect does not occur.

Humidity Testing. Humidity stress testing is designed to accelerate mechanisms sensitive to combinations of electrical bias, humidity, and temperature. Degradation mechanisms which can be accelerated by these factors include corrosion of the metallization, and electroplating one or more components of the metallization system. This type of stress test was considered a key test for determining solar cell reliability attributes because field deployment will almost certainly involve the presence of moisture and the encapsulation techniques under development merely delay, rather than prevent the ingress of moisture.

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As mentioned earlier, two types of humidity testing are included in the accelerated schedule: 85% RH at 85°C with forward bias applied, and 121°C-15 psig (pressure cooker) without bias. As might be imagined, the pressure cooker stress was the more severe test, resulting in the greatest decrease in P_m. However different devices showed different relative sensitivities to the two types of tests indicating that they probably accelerate different failure modes.

Response of the A-cells (solder) to humidity testing (Figure 9) shows about a 15% decrease in P_m after 500 hours of pressure cooker testing compared with only a 4% reduction due to 85/85 testing.

Again, as was the case in B-T testing, the E-cells (printed) show appreciably different behavior from the A-cells as can be seen from Figure 10. E-cells showed no degradation with 85/85, but rather severe degradation with pressure cooker stress. It is interesting to note that there is remarkably little spread between the best cell and the worst cell. All cells in the group seem to degrade at about the same rate.

The B-cells (vacuum deposited) showed no change when subjected to either 85/85 or pressure cooker testing. On the other hand the H-cells, which were also vacuum deposited, and the solder based I-cells typically showed a 20% to 25% drop in P_m within about 200 hours and only a very slight decrease thereafter, as shown in Figure 11. In the case of both the H- and I-cells the decease in P_m was directly correlatable with the decrease in I_{sc} and not due to an increase in series resistance. This would indicate leaching of the AR coating rather than a metallization effect. Visual inspection confirmed that this was indeed the case.

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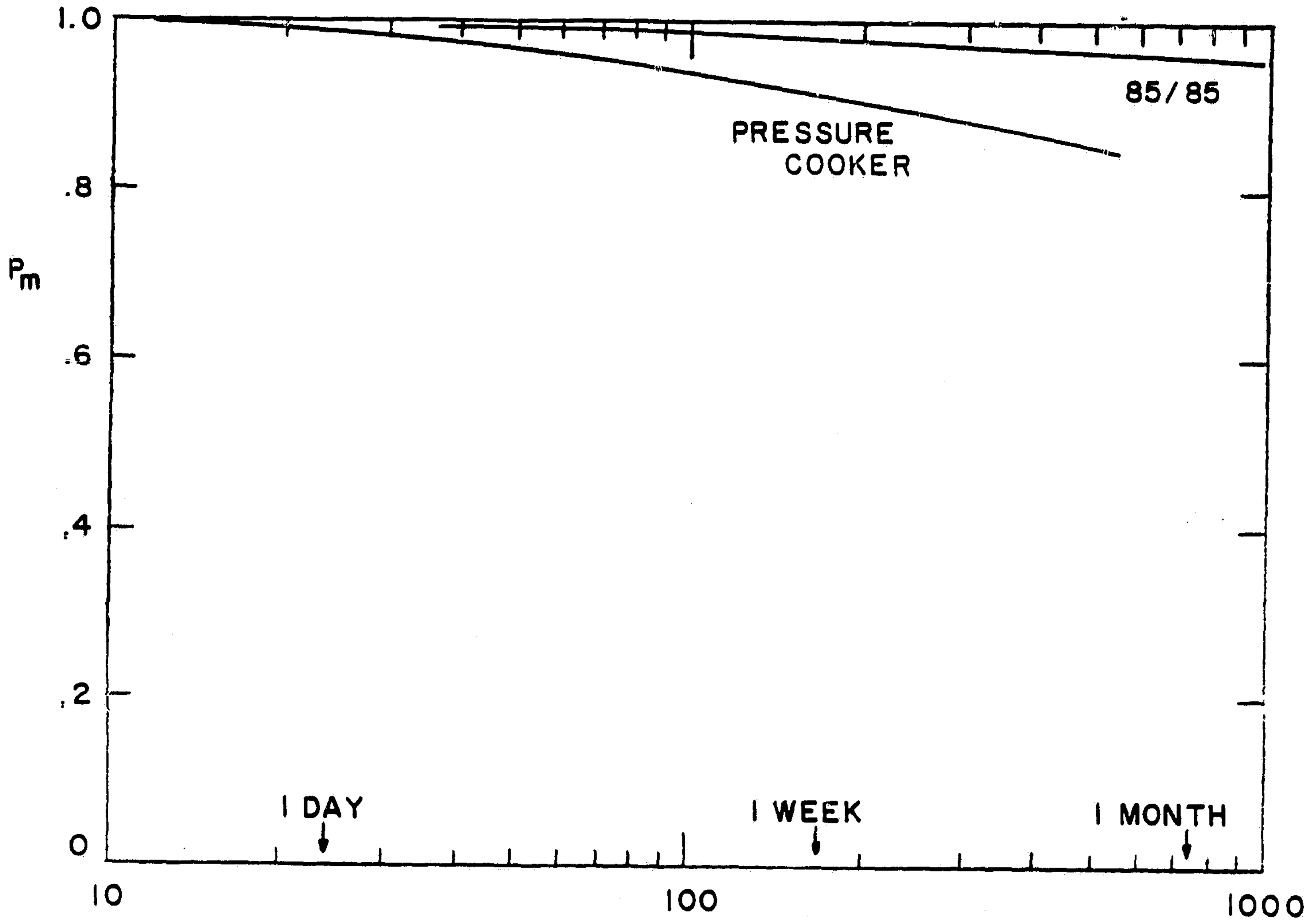

Figure 9. Average Normalized Pm as a Function of Humidity Stress for A-Cells (Au/Ni/Solder).

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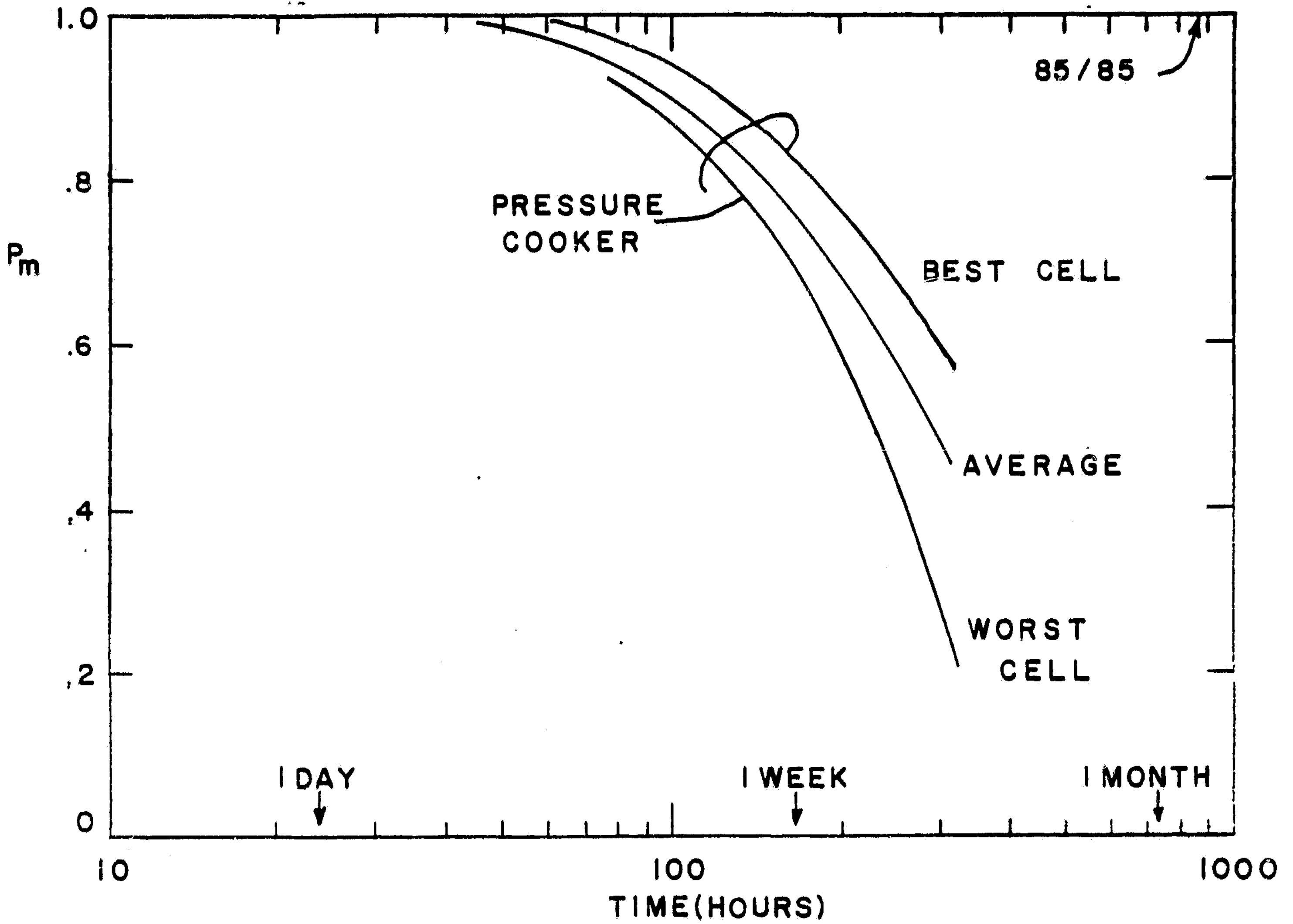

Figure 10. Average Normalized Pm as a Function of Humidity Stress Time for E-Cells (Printed Ag).

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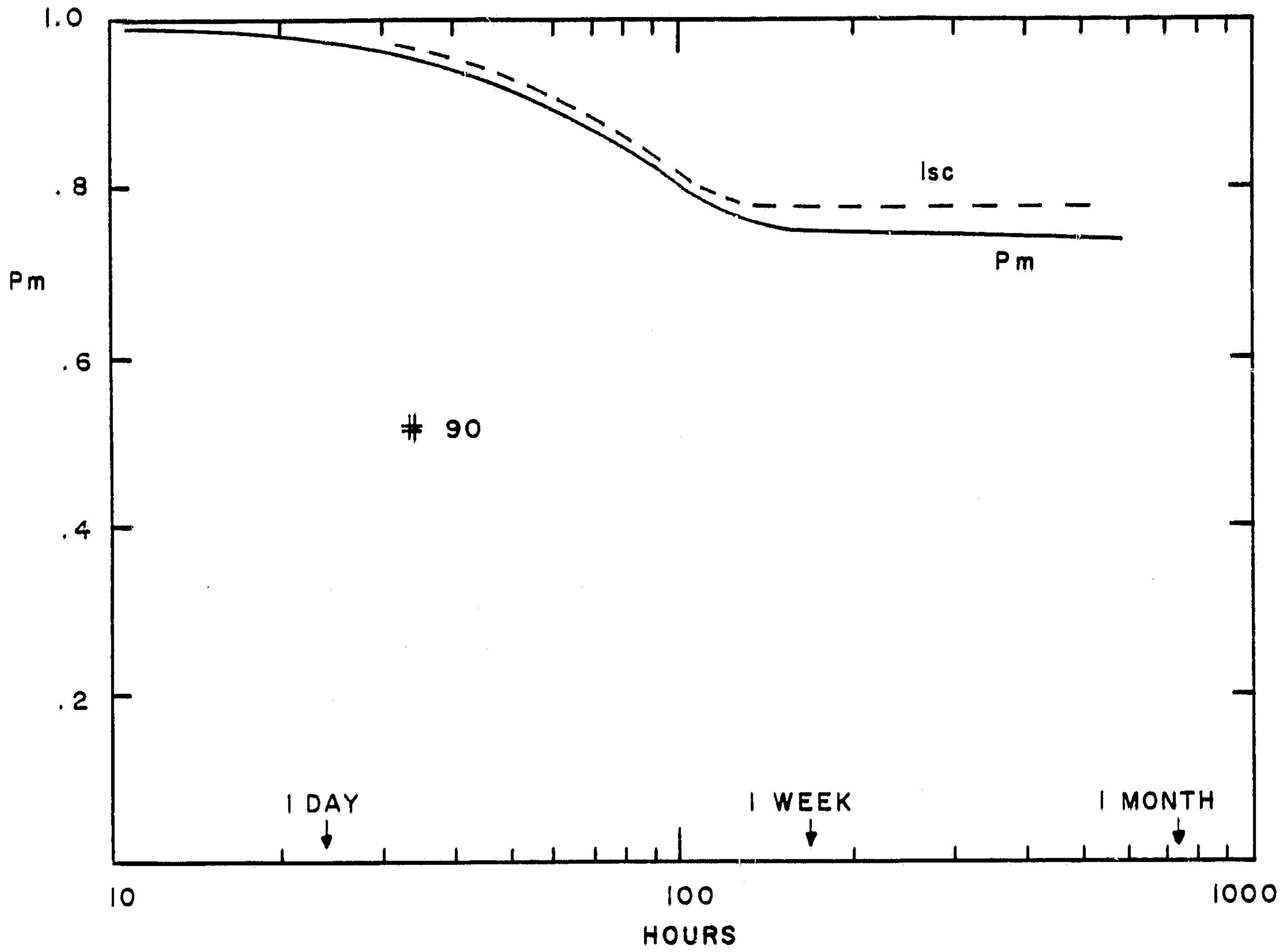

Figure 11. Normalized Pm as a Function of Pressure Cooker Stress Time for a Typical H-Cell.

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Copper plated cells subjected to humidity testing showed some moderate degradation with 85/85 testing, but disasterous degradation with pressure cooker testing. As can be seen from Figure 12, the pressure cooker degradation was roughly an order of magnitude worse than for the E-cells. The effect was so bad, in fact, that the cells became essentially unmeasurable (catastrophic failures) and the test could not run to its planned conclusion. The failure mode was a lifting of the front grid contact from the silicon, presumably due to corrosion. This will be discussed under the catastrophic failure section as well. The effect is illustrated dramatically by the distribution of Figure 13 which shows that 50% of the cells had essentially become zero power producers after only 100 hours.

It should be noted, however, that subjecting bare cells to a high humidity ambient may be different than subjecting encapsulated cells to the same environment. Since there is opportunity for trapping contaminants at the cell-encapsulant interface bare cells could show less degradation. On the other hand, the presence of an encapsulant will tend to retard the penetration of mosture and hence bare cells may show degradation sooner. In order to explore these possible differences some preliminary measurements have been made on encapsulated slices and the results are described in Section 4.0.

Thermal Cycle/Thermal Shock Testing. It was stated earlier that thermal cycle/thermal shock tests should be considered as primarily accelerating catastrophic events, rather than resulting in electrical degradation. On the other hand, when electrical performances was measured in conjunction with TC/TS testing a number of cell types showed degradation effects. As an example, Figure 14 plots average normalized P_m as a function of the number

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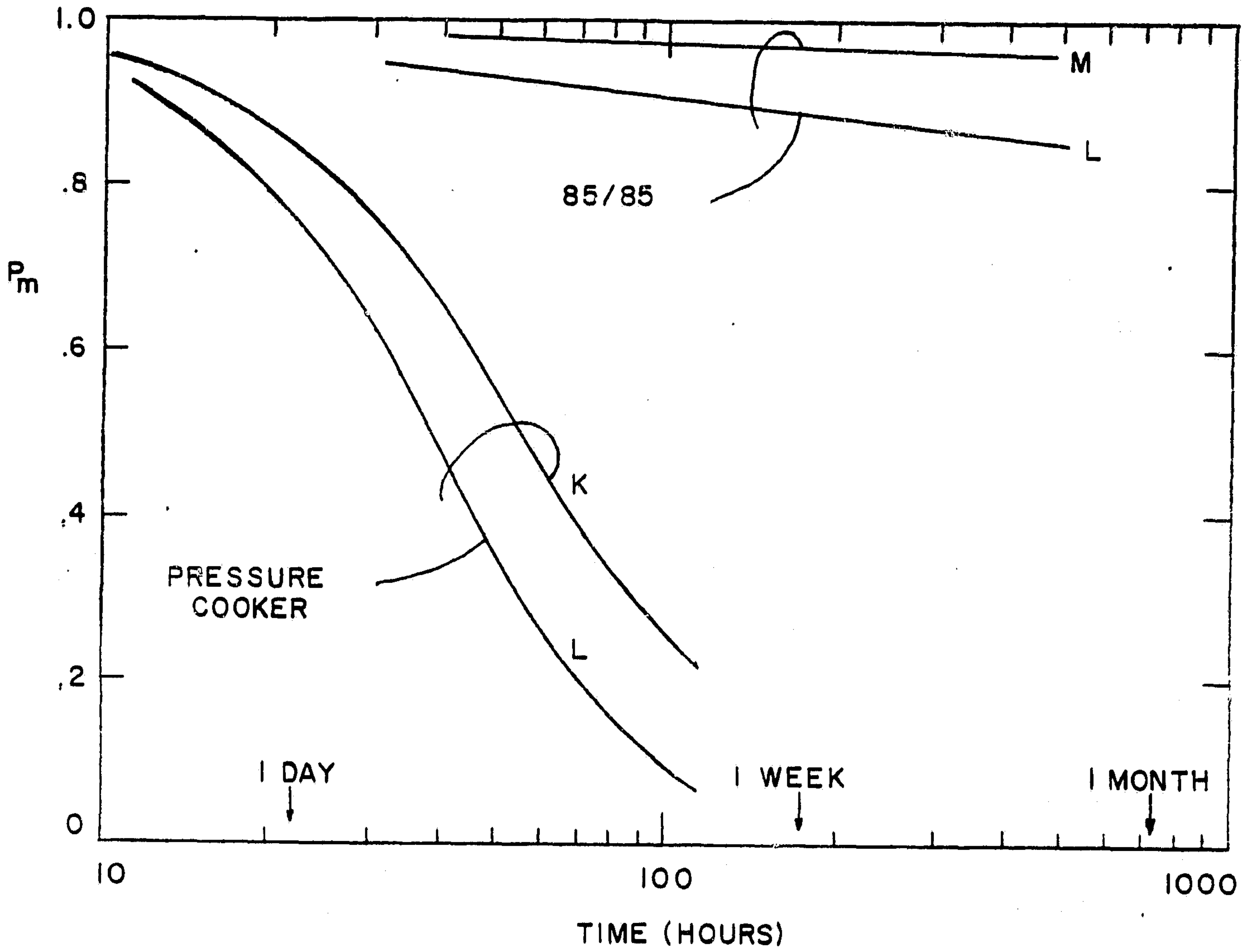

Figure 12. Average Normalized Pm as a Function of Humidity Stress Time for K, L, and M-Cells (Cu Plated).

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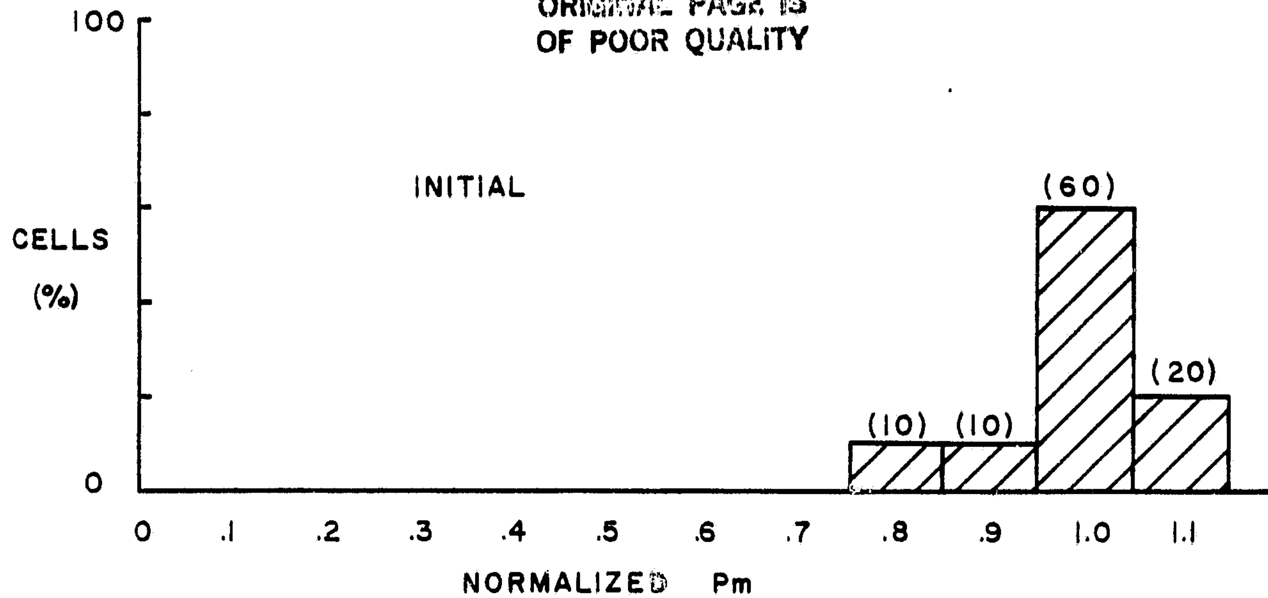

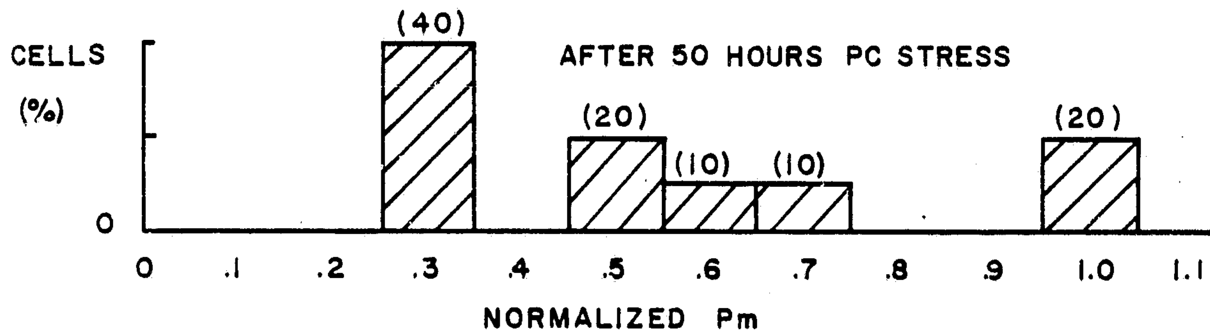

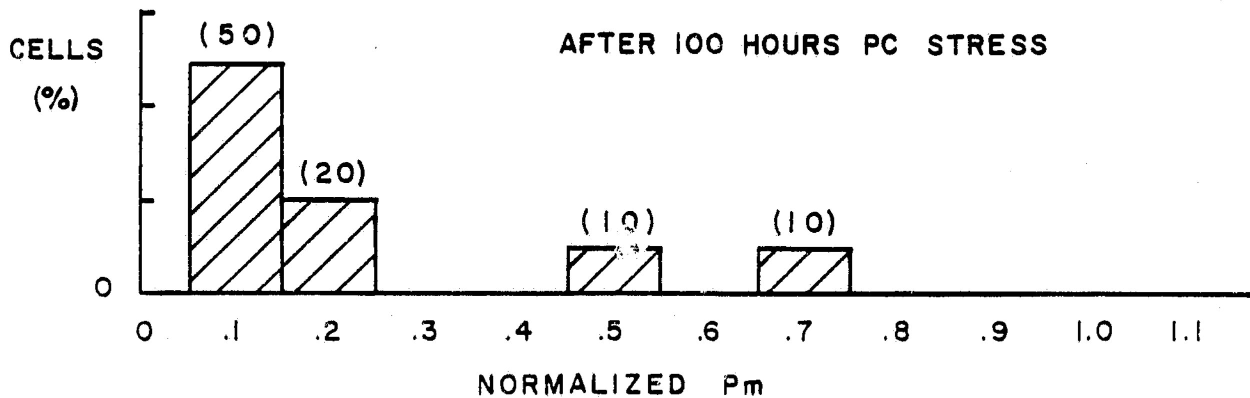

Figure 13. Change in the Pm Distribution of K-Cells as a Function of Pressure Cooker Stress.

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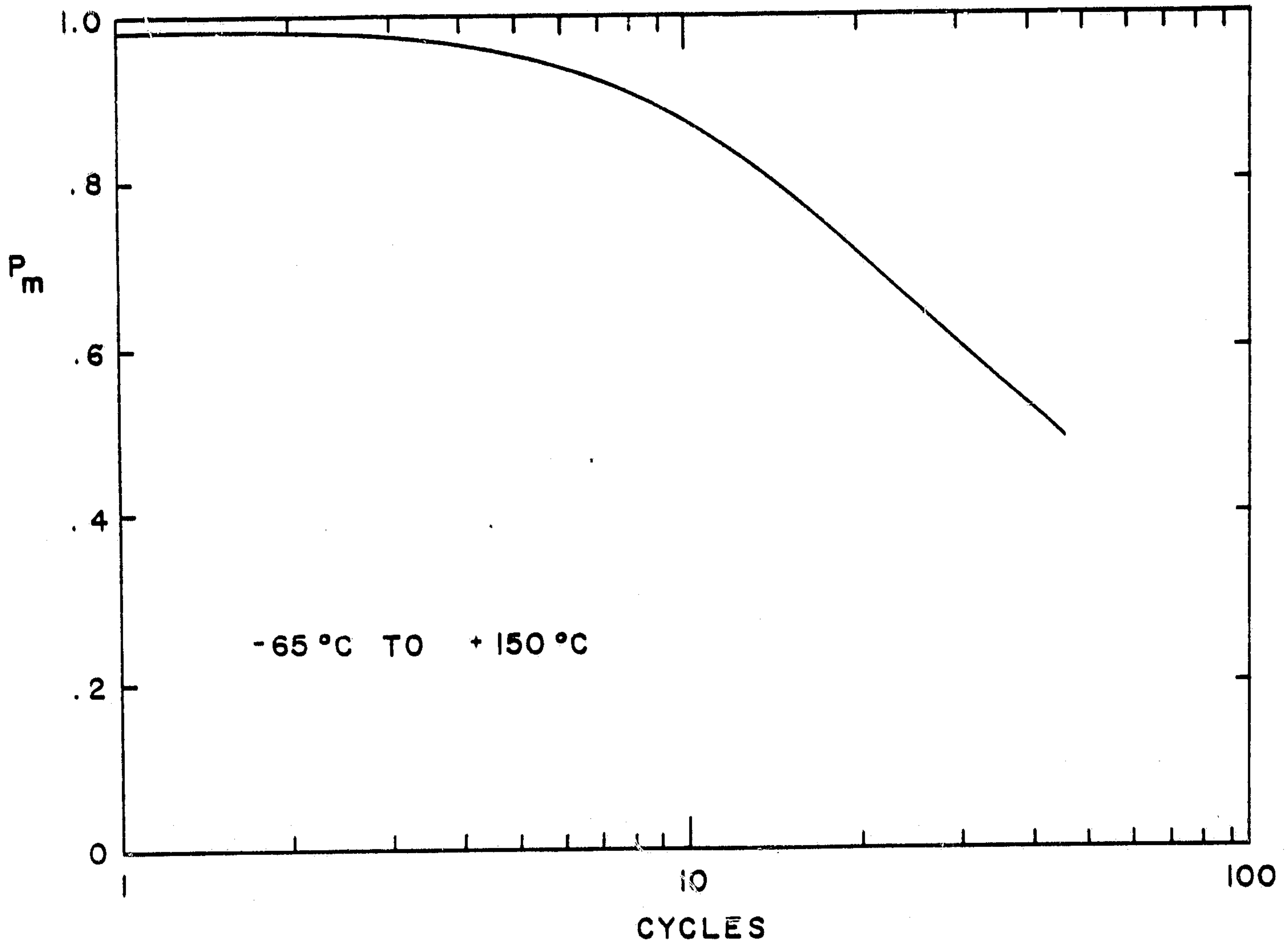

Figure 14. Normalized Pm as a Function of the Number of Thermal Cycles for I-Cells.

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of thermal cycles for a group of I-cells. The I-cell grid configuration is designed to accomodate six leads. Subjecting the cells to thermal cycling caused some of the leads to come off reducing each cell's output, but not causing catastrophic failure. Tests indicated that, depending on what geometrical pattern the removal occurred in, a cell with one or two leads attached would output approximately half its normal power while a cell with four or five leads attached would output 80% to 90% of its normal power. Figure 15 shows a plot of normalized P_m for three typical cells interpreted in terms of lead removal. It is obvious therefore that the I-cell degradation is essentially the result of "catastrophic" events which do not result in complete failure. This is consistant with the original assumptions regarding the relative failure mode effectiveness of TC/TS testing. It is felt that it is possible to interpret the test results of other cell types in an analogous fashion.

Electrical Degradation Summary. In an attempt to present a summary of the degradation effects of accelerated stress testing, Figure 16 has been prepared showing the total percentage reduction in P_m for different cells subjected to the total test schedule. For reference the length of time or number of cycles, is indicated in the parentheses.

The study increase in degradation with B-T test temperature for the A-cells is readily apparent. Cells in the same grouping, such as the C-cells, which do not have a gold barrier layer do not show this affect. The vacuum deposited and plated cells are also quite insensitive to this test. The threshold affect observed on the E-cells is not apparent in this figure because the total hours used as a common basis of comparison is not sufficient.

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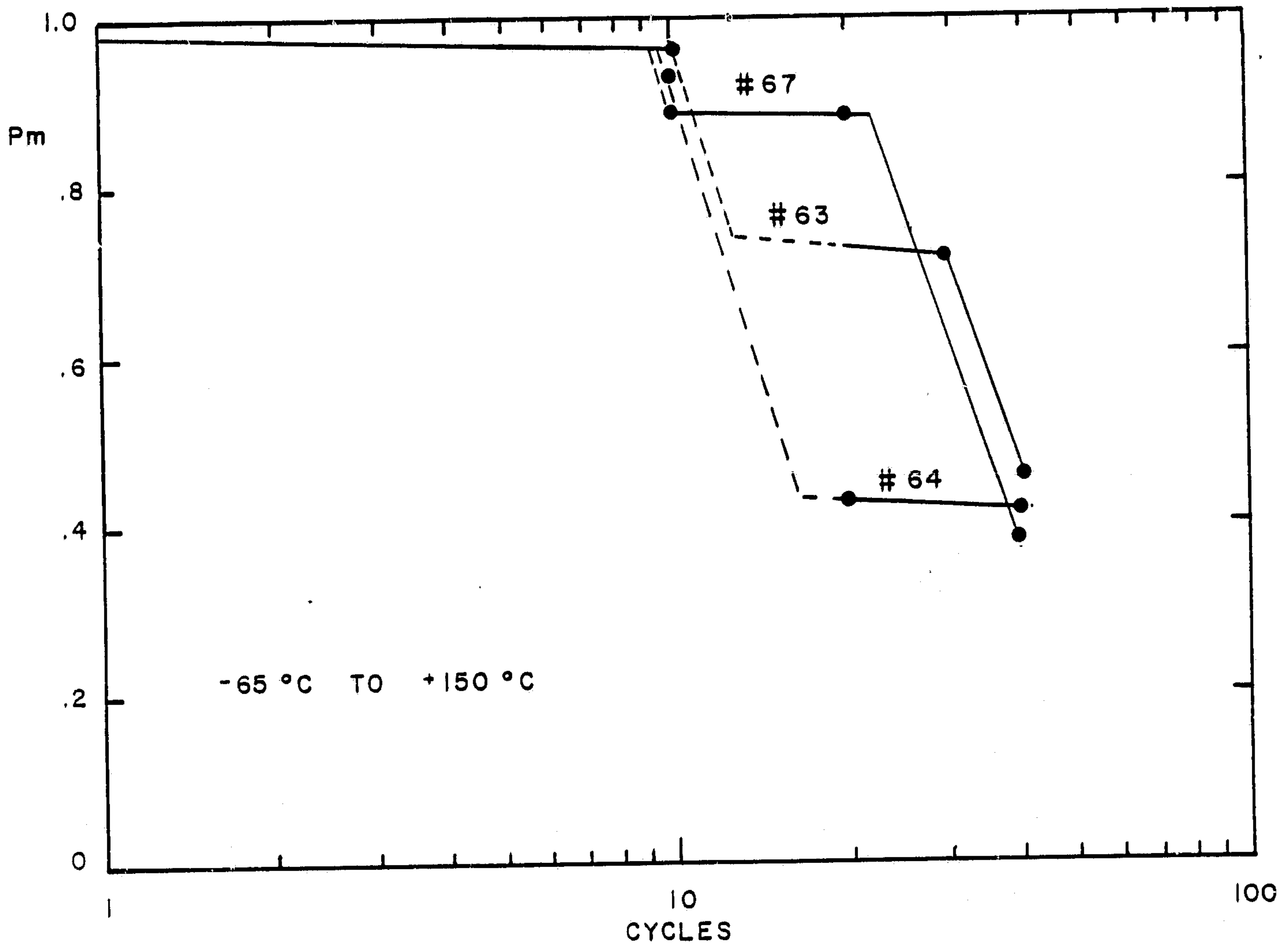

Figure 15. Normalized Pm as a Function of the Number of Thermal Cycles for Three Typical I-Cells Plotted to Show the Effect of Lead Loss.

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		SOLDER					VACUUM		PLATE			PRINT	
		A	C	F	G	I	B	H	K	L	M	E	J
BIAS TEMP	75°C (2400)								NA	NA			
	135°C (2400)									NA	NA		
	150°C (1200)										NA		
HUMIDITY	85/85 (1000)								NA				
	PC (300)								*	*	NA		
THERMAL CYCLE	(40)										NA		*
THERMAL SHOCK	(40)									NA	*		*

* ALL CELLS FAILED CATASTROPHICALLY

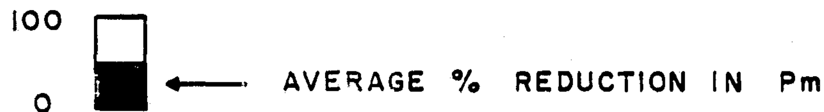

Figure 16. Degradation Failure Mode Summary

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With regard to humidity testing, all solder based cells behave very similarly showing a maximum of 10% decrease, except for the I-cells which lost their AR coating. Loss of AR coating was also observed with the H-cells. The severe degradation of the copper plated cells is indicated although it was not possible to carry the test to the full 300 hours. The moderately severe degradation of the printed cells is apparent. Although the cause is unknown, because both cells in this catagory showed similar effects it is felt that the observed effect is related to the silver screened metallization system used.

As was discussed, thermal cycle/thermal shock testing primarily results in such effects as lead removal which can best be discussed under the catastrophic effects section.

It would appear, in light of the C-cell and the B-cell results, that highly reliable cells are possibly using either solder or vacuum deposited metallization.

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3.2 Accelerated Test Results--Catastrophic Changes

As mentioned earlier, observed physical changes after testing were classified as either 0, 1, or 2 with 2 being sufficiently severe to prevent acquiring meaningful electrical data. The percentage of catagory 2 changes (hereafter referred to as catastrophic changes) which occured after each cell type had been exposed to a full schedule of thermal cycle, thermal shock, and pressure cooker testing is plotted in Figure 17. It can be quickly seen that problems exist with regard to some cells in all four metallization catagories: solder (I), vacuum (H), plated (K,L,M), and printed (E,J). In order to understand what is really happening to each cell type it is necessary to analyze the data further in terms of specific failure modes. Four basic catastrophic failure modes were identified: cracked cell, open lead (metal-silicon), open lead (metal-metal), and open lead (silicon-silicon). The three open lead categories need some explanation. All cases refer to attachment of the metal tab to the cell metallization. Open lead (metal-silicon) occurs when the tab comes off leaving bare, undisturbed silicon exposed. Open lead (metal-metal) occurs when the tab comes off, but the underlying metallization remains attached to the silicon. Open lead (silicon-silicon) occurs when the tab comes off taking with it some of the silicon substrate and leaving a crater behind. Examples of these three failure modes are shown in Figure 18. It should be noted that in all cases the tabs were removed with zero force, i.e., the tabs were not intentionally pulled--they just "fell off".

Figure 19 summarizes the frequency of the observed catastrophic failures in terms of the four failure modes. The height of the black bar represent the fraction of the total cells tested which exhibited catastrophic failure. It is not necessary that the sum of the failure modes for a given stress test add

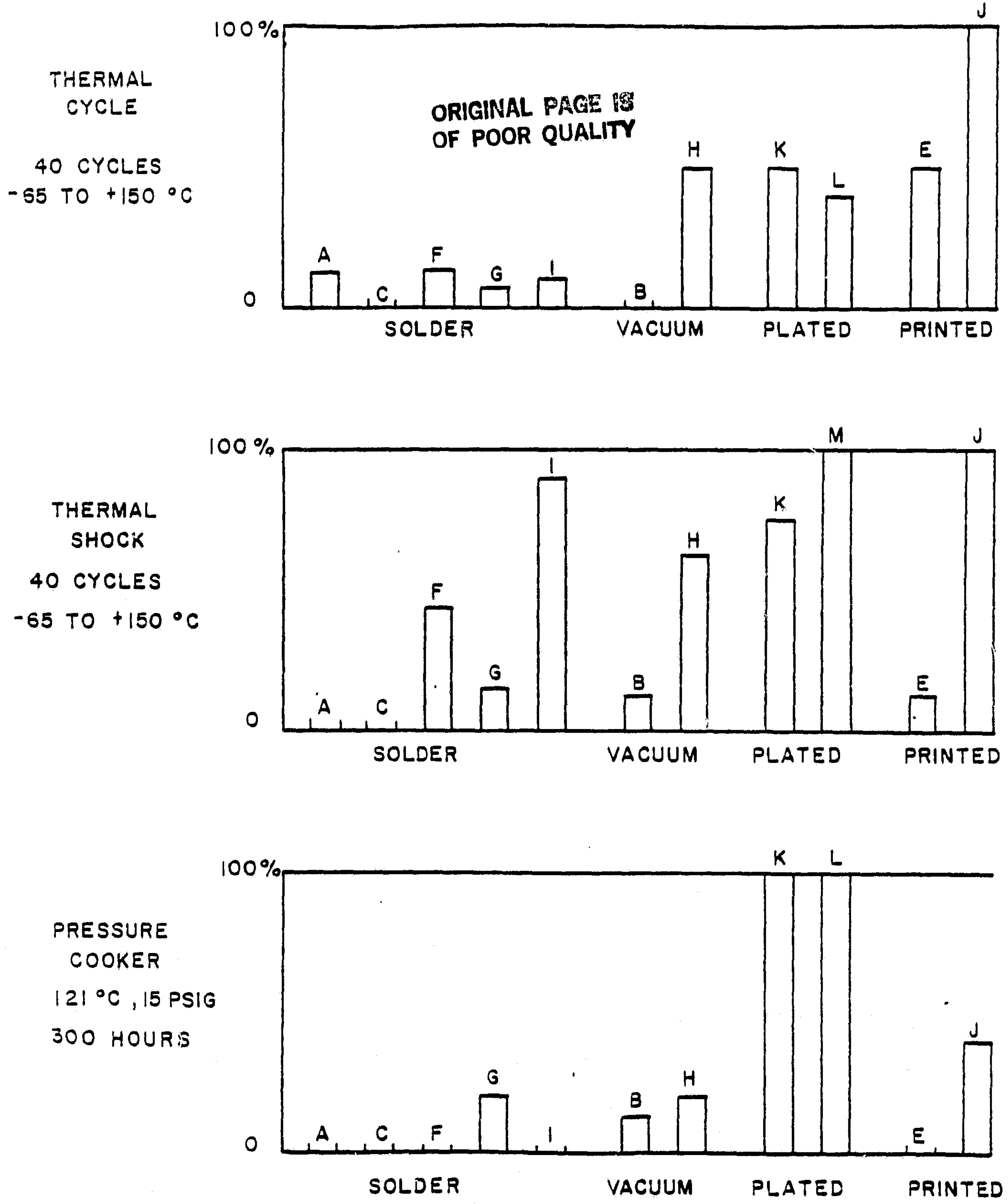
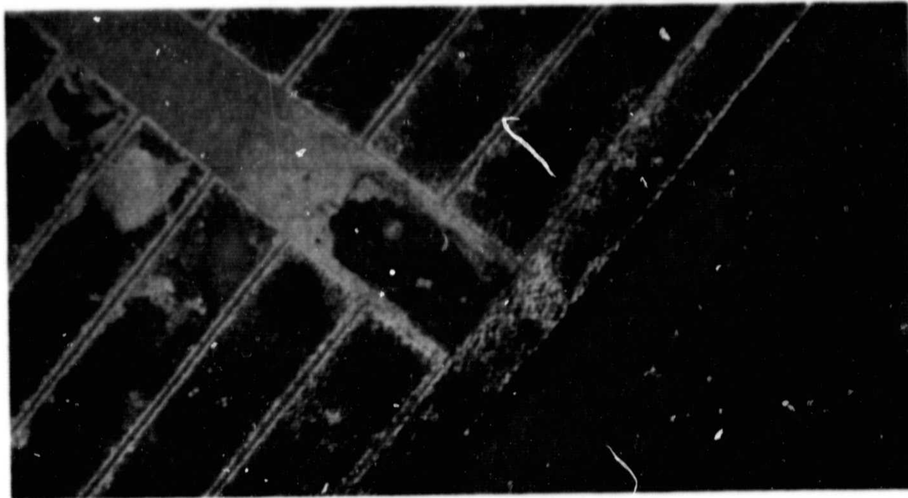
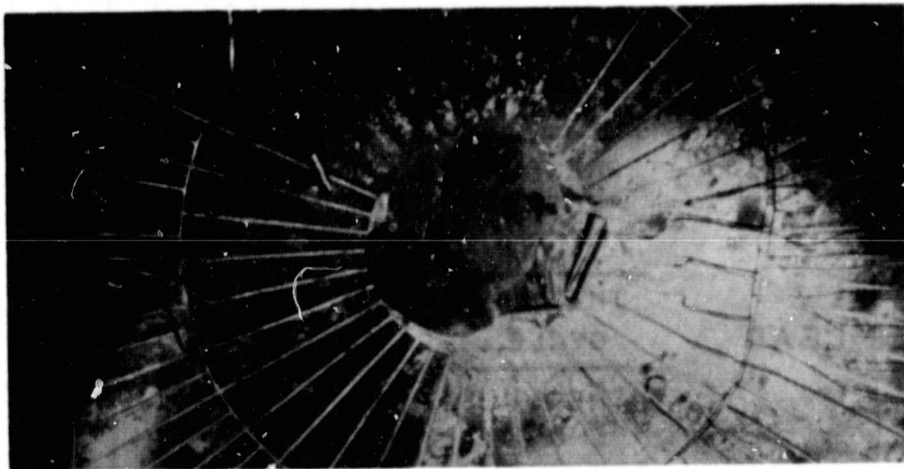


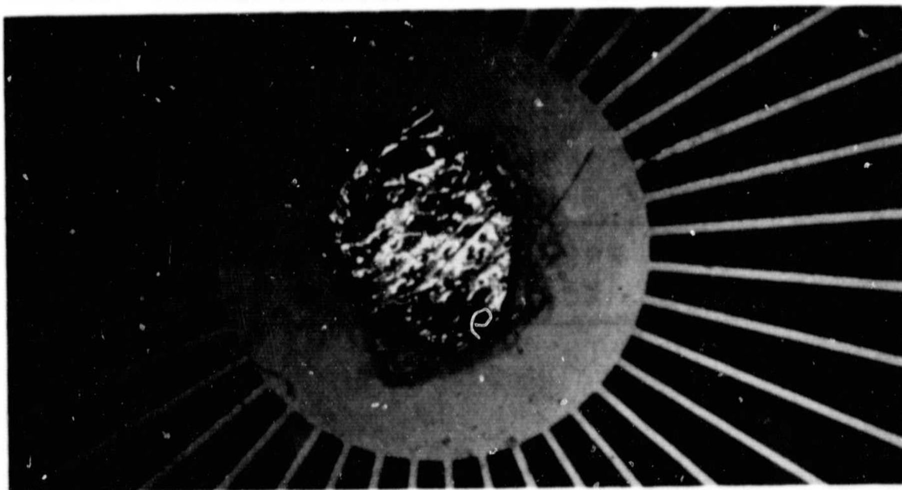
Figure 17. Gross Failure Rates for Catastrophic Tests.



a) OPEN LEAD (METAL-METAL)



b) OPEN LEAD (METAL-SILICON)



c) OPEN LEAD (SILICON-SILICON)

Figure 18. Photographic Examples of Catastrophic Failure Modes.

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		SOLDER					VACUUM		PLATE			PRINT	
		A	C	F	G	I	B	H	K	L	M	E	J
CRACKED CELL	THERMAL CYCLE										NA		
	THERMAL SHOCK									NA			
	PRESSURE COOKER										NA		
OPEN LEAD METAL-SILICON	THERMAL CYCLE				NA						NA		
	THERMAL SHOCK				NA					NA			
	PRESSURE COOKER				NA						NA		
OPEN LEAD METAL-METAL	THERMAL CYCLE				NA						NA		
	THERMAL SHOCK				NA					NA			
	PRESSURE COOKER				NA						NA		
OPEN LEAD SILICON-SILICON	THERMAL CYCLE				NA						NA		
	THERMAL SHOCK				NA					NA			
	PRESSURE COOKER				NA						NA		

KEY: ← % CATASTROPHIC FAILURE

Figure 19. Catastrophic Failure Mode Summary

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to 100% since it is possible to have two failure modes, such as cracked cell and open lead, simultaneously. Among the solder metallized cells the C-cell showed no catastrophic failures. It should be pointed out that this cell was only 2 inches in diameter and relatively thick, giving greater resistance to cracking. The A-cell, which with a diameter of 4 inches was the largest cell, also showed a remarkable resistance to catastrophic failure, but it was also the thickest. Among this category only the F-cell exhibited the metal-metal falure mode and this occurred on thermal shock. Because of the ease with which soldered connection can be made, one would expect few metal-metal failures to occur in solder metallized cells or in copper plated cells and this is what was observed. The I-cells showed an abnormally high incidence of open lead (silicon-silicon). Since no other solder cell type showed this type of failure it is attributed to some factor associated with that particular design or manufacture, such as tab material composition or stress introduced during tab attachment.

Cells with vacuum deposited metallization appear quite insensitive to catastrophic failure except for the abnormally high incidence of metal-metal failures exhibited by H-cells. As has been discussed, soldering to silver metallization is relatively difficult because of such factors as silver leaching, and it is apparent that this manufacturer had not adequately mastered the technique. Because the B-cell did not exhibit this failure mode, however, it should not be considered indigeneous to this type of construction.

The copper plated cells exhibited the greatest fraction of catastrophic failures of any metallization. The high fraction of cracked cells in perhaps significant in view of the fact that the N-cell was only 2 inches in diameter

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and should have been more resistant. Furthermore, this cracking appears induced by thermal stresses rather than handling since it was not observed during pressure cooker stress. The truly significant result for this construction category, however, was the large number of metal-silicon failures observed during pressure cooker testing. This has been discussed to some extent in the section on electrical degradation. Figure 20 illustrates this type of metal-silicon failure on a K-cell. Copper plated cells are the only type which exhibit this failure model. A certain amount of silicon fracturing under the tabs was also observed on K-cells, but not on the M-cells.

Of the printed cells, the E-cell behaved quite well except for excessive silicon-silicon fracturing during thermal cycle. The J-cell, on the other hand, showed additional cell cracking, serious metal-metal separation problems, and severe silicon-silicon fracturing. As was the case for the vacuum deposited cells, one manufacturer appears to have lead soldering under control while the other does not. The silcon-silicon fracturing problem on thermal cycle may be a problem associated with the thermal expansion properties of the frit since it is common to both types. The J-cells, however, showed proportionately greater open circuit fracturing and cell cracking.

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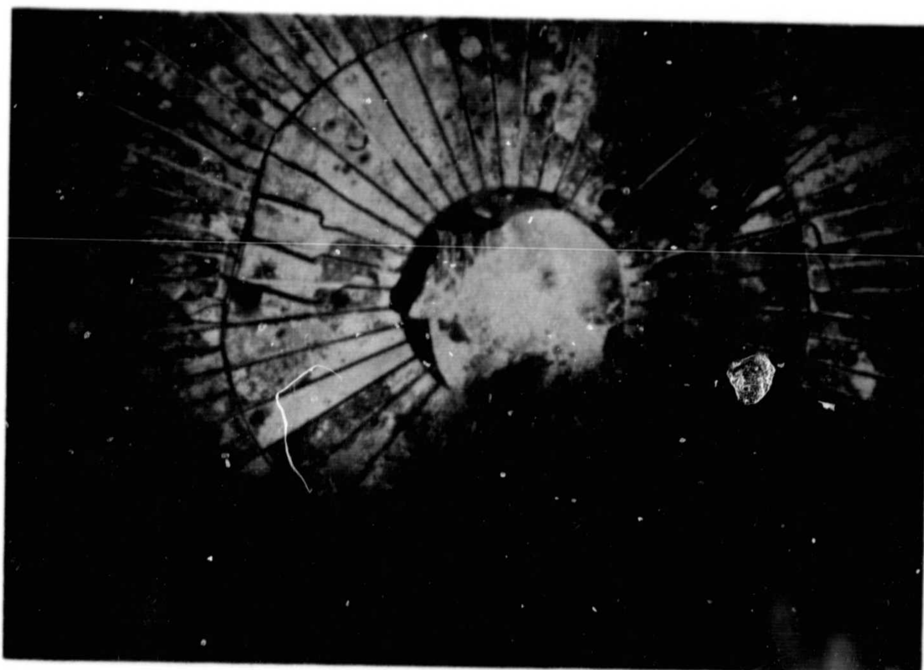

Figure 20. Photograph of Metal-Silicon Catastrophic Failure in Copper-Plated K-Cell.

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4.0 EXPERIMENTS TO INVESTIGATE APPROACHES TO ENCAPSULATED CELL TESTING

While the major emphasis in the program has been on unencapsulated cells, it would be of considerable interest to be able to relate the unencapsulated test results to the behavior of cells in the encapsulated environment of the module. In order to explore this possibility in the laboratory a number of square minimodules containing a single 3 1/2 inch diameter encapsulated cell was fabricated by Springborn Laboratories, and these minimodules, along with unencapsulated control cells, were subjected to a series of accelerated tests. The minimodules consisted of two types: glass superstrate and masonite substrate. Construction details are shown roughly to scale in Figure 21. No edge protection was provided for the minimodules in contrast to full scale modules. For ease of notation the minimodules are referred to in a shorthand fashion as either glass or plastic, according to the front surface material. The photovoltaic cells which were used were the same in both cases: solder based cells very similar, except for size, to the A-cell discussed previously. The minimodules and their unencapsulated controls were subjected to the abbreviated test schedule shown in Figure 22. Both types of modules and the unencapsulated control cells were simultaneously stressed in the same environment chamber. The quantities in each test were small: 3 of each minimodule type plus 6 unencapsulated controls, except for the 75°C B-T test which had 5 of each minimodule type plus 10 controls. Consequently the results, while useful in ascertaining general trends, are of questionable statistical significance. No category 2 catastrophic changes in either the minimodules or the unencapsulated controls were observed as a result of the tests, so results are entirely in terms of electrical degradation and associated visual observation.

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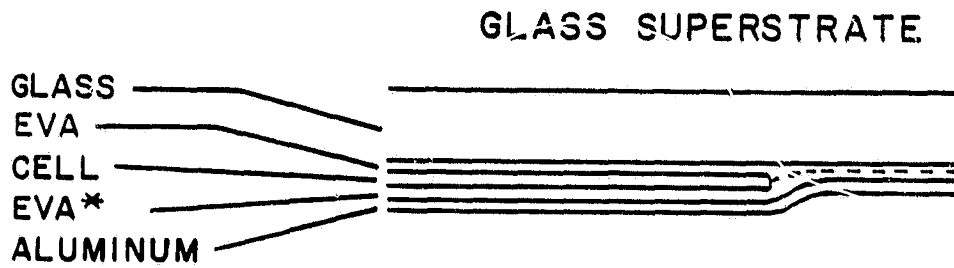

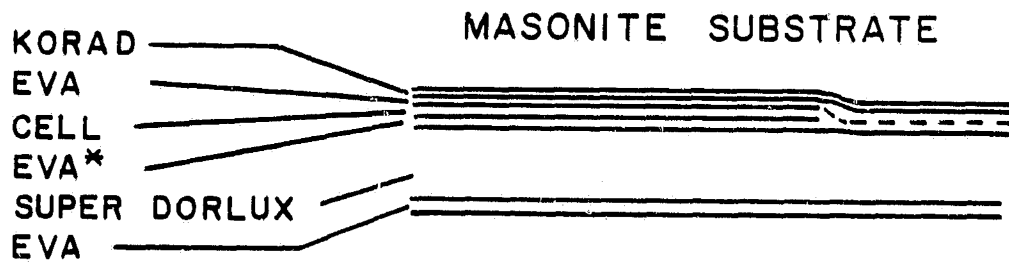

* EVA WITH GLASSMAT AND WHITE PIGMENT

Figure 21. Detail of Minimodule Construction

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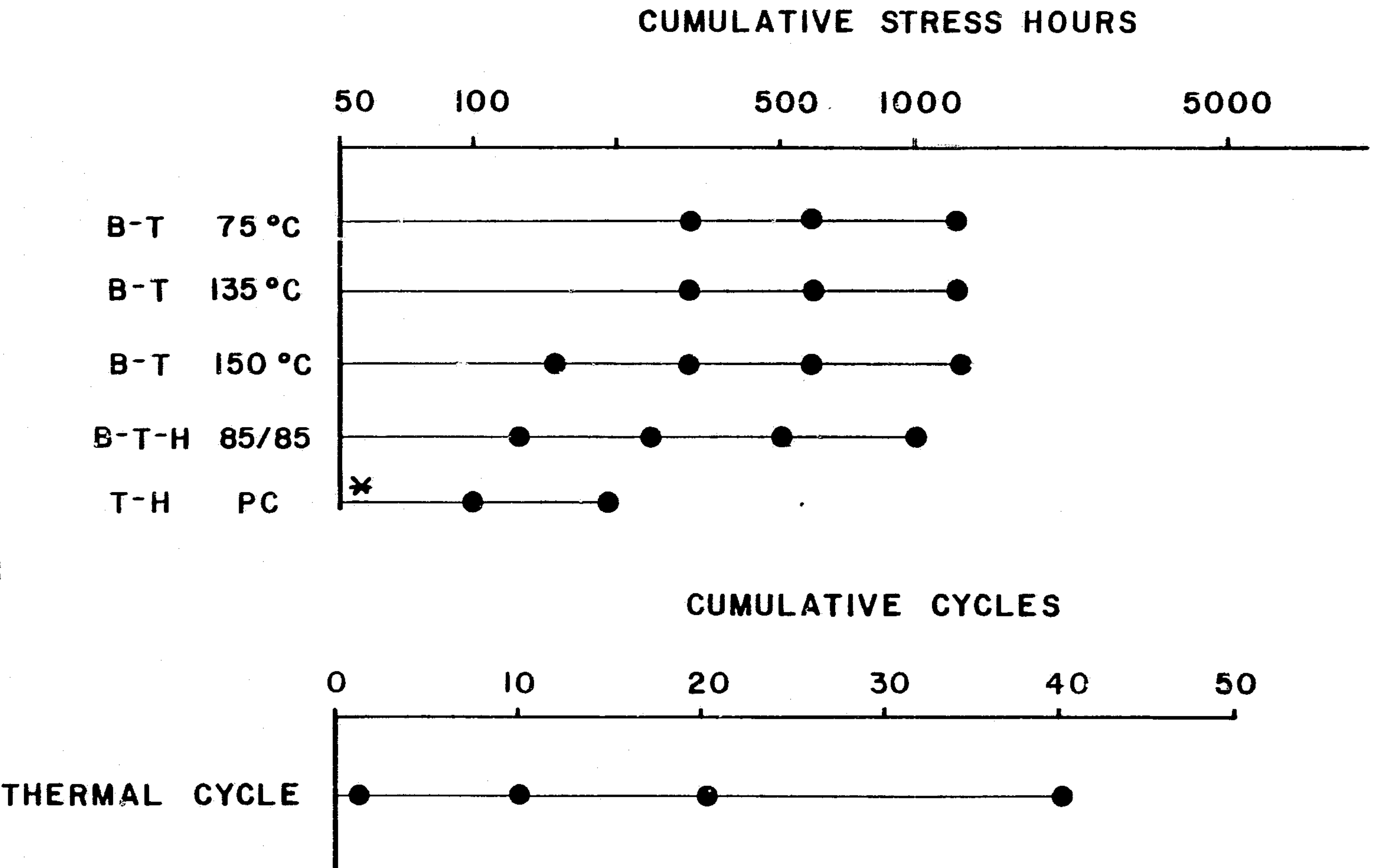

Figure 22. Accelerated Test Schedule used for Encapsulated Minimodules, Showing Points at which Electrical Measurement and Visual Inspection are made.

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4.1 B-T Test Results

Essentially no electrical degradation was observed on the encapsulated cells during 75°C B-T Testing. Aside from a slight melting of the Korad on the plastic modules at 600 hours no physical changes were noted either.

Higher temperatures, however, resulted in significant physical changes. The glass modules experienced delamination after 150 hours at 150°C and after 300 hours at 135°C. Figure 23 shows an example of the typical delamination observed. The encapsulation material began to turn light brown during this time and became more promounced with subsequent stress periods. The plastic modules also began to darken. After 1200 hours at 150°C the plastic module encapsulation was so badly charred that the light actually reaching the cell had to be greatly attenuated. The initially soft, pliable plastic modules became thinner and more rigid with stressing. Unfortunately no record was made of the weight or thickness before and after stressing so this effect was not quantified. The unencapsulated cells, on the other hand, showed essentially no physical change when subjected to the same stresses.

Each of the module types, as well as the controls, exhibited considerable electrical degradation as shown in Figures 24 and 25. Because of the small number of cells (3) in each test the relative shape of each curve is more important than its specific position. The unencapsulated controls show the same sort of gradual degradation with time found for the A-cells which was attributed to a diffusion phenomenon. The glass modules appear to exhibit the same sort of behavior, while the plastic modules show a faster rate of degradation at the longer stress times. It would appear that in addition to increased series resistance as a result of metallization diffusion, the observed charrring of the encapsulant was physically obstructing light to the cell and reducing the short circuit current. This can be seen clearly when I_{sc} is

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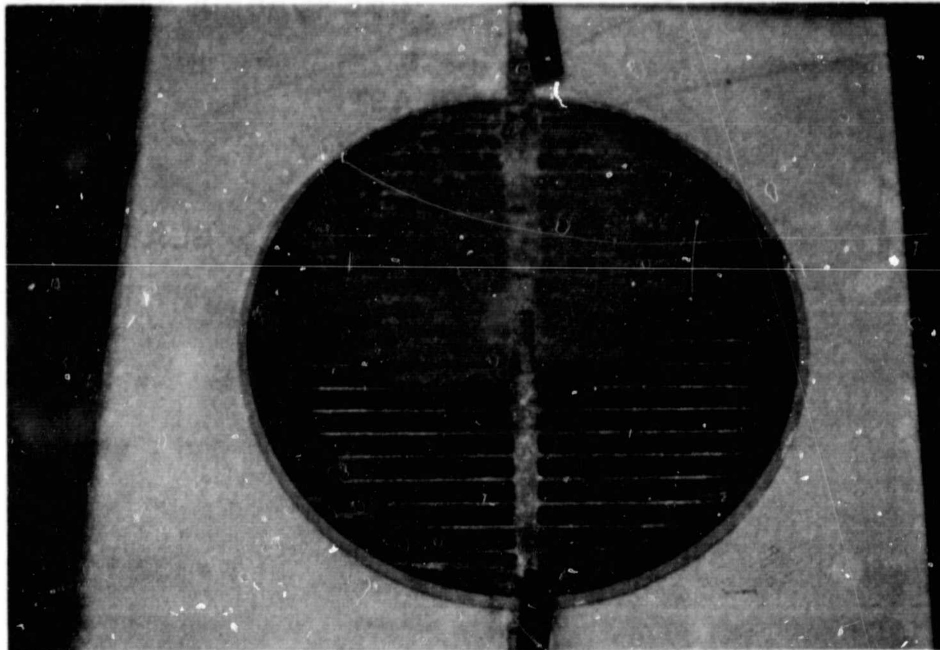

Figure 23. Photograph of Delamination Observed in Glass Superstrate Minimodule as a result of B-T Testing.

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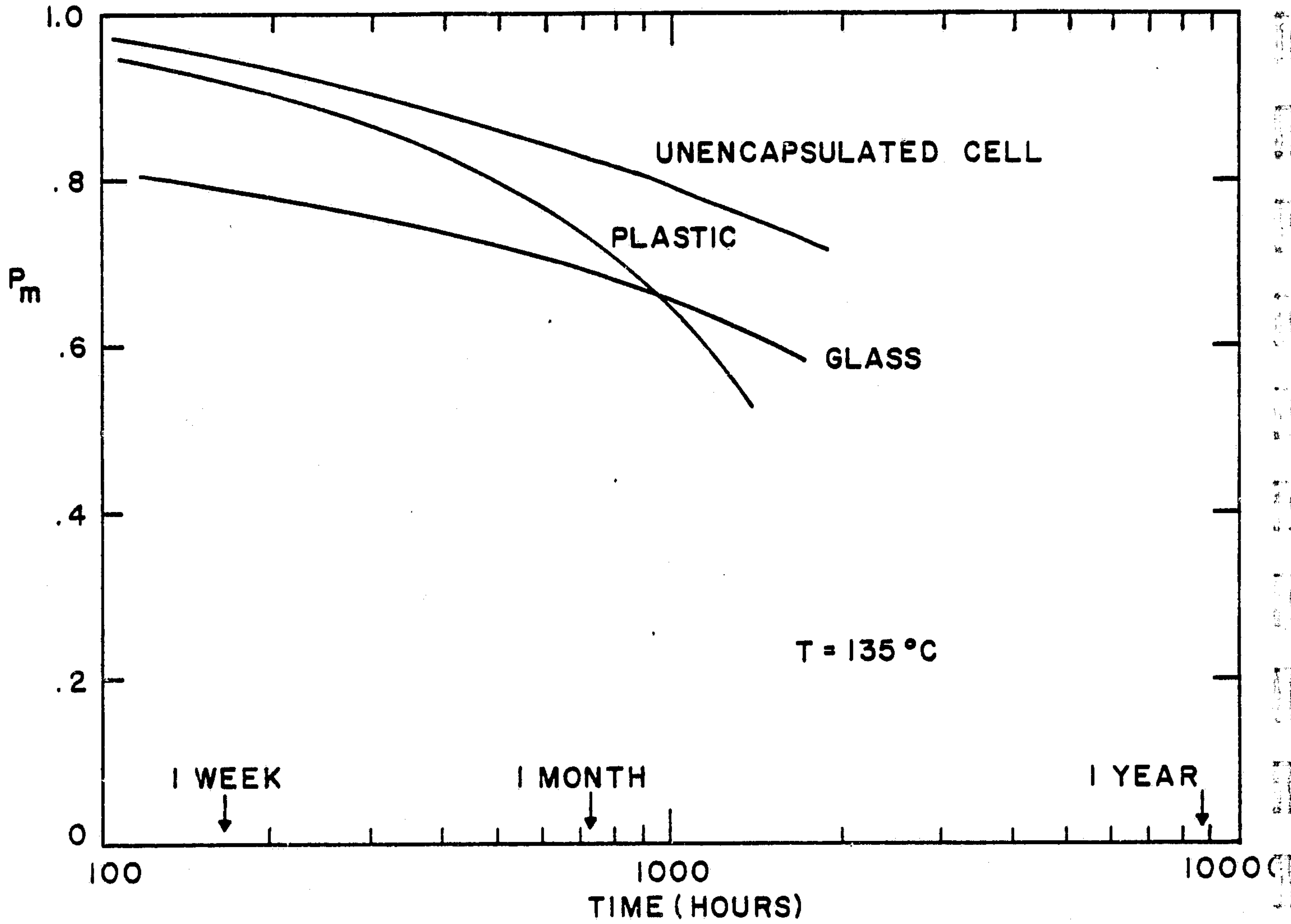

Figure 24. Average Normalized Pm as a Fuction of B-T Stress Time at 135°C for Minimodules and Control Cells.

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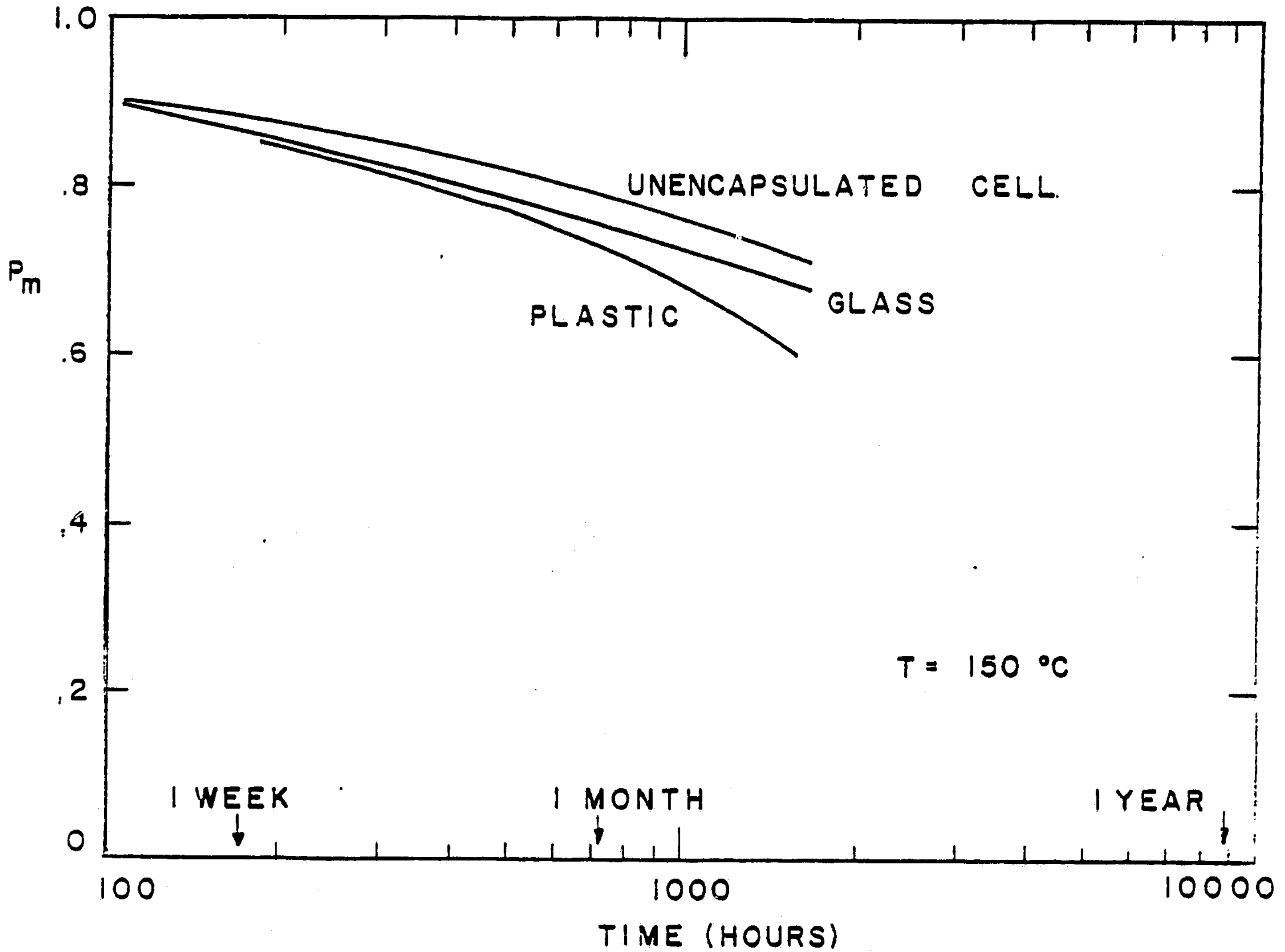

Figure 25. Average Normalized Pm as a Function of 150°C B-T Stress Time for Minimodules

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plotted vs test time as in Figure 26. Charring of the encapsulant material is a chemical process which should have a threshold rather than exhibit Arrhenius behavior. Therefore it is not logical to expect to accelerate this phenomenon. In other words, instead of only seeing the effect of accelerated use conditioning failure modes, the high temperature tests were introducing a new failure mode--one which did not occur under use conditions.

4.2 Humidity Test Results

The 85/85 stress left water spots on the glass encapsulated cells during the first 125 hours and the aluminum backing showed signs of peeling away during the first 250 hours. These effects did not appear to worsen with further testing and are considered minor. The plastic encapsulated cells, on the other hand, became thin and rigid with a dark tan color after only 125 hours of stress. These effects became more pronounced with further testing. The unencapsulated controls displayed essentially no visual change. In some contradiction to the visual changes, the glass minimodules showed twice the electrical degradation of the plastic minimodules or the unencapsulated cells as shown in Figure 27. An increase in series resistance rather than a decrease in I_{sc} was observed in all cases indicating that darkening was not a factor. No explanation can be given for the anamalous results at this time.

Pressure cooker testing proved to be more damaging than 85/85 testing. The glass encapsulated minimodules showed water spots and a light green tinted surface after 25 hours. After 50 hours some delamination occurred and the backs became wrinkled. At 200 hours the backs were seperating from the glass. After 500 hours water had seeped into the modules and caused obvious corrosion at the edge of the cell. The plastic modules displayed numerous air bubbles, water deposits, and rough surfaces after 25 hours. A significant thinning of

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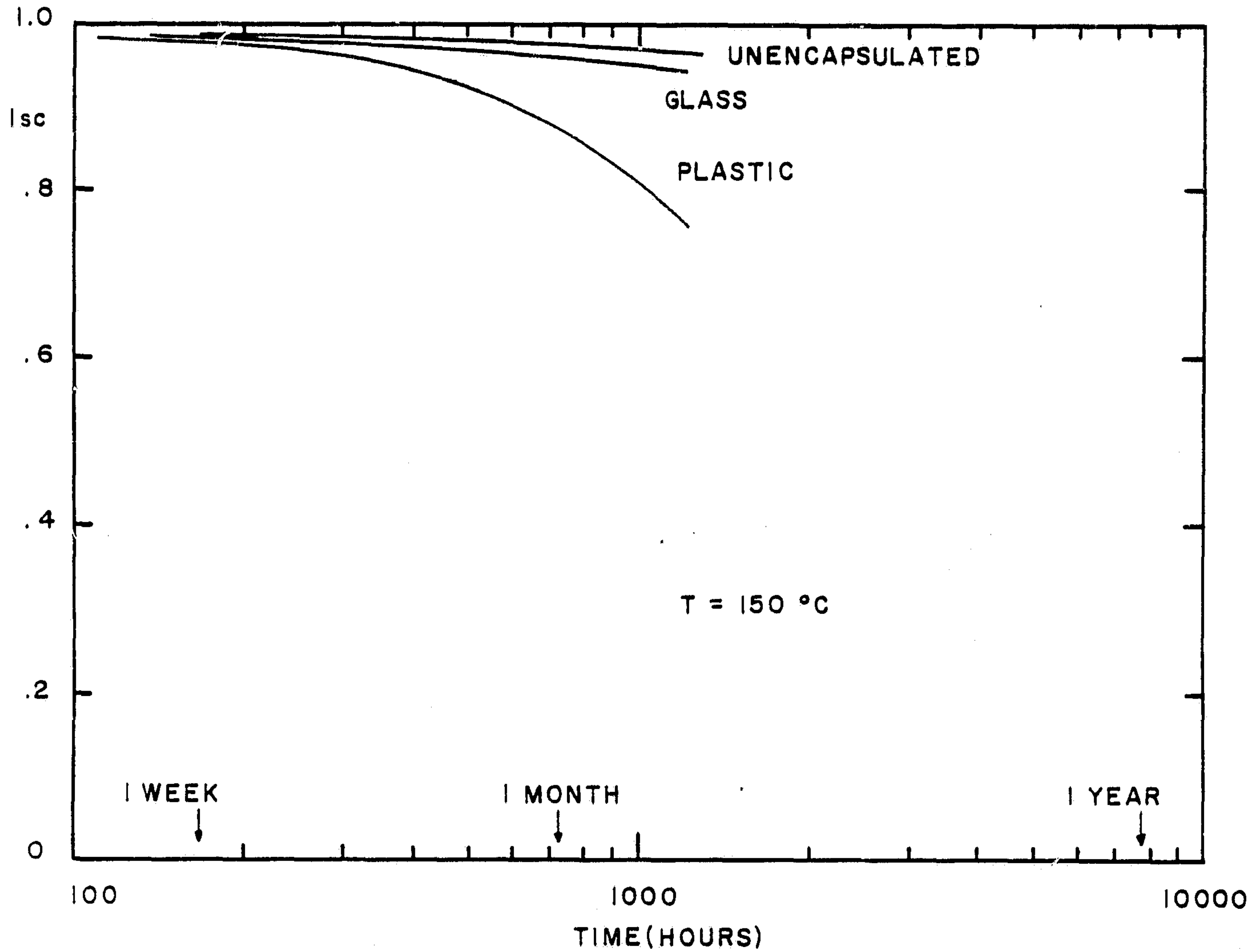

Figure 26. Average normalized Isc as a Function of B-T Stress Time at 150°C for Minimodules and Controls.

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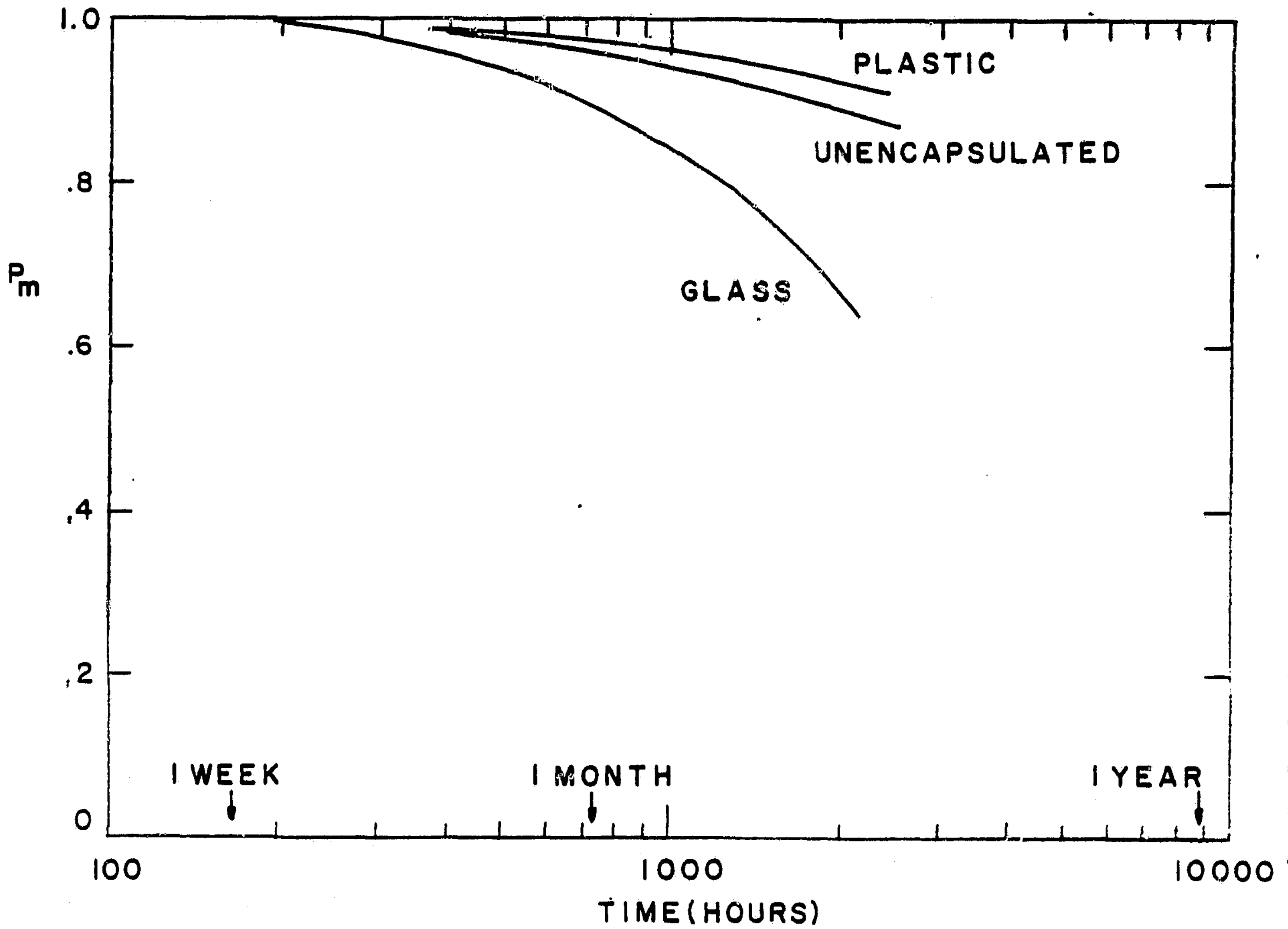

Figure 27. Average Normalized Pm as a Function of 85°C/85%RH Stress Time for Minimodules and Controls.

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the plastic modules was observed after 50 hours. At the end of 200 hours the plastic modules contained a white cloudy substance within the plastic encapsulation as shown in Figure 28. Interestingly enough, this material vanished after 500 hours leaving only a few spots. Electrically all modules and their controls seemed to degrade at about the same rate as shown in Figure 29. No abnormal electrical effects were noted.

4.3 Thermal Cycle Testing

Thermal cycle testing caused some wrinkling of the plastic module surfaces and a thinning of the backs. No significant changes were observed on the glass minimodules or the unencapsulated controls. Electrically only the plastic minimodules exhibited degradation, as shown in Figure 30.

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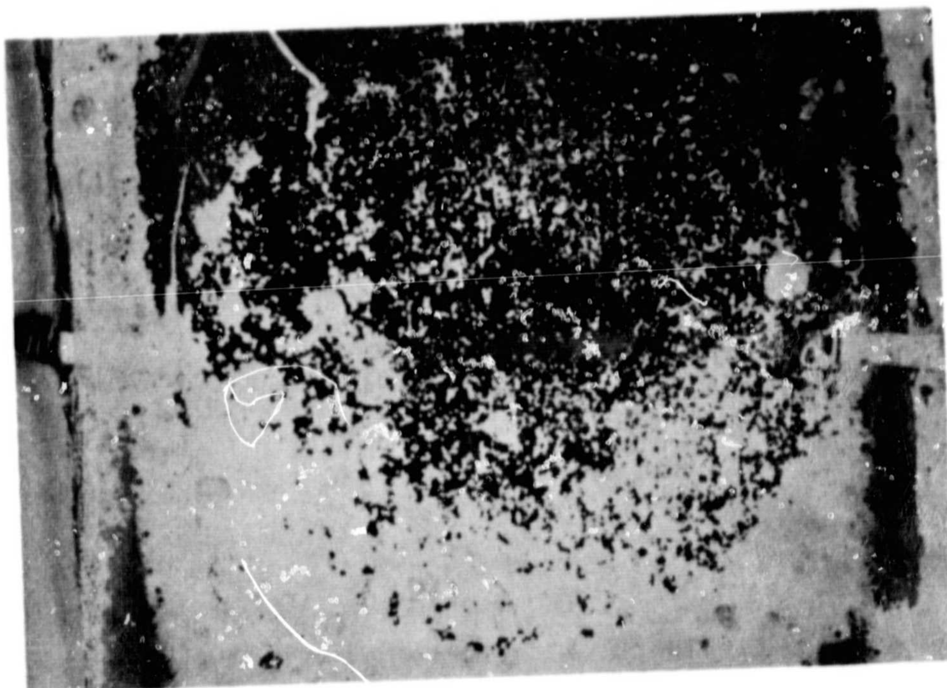

Figure 28. Photograph of Plastic Minimodule after 200 Hours Pressure Cooker Stressing.

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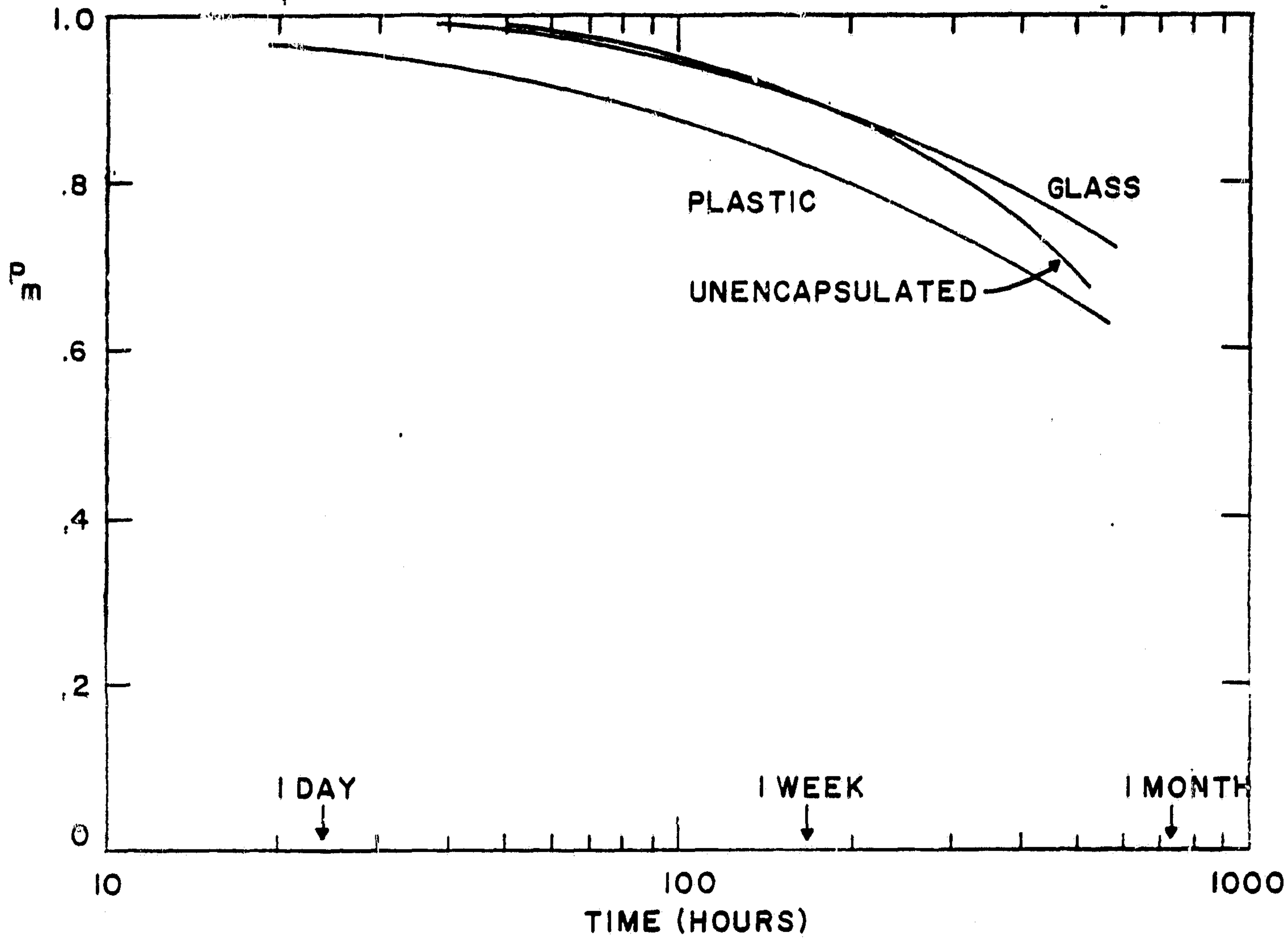

Figure 29. Average Normalized Pm as a Function of Pressure Cooker Stress Time for Minimodules and Controls.

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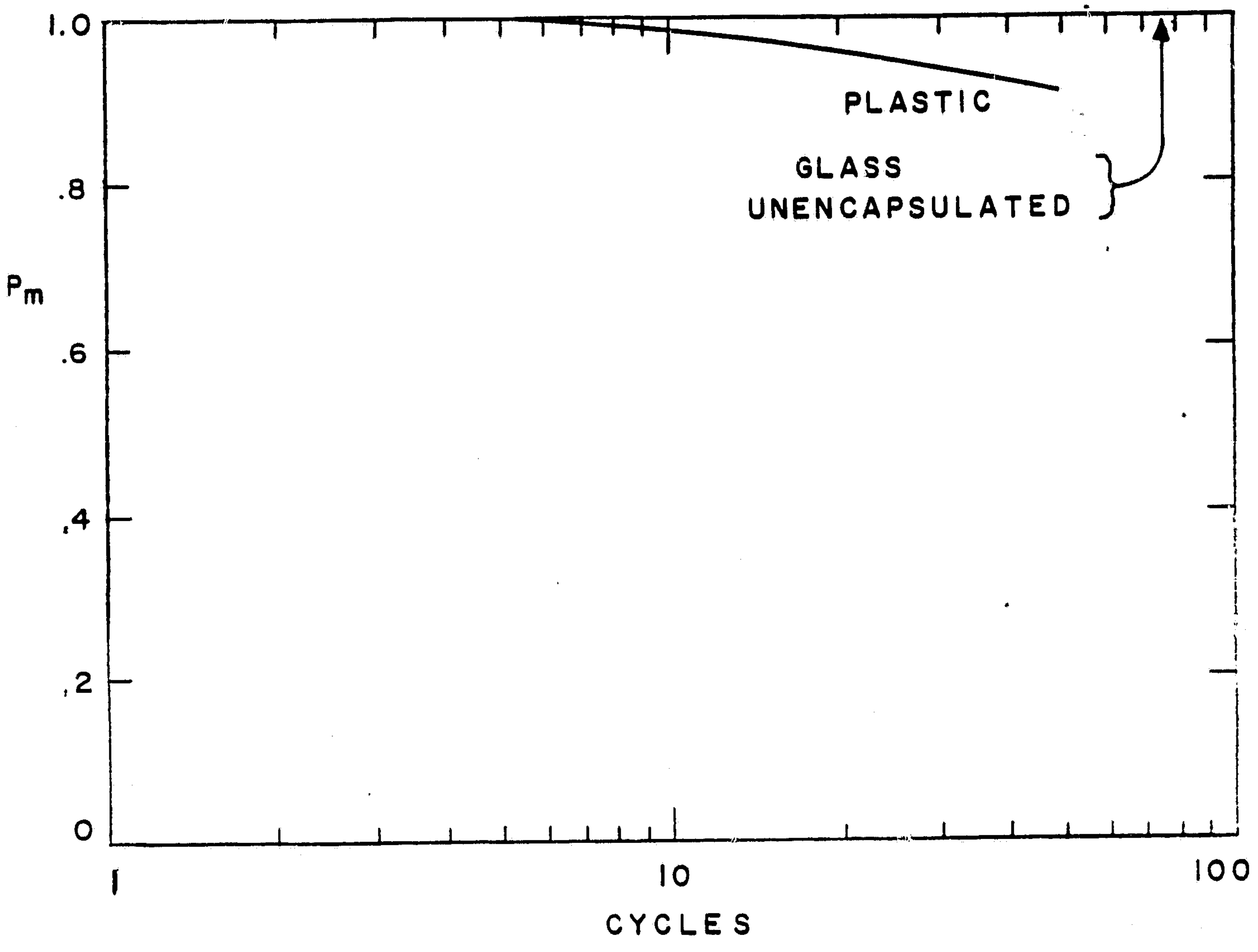

Figure 30. Average Normalized Pm as a Function of the Number of Thermal Cycles (-50°C TO +125°C)

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5.0 CONCLUSIONS

An accelerated test schedule has been designed and developed to enhance the anticipated falure modes of terrestrial solar cells. When a variety of cell types were subjected to this schedule different constructions responded differently, both electrically and mechanically, thus demonstrating the usefulness of an accelerated stress test program in discriminating between cell types and technologies. Accelerated testing of unencapsulated cells should be a valuable technique for rank-ordering low cost designs with respect to their potential field reliability prior to committing to large scale production.

Two types of changes were observed on bare cells after stressing: gradual electrical degradation and sudden "catastrophic" mechanical changes. The relative ability of accelerated testing to induce electrical degradation changes in the 12 cell types tested thus far in the program is summarized in Figure 16, and similarly, to induce mechanical catastrophic changes, in Figure 19. While these figures are based on average values, the rate at which electrical parameters, such as P_m, decrease when subjected to a particular stress varies not only between cell types, but from cell to cell within a given type. Because cells function together in complex series - parallel configurations[12], the statistical non-uniformity of parametric cell changes may be more significant than the absolute value of the change.

The occurrence of discontinuous mechanical effects is a complicated function of both the metallization system and the techniques and workmanship used during cell fabrication. Since an open circuit caused by lead failure can remove an entire series string from the array resulting in the overloading of other interconnected strings, this is a particularly serious failure mode.

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Cracking of a cell can similarly overload one portion of the cell provided the other portion is unconnected. Overloading can cause mismatched cells to become reverse biased resulting in localized heating, which in turn can cause rapid and perhaps catastrophic changes overloading other portions of the array. Detection of catastrophic (open circuit) tendencies is best accomplished through visual observation of stressed cells, and the major accelerating tests for these changes appear to be thermal cycle, thermal shock, and pressure cooker.

Accelerated stress testing of unencapsulated cells is valuable, since without the encapsulant present it is possible to utilize temperatures as high as the melting point of solder without introducing extraneous failure modes. Bias-temperature testing accelerates processes involving diffusion, and increasing temperature in this test will exponentially increase the speed with which the resulting effects can be detected. When the same range of temperature was used on encapsulated cells it was observed that the organics in many systems changed chemically introducing non-typical failure modes. The presence of absence of an encapsulant is not expected to influence diffusion in the semiconductor-metal system. On the other hand, an encapsulant can affect the ability of moisture to reach the cell surface and consequently can influence the speed of any corrosive chemical reactions which take place. This implies that the accelerated testing of encapsulated cells should involve primarily humidity and temperature cycling where the temperature can be kept below 100°C. A comparison between humidity induced degradation with and without encapsulation should be able to give an indication of the effect of the encapsulant. Preliminary experiments performed at relatively high stress levels failed to show much difference between cells with and without encapsulation perhaps indicating that the primary benefit of encapsulation may be mechanical protection. A more elaborate program is planned to investigate the effects of encapsulation using accelerated testing methods.

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APPENDIX A

DATA COLLECTION AND ANALYSIS PROCEDURES

The importance of rapid and accurate data collection and analysis was recognized early in the program and a consistent effort has been made throughout to implement such a system. This work has led to development of the short interval tester[5] and the associated hardware and software to transfer data to the IBM 370 for analysis using a commercial software program, Statistical Analysis System (SAS). This appendix summarizes the equipment and procedures which have been developed to accomplish this analysis.

Data Collection

Data collection consists of both electrically measuring the cells and visually inspecting them. Inspection procedures and an approach to quantifying the observations have been developed and are described in Section 3.0 of this report. Material in this Appendix deals only with the electrical measurements. Electrical measurement is accomplished by the Short Interval Tester which starts by recording in digital form the IV characteristic of the cell. Approximately 200 separate coordinates are measured from $V = V_{oc}$, $I = 0$ to $V = 0$, $I = I_{sc}$. This data is then reduced by the tester to determine the parameters V_{oc}, I_{sc}, V_m, I_m, and P_m. Further software development will shortly make two additional parameters, dV/dI at $V = 0$ and dV/dI at $I = 0$, available. These values are proportional respectively to the cell's series and shunt resistances. Both the reduced parameters and the raw data are stored on a floppy disk for later transfer to the IBM-370 computer.

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Measurement begins by entering the disk operating system through the system monitor as shown in Figure A1. In other words, the microcomputer is commanded by teletype to begin execution of the disk operating system program at its starting address. The disk operating system acknowledges:

"CRISIS II DISK OPERATING SYSTEM"

Data is always appended to a disk in IBM format based on a disk location containing the last used area on the disk, called Data Set Extent (EOE). As cells are added to the disk, the end of extent is updated to indicate the placement of new cell data. Since floppy disk memory is non-volatile, the end of extent marks the last used area on the disk between measurement sessions.

Following the flowgraph of Figure A1, the operator must first decide whether to append data to the diskette data set containing cell data or to command software to begin at the beginning of the data set, overwriting whatever data is on the disk. Reinitialization must occur after data on the diskette has been transferred to the IBM-370. If reinitialization is required the operator types

"-I"

otherwise the operator procedes to the next step.

One type of disk data set used by the tester is contained on a diskette called the Data Disk. The Data Disk contains the reduce parameters and is in IBM format. Another type disk dataset used by the tester is contained on a diskette called the system disk. The system disk is used to store software which is in charge of controlling cell measurement between measurement sessions. This data set is in Intel format. The disk operating system can therefore communicate with both the IBM-370 computer used for data analysis,

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and with an Intel Development System used for tester software development. Since the disk operating system is customized, the only restriction in communication between the tester and any computer is that the two devices must use the same type of diskette.

A third type of diskette used is called the IV disk. This disk is used to store the complete IV characteristic of each solar cell so that both the reduced set of parameters and the complete IV characteristic of each cell may be transferred to the 370 for analysis and storage. Since the details of storing the large amount of information contained in the IV data points permanently have not been completely worked out IV characteristics will be accumulated in volumes of diskettes in non standard format until 370 software can be developed to store them with the other data on magnetic tape at the Clemson Computer Center.

Before measurement begins, referring again to the flowgraph on Figure A1, the operator must command the Disk Operating System to load the tester cell measurement program into RAM. The necessity of disk program storage is illustrated in the tester memory map given in Figure A2. The tester program requires ten kilobytes of non-volatile memory for permanent storage. The choices for the storage medium were EPROM or diskette. Since EPROM storage is limited in flexibility and the addition of another EPROM board would exceed the number of slots in the tester's PC board card cage, disk storage was chosen.

As shown in the flowgraph, the operator loads the system disk and commands the tester DOS to transfer the program from disk into RAM. The operator types

"-X"

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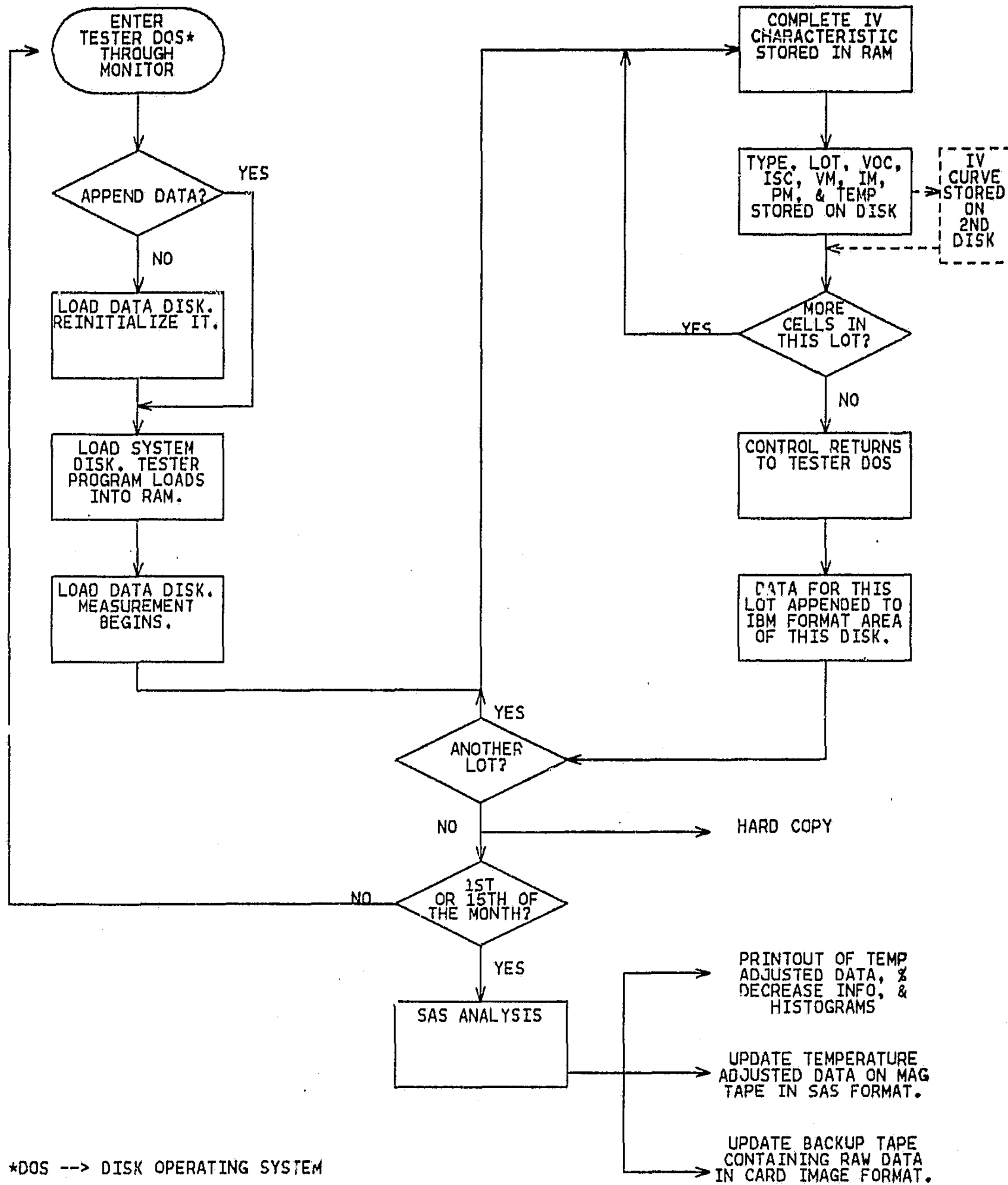

Figure A1. Tester Data Flow

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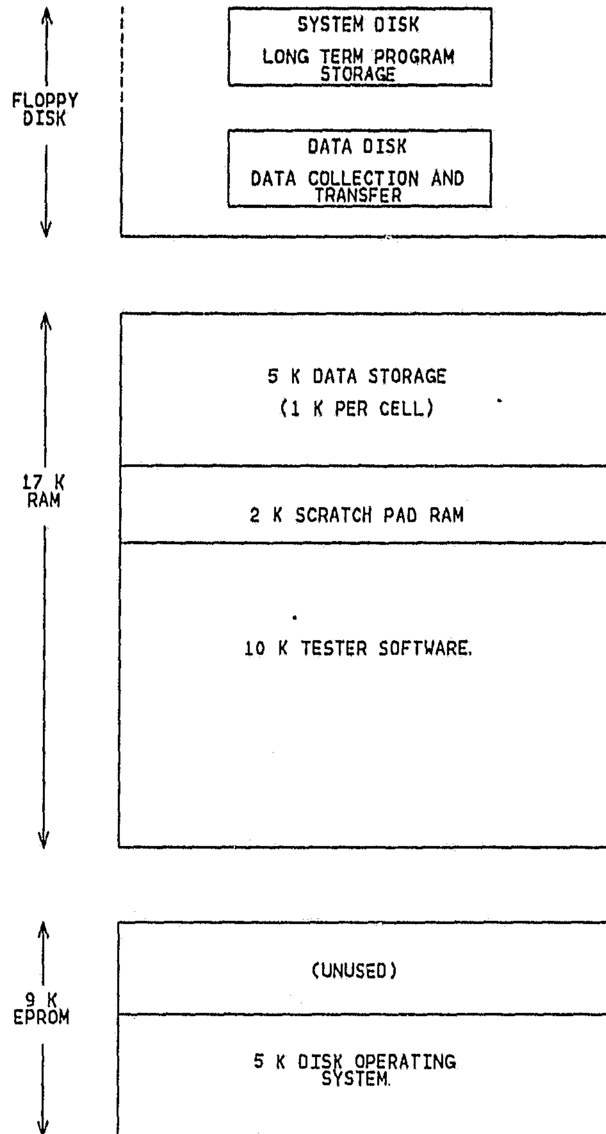

Figure A2. Tester Memory Map

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The computer responds:

"LOAD CRISIS II DATA DISK"

After software checks to ensure that the system disk has been removed from the drive so as not to overwrite data on the measurement program, cell measurement procedes as discussed in the Third Annual Report, except that disk storage has replaced paper tape storage. The operator inputs each solar cell's type, lot, and temperature. The tester automatically opens the shutter to the solar simulator, then electrically alters the cell current to force it to traverse the entire IV characteristic. The IV characteristic is visually displayed on a CRT and the reduced parameters simultaneously printed out on the teletype. After inspection, if the operator feels the data is reasonable he causes the tester to store the reduced parameters in temporary dataset on the Data Disk and to store the complete IV characteristic on the IV disk. The reduced parameters are stored in a temporary disk buffer for editing purposes. After measuring all cells in a lot, the operator transfers data from the temporary disk buffer to the IBM dataset by typing

"-X"

If there are other lots to measure, the process begins again by transferring the measurement program from disk to RAM, otherwise the measurement session ends with this data saved on disk. More data can be added next measurement session or this data along with the accumulation of data on the Data Disk can be transferred to the IBM-370 for analysis and storage.

Data Analysis

Data is transferred from diskette to the IBM 370 on the first and fifteenth of the month. A very short program initially reads the data from the diskette and then prints the data set contents on paper. The difficulty

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in spotting and fixing an error after data has been transferred to magnetic tape justifies the time required to make a dummy run to check for system or operator errors stored on disk. After the data check, a SAS program reads the data from diskette, adjusts the data for temperature affects on the parameters, performs percent decrease analysis on Pm and Isc and other variables if desired, prints normalized distributions of all the parameters, and finally stores the data on two magnetic tapes which never leave the computer center. One magnetic tape is used for analysis purposes while the other is used as backup. Sample printouts are given in Figures A3 through A10.

These printout examples are based on the supposition that the tester Data Disk contained only lot J 11, stress level 2, before the program was run. Figure A3 exemplifies the summary section of the printout. The summary section shows exactly where each lot stands in its stress schedule, and in the complete printout, lists all lots under study. Figure A4 gives the current lots section of the printout. Since only lot J 11 stress 2 was on the Data Disk, only that information is printed here. Figure A5 gives a listing of the data taken from the disk. Note that F, G, and H cells are corrected for temperature variations, before being printed in this section. (Refer to the second annual report for more information on temperature correction.) Figures A6 through A9 give percent decrease information about Pm for J 11. Figure A6 gives the complete history of the percent decrease of Pm for each cell in J 11. Note all percent change comparisons are made to prestress values. Figure A7 shows average of percent decreases for J 11 and the distribution of Pm for each stress level of J 11. For example, PCD1 is the average of percent decreases for J 11 stress 1; PGT5PD1 is the percent of the total population decreased more than five percent. Figure A8 gives the average Pm for each

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SUMMARY OF LOTS AND STRESS LEVELS

------------------------------ TYPE=J ------------------------------

DESC		
L12	T 0	150C B-T INITIAL
L12	T 1	150C B-T AFTER 300 HRS
L12	T 2	150C B-T AFTER 600 HRS
L12	T 3	150C B-T AFTER 1200 HRS
L15	T 0	BTH 85/85 INITIAL
L15	T 1	BTH 85/85 AFTER 250 HR
L15	T 2	BTH 85/85 AFTER 500 HR
L17	T 0	THERMAL CYCLE INITIAL
L17	T 1	THRM CYC 1 CYC -65C/150C
L17	T 2	THRM CYC 10 CYC -65C/150C
L17	T 3	THRM CYC 20 CYC -65C/150C
L18	T 0	THERMAL SHOCK INITIAL
L18	T 1	THERMAL SHOCK AFTER 1 SHKS
L19	T 0	UNBIASED PRES COOK INITIAL
L19	T 1	UNB PRES COOK AFTER 50 HR
L19	T 2	UNB PRES COOK AFTER 100 HR
L19	T 3	UNB PRES COOK AFTER 200 HR
L19	T 4	UNB PRES COOK AFTER 500 HR

Figure A3. Example of SAS Printout of Summary of Lots and Stress Levels

********* CURRENT LOTS ***********

-------------------- TYPE=J --------------------

DESC

L11 T 2 135C B-T AFTER 1200 HR

Figure A4. Example of SAS Printout of Current Lots

PRCOCESSED DATA

F G H - CELLS ARE TEMPERATURE CORECTED

---------------- TYPE=J DESC=L11 T 2 135C B-T AFTER 1200 HR ----------------

OBS	CELLNO	VOC	ISC	VM	IM	PM
1	27	0.573	0.879	0.448	0.819	0.366912
2	28	0.574	0.867	0.440	0.817	0.359480
3	29	0.576	0.890	0.451	0.819	0.369369
4	30	0.575	0.906	0.451	0.860	0.387860
5	31	0.578	0.866	0.449	0.821	0.368629
6	32	0.576	0.896	0.454	0.840	0.381360
7	33	0.574	0.894	0.440	0.857	0.377080
8	34	0.574	0.860	0.438	0.819	0.358722
9	35	0.570	0.861	0.452	0.801	0.362052
10	36	0.575	0.878	0.462	0.801	0.370062
11	37	0.570	0.869	0.452	0.799	0.361148
12	38	0.571	0.867	0.440	0.819	0.360360
13	39	0.563	0.872	0.445	0.801	0.356445
14	40	0.575	0.866	0.448	0.801	0.358848
15	41	0.576	0.869	0.446	0.819	0.365274
16	42	0.573	0.866	0.459	0.801	0.367659
17	43	0.569	0.866	0.482	0.761	0.366802
18	44	0.578	0.864	0.454	0.801	0.363654
19	45	0.570	0.862	0.452	0.800	0.361600

Figure A5. Example of SAS Printout of Processed Data

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PERCENT DECREASE IN PM CELL BY CELL

PCDX = % DECREASE OF PM AFTER X STRESS LEVELS

-- TYPE=J LOT=11 --

OBS	CELLNO	PM0	PM1	PCD1	PM2	PCD2	PM3	PCD3	PM4	PCD4
1	27	0.348	0.362	-4.023	0.367	-5.460	.	.	.	.
2	28	0.358	0.352	1.676	0.359	-0.279	.	.	.	.
3	29	0.354	0.350	1.130	0.369	-4.237	.	.	.	.
4	30	0.356	0.359	-0.843	0.388	-8.989	.	.	.	.
5	31	0.363	0.405	-11.570	0.369	-1.653	.	.	.	.
6	32	0.351	0.400	-13.960	0.381	-8.547	.	.	.	.
7	33	0.353	0.396	-12.181	0.377	-6.799	.	.	.	.
8	34	0.355	0.355	0.000	0.359	-1.127	.	.	.	.
9	35	0.361	0.357	1.108	0.362	-0.277	.	.	.	.
10	36	0.356	0.383	-7.584	0.370	-3.933	.	.	.	.
11	37	0.357	0.361	-1.120	0.361	-1.120	.	.	.	.
12	38	0.359	0.358	0.279	0.360	-0.279	.	.	.	.
13	39	0.355	0.354	0.282	0.356	-0.282	.	.	.	.
14	40	0.349	0.356	-2.006	0.359	-2.865	.	.	.	.
15	41	0.365	0.365	0.000	0.365	0.000	.	.	.	.
16	42	0.360	0.366	-1.667	0.368	-2.222	.	.	.	.
17	43	0.367	0.365	0.545	0.367	0.000	.	.	.	.
18	44	0.357	0.361	-1.120	0.364	-1.961	.	.	.	.
19	45	0.351	0.359	-2.279	0.362	-3.134	.	.	.	.

Figure A6. Example of SAS Printout of Percent Decrease of Pm Cell by Cell

AVERAGE OF % DECREASES OF PM AND CUMULATIVE DISTRIBUTION

PCDX = AVERAGE OF % DECREASES OF PM AFTER X STRESS LEVELS .
PCTYPDX = % OF CELLS WITH MORE THAN Y% DECREASE AFTER X LEVELS
TYPE=J LOT=11

VARIABLE	N	MEAN	STANDARD DEVIATION
PCD1	19	-2.80710319	4.84258989
PCT5PD1	19	0.00000000	0.00000000
PCT10PD1	19	0.00000000	0.00000000
PCT25PD1	19	0.00000000	0.00000000
PCT50PD1	19	0.00000000	0.00000000
PCD2	19	-2.79806327	2.85707598
PCT5PD2	19	0.00000000	0.00000000
PCT10PD2	19	0.00000000	0.00000000
PCT25PD2	19	0.00000000	0.00000000
PCT50PD2	19	0.00000000	0.00000000
PCD3	0	.	.
PCT5PD3	0	.	.
PCT10PD3	0	.	.
PCT25PD3	0	.	.
PCT50PD3	0	.	.
PCD4	0	.	.
PCT5PD4	0	.	.
PCT10PD4	0	.	.
PCT25PD4	0	.	.
PCT50PD4	0	.	.
PCD5	0	.	.
PCT5PD5	0	.	.
PCT10PD5	0	.	.
PCT25PD5	0	.	.
PCT50PD5	0	.	.

Figure A7. Example of SAS Printout of Average Percent Decreases of Pm

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AVERAGE PM

MPMX = AVERAGE PM AFTER X STRESS LEVELS
TYPE=J LOT=11

VARIABLE	N	MEAN	STANDARD DEVIATION
PM0	19	0.35657895	0.00515661
PM1	19	0.36652632	0.01664788
PM2	19	0.36647368	0.00820141
PM3	0	.	.
PM4	0	.	.
PM5	0	.	.

Figure A8. Example of SAS Printout of Average Pm

PERCENT DECREASE OF AVERAGE PM

PMDX = % DECREASE OF AVERAGE PM AFTER X STRESS LEVELS

---------------------- TYPE=J LOT=11 ----------------------

OBS	PMD1	PMD2	PMD3	PMD4	PMD5
1	-2.7897	-2.7749	.	.	.

Figure A9. Example of SAS Printout of Percent Decrease of Average PM

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stress level Figure A9 gives the percent decrease of average Pm. The difference in this section and the average of percent decreases section discussed earlier is that this section gives the percent decrease of lot average while Figure A7 gives the average of the percent decreases over all the cells for a particular lot and stress level. A similar section of the printout, no shown, conveys the same information as figures A6 through A9 except that percent decrease in Isc information is being presented instead of percent decrease in Pm information.

The next section of the SAS printout contains distribution histograms of the electrical parameters. Consider, for example, Figure A10, which shows the distribution of Pm after stress level 2. The horizontal axis is normalized volts. For example a normalized Pm of 1.0 has a magnitude equal to the average of all prestress Pm values for this lot. The horizontal axis gives the percent of the total cell population within five percent of a normalized Pm midpoint. So for Figure A10, 84 percent of the population has Pm between 95 and 105 percent of the prestress average Pm for this lot, while 16 percent of the population has Pm which is 5 to 15 percent greater than the prestress Pm for this lot. Similar information is conveyed about Voc, Isc, Vm, and Im, in histograms not shown.

System Improvement

Just as analysis relies on the IBM-370 computer and an upper level language called SAS, system improvement procedures rely on an Intel development computer system called MDS and an upper level language called PLM/80. As new features are added to the tester, the tester software must be modified so that the system will process the new data automatically. Since development software is expensive and often requires a system architecture unsuited for application oriented projects, an MDS system owned by the Clemson University

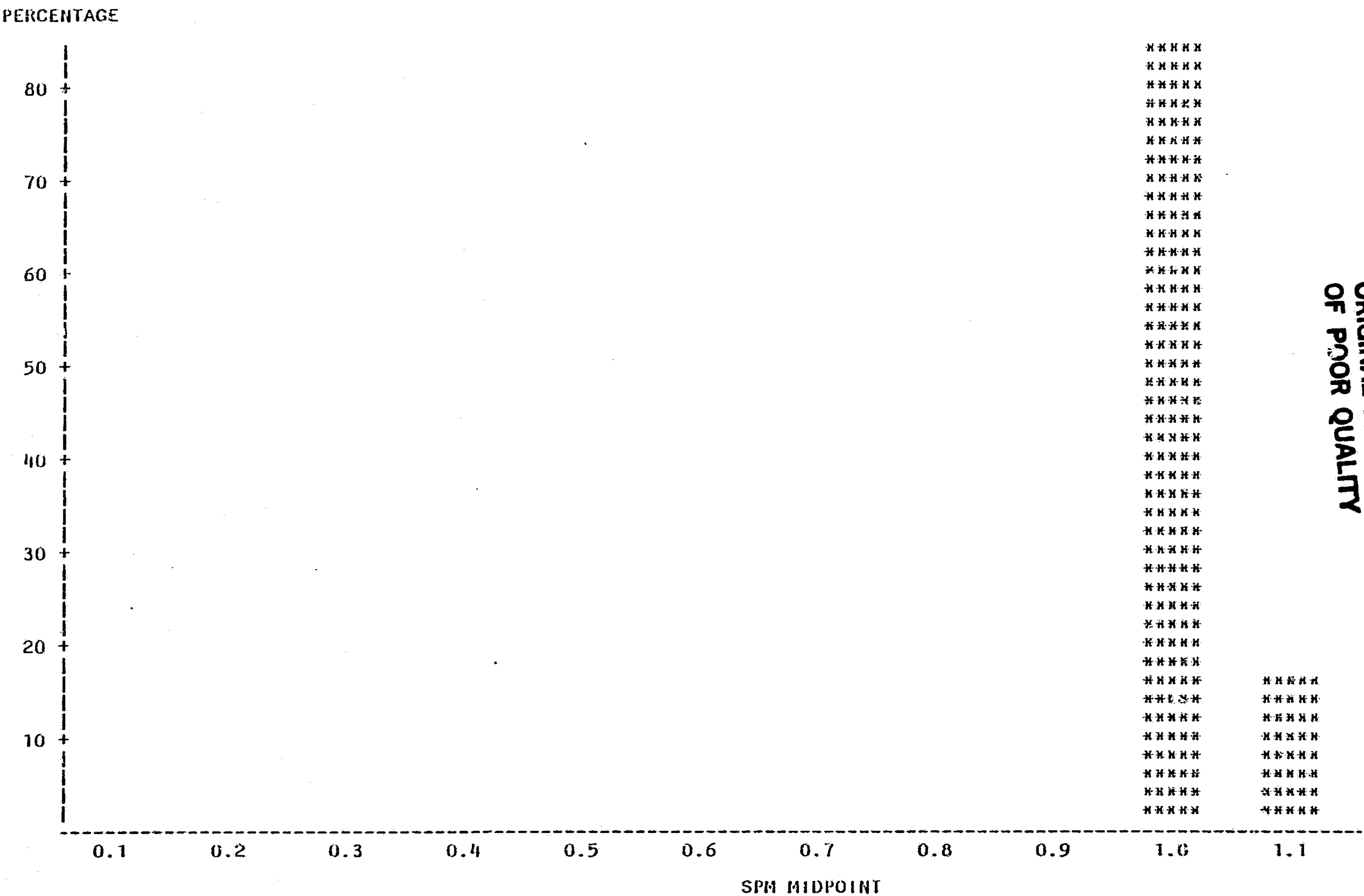

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Figure A10. Example of SAS Printout of Pm Distribution Histogram

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Electrical Engineering Department has been utilized.

As shown in the memory map of Figure A2, there are two areas of memory that contain software for two independent tester functions. Cell measurement software is stored on diskette in non-executable ASCI representation of the machine code (object code), while the disk operating system is stored in EPROM as executable object code. While the two programs are distinct and system improvement usually only requires modification of the tester program, care must be taken to ensure that the tester software is linked correctly to the disk operating system. In many cases, a change in measurement software can be effected without changing EPROM contents, realizing a savings in time, complexity, and, since the number of time an EPROM can be programmed is finite, EPROM life. In general however, unless special care is taken to assure that starting addresses are correct and PLM/80 library functions are complete, but not duplicated, the entire EPROM section must be reprogrammed. A flowgraph showing the tester program development flow is given in Figure All.

Tester program modifications are made by adding or changing tester subroutines called modules, with the MDS editor. Although program modifications are usually made in the PLM/80 language as it is a powerful and easily read language, the MDS disk operating system, ISIS allows assembly language modules to be linked with PLM/80 modules when the application calls for high speed or flexibility beyond the scope of PLM/80. After the tester program has been modified it is in source code form. Source code means that the assembly language commands are in non-executable mnemonics. Following the flowgraph of Figure 11, the source code is next transformed to machine executable object code with either the PLM/80 compiler or, in rare cases, the 8080 assembler. After compiling the modules the tester program must be linked to the disk

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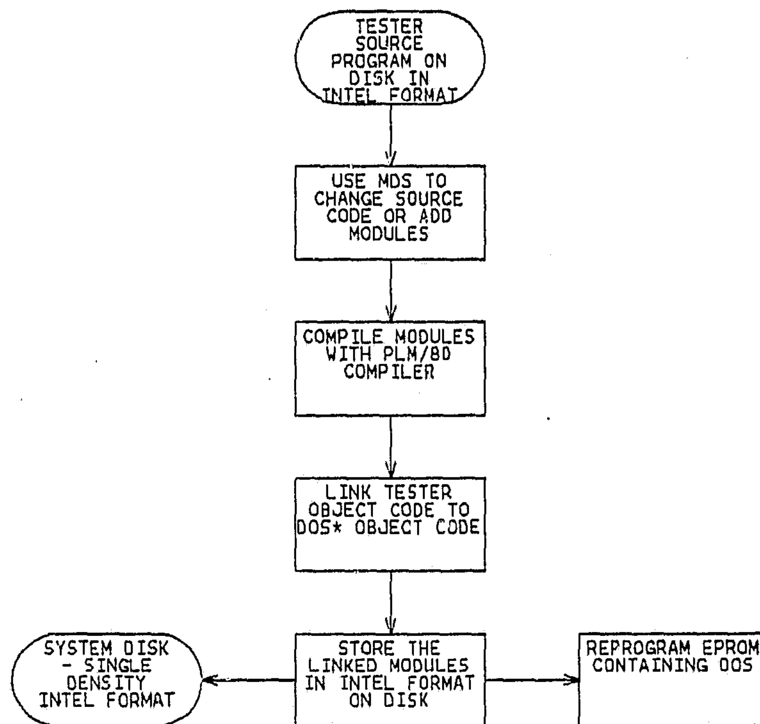
TESTER PROGRAM DEVELOPMENT FLOW



DOS --> TESTER DISK OPERATING SYSTEM

Figure A11. Tester Program Development Flow

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operating system. Linking is necesary because the tester software must make calls to subroutines in the disk operating software when writing data to the diskette. Following the linking of measurement software to the tester disk operating system software, two separate but interfaced programs exist. The data set containing the measurement program is transferred to diskette in INTEL ASCI representation of the object code. This diskette may now be used as the System Disk. The dataset containing the disk operating system must be transferred to EPROM unless special pains are taken to avoid this step.