MEMORY TECHNOLOGY SURVEY

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ABSTRACT

The current status of semiconductor, magnetic, and optical memory technologies is described in this report. Research activities planned for the short term future were discussed with cognizant personnel. Projections based on these discussions are presented. Conceptual designs of specific memory buffer applications employing bipolar, CMOS, GaAs, and Magnetic Bubble devices are discussed. The Memory Technology Survey was performed by McDonnell Douglas Astronautics Company under the direction of John A. Newell, for the National Aeronautics and Space Administration, Goddard Space Flight Center under contract number NAS 5-25599.

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SECTION I
INTRODUCTION

A Memory Technology Survey (MTS) has been performed for the NASA End-to-End Data System (NEEDS) Modular Data Transport System (MDTS) at the Goddard Space Flight Center (GSFC).

The objectives of the NEEDS program, as stated in NEEDS System Concept (Feb. 1979), are to "provide the system concepts, techniques, and technology which will increase the end-to-end data system responsiveness, reduce the relative cost of extracting information from space data, and increase the degree of standardization throughout the system."

The MTS is one of several activities which have been undertaken by GSFC in support of the NEEDS objectives. Figure 1-1 indicates the role of this study in the NASA's overall system plan.

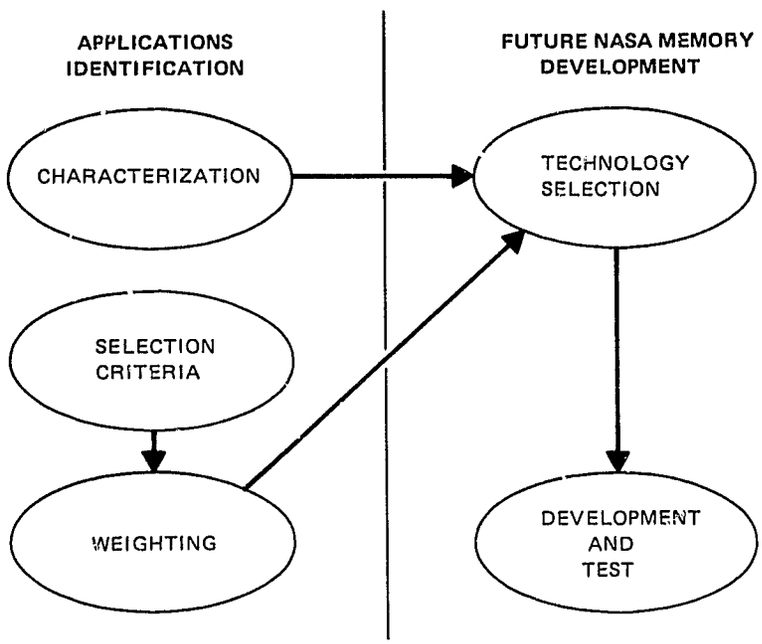

FIGURE 1-1 THE NASA'S SYSTEM APPROACH

A 36 week project plan was devised to execute the three major sub-tasks shown in Figure 1-2 and to prepare a final report.

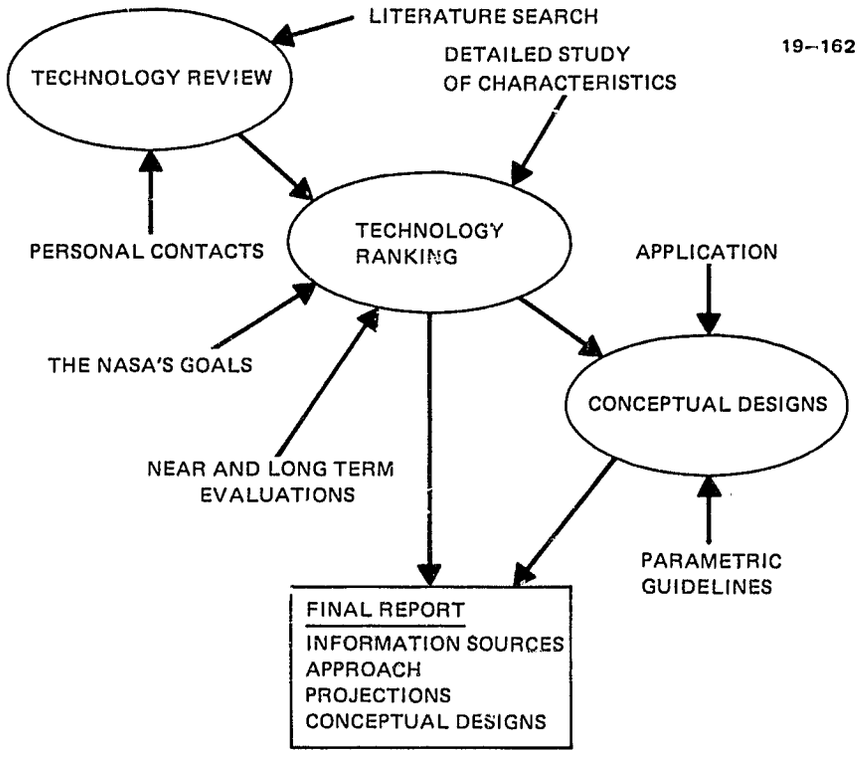

FIGURE 1–2 STUDY APPROACH

Task 1 consisted of a survey and review of memory technology literature for the period from 1975 to 1980. During this phase many authors were contacted via telephone and/or personal visits.

Task 2 identified those technologies which offer potential for present or future NASA memory applications. This task was delayed somewhat because application data were not received as scheduled. Near (1982-1987) and long (1987-1992) term technology rankings in terms of NASA applications were a further result of Task 2.

Task 3 produced conceptual designs of five (5) specific applications using technologies suggested or approved by the NASA personnel at GSFC.

This report is arranged along the same logical flow employed in conducting the study. It is thus demonstrated that the statement of work was properly addressed and the tasks were stepping stones to the final report.

SECTION 2
STUDY TASK 1
LITERATURE SEARCH

Libraries at GSFC, McDonnell Douglas Corporation (MDC), and Washington University were the primary resources utilized during the accomplishment of this task. Current issues of appropriate periodicals, e.g., ELECTRONIC ENGINEERING TIMES and ELECTRONICS provided additional relevant information. Many of the researchers provided copies of papers which were not revealed by the libary data bank searches. A bibliography appears as an appendix to this report.

The statement of work upon which this study is based includes a comment to the effect that a literature search is not a sufficient basis for determination of the state of the art of memory technology because the literature lags the art by at least a year. While this is true, the effectiveness is further compounded by the fact that devices are often described two or three years before even samples are available.

Another difficulty exists because a majority of the papers describing research activity are highly theoretical treatments. These seldom offer any firm data relative to the applicability of the technology to specific memory applications. Some of these problems were overcome by personel contact with the authors.

A memory technology assessment prepared in 1975 by James E. Partak at the White Oak Naval Surface Weapons Center in Silver Spring, Maryland identified 24 memory technologies complete with 1975 characteristics and those projected for 1980. This list, presented as Table 2-1, formed the basis of the study. No technologies not included in the table appeared during the course of the study.

To establish a common basis of understanding between the author and the readers of this report, the following terms and acronyms are defined.

TABLE 2–1a SEMICONDUCTOR MEMORIES

19–134

BIPOLAR DEVICES
TRANSISTOR-TRANSISTOR LOGIC (TTL)
EMITTER COUPLED LOGIC (ECL)
INTEGRATED INJECTION LOGIC (I^2L)
METAL-OXIDE-SEMICONDUCTOR
P CHANNEL (PMOS)
N CHANNEL (NMOS)
COMPLEMENTARY (CMOS)
CHARGE COUPLED DEVICE (CCD)
METAL-NITRIDE-OXIDE SEMICONDUCTOR (MNOS)
FLOATING GATE (FAMOS)
OTHER SEMICONDUCTOR TYPES
GALLIUM ARSENIDE (GaAs)
AMORPHOUS SEMICONDUCTOR (OVONIC)
CRYOGENIC (JOSEPHSON)

TABLE 2–1b MAGNETIC MEMORIES

CORES
PLATED WIRE
MATED FILM
CLOSED FLUX
FERROELECTRIC
FERROACOUSTIC
CROSSTIES
TAPE
DISC
BUBBLES

TABLE 2–1c OTHER MEMORY TECHNOLOGIES

ELECTRON BEAM ADDRESSED (EBAM)
OPTICAL DISC

Read Only Memory (ROM): A memory device in which the stored information is fixed. By convention ROM's are mask programmed during wafer fabrication and it is not possible to alter the contents.

Programmable Read Only Memory (PROM): A ROM whose contents are inserted by the user after fabrication. Typically the devices are manufactured with a binary "1" stored in each memory location. Fuse links are provided to allow the user to insert "0's" as desired. Reprogramming is limited because "1's" cannot be recreated. PROM's are typically less expensive than ROM's for low volume applications.

Erasable Programmable Read Only Memory (EPROM): A PROM in which information is stored in charge packets which are isolated from direct leakage paths. Alteration of the conducting characterisitcs of one or more circuit element per memory cell represents the stored data. Application of ultra-violet light to the charge packets dissipates the charge and returns all memory cells to a common state. Charge packets may be created individually in desired cells by application of a sufficiently high voltage to produce the necessary tunneling effect.

Electrically Alterable Read Only Memory (EAROM): Like the PROM, the EAROM may be reprogrammed. The essential difference lies in the technique employed to erase the device. The EAROM may be erased by application of a voltage (of opposite polarity to that used for programming) to the programming pins. Typically these are Metal-Nitride-Oxide Semiconductor (MNOS) devices.

Electrically Erasable Programmable Read Only Memory (EEPROM): This device is similar to the EAROM. Organization is typically Byte (8 bits) wide with a single Byte or entire chip erasure provided. The essential difference between EEPROM's and EAROM's appears to be in the storage medium; the surface layer between nitride and oxide in the former, and a floating silicon gate in the latter.

Random Access Memory (RAM): The designation RAM is misleading but generally accepted terminology. It implies that ROM's are not random access. These should be called Read Write Memories (RWM's). Information is stored in bistable circuit elements whose states may be altered by application of appropriate voltages during the write operation. Typically RAM's are volatile storage devices, that is the stored information is lost if the operating voltage is removed.

Block Oriented Random Access Memory (BORAM): A RAM in which addressing may be accomplished only to a block of data bits (typically from 32 to several thousand bits) as opposed to the individual bit addressability of RAMs.

Serial Addressed Memory (SAM): Reading or writing may be accomplished only by addressing the initial location involved in the data transfer. Subsequent transfers involve locations specified by the memory circuitry.

Table 2-1 is subdivided into three technology classes; Semiconductor, Magnetic, and Other. These subdivisions are not mutually exclusive. Nevertheless it is reasonable to group the technologies in sets whose members exhibit similar operating characteristics.

A brief discussion of each of the technologies which were investigated is presented in the appendix. Tables 2-2, 2-3, and 2-4 summarize the current status of semiconductor memories. Section 3 provides similar information for each of the technologies selected for further investigation.

TABLE 2–2 CURRENT STATUS OF BIPOLAR MEMORIES

19–163

	TTL		ECL		I^2L	
	RAM	ROM	RAM	ROM	RAM	ROM
MAXIMUM CAPACITY	4K	16K	4K	1K	4K	16K
CYCLE TIME	80 nS	110 nS	60 nS	40 nS	240 nS	300 nS
OPERATING VOLTAGE	5	5	–5.2	–5.2	5	5
OPERATING POWER	560 mW	825 mW	1.01 W	780 mW	500 mW	
STANDBY POWER	560 mW	825 mW	1.01 W	780 mW	50 mW	
OPERATING TEMP. RANGE	–55 TO 125°C	–55 TO 125°C	0 TO 85°C	–55°TO 125°C	0 TO 70°C	0 TO 70°C
RAD. TOL RADS (Si) TOTAL	10^6 –10^7	10^6 –10^7			10^6	10^6
ARCHITECTURE	4K x 1	2K x 8	4K x 1	256 x 4	DYNAMIC 4K x 1	

TABLE 2–3 CURRENT STATUS OF MOS MEMORIES

19–164

	NMOS	CMOS	MNOS	FLOATING GATE CCD	
MAXIMUM CAPACITY	64K	64K	8K	16K	64K
WRITE TIME	250 nS	600 nS	50 μS	10 mS	200nS
READ TIME	250 nS	600 nS	1 μS	250 nS	200 nS
OPERATING VOLTAGE	5	5	–15, 15	5, 21	–5, 5, 12
OPERATING POWER	200 mW	300 mW	400 mW	495 mW	336 mW
STANDBY POWER	20 mW	5 mW	ZERO	132 mW	66 mW
OPERATING TEMP. RANGE	0 TO 125°C	0 TO 125°C	–55 TO 125°C	0 TO 70°C	0 TO 55°C
RAD. TOL. RADS (Si) TOTAL	10^3	10^5 – 10^6	3×10^4	10^6	10^3
ARCHITECTURE	64K x 1	16K x 4 8K x 8	256 x 32	2K x 8	64K x 1
TYPE	DYNAMIC RAM	HYBRID RAM	BORAM	EAROM	SPS SHIFT REG.

TABLE 2-4 CURRENT STATUS OF OTHER SEMICONDUCTOR MEMORIES

	AMORPHOUS	CRYOGENIC	G_aA_s
MAXIMUM CAPACITY	1K	16K	4K
WRITE TIME	250 μS	30 nS	10 nS
READ	10 nS	30 nS	10 nS
OPERATING VOLTAGE	5, 15	AC	5
OPERATING POWER	200 mW WRITE 2 mW READ	40 μW	75 mW
STANDBY POWER	ZERO	ZERO	20 mW
OPERATING TEMP. RANGE	0 TO 70°C	+4°K	TO 300°C
RAD TOL. RADS (Si) TOTAL	10^7	UNKNOWN	10^7 (GaAs)
ARCHITECTURE	1K x 1	16K x 1	4K x 1
TYPE	EAROM	RAM	RAM

SECTION 3
STUDY TASK 2
TECHNOLOGY COMPARISON

After the results of the literature search were studied and discussed with technical representatives of the NASA the following technologies were eliminated for the reasons listed:

PMOS Compared to NMOS these devices are more difficult to interface to TTL logic levels. The speed power product is inferior and the bit density (for a given operating speed) is less.

Plated Wire This technology which was originally intended as a replacement for magnetic core memories has not lived up to expectations. The primary disadvantages are high cost, complexity of interfacing, and operating power requirement.

Closed Flux This is a planar counterpart of plated wire. It has been abandoned for the same reasons.

Mated Film Another variation on the core replacement theme, this technology could not compete with semiconductor memory devices.

Ferroelectric This was originally intended to be an EAROM. It could not compete with ultra-violet EPROMs.

Ferroacoustic An early BORAM technology, this could not compete with MNOS BORAMs and Magnetic Bubble devices.

Electron Beam Addressed Memory Difficulties associated with production of reliable targets and tubes have caused this technology to be shelved temporarily in favor of solid state devices.

TECHNOLOGY RANKING

The remaining 17 technologies from Table 1.1 have been compared according to a set of selection criteria supplied by the NASA. Table 3-1 is a tabulation of the technologies and their ranking.

TABLE 3–1 1980 TECHNOLOGY RANKING

19–181

TECHNOLOGY	RAD. TOL.	RISK	SYS. REL.	AVE. SYS. POWER	SYS. WT. & VOL.	FUTURE AVAIL.
TTL	10^6	1	1	13	7	1
ECL	10^6	1	1	14	7	1
I^{2}L	10^6	3	1	12	7	1
NMOS	10^3	1	1	2	2	1
CMOS	10^5	1	1	5	5	1
MNOS	10^4	2	1	11	6	1
CCD	10^3	1	1	3	2	1
FLOATING GATE	10^6	3	1	10	5	1
AMORPHOUS	10^7	4	2	14	10	3
GaAs	10^7	5	1	8	7	2
CRYOGENIC	UNK	5	5	6	UNK	2
MAG. CORE	10^7	1	3	7	8	1
MAG. DISC	10^7	2	5	9	9	1
MAG. TAPE	10^7	1	4	1	3	1
MAG. BUBBLE	10^7	3	1	4	4	1
CROSSTIE	10^7	5	UNK	UNK	UNK	3
OPTICAL DISC	UNK	4	6	9	1	2

The technologies which are included have widely differing characteristics and are intended for diverse applications. It is difficult to derive accurate comparisons because parameters of specific applications affect the rankings. For example the volume and power requirements of a magnetic tape recorder are to a large degree independent of the storage capacity of the tape.

In an attempt to provide a modicum of consistency the average system power and system weight and volumes are based upon a storage capacity of 10^8 bits.

Actual total dose tolerance for each technology is given in the Radiation Tolerance column. Entries in the other columns are comparative with 1 indicating the optimum technology in terms of the characteristic to which the column is dedicated.

The entries in the Risk column are based upon the following code:

1. Mature technology which has been used in space systems.
2. Mature technology which has been used in military aircraft systems.
3. Mature technology which has been used in ground based systems.
4. Emerging technology for which full scale laboratory versions exist.
5. Experimental technology which has no significant laboratory models.

The entries in the System Reliability column rate the reliability without regard to radiation tolerance. The number 1 indicates the most reliable system. Those systems with mechanical subsystems naturally are less reliable. This accounts for the poor rating of magnetic discs and tape recorders. The refrigeration unit required for the cryogenic system is the primary reason for its poor rating.

Average system power and system weight and volume comparisons are based upon bit density and power requirements per bit. System data were available for cores, discs, and tape. The rankings of the other systems were obtained by multiplying storage section parameters by a factor of 1.25. The lowest numbers in these columns represent optimum values.

In the future availability column the numbers indicate the following:

1. Availability of military and commercial versions is assured.
2. Commercial versions are virtually certain. Military versions will require financial support.
3. The technology is emerging. Future availability of military versions is highly doubtful without tremendous support.

NEAR TERM (1982-1987) PROJECTIONS

BIPOLAR DEVICES

In the past the advantages of Bipolar Memories have been operating speed and radiation tolerance. These have been enhanced at the expense of storage density and power requirement.

Recent research reported by Bhattacharyya et. al. of IBM has produced a 64K bipolar RAM which is referred to as a I/N device. This approach provides bipolar performance with density approaching that of FET devices.

Design goals for the 64K RAM are 100 ns cycle time with 500 mw power dissipation using a single 5 volt power supply. The chip size is 30 mm^2.

National Semiconductor bipolar research is aimed at reducing the cycle time. Mike Milhollan of National predicts a 4K ECL RAM in the 5 ns range before 1987. 16K bipolar static RAMs should be commonplace by the latter part of this time period.

MOS DEVICES

Research in MOS devices will be directed toward increasing storage density, improving yield, increasing speed, and reducing the cost of testing. Several companies have announced 64K RAMs. Typically these large devices contain redundant rows of cells which can be used to replace rows containing defective cells.

Bell Labs has recently announced an improved Xray lithography system which they predict will lead to production of submicron channel length MOS devices. They report a speed power product of 5 femtojoules at a toggle rate of 2.5 GHz.

If the promises are fulfilled MOS switching speeds will exceed those of ECL and begin to challenge GaAs. It is difficult to predict whether or not this technique will yield production devices by 1987, but based upon past performance of the industry it is reasonable to assume that it will. The VHSIC program should increase the probability of success of this technique.

Fairchild predicts a static 64K MOS RAM in production by 1985 with a 256K version by 1987. The latter will be a prototype 0.5 micron device. They also predict 256K DRAM and 1 Mbit CCD production units by 1987. Projected cost of the latter is 0.75 millicent per bit in 1980 dollars. Fairchild is attacking the radiation tolerance problem by developing cool package circuitry. Cool package lids are made from materials which do not themselves emit alpha particles.

Robert Dennard of IBM, Yorktown Heights, New York predicts that 0.5 micron technology will yield a 2 Mbit MOS RAM by 1987 or 1988. Threshold voltage scaling restrictions will probably limit storage density in MOS devices to 2 M bits. He feels that radiation tolerance problems can be solved at the 1 micron level by incorporating some processing modifications.

OTHER SEMICONDUCTOR DEVICES

Present indications are that 4K GaAs RAMs will be in production by 1983 or 1984. Hence it is reasonable to assume that 16K versions will be available by 1987. The suppliers might elect to proceed directly from 4K to 64K devices because they have a bank of processing experience carried over from other technologies.

National Semiconductor predicts a 128K FAMOS E^2 PROM by 1987. Since Intel has a 16K E^2 PROM in production now, it is reasonable to assume that they too will have a 128K device by 1987. These memories become viable at this storage density because they represent an alternative to MNOS for nonvolatile RAMs.

MAGNETIC MEMORY DEVICES

The near term time frame will see 9 mil magnetic cores in volume production. Intel Magnetics predicts 4 M bit bubble chips with 200 K bit data rate and operating temperature range of -20° to 85°C. 16 M bit devices will probably use current access in a bubble lattice configuration. These devices will probably not be available by 1987.

RCA has demonstrated 60 M bit per in^2 storage density on magnetic tape. Laboratory versions have successfully operated at a 600 M bit data rate with 10^{-6} bit error rate. Storage capacity on a 1" by 4800' tape is 5.4×10^{11}. Production versions of this unit will require about 2 to 3 years. If funding is committed this will be available during the 1982-1987 time period.

OPTICAL DISC MEMORIES

If sufficient development funds are provided this technology will provide production models with 10^{11} bits storage capacity on one 12" disc. Data rates of from 5 to 300 M bits will be achieved with bit error rate of 10^{-5} to 10^{-7}. This will require a multi-million dollar investment over a 2 to 5 year period.

Table 3-2 summarizes the projections which have been discussed relative to the 1982-1987 time period. Those technologies which are excluded from the table are not considered likely candidates for spacecraft buffer applications in this time period.

TABLE 3–2 1982–1987 PROJECTIONS

19–182

TECHNOLOGY	CAPACITY	RAD. TOL.	DATA RATE	AVAILABILITY
BIPOLAR	64K	10^7	100M	2
NMOS	256K	10^5	2.5G	2
CMOS	64K	10^6	10M	2
CCD	1M	10^5	10M	1
MNOS	131K	10^5	2M	1
FLOATING GATE	128K	10^6	5M	1
GaAs	16K	10^7	4G	1
TAPE	10^{12}	10^7	600M	2
BUBBLES	4M	10^7	200K	1
OPTICAL DISC	10^{11}	UNK	300M	2
CROSSTIE	128K	10^7	20M	3

The "2" and "3" entries in the Availability column indicate that considerable development effort will be required to achieve the projected parameter values.

LONG TERM (1987-1992) PROJECTIONS

It is not possible to project accurately this far ahead. Too many variables are involved. Therefore the following is submitted.

The most promising technology for medium capacity (1 to 10 M bit) RAMs in the 1987-1992 time period is GaAs. It will, with adequate support experience the same increase in density as MOS devices have. 256K GaAs RAMs should be available during this time period. This technology should be supported.

16 M and larger Magnetic Bubble devices will require an approach different from that of present production devices. One technique is a bubble lattice structure controlled by magnetic fields produced by current sheets. As indicated earlier, IBM has temporarily shelved this approach in favor of the conventional bubble devices. Bell Labs continue to investigate this technique. A great deal of time and money will be required to implement this technique.

Optical discs which write and read with laser diodes on an erasable medium will be available by 1992 with or without military funding. The tremendous consumer and commercial markets provide the incentive to develop this technology. External funding will be required if military and/or space qualified versions are desired. Even if optical disc memories are not destined to fly, the technology should be supported because it is an attractive approach to low cost archival storage.

The VHSIC program will no doubt produce breakthroughs in semiconductor processing which could conceivably produce 1 M bit or larger radiation hardened RAMs by 1992. In that event it will be practical to consider 10^8 bit solid state memory systems.

SECTION 4
STUDY TASK 3
CONCEPTUAL DESIGNS

A group of five specific memory applications was provided by the NASA as a result of a companion study which was performed by G. Mosley of General Electric Space Division in Valley Forge, Pennsylvania. The applications include: Packet Buffer, Packet Queuing Buffer, Experiment Data Storage, High Rate Data Processing Buffer, and Retrievable Buffer. Tables 4-1 through 4-5 describe the characteristics of the individual applications. These tables were taken from G. E. Document No. 80SDS4242, October, 1980.

As an aid in selecting appropriate technologies for each of the applications, the NASA supplied a "model" set of characteristics for each, including guideline values of weight, volume, and power. These models appear in discussions of the individual conceptual designs.

TABLE 4–1 PACKET BUFFER

A Fixed Size Buffer Used by Instruments and Experiments to Accumulate Data, Format Data and Merge Ancillary Data

19–183

REQUIREMENT	SPECIFICATION	COMMENT
CAPACITY	256 TO 4M BIT	4000 BIT PACKET TYPICAL TODAY
ORGANIZATION	BY WORD, 8/16 BITS	
STORAGE ACCESS.	RANDOM ACCESS	SUPPORTS CREATION OF AUTONOMOUS DATA PACKETS
I/O PORTS	MULTI IN/SINGLE OUT	
INPUT MODE	SERIAL/PARALLEL	
OUTPUT MODE	SERIAL	
READ RATE	1 Kbps TO 2.0 Mbps	
WRITE RATE	1 Kbps TO 2.0 Mbps	
NON-VOLATILITY	NOT REQUIRED	
OPERATIONAL LIFE	3–10 YRS.	DEPENDS ON S/C MISSION LIFE
RAD. HARDENING	REQUIRED	SOME NON-HAZARDOUS MISSION REQUIREMENTS MAY BE EXPECTED
PRIMARY APPL.	DATA ACCUMULATION, TIME TAGGING, FORMATTING AND MERGING OF ANCILLARY DATA LOW VOLUME DATA BUFFERING FOR EXPERIMENT	
APPLICATION MODE	MULTI-SOURCE, BURST OR TRICKLE INPUT; CONTINUOUS PACKET TRANSFER	
APPROX. DATE REQUIRED	1984	

TABLE 4–2 PACKET QUEUING BUFFER

A Buffer Used at the System Level by the Spacecraft Bus to Store Data from Individual Experiments for Subsequent Transmission or Storage on a Tape Recorder. The Structure is not Necessarily a Fifo.

19–184

REQUIREMENT	SPECIFICATION	COMMENT
CAPACITY	10K – 10^7 BITS	DEPENDS ON DATA SYSTEM STRUCTURE
ORGANIZATION	BORAM	
STORAGE ACC.	RANDOM BY BLOCKS	COMPUTER COMPATIBLE
I/O PORTS	ONE IN/ONE OUT	
INPUT MODE	SERIAL/PARALLEL	
OUTPUT MODE	SERIAL/PARALLEL	
READ RATE	1 Kbps TO 2.0 Mbps	
WRITE RATE	2.0 Mbps	
NON-VOLATILITY	NOT REQUIRED	
OPERATIONAL LIFE	2 TO 5 YEARS	
RAD. HARDENING	RADIATION HARDENING TO 200K RAD	FUNCTION OF MISSION PROFILE
PRIMARY APPL.	GRO, ISPM, NOSS, COBE UARS	
APPL. MODE	PERIODIC BURST INPUT, CONTINUOUS OUTPUT	
APPROX. DATE REQ.	1984	
SPECIAL	LOW POWER AND SIZE. STANDARDIZE INTERFACE	

TABLE 4–3 EXPERIMENT DATA STORAGE

A Buffer Controlled by an Experiment used to Store Large Blocks of Data Which Occur too Fast to be Transmitted Real Time to the Spacecraft Bus Mass Data Storage Units.

19–185

REQUIREMENT	SPECIFICATION	COMMENT
CAPACITY	3×10^6 BITS	10^{13} FOR SAR
ORGANIZATION	BY WORD, 8, 16, OR 32 BIT	
STORAGE ACCESS.	RANDOM ACCESS	COULD BECOME AUXILLARY COMPUTER COMPATIBLE MEMORY
I/O PORTS	SINGLE IN/SINGLE OUT	
INPUT MODE	SERIAL/PARALLEL	
OUTPUT MODE	SERIAL/PARALLEL	
READ RATE	50K – 2.0M WORD/SEC	COMPATIBLE WITH SPACECRAFT BUS RATE
WRITE RATE	50K – 2.0M WORD/SEC	
NON-VOLATILITY	NOT REQUIRED	
OPERATIONAL LIFE	2–5 YEARS	
RAD. HARDENING	REQUIRED	APPL. IS USUALLY IN UNKNOWN, HAZARDOUS ENVIRONMENTS FOR LONG MISSIONS
PRIMARY APPL.	ICEX, AMPTE, PARTICLE DETECTORS, FIELD DETECTORS, BATSE, SAR	
APPLICATION MODE	BURST OR CONTIN. IN BURST OR CONTIN OUT	THIS MEANS EVENT ORIENT RECORDING
APPROX. DATE REQUIRED	1985	
SPECIAL	IN FLIGHT TESTING OF MEMORY AND BLOCKING OUT OF BAD SECTIONS	

TABLE 4–4 HIGH RATE DATA PROCESSING BUFFER

A High-Speed Buffer to Support On-board Processing of Image Data

19–186

REQUIREMENT	SPECIFICATION	COMMENT
CAPACITY	256K TO 1M BITS	MULTIPLE BLOCKS COULD MAKE UP ACTUAL MEMORY SYSTEM
ORGANIZATION	BY WORD, 8, 16 BITS	
STORAGE ACCESS.	RANDOM ACCESS	COMPUTER COMPATIBLE
I/O PORTS	SINGLE IN/SINGLE OUT	MOST APPLS. DIRECTED AT A SINGLE SENSOR
INPUT MODE	PARALLEL	
OUTPUT MODE	PARALLEL	
READ RATE	25 M BYTES/S	
WRITE RATE	25 M BYTES/S	
NON-VOLATILITY	NOT REQUIRED	
OPERATIONAL LIFE	5 YEARS	
RAD. HARDENING	NOT REQUIRED	MODERATE LEVEL MAY BE REQUIRED ON SPECIFIC MISSIONS
PRIMARY APPL.	CCD ARRAYS ON-BOARD PROCESSING ON-BOARD DISPLAY	
APPLICATION MODE	CONTINUOUS OR PERIODIC BURST	HIGH RATE DATA INPUT LOWER RATE OUTPUT; DATA CAN BE REFORMATTED BY OUTPUT
APPROX. DATE REQUIRED	1984	

TABLE 4–5 RETRIEVABLE BUFFER

Provide Storage for Short Duration Mission Where Payload is Recoverable and Real-Time Data Transmission is not Required.

19–187

REQUIREMENT	SPECIFICATION	COMMENT
CAPACITY	10^7 – 10^{10}	
ORGANIZATION	BLOCK ORGANIZED	BLOCKS RETRIEVABLE SERIALLY
STORAGE ACCESS.	SERIAL	
I/O PORTS	SINGLE INPUT/SINGLE OUTPUT	
INPUT MODE	SERIAL	
OUTPUT MODE	SERIAL OR PARALLEL	
READ RATE	25 Kbps – 1 Mbps	
WRITE RATE	100 bps TO 4 Mbps	HIGH RATE SUPPORTS AN IMAGING SENSOR
BIT ERROR RATE	10^{-7}	
NON-VOLATILITY	REQUIRED	POWER WOULD BE REMOVED IN A PLANNED PROCEDURE
OPERATIONAL LIFE	1 YEAR	SHUTTLE FLIGHT; "GET-AWAY-SPECIAL"
RAD. HARDENING	NOT REQUIRED	
PRIMARY APPL.	SHUTTLE FLIGHTS	USE FOR DATA COLLECTION THAT DOES NOT REQUIRE REAL TIME LINK TO EARTH
APPLICATION MODE	CONTINUOUS OR PERIODIC BURST INPUT; CONTINUOUS OUTPUT	
APPROX. DATE REQUIRED	1983	

Packet Buffer (PB): The NASA Packet Data Guideline dated September 1980 defines a packet as "A block of data from a single instrument, spacecraft subsystem, or related group of instruments which contains a set of measurements along with any onboard reference or ancillary information that will be needed to analyze and interpret the source data."

The function of the PB is to create autonomous source data packets in accordance with NEEDS format specifications, and transmit them to the Packet Queuing Buffer for subsequent transmission. The source data packet format is presented in Figure 4-1.

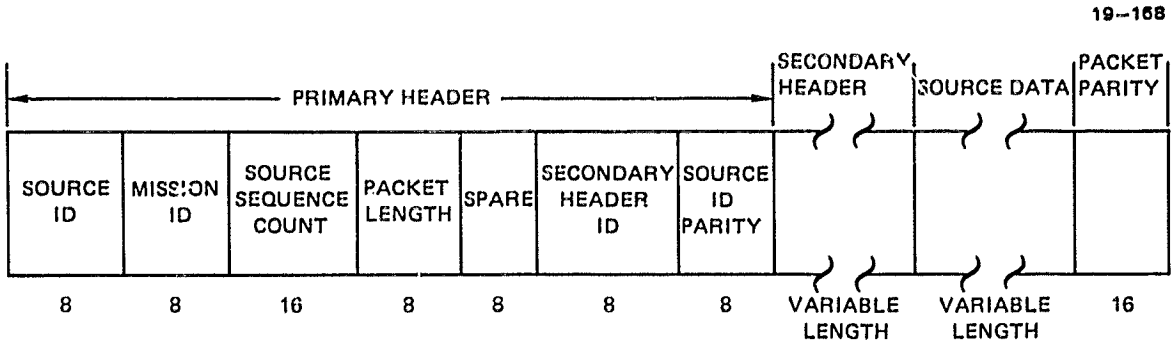

FIGURE 4--1 SOURCE PACKET FORMAT

The primary header contains eight bytes of data which serve to characterize the packet. The Source and Mission IDs, Source ID Parity, Packet Length, and Secondary Header ID are not subject to change during a mission. It is, therefore, only necessary to provide permanent, non-volatile storage for these data fields and to insert them in the proper Source Packet byte locations.

The packet length in bits is defined as:

$$L = (128 + 8M) \times 2^{E}$$

where M (4 bits) can be any integer from 0 through 15 inclusive and E (4 bits) can be any integer from 1 through 14 inclusive. This format defines 224 valid packet lengths ranging from 256 to 4,063,632 bits. The packet length includes all bits in the Primary and Secondary Headers, Source Data Field, and the optional 16 bit Error Control Parity Field. Special packet lengths may be defined by utilizing packet length code words in which E = 0 or E = 1.

The Secondary Header is composed of an even integral number of 8 bit bytes (integral number of 16 bit words). The Secondary Header ID uniquely defines the length and format of the Secondary Header. In addition to time specification to a resolution not greater than one second, this header may contain such other ancillary data as the individual mission directors deem appropriate.

Figure 4-2 depicts a PB conceptual design based upon the following assumptions:

1) Separate 8 bit parallel input ports for source and ancillary data.
2) Single serial output data port.
3) Access to system clock.
4) Source data transfer signal prior to source data input.
5) Ancillary data transfer signal prior to ancillary data input.
6) Source data bytes stored in the order in which they are received.
7) Ancillary data formatted external to PB and stored in secondary header.
8) No need to have random access.
9) Packet polling signal provided prior to reading.

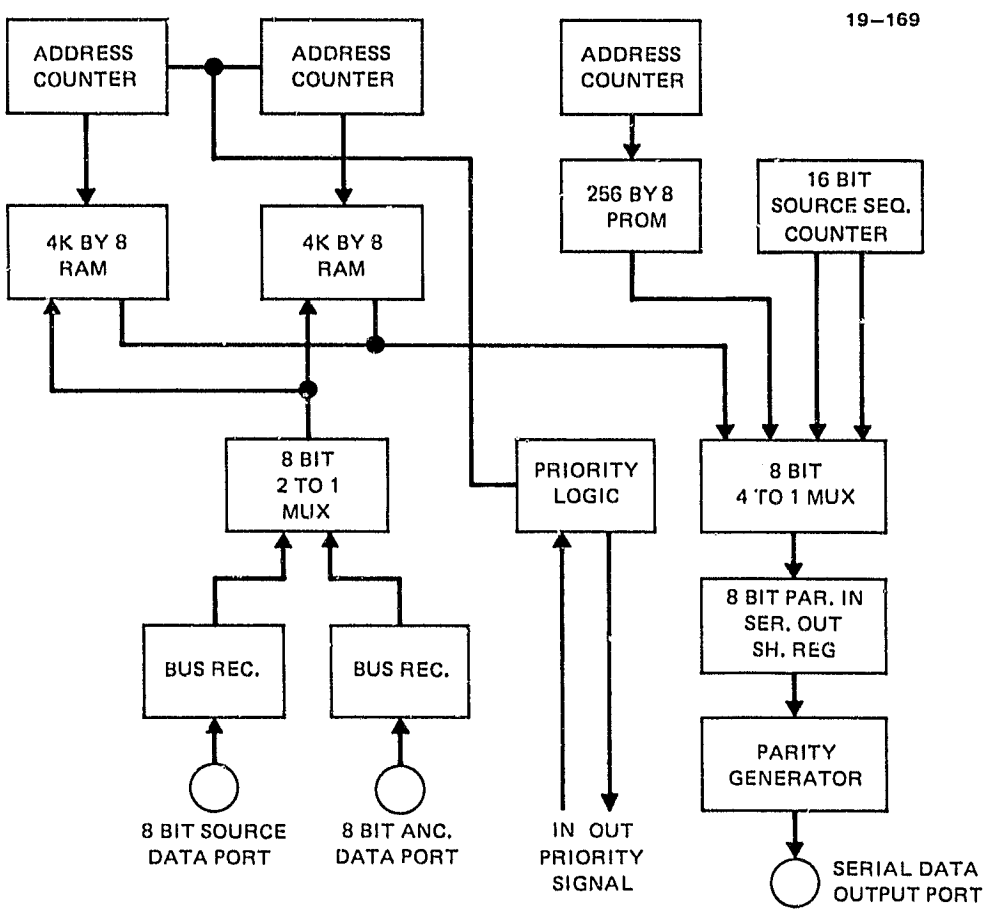

FIGURE 4-2 PACKET BUFFER CONCEPTUAL DESIGN

The 4K by 8 RAM sections in Figure 4-2 are composed of eight 4K by 1 RAMs. Separate address counters are provided to facilitate reading one section while writing into the other. Each of the address counters is a 16 bit device which will accommodate 64K by 1 RAMs when they become available. The current maximum packet length is 32K bits, but this will increase to 512K bits when 64K by 1 RAMs are employed.

In this design Packet Data are stored in ROM, RAM, the source sequence counter and the parity generating circuitry. Table 4-6 specifies the contents and storage location of each byte of the Source Data Packet. L_1, the length of the Secondary Header, is contained in ROM byte 4. This can be used to preset the RAM address counter just prior to storing source data. The only other presetting required for this counter is clearing it at the start of Ancillary Data Storage. Control signals supplied to the 8 bit 4 to 1 multiplexer in the output section of Figure 4-2 must guarantee that the order listed in Table 4-6 is maintained when the packet is read. When the RAM address counter contains the address of the last byte location reserved for source data during a storage operation a Packet Ready signal is generated. This signal is used in the Priority Determing logic circuitry. Missing control signals in Figure 4-2 are considered beyond the scope of a conceptual design.

The 16 bit source sequence counter poses a special problem. It must maintain a count (module 2^{16}) of the number of source packets generated by the specific source assembly. For this reason provisions must be made to restore its contents in case of loss thereof, or it must be made nonvolatile. Battery backup could be provided or each bit of the counter could be stored in a nonvolatile cell such as an MNOS device. For example, Xicor has announced counters in which each cell is backed up by a nonvolatile shadow cell into which the counter contents are written when the operating voltage drops below a specified value.

TABLE 4--6 SOURCE DATA PACKET MAP

19-188

PACKET BYTE	CONTENTS	STORAGE LOCATION
0	SOURCE ID.	ROM BYTE 0
1	MISSION ID.	ROM BYTE 1
2	SOURCE SEQ. COUNT	COUNTER
3	SOURCE SEQ. COUNT	COUNTER
4	PACKET LENGTH	ROM BYTE 2
5	SPARE	ROM BYTE 3
6	SEC. HDR. ID.	ROM BYTE 4
7	SOURCE ID. PARITY	ROM BYTE 5
8 THROUGH L_1 + 8	ANCILLARY DATA	RAM BYTES 0 THROUGH L_1
L_1 + 9 THROUGH L--3	SOURCE DATA	RAM BYTES L_1 + 1 THROUGH L--3
L--2	E.C. PARITY	PARITY GENERATING CIRCUITRY
L--1	E.C. PARITY	PARITY GENERATING CIRCUITRY

A comparison has been made between Gallium Arsenide and CMOS versions of the Packet Buffer. Table 4-7 is a comparison of power requirements for the functional elements which constitute the Packet Buffer. Since none of the Gallium Arsenide devices currently exist power requirements assigned to them are based upon 100 microwatts per gate. Research at McDonnell Douglas indicates that dissipation in GaAs at 10 MHz or less should be from 50 to 100 microwatts per gate and 200 to 300 microwatts per package output buffer. The fact that Gallium Arsenide requires more power than CMOS is not surprising considering the frequency of operation. At 10 MHz the GaAs dissipation would not change, while that for CMOS would increase by about a factor of five. Either approach should require about 45 dual in line packages which can be mounted on one 6 by 8 inch PC board. Volume estimate (excluding shielding and enclosure) is 24 cubic inches.

The RAM power requirements listed in Table 4-7 represent maximum operating power at 2 MB/s. In standby mode these requirements are reduced to 160 mw and 30 mw.

TABLE 4–7 PACKET BUFFER POWER COMPARISON 19–189

FUNCTION	NUMBER REQUIRED	TOTAL POWER (mw)	
		GaAs	CMOS
4 BIT BINARY COUNTER	14	105	92
DUAL 4 TO 1 MUX	4	9	4
8 BIT SH REG	3	27	8
QUAD 2 TO 1 MUX	2	6	4
8 BIT BUS REC	2	16	45
MISC QUAD GATES	15	6	45
256 x 8 PROM	1	50	50
4K x 1 RAM	16	1600	1200
TOTAL		1.8 WATTS	1.5 WATTS

Table 4-8 is a comparison between this design and the model supplied by the NASA. Deviations of design characteristics from those of the model are discussed below.

TABLE 4–8 PACKET BUFFER CHARACTERISTICS COMPARISON

19–190

CHARACTERISTIC	MODEL	DESIGN
CAPACITY (BITS)	4K	32K
STORAGE ACCESSIBILITY	RANDOM ACCESS	SEE TEXT
INPUT/OUTPUT PORTS	TWO	THREE
INPUT/OUTPUT MODES	UNSPECIFIED	PARALLEL/SERIAL
READ RATE	1 Mb/s	2 M BYTES/SEC
WRITE RATE	1 Mb/s	2 Mb/s
NON-VOLATILITY	NOT REQUIRED	NOT PROVIDED
RADIATION HARDNESS	REQUIRED	SEE TEXT
WEIGHT	1 POUND	1.2 POUNDS
VOLUME	36 CU. IN.	24 CU. IN.
POWER	0.5 WATT	1.8 WATTS
ORBITAL LIFE	5 YEARS	SEE TEXT

The capacity was changed to 32K bits to facilitate working with bytes (8 bits) of data from the input ports. CMOS byte wide RAMs are not as plentiful as the 4K by 1 devices. Because failures in RAMs tend to affect all bits in a package, error detection capability is enhanced by storing only 1 bit of a data word in any single RAM package. Since 4K by 1 CMOS RAMs are currently available and Gallium Arsenide versions are projected by 1983, 4K byte storage is provided by using 8 packages. The RAM address counters are 16 bits wide to accommodate 64K by 1 RAMs when they become available. This will expand the capacity of the Packet Buffer to 512K bits.

Consistent with anticipated usage of the Packet Buffer it was decided that random access was not required. To incorporate this feature it would be necessary to provide 12 address lines along with suitable decoding circuitry for the present capacity. Naturally the address requirements will be compounded if larger capacity RAMs are employed.

Total dose radiation hardness of 10^5 Rads (Si) is reported for CMOS by J. P. Spratt of Questron, while R. Zuleeg of McDonnell Douglas reports that Gallium Arsenide exhibits negligible degradation of performance after 10^7 Rads (GaAs) total dose.

The weight estimate of 1.2 pounds (550 grams) is based upon using 45 integrated circuit packages mounted on a 4 layer fiber-glass printed circuit board. Detailed estimates are:

Housing	200 Grams
Populated P.C. Board	250
Connector	20
Hardware	15
Wire	15
Tolerance	50

Two factors contribute to the power variance in Table 4-8. The capacity has been increased by a factor of 16 and the 1.8 watt figure represents the maximum operating power at 2 million read or write operations per second with 100 percent duty factor. During a read operation the duty cycle of the RAMs is 12.5 percent. Therefore, one 32K RAM section dissipates 160 mw 87.5 percent of the time and 800 mw the other 12.5 percent. This averages to 240 mw (compared to 800 mw with 100 percent duty factor). The total power could be reduced to 1.24 watts.

TABLE 4–9 PACKET QUEUING BUFFER COMPARISON

CHARACTERISTIC	MODEL	DESIGN
CAPACITY	10^7 BITS	8×10^6 BITS
ACCESS	BORAM	BORAM
I/O PORTS	MULTIPLE	MULTIPLE
I/O MODE	SERIAL	SERIAL
READ RATE	1 Mbit/sec	1 Mbit/sec
WRITE RATE	1 Mbit/ sec	1 Mbit/sec
RADIATION HARDNESS	REQUIRED	SEE TEXT
WEIGHT	9 POUNDS	7.5 POUNDS
VOLUME	330 IN^3	220 IN^3
POWER	25 WATTS OP. 1 WATT ST. BY	SEE TEXT
ORBITAL LIFE	5 YEARS	SEE TEXT

19–191

Packet Queuing Buffer (PQB): After the source data packets have been created in the PBs or in packet forming logic associated with "intelligent" instruments they must be stored in a queue for subsequent transmission. The packets must be imbedded in specific sized data packages called Transport Frames.

Synchronization and control data are a part of each frame. Depending upon the source packet and frame sizes a frame may contain an entire source packet, a fraction thereof, or multiple source.

According to the Aerospace Data Standard on PCM Telemetry (Document No. 560-63-2) the Transport Frame length must not exceed 8,192 bits. This is referred to as a minor frame. A source data packet which requires more than one minor frame is transmitted via a contiguous group of transport frames called a major frame. According to the above document a major frame may not contain more than 256 minor frames. This implies a maximum source data packet length of 2,097,152 bits.

As shown in Figure 4-3 the Transport Frame contains a Frame Header, a Status Insert Field, the Source Packet(s), and a Frame Parity Field. The 24 bit Synchronization Code and the 8 bit Frame ID field contain data which will not change during a mission. They should, therefore, reside in non volatile memory.

19-170

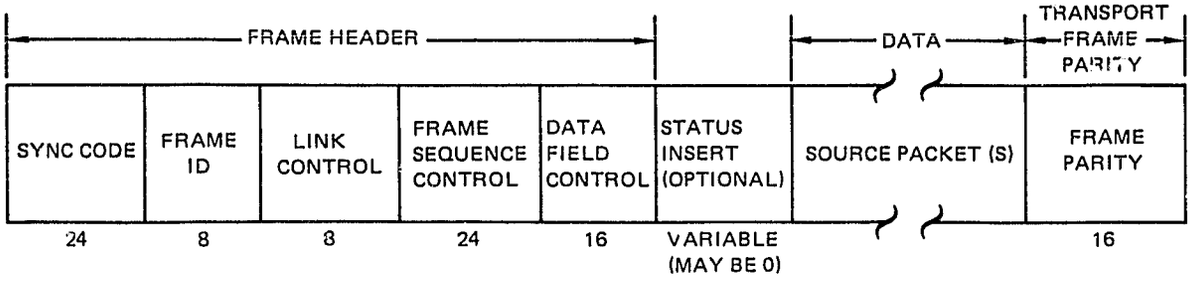

FIGURE 4-3 TRANSPORT FRAME FORMAT

The PQB described by Table 4-2 is a Block Oriented RAM (BORAM) with maximum capacity of 10^7 bits. The table does not completely define the PQB. For instance, the frame forming logic is not mentioned, nor is the fact that simultaneous reading and writing are required.

Magnetic Bubble technology was selected for the conceptual design of the PQB because it is BORAM by nature and can be made to operate at the required data rate. The memory chips have sufficient radiation tolerance to withstand the 200 K Rad total dose specified in Table 4-2. However, the support chips and control circuitry may require shielding. The design is based upon the Intel 7110 1 M Bit Magnetic Bubble Memory chip and the associated family of integrated circuit support devices. National Semiconductors, Texas Instruments, and Rockwell all plan to introduce competitive devices in the near future.

Figures 4-4 and 4-5 represent the conceptual design of the PQB. The input (Figure 4-4) and output sections share a common data bus. The dual sections are necessary to provide the capability to read and write simultaneously. Details of the 4 M bit storage modules are provided by Figure 4-6. As indicated in part (a) of the figure, one controller handles all four memory chips, but the other support chips must be replicated in each cell.

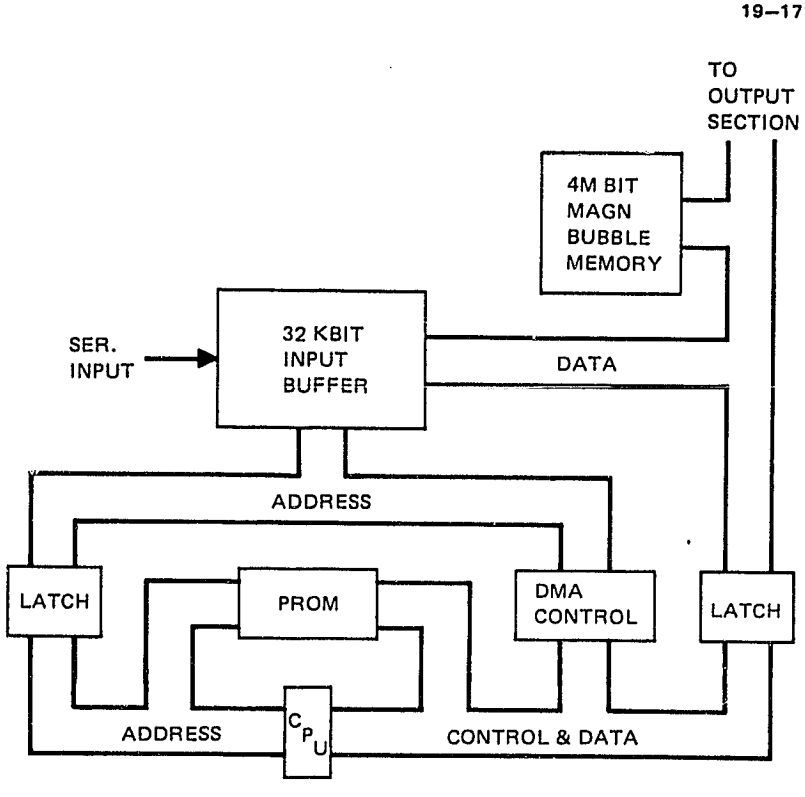

FIGURE 4–4 PACKET QUEUING BUFFER INPUT

The configuration shown in Figure 4-6 yields 2048 pages of 2048 bits each. This will allow 1024 packets of 4096 bits each to reside in the queue provided by one section of the PQB. Operating four bubble chips in parallel provides a nominal data rate not greater than 544 K bits per second, but this is not a problem since input and output buffers (to be described later) are provided. The operating (100% duty factor)/standby power requirements for each 4 M bit section are 20 watts and 3.7 watts respectively.

19--172

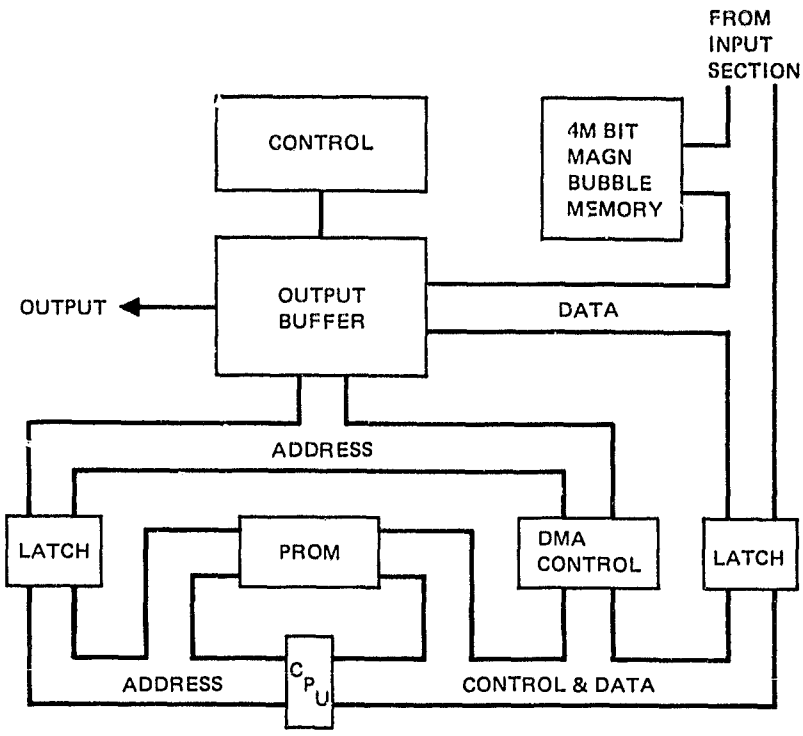

FIGURE 4--5 PACKET QUEUING BUFFER OUTPUT

19--173

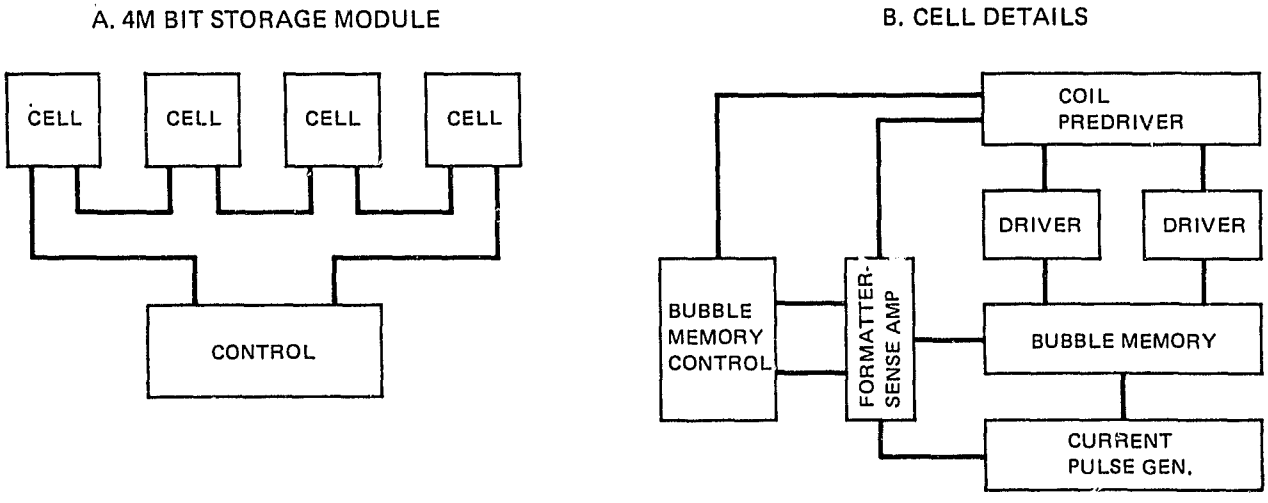

FIGURE 4--6

The input buffer shown in Figure 4-4 is a duplicate of the storage portion of the P.B. This will accommodate the 2 M bit writing rate specified in Table 4-2 and the 544 K bit rate discussed above. Dual port RAMs in this section are controlled by the microprocessor (CPU) for loading and by the CPU and Direct Memory Access (DMA) control device for transferring their contents to the appropriate section of the PQB.

In order to store the source packets in the queue according to the relative priority of the data which they contain, some sort of definite ordering scheme is required. It is possible for the PB control circuitry to signal the PQB when a packet is ready. Alternatively the PQB could poll the PBs via a schedule defined by the relative urgency of the data. The latter approach has been chosen for this design. The following discussion refers to the arrangement shown in Figure 4-7.

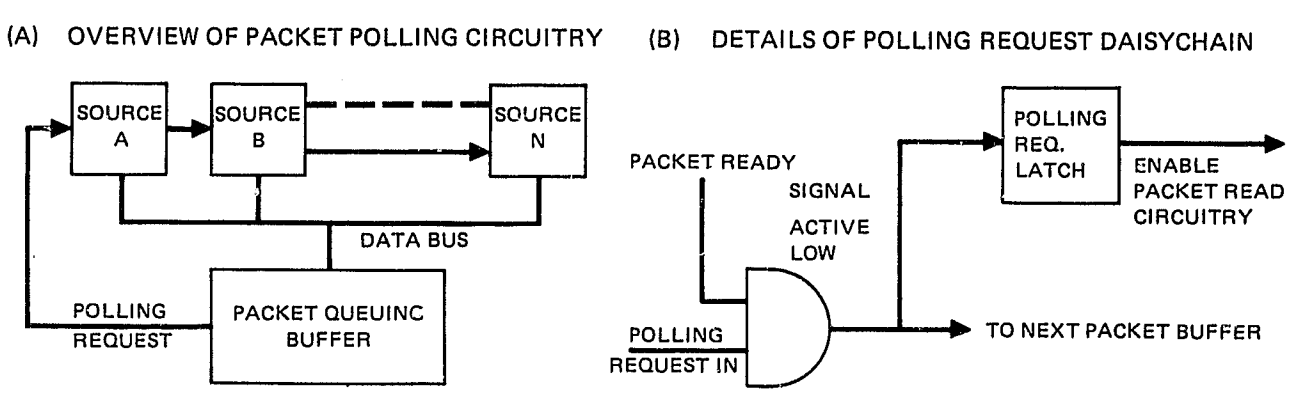

FIGURE 4–7 PACKET BUFFER POLLING SCHEME

The PQB periodically issues a polling request which is active high. If source A (highest priority) does not have a source data packet ready to be placed in the queue its packet ready signal will be high (inactive) and the polling request will be forwarded to the source with the lower priority.

If source A has a packet ready for transfer the polling request will not be forwarded to any sources with lower priority. The polling request latch will activate the necessary circuitry to accomplish the data transfer between the PB and the PQB input buffer. If a PB has a data packet ready for transfer to the queue, it will gain access to the data bus when, and only when, a polling request is received and no PB with higher priority has a packet ready for transfer.

The control circuitry shown in Figure 4-5 must perform the following functions:

1) Provide a binary count (modulo 2^{24}) of the number of minor frames which have been transmitted. As in the case of the source sequence counter (see discussion of PB) this must be non volatile.
2) Generate the Data Field Control Field. This uses bit 0 as a last frame flag while bits 1 through 15 provide a nonvolatile binary count (modulo 2^{15}) of source packet segments.
3) Accept data for Link Control and Status Insert Fields from the C and DH facilities and provide storage for these.
4) Provide nonvolatile storage for the synchronization code and frame ID.
5) Assemble all of these in the correct order along with the source data packet to create a transport frame.
6) Generate the frame parity field as the final 16 bit field of the frame.

The design of the control circuitry and the polling strategy are mission dependent. Accurate estimates of power, weight, and volume requirements are thus not possible. It is reasonable to assume, however, that for missions utilizing not more than five non-imaging instruments the necessary MSI and LSI components could be mounted on one 6 x 8 inch card.

The transport frames are stored in the output buffer to await transmission. Given that the maximum frame size is 8,192 bits, a 32K dual port RAM buffer would hold 4 frames. This should provide adequate buffering between the 544 K bit data rate of the magnetic storage and the desired 1 to 2 M bit per second PQB output data rate. Figure 4-8 depicts the PQB output section.

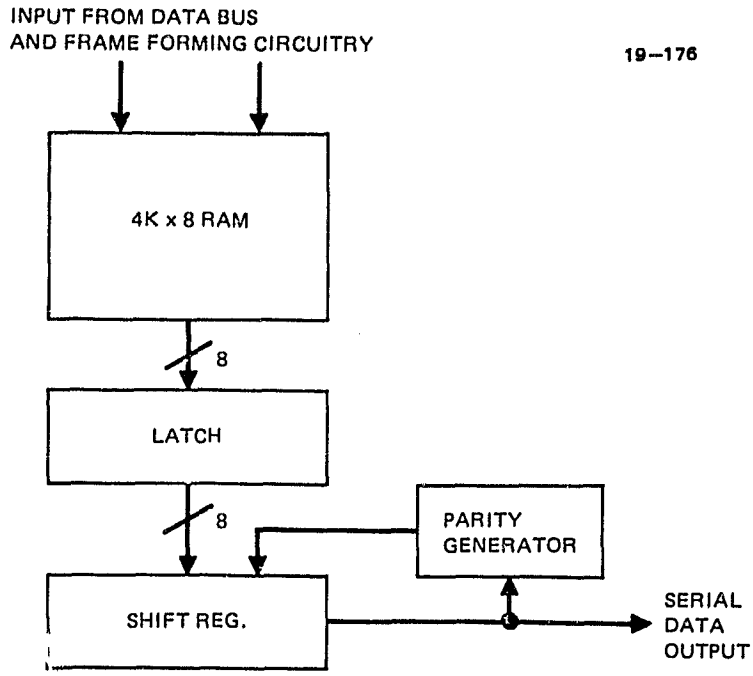

FIGURE 4–8 PQB OUTPUT BUFFER

Table 4-9 is a comparison of this design with the model supplied by the NASA. Deviations of the design characteristics from those of the model are discussed below.

The PQB capacity given in the original application (Table 4-2) was 10^4 - 10^7 bits. Eight megabits capacity was selected because it allows a convenient and efficient utilization of existing hardware. Four megabit bubble memory chips will expand the capacity to 3.2×10^7 bits with minimal redesign effort.

As indicated previously, the magnetic bubble devices can easily tolerate the 200 K Rad total dose listed in Table 4-2. The support chips and control circuitry may require shielding.

Intel reports the weight of the 1 M bit bubble chip to be 100 grams. Allowing 10 grams each for the support chips which are required (see Figure 4-6) yields 410 grams for the 41 pieces. Each 4 M bit section requires a 6 by 8 inch printed circuit board which weighs about 180 grams. The two populated 4 M bit boards should weigh a total of 1600 grams.

The control circuitry, input buffer, and output buffers should require no more than 3 additional populated 6 by 8 inch cards at 250 grams each. Thus, the total weight of the 5 cards is estimated at 2650 grams. Allowing 600 grams for housing and 100 grams for connectors, hardware, and wiring yields a total weight of 3350 grams (7.37 pounds) excluding shielding and power supply.

Estimating the power required is difficult because the total number and type of logic functions are unknown. Assuming that each of the three non storage boards requires about 1.2 watts yields operating/standby power requirements of 43.6 and 11 watts respectively.

The orbital life of 5 years should be no problem provided that a reliable technology is used to design the control and interface circuits.

It is strongly recommended that the NASA pursue the development of the PQB. If CMOS or GaAs devices can be employed to perform the control and interface logic the power requirements can probably be reduced from those listed herein. The prospect of 4 M bit bubble memory chips and appropriate support chips is a further reason to develop this concept.

Experiment Data Storage Buffer (EDSB): This buffer provides storage for large blocks of data (from an experiment) which would exceed the spacecraft bus data rate if real time transmission were attempted. For example, a requirement exists for writing 600 thousand 32 bit words per second. The data are transmitted to the Spacecraft Mass Data Storage via the spacecraft bus at a typical rate of 1 M bit per second. Since it is anticipated that this buffer will also serve as auxillary storage for on board data processors, random access by word is required. Table 4-3 lists the characteristics of the Experiment Data Storage.

The combination of 3M bit capacity, 180 cu in volume, 4 pounds weight, and radiation hardening listed in the model EDSB strongly suggest hybrid memory packages. It is recognized that problems may exist regarding space qualifications, but the largest currently available CMOS RAM chip has 4K bit capacity. For example, 3M bits composed of 4K devices mounted two per square inch of board space would require a volume of 192 cu in without any allowance for interface and control circuits.

Figure 4-9 depicts the suggested architecture of a 32K by 2 hybrid composed of sixteen 4K by 1 static RAMs. To satisfy power and radiation hardness guidelines CMOS and Gallium Arsenide versions will be compared. A package of sufficient size to accommodate 16 individual chips occupies 2 sq in of board space with room for 40 pins. As shown in Figure 4-9 the individual chips are selected in pairs.

Three address lines must be decoded to activate 1 of the 8 chip select lines. These three lines coupled with the 12 lines connected to the individual chips provide the 32K unique addresses required.

It is suggested that 16 hybrids be mounted on a 6 by 8 inch printed circuit board. In this manner 32,768 words can be stored on each board. Three boards provide the suggested 3M bit storage capacity, but a minimal increase in address decoding complexity will accommodate 4 Mbits, the capacity upon which this design is based.

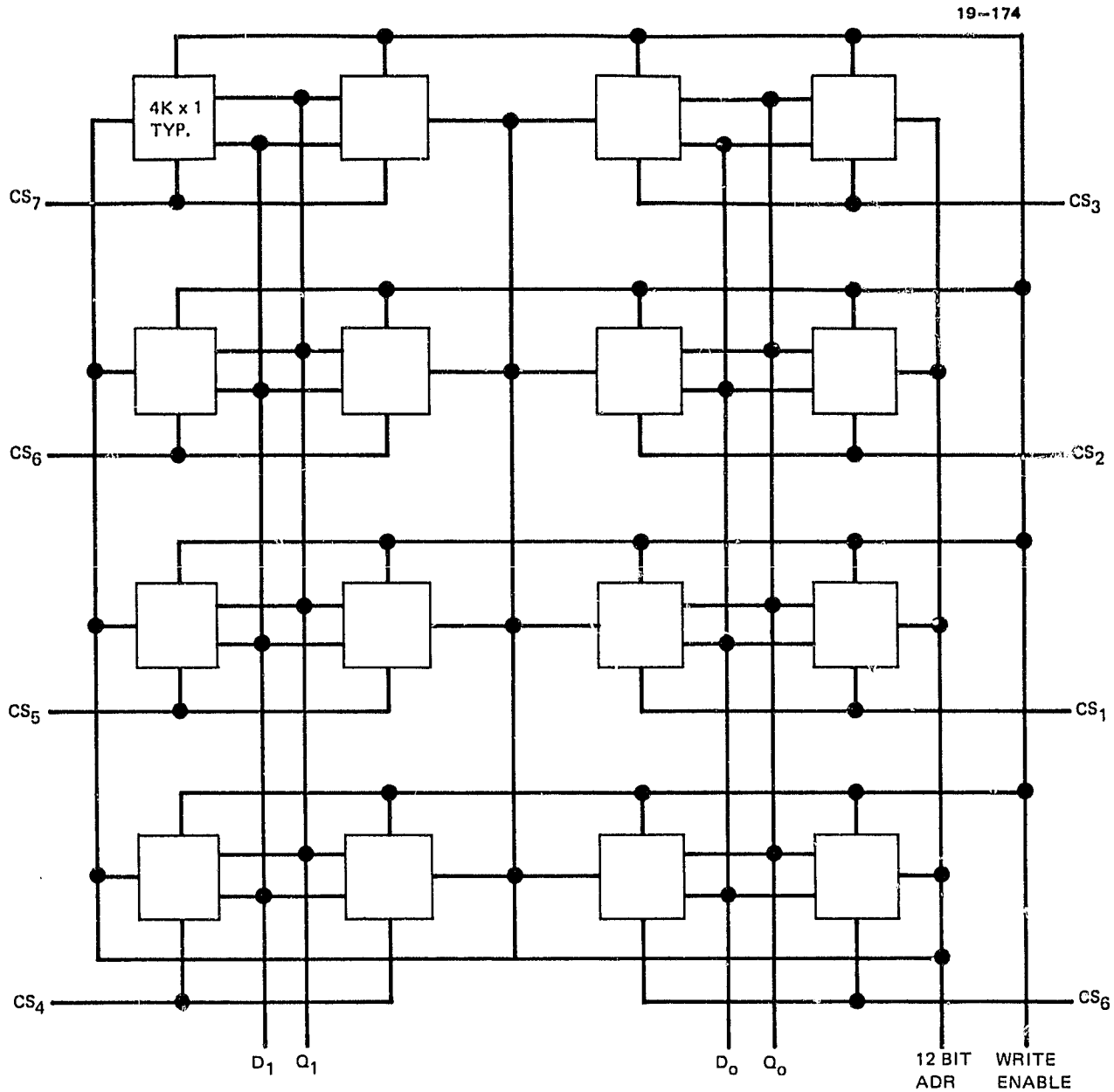

FIGURE 4--9 SUGGESTED ARCHITECTURE OF 32K BY 2 HYBRID MEMORY

Given a 32 bit input data port and data rate of 600K words per second, a variety of writing schemes exist. Since the RAMs dissipate less power in the standby mode than when they are active, total power requirements may be eased by reducing the number of bits involved in each write operation. Memory write cycle time must be consistent with the multiple operations involved, and addressing smaller groups of bits requires more complex decoding circuitry.

The minimum address requirement is 17 bits, 12 of which are decoded on the individual RAM chips. This assumes 32 bits written in parallel. For CMOS RAMs the operating/standby power requirements are 75 mw/0.4 mw and write cycle time is 600 ns. Writing two 16 bit segments for each input word would require 1200 of the 1667 ns available. RAM power requirements would be reduced from 2.8 watts to 1.6 watts at the expense of decoding one extra address bit.

According to Zuleeg GaAs RAMs will have a 12 ns write cycle time with operating/standby power dissipation of 100 mw/10 mw. Power reduction achieved by reducing the number of active chips is not as dramatic as with CMOS devices because of the relatively high standby power requirement. Writing 16 bit segments in GaAs reduces dissipation from 13.1 watts to 11.7 watts. The 12 ns write cycle time would permit writing 16 two bit segments per word. However, the 4M bit system would still dissipate 10.4 watts and it would be necessary to decode 9 address bits.

The upshot is that GaAs is not as attractive as CMOS in this application unless a premium is placed on the increased radiation tolerance. However, the scheme discussed in the preceding paragraph would facilitate writing four million 32 bit words per second.

Because of the excessive power requirements GaAs is not suggested for this application. The conceptual design is based upon 64K CMOS hybrids.

Reading is accomplished by transferring sixteen bits of data from the appropriate RAMs to a shift register driven by a 1 MHz clock.

Figure 4-10 depicts a conceptual design of the Experiment Data Buffer. Table 4-10 is a comparison of the model supplied by the NASA and the design discussed in this report.

19-175

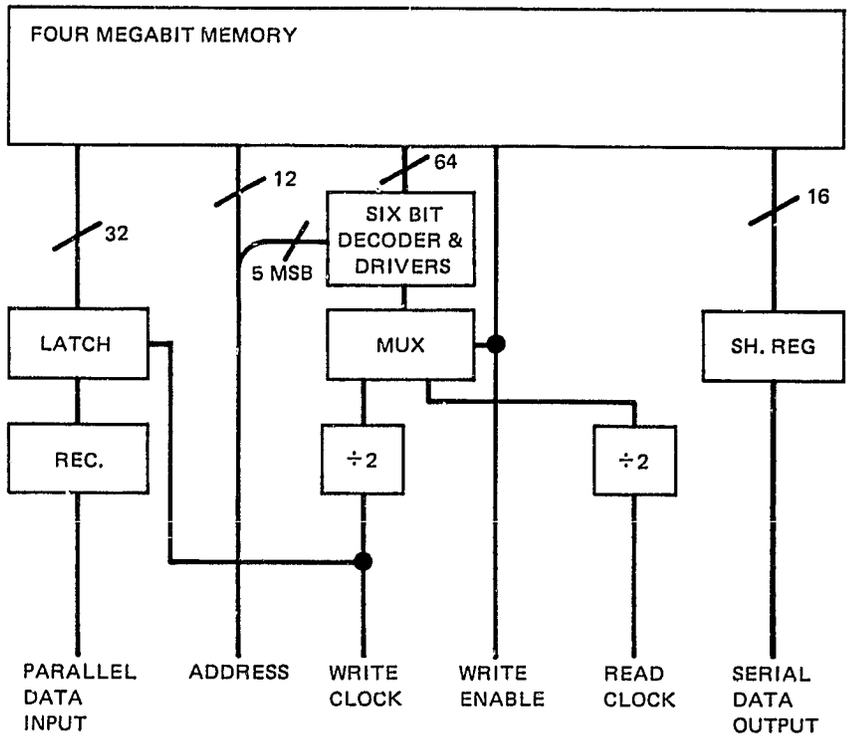

FIGURE 4–10 EXPERIMENT DATA BUFFER CONCEPTUAL DESIGN

TABLE 4–10 EXPERIMENT DATA BUFFER COMPARISON

19–192

CHARACTERISTIC	MODEL	DESIGN
CAPACITY (BITS)	3×10^6	4×10^6
ACCESSIBILITY	RANDOM ACCESS	RANDOM ACCESS
INPUT/OUTPUT PORTS	SINGLE/SINGLE	SINGLE/SINGLE
INPUT/OUTPUT MODE	PARALLEL/SERIAL	PARALLEL/SERIAL
READ RATE	1 Mb/Sec	1 Mb/Sec
WRITE RATE	600K WORDS/SEC 32 BIT WORDS	SAME AS MODEL
NON-VOLATILITY	NOT REQUIRED	NOT PROVIDED
RADIATION HARDNESS	REQUIRED	10^5 RADS TOTAL
WEIGHT	4 POUNDS (PLUS SHIELDING)	5.8 POUNDS
VOLUME	180 CU. IN.	168 CU. IN.
POWER	5W OPERATING 1W STANDBY	1.8W OPERATING 0.65W STANDBY
ORBITAL LIFE	5 YEARS	5 YEARS

The weight estimate of 5.8 pounds (2640 grams) is based upon using five 4 layer 6 by 8 inch fiberglass printed circuit boards. Detailed estimates are:

Four memory boards @ 420	1680 Grams
Control logic board	250
Housing	400
Connector	30
Hardware	20
Wire	20
Tolerance	240
Total	2640 Grams

High Data Rate Processing Buffer (HDRP): To reduce the volume of data which must be transmitted via the down-link it is desirable to process data on board the spacecraft. A requirement therefore exists for a dedicated buffer with read-write rates in the vicinity of 25 magabytes per second. One application is radiometric calibration using CCD detectors. Parameters such as constants associated with gain and offset must be stored. Dynamic parameters (e.g., the dark current of a CCD) dictate read-write capability.

The nature of the storage and retrieval operations involving the HDRP is such that random access is not necessary. Typically the entire memory contents are involved in each transfer of data. This permits a serial addressing technique. It also eases the problems associated with the high data transfer rate.

Table 4-4 lists the characteristics desired in the HDRP. Table 4-11 is a comparison of a model HDRP supplied by the NASA and a conceptual design based on Gallium Arsenide. GaAs was selected because of the anticipated 12 ns cycle time, its radiation tolerance and low power requirements.

The GaAs conceptual design is given by Figure 4-11. The cycle time of this technology is short enough to allow direct storage and retrieval without resorting to interleaving tactics. The address counter must be driven by the same clock which controls the data transfer.

TABLE 4–11 HDRP COMPARISON

19–193

CHARACTERISTIC	MODEL	DESIGN
CAPACITY	10^5 BITS	1.28×10^5 BITS
ACCESSIBILITY	SERIAL	SERIAL
I/O PORTS	SINGLE	SINGLE
I/O MODE	8 BIT PARALLEL	8 BIT PARALLEL
READ RATE	40 ns/BYTE	40 ns/BYTE
WRITE RATE	40 ns/BYTE	40 ns/BYTE
NON-VOLATILITY	NOT REQUIRED	NOT PROVIDED
RAD. HARDNESS	REQUIRED	10^7 RADS (GaAs) TOTAL
WEIGHT	1.5 POUNDS	2 POUNDS
VOLUME	130 IN^3	80 IN^3
POWER	17 WATTS	4.64 WATTS
ORBITAL LIFE	5 YEARS	SEE TEXT

19–177

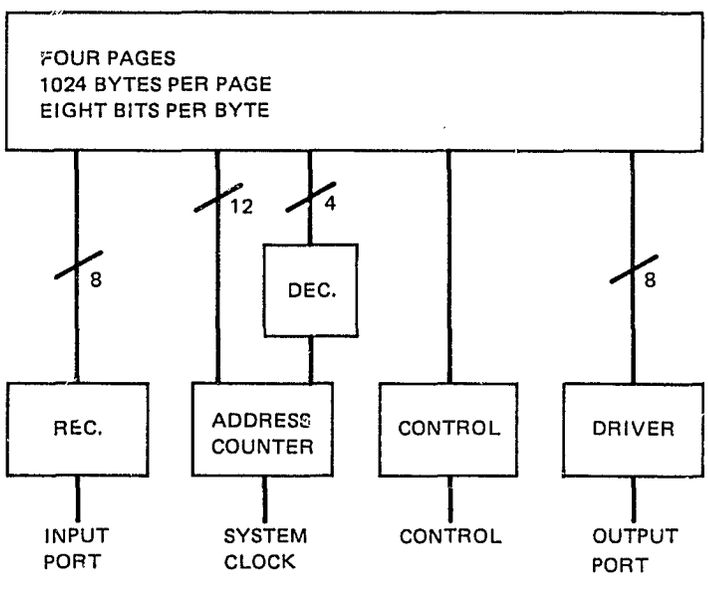

FIGURE 4–11 HIGH DATA RATE PROCESSOR CONCEPTUAL DESIGN

The storage section of the HDRP is composed of thirty two 4K by 1 RAMs. Each RAM stores only one bit of each of 4096 bytes. Thus 8 memory chips are involved with each read or write operation. Twelve of the outputs of the address counter are decoded on the RAM chips. The other two are decoded to produce four page address signals. The address counter is simply cleared at the beginning of a storage operation and then sequentially advanced by the system clock. If the entire memory capacity is not utilized, the address counter contents can be stored when the last byte is written. Subsequent read operations can then be terminated without involving unused byte locations.

GaAs memory devices will be TTL compatible. Thus the non storage circuit elements in the HDRP can be bipolar. No significant power penalty results from this approach because the memory devices far outnumber these packages. In the near term time period (1982 to 1987) the non storage elements will have to be bipolar or CMOS. The latter will not support the 25 megabyte data transfer rate.

Total operating power requirements are 4.64 watts; 800 mw for 8 active RAMs, 240 mw for 24 RAMs in standby mode, and an estimated 3.6 watts for the bipolar devices. Standby power is 3.92 watts because the RAM power requirements are reduced by 720 mw.

The components can easily be mounted on two 6 by 8 inch cards requiring a volume of 80 in^3 exclusive of power supply. Estimated weight is 920 grams (2 pounds).

Increasing the capacity of the HDRP to 1 Mbit (128K bytes) can be accomplished by using 128K RAMs and absorbing a minimal increase in control circuitry. Estimated consequences are: operating/standby power requirements increased to 7 watts/6.28 watts, volume increased to 160 in^3, and weight increased to 1450 grams (3.2 pounds).

A CMOS version of the HDRP can be designed using 2K by 8 RAMs. Since the cycle time of these devices is about 120 ns direct reading and writing cannot be employed. Some form of interleaving is required.

One approach is to terminate each data input line at the input to an 8 bit shift register. When 8 bytes of input have been received the contents of the shift registers can be transferred to 8 bit latches which serve as sources for the RAM input buses. Each 8 bit latch would communicate with the 8 data input lines of 1 RAM, thus, the combination of eight 8 bit shift registers, eight 8 bit latches, and eight 2K by 8 RAMs will accommodate 16K bytes during the write operation. The latches and RAMs will operate with 320 ns cycle time if the data rate is 25 M bytes per second. The shift registers and latches will have to be bipolar because CMOS cannot operate at 25 MHz. Similar latch and shift register combinations must be provided for reading.

The capacity of this version can be expanded in integer multiples of 16K bytes by adding groups of eight 2K by 8 RAMs and increasing the complexity of the addressing and control circuitry.

Hitachi supplies a 2K by 8 CMOS RAM for which they report 120 ns cycle time and operating/standby power requirements of 400 mw/75 mw. NEC and Toshiba are listed as second sources.

A 128K HDRP using CMOS storage devices and a mixture of CMOS and bipolar control and interface circuitry should require an operating power of about 7.5 watts. Volume, weight, and development cost should not differ greatly from those of the GaAs version discussed above.

Retrievable Buffer (RB): Table 4-5 lists the requirements for a retrievable buffer. The anticipated application of this device is the collection of data which do not require a real time link to earth. One example is recording data on space shuttle flights.

The major difficulty associated with the requirements of the RB is the 10^{10} bit capacity. The only technology which offers any significant change to provide 10^{10} bits storage capacity within the next five years is Magnetic Tape Recording.

The closesest competitor to Magnetic Tape for this application is the Optical Disc. Unfortunately this is an emerging technology. Experimental models have demonstrated the required data rate and storage density, but no production units exist. RCA and Phillips are the major investigators of this technology. Neither company has announced a reliable production version of a laser diode.

Reliable laser diodes are an absolute necessity if optical disc recorders are to be flown aboard spacecraft. The volume and power requirements of gas lasers make them totally unsuitable. Larry Miller of Phillips Laboratories feels that the work being done at their Eindoven facility will lead to production units by 1983. Details of their laser diode operation are considered proprietary. Donald Herzog of RCA feels that laser diodes with 10K hour lifetime priced at about $1K each in small quantities will be available within two years.

Much of the impetus behind the research efforts by RCA and Phillips is the potential market for commercial and consumer devices. If any flight qualified units are to be developed, considerable financial support will be required. For instance, Herzog feels that such a program would require two to three years.

Mark Goldberg of NSA has been working with an Optical Disc recorder which has a 5 M bit data rate and 10^{10} bit capacity. He feels that these devices are potentially less reliable than Magnetic Tape recorders because they require mechanical servo systems which are more numerous and more complex.

NSA is interested in Optical Disc recorders for ground based mass storage because access time to a block of data is much less than that of Magnetic Tape recorders with similar capacity. The improvement in storage density will ease the problem of archival data storage.

Figure 4-12 depicts the potential use of the five conceptual designs which have been presented. Clearly this is not a known spacecraft system. It is presented as an aid to understanding how the individual buffers and spacecraft hardware interact to form a complete system.

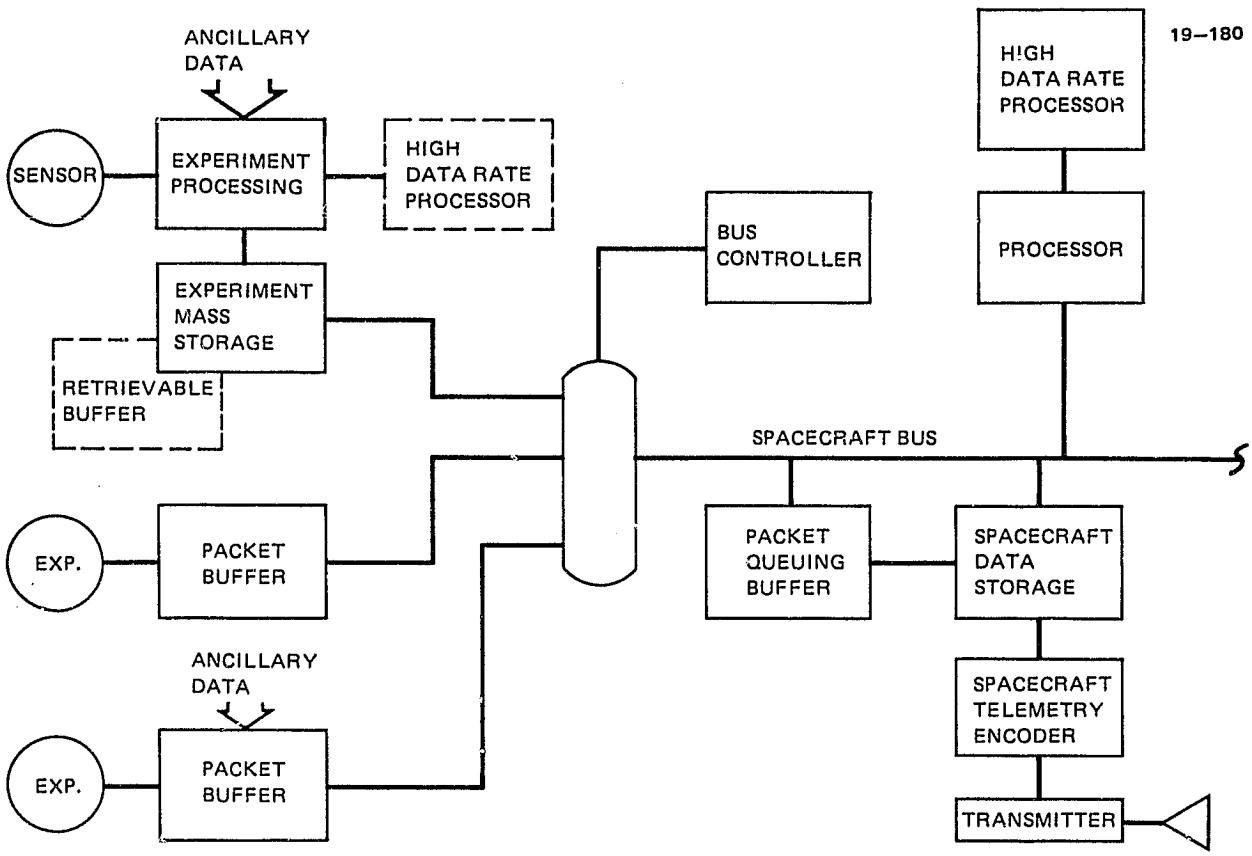

FIGURE 4–12 CONCEPTUAL USE OF BUFFERS

APPENDIX

GENERAL DISCUSSION OF SELECTED MEMORY TECHNOLOGIES

SEMICONDUCTOR MEMORIES

The class of semiconductor memory devices may conveniently be further divided into Bipolar, Metal-Oxide-Semiconductor, and Other Technologies. These will be briefly discussed.

BIPOLAR

The Bipolar subgroup includes Transistor-Transistor Logic (TTL), Emitter Coupled Logic (ECL), and Integrated Injection Logic (I^2L). Still another Bipolar technology is the so called I^3L which is actually a variation of I^2L.

Bipolar memory devices include RAM's, ROM's, and PROM's. Because of difficulties in scaling the individual transistors, bit densities are less than those of competing technologies such as MOS. TTL and ECL require the same power to store data as to alter their contents. This imposes a penalty on the devices in applications where it is necessary to minimize operating power. The advantages of Bipolar memory devices are high speed operation and radiation tolerance.

Bipolar technology is mature. Little research effort is indicated in the literature. Efforts to increase bit density will continue but research appears to be concentrated on increasing operating speed. For example National Semiconductor predicts a 64K static RAM within 10 years and a 4K 5ns device by 1987.

During the IEEE Solid State Circuits Conference in 1979 IBM announced the development of a 64K (8K by 8) bipolar dynamic RAM. Cycle time was reported to be 200 ns. Using a 2.5 μm lithography provides density comparable to MOS (315 μm^2 per cell).

MOS

The Metal-Oxide-Semiconductor (MOS) family of technologies includes P and N channel (PMOS and NMOS), complimentary MOS (CMOS), Metal-Nitride-Oxide Semiconductor (MNOS), Floating Gate, and Charge Coupled Devices (CCD). A majority of the solid state memory devices currently available are manufactured using the technologies of this family. Major research effort over the past five years has been directed at increasing bit density, reducing power, and increasing speed. Apparently these efforts will continue along with an attempt to improve the radiation tolerance. Limited radiation hardness is the chief disadvantage of MOS devices as they presently exist. A brief discussion of the current status of each MOS technology follows:

PMOS and NMOS devices are unipolar, i.e., only one type of charge carrier is involved in the conduction process. For PMOS the charge carriers are holes, while electrons are the carriers in NMOS. NMOS devices are easier to interface to TTL logic levels, possess superior speed-power products, and require less silicon area (for a given operating speed) than PMOS. For these reasons research activity has concentrated on NMOS. Very few PMOS memory devices are available.

16K NMOS RAM's are available from several sources. Cycle times as low as 70 ns are reported. Power requirements are typically 0.2 mw per bit in the operating mode and 0.03 mw per bit in standby. This reduced power in standby mode is possible because operating voltage can be removed from the non-storage circuit elements on the chip and the storage elements can maintain data at reduced voltage. Full operating voltage is required only when the contents are being read or altered. 64K Dynamic RAMs have been introduced by several suppliers including Texas Instruments. For example TI's TMS 4164 is reported to have a cycle time of 250 ns and power requirement of 200 mw (3 μw per bit). The refresh period is 4 ms. 64K NMOS ROMs are also available.

CMOS

Two CMOS technologies currently exist, bulk silicon and silicon-on-sapphire (SOS). SOS devices exhibit lower values of leakage current than their bulk silicon counterparts because the area between devices acts like an insulator rather than a reverse biased diode. SOS also promises greater packing density than bulk silicon. The greatest advantage of SOS over bulk silicon is, however, a potential speed advantage resulting from the reduced parasitic capacitance losses as a consequence of the insulating (sapphire) substrate. Processing difficulties have prevented SOS devices from developing at the rate predicted in 1975. Most suppliers have discontinued or severely curtailed CMOS SOS activity.

In spite of the fact that Bulk silicon CMOS memory devices exhibiting total dose radiation tolerance of 10^6 Rads (Si) have been reported in the literature, typical specifications for hardened CMOS memories (for example Harris HS-6551RH) indicate total dose tolerance of $2x10^4$ Rads (Si). No radiation hardened CMOS/SOS memory devices are currently available.

The largest CMOS memory device available today is the Harris HM5-6564. It is actually a hybrid of 16 4K by 1 memory chips which offers a choice of 8K by 8 or 16K by 4 organization. Access time is under 350 ns while operating and standby power requirements are reportedly 300 mw and 5 mw respectively. Harris also provides mask programmable CMOS ROM's with 64K capacity and access time of 550 ns over the full military temperature range.

MNOS

MNOS transistors differ from the conventional MOS devices in that a layer of silicon nitride lies between the gate and the silicon dioxide gate dielectric material. With a sufficiently thin oxide layer, it is possible to electrically insert or remove charge from traps in the nitride near the nitride-oxide interface. Stored charge is retained for long periods of time in the absence of operating voltage. Thus the MNOS device is a non-volatile storage cell. Stored information is represented by two distinct levels of threshold voltage corresponding to the presence or absence of stored charge.

Repeated switching of an MNOS transistor affects its ability to store charge. The "endurance" of an MNOS transistor is a parameter relating the number of erase-write cycles to the time during which data may be retained. Westinghouse claims that their BORAM 6008 MNOS memory chip will retain data for more than 10 years with 10^7 accumulated erase-write cycles. The 6008 is organized as 256 words of 32 bits each.

The primary disadvantage of MNOS memory devices is the relatively slow speed operation. For example, the Westinghouse BORAM 6008 requires 200 μs to erase (the entire chip or 128 cells), and 50 μs to write 32 bits. The maximum rate at which data may be read is 200 K bits per second. Power dissipation is reported to be less than 400 mw.

Radiation tolerance of the 6008 is $3x10^4$ Rads (Si) total dose. Westinghouse reports that 10^5 Rads (Si) total dose tolerance has been demonstrated on a device made using processing similar to that for the 6008.

Several suppliers provide MNOS memory devices with capacities to 8K bits. Major research activity is being directed towards increasing chip capacity, increasing speed, reducing power requirements, and increasing the radiation tolerance. MNOS devices should be given serious consideration for applications where the operating speed can be tolerated. Their non-volatility makes them a serious contender in those applications now served by magnetic tape recorders.

CHARGE COUPLED DEVICES

CCD's are composed of shift registers formed by strings of MOS capacitors. Charge storage and transferral occurs between potential wells at or near $Si-SiO_2$ interfaces. Data must be constantly recirculated to achieve storage. A typical CCD memory chip contains several individually addressable shift registers which have refresh amplifiers to prevent loss of data during recirculation periods.

The Fairchild Camera and Instrument Corporation supplies a 64K (65,536 by 1) CCD memory chip. Internal organization is 16 randomly accessible shift registers each 4096 bits long. Each of the 4K shift registers is implemented using a serial-parallel-serial (SPS) architecture. Thirty two bit input and output registers service 64 internal registers each of which is 63 bits long. The input and output register cells each accommodate two of the internal registers. The operating frequency range is 1 MHz to 5 MHz. Operating and standby power requirements are 376 mw and 80 mw respectively.

CCD's suffer the same limits of radiation tolerance as other MOS devices. Research activity is aimed at improving the radiation tolerance by: reducing the die sensitivity to radiation; coating the die; and providing on chip error correcting circuitry.

In May 1980 IBM announced a 256K CCD Memory. Organization can be either 256K by 1 or 64K by 4. The shift register building blocks are 4K (32 by 128) SPS devices. The chip has eight isolated 32K octants to balance loading on clock drivers, reduce undesired coupling between different sections of memory, and to permit use of fractionally good devices. Power dissipation is listed as 310 mw with operating voltages of +8.5, +5.0, and -2.2 volts. The chip is laid out using a set of 2.0 μm minimum feature size photolithographic design rules.

FLOATING GATE DEVICES

The Floating Gate memory cell stores information by trapping charge on a floating (isolated) polysilicon gate. Since charge storage occurs as a result of avalanche injection of electrons, and since the device is basically an MOS structure, this technology is sometimes referred to as FAMOS (Floating-Avalanche-Metal-Oxide Semiconductor). Actually, PROM's which use ultraviolet light for erasing are FAMOS devices.

The most recent entry in this technology is the Intel 2816 EEPROM. It features a 250 ns access time and a 2K by 8 bit architecture. Individual bytes may be erased or rewritten in 10 ms, or the entire chip may be erased in the same time. Operating/standby power requirements are 495 mw and 132 mw respectively. Operating voltages are 5 v for reading and 21 v for erasing or writing.

Radiation tolerance of these EEPROMs is the same as that for any MOS device. It is in this area where significant improvement will be required before Floating Gate devices can be seriously considered for application in harsh environments. The slow writing speed also severely limits their usefulness where non-volatile RAM is required.

OTHER SOLID STATE TECHNOLOGIES

CRYOGENIC MEMORIES

Cryogenic memory cells are based upon circulating current in superconducting loops. The magnetic flux created and maintained by the circulating current may be sensed to indicate the logic value of the stored data. Josephson Junctions are used to provide high speed switching of the circulating currents. Zero power is required to maintain data. This is somewhat overshadowed by the need to maintain the device at 4 degrees Kelvin. Approximately 3000 watts of refrigerator input power are required for each watt dissipated by cryogenic devices.

Little is known about the radiation tolerance of Cryogenic memory devices. The technology is by no means mature. No information concerning radiation tolerance appeared as a result of the literature search.

The principal investigator of Cryogenic memories is IBM. Sperry Univac is also involved in a limited fashion. IBM has simulated, designed, and tested all the components necessary to build a 4k by 1 Cryogenic RAM. Operating power requirement for this 1.? ns access time chip is 6 mw. Readout is non-destructive. They are also developing a 16K Josephson memory chip. This device uses a single flux quantum memory cell which has destructive readout. Since data must be restored after reading, the 16K chip is slower than the 4k device described above. Cycle time is 30 ns, but the operating power is only 40 μw.

The great disadvantage of Cryogenic memory devices is the necessity to provide refrigeration. Refrigeration power requirements impose severe limitations on the use of these devices for space flight applications. However, the non-volatility, high speed operation, and low power requirements justify serious investigations of alternate methods of maintaining the necessary temperature.

AMORPHOUS SEMICONDUCTORS

The amorphous semiconductor memory element utilizes semiconducting glass as the storage medium. The resistance of the device is reduced to a low value by applying a specified voltage and establishing a current of about 8 ma for 1 msec. Resetting the resistance to a high value requires a current of 200 ma for about 5 microsec. Reading is accomplished by measuring the resistance of the cell. This device is intended to be used as an EAROM.

Energy Conversion Devices of Troy, Michigan has designed and built a 1K device and has signed a licensing agreement with Burroughs to manufacture the chips. The individual cell size is less than 1 square mil indicating that a 16K chip is reasonable using existing processing techniques. Mr. S. H. Holmberg of ECD estimates the cost to design and develop a 16K chip at $200K. A conservative cost estimate for a 100K bit memory system in small quantities is 30 cents per bit.

Readout is non destructive and data storage is non volatile. The current devices can be operated at temperatures ranging from 0°C to 70°C and stored at a temperature of 100°C. Roy Shanks of Burroughs stated that they built a 1K chip several years ago. Access time was 10 ns. He feels that a 16K chip could be developed in two years at a cost of $200K. He feels that amorphous devices using MOS techniques would yield a 64K chip within four years if a serious commitment were made.

The radiation tolerance of the amorphous memory element exceeds that of any other electrically alterable memory. No evident degradation occurs at $3x10^{16}$ n/Cm^2 and 10^7 Rads (si) total dose. Transient upset (due to extreme temperature excursions) occurs at 1.5×10^{14} Rads/sec. Destruction occurs at $2x110^{14}$ Rads/sec from shattering of the silicon substrate.

This technology warrants serious consideration for applications requiring relatively small non-volatile RAMs in harsh environments.

GALLIUM ARSENIDE

The electron mobility in lightly doped Gallium Arsenide at 300°K is 8500 Cm^2/volt second, compared to 1500 Cm^2/volt sec for Silicon. This fact along with the ability of GaAs to operate at 350°C (maximum operating temperature for Silicon is 200°C) makes GaAs logic and memory devices very promising for future space applications.

Dr. R. Zuleeg of the McDonnell Douglas Astronautics Company in Huntington Beach, California has evaluated small scale integrated GaAs planar circuits in radiation environments. These devices have operated with negligible degradation of electrical performance after irradiation as described below:

10^5 n/Cm^2 (E > 10 KeV)	Fast Neutrons
10^7 Rads (GaAs)	Total Dose
8×10^9 Rads (GaAs)/sec	Dose Rate for Logic Upset
10^{16} Rads (GaAs)/sec	Survival Rate

These levels of radiation tolerance can be increased through advances in fabrication and material technology. For example total dose tolerance of 10^8 Rads (GaAs) is a reasonable expectation.

Several companies including Rockwell, Hughes, Lockheed and McDonnell Douglas are conducting research in GaAs. Data rates are projected to be from six to ten times those achieved with present day silicon devices. D. Howard Phillips of Lockheed has projected 2-10 GHz logic ICs and 40 GHz transistors.

Hughes Aircraft has a Navy contract to study the feasibility of a 1K, 1 μs GaAs RAM.

Rockwell has completed the design of a 4K GaAs RAM which they plan to demonstrate during the fourth quarter of 1983. Production quantities will be available in the fourth quarter of 1985 if the project is funded.

Dr. Richard Eden of Rockwell International Electronic Research Center in Thousand Oaks, California reports development and fabrication of two binary multipliers. The initial effort was a 5 by 5 multiplier. They have achieved 19.5% yield on 3 inch GaAs wafers. This part uses 260 gates.

An 8 by 8 latched multiplier using 1008 gates has been designed. As of September 1980 the best processing run had yielded a part with 1006 of the 1008 gates functioning. Defects in processed devices are not well understood at this time. Defect density is the most important obstacle which must be overcome before the 16K GaAs RAM becomes a reality. According to Eden, Rockwell will concentrate on reducing the defect density before attempting to fabricate high density devices.

MDAC HB has been awarded a DARPA contract to develop a 4K by 1 GaAs RAM. The memory cell requires 1.25 μw (per bit) with 5 to 10 ns access time. The total power requirements for the 4K RAM, including required on-chip logic is 73.3 mw. Since the operating voltage can be removed from the peripheral circuitry when the memory contents are not being read or altered, a 2 M bit memory would require only 2.56 watts in the standby mode.

While GaAs is an emerging technology, it clearly has great potential for future spacecraft memory applications. There are strong indications that 4K GaAs RAMs will be available from at least two sources by 1984.

MAGNETIC MEMORIES

CORES

Ferrite cores were the storage elements of the first random access memories used extensively in digital computers. The core is a torroid formed of a mixture of powdered ferrite and bonding materials. To be suitable as a storage element the core must have a nearly rectangular hysterisis loop in its B-H curve. Figure A-1 depicts such a curve.

The individual cores are threaded on wires to form memory arrays. As shown in Figure A-1 a threshold current (Is) exists such that the magnetomotive force produced thereby will switch the core to the logical 1 state. Since Is/2 will not switch the core, selection is accomplished by the coincidence of half select current in each of two wires passing through the cores.

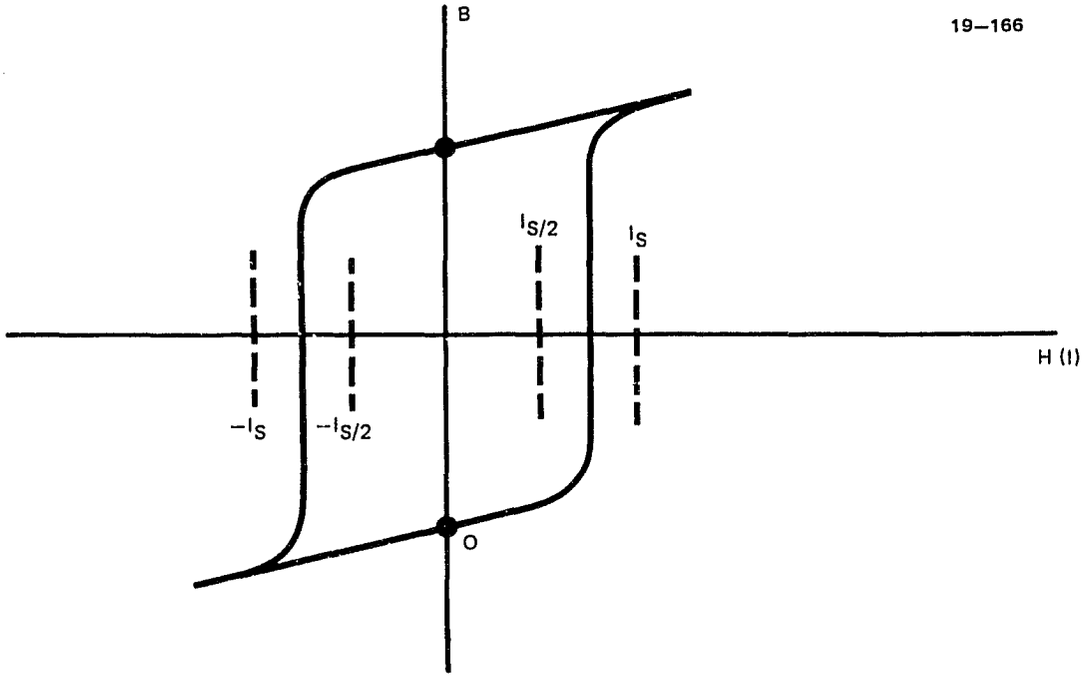

FIGURE A–1 B–H CHARACTERISTIC OF A FERRITE CORE

Reading is accomplished by writing a zero (clearing) the core and noting the magnitude and time of occurrence of a voltage pulse induced in a sense wire which passes through the core. After a group of cores has been read each of them is in the zero logic state. This is an example of destructive reading. It is necessary to rewrite the data if permanent storage is desired. Writing is also a double operation, i.e., the cores are all cleared and logical 1's written in the appropriate locations.

The disadvantages of core memories include relatively slow speed operation, the need for extensive address decoding circuitry, line drivers capable of supplying 1 ampere or more for selection, and the relatively low bit density of the complete system. The advantages of core memories during their heyday were random access, nonvolatility, and radiation tolerance. The significance of the latter is diminished by the fact that the support electronics limits the radiation tolerance of the system.

The present status of core memories is perhaps best described by the units available from Ampex Corporation. They produce 36 billion cores per year of which 25 billion are delivered to military customers. Those destined for military applications are 100 percent tested at -60°, 25°, and 110°C. Yield varies from 60 to 80 percent.

Cores with overall diameters of 18 mils and 13 mils with thickness of 1.5 or 3.0 mils are in production. Output signal amplitudes are 20 mv and 15 mv respectively. A 9 mil core with 10 mv output is under development. The 13 mil cores can be packed such that the areal density is 1782 bits per square centimeter.

A typical 32 megabit system requires 720 watts (22 mw per bit). System bit density is 210 bits per CM^3. Maximum data transfer rate is 2 megabits per second.

Ampex has recently introduced a 256 by 8 Ferrite core memory housed in a 2" by 2" 40 pin DIP. The memory element is a 13 mil core. Cycle time is 1.6 μsec yielding maximum data rate of 625K bits per second.

PLATED WIRE

In an attempt to overcome some of the disadvantages of Ferrite core memories Plated Wire memory systems were developed by Sperry Univac and others. The storage medium is a thin film of magnetic material (e.g., a nickel-iron alloy) deposited on a conducting wire.

A storage system is created by establishing a group of closely spaced parallel plated wires overlaid by an associated transverse set of conductors called word lines. Figure A-2 illustrates the principal. Storage locations are at the intersections of word lines and the plated wire pairs.

19–167

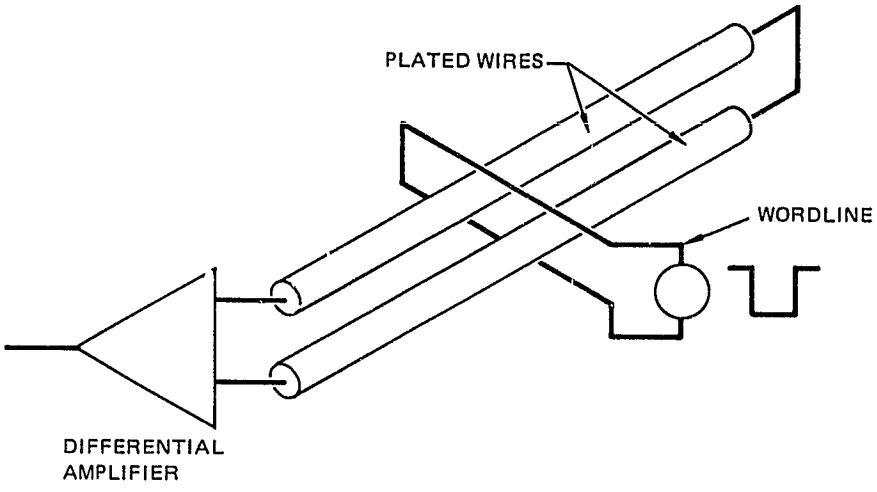

FIGURE A–2 PLATED WIRE MEMORY CELL

The plated wires serve as carriers for one of the coincident currents required for writing (the word line carries the other) and also as the sense lines during a read operation. Readout is non destructive and storage is non volatile. Radiation tolerance of 10^6 Rads (Si) total dose is typical.

Sperry Univac has built and delivered Plated Wire memory systems using 2.5 mil (63.5 μm) diameter wires on 12.5 mil centers. System bit density is about 45 bits per CM^3. Operating power is 75 watts for 16,384 36 bit words (0.13 mw per bit). Read and write cycle times are 500 ns and 750 ns respectively. Note that the data rate is comparable to that of cores, the operating power per bit is much lower, but the bit density is lower by a factor of five.

Sperry Univac proposed an 18 megabit system (which was never built) with a density of 366 bits per CM^3, operational power of 11.1 μw per bit, cycle time less than 1 μsec, and projected cost of less than 1 cent per bit. It should be noted that the only military plated wire memory system which Sperry Univac ever delivered cost about $2 per bit.

Plated Wire memories did not replace cores in random access applications due in some measure to difficulties encountered in fabrication. The major obstacle to their development, however, was the development of solid state RAMs.

CLOSED FLUX MEMORY

In 1973 this planar counterpart of plated wire memories appeared very promising. The Navy awarded development contracts to Ampex Corporation, Redwood City, California from 1970 to 1973. According to John Mallinson of Ampex, funding was withdrawn in 1973.

Ampex claimed that Closed Flux memories were 10 times faster than cores. Apparently they were never mass produced because they could not compete with solid state devices in critical areas such as bit density (155 bits/CM^2), and power requirements (0.2 watt per bit while reading). Since production versions were apparently never made, realistic cost estimates are not available. In 1973 John Keenan of Ampex reported that to make this technology cost competitive with semiconductor memories would have required "a multi-million dollar plant and huge volume." Apparently the anticipated volume did not justify the necessary investment.

John Mallinson of Ampex indicated (in September 1980) that one hundred 256 by 256 Closed Flux planes were produced in 1973, after which the project was shelved.

MATED FILM MEMORY

This too was intended to replace Ferrite cores. The memory elements are formed by a series of vacuum depositions on a glass substrate. Copper sense/digit lines enclosed by nickel-iron bit locations need only to be driven by word drive lines which bracket the storage strips at regular intervals. Bit density in 1975 was 40 bits/CM^2.

The read operation is destructive thus requiring a restoring cycle if stored information is to be maintained after reading. Partak reported a 750 ns cycle time in 1975. A proposed 1 Mbit system described in his paper listed a density of 60 bits per CM^3 and a power requirement of 250 watts.

Since the literature search spanning the 1975 to 1980 time period revealed nothing about this technology, it is clear that no significant work is being done. Obviously tremendous improvements in bit density and power requirements must be made if Mated Film is to compete favorably with Semiconductor memories.

FERROELECTRIC MEMORY

The storage medium in this device is Pottasium Nitrate, which exhibits a binary polarization phenomenon in response to an electric field. This is analogous to the response of ferrite materials to a magnetic field. According to Partak, the original ferroelectric memories were intended to be used as EAROMs.

Technology Service Corporation apparently supplied 100 bit (10 by 10) ferroelectric memory chips with 5 μsec write cycle time. Since readout was destructive it is reasonable to assume that the read cycle was similar.

This technology was apparently doomed by the appearance of ultra-violet erasable PROMs because of their improved bit density, lower power requirements, and much shorter read cycle time.

The literature search revealed no significant activity in this technology. Abstracts of papers published in the United States and Japan indicate research activity investigating fundamental properties, but nothing offering a promise of a serious contender to EPROMs.

FERROACOUSTIC MEMORY

Sangamo Electric Company produced a study report on this technology for the Navy some time in the early 1970s. It was intended as a BORAM device in which writing was accomplished by a combination of an electrical current and a sonic pulse. The memory element (Soniscan^{R}) was apparently developed by Sylvania.

A 1.2 Mbit system proposed in Partak's document had a 14 MHz data rate. Storage was nonvolatile, readout was non destructive and bit density was 120 bits per CM^3. The system had an operating power requirement of 100 watts and required a 120 volt source to generate the sonic pulse.

This technology was not able to survive the competition from MNOS BORAMs and Magnetic Bubbles. No research in this area was revealed by the literature search.

MAGNETIC BUBBLE MEMORY

The storage medium in a Magnetic Bubble memory device is a thin film of magnetic material situated between two permanent bias magnets. Garnet is typically used as the thin film material. The easy axis of magnetization of the garnet is perpendicular to the plane of the film. In the absence of external magnetic fields magnetic domains within the thin film are evenly distributed and are alternately magnetized in opposite directions normal to the plane of the film.

In the presence of a bias field (from a permanent magnet) normal to the plane of the garnet film domains whose direction of magnetization coincide with that of the applied field grow at the expense of those which are magnetized in the opposite direction. When the bias field strength exceeds a critical value the shrinking domains (those with magnetic polarity opposite to the applied field) divide into small segments which then contract until they become minute cylinders. When viewed head on these cylinders resemble bubbles on the surface of a liquid.

Nonuniformity in the external magnetic field causes the bubbles to drift towards those areas of weakest field strength. This characteristic is exploited in Magnetic Bubble memory devices. Permalloy tracks which are vacuum deposited above the garnet film form shift registers in the presence of a constant bias field (normal to the plane of the film) and a rotating in-plane field. By suitable placement of the permalloy circuit elements and application of appropriate magnetic field components bubbles can be created (nucleated), moved along prescribed paths, duplicated, detected, and anihilated.

Early MBM devices consisted of one single shift register with a "seed" bubble from which bubbles could be replicated when writing logical 1's. The register contained one stable bubble location for each bit of storage capacity. A replicator-detector at the output made non destructive reading possible. Storage was nonvolatile because the bias field was created by permanent magnets.

The single shift register approach suffers from two disadvantages. The access time to a desired bit position may be excessive. Of more concern, however, is the fact that a single fault in the shift register structure renders the device useless. In practice a serial-parallel-serial shift register arrangement is used. Redundant minor loops are incorporated to increase the yield of the finished chips.

MBM devices are available from at least four American and two Japanese sources. Maximum capacity at this writing is 1 Mbit. The 7110 from Intel Magnetics is the only 1 Mbit chip available in production quantities. It will serve as the model for the remainder of this discussion.

The 7110 uses 3 micron bubbles in a major track minor loop architecture. There are a total of 320 minor loops within the 7110. Each has 4096 storage locations. The chip is separated into two equal sections each of which contains 160 minor loops. Only 136 of these loops are utilized. Thus, as many as 24 of them in each half of the chip may be defective without reducing the effective storage capacity of the chip. Each half also contains two "bootstrap" loops (only one of which is bonded) which are used to store data defining which of the minor loops are used for storage. Of the 136 storage loops in each half 128 are used for data storage, 7 for error correction bits, and 1 is a spare. Both halves share common drive coils. Thus, data are stored in 256 bit data fields with as many as 16 bits available for error correction code storage.

The nominal frequency of the rotating magnetic field is 50K Hz and the corresponding data rate is 100K bits per second. This data rate is achieved by writing two data bits per page in each of the minor loops. Thus, the storage capacity is 2048 pages of 512 bits each.

Intel was the first supplier to provide a complete set of support electronics housed in IC packages. The minimum system requires (in addition to the 7110); an HMOS bubble memory controller, an NMOS Formatter/Sense Amplifier, a Schottky Bipolar Current Pulse Generator, a CMOS Coil Predriver, and two quad VMOS Fet drive transistor packs. The complete 1 Mbit system can be mounted on a 4" by 4" printed circuit board.

One Bubble Memory Controller can directly control as many as eight MBM chips. By operating the eight MBMs in parallel the nominal data rate is increased to 800 KHz. The page size becomes 4K bits in this configuration. Average access time to the first page is 20 ms. Operating power, assuming 100 percent duty factor is 40 watts while standby power is 7 watts. If the MBMs are individually accessed these power requirements are reduced to 6 watts and 1.3 watts respectively.

National Semiconductor, Rockwell, and Texas Instruments are each developing 1M bit MBM chips and support electronics. Intel does not have a second source at this time.

Research efforts in Magnetic Bubble devices is directed towards increasing bit density (reducing bubble size), increasing data transfer rate, and decreasing operating power requirements. Elimination of the drive coils which generate the rotating magnetic field would be highly desirable.

One approach which would eliminate the need for drive coils is the so-called Current Access MBM device. This technique was introduced by Bell Telephone and has been pursued by others including IBM and the NASA Langley Research Center in Hampton, Virginia.

Larry Rosier of IBM, San Jose, stated (Sep. 1980) that after investing two years and "considerable resources" in Bubble Lattice devices which used current sheet drive IBM has shelved the technique in favor of more conventional bubble devices. They experienced severe problems trying to drive the low impedance (0.1 ohm) current sheets.

CROSSTIE MEMORY

The Crosstie Memory storage medium is a thin polycrystalline nickel-iron film. Information is stored in domain walls of serrated permalloy strips which are deposited or sputtered onto a substrate at about 300°C in the presence of a magnetic field. An anisotropic field of about 4 O_e is induced in the permalloy strips by this technique. According to Dr. L. J. Schwee of Naval Surface Weapons Center (NSWC), Silver Spring, Maryland the properties of the deposited permalloy do not change more than about 5 percent over a temperature range of -50°C to 100°C.

Magnetic phenomena known as Crossties and Bloch Lines can be nucleated and annihilated by application of appropriate magnetic fields which are created by current pulses in conductors located near the permalloy strips. Serrations in the edges provide stable locations for crossties and Bloch lines. These are the storage (bit) locations.

In permalloy with anisotropic field strength of 4 O_e the maximum crosstie linear density is about 3,000 per CM. Since the crossties can be made to propagate down the strip in the presence of an appropriate magnetic field the serrated permalloy strips serve as shift register tracks. Typical bit locations are 10 μm apart (1000 locations per CM) to permit the use of a 50 ns period in the shifting mode. Strip width is less than 45 μm at its widest point. Strip to strip spacing of 20 μm is feasible and will accommodate 150K bits per Cm^2. The 50 ns period referred to above constitutes a data rate of 20M bits per second in the individual shift registers.

The permalloy strips may be deposited on a silicon substrate thus making it possible to include driving and detection circuitry on chip. Present technology should support a 512 x 32 bit BORAM on one chip. No bias magnetic field is required. Operating temperature range is -50°C to 100°C.

Radiation tolerance data have not been presented, but other magnetic storage devices composed of similar materials can withstand 10^6 Rads (Si) total dose.

Dr. L. J. Schwee of NSWC, Silver Spring, Maryland has conducted research on Crossties and published annual reports since 1973. Sperry Univac in St. Paul, Minnesota has developed and demonstrated shift registers. Progress has been hampered by limited financial support.

The Crosstie appears to offer great potential for BORAM applications requiring high data transfer rates in harsh environments.

MAGNETIC TAPE MEMORIES

The lowest cost mass data storage medium in common use is Magnetic Tape. Present day techniques provide storage density of 3 M bits per inch of tape and data transfer rates of 160 M bits per second. These density and transfer rate values are achieved by establishing many data tracks in parallel. Access time to the first data word of a block may be very long due to the serial organization of data in the tracks.

Because a major portion of the control and drive hardware involves mechanical devices the reliability of tape recording equipment is much less than that of nonmechanical storage systems.

RCA reports an engineering model of a Magnetic Tape Recorder (the 1231) which stores 7.0×10^{11} data bits on a single 1" by 4800' reel of tape. They use 555 tracks per inch and achieve a bit density of 12.2×10^{6} bits per inch. The data rate is said to be 80 M bits per second which implies a tape speed of about 6.5 inches per second. They have demonstrated (on a laboratory model) the feasibility of increasing the storage density to 60 M bits per square inch and providing a 600 M bit per second data rate. The system error rate under these conditions is 1 bit in 10^{6}.

RCA estimates that it would require about two years to develop and build a production version of the laboratory model described above.

Radiation tolerance of the storage medium is excellent. System tolerance is limited by the interfacing and control electronics.

MAGNETIC DISC MEMORY

The rigid storage disc consists of an aluminum disc (typically 8 or 14 inches in diameter) which is coated on each side with iron oxide. The hysterisis exhibited by the iron oxide is such that relatively small magnetic domains may be established in a predictable manner and maintained for long periods of time in the absence of operating power or external magnetic fields. It is possible to mount several discs on one drive spindle to increase system capacity.

Fixed head systems employ one head for each track on the disc. Alternatively one or more moveable heads may be used to reduce the complexity of the read-write circuitry. In moveable head systems the disc is usually removeable while in fixed-head systems it is not.

Data are stored in concentric circular tracks, usually in bit-serial form. As many as 1000 tracks per inch are possible on rigid discs. Typical density along a given track is 10,000 bits per inch. This implies a storage density of 3 M bits per cm^2 and single side capacity of 2.5×10^9 bits. Some of the storage area is used for system overhead but storage densities of 1.5×10^6 bits per cm^2 are currently obtainable.

The speed with which a Magnetic Disc storage device stores or retrieves data depends upon access time and data transfer rate. The access time is the sum of the time required to position the head over the proper track ("seek time") and the time required to rotate the disc such that the proper sector of the track is in the correct position relative to the head. The latter component is defined as the "latency time." Typically Magnetic Disc Memory systems operate with access times ranging from 10 to 100 ms. Data rates of 10^7 bits per second (per track) are available when the disc is rotated at 50 revolutions per second.

Radiation tolerance of disc systems (as in virtually all magnetic memory technologies) is limited by the tolerance of the support and drive electronics. The magnetic storage medium and the heads can easily withstand total dose levels in excess of 10^6 Rads (Si).

Magnetic Disc Memories exhibit several disadvantages when considered for space applications. They are heavy. A single disc system capable of storing 10^9 bits may weigh in excess of 200 pounds. They require considerable power. The 10^9 bit system may require as much as 5000 watts. The rotating mass produces a gyroscopic affect which may be troublesome in a spacecraft environment, particularly if the disc rotation is interrupted or significant changes in rotational speed occur. The clearance between the head and the rotating disc is very small, typically only a few microns. If physical contact is made between the two, or if any small object (such as a dust particle) contacts both the head and the disc while the latter is rotating, extensive permanent damage and catastrophic loss of data occur. For these reasons Magnetic Disc Memories are not recommended for mass data storage in spacecraft applications.

OTHER MEMORY TECHNOLOGIES

ELECTRON BEAM ADDRESSED MEMORY

The storage device employed in this technology is a tube (similar to a cathode ray tube) in which the target of the electron beam is an MOS structure in which charge is stored in a silicon dioxide layer which is sandwiched between a metal film (exposed to the beam) and a layer of N type silicon which in turn overlays a layer of P type silicon. A beam current of 20 na is sufficient to establish isolated charge packets in the silicon dioxide.

Storage density is determined by the area of the electron beam at the target. Donald O. Smith of Control Data reported 80 M bits per square inch in 1979. Data are accessed by electrostatic deflection of the beam. Access may be random by bit, or a raster scan technique may be employed to achieve block access. Reading is accomplished by scanning the target and detecting the output current of the NP layers beneath the silicon dioxide storage area. Data rates on the order of 1 M bit per second per tube were reported in 1975. Storage is essentially nonvolatile, but since readout is partially destructive periodic restoration is necessary to maintain data.

This technology has been plagued with problems from the outset. The main difficulties were involved with the high voltages (five to ten thousand volts) required for the deflection circuits and the production of reliable target surfaces and tubes. The technology has been temporarily shelved because of its inability to compete with MOS memories.

OPTICAL DISC MEMORIES

This technology utilizes a relatively low power laser beam to burn holes in a thin film of thermoplastic or metal which is sandwiched between two transparent protective sheets. The actual storage element is a 12 inch diameter disc. Using 3 mw 100 ns laser pulses holes as small as 0.6 micron have been reported by Drexler Technology Corporation of Mountain View, California. It is thus possible to store about 10^{10} data bits on each side of the disc. Writing speeds of 10 M bits per second have been recorded.

Reading is also accomplished by using a laser beam. The absence of a hole is detected by energy reflected from the remaining film material. Reading rates in excess of 20 M bits per second are reported.

The primary disadvantages of Optical Disc Recording systems as they presently exist are the necessity to use gas lasers for recording and the fact that erasure is not possible. Gas lasers are physically large and require too much power for spacecraft applications.

Magnavox (Phillips) and RCA are conducting research aimed at developing solid state lasers with sufficient power for recording. Laboratory models have been developed but their characteristics are not repeatable. Average lifetime is 2000 to 3000 hours. At least 30 companies throughout the world are researching film materials which will require lower power for recording, provide good archival lifetimes, and permit data to be erased and rewritten.

Literally no data are available concerning the radiation tolerance or temperature range of optical storage media. The technology is in its infancy.

Research in all phases of Optical Disc Recording will continue with or without outside support because of the tremendous potential commercial market. It will be necessary for the military to sponsor research if ruggedized and radiation hardened versions are desired. This technology offers the most potential for inexpensive high speed mass storage systems of any of the technologies currently available.

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