RECENT DEVELOPMENTS IN THIN SILICON SOLAR CELLS*

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COPLANAR BACK CONTACT CELLS

50um thick cells 2x4cm^2 area with coplanar back contacts were made with good yield, and with output equivalent to conventional top/bottom contact cells of the same thickness. A wraparound junction (WAJ) design was selected, and used successfully. The contact configurations are shown in Figure 1. The low αs cells delivered were all above 12%, the average efficiency was 13% and the best was 14%. The overall yield was 35-40%, comparable to that for conventional 50um cells (see Table 1). The process sequence was moderately complex, but showed good reproducibility. The CBC cells performed well under several important environmental tests. High αs CBC cells were made, with about 1% increase in conversion efficiency.

The most important design criteria were the choice of back surface N+ and P+ areas.

P+ AREA

Any giveaway P+ area introduced series resistance losses. The losses depended on both the area and the configuration of the giveaway area. This WAJ design did not allow reduction of this loss by use of the P+ BSF layer. The final design reduced this giveaway area, with minimal loss in output.

N+ AREA

The N+ layer on the edges and back surface introduced shunt losses. These were minimized by reducing the N+ area. Table 2 shows the improved cell performance (CFF) as the N+ area was decreased systematically (at the same time the P+ contact was correspondingly increased). Reduction of the N+ back surface area to ~2.5% also decreased shunting components in the diode dark forward current, and eliminated some inhomogeneities caused by illumination at different parts of the cell.

SILICON

FZ Si gave higher output than CZ. Cells were made with either 10 ohm-cm and 2 ohm-cm silicon; histogram plots of the output (Figure 2) show the distributions

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were similar. These two groups can be used for close comparison of the radiation resistance of CBC cells.

I-V DATA

Typical values were Isc ~312mA, Voc ~610mV, and CFF ~0.76. The best cell had Isc 312, Voc 0.619, and FF ~.79; the I-V curve for this cell is shown in Figure 3. αs was measured ~0.72.

CONCLUSIONS

If the array advantages are sufficient to require 50um cells with coplanar back contacts, cells of good performance can be made, and there is further chance that the fabrication processes can be streamlined to reduce the most differential against conventional 50um thick cells.

VERY LOW αs 50um CELLS

The goals of this program, αs <0.64 with efficiency →14% have involved careful examination of the tradeoffs needed to combine these two goals. To reduce αs, several cell design features are required:

a) The front surface should not be textured (the loss of power from increased αs offsets the increased current).
b) The back surface must have high optical finish.
c) A high IR reflectance back surface contact layer is required.
d) Slight advantage can be taken of the use of high UV reflectance coatings on the coverglass.

NOTE: We have not assumed the use of a separate blue-red rejection filter.

In addition, several essential process steps are needed, especially for thin cells:

i) A shallow diffused layer is required on the front surface.
ii) Grid patterns with minimum shading.
iii) Good quality AR coating.
iv) A back surface field (BSF) is needed.

For (ii) and (iii) we estimated the tradeoff between power loss and cell αs, for two limiting cases, namely full front surface metal coverage, and omission of AR coating. The estimated αs values were ~0.25 and ~0.50 respectively, but the increased power available from these low αs values was much less than the decreased power caused by these extreme conditions. We concluded by analysis and from tests, that any attempt to reduce αs at the expense of active area or AR effectiveness was also counter productive.

PROCESS SELECTION FOR LOW αs, 50um CELLS

(a) A suitable method is needed for thinning to 50um while maintaining high surface finish, especially on the back surface. We developed an etch-thinning process which leaves a mirror finish on the back surface, and a near specular finish on the front surface.

(b) For BSR metals, we extended earlier comparisons of metals with high IR reflectance, and selected gold for this work. Later, to improve the environmental performance we have used a very thin layer of aluminum under the gold. To ensure low contact resistance, we have returned to a structure used earlier, where the ohmic contact to the back surface is provided by a grid contact (deposited over the BSF layer) and the BSR metal is deposited on the remainder of the back surface. The grid pattern was designed to minimize series resistance at the sheet resistance levels introduced by the BSF.

(c) The BSF formation involves the major trade-offs. For thin cells, a good BSF (increased Voc, increased long wavelength response) is essential. Usually a good BSF layer involves high doping levels and reasonable depth of the layer. Often these steps reduce the optical quality of the back surface. We have avoided this possibility by using boron-diffusion, a process we have shown effective for highest output 50um cells. However, the high boron doping levels have led to another trade-off, caused by free carrier absorption in the BSF layer. This free carrier absorption (beyond 1.1um) decreases the overall reflectance, and the decrease is more serious at longer wavelengths.

We have found that the effective reflectance values can be shown to have λ^2 dependence, as prediced for free carrier absorption.

We have varied the boron doping levels systematically (keeping other factors constant) and have shown steady decrease in IR reflectance (Figure 4). In addition, we evaluated the BSF effectiveness of these varying boron conditions, and showed that to achieve αs <0.65 will require loss of cell efficiency.

Figure 5 shows the present combination of I-V output and αs achieved. At present we are fabricating 50 deliverable cells to show the best state-of-the-art.

CONCLUSIONS

It is possible to make silicon cells with αs below ~ 0.60. However, to maintain state-of-the-art efficiency ($>12\%$) sets a limit to αs ~ 0.63, and suggests that in practice, the additional difficulties in reducing αs to this range for thin cells, are accompanied by reduced cell output. The best compromise appears to be operation at high efficiency down to αs <0.67.

WELDING TESTS

Weldable cells made on a pilot line (50um thick, 2x2cm, low αs ~ 0.72 and average AMO efficiency ~13%) have been distributed to the array industry. In most cases, the cells have shown good weldability, especially after suitable handling techniques were developed. (Fuller reports on these cells will be given in other papers at this conference.)

TABLE 1

PROCESS LOSS AND YIELD SUMMARY FOR THE THREE FINAL PILOT RUNS

PROCESS LOSS AND REJECT MODE	LOT NUMBER I(%)	II (%)	III(%)
CLEANING AND ETCHING	10.2	12	10.7
SiO_2 DEPOSITION	2	2.5	3.5
DIFFUSION ($POCl_3$, BN)	6	5.5	2
PHOTORESIST WORK	12.8	3.5	8.7
METALLIZATION	4	6	6
PLATING	6.4	8	8.5
CUTTING AND AR COATING	0.6	0.5	1.3
MECHANICAL REJECT	6.7	8	18
ELECTRICAL REJECT (< 12% AMO)	14	12.7	7.3
TOTAL YIELD (≥ 12%)	37.3	41.3	34

TABLE 2

TESTS TO DETERMINE TRADEOFF N+ AND P+ BACK SURFACE AREA

N+ AREA (%)	P+ AREA (%)	Voc (mV)	Jsc (mA/cm^2)	CFF (%)	EFF (%)	Rs (ohm)
10.2	88.5	602	37.3	74	12.3	0.080
5.1	93.6	590	37.9	75	12.5	0.058
2.3	96.4	598	37.7	77	12.9	0.056
0	100	592	37.8	78	12.9	0.055

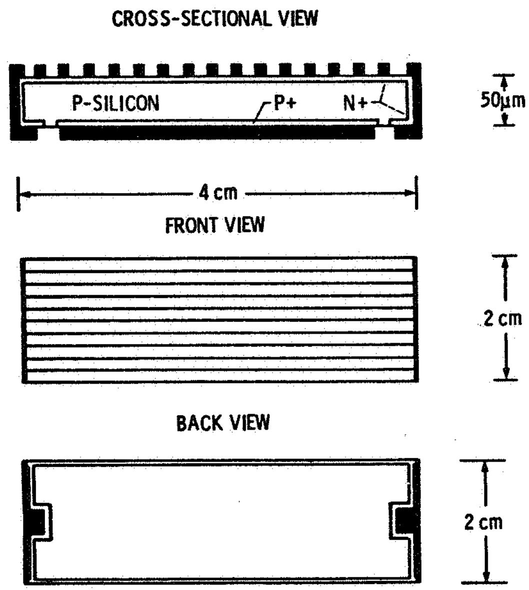
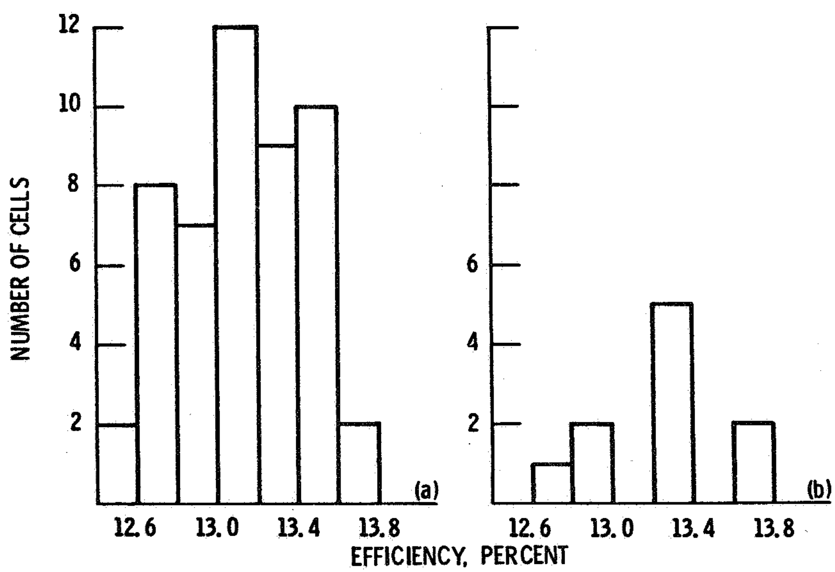


Figure 1. - 2-mil coplanar back contacts cell (WAJ).



(a) 10 ohm-cm (50 cells).
(b) 2 ohm-cm (10 cells).
Figure 2. - Histogram plot for delivered 50-μm CBC cells.

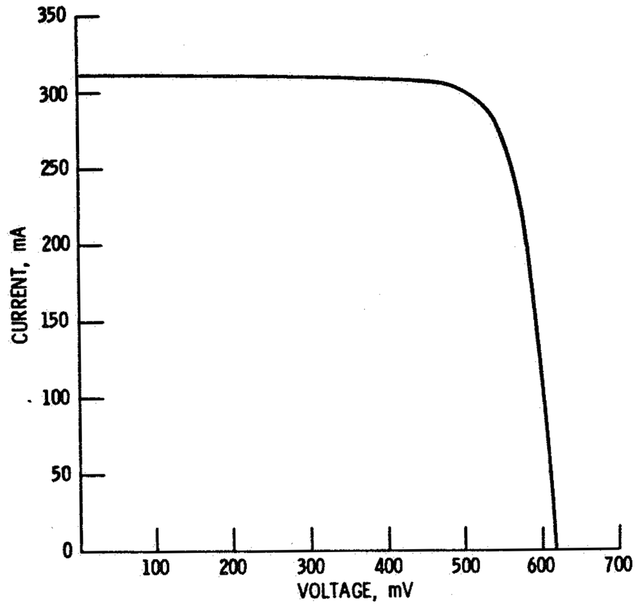


Figure 3. - Current-voltage curve for 50-μm CBC cell.

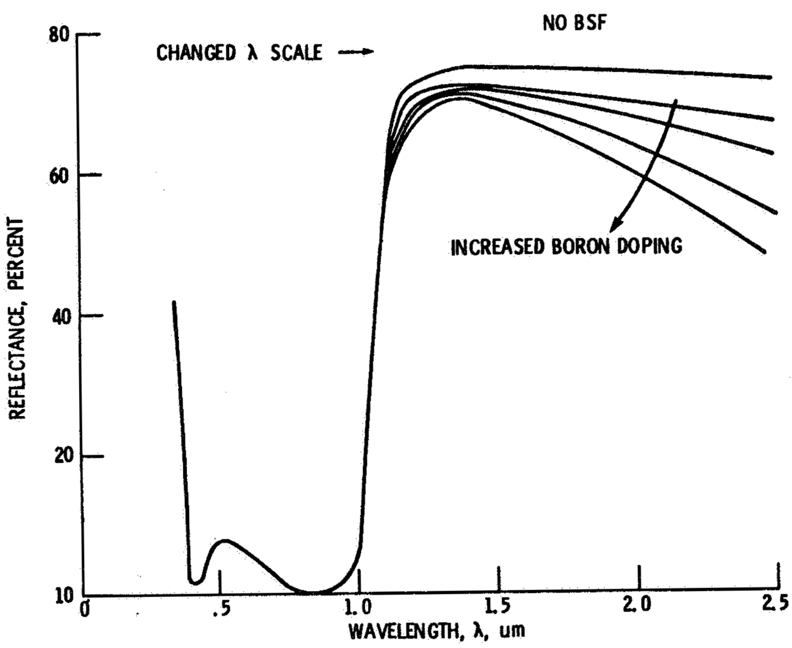


Figure 4. - Specular reflectance and wavelength (varying boron doping).

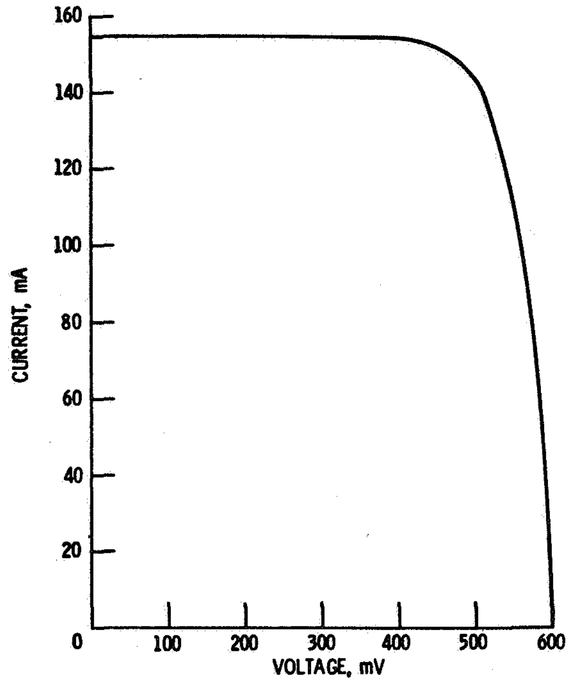


Figure 5. - Current-voltage curve for 50-μm, low α_s cells.