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NASA CONTRACTOR REPORT 166439

Si:Bi Switched Photoconductor Infrared Detector Array
Final Technical Report

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NASA

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Final Technical Report

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FORWARD

This final technical progress report on a bismuth-doped
silicon, switched-photoconductor, infrared-detector array
delivered to NASA Ames Research Center at Moffett Field,
California was prepared in accordance with Statement of Work
2-30867 under Contract NAS2-11248.

AEROJET ELECTROSYSTEMS COMPANY

C. E. Eakin, Program Manager
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IR Detector Array Program

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1   INTRODUCTION

This report covers design and test details for a multiplexed infrared detector array delivered to the Ames Research Center of the National Aeronautics and Space Administration under Contract NAS 2-11248. The small demonstration prototype consisted of two cryogenically cooled, bismuth-doped silicon, extrinsic photoconductor pixels multiplexed onto a single output channel using an on-focal-plane switch-integration-sampling technique. Noise levels of the order of 400 to 600 rms electrons per sample were demonstrated for this "chip and wire" hybrid version; that value could be improved significantly with a monolithic custom design.

2   ARRAY DESIGN

The unit cell of a multiplexed switch-sampled photoconductor (SSPC) is shown in Figure 1. The photocurrent in the detector is integrated at the input capacitance of the readout source-follower MOSFET, which is normally off. At the end of a sample-integration interval, the readout MOSFET is turned on through the ENABLE switch. The accumulated photo-charge is "read" by measuring the change in the amplifier source voltage as the integration node is reset to some reference voltage by momentarily activating the RESET transistor switch. The amplifier can then be turned off as the integration cycle begins anew. During this integration interval, the other unit cells in the array, which share the same output data channel (i.e. source bus), may similarly be read out in sequence.

2.1   Array Packaging

The two 0.25-mm^2 detectors (0.020 x 0.020 in.) and their associated cryogenic-readout electronics are assembled in two 3/8-in. x 5/8-in. butterfly cases epoxied back to back. A cover plate, which also serves as a mounting clamp, provides separate field-of-view-defining apertures for the two detectors, either of which can be blocked by fastening a thin plate over it.

Pin assignments and the "detector" case assembly are illustrated in Figure 2. In addition to the two Si:Bi detectors, the case contains two high-value load-resistor chips (Eltec 112) and a carbon-resistor temperature sensor. Table 1 shows the sensor calibration. The two resistor chips are provided so that, for comparison purposes, the detectors may be operated (one at a time)

with separate conventional (i.e., nonmultiplexed) source-follower amplifiers if desired. The two detector-bias connections (pins B1, B2) are made common internally.

TABLE 1   CALIBRATION DATA FOR TEMPERATURE MONITOR 239

Temp, K	Resistance 10^3 ohms
·7.0	120.9
8.0	92.0
9.0	73.7
10.0	61.2
11.0	52.3
12.0	45.7
13.0	40.7
14.0	36.7
15.0	33.4
16.0	30.8
17.0	28.6
18.0	26.7
19.0	25.1
20.0	23.7

The "electronics" case shown in Figure 3a contains the cryogenic PMOS active components. The operating points of the two A4T163 output source-follower MOSFET chips were matched by preselection at cryogenic temperatures. Their sources are connected internally to provide a single source output. The enable and reset switches are all M104 chips and may be turned on hard at a gate-to-source potential (V_{gs}) of -10 volts. They are hard off at +5 volts. The interconnects and pinouts for the electronics case are identified in Figure 3b.

The electronics package is designed to allow operation in the conventional mode or the switch-sampled source-follower mode. In either case the temperature sensor (TM1, TM2), common source (S_{com}), common bias (B1, B2) and amplifier drains (D1, D2) must be connected externally to the cryostat.

It is further noted that, in either mode, the protective jumper between the common source and the common bias must be removed after installation in the cryostat. This jumper is provided to protect the amplifier MOSFET gates against excess static charge during handling and shipment. Because none of the PMOS devices has an internal protective diode, particular care should be taken to avoid the mishandling of switch terminals EG1, EG2 and RG1, RG2.

For operation as a conventional source follower, the load-resistor terminals RL1 and RL2 would be connected externally or possibly would be internally grounded; by grounding drain D1 or D2, leaving the other unconnected, the associated source-follower MOSFET would be turned on.

In the switch-sampling mode the sources (RS1 and RS2) and gates (RG1 and RG2) of the reset MOSFETs and the gates (EG1 and EG2) of the enable MOSFETs must be connected externally. Any wires to pins RL1 and RL2 for the load resistors must be removed in order to minimize the node capacitance of the output MOSFETs.

2.2 Timing and Drive Signals

For voltage-mode operation, only dc supplies (detector bias and MOSFET source supply) are required. For multiplexed SSPC operation, additional voltage pulses must be provided to the gates of the various switches in the proper sequence. The desired timing and drive waveforms are shown in Figure 4.

The enable pulses are timed so that while one pixel is being sampled all the others (only one in this two-pixel case) are off. To minimize voltage excursions on the output line (S_{com}), one pixel is on at all times; the succeeding pixel is enabled simultaneously as the currently active one is turned off. In this particular case, therefore, each is enabled for half the integration time (T_{int}). With N channels in the string, each channel would be enabled for T_{int}/N. Within the interval that each channel is enabled, a reset pulse of 1 to 2 microsecond duration is applied to reset the gate of the source follower to its dc reference level.

The external ac-coupled sampling amplification and measurement circuit used by Aerojet is shown schematically in Figure 5.

Immediately prior to the reset pulse, a dc-restore pulse sets the "integrated charge" potential to system ground; immediately after the reset

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(R/S) pulse, the sample-and-hold (S/H) acquires and holds the "reset" level, which (in this ac-coupled circuit) represents the amplitude of the charge integration during T_{int}. This delayed differential or correlated double sampling (CDS) effectively filters out the effects of dc drift and low-frequency ($1/f$) noise in the cryogenic MOSFET while the samples still represent the total amplitude (i.e., including dc) of the detector photocurrent.

If each pixel were to be continuously enabled, one would expect the MOSFET output waveform during integration and reset to appear somewhat as shown in Figures 6a and 6b. Enabling each pixel in sequence during one half of the integration period is then expected to produce a characteristic similar to that shown in Figure 6c. This is the waveform that is input to the external dc-restore and S/H circuit. The expected S/H output for this case is illustrated in Figure 6d.

3   ARRAY TEST AND EVALUATION

The SSPC demonstration array was tested to ensure its operability and to establish some of the more fundamental performance parameters. The principal measurement steps included

- Calibration of the internal test Dewar sources under high-background conditions
- Conventional low-background "voltage mode" performance evaluation
- Characterization of SSPC generation under low-background conditions.

3.1   High-Background Calibration

The SSPC array was installed in a liquid-helium-cooled Dewar vessel. Both leads (RL1 and RL2) were grounded, and the detector nodes (D1 and D2) and bias were externally connected. The cold cavity within which the array was mounted was provided with an aperture through which the 300 K background and radiation from a chopped 500 K blackbody source, filtered by a well-characterized 15-micrometer narrow-band cold filter (on the liquid-nitrogen-cooled shroud), were incident on both detectors. The response of each detector to these known infrared signals was measured and recorded.

The responses were then compared with those evoked by the radiation from an indium antimonide emitting diode (approximately 5.5 micrometers) operated at the same frequency (50% duty cycle) and at various excitation-current amplitudes. Comparison of the signals due to the blackbody (and therefore presumably linear response conditions) provided a calibration of the latter source in terms of an equivalent flux at 15 micrometers.

The resistance of each of the Eltec 112 loads was measured at bias levels below 100 mV. At 10 K the values were 3.03×10^9 ohms and 4.46×10^9 ohms for Channels 1 and 2, respectively.

3.2 Low-Background Voltage-Mode Performance

The aperture in the helium-cooled cavity was then closed to provide very-low-background conditions. The source-follower voltage-mode configuration was set up and the responsivity and amplifier bandwidth for each channel were measured using the calibrated InSb light-emitting-diode (LED) source. Responsivity values of 2.63 and 3.28 amp/watt at 15 micrometers and a bias of 8 volts were calculated for Channels 1 and 2, respectively. The gate-input capacitances for Channels 1 and 2 were 2.29 and 2.62 pF, respectively.

3.3 SSPC Operation

Maintaining the low-background closed-cavity optical configuration, the Dewar wiring was revised for multiplexed switch-sampled operation of the array. The pulse timing and drive waveforms are shown in Figure 7.

Figure 8 shows the outputs from the two channels individually operated, continuously enabled, and integration-sampled at 1000 samples per second. The expected waveforms are shown in Figure 6a and 6b. Based on the assumption and evidence that the capacitance at the integration node does not change appreciably from that of the voltage-mode configuration, current-responsivity values of 9.1 and 11.3 amp/watt at 15 micrometers were computed for the two channels.

Typical source waveforms under two background levels in the multiplexed mode (with X10 gain) are reproduced in Figures 8b and 8c. They correspond respectively to Dewar ambient conditions ($< 10^8$ photons/cm^2-sec) and a large dc LED flux (approximately 10^{12} p/cm^2-sec).

The large 2 V dc offset between the two channels is attributed to differences in the operating points of the two reset FETs; unlike the amplifier FETS, they were not carefully matched.

Any further gate-voltage excursion after the switch is turned off will generate a displacement-current transient in the gate-to-node capacitance. This current will be integrated at the node, thereby changing the operating point of the amplifier. Because, under cryogenic conditions, the threshold voltages of the switches can typically vary by ±0.2 volt, channel-to-channel variations in dc operating point of this order are easily accounted for. With some judicious selection, or through the use of monolithic multiplexer-switch arrays, far better uniformity and correspondingly lower pixel-to-pixel operating-point variation would easily be achievable. Fortunately, with only two channels, it was possible in this case to compensate for the switch-transient nonuniformity by providing a separate reset-voltage supply to each pixel. By this means the dc offset could nearly be eliminated, as shown in Figure 9.

The noise in the correlated-double-sampling output was measured for each channel with a Hewlett-Packard 3582A spectrum analyzer and recorded with an H-P 9845B desktop computer interfaced with the analyzer. Typical dark-noise spectra at a 1-kHz sampling rate (F_s) are reproduced in Figures 10 and 11. The root-mean-squared noise ($\overline{N}$) can be calculated from an integration of this spectrum:

$$\overline{N} = \left[\int_0^\infty S^2(f) \, df \right]^{1/2}$$

The integral reduces to $N_{max} \sqrt{\dfrac{F_s}{2}}$ because the noise spectra are closely approximated by a function of the form $N_{max} \left| \dfrac{\sin x}{x} \right|$, where $x = \dfrac{\pi f}{F_s}$. The equivalent noise in electrons per sample ($\overline{N}_e$) can be calculated from

$$\overline{N}_e = \frac{\overline{N} \, C_{in}}{A_o \, q}$$

where C_{in} is the input (integration-node) capacitance at the gate of the amplifier MOSFET, A_o is the overall gain of the amplifier, and q is the electronic charge.

Such calculations were made for both channels, yielding noise values of 421 and 596 electrons per sample for Channels 1 and 2, respectively. These values meet the requirement that the system be capable of sensing a photocurrent equivalent to or less than 1E-16 ampere in 1 second (625 electrons per sample). Lower noise values would be realized through the reduced node capacitance that could be provided by a monolithic chip.
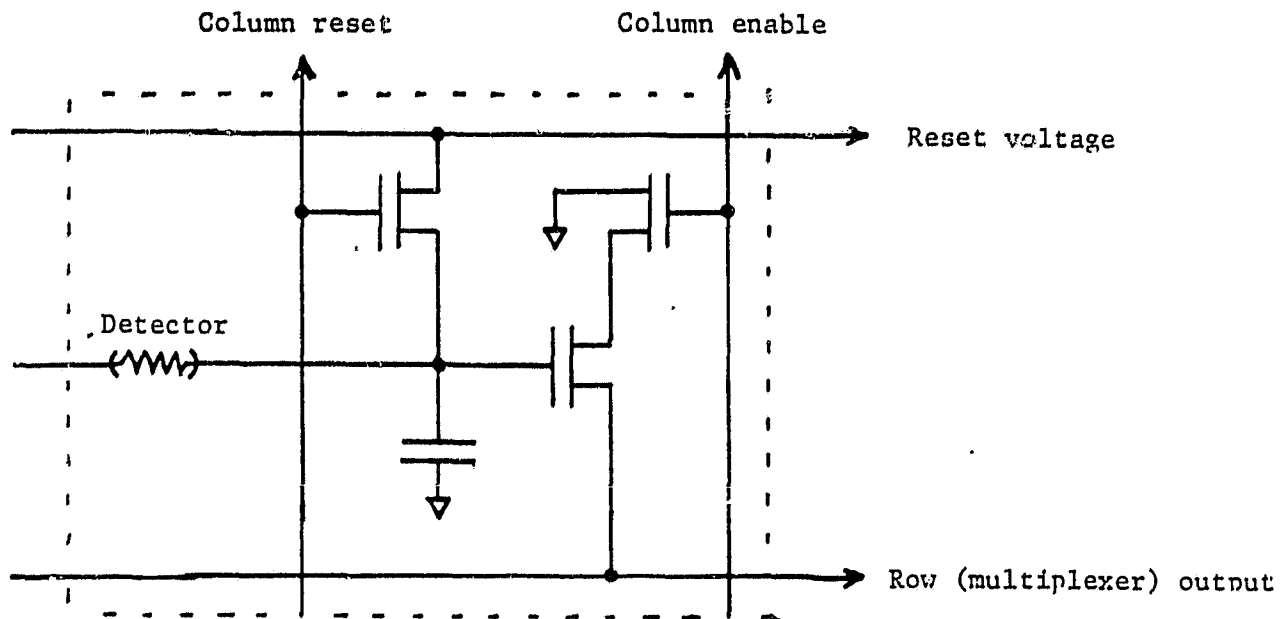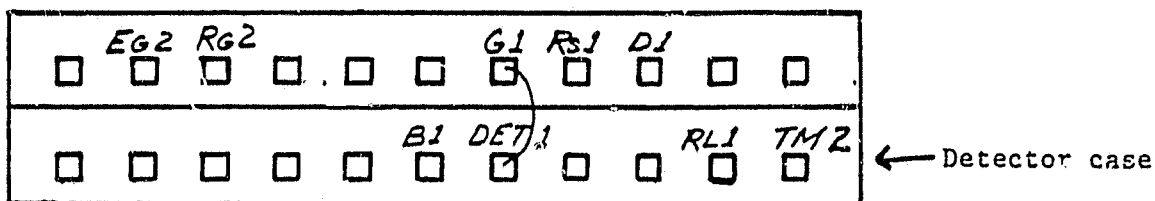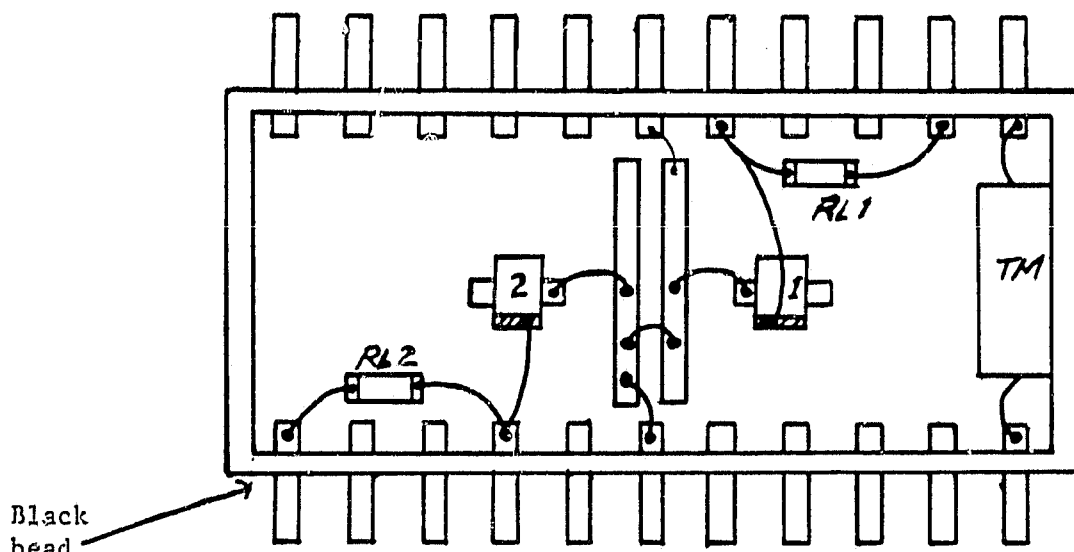
FIGURE 1 SPCC UNIT CELL

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(a)   Pin assignment for Detector 1 side

(b)   Component layout in detector case
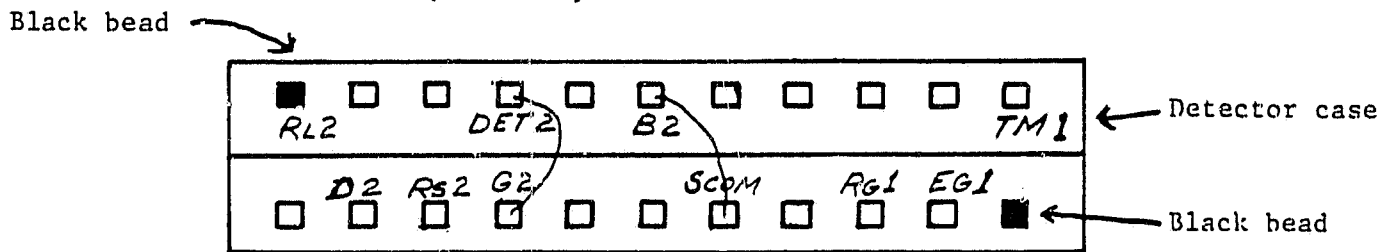
(c)   Pin assignment for Detector 2 side

FIGURE 2   SSPC ARRAY DETECTOR CASE

D1 Rs1 G1   RG2 EG2

(a)   Layout of Components

D1   Rs1   G1   RG2   EG2

M104   M104

3N163

3N163

M104

M104

EG1   RG1   Scom   G2   Rs2   D2
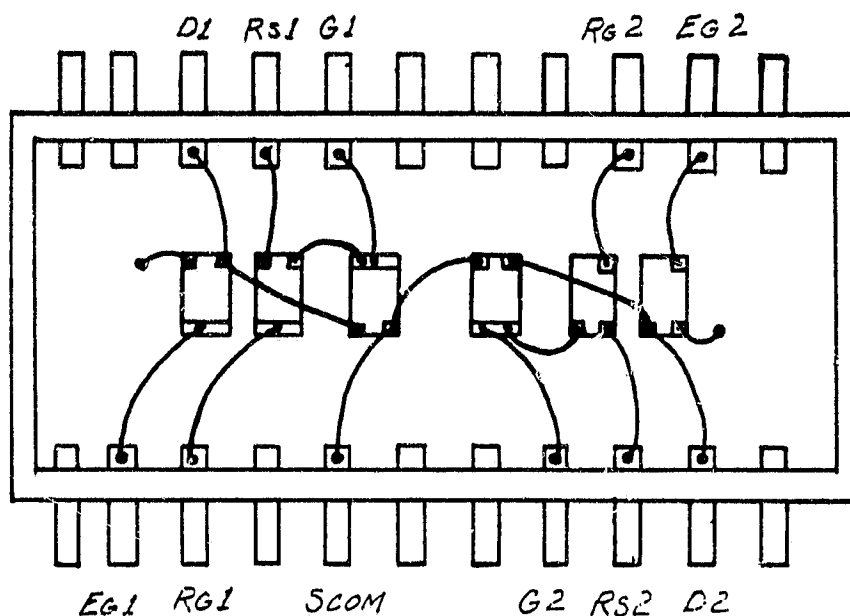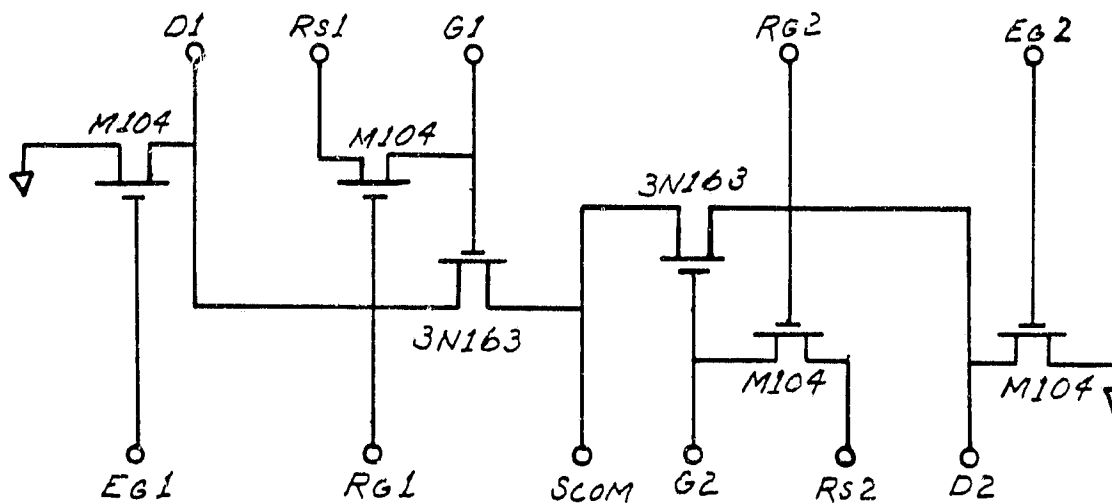
(b)   Schematic Diagram

FIGURE 3   SSPC ELECTRONICS CASE

10
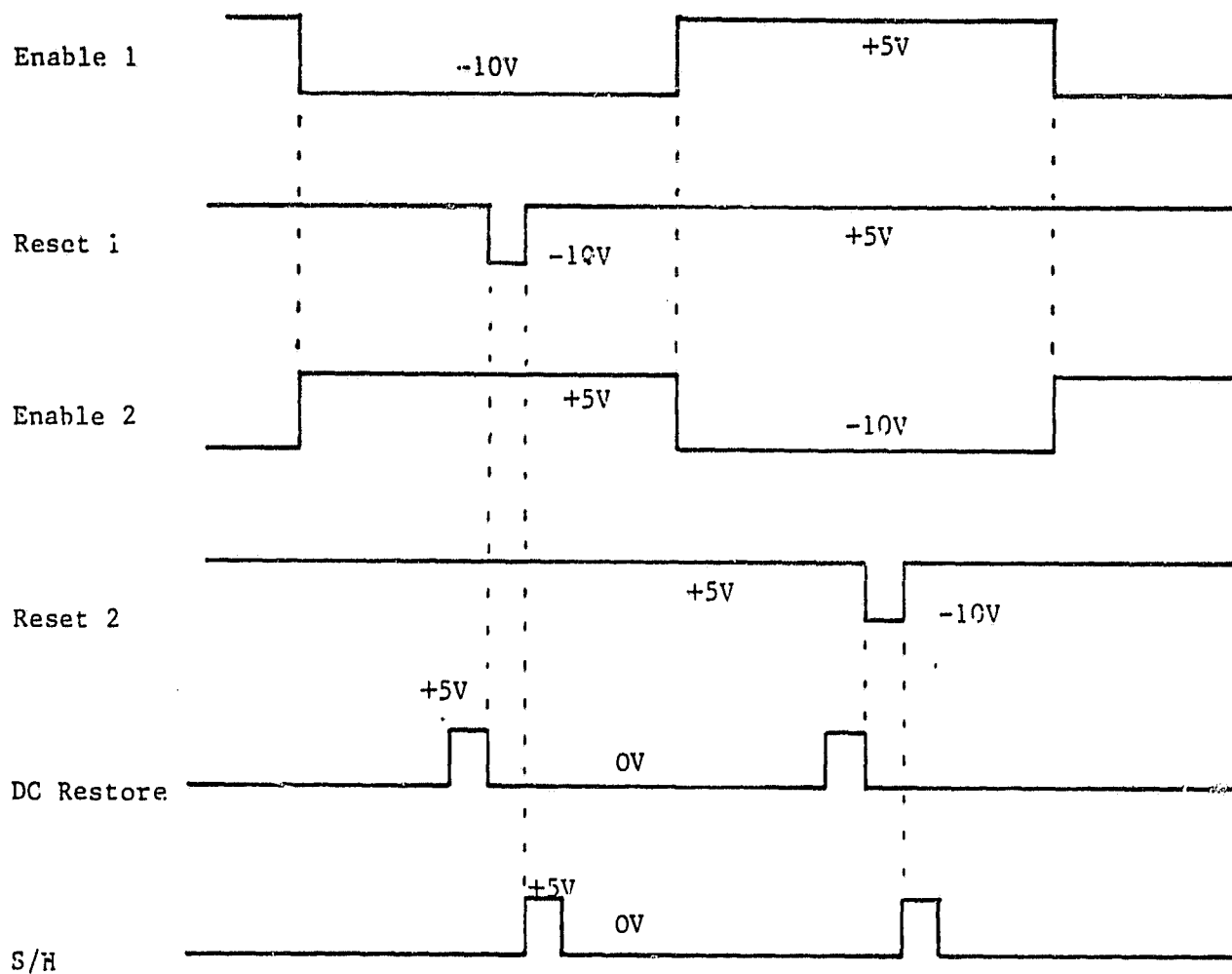
FIGURE 4   TIMING DIAGRAM FOR SSPC

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From S_{com}

V_{ss} source
supply

DC Restore

S/H

S/H
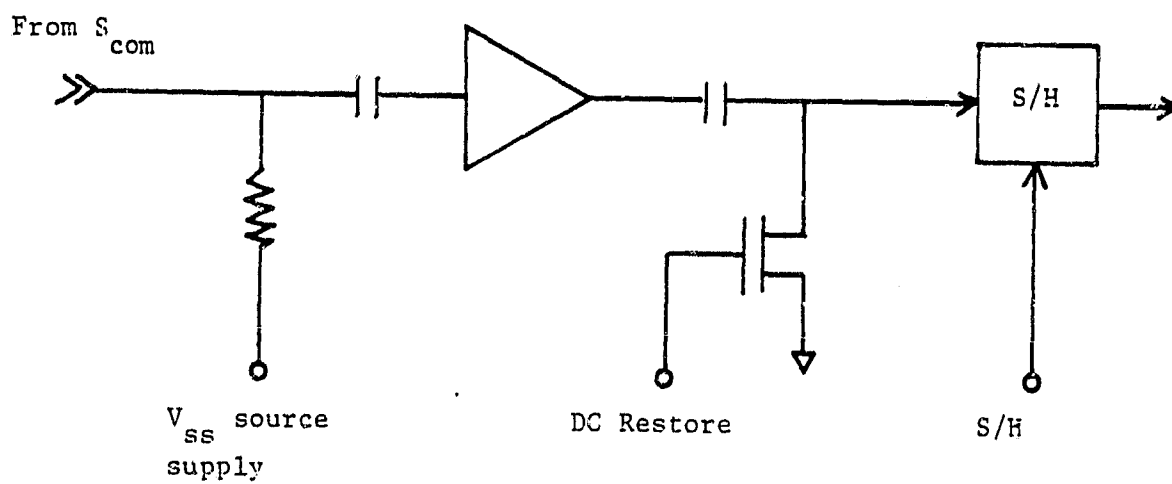
FIGURE 5   SAMPLE MEASUREMENT CIRCUIT

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Sample amplitude

a Channel 1 Alone

b Channel 2 Alone

Sample amplitude

Ch 1
enabled

Ch 2
enabled

Ch 1
enabled

c Sample and Hold Input

Zero-restore
level

Signal
Source
Turned
On

Ch 1

Ch 2

d Sample and Hold Output
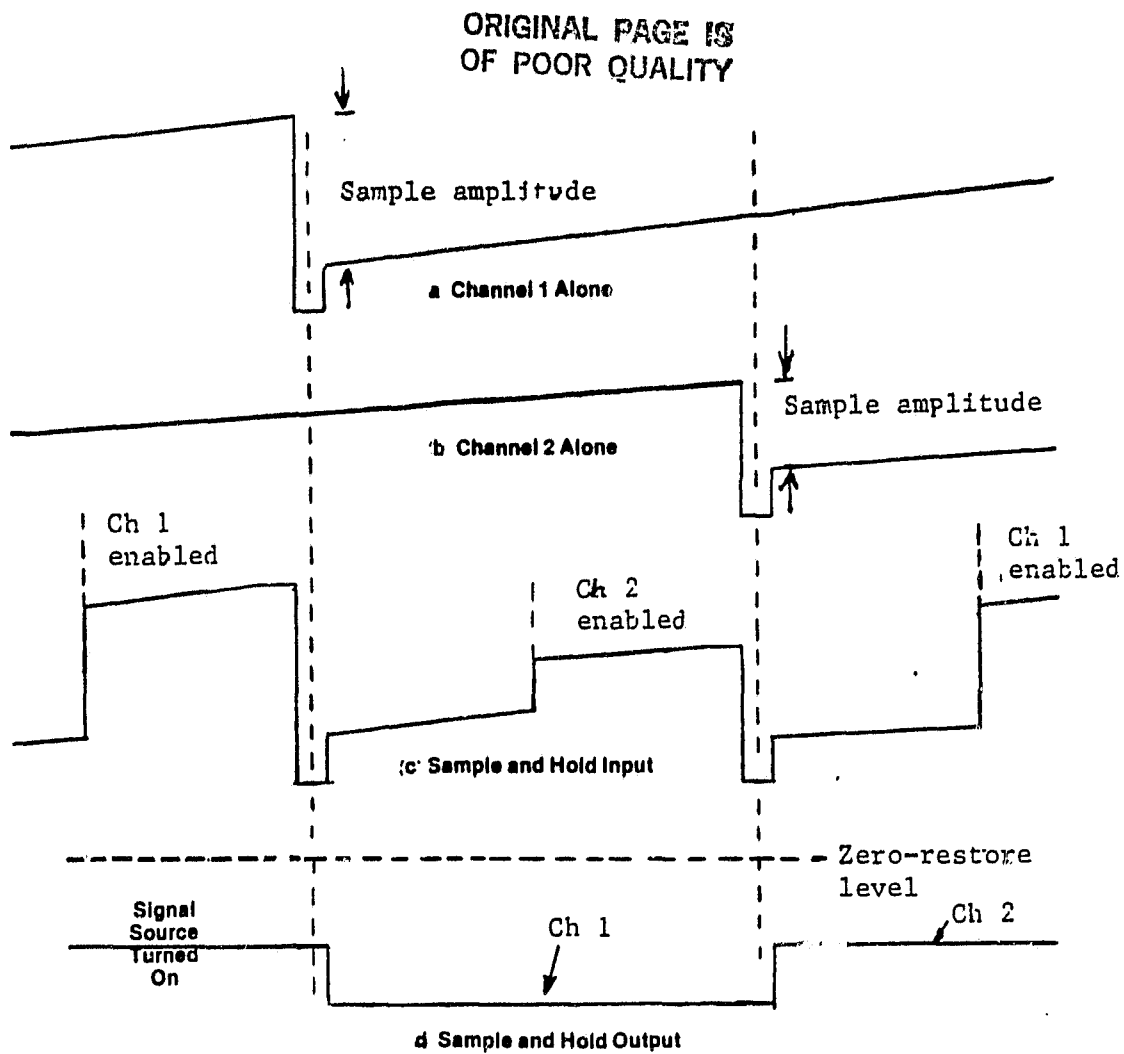
FIGURE 6   OUTPUT OF SSPC

13
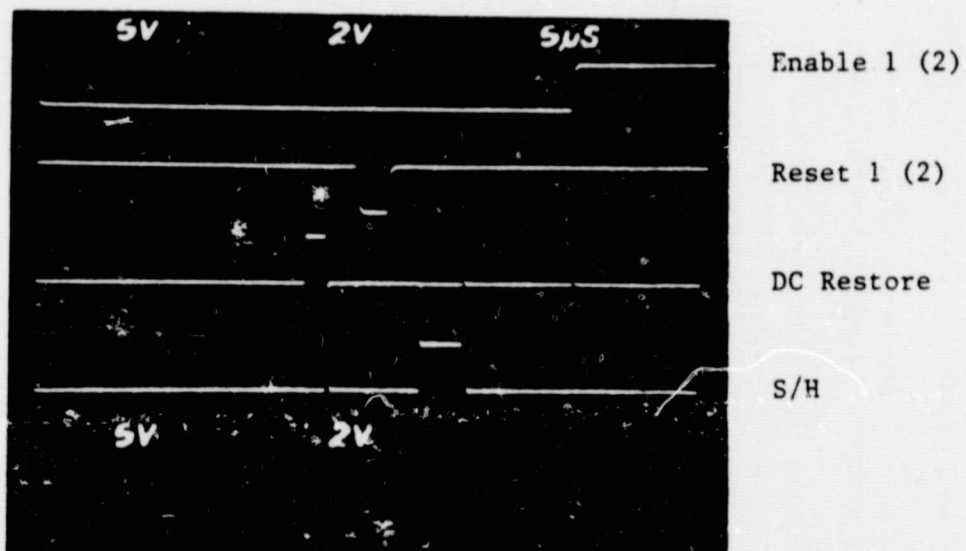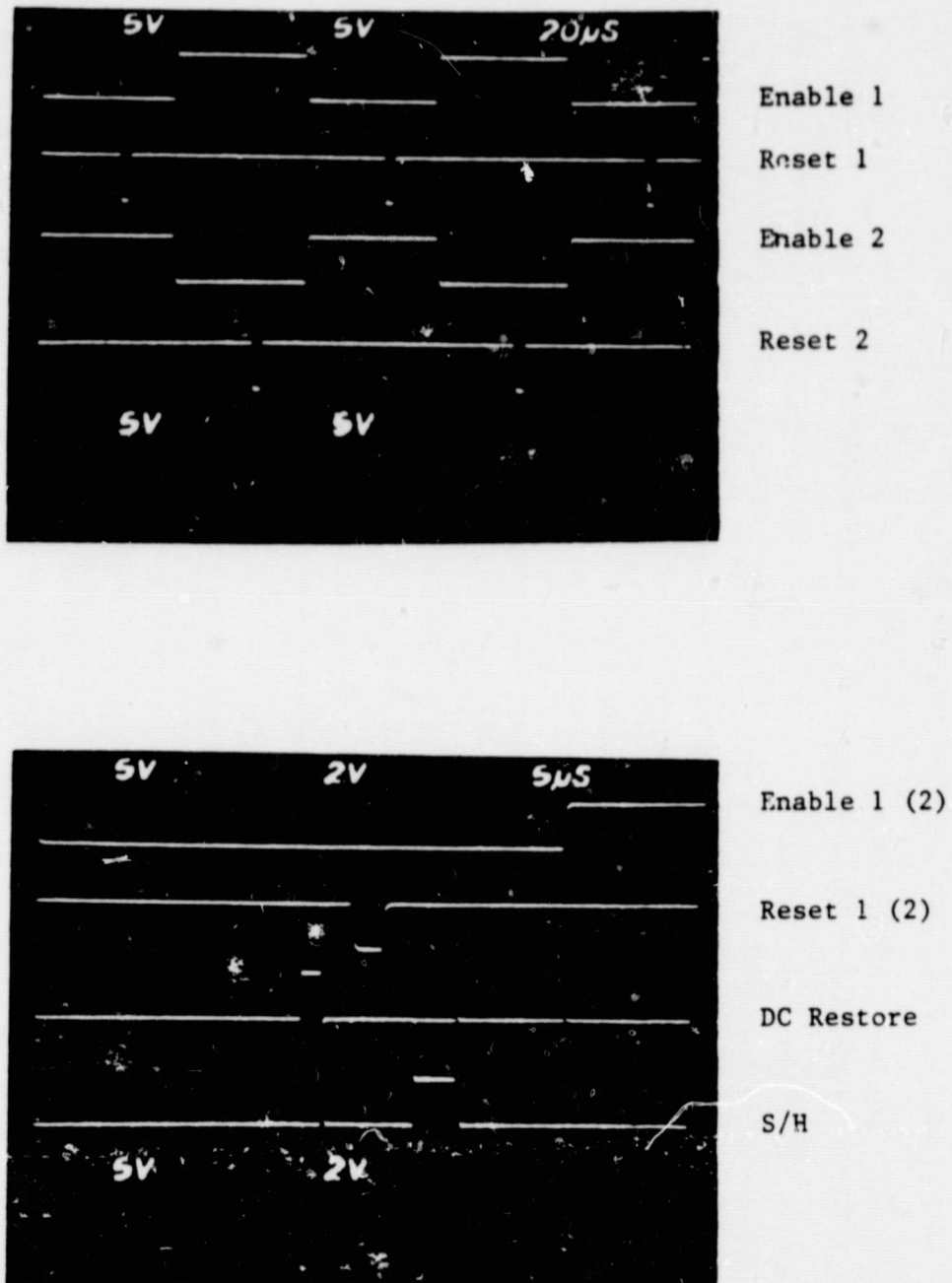
FIGURE 7   TIMING PULSES FOR SSPC MULTIPLEXING

(a) Individually
Operated
Channels

Reset Ch 1   Ch 2   Ch 1   Ch 2
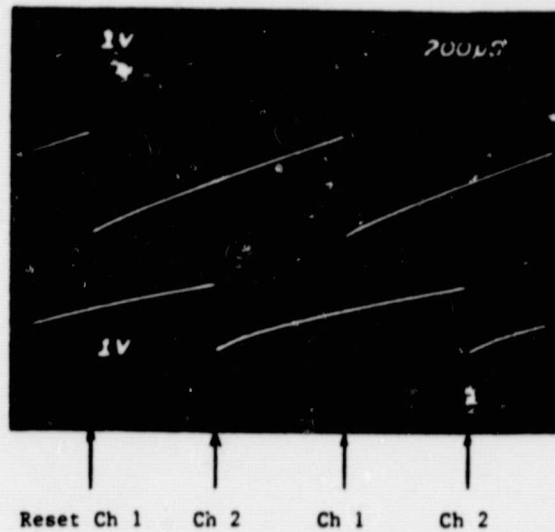
(b) Multiplexed
Mode in
the Dark
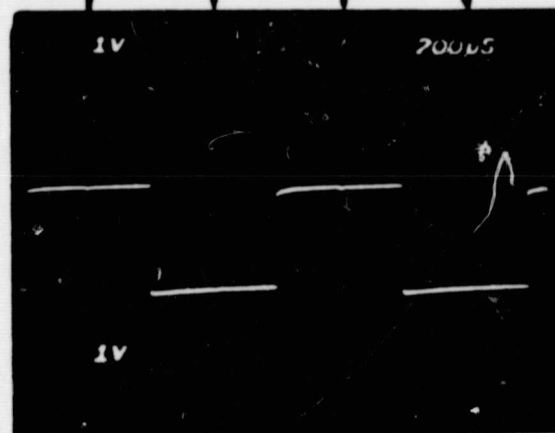
(c) Multiplexed
Mode with DC
Background

Signal 1

Signal 2

FIGURE 8   SOURCE OUTPUTS (PAR Gain = 10)

Reset Voltages	
Channel	V
1	0
2	0
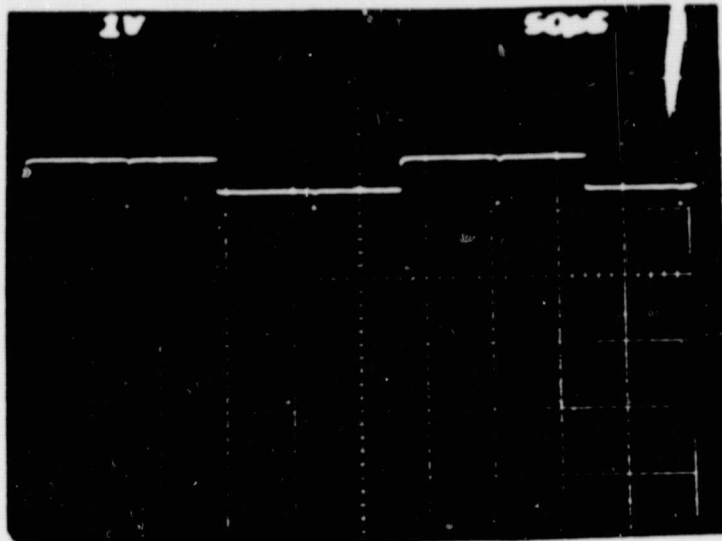
(a) Without DC Offset Adjustment

1	-0.65
2	0
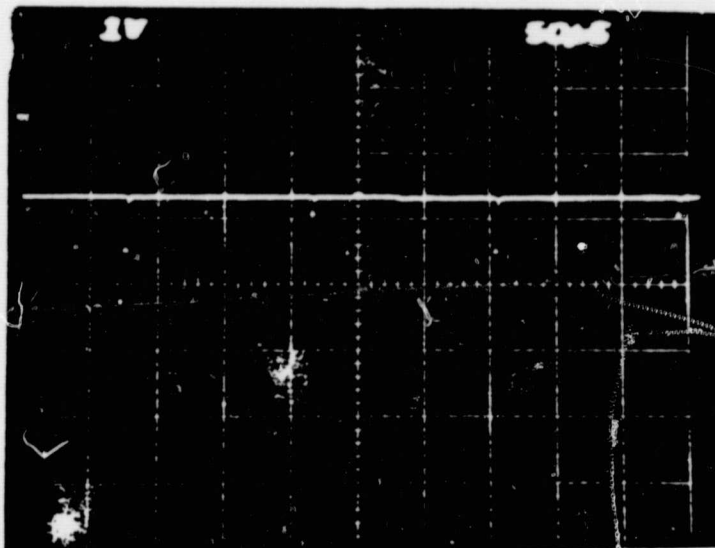
(b) With DC Offset Adjusted to Nearly Zero

FIGURE 9   SOURCE OUTPUT IN THE DARK
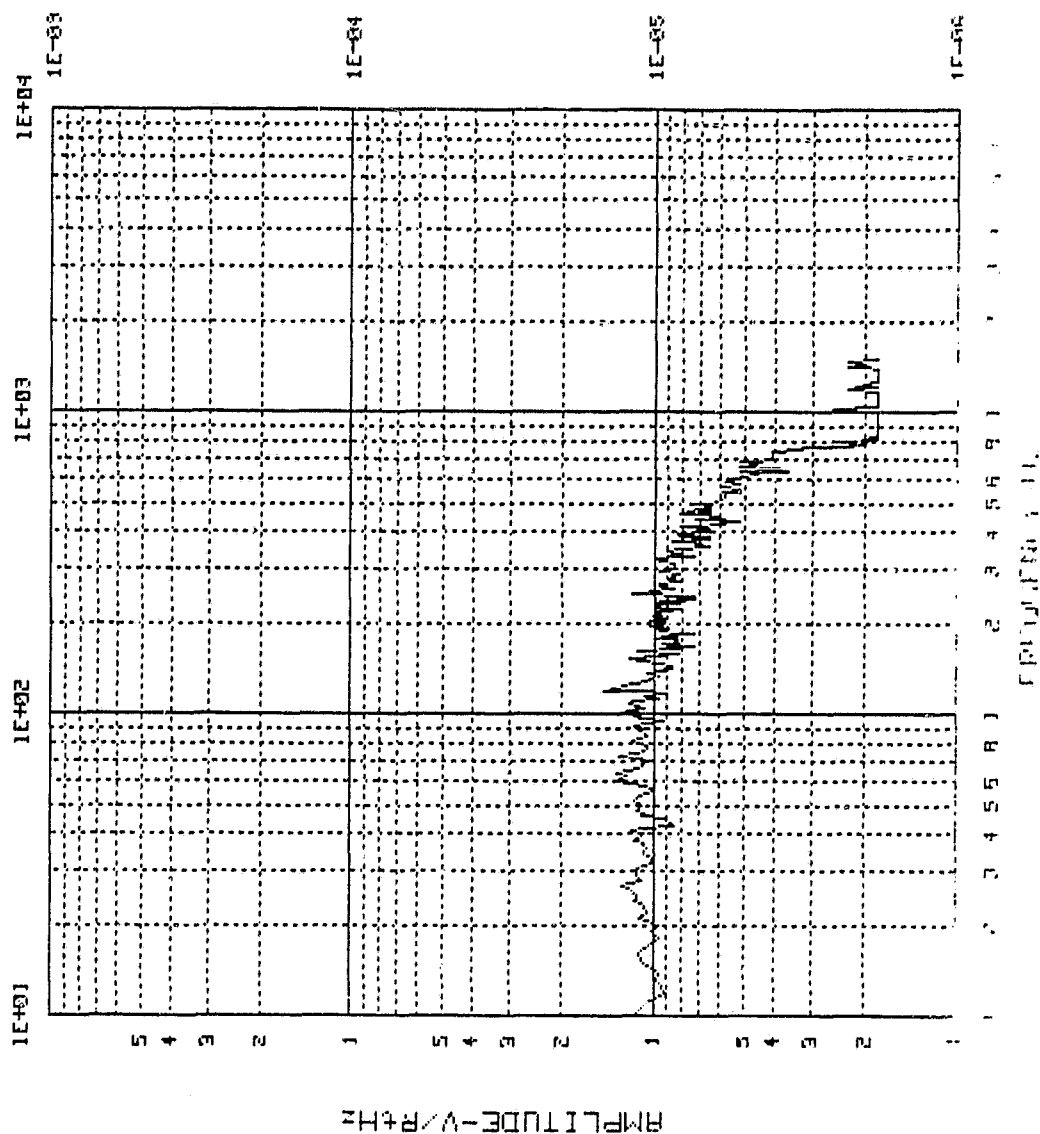
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FIGURE 10   DARK NOISE SPECTRUM OF CHANNEL 1 AT F_s = 1 kHz
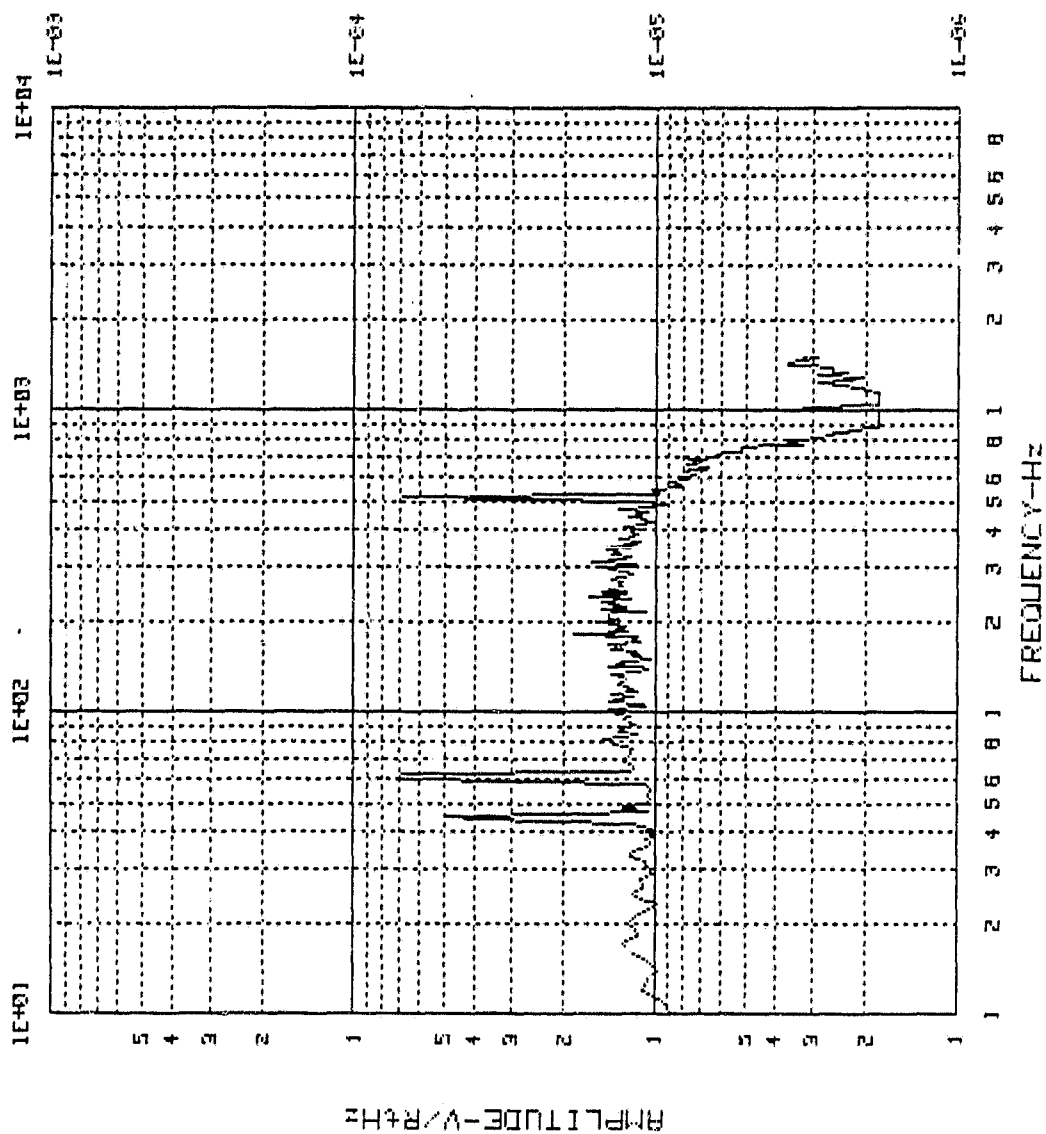
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FIGURE 11   DARK NOISE SPECTRUM OF CHANNEL 2 AT F_s = 1 kHz